IDESA

IDESA Advanced Tutorial Series

Analog Design in scaled technologies

Exercises

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Analog Design in ScalTech

Outline

- Transistor Behaviour
  - Experience 1- Coarse MOS parameter extraction
  - Experience 2- MOS behaviour worst case variation
  - Experience 3- Channel length modulation effects
  - Experience 4- Low-voltage current mirror design
  - Experience 5- V_{TH} dependence on MOS gate length (L)
  - Experience 6- V_{TH} dependence on MOS gate width (W)
  - Experience 7- Velocity saturation effects
- Circuit design
  - Experience 1- A Low-voltage bandgap
  - Experience 2- A two-stage opamp

Analog Design in ScalTech

Exercise Document Structure

- The exercise document will be organized in several "Experiences"
- In each Experience
  - The problem
    - The starting point and the target of the experience are clearly stated
    - The problem will address two main issues
    - Investigate the fundamental limitations
    - Develop a design procedure for achieving a given target
  - The solution
    - The circuit solution, the simulation set-up and the simulation results are given
  - Eventual comments for the professor
    - Useful points for the teacher to fruitfully drive the experience are indicated

Analog Design in ScalTech
Design environment

- Technology
  - ALL the exercises have been developed using a basic CMOS technology featuring 65nm minimum gate size
    - When a longer gate size is used
      - ➔ This is designed in the 65nm CMOS technology using non-minimum gate length

- Simulation environment
  - Environment: Cadence
  - Circuit simulator: SpectreRF

Transistor Behaviour - Experience 1

Coarse MOS parameter extraction

The problem

- Target:
  - Extract the basic parameters (k, V_{TH}, V_A) for the MOS behavior, assuming the following equation

$$I_D = k \cdot \left(\frac{W}{L}\right) \cdot \left(V_{GS} - V_{TH}\right)^2 \cdot \left(1 + \frac{V_{DS}}{V_A}\right)$$

    - Consider an NMOS device with W/L=10, and L=90nm.

  - Evaluate the error introduced by assuming the above equation and the effective transistor behavior, as given by the specific design-kit simulation environment

  - Repeat the same operation for a different value of L, to see the parameter dependence on the gate length

Transistor Behaviour - Experience 1

Coarse MOS parameter extraction

Comments

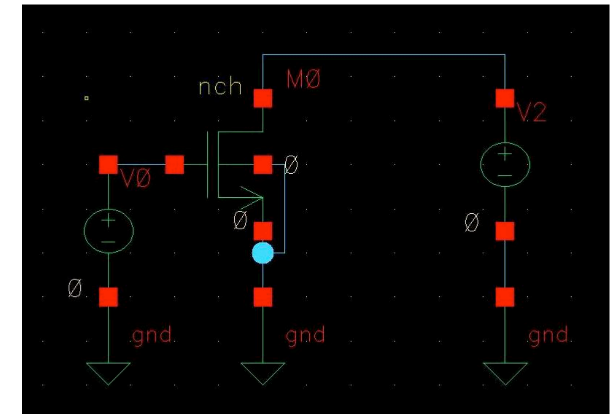
- At the beginning of designing in a given CMOS technology, it is important to have a coarse knowledge of the performance parameters of the available devices.
  - However, the effective behavior of the transistor is quite different from the quadratic law, in particular for scaled technologies
    - ➔ using the quadratic basic equation is quite inappropriate for accurate design
  - Their values are going to be used in a rough design, to be optimized by accurate and extensive simulations

Transistor Behaviour - Experience 1

Coarse MOS parameter extraction

The solution

- The circuit
  - Consider an NMOS device
    - A PMOS device should have to be considered as well
      - This is left to the student
  - Consider the device with a fixed ratio W/L=10
  - Choose L=90nm (and W=900nm)
    - Using non-minimum L avoids short channel effects



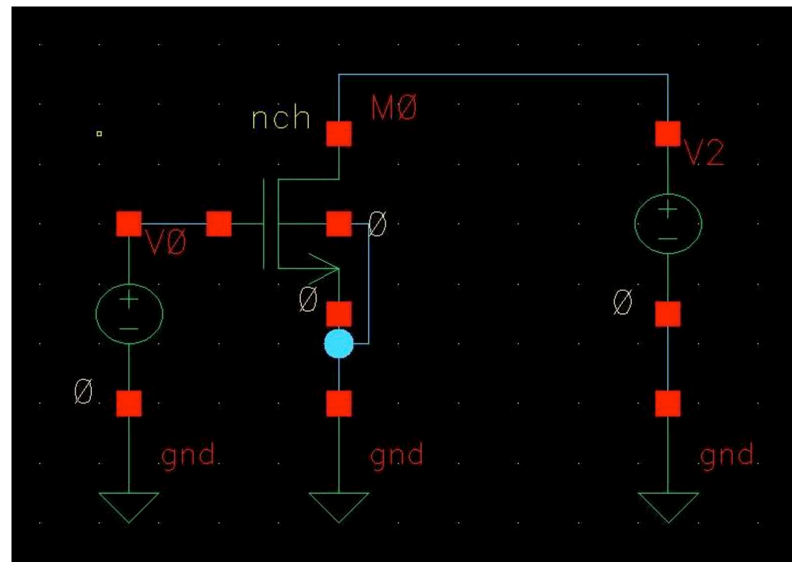
  - Connect V_D to V_{DD} = 1.2V
  - Connect V_G to bias voltages around 700mV (assuming V_{TH}<700mV)
    - ➔ the transistor is active ($V_{GS}>V_{TH}$, to be verified)
    - ➔ the transistor is in saturation ($V_{DS}>V_{GS}>V_{GS}-V_{TH}$)

Transistor Behaviour - Experience 1

Coarse MOS parameter extraction

The solution

- Simulation analysis
  - Fix V_{GS} = 700mV & V_{GS} = 730mV
    - For each value perform a DC analysis on V_{DS}
      - V_{DS} is moved from 0 to 700mV
- Plot the curves I_D-vs.-V_{DS} for the two cases



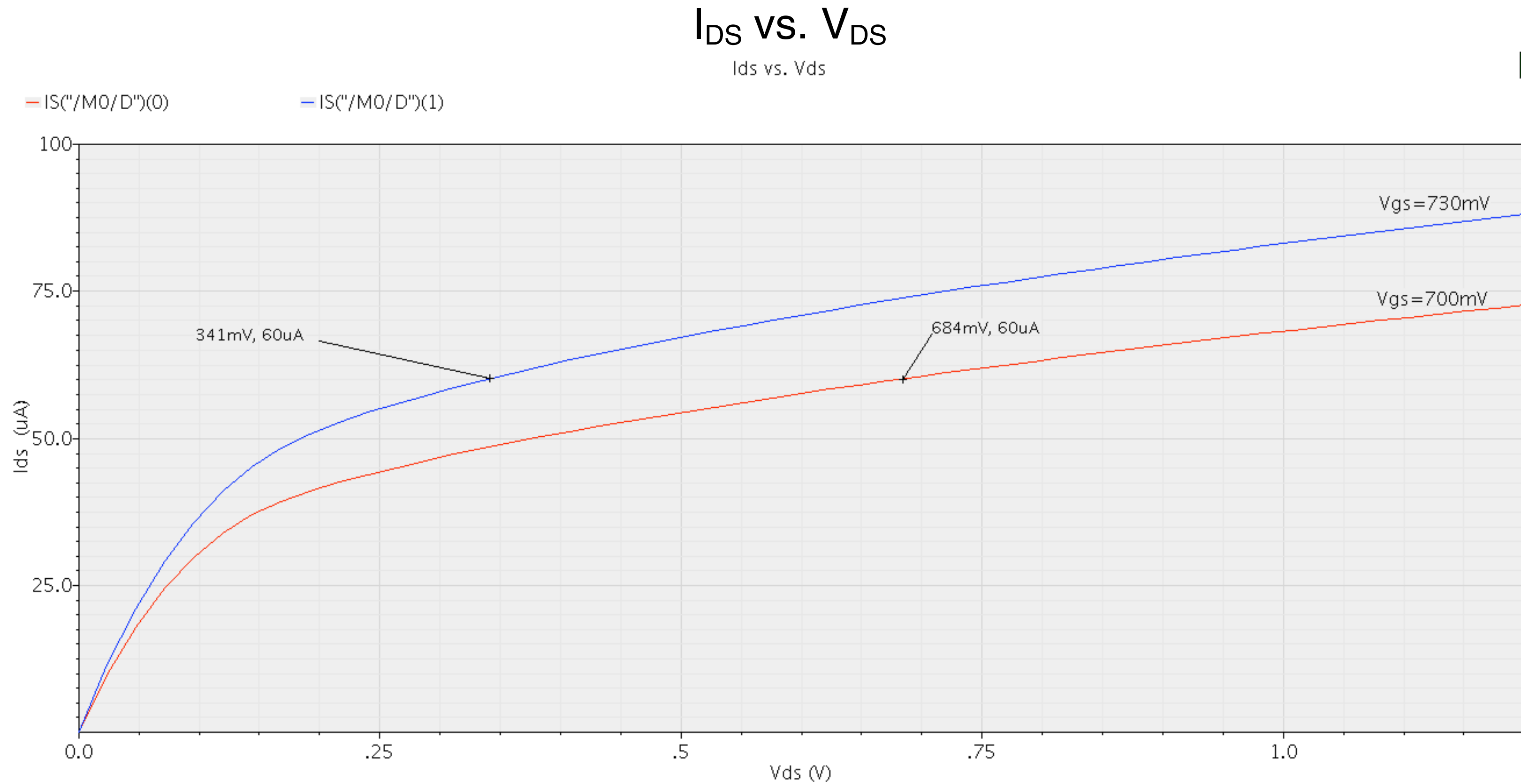
Transistor Behaviour - Experience 1

Coarse MOS parameter extraction

The solution

- Simulation results

I_{DS} vs. V_{DS}

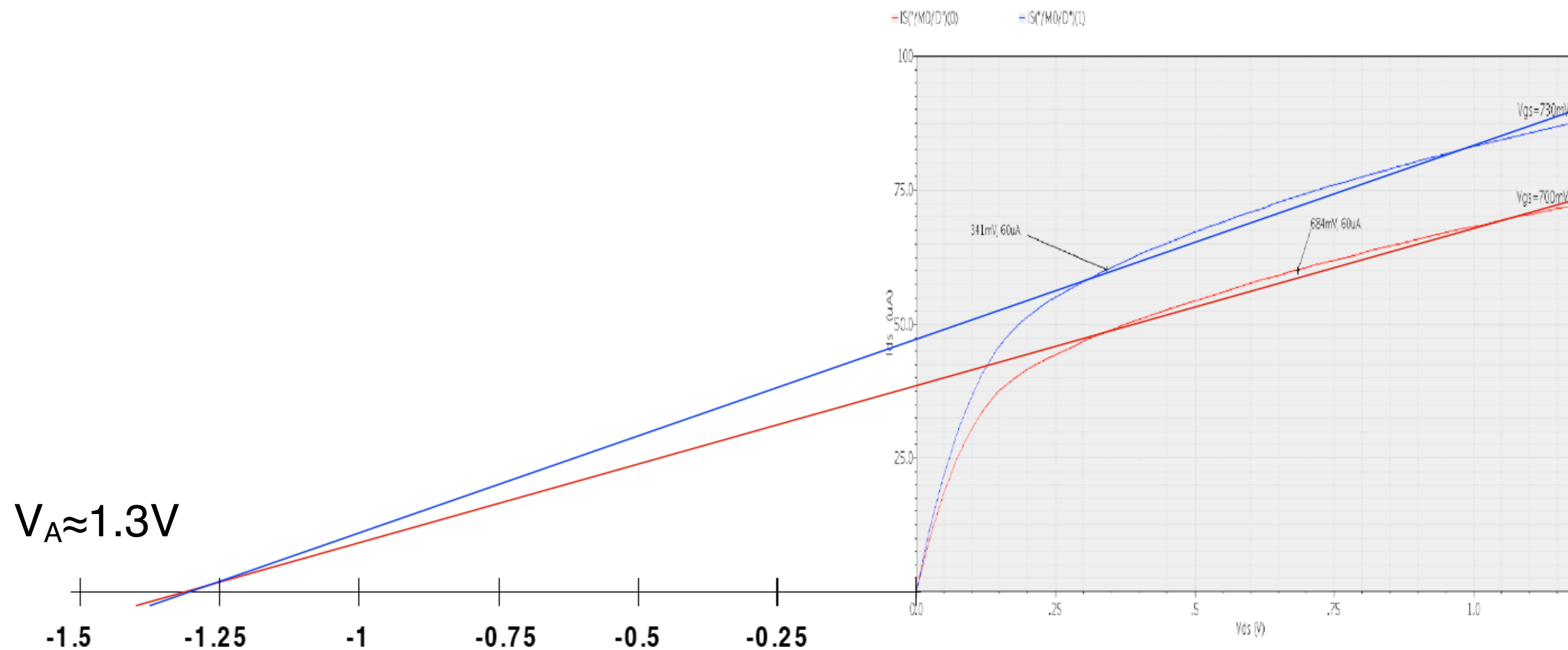


Transistor Behaviour - Experience 1

Coarse MOS parameter extraction

The solution

- Parameter extraction: Early voltage (V_A)
  - The V_A parameter is extracted by graphical extrapolation



- Notice: a very low value of V_A is obtained
  - This is the typical performance in scaled technologies

Transistor Behaviour - Experience 1

Coarse MOS parameter extraction

The solution

- Parameter extraction $\{k, V_{TH}\}$
  - Consider the basic equation

$$I_D = k \cdot \left(\frac{W}{L}\right) \cdot (V_{GS} - V_{TH})^2 \cdot \left(1 + \frac{V_{DS}}{V_A}\right)$$

  - Consider two points for L=90nm
    - $\{I_D, V_{DS}$, and $V_{GS}\}$ are known for each point

$$I_{D1} = k \cdot \left(\frac{W}{L}\right) \cdot (V_{GS1} - V_{TH})^2 \cdot \left(1 + \frac{V_{DS1}}{V_A}\right)$$

$$I_{D2} = k \cdot \left(\frac{W}{L}\right) \cdot (V_{GS2} - V_{TH})^2 \cdot \left(1 + \frac{V_{DS2}}{V_A}\right)$$

Transistor Behaviour - Experience 1

Coarse MOS parameter extraction

The solution

- Parameter extraction {k, V_{TH}}
  - Rationing the two equation (k·(W/L) is the same)

$$(V_{GS1} - V_{TH})^2 \cdot \left(1 + \frac{V_{DS1}}{V_A}\right) = (V_{GS2} - V_{TH})^2 \cdot \left(1 + \frac{V_{DS2}}{V_A}\right)$$

$$(V_{GS1} - V_{TH}) \cdot \alpha = (V_{GS2} - V_{TH})$$

$$\alpha = \sqrt{\left(1 + \frac{V_{DS1}}{V_A}\right) \Big/ \left(1 + \frac{V_{DS2}}{V_A}\right)}$$

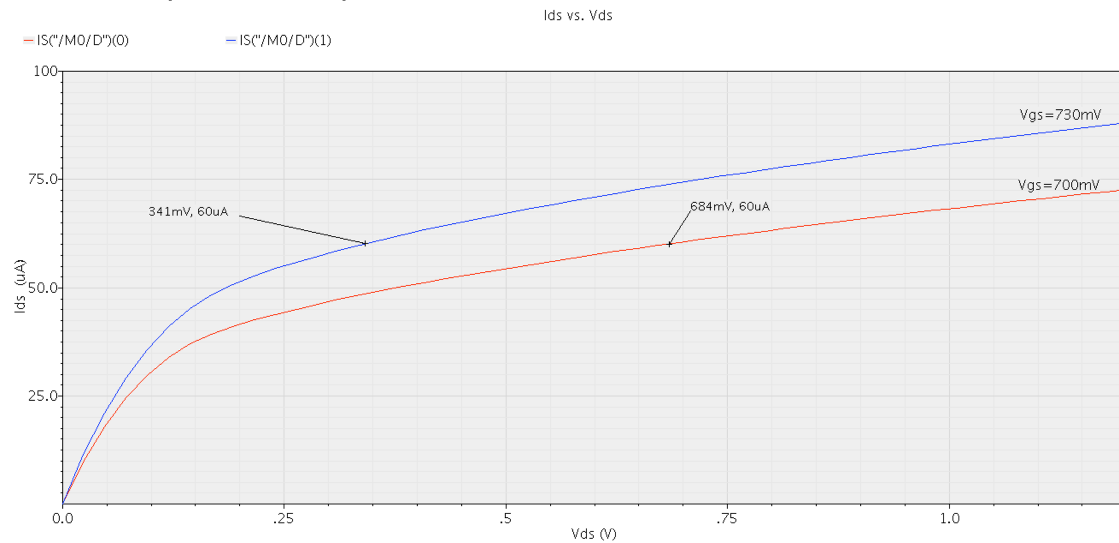
$$V_{TH} = \frac{(\alpha \cdot V_{GS1} - V_{GS2})}{(\alpha - 1)}$$

Transistor Behaviour - Experience 1

Coarse MOS parameter extraction

The solution

- From the simulation (L=90nm)



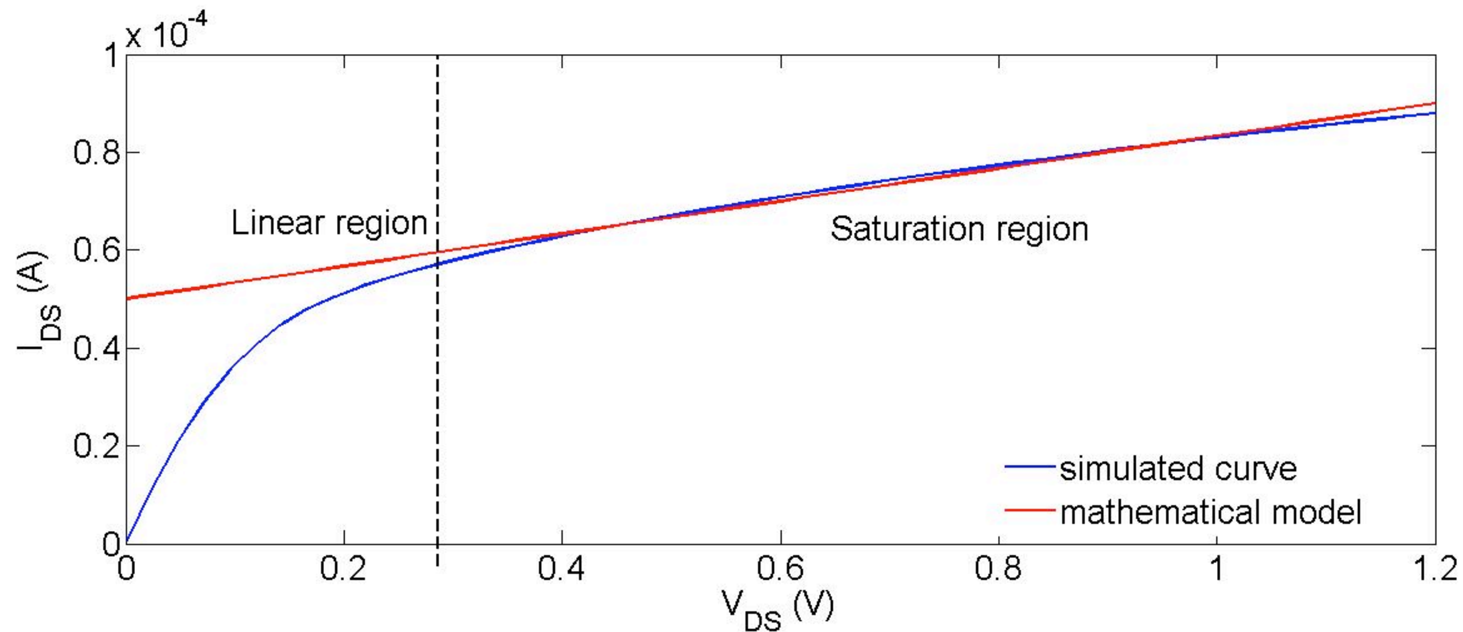
	I_D [μA]	V_{DS} [V]	V_{GS} [V]	V_A [V]
Point 1	60	0.341	0.730	1.300
Point 2	60	0.684	0.700	1.300
		α =	0.909	
		V_{TH} [V]=	0.399	
		k=	4.329E-05	

Transistor Behaviour - Experience 1

Coarse MOS parameter extraction

Comments

- The simple approximation so extracted is compared with the actual transistor behavior as given by the complete model
  - The two plots are compared for the case W/L=900nm/90nm in the saturation region

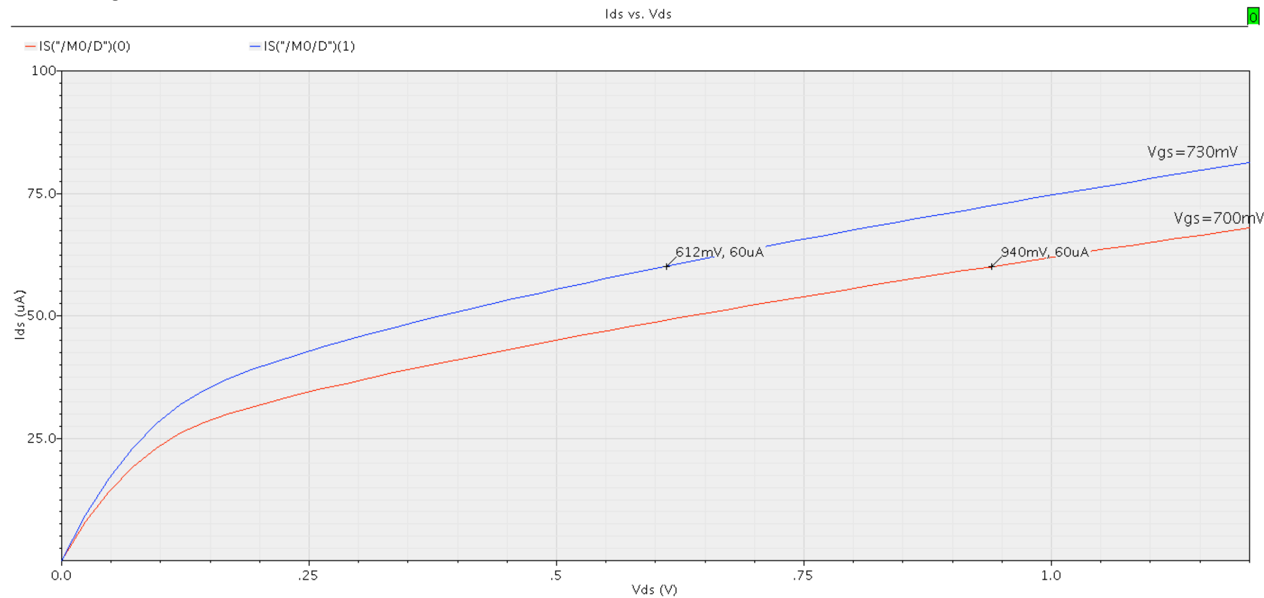


Transistor Behaviour - Experience 1

Coarse MOS parameter extraction

The solution

- The same analysis is carried out for L=65nm



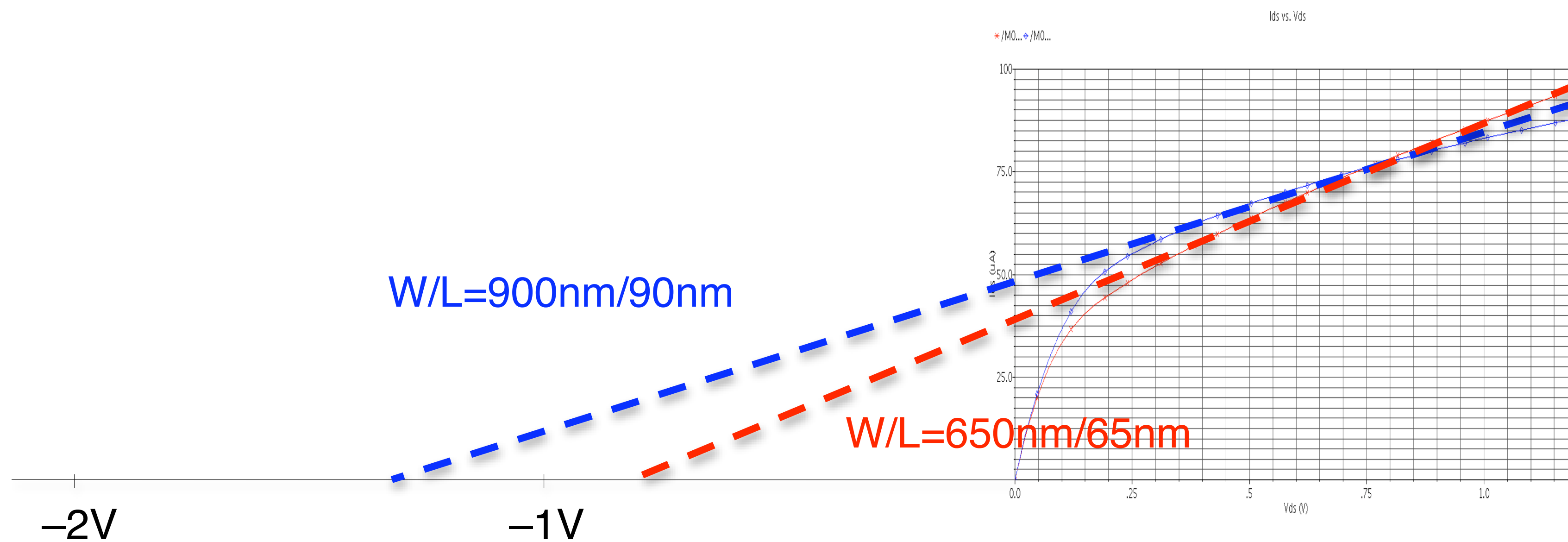
	I_D [μA]	V_{DS} [V]	V_{GS} [V]	V_A [V]
Point 1	60	0.612	0.730	0.850
Point 2	60	0.940	0.700	0.850
α =			0.904	
V_{TH} [V]=			0.418	
k=			3.591E-05	

Transistor Behaviour - Experience 1

Coarse MOS parameter extraction

Comments

- The two above evaluations show also the dependence of the Early voltage (V_A) on the transistor length (L)
- The curves I_{DS}-vs.-V_{DS} are here compared



Transistor Behaviour - Experience 2

MOS behaviour worst case variation

The problem

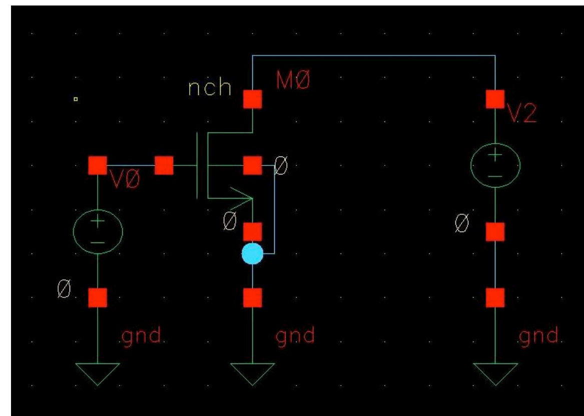
- Target:
  - For the previous design (W/L=900nm/90nm), evaluate the performance variation of the MOS in worst-case conditions, i.e.:
    - for technology worst cases
    - for temperature variations in the range [-40 °C to 120 °C]
- Evaluate the same performance variation for
  - a device with (W/L=1800nm/180nm)
  - a device with (W/L=650nm/65nm)

Transistor Behaviour - Experience 2

MOS behaviour worst case variation

The solution

- The circuit:
  - A W=900nm, L=90nm device is used



- The simulation:
  - Operating point (OP)
    - V_{GS}=730mV; V_{DS}=1.2V
  - Extract the device numbers from simulator output file

Transistor Behaviour - Experience 2

MOS behaviour worst case variation

The solution

- The following table is composed for:
  - L=90nm; V_{GS}=730mV; V_{DS}=1.2V

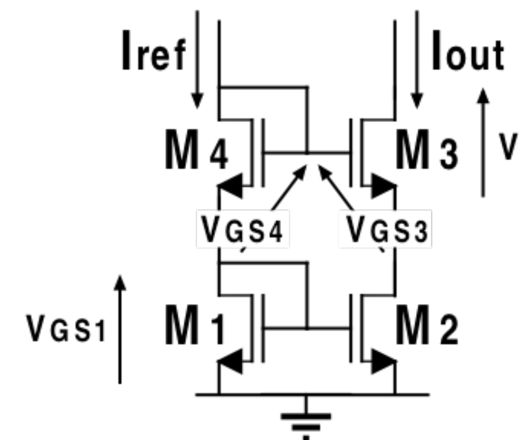
	Nominal			Fast			Slow		
	-40°C	27°C	120°C	-40°C	27°C	120°C	-40°C	27°C	120°C
I (μA)	79.69	87.63	95.78	129.5	133.5	137.4	46.38	56.34	66.87
V_{TH} (mV)	581	540	484	527	486	430	631	590	533
g_{ds} (μA/V)	24.2	24.8	25.6	34.7	34.6	34.5	15.6	17.0	18.6
g_m (μA/V)	633	560	492	784	680	580	47V	444	409
g_m/g_{ds}	26.2	22.6	19.2	22.6	19.6	16.8	30.4	26.1	22.0

Transistor Behaviour - Experience 2

MOS behaviour worst case variation

Comments

- About V_{TH}
  - V_{TH} changes in the range [430mV – 630mV] ➔ A very large V_{TH} variation
    - These variations have to be considered in conjunction with the available supply voltage of 1.2V.
    - Even in the same worst case (i.e. for a given technology case – fast, nominal or slow) the variation is in the range of about 100mV
    - A robust design needs to take into account these spreads
  - Example 1: in a basic current-mirror the minimum V_{GS} depends on V_{TH}
    - ➔ it can significantly change
  - Example 2: a cascode current mirror requires for the two cascode diodes at least $2 \cdot V_{GS} > 2 \cdot V_{TH} \geq 1.2V$ in the worst case
    - ➔ A cascode current mirror cannot be used in a safe design



Transistor Behaviour - Experience 2

MOS behaviour worst case variation

Comments

- About g_{ds} & g_m
  - Their variations are within ±30% w.r.t. nominal values
    - This is typically accepted in IC realization

- About intrinsic gain (g_m / g_{ds})
  - This can change a lot with a large relative variation
    - To be considered in the opamp design

Transistor Behaviour - Experience 2

MOS behaviour worst case variation

The solution

- The same analysis is carried out for other two transistor L sizes (W/L is constant)
  - L=65nm; V_{GS}=730mV; V_{DS}=1.2V

	Nominal			Fast			Slow		
	-40°C	27°C	120°C	-40°C	27°C	120°C	-40°C	27°C	120°C
V_{TH} [mV]	584	547	496	510	475	425	646	606	552
g_{ds} [μA/V]	34.4	34.1	34.1	50.9	49.2	47.4	19.6	21.0	22.5
g_m [μA/V]	548	486	432	667	583	505	392	370	348
g_m/g_{ds}	15.9	14.3	12.7	13.1	11.8	10.6	20	17.6	15.5

  - L=180nm;V_{GS}=730mV; V_{DS}=1.2V

	Nominal			Fast			Slow		
	-40°C	27°C	120°C	-40°C	27°C	120°C	-40°C	27°C	120°C
V_{TH} [mV]	565	522	462	523	480	421	605	562	503
g_{ds} [μA/V]	12.3	12.9	13.4	16.5	16.7	16.9	8.8	9.6	10.6
g_m [μA/V]	754	660	564	930	786	651	580	533	480
g_m/g_{ds}	61.3	51.2	42.1	56.4	47.1	38.5	65.9	55.5	45.3

- For L = 65nm ➔ the intrinsic gain g_m/g_{ds} is lower
- For L = 180nm ➔ the V_{TH} is slightly lower

Transistor Behaviour - Experience 3

Channel length modulation effects

The problem

- Target:
  - Design a transistor in saturation region with:

    $V_{DS} \approx 0.3V$

    $I = 10\mu A$

    $r_o > 250k\Omega$

  - Verify the r_o dependence on the current level

Comment

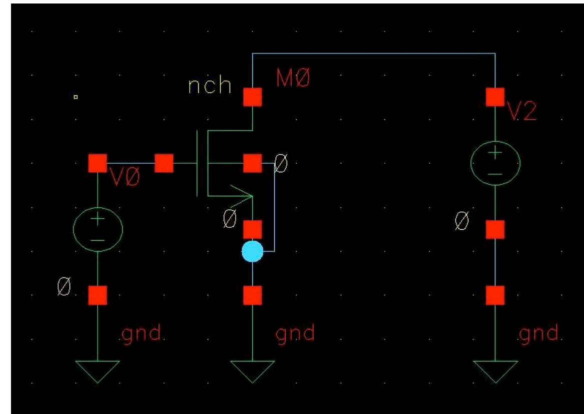
- This is the transistor in the output stage of an opamp with rail-to-rail output swing
  - The output node is biased with $V_{DS} \leq V_{DD}/2 = 0.6V$

Transistor Behaviour - Experience 3

Channel length modulation effects

The solution

- The scheme



- The simulation
  - Use an .OP (operating point) analysis
  - With $V_{DS} \geq 0.3V$ ➔a safe condition is using $V_{GS} - V_{TH} \approx 0.2V$
    - This respects the requirements for saturation region, i.e. $(V_{DS} > V_{ov})$
  - With I & V_{ov}➔ the (W/L) ratio (neglecting V_A effect)
    - $k = 43.6\mu A/V^2$

$$\left(\frac{W}{L}\right) = \frac{I_D}{k \cdot (V_{GS} - V_{TH})^2}$$

Transistor Behaviour - Experience 3

Channel length modulation effects

The solution

- Device size design
  - Assuming L=90nm ➔

$$\left(\frac{W}{L}\right) = \frac{I_D}{k \cdot (V_{GS} - V_{TH})^2} = 3$$

  - Assuming L=90nm ➔ W=270nm
    - ➔ The output impedance from simulation results

$$r_o > 160k\Omega$$

- In order to respect the requirement (r_o>20kΩ)
  - ➔ the L is increased until the requirement is satisfied
    - W is accordingly increased in order to maintain the above (W/L) ratio

Transistor Behaviour - Experience 3

Channel length modulation effects

The solution

- By consecutive simulation the L values is extracted

L=90nm → g_{ds} =6.28 μA/V → r_o =159kΩ
L=100nm → g_{ds} =5.68 μA/V → r_o =176kΩ
L=110nm → g_{ds} =5.18μA/V → r_o =193kΩ
L=120nm → g_{ds} =4.83μA/V → r_o =207kΩ
L=130nm → g_{ds} =4.53μA/V → r_o =221kΩ
L=140nm → g_{ds} =4.27μA/V → r_o =234kΩ
L=150nm → g_{ds} =4.05μA/V → r_o =247kΩ
L=160nm → g_{ds} =3.87μA/V → r_o =258kΩ
L=170nm → g_{ds} =3.70μA/V → r_o =270kΩ
L=180nm → g_{ds} =3.56 μA/V → r_o =281kΩ
L=190nm → g_{ds} =3.43μA/V → r_o =292kΩ
L=200nm → g_{ds} =3.32μA/V → r_o =301kΩ

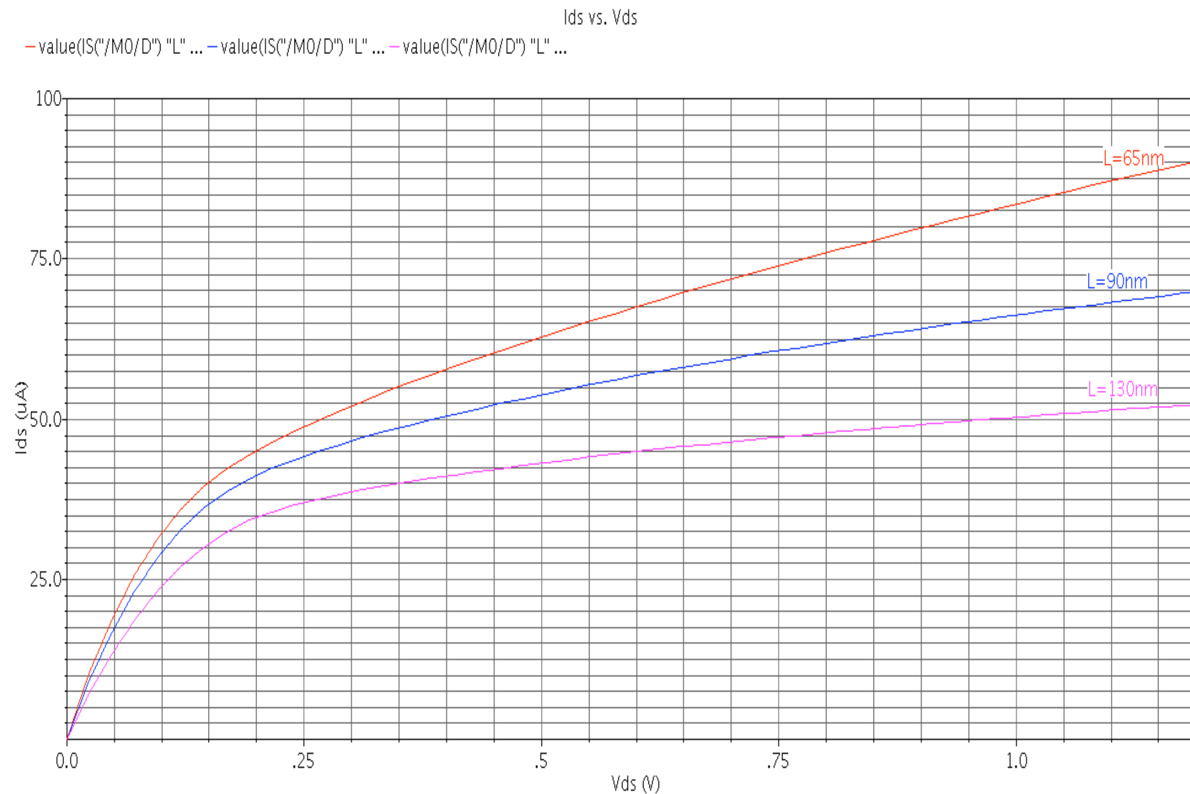
- The target value r_o>250kΩ requires L> 160nm

Transistor Behaviour - Experience 3

Channel length modulation effects

The solution

- The output characteristic (I_{DS}-V_{DS}) of the MOS transistor is plotted for different L value, while maintaining the same W/L ratio (=10)



L=65nm

L=90nm

L=130nm

Transistor Behaviour - Experience 3

Channel length modulation effects

The solution

- The inverse of derivative of (I_{DS}-vs.-V_{DS}) is the output impedance ($r_o=(\partial I_{DS}/\partial V_{DS})^{-1}$)

Ro vs. Vds

L="65n";... L="90n";... L="130n...

Ro (E3): 25.0, 50.0, 75.0, 100

Vds (): 0.0, .25, .5, .75, 1.0

L=130nm

L=90nm

L=65nm

Linear Region

Low r_o

Saturation Region

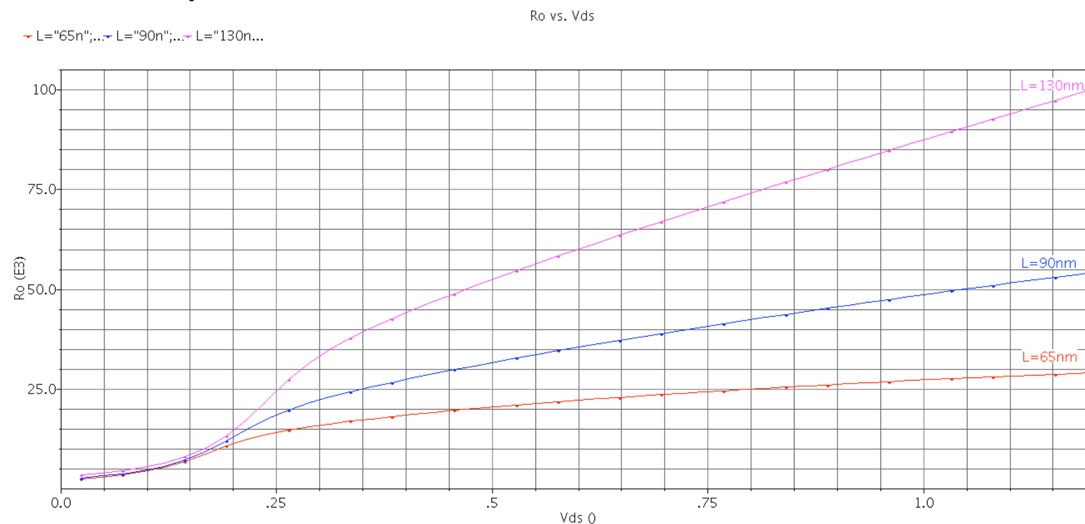
High r_o

Transistor Behaviour - Experience 3

Channel length modulation effects

Design issues

- The above simulation allows to evaluate the minimum L for a given target output impedance (i.e. λ)
- Design example
  - Target value r_o=10kΩ @ I_D = 100μA
  - From the I_{DS}-vs.-V_{DS} plot, and from the r_o plot
    - ➔ L_{min} = 0.18μm



- Notice that for certain L values there is a maximum r_o

Transistor Behaviour - Experience 3

Channel length modulation effects

Comments

- Note that the basic MOS quadratic law relationship does not include this effect
  - Assuming a I_D-vs.-V_{DS} equation as:

$$I_D = \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \cdot (1 + \lambda \cdot V_{DS})$$

  - There would not be I_D variation for different L value (while maintaining the same W/L ratio)
  - An I_D-vs.-V_{DS} variation for different L values is possible only considering

$$\lambda = \frac{\lambda^{l}}{L}$$

- Note that at very low V_{DS} values, output impedance value is very small
  - This is due to the fact that for (V_{DS}<V_{GS}-V_{TH}) the MOS operates in linear region,
    - ➔ i.e. like a small resistor

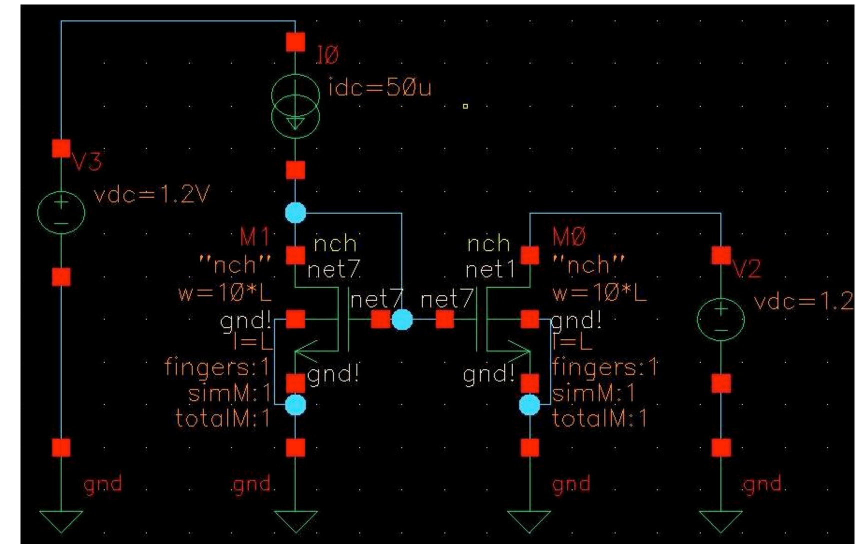
Transistor Behaviour - Experience 3

Channel length modulation effects

Solution - r_o vs. Current level

- The same analysis can be done changing I_D
  - Maintaining W/L
  - Maintaining V_{DS}
  - Moving V_{GS} from 300mV (<V_{TH}) to 1.2V (=V_{DD})

- The simulation scheme is:



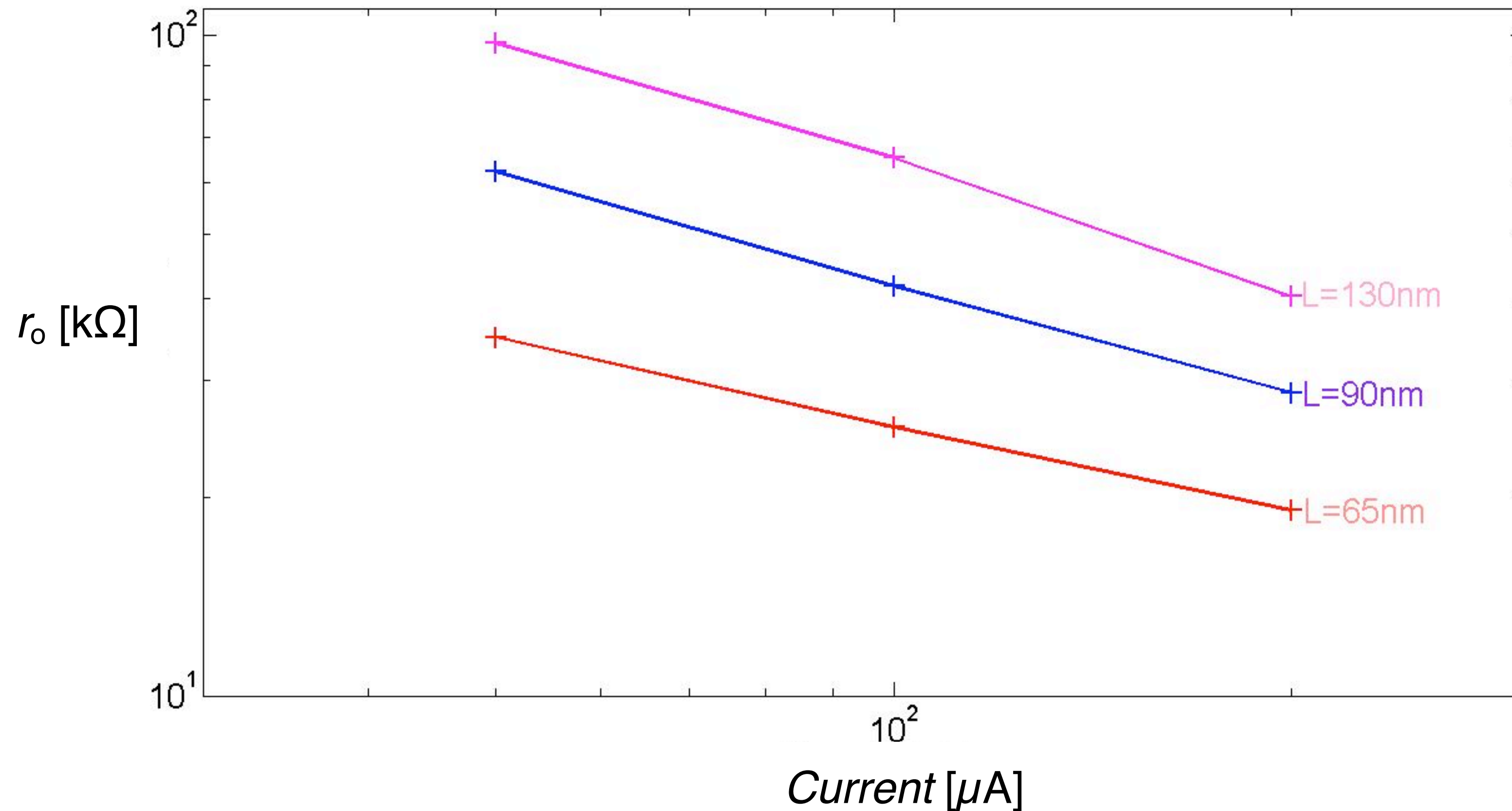
- V_G is biased at a fixed voltage
- I_D is changed for different bias conditions
  - An AC signal is superimposed to V_{DD}
    - The AC signal current from V_{DD} is monitored
      - r_o is calculated as a function of I_o

Transistor Behaviour - Experience 3

Channel length modulation effects

Solution - r_o vs. Current level

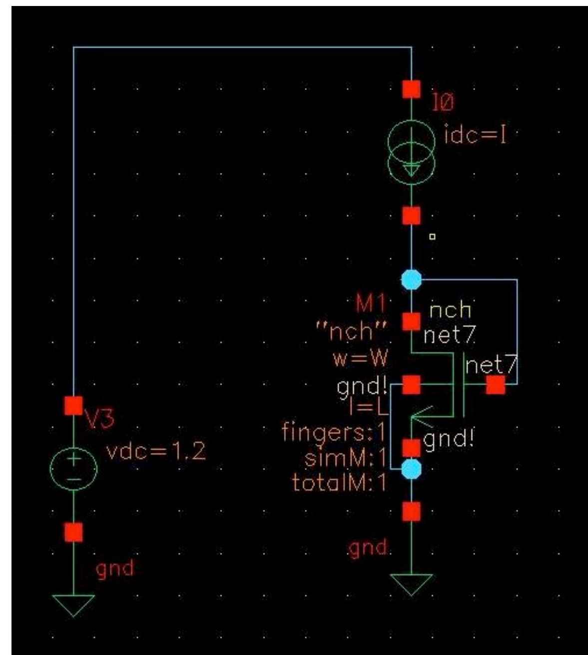
- Simulation results



Transistor Behaviour - Experience 3

V_{ov} vs. V_{DS}

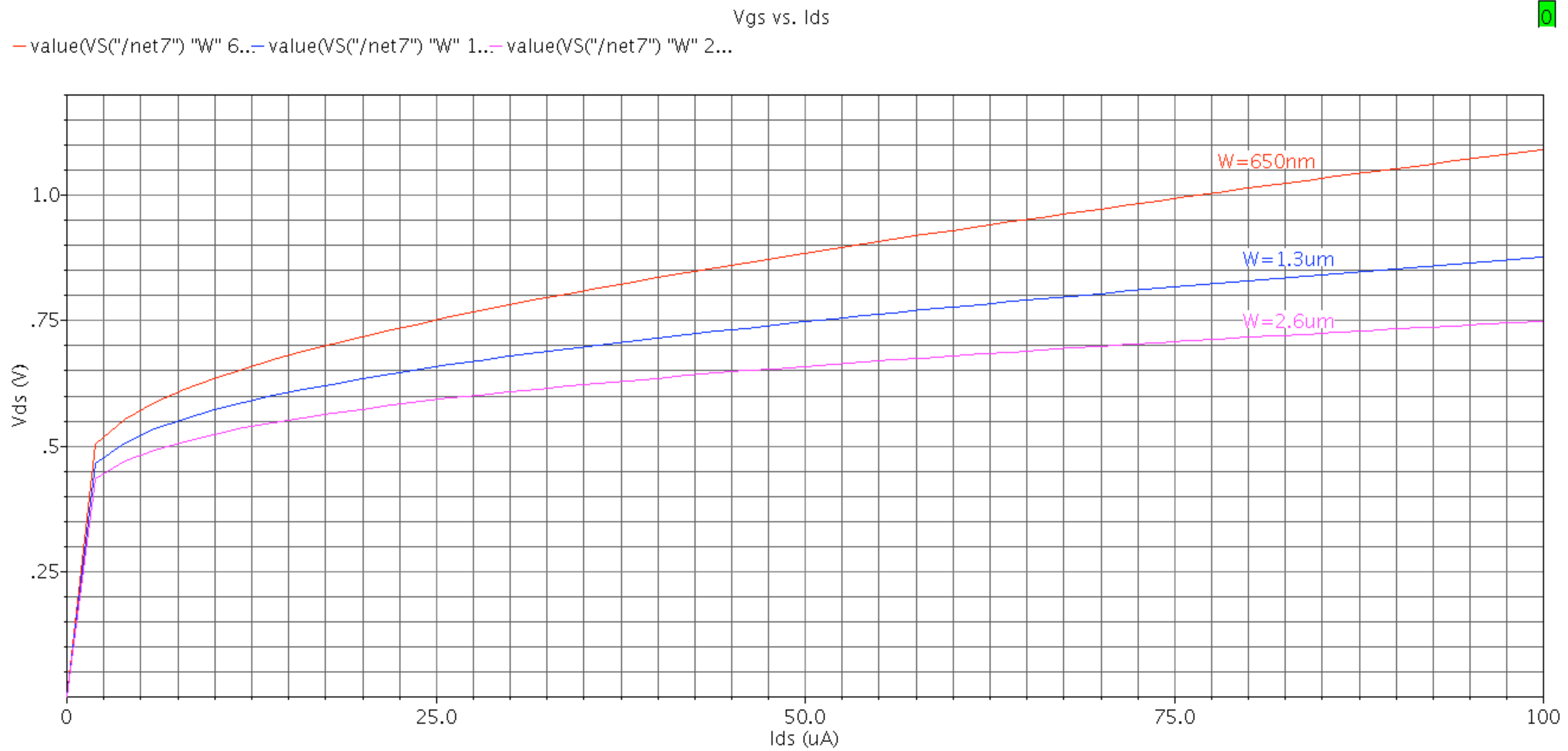
- Effect on the MOS sizing on the saturation voltage V_{DSat}
  - The circuit



  - The simulation
    - A DC analysis
      - sweeping I_{DS}
        - ➔ monitoring $V_{DS} = V_{GS}$

Transistor Behaviour - Experience 3

V_{ov} vs. V_{DS}



- L = 300nm
  W=650nm → W=1300nm → W=2600nm

Transistor Behaviour - Experience 4

Low-voltage current mirror design

The problem

- Design a simple current mirror for:

$$I_{out} = 50\mu A$$
$$V_{out} \text{ down to } 350mV$$

- Minimize output device area

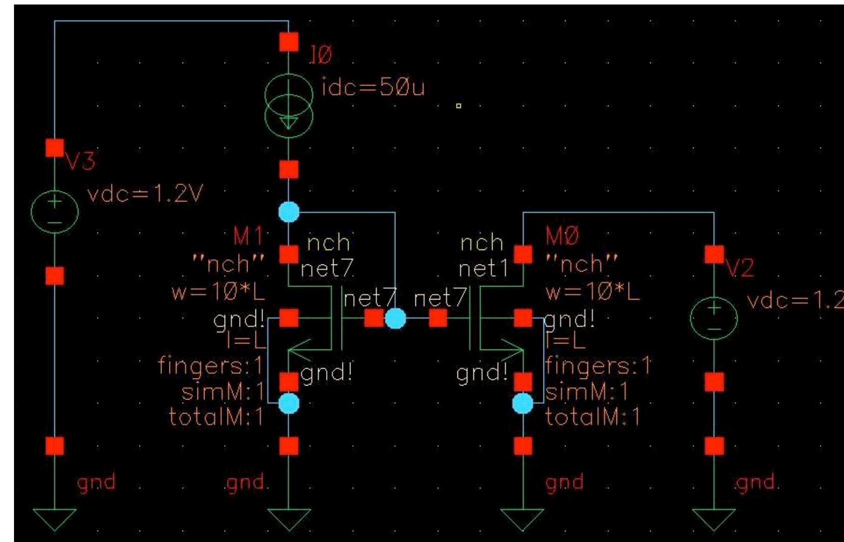
- Verify the circuit behavior for the different worst case & temperature conditions

Transistor Behaviour - Experience 4

Low-voltage current mirror design

The solution

- The circuit



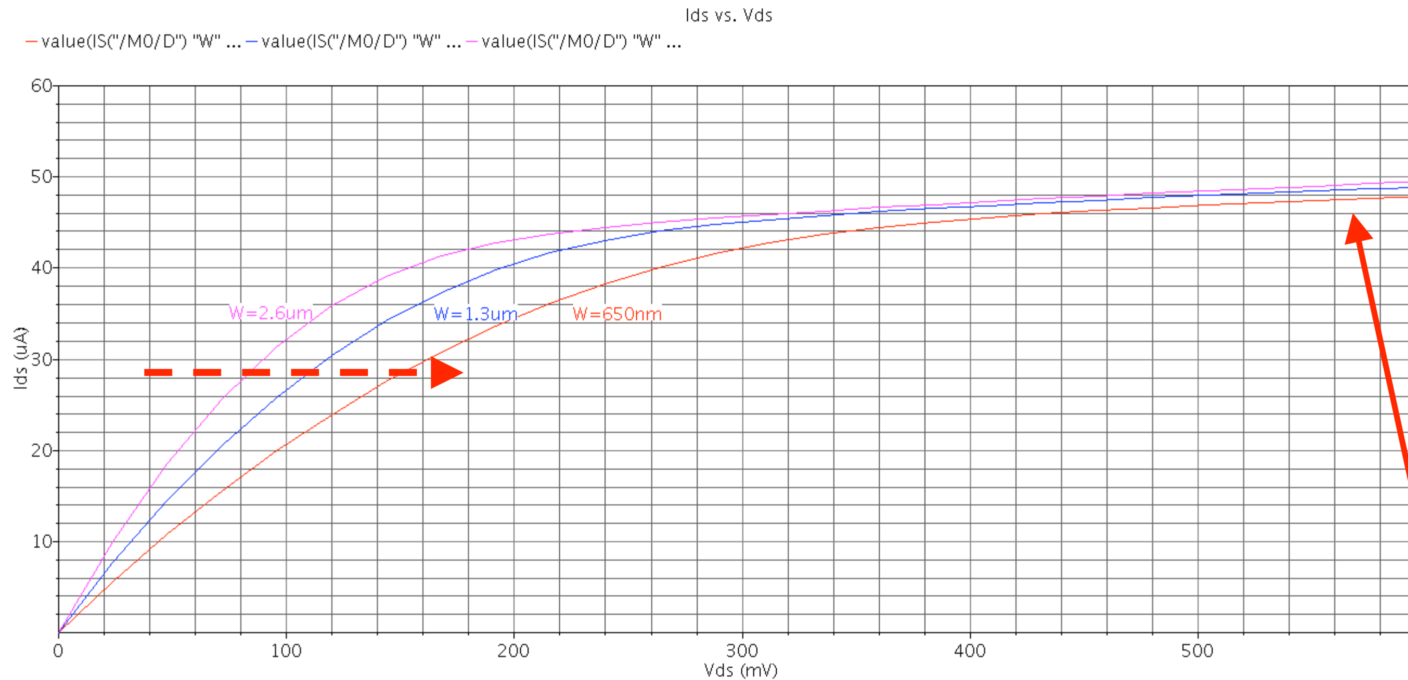
- A 50µA current is pushed in the reading transistor (M1)
- Both transistors of the mirror are sized with the same W&L (W/L=1.3um/300nm) in order to have V_{GS}=730mV
- The V_{DS} of the output transistor (M0) is changed in the [0V - 1.2V] range with a DC analysis

Transistor Behaviour - Experience 4

Low-voltage current mirror design

The solution

- Plot I_{DS}-V_{DS} curves with constant current I, while varying W/L



W=2.6um
L=300nm

W=1.3um
L=300nm

W=650nm
L=300nm

- By keeping I_{ds} constant and the same sizes for both the transistors of the mirrors,
  If W/L decreases
  ➔ V_{ov} and V_{DSat} increase and viceversa

Transistor Behaviour - Experience 4

Low-voltage current mirror design

Comment

- For the target current I=50µA
- Increasing W/L, with the same L=300nm
  - ➔ Reduces V_{ov}
    - ➔ Reduces V_{DSsat}

      W/L=650nm/300nm ➔ $V_{GS}–V_{TH}$ = 386mV

      W/L=1300nm/300nm ➔ $V_{GS}–V_{TH}$ = 242mV

      W/L=2600nm/300nm ➔ $V_{GS}–V_{TH}$ = 150mV
  - Increases the output capacitance C_D (capacacance on the drain)

    W/L=650nm/300nm ➔ C_D=0.4fF

    W/L=1300nm/300nm ➔ C_D=0.8fF

    W/L=2600nm/300nm ➔ C_D =1.5fF
- The capacitance C_D has been evaluated through the small signal analysis.
  - The C_D small signal parameter calculated by simulator corresponds to the overall capacitance on the drain of the MOS.
    - It is referred to ground

Transistor Behaviour - Experience 5

V_{TH} dependence on MOS gate length (L)

The problem

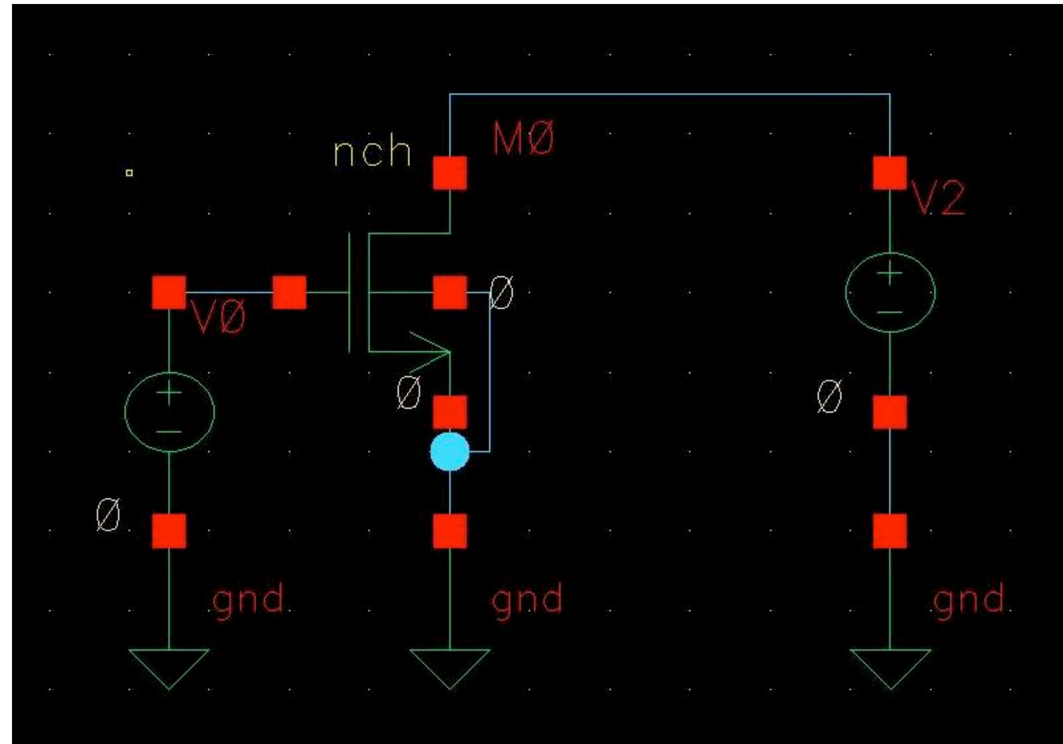
- Design the W length of a MOS device (Example W=1µm)
  - Fix L=65nm
  - Bias the MOS with V_{GS}=0.5V & V_{DS} = 1V
    - Extract V_{TH} from the operating point indicated in the simulator output file
  - Repeat the simulation for
    - L=[75nm 90nm 110nm 130nm 180nm 250 nm 350nm 500nm 1µm]
  - Plot V_{TH} vs. L

Transistor Behaviour - Experience 5

V_{TH} dependence on MOSgate length (L)

The solution

- The circuit

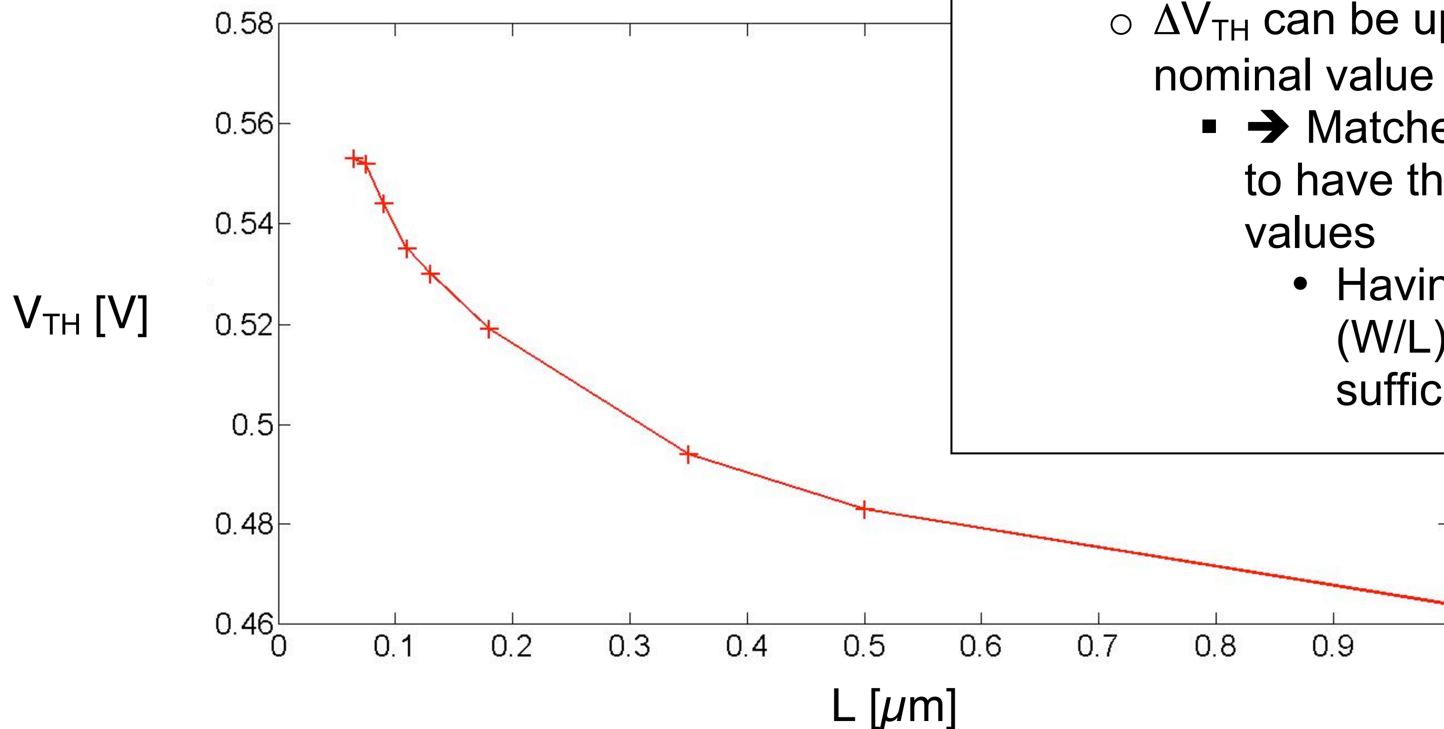


Transistor Behaviour - Experience 5

V_{TH} dependence on MOS gate length (L)

The solution

- The simulation
  - Use a DC simulation for different L values
  - Extract V_{TH} from the simulator output file
    - Plot V_{TH}-.vs.-L



- V_{TH} changes for different L values
  - ΔV_{TH} can be up to 80mV for a nominal value of 550mV
    - ➔ Matched devices need to have the same W&L values
      - Having the same (W/L) ratio is not sufficient

Transistor Behaviour - Experience 5

V_{TH} dependence on MOS gate length (L)

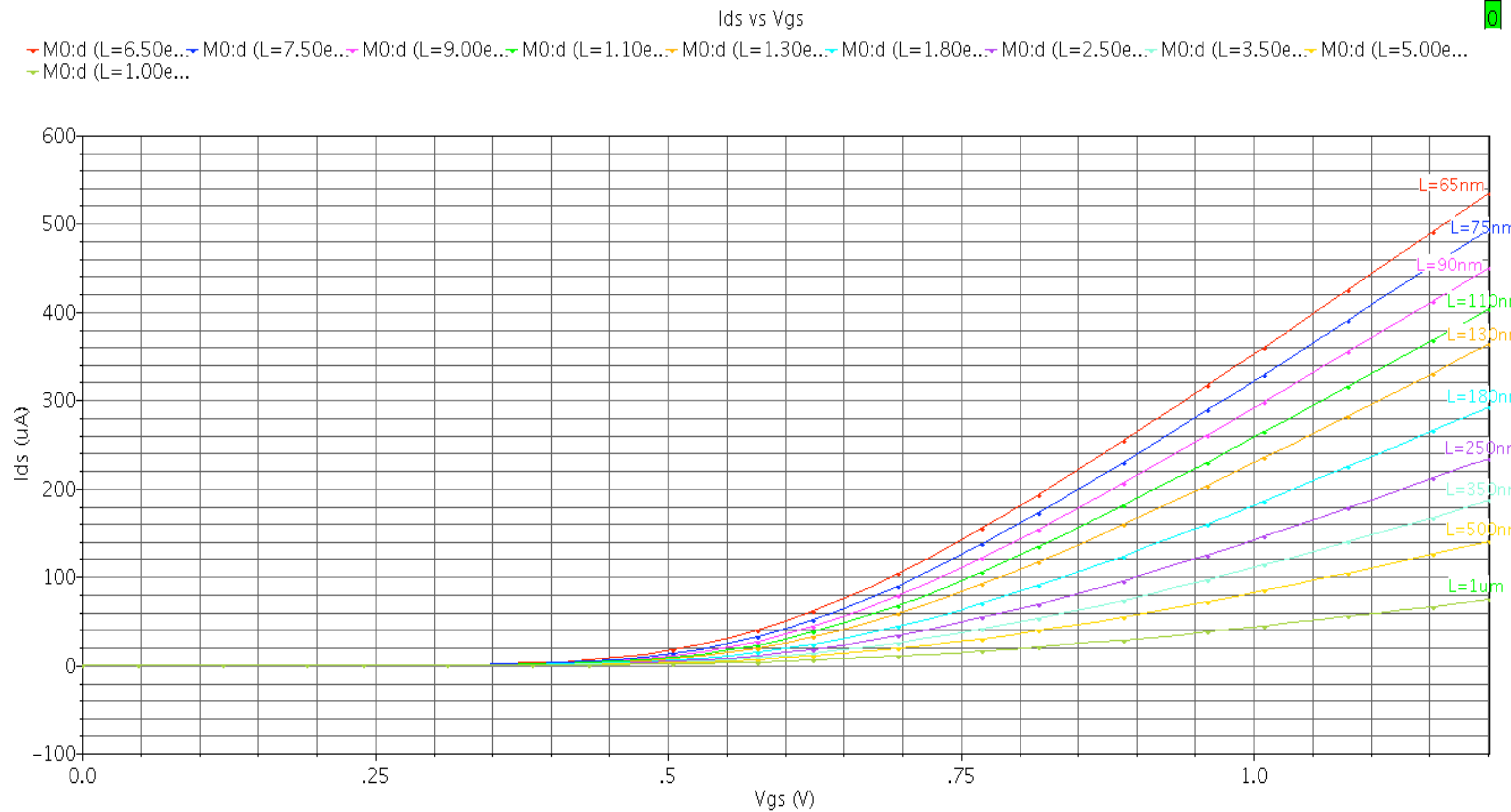
- The V_{TH} value is affected by the device size, due to the edge phenomena
  - They are typically negligible in larger device size
- In short channel,
  - The depletion region under the gates includes all the charge from source to drain
    - At source and drain, a part of the charge (Q_{CHL}) is due to the depletion region
    - It has not to be generated by the gate voltage.
      - ➔ V_{TH} reduction.
  - The drain voltage moves (Drain-Induced Barrier Lowering effect – DIBL)
      - ➔ V_{TH} reduction
      -
  - Very low V_{TH} values can be reached ➔ critical situation
  - Solution: some additional technological steps (typically a modified doping profile at the channel edges, like HALO) are introduced
    - V_{TH} is maintained at a certain value
      - ➔ the channel lenght reduction results in V_{TH} increase

Transistor Behaviour - Experience 5

V_{TH} dependence on MOSgate length (L)

The solution

- The simulation
  - Use a DC simulation for different L values (W is costant)
    - Plot I_D-.vs.-V_{GS}



Transistor Behaviour - Experience 6

V_{TH} dependence on MOS gate width (W)

The problem

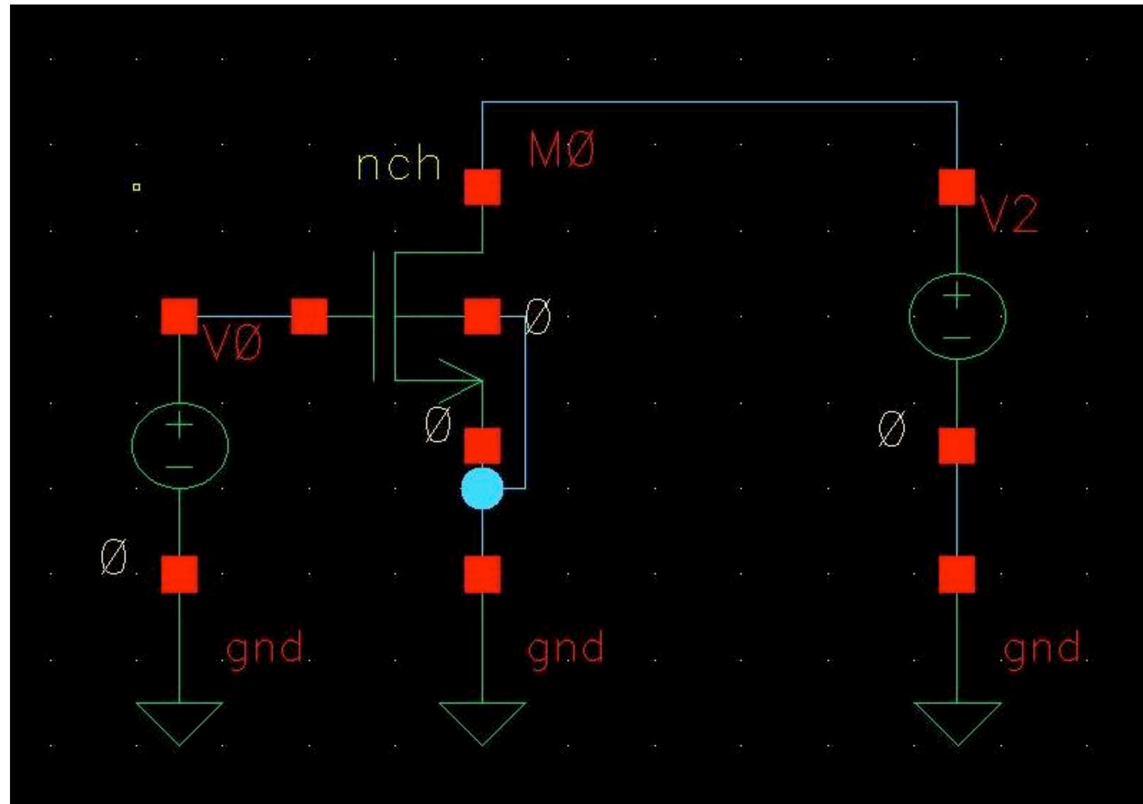
- Design the L size of a MOS device (Example L=100nm)
  - Fix W=200nm
  - Bias the MOS with V_{GS}=0.5V & V_{DS} = 1V
  - Extract V_{TH} from the simulator output file in the OP analysis
    - Repeat the simulation for different W values in the range W=[200nm to 1.5µm]
      - Plot di V_{TH} vs. W

Transistor Behaviour - Experience 6

V_{TH} dependence on MOS gate width (W)

The solution

- The circuit

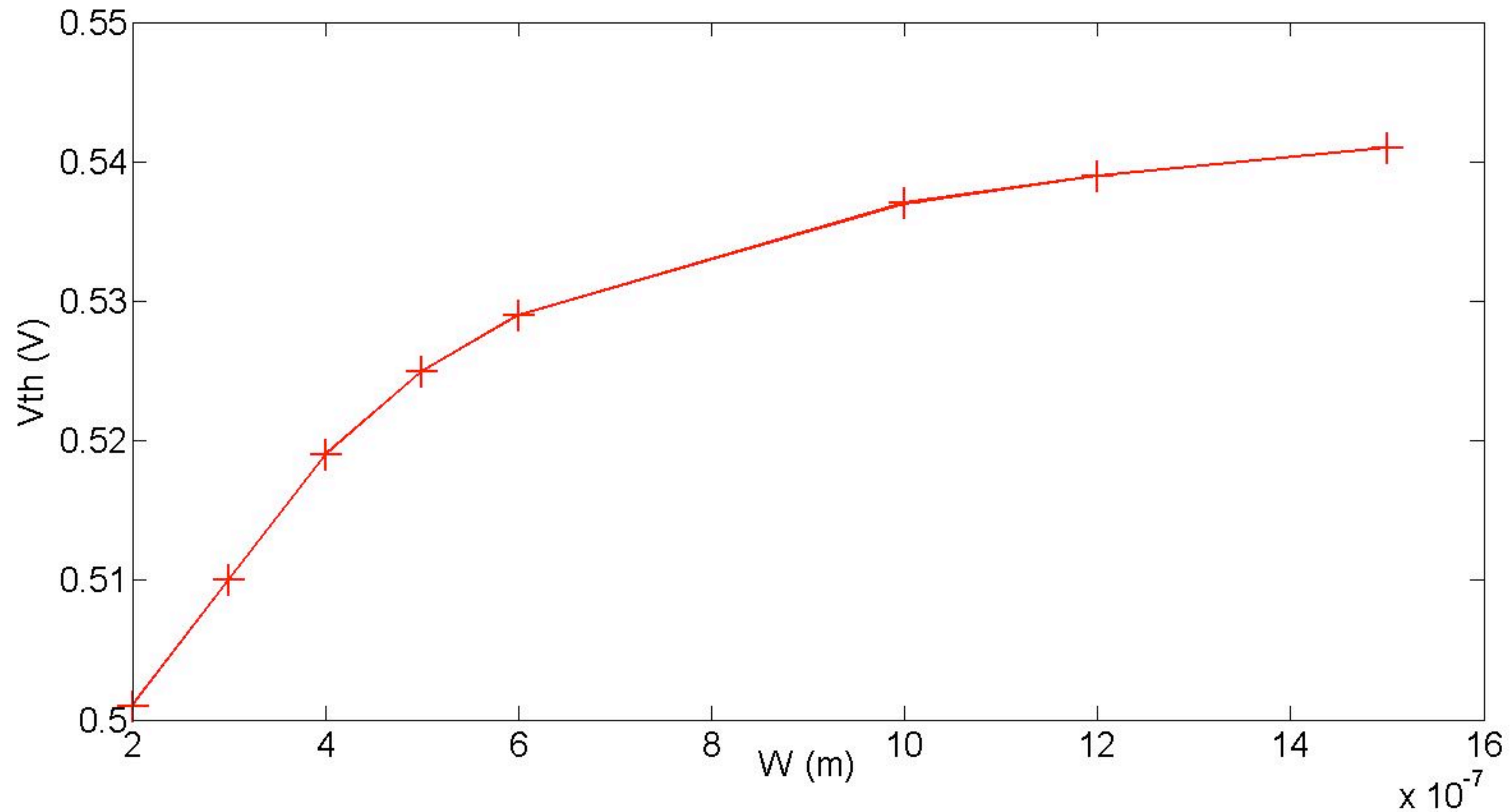


Transistor Behaviour - Experience 6

V_{TH} dependence on MOS gate width (W)

The solution

- The simulation



Transistor Behaviour - Experience 7

Velocity saturation effects

The problem

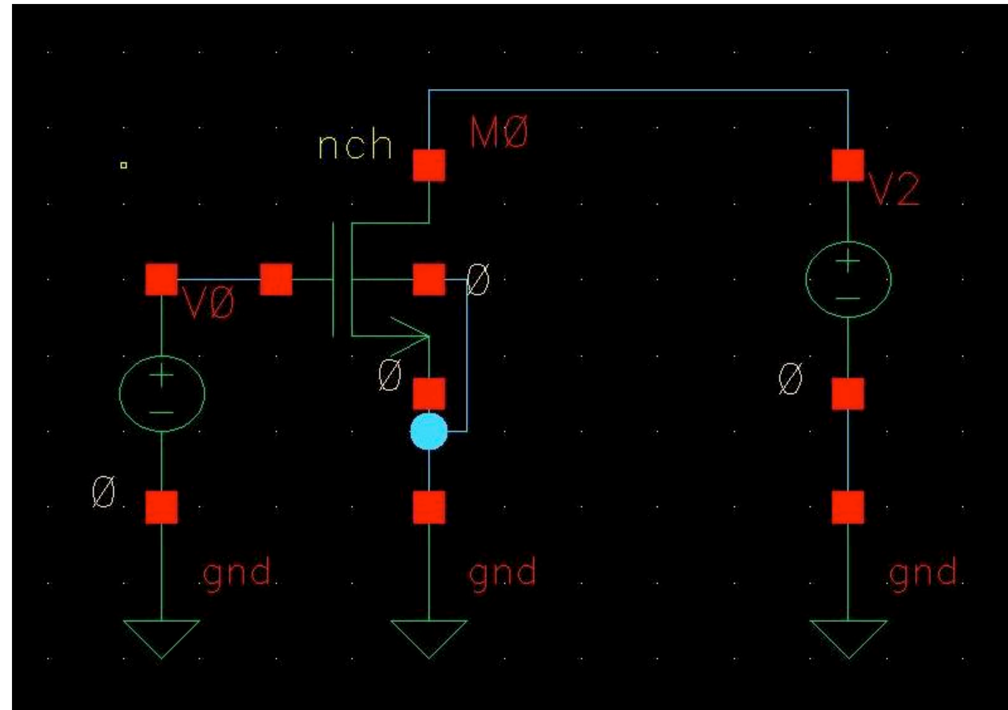
- Target:
  - Verify the effect of the velocity saturation
    - These effects can be observed plotting g_m vs. V_{GS}
      - V_{GS} is assuming a value between 0.2V to 1.2V
    - Higher is V_{GS}, higher is the electric field
  - Use L=65nm,W=500nm, V_{DS} = 1.2V

Transistor Behaviour - Experience 7

Velocity saturation effects

The solution

- The circuit

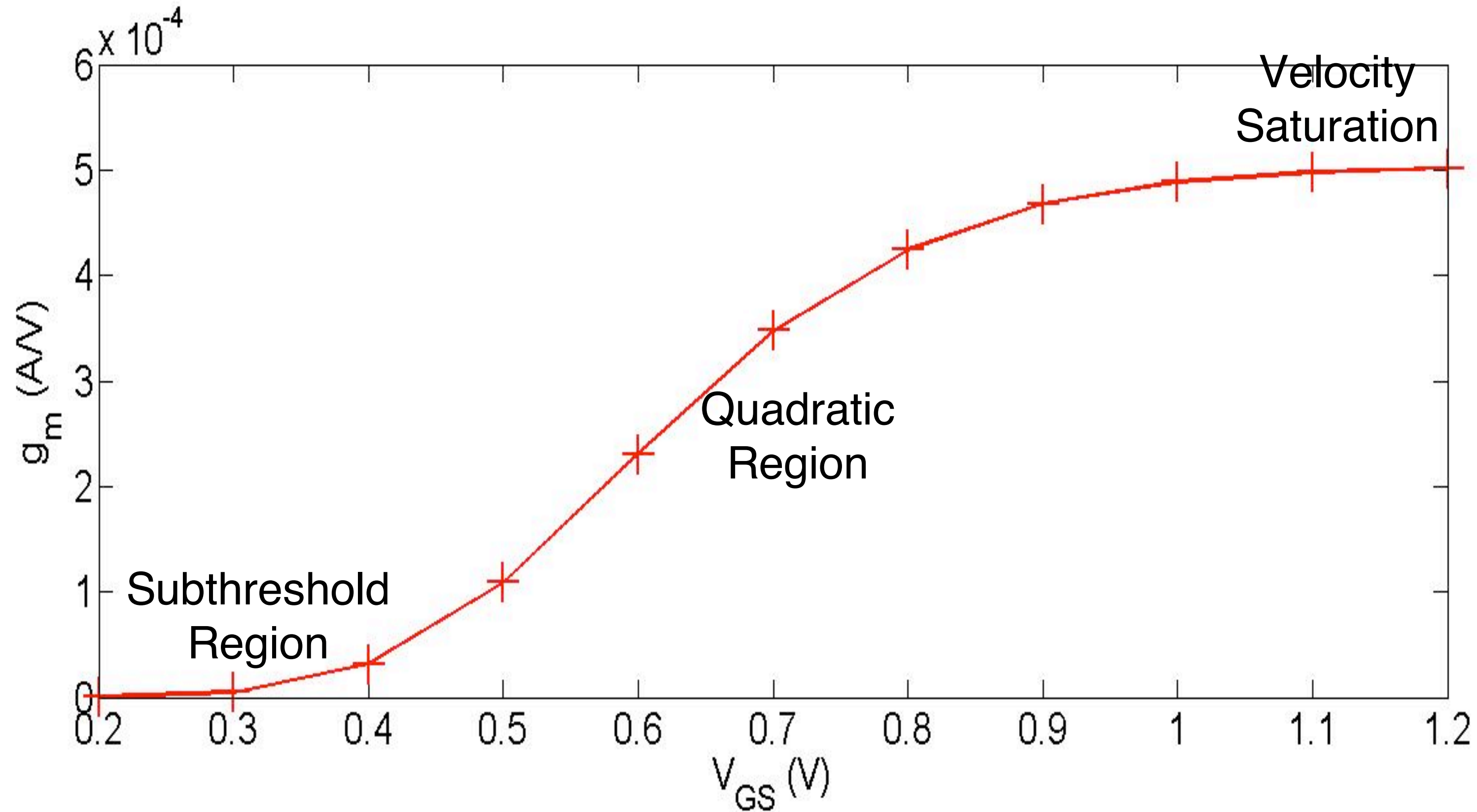


Transistor Behaviour - Experience 7

Velocity saturation effects

The solution

- The simulation
  - Use a DC analysis (one per each V_{GS} value)
    - Extract the g_m value from the simulator output file



Transistor Behaviour - Experience 8

Gate current effects

The problem

- Design a simple current mirror with

  I_{REF} = 10μA

  W/L = 120nm/65nm

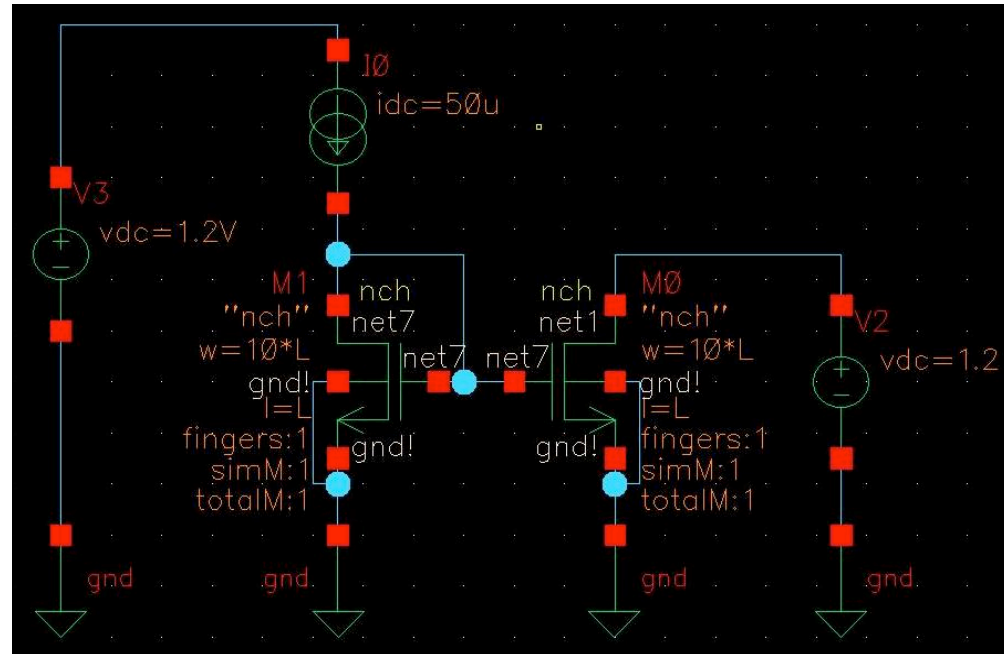
  - Plot I_{out}-vs.-V_{out} for V_{out} in [200mV – 1V]
  - Repeat the simulation increasing both W & L device sizes for 2x, 4x, 8x, 16x
    - i.e. maintaining W/L constant

Transistor Behaviour - Experience 8

Gate current effects

The solution

- The circuit



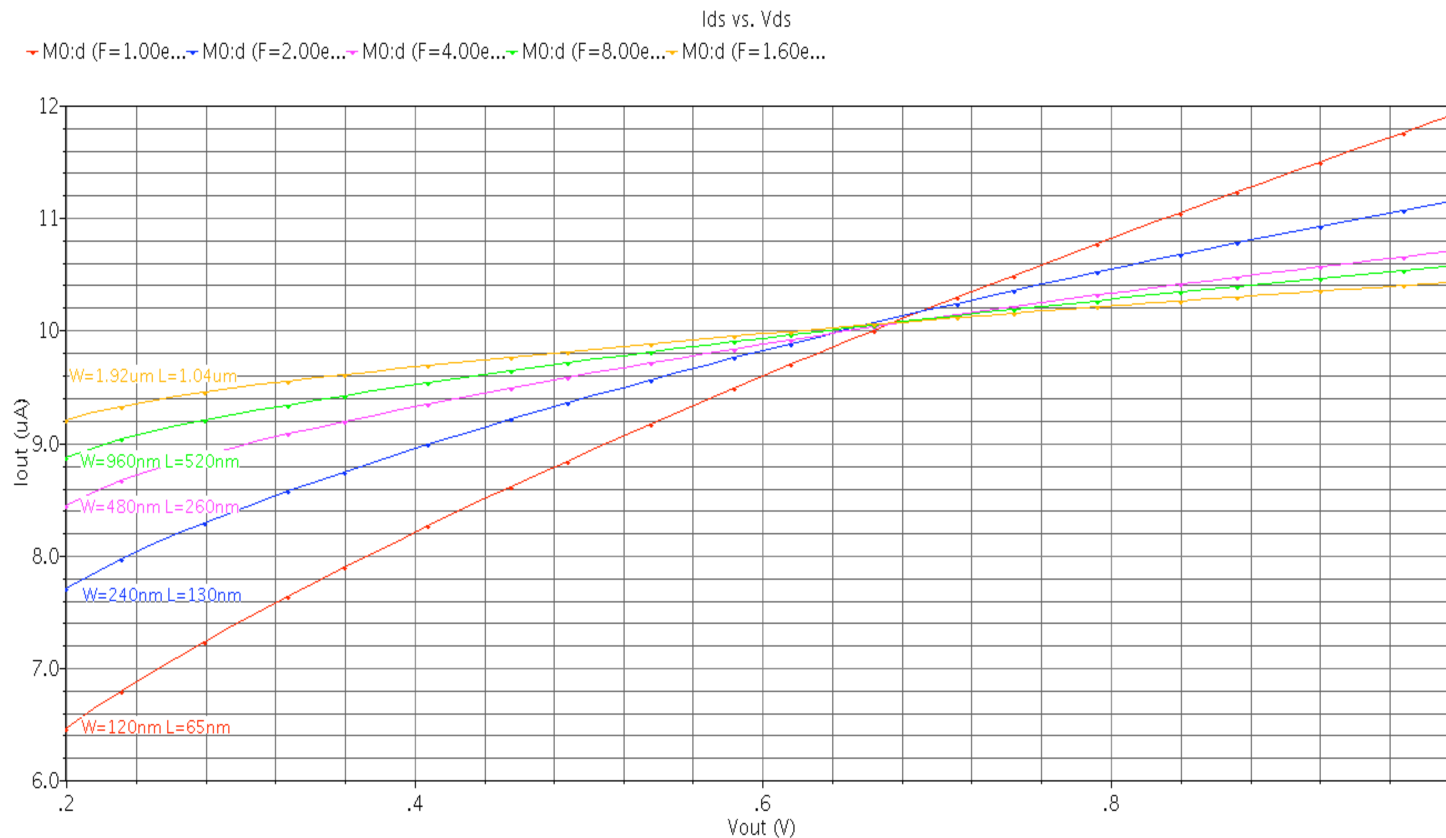
- The simulation
  - A DC analysis is used

Transistor Behaviour - Experience 8

Gate current effects

The solution

- The simulation results
  - The current mirror performance is exhibited in the following plot
  - Different L values (maintaining a constant (W/L)=120/65

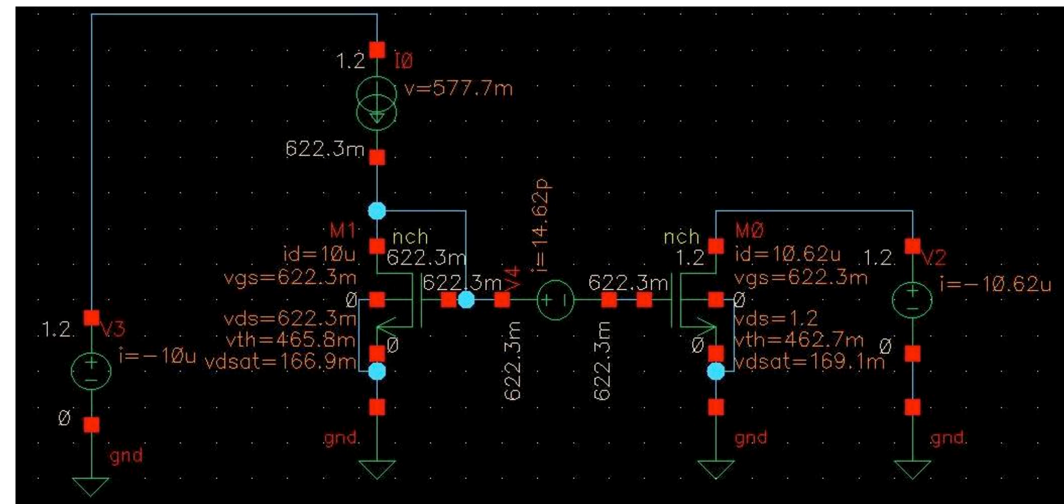


Transistor Behaviour - Experience 8

Gate current effects

Comments

- The inaccuracy of the current mirror in the above analysis is due to two main reasons:
  - The output impedance
  - The current gate
  - The importance of the contributions would have to be separated
    - The gate current effects can be nulled by introducing an ideal voltage buffer (a VCVS block) in series of each gate
      - The M_0 gate current is not extracted from the M_1 current
- The resulting scheme is:

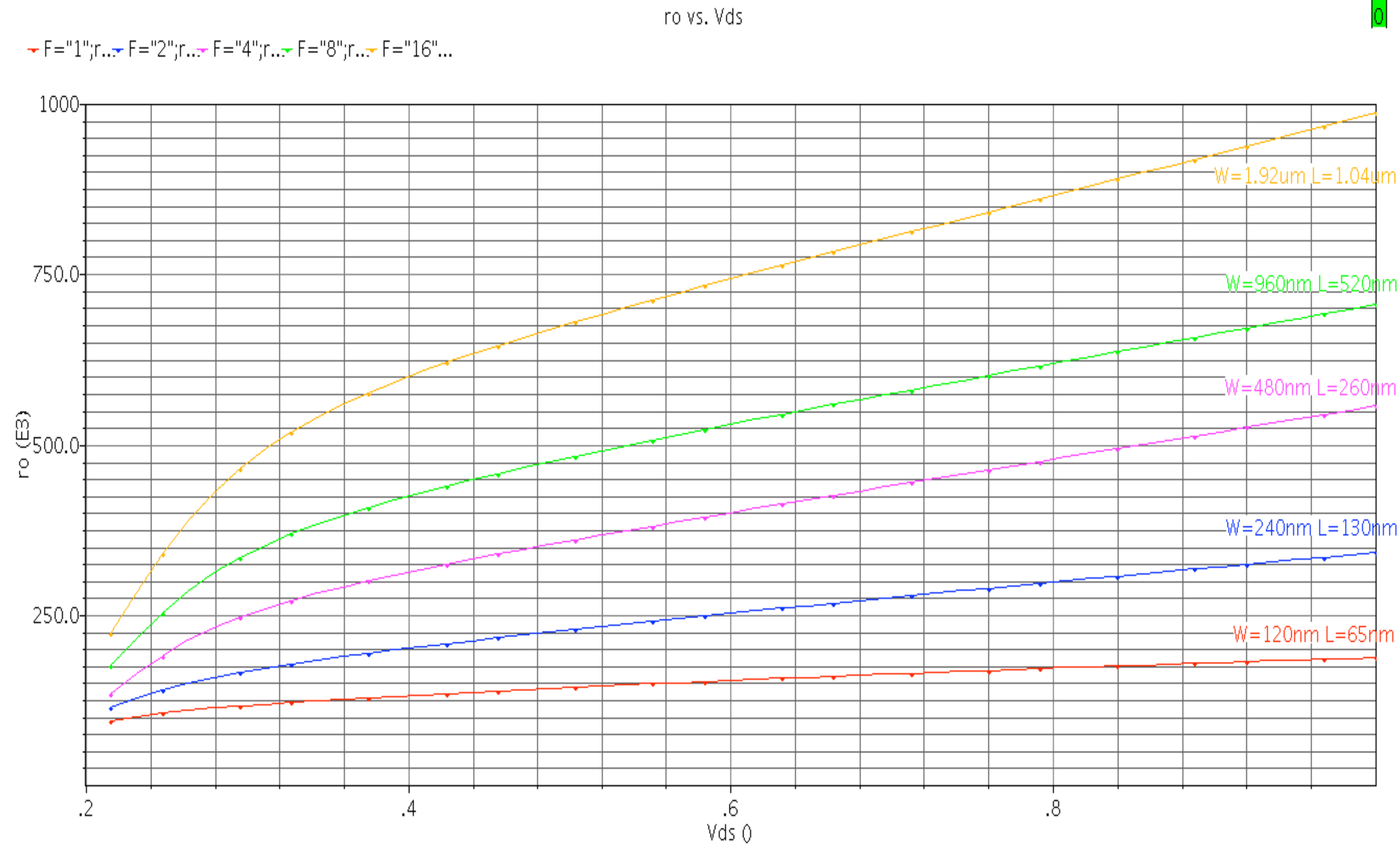


Transistor Behaviour - Experience 8

Gate current effects

The solution

- Verify that the output impedance increases with L increase

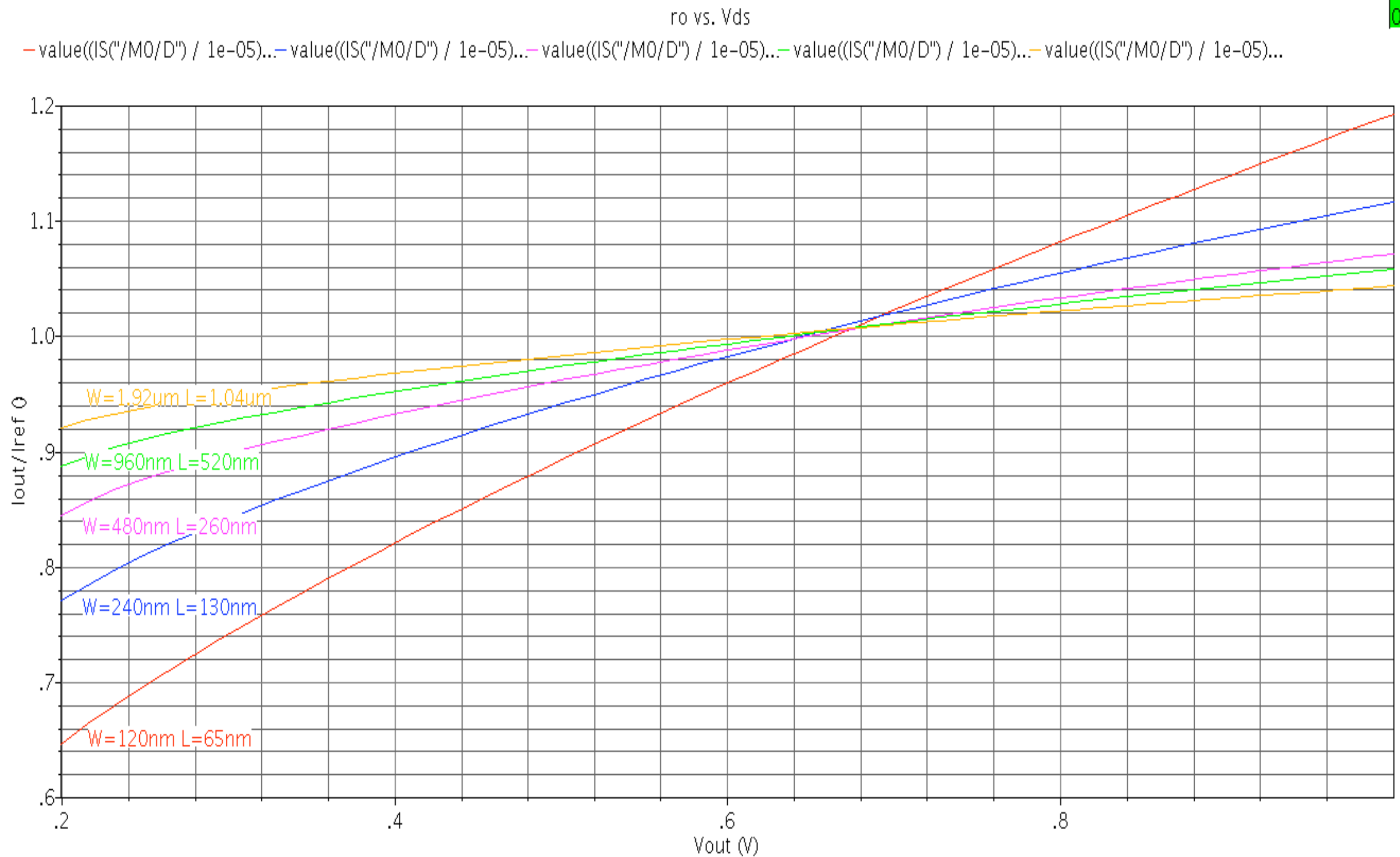


Transistor Behaviour - Experience 8

Gate current effects

The solution

- Verify the gain accuracy

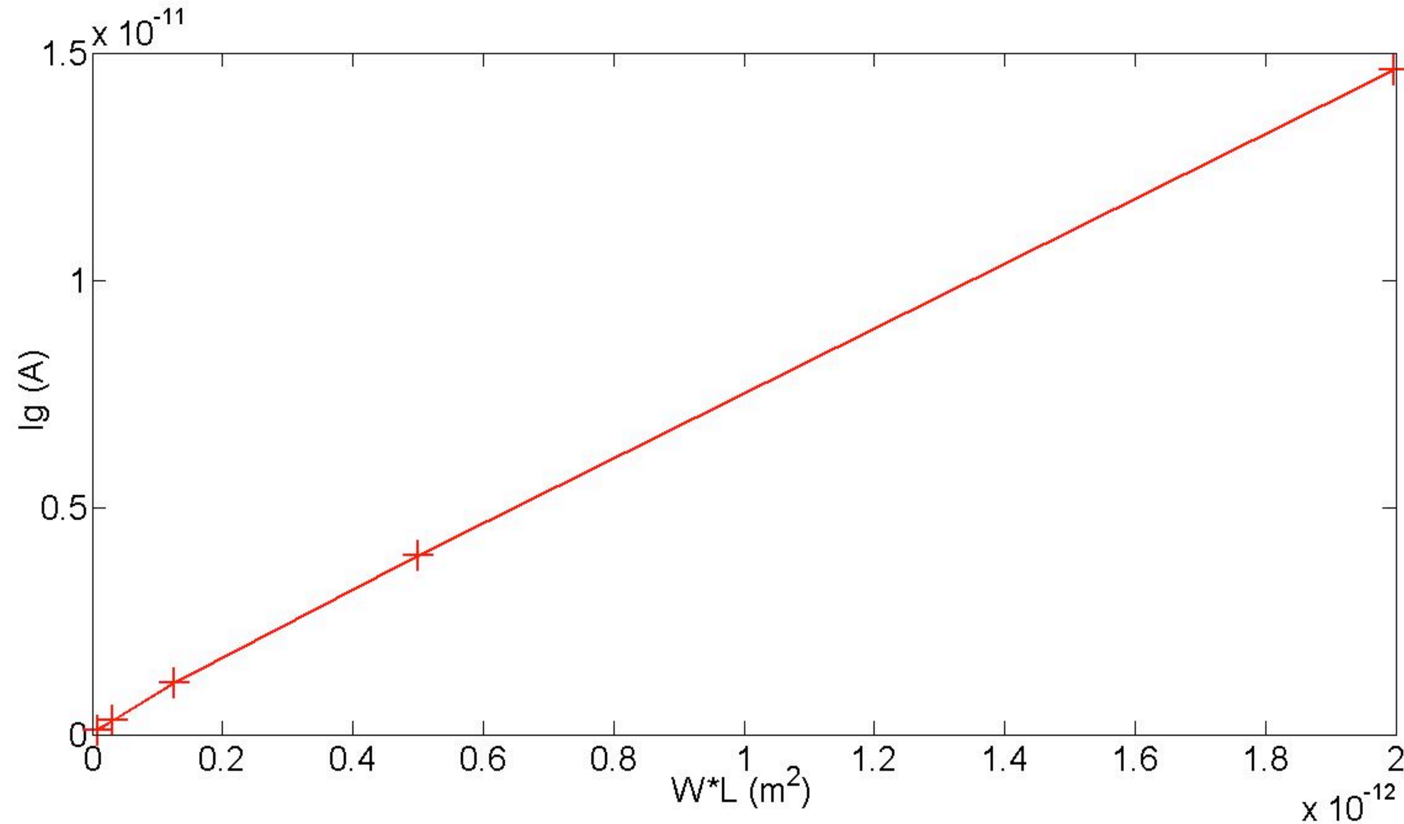


Transistor Behaviour - Experience 8

Gate current effects

The solution

- Plot I_G for the different L value



Circuit Design - Experience 1

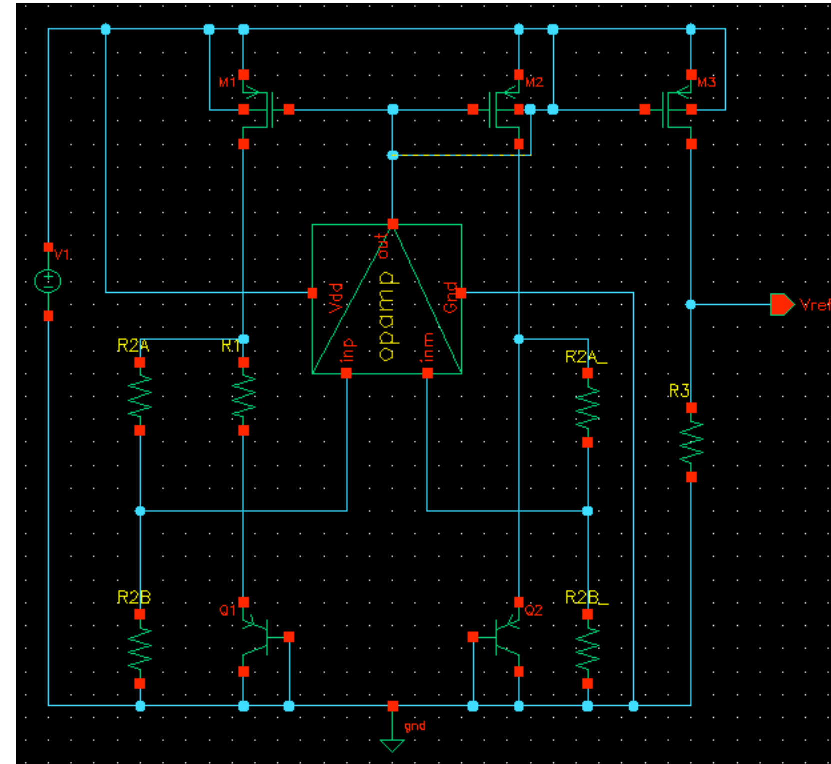
LV Bandgap design

The problem

- Design a low-voltage bandgap using the following scheme
- Starting points

$$I_{total} = 50\mu A$$
$$V_{DD} = 1.2V$$
$$\text{Target } V_{ref}=600mV$$

- Verify / Plot
  - V_{REF} vs. V_{DD}
  - V_{REF} vs. TEMP
  - Output noise spectrum



Circuit Design - Experience 1

LV Bandgap design

Comment

- Typical bandgap voltage V_{BG} = 1.26V
  - In scaled technology (like 65nm)

    $$V_{BG} (= 1.26V) > V_{DD} = 1.2V$$

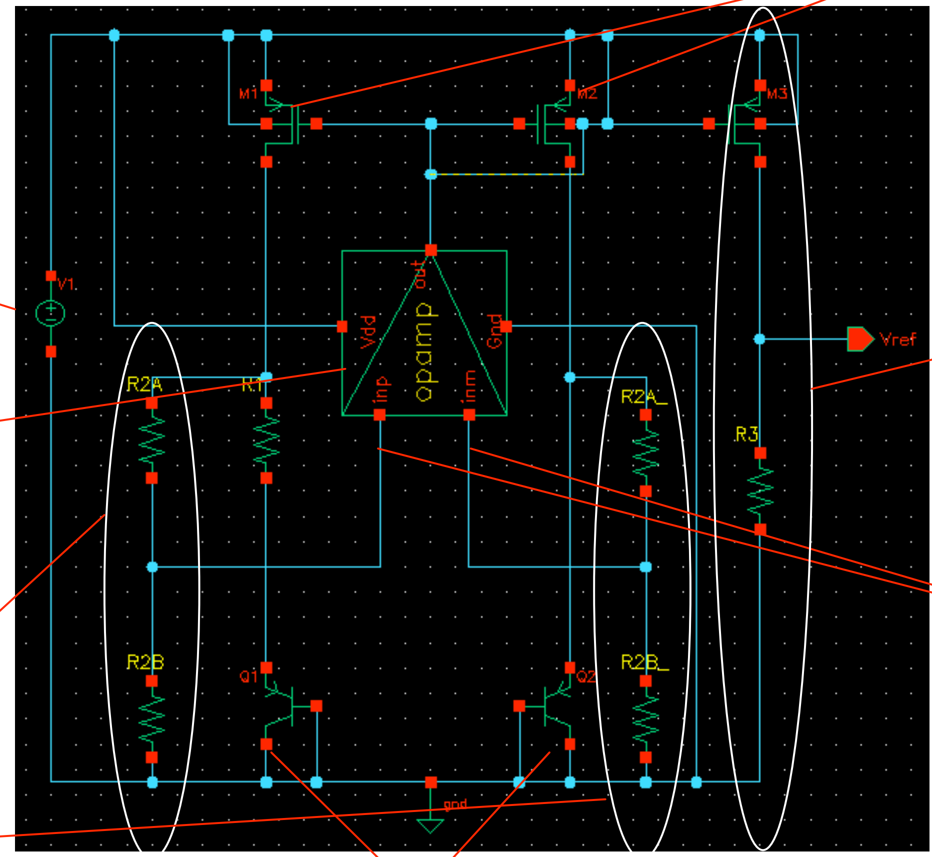
  - Standard Bandgap Voltage Generator circuits cannot be used
  - Alternative Low-Voltage circuits have to be used
    - The generated V_{BGLV} is lower
      - But V_{BGLV} guarantees the required temperature behavior

Circuit Design - Experience 1

LV Bandgap design

Solution – Design analysis

- The scheme



Circuit Design - Experience 1

LV Bandgap design

Solution – Design analysis

- V_X and V_Y are forced to be equal (virtual ground)
- V_E and V_F are forced indirectly through resistive partition:

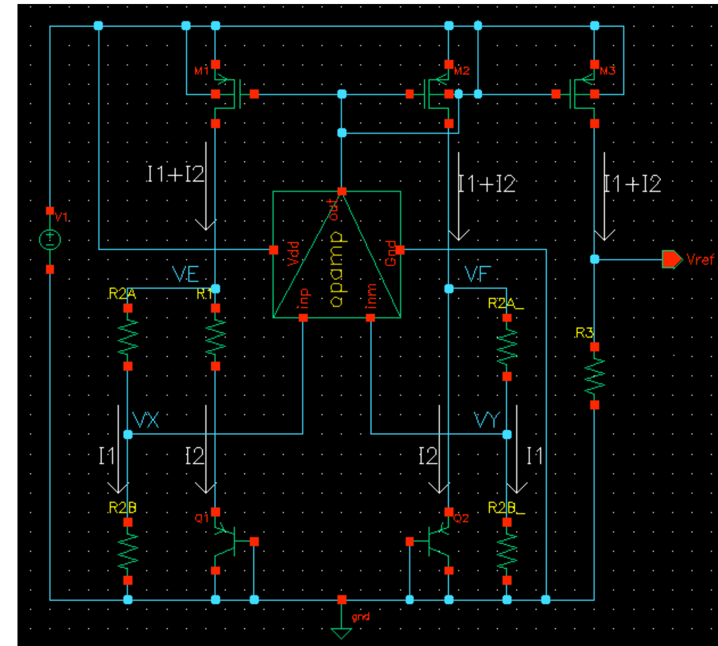
$$V_E = V_X \cdot \left(\frac{R_{2A} + R_{2B}}{R_{2B}} \right) = V_X \cdot k_E$$

$$V_F = V_Y \cdot \left(\frac{R_{2A} + R_{2B}}{R_{2B}} \right) = V_Y \cdot k_F$$

- Nominally (no mismatch)

$$k_E = k_F = k_R$$

- k_E and k_F depends on resistive matching



$$V_F = V_Y \cdot k_F = V_X \cdot k_F = V_E \cdot \frac{k_F}{k_E} = V_{EB2}$$

Circuit Design - Experience 1

LV Bandgap design

Solution – Design analysis

- Assuming:

$$I_1 = I_2$$

- For a good transistors matching:

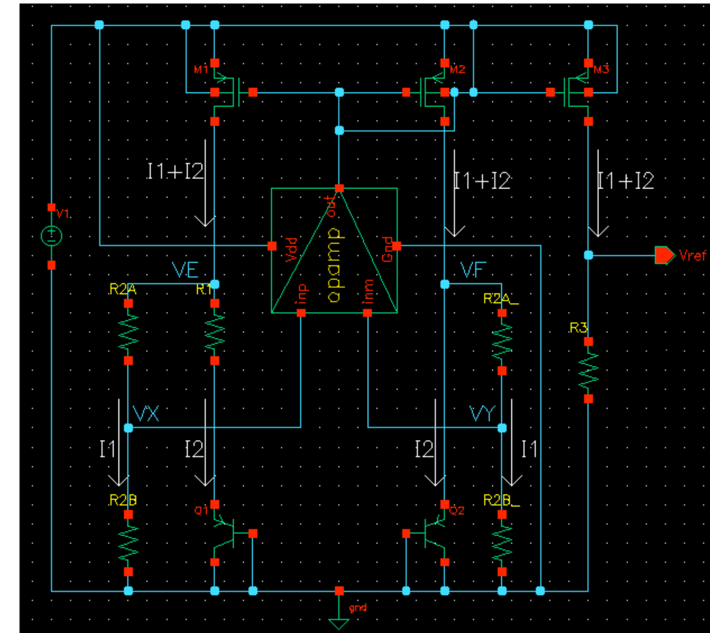
$$Area_Q_1 = N \cdot Area_Q_2 \quad \text{with } N = 8$$

- From the basic bandgap rule:

$$I_1 = V_T \cdot \ln(N)/R_1$$

$$I_2 = V_{EB2}/(R_{2A}+R_{2B}) = V_{EB2}/R_{2Tot}$$

$$V_{REF} = (I_1 + I_2) \cdot R_3$$



$$V_{REF} = \left(\frac{R_3}{R_{2Tot}}\right) \cdot \left[\left(\frac{R_{2Tot}}{R_1}\right) \cdot \ln(N) \cdot V_T + V_{EB2}\right]$$

Circuit Design - Experience 1

LV Bandgap design: Solution – Design procedure

- Current budget

$$I_{tot} = I_{Branch} + I_{Opamp} + I_{OutputStage}$$

- $I_{Branch} = 20\mu A$
  - For a good current-mirror matching
    - ➔ the same current for each current branches

$$\begin{cases} 2 \cdot (I_1 + I_2) = 20\mu\ A \\ I_1 = I_2 = 5\mu\ A \end{cases}$$

$I_1 = I_2 \rightarrow 5\mu A$

- $I_{Opamp} = 20\mu A$
- $I_{OutputStage} = 10\mu A$

- Separate the two designs
  - The two MOS branches
  - The embedded opamp

Circuit Design - Experience 1

LV Bandgap design

Solution – Design procedure: Two MOS branches

- MOS device bias

$$V_E = V_F = V_{EB2} \approx 600mV$$

$$V_{DSM2} = V_{DSM1} = V_{DD} - V_E \approx 600mV$$

- For good current-mirror matching: $V_{ovM2} = V_{ovM1} \approx 100mV$
  - ➔ calculate $(W/L)_{M2} = (W/L)_{M1}$ as follows:

$$\left(\frac{W}{L}\right)_{M2} = \left(\frac{W}{L}\right)_{M1} = \frac{I_D}{K_p \cdot V_{ov}^2} = 20$$

- The assigned current I_D is:

$$I_D = I_1 + I_2 \approx 20\mu A$$

- Non minimum L for current-mirror matching and output-impedance purpose
  - Assuming $L_{M2} = L_{M1} = 0.3\mu m$ ➔ $W_{M2} = W_{M1} = 6\mu m$

Circuit Design - Experience 1

Bandgap design

Solution – Design procedure: Two MOS branches

- BJT Transistor design

$$Area_{Q1} = N \cdot Area_{Q0} \text{ where } N=8$$

- Resistor design:
  - Assuming $I_1=I_2=5\mu A$, from bandgap relationship:

$$I_1= V_T \cdot \ln(N)/R_1=5\mu A \rightarrow R_1 = 22.58k\Omega$$

  - From current level

$$I_2= V_{EB2}/(R_{2A}+R_{2B})=5\mu A \rightarrow R_{2A} +R_{2B} = V_{EB2} / I_2= 120k\Omega$$

  - From level shift:

$$V_E = V_X \cdot \left(\frac{R_{2A} + R_{2B}}{R_{2B}} \right) = V_X \cdot k_R$$

  - For a good resistors matching $K_R=2 \rightarrow R_{2A} = R_{2B} \cdot (k_R - 1) = R_{2B}$
  - → Final values

$$R_{2A} = 60k\Omega \qquad R_{2B} = 60k\Omega$$

Circuit Design - Experience 1

Bandgap design

Solution – Design procedure: Output stage

- R_3 design:
  - Output voltage target:

$$V_{REF} = 600mV$$

  - From bandgap relationship:

$$V_{REF} = \left(\frac{R_3}{R_{2Tot}}\right) \cdot \left[\left(\frac{R_{2Tot}}{R_1}\right) \cdot \ln(N) \cdot V_T + V_{EB2}\right] \quad \rightarrow R_3 = 60k\Omega$$

  - The output stage current, I_{M3} is the same of the two MOS branches:

$$I_{M3} = I_1 + I_2 = I_{M1} = I_{M2} = 10\text{“}A$$

  - For guarantee a good current-mirror matching
    - ➔ Design M3 with the same sizes of M1 and M2:

$$L_{M3} = L_{M2} = L_{M1} = 0.3\mu m$$
$$W_{M2} = W_{M2} = W_{M1} = 6\mu m$$

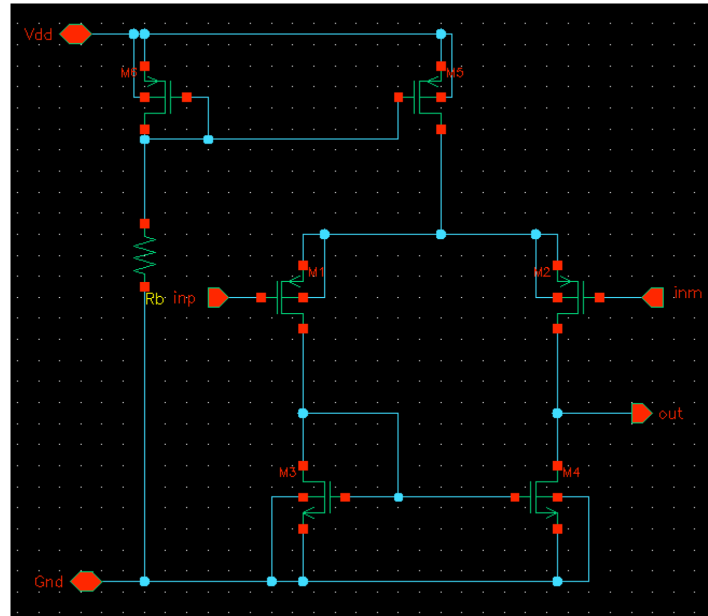
Circuit Design - Experience 1

Bandgap design

Solution – Design procedure: Embedded opamp

- Opamp Topology choice:
  - Differential input with low (≈300mV) common mode level
    - ➔PMOS input differential pair

- The chosen embedded opamp scheme:

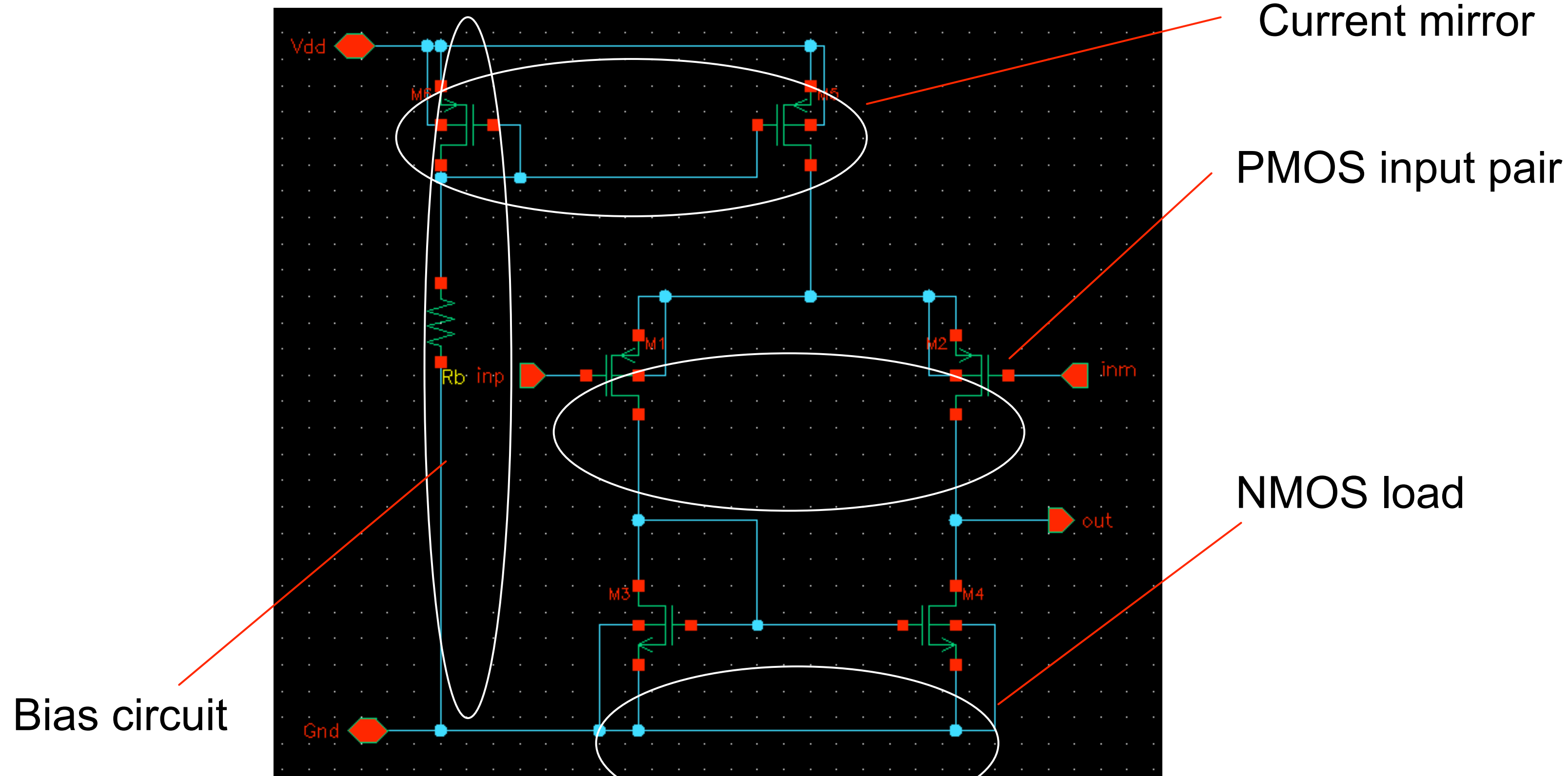


Circuit Design - Experience 1

Bandgap design

Solution – Design procedure: Embedded opamp

- The embedded opamp scheme: single stage opamp with PMOS input pair



Circuit Design - Experience 1

Bandgap design

Solution – Design procedure: Comments on the embedded opamp

$$V_X = V_Y = \left(\frac{R_{2B}}{R_{2A}+R_{2B}}\right)\cdot V_{EB2}$$

- ➔ A PMOS error amplifier input stage
- ☺ V_{DDmin} lowers (limited by the input stage of the voltage-mode error amplifier)

$$V_{REF} = \left(\frac{R_3}{R_2}\right)\cdot\left[V_{EB2} + \left(\frac{R_2}{R_1}\right)\cdot ln(N)\cdot V_T\right]$$

- ☹ The amplified effect of the offset voltage (V_{OFF}) due to the error amplifier.

$$V_{REF} = \left(\frac{R_3}{R_2}\right)\cdot\left\{V_{EB2} + \left(\frac{R_2}{R_1}\right)\cdot\left[ln(N)\cdot V_T + V_{ERR1}\right]\right\}$$

$$V_{ERR1} = [(R_{2A} + R_{2B})/R_{2A}] / V_{OFF} > V_{OFF}$$

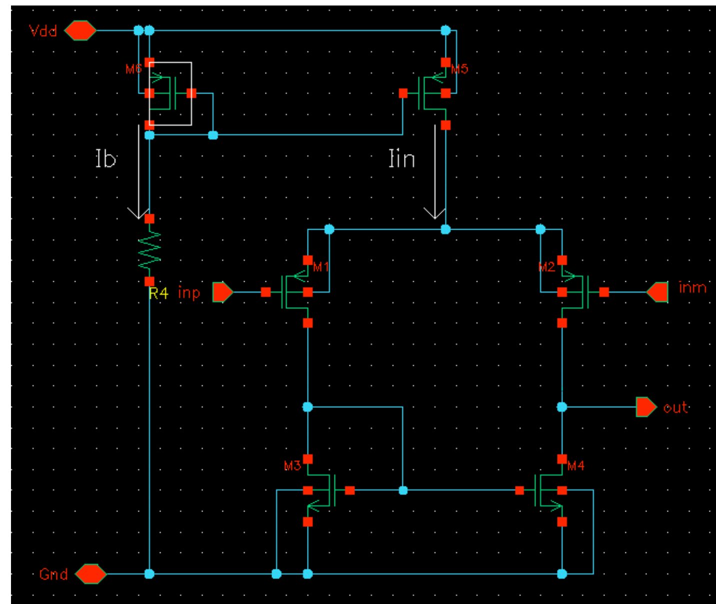
- By using a large value of N(N=64)→$\Delta V_{be}=V_{tT}\cdot\log(N)$ increases→V_{OFF} has less impact

Circuit Design - Experience 1

Bandgap design

Solution – Design procedure: Embedded opamp

- Current branches
  - The total current budget for the opamp is 20µA
  - For good current mirror matching
    - Assign: $I_{in}=I_b=10\mu A$



Circuit Design - Experience 1

Bandgap design

Solution – Design procedure: Embedded opamp

- MOS and bias circuit design
- For a good matching design all MOS overdrive $V_{ov} \approx 100mV$
  - ➔ calculate the MOS sizes as follows:

$$\left(\frac{W}{L}\right)_{M2} = \left(\frac{W}{L}\right)_{M1} = \frac{I_{in}/2}{K_p \cdot V_{ov}^2} = 10$$

$$\left(\frac{W}{L}\right)_{M5} = \left(\frac{W}{L}\right)_{M6} = \frac{I_{in}}{K_p \cdot V_{ov}^2} = 20$$

$$\left(\frac{W}{L}\right)_{M3} = \left(\frac{W}{L}\right)_{M4} = \frac{I_{in}/2}{K_n \cdot V_{ov}^2} = 3$$

- Non minimum L for current-mirror matching and output-impedance purpose
- Assuming L_M=0.3µm for all transistors➔

$$W_{M2} = W_{M1} = 3\mu m$$
$$W_{M5} = W_{M6} = 6\mu m$$
$$W_{M3} = W_{M4} = 1\mu m$$

- Since I_b=10µA➔ $R_b=(V_{dd}-|V_{GS}|_{M6})/I_b=66k\Omega$

Circuit Design - Experience 1

Bandgap design

Solution – Design procedure: Two MOS branches

- Transistor operating point

device	M1	M0	M5		device	Q1	Q0
betaeff	4.33m	4.33m	4.33m		betaac	1.015	1.017
gbd	1.369p	1.369p	1.362p		betadc	1.014	1.017
gbs	8.102p	8.102p	8.102p		cmu	3.117p	48.7f
gds	2.877u	2.876u	2.865u		cmux	0	0
gm	185.2u	185.2u	185.5u		cpi	2.252p	36.42f
gmbs	30.08u	30.08u	30.13u		csub	0	0
gmoverid	18.35	18.35	18.34		ft	2.863M	180.8M
ibulk	792.9f	793f	795.3f		gm	96.58u	96.69u
id	-10.09u	-10.09u	-10.11u		ib	-2.478u	-2.476u
ids	-10.09u	-10.09u	-10.11u		ic	-2.512u	-2.518u
igb	-628.7a	-628.7a	-628.7a		isub	-0	-0
igcd	-432.2f	-432.2f	-432.1f		pwr	3.039u	3.582u
igcs	-463f	-463f	-463f		rb	870.6m	55.4
igd	-112.6a	-105.5a	-10.78a		rc	70.21m	4.494
igidl	-0	-0	-0		region	1	1
igisl	-0	-0	-0		ro	193M	192.2M
igs	-496.9f	-496.9f	-496.9f		rpi	10.51K	10.51K
pwr	4.866u	4.87u	4.941u		struct	1	1
rdeff	7.649	7.649	7.649		type	1	1
region	2	2	2		vbc	0	0
reversed	0	0	0		vbe	-609m	-717.4m
rgbd	0	0	0		vce	-609m	-717.4m
ron	47.76K	47.8K	48.33K		vsub	2.157u	137.2u
rseff	7.649	7.649	7.649				
vbs	0	0	0				
vds	-482.2m	-482.6m	-488.8m				
vdsat	-79.52m	-79.52m	-79.52m				
vgs	-489.5m	-489.5m	-489.5m				
vth	-467.3m	-467.3m	-467.3m				

Circuit Design - Experience 1

Bandgap design: Solution – V_{REF} vs. TEMP

- Nominal

  V_{REF} = 602mV
  T = 27°C

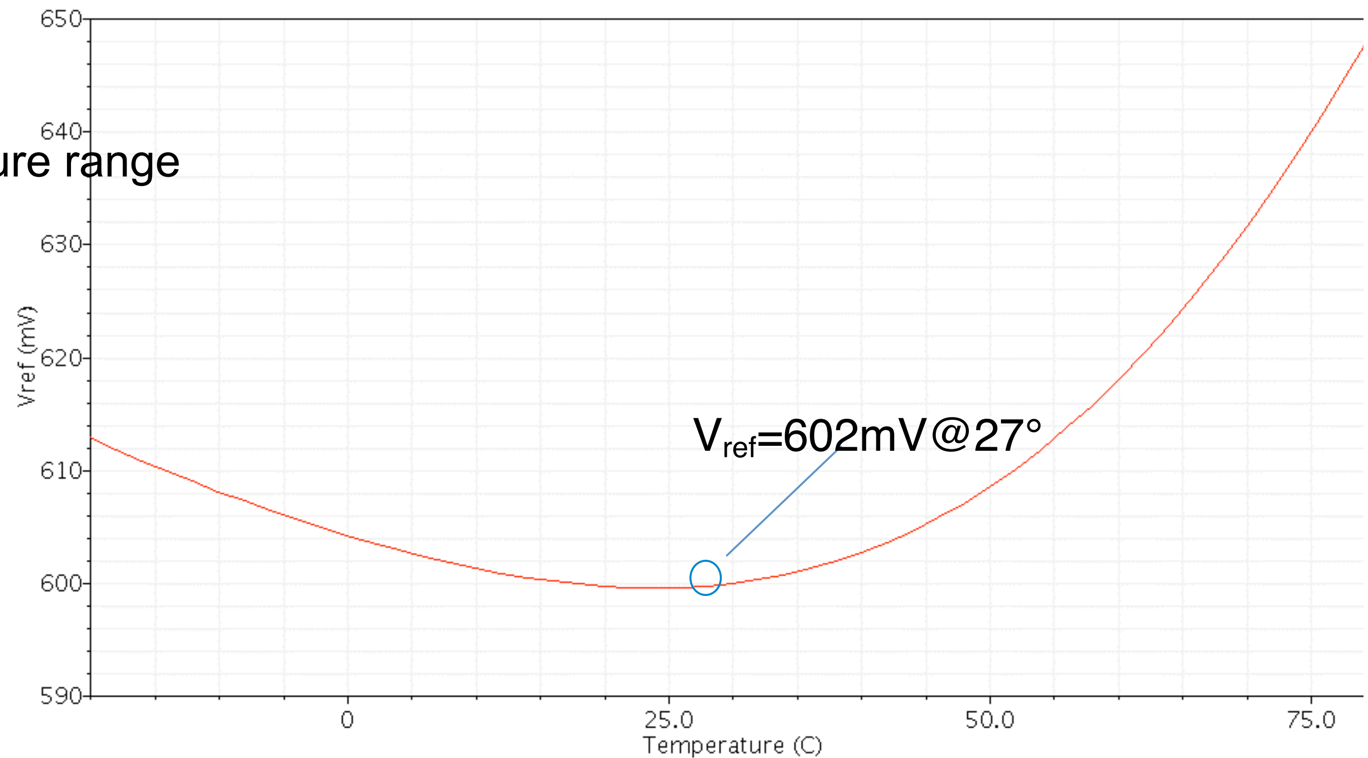
- Edges of the temperature range

  V_{REF} = 611.5mV
  T = -20°C

  V_{REF} =649mV V_{ref}
  T = 80°C

  ➔ ΔV_{REF}= 47mV

  ➔ $\Delta V_{REF}/V_{REF}$ =7.8%

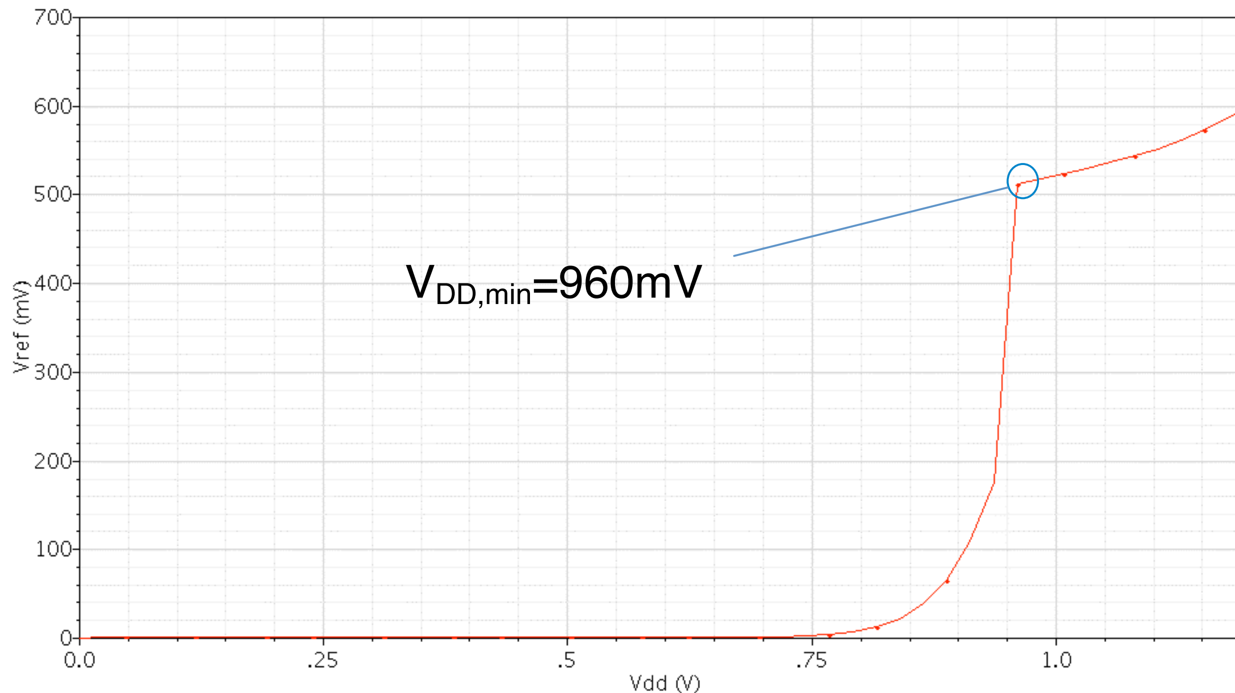


Circuit Design - Experience 1

Bandgap design

Solution – V_{REF} vs. V_{DD}

- Simulation: power supply dependence



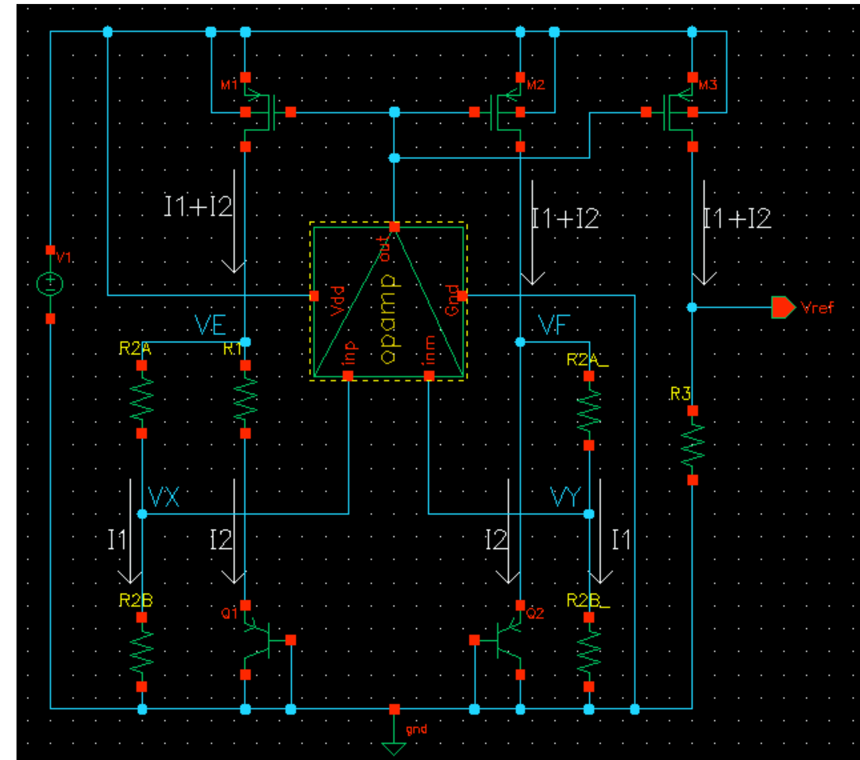
- The minimum supply voltage ($V_{DD,min}$) is 960mV
- Under this value the V_{REF} changes rapidly according to V_{DD}
  - ➔ Poor rejection of the disturbs on the supply

Circuit Design - Experience 1

Bandgap design

Solution – LV Bandgap design

- V_{DD} is limited by the bias condition of the opamp input stage
- A lower V_{DD}
  - ➔ a lower power consumption
  - ➔ a lower immunity to the large disturbs
- To lower V_{DD} ➔ lower V_X
  - ➔ higher k_F & k_E
    - R_{2B} has to be larger than R_{2A}
  - ➔ higher sensitivity to resistor mismatch
    - R_{2B} and R_{2A} are differently sized ➔ they suffers more the mismatch
      - ➔ higher sensitivity to opamp offset
        - ➔ the opamp offset is amplified by k_R



Circuit Design - Experience 1

Bandgap design

Comment on the temperature dependence and the VREF design

- (R_{2Tot}/R_1) & N reduces temperature dependence
- $R_3/R_{2Tot} < 1$ ➔ $V_{REF} < 1.2V$
- ➔ V_{REF} adjusted for different applications
  - Ex.: $V_{REF} \approx 550mV$

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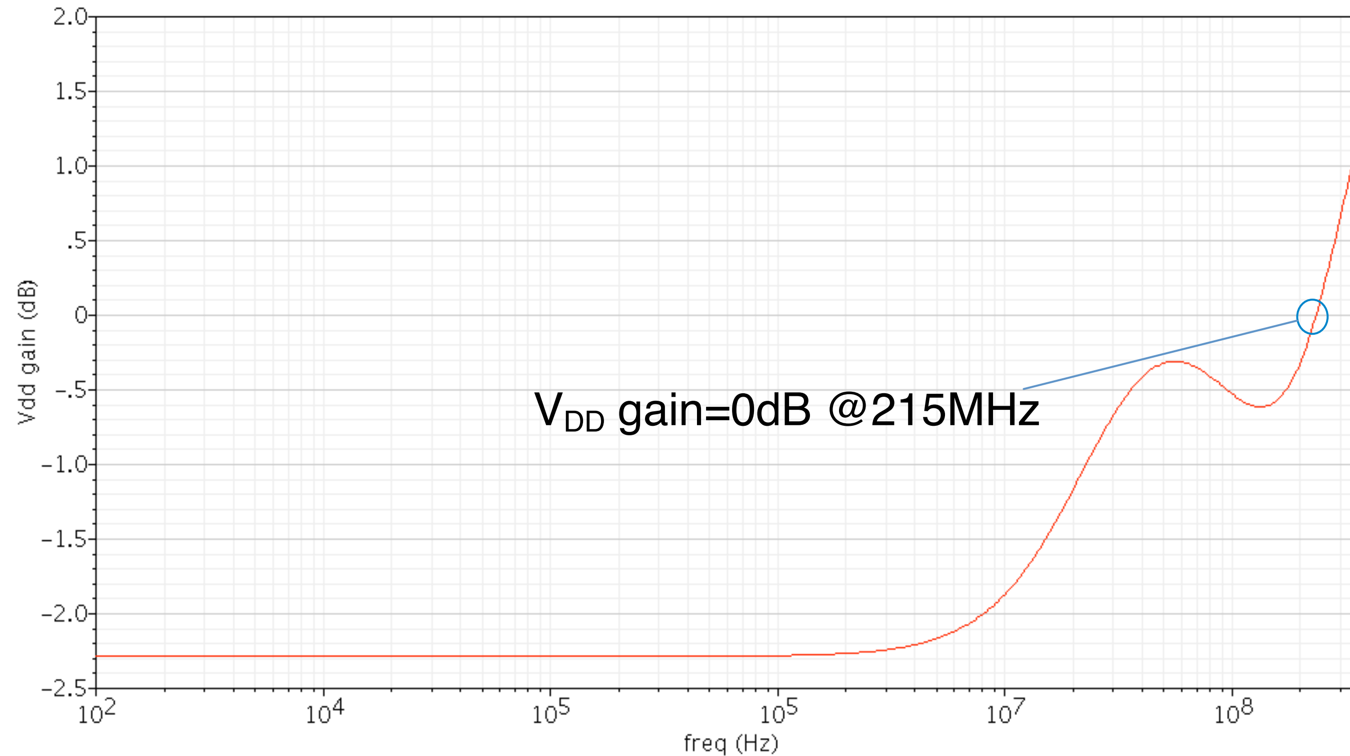
Circuit Design - Experience 1

Bandgap design

Solution – V_{DD}gain

- Gain from V_{DD} to V_{ref} (V_{DDgain}) in the frequency domain



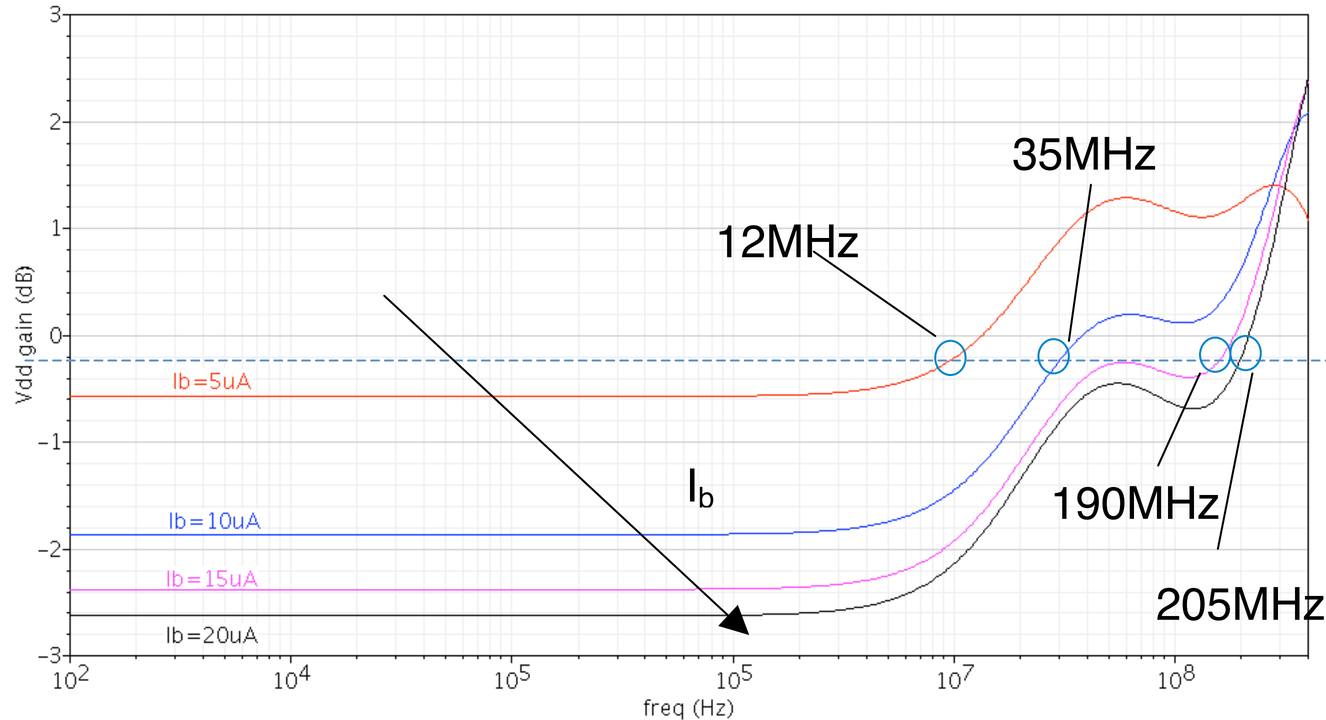
- V_{DDgain} is 0dB @ 215MHz
  - ➔ over this frequency the disturbs from supply are amplified

Circuit Design - Experience 1

Bandgap design

Solution – V_{DD}gain

- Improvement of the $V_{DD\ gain}$



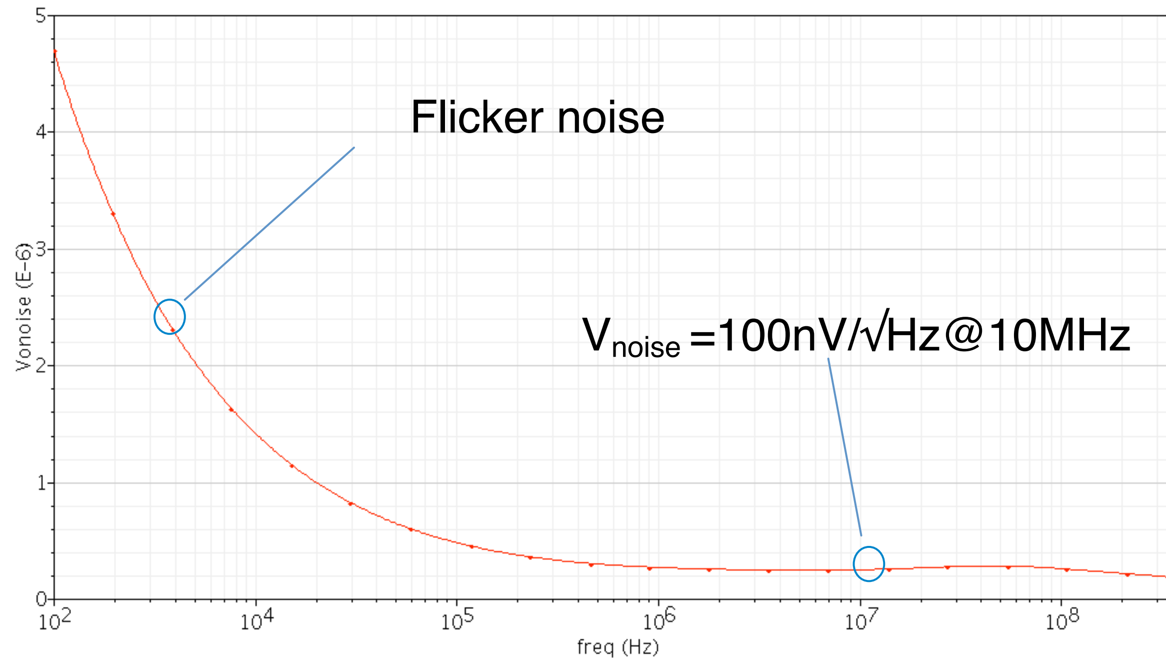
- Increasing the bias current of the opamp
  - ➔ $V_{DD\ gain}$ improves @ higher frequency
  - ➔ Higher power consumption

Circuit Design - Experience 1

Bandgap design

Solution – Noise analysis

- Plot the output noise V_{noise}

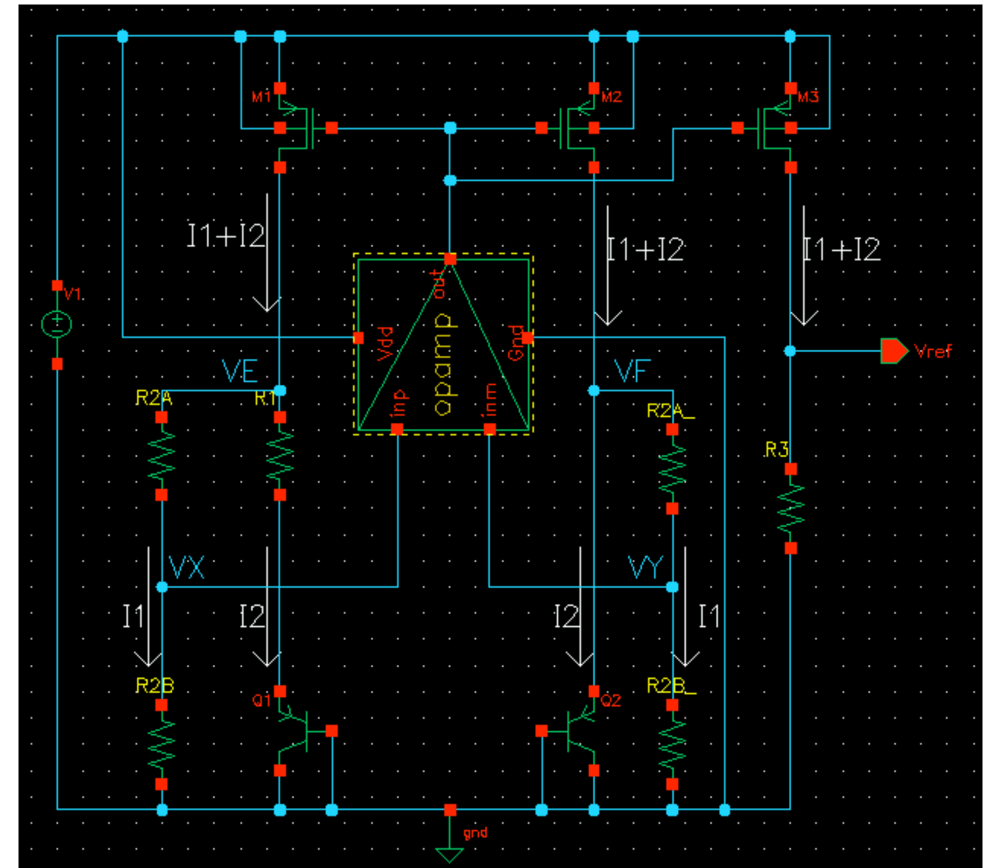


- Comments:
  - At low frequency the flicker noise is dominant
  - At high frequency the thermal noise is dominant
    - V_{noise}=100nV/√Hz@10MHz

Circuit Design - Experience 1

A Sub-1-V CMOS Bandgap without Low V_{TH} Devices

- The bulk-source junctions of M_1-M_3 are forward-biased
  - ➔ $|V_{THP}|$ is reduced
- The forward bias voltage is set to about 0.3V at the highest operational temperature
  - ➔ the p-n junction of the p-substrate and N-well will not be turned on
  - ➔ the error amplifier can operate in its high-gain output region to enforce voltages at nodes X and Y more closely



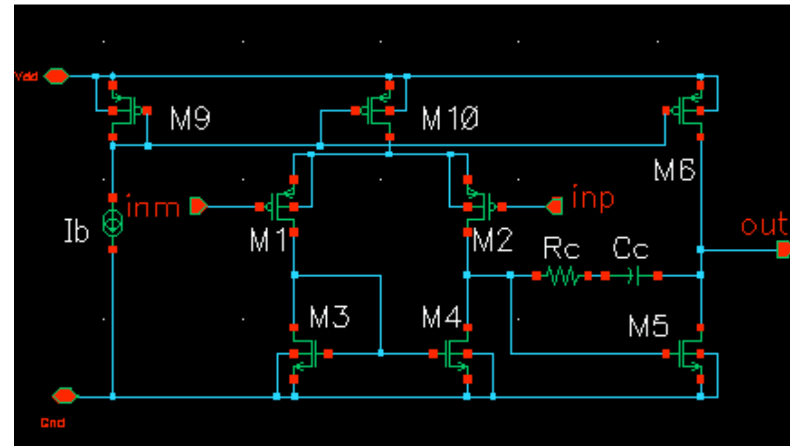
Circuit Design - Experience 2

Two-stage opamp design

The problem

- Design a two stage opamp with Miller-Compensation scheme

  - Opamp requirements:
    DC-gain ≥ 50dB
    UGB =100MHz
    C_L = 2pF
    SR = 63V/μs
    $\sqrt{v_{i,noise}^2} = 5nV/\sqrt{Hz}$



- Technology parameters:

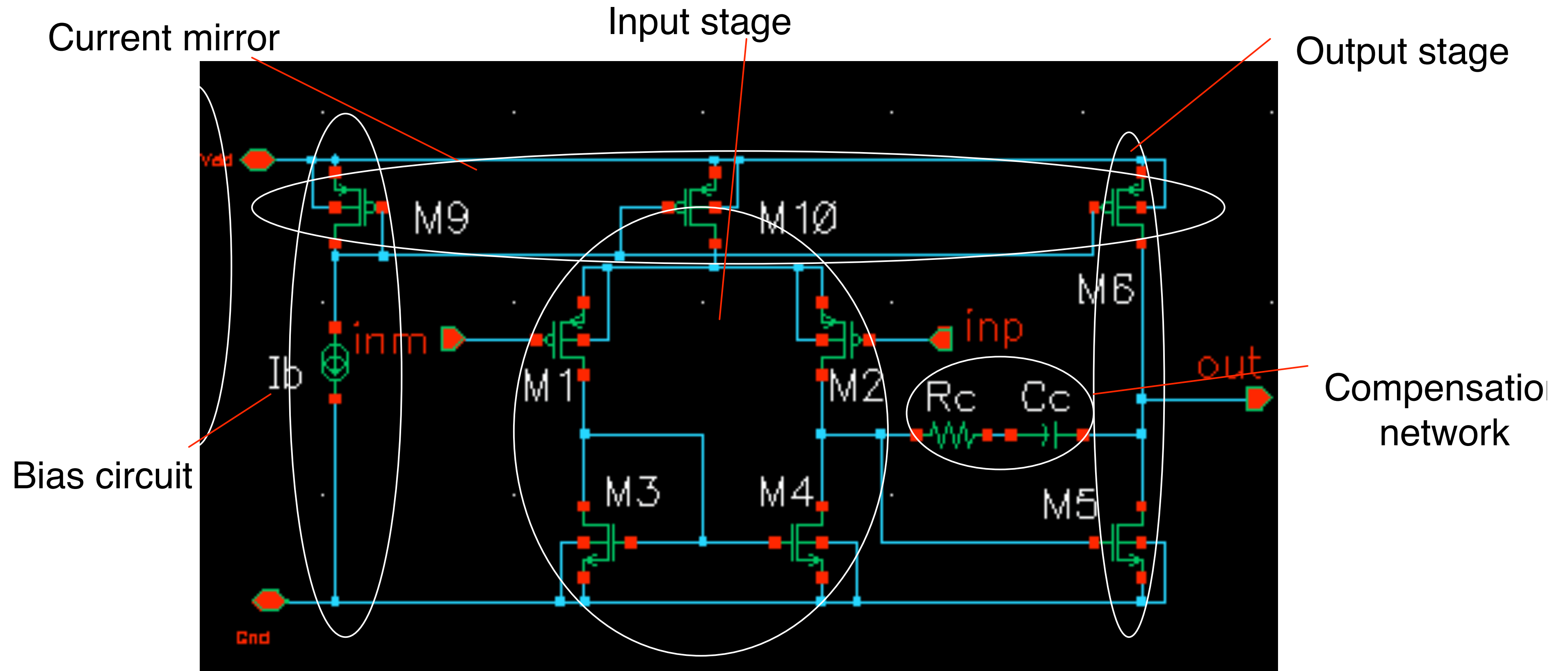
$\lambda=0.25V^{-1}$ @ L=300nm
$k_p=\mu_p \cdot C_{ox}=20\mu A/V^2$
$k_n=\mu_n \cdot C_{ox}=60\mu A/V^2$

Circuit Design - Experience 2

Two-stage opamp design

The solution

- The scheme

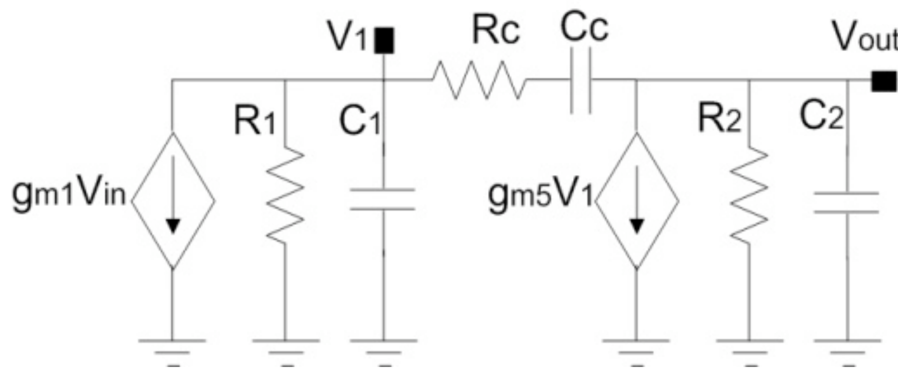


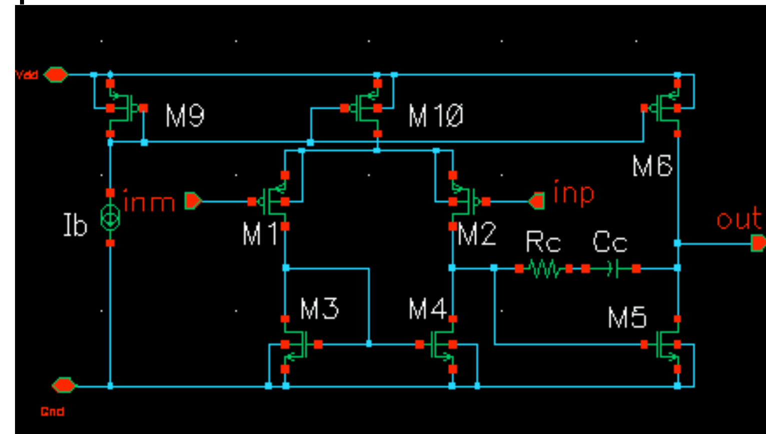
Circuit Design - Experience 2

Two-stage opamp design

The solution - Analysis

- Frequency response
  For the small signal analysis, consider this equivalent circuit





- In the small signal model:

$$R_1 = r_{ds2} || r_{ds4}$$

$$R_2 = r_{ds5} || r_{ds6}$$

$$C_1 = C_{db2} + C_{db4} + C_{gs5}$$

$$C_2 = C_{db5} + C_{ds6} + C_L$$

Circuit Design - Experience 2

Two-stage opamp design

The solution - Transfer function analysis

- Poles and zeros evaluation:
  - The dominant pole ω_p, the second pole ω_{p2} and the zero ω_z can be calculated

$$\omega_p = \frac{1}{g_{m5} \cdot R_1 \cdot R_2 \cdot Cc}$$

$$\omega_{p2} = \frac{g_{m5}}{C_1 + C_2}$$

$$\omega_z = -\frac{1}{\left(\frac{1}{g_{m5}} - Rc\right) \cdot Cc}$$

  - To compensate ω_{p2} with ω_z:

$$R_c = \frac{1}{g_{m5}} \cdot \left(1 + \frac{C_1 + C_2}{Cc}\right)$$

Circuit Design - Experience 2

Two-stage opamp design

The solution - Transfer function analysis

- The DC-gain (A_{tot}) is given by the product of the gain of the input stage (A_1) and output stage (A_2):

$$A_1 = g_{m1} \cdot R_1$$

$$A_2 = g_{m5} \cdot R_2$$

$$A_{tot} = A_1 \cdot A_2 = g_{m1} \cdot R_1 \cdot g_{m5} \cdot R2$$

- The Unity Gain Bandwidth (UGB) is given by the product (ω_{p1} x A_{tot}):

$$UGB = A_{tot} \cdot \omega_p = \frac{g_{m1}}{2\pi \cdot C_c}$$

Circuit Design - Experience 2

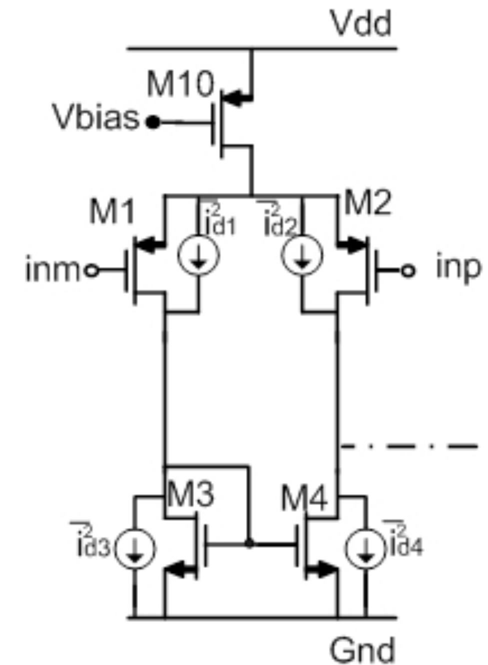
Two-stage opamp design

The solution - Noise analysis

- The output stage noise contributions are divided by the gain of the input stage (when referred at the input)
  - ➔ they can be neglected

- Only the thermal noise of the input stage MOS is considered
  - ➔ the input referred noise $\bar{v}^2_{i,noise}$ can be calculated as follows:

$$\overline{v^2_{i,noise}} = \frac{16}{3} \cdot kT \cdot \frac{1}{g_{m1}} \cdot \left(1 + \frac{g_{m3}}{g_{m1}}\right) = \frac{16}{3} \cdot kT \cdot \frac{1}{g_{m1}} \cdot \left(1 + \frac{V_{ov1}}{V_{ov3}}\right)$$



- Increasing V_{ov3}
  - ➔ the M_3 and M_4 noise contributions decrease

Circuit Design - Experience 2

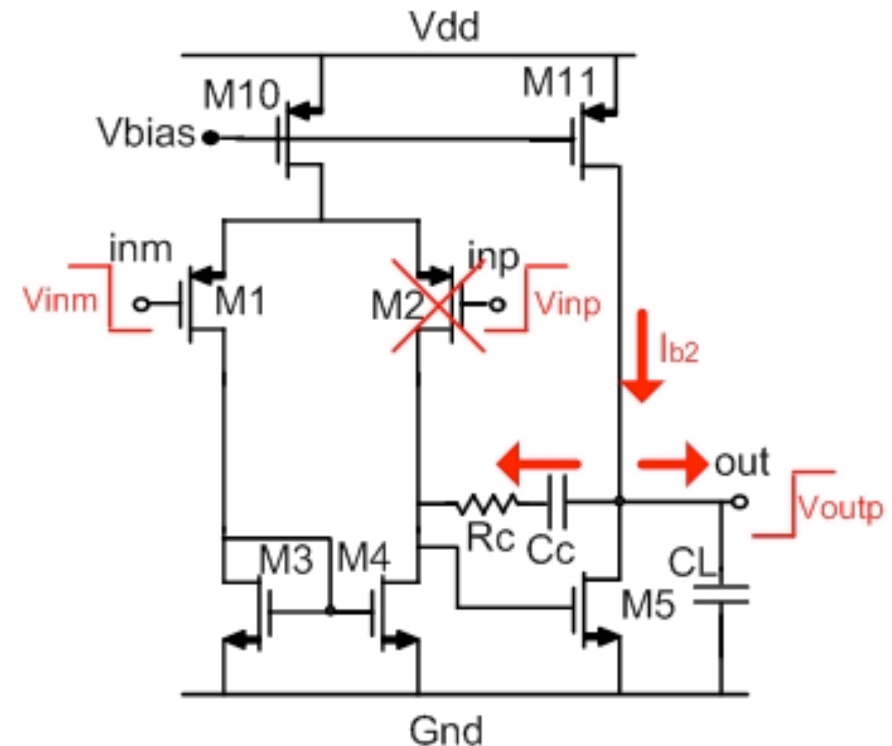
Two-stage opamp design

The solution - Slew-rate analysis

- The slew rate performance can be dominated by:
  - the input stage
  - the output stage

- For a positive output signal:
  - a positive input step is required
    - ➔ M2 results to be turned off
    - ➔ M4 enters the linear region
  - ➔The output stage current, I_{b2}, charges both C_c& C_L
  - ➔The positive slew-rate (SR^+) is:

$$SR^+ = \frac{I_{b2}}{C_c + C_L}$$



Circuit Design - Experience 2

Two-stage opamp design

The solution - Slew-rate analysis

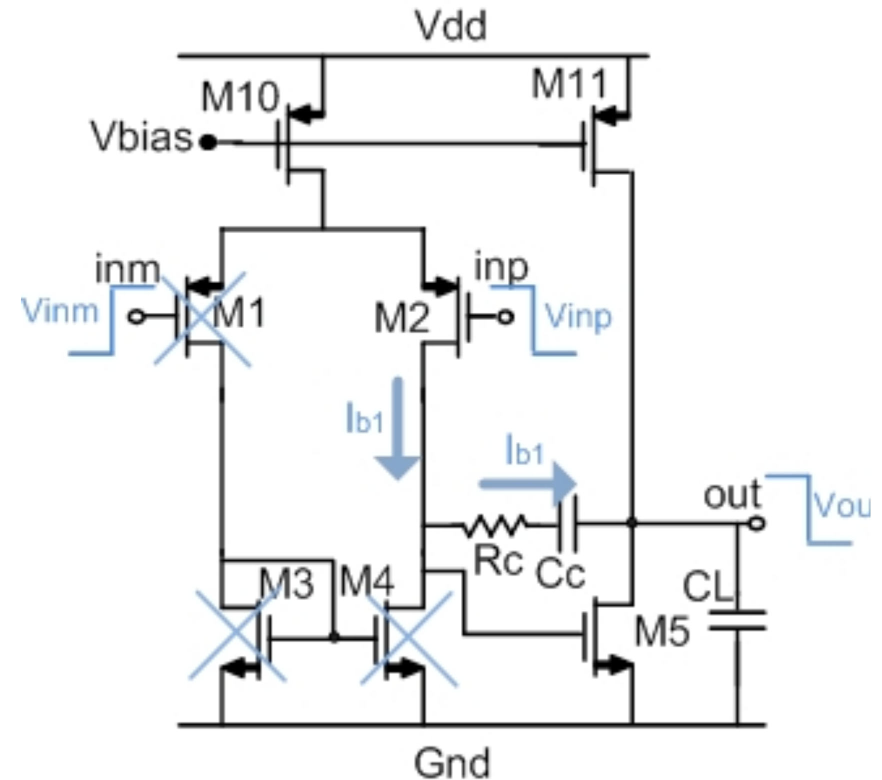
- For a negative output signal:
  a negative input step is required
  M2, M3 and M4 result to be turned off

  - ➔ All the input stage current, I_{b1},
    passes through M1
    discharges Cc
  - ➔ The negative slew-rate (SR^-) is

$$SR^- = \frac{I_{b1}}{C_c}$$

- SR^- can be expressed as a function of
  the input transistor overdrive (V_{ov1}), and of
  the unity gain bandwidth (UGB)

$$SR^- = \frac{I_{b1}}{C_c} = \frac{I_{b1}}{g_{m1}} \cdot UGB = V_{ov1} \cdot 2\pi \cdot UGB$$



Circuit Design - Experience 2

Two-stage opamp design: Systematic offset analysis

- To avoid systematic offset
  - ➔ V_{GS5} such that $I_{d5}=I_{b2}$

$$\rightarrow V_{GS5} = \sqrt{\frac{2 \cdot I_{b2}}{\mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_{M5}}} + V_{TH}$$

- When the input voltage is zero,
  - ➔ V_{DS} of M3 and M4 are equal for arguments of symmetry

$$\rightarrow \quad V_{GS5} = V_{DS4} = V_{GS3}$$

- Since $V_{GS3} = \sqrt{\frac{2 \cdot I_{b1}}{\mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_{M3}}} + V_{TH}$

$$\rightarrow \quad V_{GS5} = V_{GS3}$$

$$\rightarrow \quad \frac{2 \cdot I_{b2}}{\mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_{M5}} = \frac{I_{b1}}{\mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_{M3}}$$

Circuit Design - Experience 2

Design procedure: input stage design

- From the slew-rate analysis, assuming $SR = SR^{+} = SR^{-}$:

$$V_{ov1} = \frac{SR}{2\pi \cdot UGB} \approx 100mV$$

- From the noise analysis, assuming $V_{ov3}=3 \cdot V_{ov1}$
  - To reduce the noise contributions due to M3 and M4:

$$\overline{v_{i,noise}^{2}} = \frac{16}{3} \cdot kT \cdot \frac{1}{g_{m1}} \cdot \left(1 + \frac{V_{ov1}}{V_{ov3}}\right) = \frac{16}{3} \cdot kT \cdot \frac{1}{g_{m1}} \cdot \left(1 + \frac{1}{3}\right)$$

$\rightarrow g_{m1} \approx 1.2mA/V$

$g_{m1} = I_{b1} / V_{ov1} \rightarrow I_{b1} = g_{m1} \cdot V_{ov1} = 120\mu A$

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Circuit Design - Experience 2

Design procedure: input stage design

- Design of the input stage MOS:

$$\left(\frac{W}{L}\right)_{M1} = \left(\frac{W}{L}\right)_{M2} = \frac{I_{d1}}{\frac{1}{2}\cdot\mu_p\cdot C_{ox}\cdot V_{ov1}^2} = \frac{I_{b1}}{\frac{1}{2}\cdot\mu_p\cdot C_{ox}\cdot V_{ov1}^2} = 600$$

$$\left(\frac{W}{L}\right)_{M3} = \left(\frac{W}{L}\right)_{M4} = \frac{I_{d3}}{\frac{1}{2}\cdot\mu_p\cdot C_{ox}\cdot V_{ov3}^2} = \frac{I_{b1}}{\mu_p\cdot C_{ox}\cdot V_{ov3}^2} = 22$$

- The MOS length L is decided on the base of considerations on:
  - Input offset
  - Flicker noise
  - Output MOS impedance
- Nanometer technologies
  - Input offset and 1/f noise minimization
    - ➔ non-minimum input stage MOS lengths
  - Larger output impedance
    - ➔ longer MOS device
- ➔ Assuming L=300nm for all the MOS:

$$W_1 = 150\mu m \qquad W_2 = 7\mu m$$

Circuit Design - Experience 2

Design procedure: compensation network and output stage design

- From the UGB expression:

$$C_C = \frac{g_{m1}}{2 \cdot \pi \cdot UGB} \approx 2pF$$

- From the SR⁻ expression:

$$I_{B2} = SR^{+} \cdot (C_C + C_L) = 240\mu A$$

- From the systematic offset analysis:

$$\left(\frac{W}{L}\right)_{M5} = \left(\frac{W}{L}\right)_{M13} \cdot \frac{I_{B2}}{I_{B1}/2} = \left(\frac{W}{L}\right)_{M3} \cdot 4$$

- Assuming L_5 = 300nm ➔ W_5 = 28µm
  - For the compensation resistor design R_C

$$g_{m5} = \sqrt{2 \cdot \mu N \cdot Cox \cdot \left(\frac{W}{L}\right)_{M13} \cdot I_{B2}} = 1.64\ mA/V$$

$$\rightarrow \quad R_C = \frac{1}{g_{m5}} \cdot \left(1 + \frac{C_1 + C_2}{C_C}\right) \approx \frac{1}{g_{m5}} \cdot \left(1 + \frac{C_L}{C_C}\right) \approx 1.2k\Omega$$

Circuit Design - Experience 2
Design procedure: DC gain verification

- The opamp DC-gain requirement is 50dB
- The opamp DC-gain (A_{tot}) can be evaluated

$$A_{tot} = A_1 \cdot A_2 = g_{m1} \cdot R_1 \cdot g_{m5} \cdot R2$$

$$g_{m1} = 1.2mA/V$$

$$g_{m5} = 1.64mA/V$$

$$R_1 = r_{ds2} || r_{ds4} = \frac{1}{\lambda \cdot I_{B1}} = 30k\Omega$$

$$R_2 = r_{ds5} || r_{ds6} = \frac{1}{2 \cdot \lambda \cdot I_{B2}} = 7.5k\Omega$$

$$\rightarrow A_{tot} = 432 = 53dB > 50dB$$

- The opamp DC-gain requirements is satisfied
- Nanometer technology
  - The low MOS resistances limit the achievable gain

Circuit Design - Experience 2

Design procedure: current mirrors design

- The Pelgrom's formula allows to estimate the mismatch of the current-mirrors:

$$\left(\frac{\sigma_{\Delta I_{DS}}}{I_{DS}}\right)^2 \approx \frac{4\cdot\sigma_{V_{TH}}^2}{(V_{GS}-V_{TH})^2} = \frac{4\cdot A_{V_{TH}}^2}{W\cdot L\cdot V_{ov}^2}$$

  - A_{vt} is a technology parameter

- A non-minimum V_{ov} value is desirable to limit the mismatch between the current-mirrors V_{ov}=100mV is assumed

$$\rightarrow \frac{W}{L}_{M9} = \frac{W}{L}_{M10} = \frac{I_{B1}}{\frac{1}{2}\mu_P C_{ox}\left(V_{GS}-V_{TH}\right)^2} = 1200$$

$$\rightarrow \frac{W}{L}_{M11} = \frac{I_{B2}}{\frac{1}{2}\mu_P C_{ox}\left(V_{GS}-V_{TH}\right)^2} = 2400$$

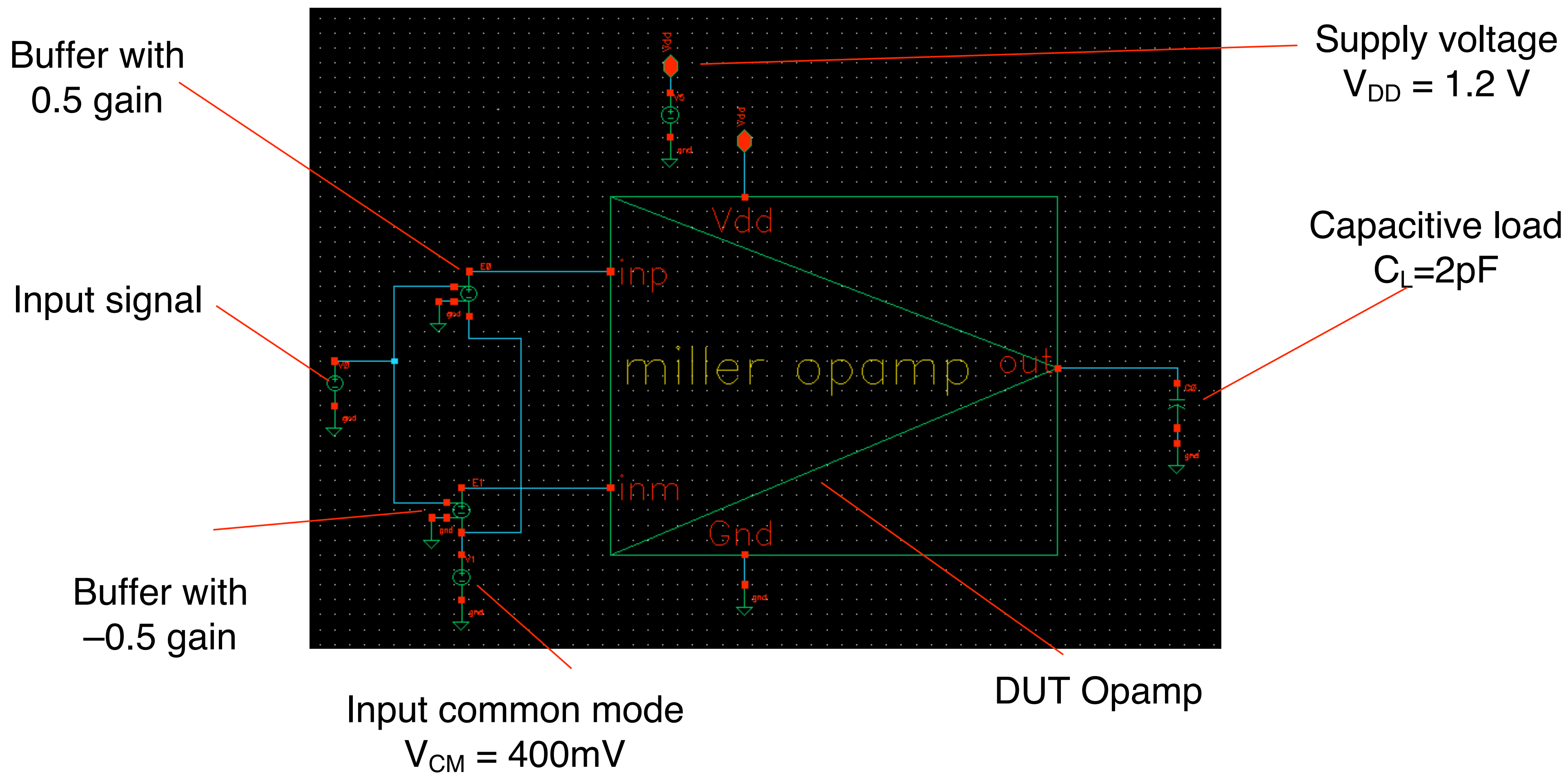
- Assuming L=0.3µm

$\rightarrow W_{M9}=W_{M10}=360\mu m \qquad W_{M11}=720\mu m$

Circuit Design - Experience 2

Two-stages opamp design

Solution – Set-up for noise, freq. response and operating point evaluation



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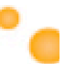
Circuit Design - Experience 2

Two-stage opamp design

Solution – The operating point

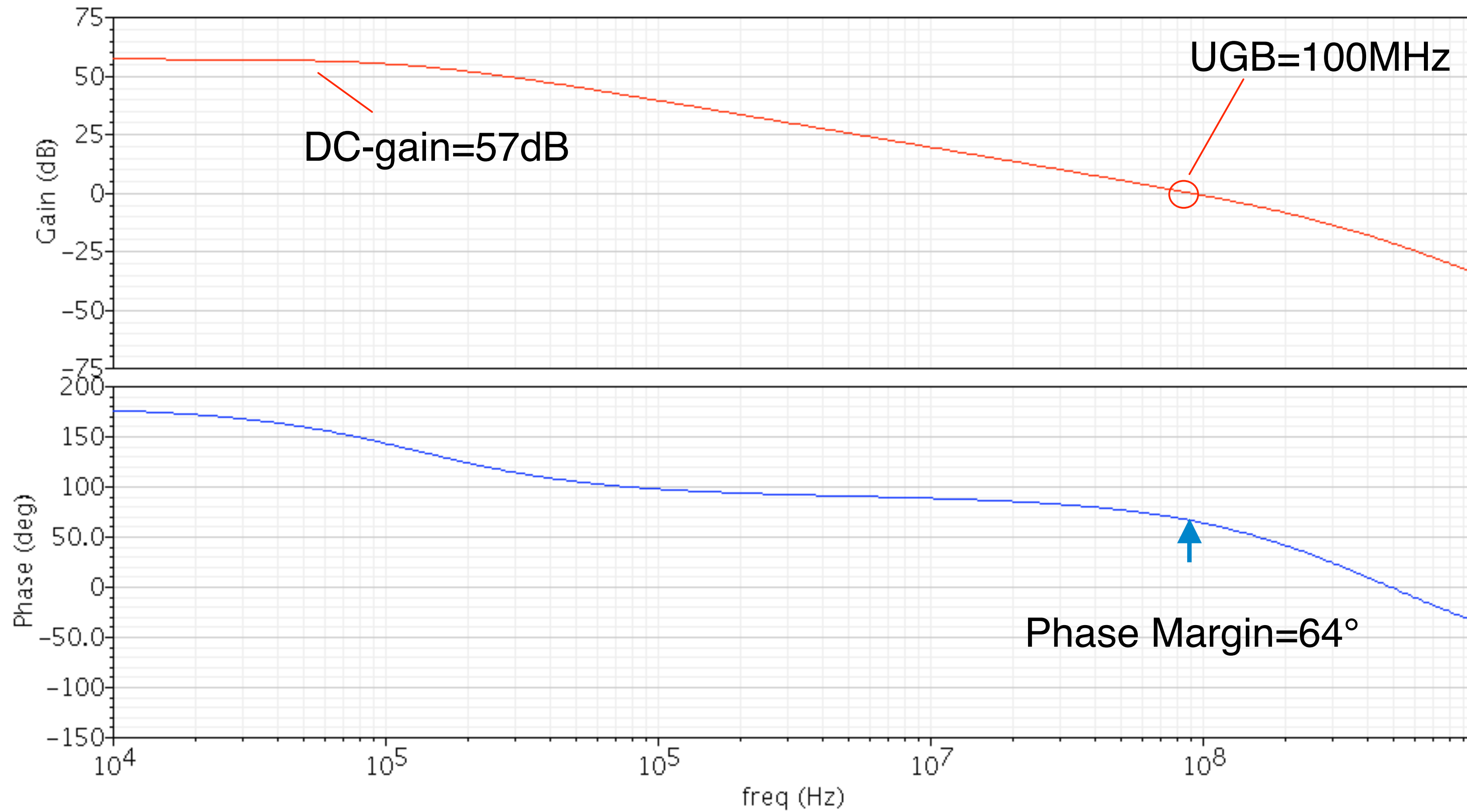
device	M9	M10	M6	M2	M1	M5	M3	M4
W	360um	360um	720um	150um	150 um	28 um	7 um	7 um
L	300nm	300nm	300nm	300nm	300nm	300nm	300nm	300nm
ids	120uA	117 uA	268 uA	58 uA	58 uA	268 uA	58 uA	58 uA
vds	434 mV	356 mV	789 mV	263 mV	263 mV	411 mV	581 mV	581mV
vdsat	58mV	58mV	58mV	61mV	61mV	137mV	132mV	132mV
vgs	434mV	434mV	434mV	444mV	444mV	581mV	581mV	581mV
vth	466mV	466mV	436mV	466mV	466mV	502mV	510mV	510mV
gds	42uA/V	45uA/V	78.4uA/V	28.2uA/V	28.2uA/V	14uA/V	83uA/V	83uA/V
gm	2.8mA/V	2.7mA/V	6.1mA/V	1.3mA/V	1.3mA/V	0.71mA/V	3.2mA/V	3.2mA/V
Cdd	166fF	171fF	297fF	74fF	74fF	14fF	4.4fF	4.4fF
Cgg	659fF	67fF	1.3pF	287fF	287fF	8fF	20fF	20fF
Css	612fF	611fF	1.2pF	268fF	268fF	83fF	21fF	21fF



Circuit Design - Experience 2

Two-stage opamp design

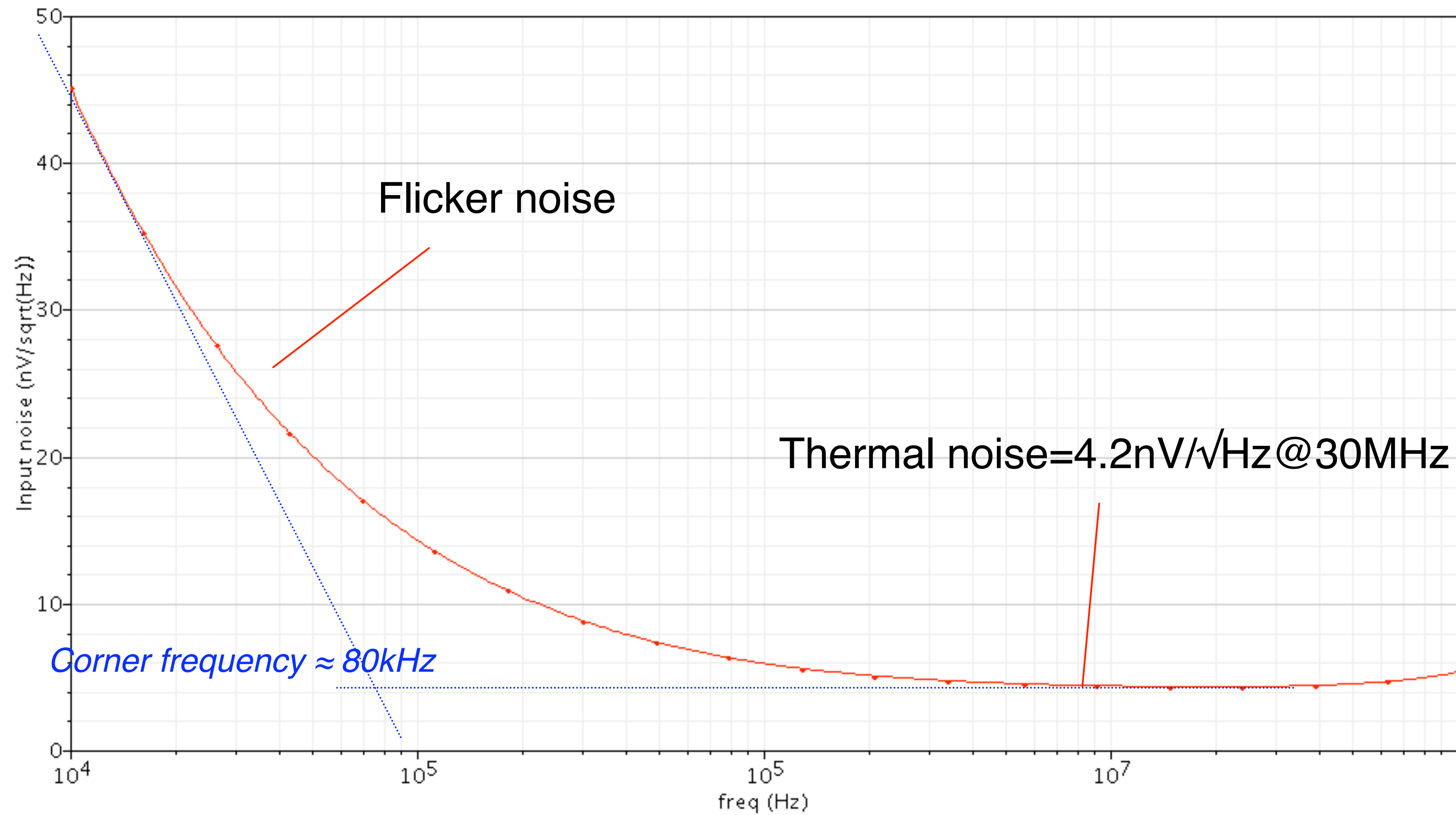
Solution – Frequency response



Circuit Design - Experience 2

Two-stage opamp design

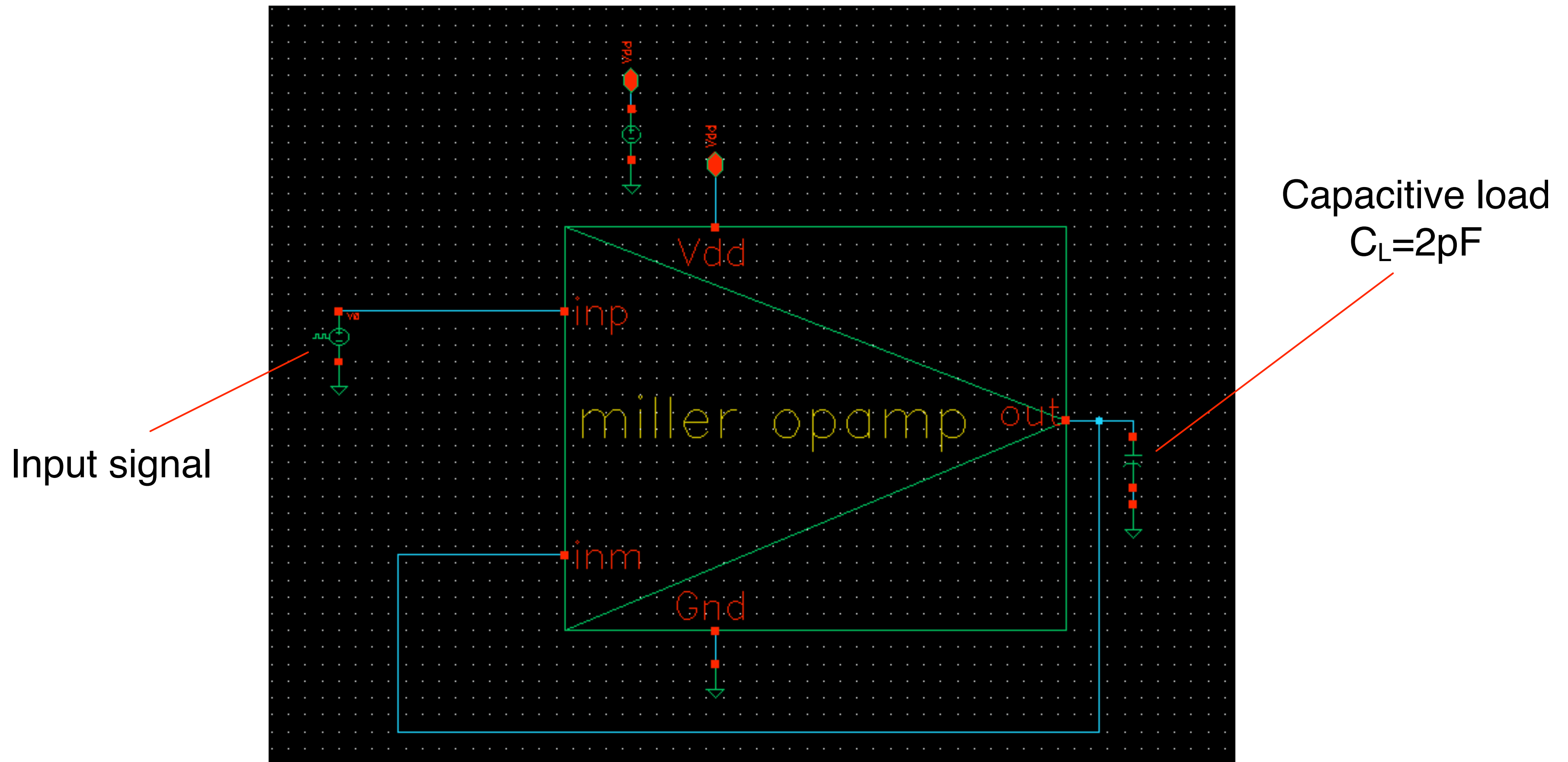
Solution – Noise performance



- 1/f noise is still important at MHz frequencies

Circuit Design - Experience 2

Two-stage opamp design: Solution – Set-up for the SR evaluation

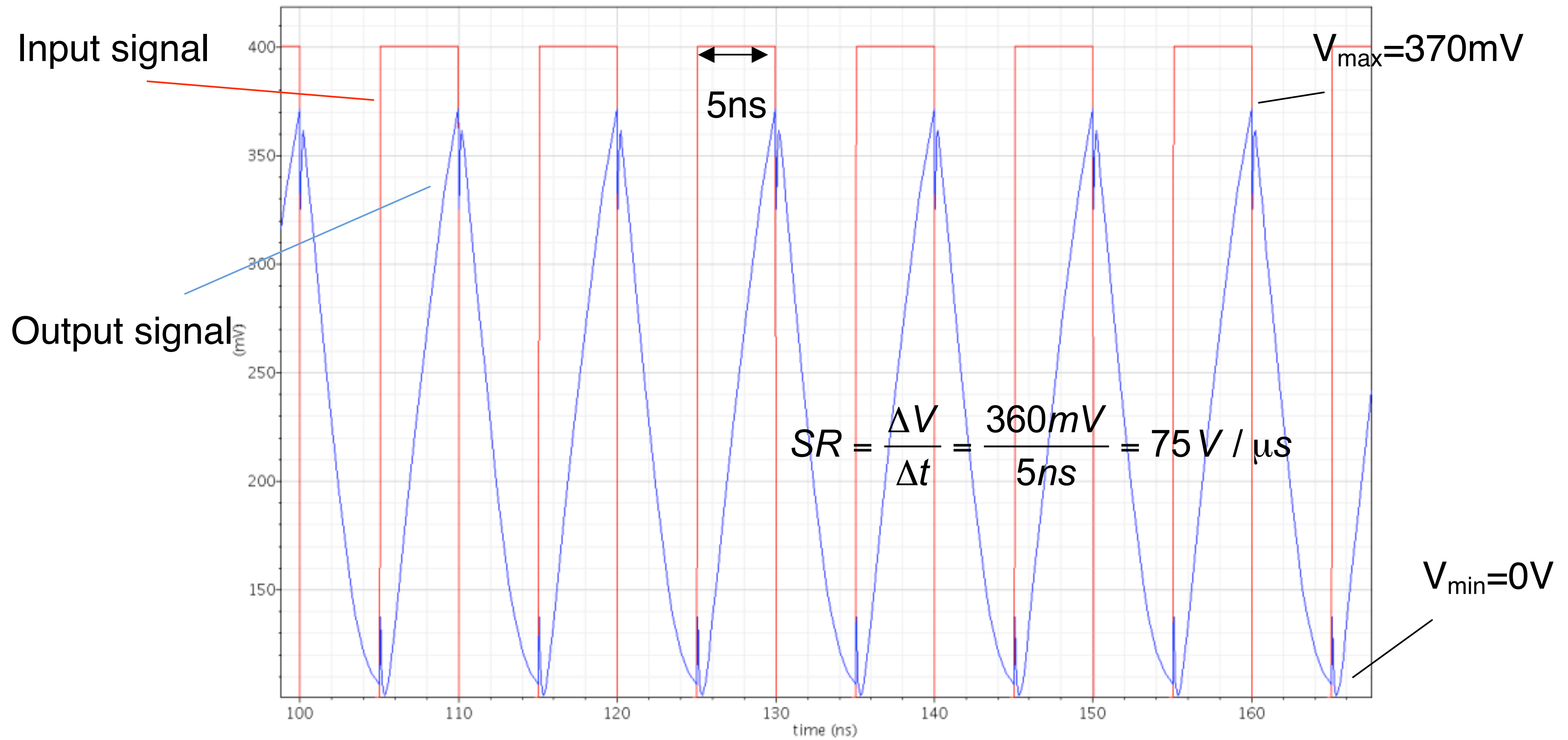


- The opamp is connected in buffer configuration

Circuit Design - Experience 2

Two-stage opamp design

Solution – SR perfomance



$$SR = \frac{\Delta V}{\Delta t} = \frac{360mV}{5ns} = 75\,V/\mu s$$

Circuit Design - Experience 2

Two-stage opamp design

Solution – Performance Summary

Parameter	Simulation results	Target performance
Gain	**57dB**	**>50dB**
UGB	**100MHz**	**100MHz**
Input referred noise	**4.2nV/√Hz**	**5nV/√Hz**
SR	**75V/μs**	**63V/μs**