Special Problem 4.5-1

In the **amplifier** below:

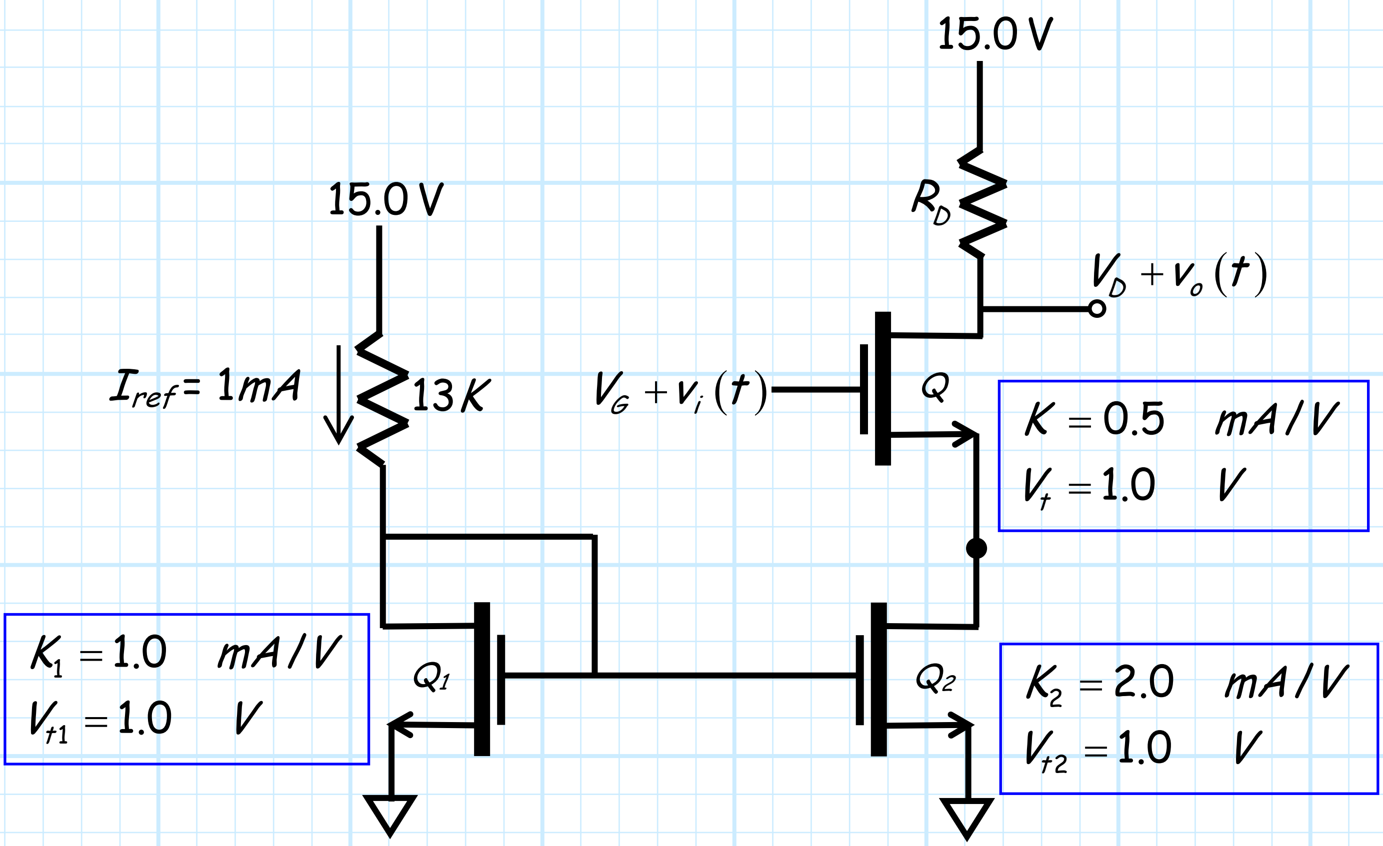
1. The transistor Q_1 is in **saturation**, with drain current $I_{ref} = 1.0 mA$.
2. **None** of the three transistors are **identical**.

Determine then the proper value of:

a) the **DC gate voltage** V_G and,
b) the **drain resistor** R_D ,

so that the magnitude of an **undistorted**, **sinusoidal** small-signal output can be as large as possible (i.e., if $v_o(t) = V_s \sin \omega t$, then magnitude V_s can be as large as possible.).

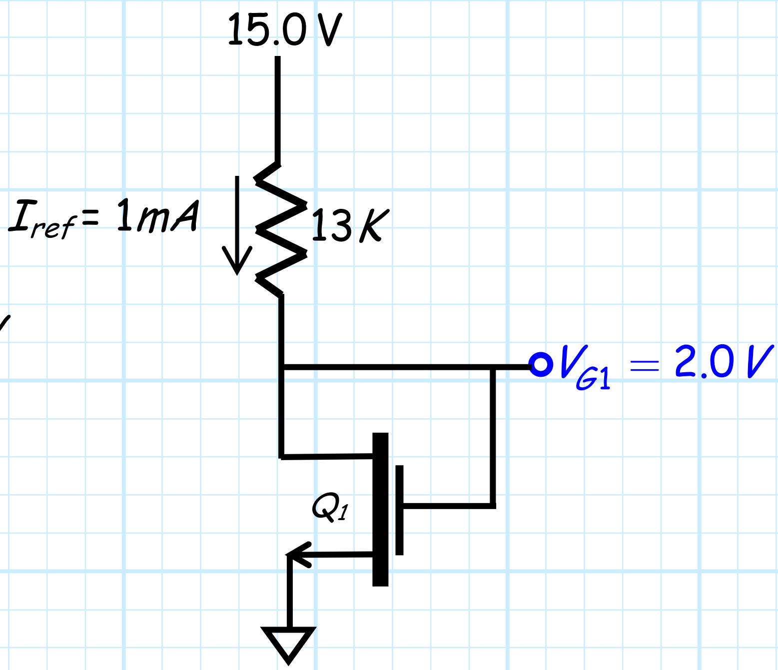
Hint: This is a **DC bias problem**, no small-signal analysis is required!



Solution

From **KVL**, we find that:

$$V_{G1} = 15 - 13(1) = 2.0$$



Note then that:

$$V_{GS1} = 2.0 - 0.0 = 2.0\,V$$

Therefore:

$$\begin{aligned} I_{D1} &= K_1 \left(V_{GS1} - V_{t1}\right)^2 \\ &= 1.0(2.0 - 1.0)^2 \\ &= 1.0\ mA \end{aligned}$$

And so we have confirmed that:

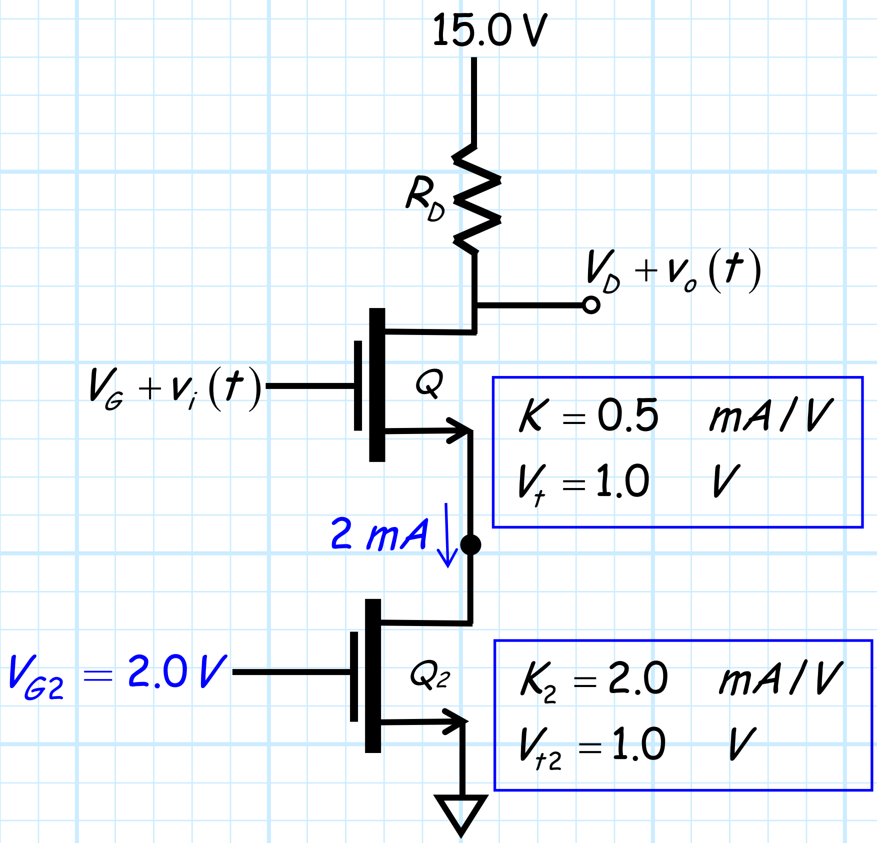
$$I_{ref} = I_D = 1.0\ mA \quad !!!$$

Now, the **gate** terminal of both Q_1 and Q_2 are connected, so that:

$$V_{G1} = V_{G2} = 2.0\,V$$

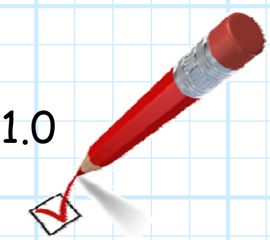
Thus, **if** transistor Q_1 is in **saturation**, its drain current is:

$$\begin{aligned} I_{D2} &= K_2 \left(V_{GS2} - V_{t2}\right)^2 \\ &= 2.0(2.0 - 1.0)^2 \\ &= 2.0\ mA \end{aligned}$$



Of course, in order for Q_2 to be in **saturation**, we know that a channel must be **induced**:

$$V_{GS2} = 2.0 > V_{t2} = 1.0$$



And also, the drain-to-source voltage V_{DS2} must be **greater** than the excess gate voltage of Q_2:

$$V_{DS2} \geq V_{GS2} - V_{t2} = 2.0 - 1.0 = 1.0$$

Since the **source** terminal of Q_2 is at **ground** potential (i.e., $V_{S2} = 0$), the above equation means that Q_2 is in saturation **only if**:

$$V_{D2} > 1.0\,V$$

Q: *So **what is** the value of voltage V_{D2} ? **Is** transistor Q_2 in saturation?*

A: That's the **point** of this **bias design problem**! We need to **determine** the values of resistor R_D and gate voltage V_G that will ensure that $V_{D2} \geq 1.0\,V$!

Q: *Aren't there **many** values of R_D and V_G for which $V_{D2} > 1.0\,V$?*

A: Absolutely!

But, there is only **one** of these solutions for which the "magnitude of an **undistorted**, **sinusoidal** small-signal output can be as large as possible".

We know that the **largest** value the total output voltage $v_O(t)$ can be (without causing transistor Q to cutoff) is:

$$L_+ = 15.0\,V$$

Now, we likewise want to **minimize** the "**floor**" voltage L_-. We know that this value is:

$$L_- = V_G - V_t$$

Thus, we need to make the **DC gate voltage** V_G as **low** as possible!

Q: *But **how small** can we make it?*

A: Well, we know from **KCL** that:

$$I_D = I_{D2} = 2.0\,mA$$

Where, **if** transistor Q is in **saturation**, this drain current must be:

$$2.0\,mA = I_D = K\left(V_{GS} - V_t\right)^2 = 0.5\left(V_{GS} - 1.0\right)^2$$

Therefore:

$$V_{GS} = \sqrt{\frac{2.0}{0.5}} + 1.0 = 3.0\,V$$

So:

$$V_G = V_S + 3.0$$

Thus, to **minimize** the gate voltage (and thus minimize L_-), we need to minimize the **DC source voltage** V_S—and we **know exactly** how low we can make the source voltage!

Recall that for transistor Q_2 to remain in **saturation**, we found that:

$$V_{D2} \geq 1.0\,V$$

And, it is apparent from the circuit schematic that:

$$V_{D2} = V_S$$

Therefore, we conclude that, for the transistor Q_2 to be in **saturation**:

$$V_S \geq 1.0\,V$$

Obviously then, the **lowest** possible value of the **DC source voltage** is:

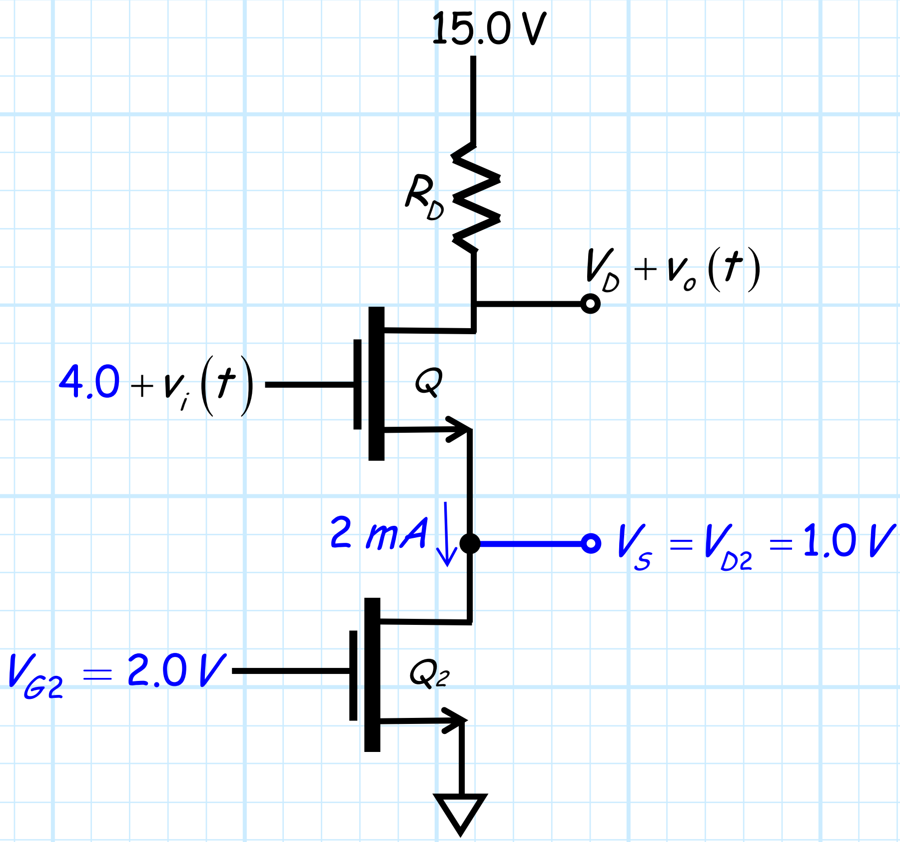
$$V_S = 1.0\,V$$

And so the **lowest** possible **DC gate voltage** is:

$$V_G = V_S + 3.0 = 1.0 + 3.0 = \underline{\underline{4.0\,V}}$$

And thus:

$$L_- = V_G - V_t = 4.0 - 1.0 = 3.0\,V$$



Now, since the **small-signal** output voltage is sinusoidal (i.e., **symmetric**), the **DC** output voltage $V_O = V_D$ should be "**half-way**" between ceiling L_+ and floor L_-:

$$V_O = V_D = \frac{L_+ + L_-}{2} = \frac{15+3}{2} = 9.0\ V$$

Now, from **Ohm's Law**:

$$R_D = \frac{15 - V_D}{I_D} = \frac{15-9}{2} = \frac{6}{2} = \underline{\underline{3.0\ K\Omega}}$$

Finally, we should **also** note that:

$$V_G = 4.0 > 1.0 = V_t$$

and

$$V_{DS} = V_D - V_S = 9.0 - 1.0 = 8.0 > 2.0 = V_{GS} - V_t$$

Transistor Q is indeed in **saturation**!