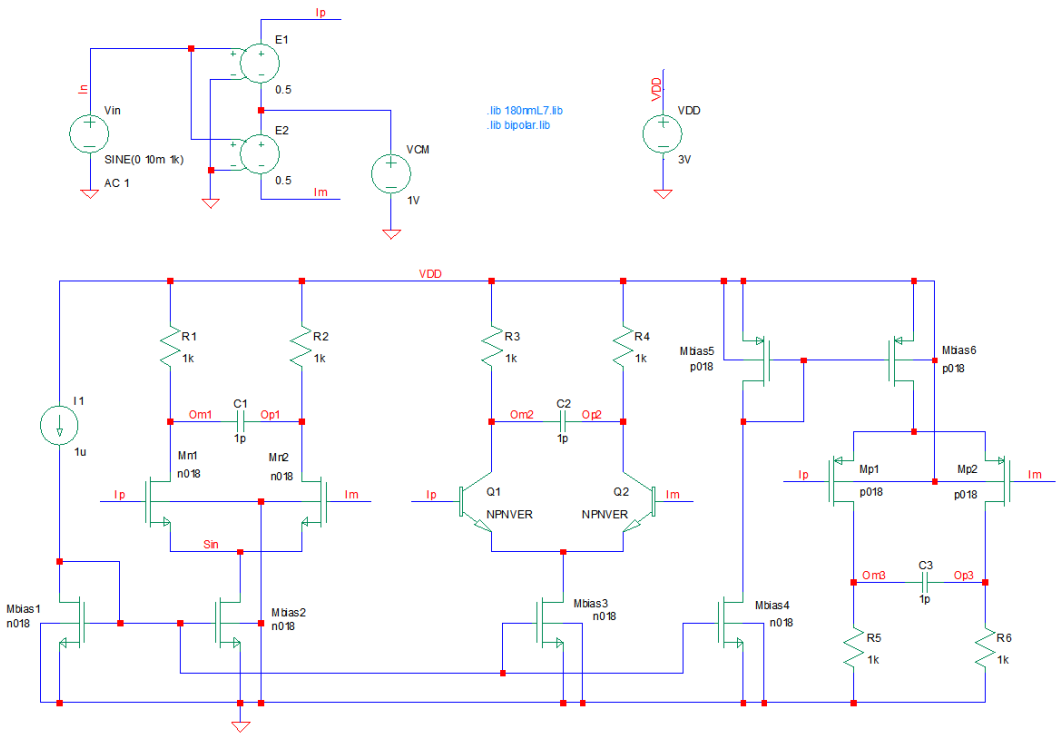
1. The differential amplifier with resistive load

The test schematic (*ampdif-sarcR.asc*):



Proposed exercises:

1. Design the amplifier for *GBW*>10MHz and C_L=5pF. In order to fulfill the design specifications in spite of the parasitic effects (capacitances, g_{mb}), the parameters should be considered 1.5–2 times larger (for example, use *GBW*=30MHz in hand calculations).

Hints:

a. from the expression of the unity-gain bandwidth (*GBW*) calculate the small signal transconductance G_m of the amplifier. The transconductance g_m of the input transistors is then equal to $2G_m$;
b. choose a usual value for the V_{DSat} voltage of the input transistors M_{n1} and M_{n2} (for example 200mV);
c. from the definition of the transconductance, a function of the drain current and the V_{DSat} voltage, determine the current flowing through the input differential pair and the branches of the current mirror M_{bias1}-M_{bias2};
d. calculate the geometry *W*/*L* of the transistor by considering V_{DSat} and V_{Th}. Also determine the lowest allowed input common mode voltage V_{inCM}, required for biasing. Choose V_{inCM} that maximizes the signal swing (for example V_{DD}/2);
e. Set the output common mode voltage to be equal to V_{inMC};
f. From V_{outCM} and the current flowing through the branches of the differential amplifier calculate the resistances R.

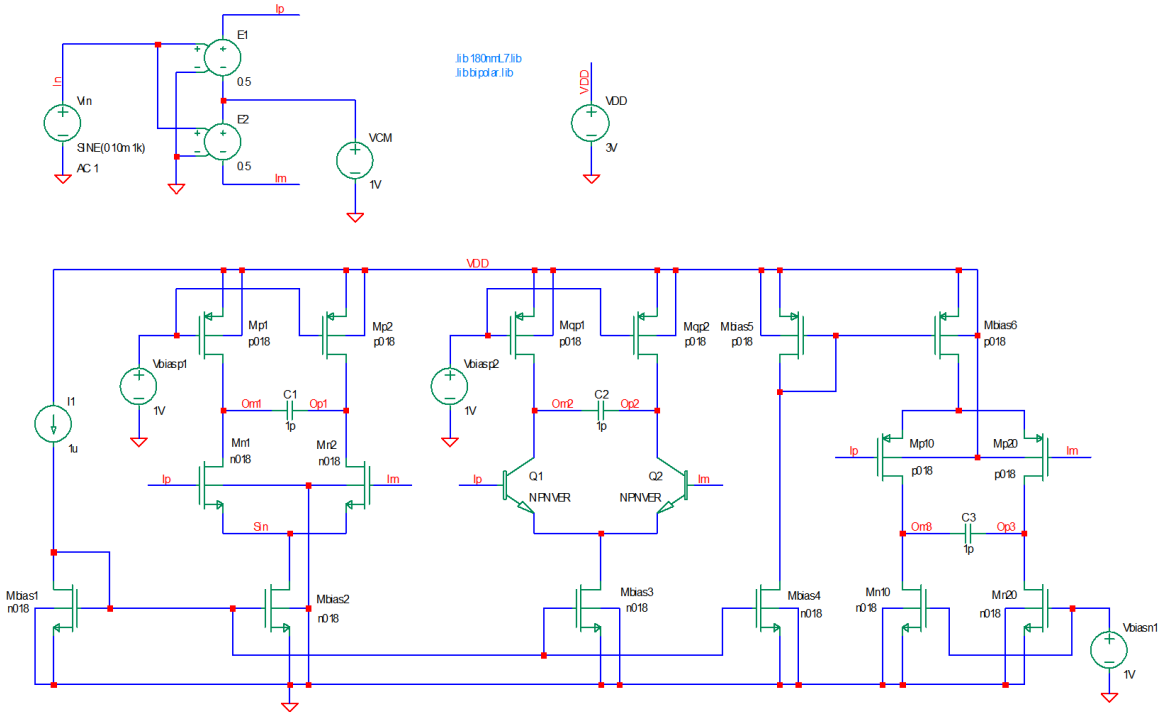
2. Validate the operating points of the components and adjust the circuit to match hand calculations. Fill the following table:

	V_{GS}	V_{DS}	V_{Th}	V_{DSat}	I_D	g_m	r_{DS}
M_{n1}							
M_{n2}							
M_{bias1}							
M_{bias2}							

3. Use the equations from the lecture notes and the small signal parameters to calculate the low frequency gain A_0 and the unity gain bandwidth *GBW* of the amplifier;
4. Estimate the output voltage range of the amplifier and validate the found values by plotting the DC transfer characteristic V_{out}/V_{in};
5. Plot the magnitude and phase responses of the amplifier. Measure A_0, the frequency of the dominant pole (f_p=*BW*) and the unity gain bandwidth *GBW*. Notice the presence of the parasitic right half plane zero caused by the Miller effect and compare the measurements with the values found in hand calculations;
6. Simulate the transient response of the amplifier for a sine wave input with 1kHz frequency and the amplitude set to 50mV, 150mV and then 300mV. At which output amplitude does the clipping occur if the input amplitude is 300mV?
7. Compare the design algorithm of the differential amplifier with the one used for the fundamental common source amplifier with resistive load.
8. Repeat the exercises 1-7 for all the amplifiers in the test schematic. Compare the current consumption and the low frequency gain of the bipolar input vs. the MOS input stages. Explain the observations.

2. The differential amplifier with current source load

The test schematic (*ampdif-sarcsrs.asc*):



Proposed exercises:

9. Design the NMOS input amplifier for *GBW*>10MHz and C_L=5pF.

Designing the amplifier means to choose the bias currents, the V_{biasp1} voltage and all transistor geometries for which the circuit fulfills the worst case specifications.

In the first step the unity-gain bandwidth can be related to the load capacitance and the small signal transconductance of the input pair. The equation leads to the expression of the transconductance. In order to fulfill the worst case design specifications in the presence of the parasitic effects, the unity gain bandwidth is typically oversized with a factor equal to 1.5-2 compared to the lowest allowed specification. Therefore, in calculations *GBW* is considered to be 20MHz.

$$GBW = \frac{G_m}{2\pi C_L} \Rightarrow G_m = 2\pi C_L \cdot GBW = 2\pi \cdot 5 \cdot 10^{-12} \cdot 20 \cdot 10^6 = 630\mu S$$

The transconductance of the input transistors is then

$$G_m = \frac{g_{m-n1,2}}{2} \Rightarrow g_{m-n1,2} = 2G_m = 1.26mS$$

In the second step the $V_{DSat\text{-}n1,2}$ voltage is set to a usual value, for example 200mV. The bias current I_B of the differential stage is calculated as

$$g_{m-n1,2} = \frac{2I_{D-n1,2}}{V_{DSat-n1,2}} = \frac{I_B}{V_{DSat-n1,2}} \Rightarrow I_B = g_{m-n1,2} \cdot V_{DSat-n1,2} = 1.26mS \cdot 200mV \cong 250\mu A$$

In the third step the parameters corresponding to the reference operating point are used to calculate the NMOS transistor geometries. For M_{bias1} with I_D=50µA and V_{DSat}=200mV it results:

$$\left(\frac{W}{L}\right)_{bias1} = \left(\frac{W}{L}\right)_{ref} \cdot \frac{I_D}{I_{D-ref}} \cdot \left(\frac{V_{DSat-ref}}{V_{DSat}}\right)^2 = \frac{5}{1} \cdot \frac{50}{50} \cdot \left(\frac{240}{200}\right)^2 = \frac{7.2\mu}{1\mu}$$

According to the width and the length of M_{bias1}, the source/drain areas and perimeters are

$$\begin{cases} AS = AD = 7.2\mu m \cdot 0.2\mu m = 1.44\mu m^2 \\ PS = PD = 2(7.2\mu m + 0.2\mu m) = 14.8\mu m \end{cases}$$

The transistor M_{bias2} provides the current I_B=250µA to the differential stage while its V_{DSat} voltage is 200mV. It results that the geometry of this transistor will be 5 times larger than M_{bias1}. Scaling the geometry is achieved by simply setting the multiplier parameter of M_{bias2} to *m*=5.

The transistors of the differential input pair can be designed in a similar manner, considering that the current flowing through each will be 125µA. The geometries are

$$\left(\frac{W}{L}\right)_{n1,2} = \frac{18\mu}{1\mu} \; ; \; AS = AD = 3.6\mu m^2 \; ; \; PS = PD = 36.4\mu m$$

Similarly, the PMOS load transistors can be designed as

$$\left(\frac{W}{L}\right)_{p1,2} = \frac{62\mu}{1\mu} \; ; \; AS = AD = 12.4\mu m^2 \; ; \; PS = PD = 124\mu m$$

In the fourth step the bias voltage V_{biasp1} can be calculated from Kirchhoff's voltage law.

$$V_{biasp1} = V_{DD} - V_{SGp1,2} = V_{DD} - V_{DSat-p1,2} - V_{Thp} = 3V - 200mV - 450mV = 2.35V$$

Finally, the input and the output common mode voltages are determined by considering transistor biasing and the signal swing. The lowest allowed input common mode voltage must insure the correct biasing of the input transistors and of the current source M_{bias2}.

$$V_{inCM-\min} = V_{GS-n1,2} + V_{DS-bias2} = V_{DSat-n1,2} + V_{Thn} + \Delta V_{Thn} + 1.5 \cdot V_{DSat-bias2} = \\ = 200\text{mV} + 450\text{mV} + 100\text{mV} + 300\text{mV} = 1.05\text{V}$$

where V_{Thn} is the NMOS threshold voltage for V_{BS}=0, while ΔV_{Thn} compensates the body effect and the increased threshold voltage with V_{BS}. The drop $1.5V_{DSat\text{-}bias2}$ across the current source M_{bias2} fulfills the V_{omin} requirement of the biasing current mirror with a margin.

For simplified calculations it can be assumed that V_{inCM}=V_{outCM} and both voltages will be equal to V_{DD}/2=1.5V.

10. Validate the operating points of the components and adjust the circuit to match hand calculations. Fill the table with the small signal parameters.

The validation of the operating points is done by running an *.OP* analysis. After reading the node voltages and branch currents returned by the simulator it can be seen that the drain-source voltage of the transistor M_{bias2} is approximately 98mV indicating that the device is biased in the linear region. Furthermore, the output common mode voltage is found to be 121mV, which leads to the failure of the entire differential amplifier.

The encountered biasing problems can be eliminated by shifting the output common mode voltage to 1.5V through subsequent adjustments of the source V_{biasp1} (the same method has been used for the fundamental common source amplifier with current source load). The procedure leads to V_{biasp1}=2.2826V for which V_{op1}=V_{om1}=1.5V.

Comment: Adjusting the V_{biasp1} source with tens or hundreds of µV precision is only a simulation artifice that allows the correct biasing and the testing of the amplifier without further circuitry. In real applications the V_{biasp1} voltage is electronically pulled to its right value by means of negative feedback.

	V_{GS}	V_{DS}	V_{Th}	V_{DSat}	I_D	g_m	r_{DS}
$M_{n1,2}$	849mV	852mV	618mV	218mV	125µA	894µS	98kΩ
$M_{p1,2}$	717mV	1.5V	450mV	195mV	125µA	897µS	72kΩ
M_{bias1}	665mV	665mV	450mV	203mV	50µA	379µS	218kΩ
M_{bias2}	665mV	651mV	450mV	203mV	250µA	1.89mS	43.5kΩ

11. Use the equations from the lecture notes and the small signal parameters to calculate the low frequency gain A_0 and the unity gain bandwidth *GBW* of the amplifier;

The low frequency gain is estimated according to the equation

$$A_0 = G_m \cdot R_{out} = \frac{g_{m-n1,2}}{2} \cdot 2\left(r_{DS-n1,2} \parallel r_{DSp1,2}\right) = 894\mu\text{S} \cdot \left(98\text{k}\Omega \parallel 72\text{k}\Omega\right) \cong 37.1 \rightarrow 31.4\text{dB}$$

The corresponding dominant pole frequency and unity-gain bandwidth are

$$BW \cong \frac{1}{2\pi R_{out} C_L} = \frac{1}{2\pi \cdot \left(2 \cdot 41.5\text{k}\Omega\right) \cdot 5\text{pF}} \cong 385\text{kHz}$$

$$GBW \cong \frac{g_{m-n1,2}}{2 \cdot 2\pi C_L} = \frac{447\mu\text{S}}{2\pi \cdot 5\text{pF}} \cong 14.3\text{MHz}$$

12. Estimate the output voltage range of the amplifier and validate the found values by plotting the DC transfer characteristic V_{out}/V_{in};

The lowest allowed voltage at the O_{p1} and O_{m1} outputs is determined by considering the voltage drops across the transistors $M_{n1,2}$ and M_{bias2}. Due to the symmetry of the differential stage the node *Sin* is a virtual ground whose potential is signal independent and equal to $V_{DSbias2}$. The saturation condition written for the transistors $M_{n1,2}$ and M_{bias1} give

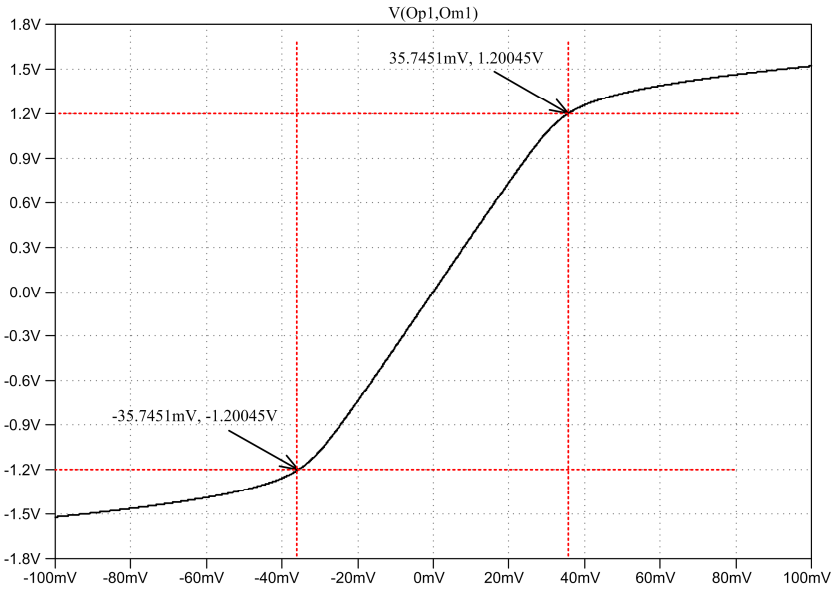
$$V_{Op1-\min} = V_{Om1-\min} = V_{DSat-n1,2} + V_{DS-bias2} = 218\text{mV} + 651\text{mV} \cong 870\text{mV}$$

The upper limit of the output voltage swing is also calculated from the saturation condition of the transistors M_{p1} and M_{p2}.

$$V_{Op1-\max} = V_{Om1-\max} = V_{DD} - V_{DSat-p1,2} = 3\text{V} - 195\text{mV} \cong 2.8\text{V}$$

However, in reality, the symmetry of the amplifier causes complementary variations of V_{Op1} and V_{Om1}. Therefore, the output voltage swing is limited to approximately V_{outCM}±630mV. This single ended swing allows a ±1.25V differential voltage swing without clipping (no distortions caused by limitation). Considering the previously calculated low frequency gain, this output swing corresponds to a 65mV input voltage amplitude.

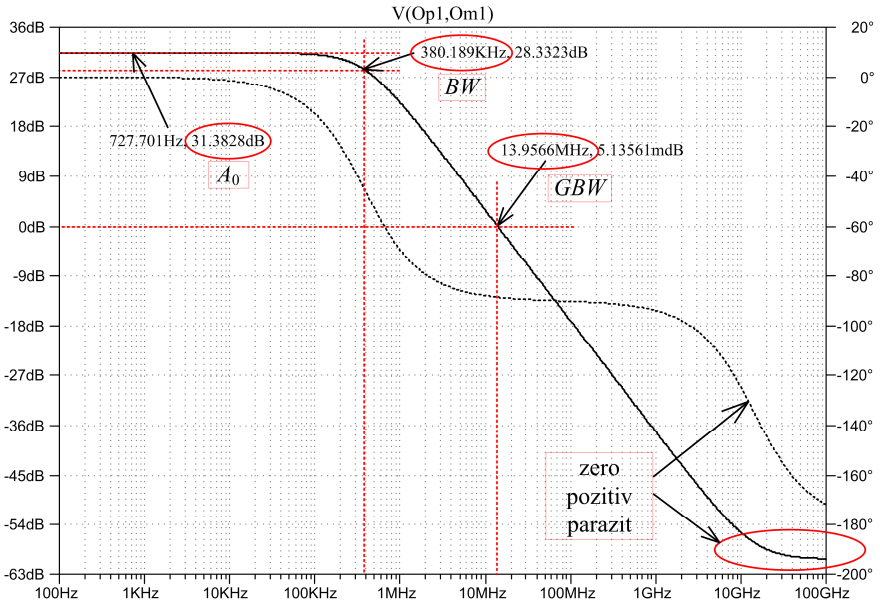
The output voltage swing can be validated by running a *.DC* analysis in which the input amplitude, provided by the source V_{in}, is swept between -100mV and 100mV with a 0.1mV step size. The corresponding Spice command is *.dc Vin -0.1 0.1 0.1m*. After running the analysis, the DC transfer function is obtained by plotting the differential output voltage V(Op1,Om1).



13. Plot the magnitude and phase responses of the amplifier. Measure A_0, the frequency of the dominant pole (f_p=*BW*) and the unity gain bandwidth *GBW*. Notice the presence of the parasitic right half plane zero caused by the Miller effect and compare the measurements with the values found in hand calculations.

The magnitude and phase responses of the differential amplifier are obtained by running an *.AC* analysis. The limits of the swept frequency range are chosen to cover the important sections of the response. For example, since the bandwidth of the amplifier is approximately 380kHz, seeing the evolution of the phase imposes the lower limit of the frequency range at a few kHz. Similarly, if the parasitic zero is located at high frequencies, the upper limit of the frequency range will be set to

tens of GHz. Considering these limits, the frequency is swept between 100Hz and 100GHz with 100 point each decade. The Spice command is *.ac dec 100 100 100G*.



The low frequency gain is measured by shifting the cursor to the constant section of the magnitude response and reading the *Oy* coordinate. It results that the measured gain is approximately 31.4dB, in accordance with the value found from the operating point analysis.

The bandwidth of the amplifier is measured by positioning the cursor to 28.4dB gain on the *Oy* axis or to -45° phase shift and reading the *Ox* coordinate from the measurement window. The bandwidth results to be approximately 380kHz.

The unity-gain bandwidth is defined as the frequency where the magnitude response intersects the frequency axis and the gain becomes equal to unity or 0dB. Positioning the cursor to 0dB on the *Oy* axis gives a *GBW* of approximately 14MHz.

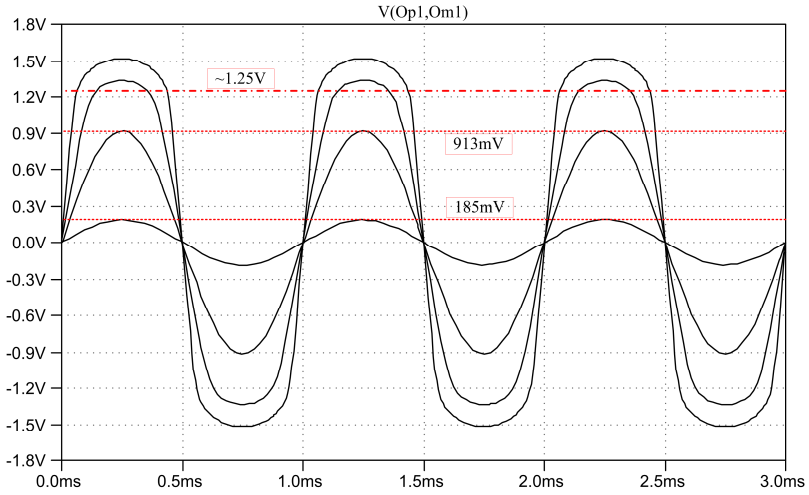
14. Simulate the transient response of the amplifier for a sine wave input with 1kHz frequency and the amplitude set to 5mV, 25mV, 50mV and then 100mV. At which output amplitude does the clipping occur if the input amplitude is 100mV?

Simulating the time domain behavior requires a transient simulation run for at least 4-5 full periods of the input signal. The input frequency should be sufficiently small to emphasize the low frequency gain. Also, the maximum step size must be set as a compromise between resolution and simulation time. For linear circuits, reasonable simulation times and accuracies are obtained for about 1000 point for each signal period. For a 1kHz input signal the analysis may be run up to 3mS with a 1µs maximum time step. The corresponding Spice command is *.tran 0 3m 0 1u*.

The parametric analysis imposed by the exercise requires the definition of the input amplitude as additional parameter. Then, the simulator must be instructed to run a transient analysis for each value of the input amplitude

The additional parameter is defined by adding the Spice command *.param Ain=10mV* to the schematic sheet (*Edit → Spice Directive*, the *.op* icon from the menu bar or the *CTRL+S* keyboard shortcut), where *Ain* is the additional parameter. This parameter can be associated with the input amplitude *Ain* if the transient component of the source V_{in} is changed to *SINE(0 {Ain} 1k)*.

The simulator is instructed to repeat the transient analysis for every value of the parameter *Ain* through the command *.step param Ain list 10m 25m 50m 100m*. The *.STEP* command defines *Ain* as a parameter and will run the main analysis for all the values enumerated in the list. The values must be specified in increasing order.

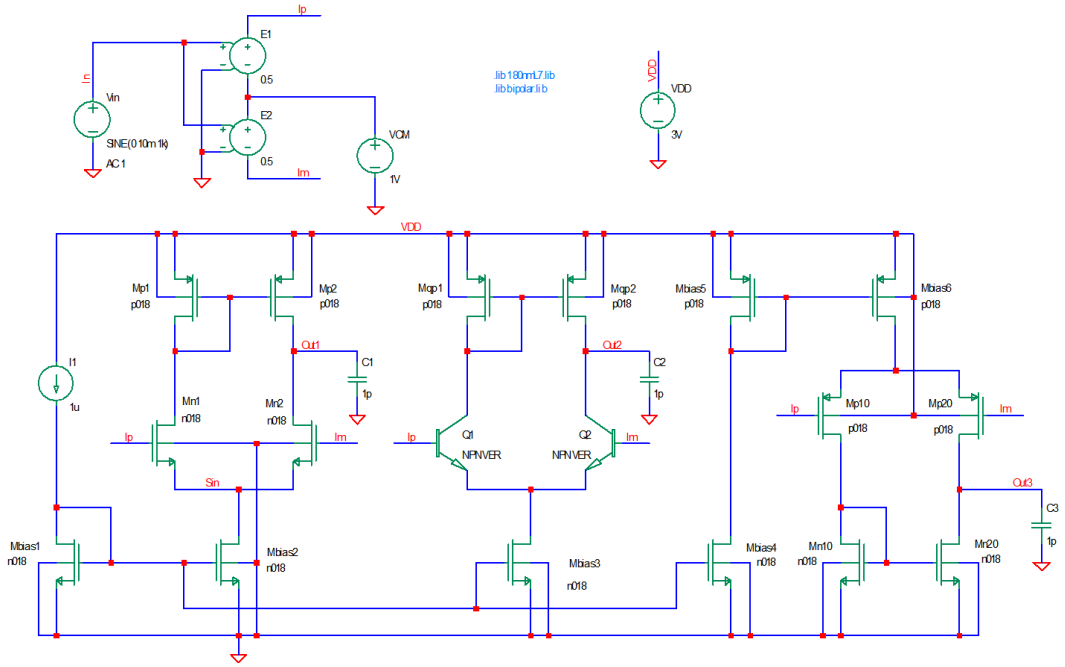


The amplitude of the output voltage, corresponding to different *Ain* values, is measured by choosing *Select Steps* from the *Plot Settings* menu and plotting the curves returned by the simulator one by one. The measured amplitudes are 185mV for *Ain*=5mV (5mV·A_0) and 913mV for 25mV. The larger input amplitudes, 50mV and 100mV, will overdrive the amplifier output as predicted by the DC transfer function, causing the clipping of the output voltage at approximately 1.25V.

15. Repeat the exercises 8-13 for all the amplifiers in the test schematic. Compare the current consumption and the low frequency gain of the bipolar input vs. the MOS input stages. Explain the observations.

3. The differential amplifier with current mirror load

The test schematic (*ampdif-sarcogl.asc*):



Proposed exercises:

16. Design the amplifier for *GBW*>10MHz and C_L=5pF. In order to fulfill the design specifications in spite of the parasitic effects (capacitances, g_{mb}), the parameters should be considered 1.5–2 times larger (for example, use *GBW*=30MHz in hand calculations).

Hints:

a. from the expression of the unity-gain bandwidth (*GBW*) calculate the small signal transconductance G_m of the amplifier. The transconductance g_m of the input transistors is then equal to G_m;
b. choose a usual value for the V_{DSat} voltage of the input transistors M_{n1} and M_{n2} (for example 200mV);
c. from the definition of the transconductance, a function of the drain current and the V_{DSat} voltage, determine the current flowing through the input differential pair and the branches of the current mirror M_{bias1}-M_{bias2};
d. calculate the geometry W/L of the transistor by considering V_{DSat} and V_{Th}. Also determine the lowest allowed input common mode voltage V_{inCM}, required for biasing. Choose V_{inCM} that maximizes the signal swing (for example $V_{DD}/2$);
e. use the drain currents and the V_{DSat} voltages of the PMOS load transistors to calculate their geometry;

17. Validate the operating points of the components and adjust the circuit to match hand calculations. Fill the following table:

	V_{GS}	V_{DS}	V_{Th}	V_{DSat}	I_D	g_m	r_{DS}
M_{n1}							
M_{n2}							
M_{p1}							
M_{p2}							
M_{bias1}							
M_{bias2}							

18. Use the equations from the lecture notes and the small signal parameters to calculate the low frequency gain A_0 and the unity gain bandwidth *GBW* of the amplifier;
19. Plot the magnitude and phase responses of the amplifier. Measure A_0, the frequency of the dominant pole (f_p=*BW*) and the unity gain bandwidth *GBW*. Notice the presence of the parasitic right half plane zero caused by the Miller effect and the additional pole-zero pair introduced by the current mirror load.
20. Simulate the transient response of the amplifier for a sine wave input with 1kHz frequency and the amplitude set to 5mV, 10mV and then 20mV. At which output amplitude does the clipping occur if the input amplitude is 20mV?
21. Repeat the exercises 16-20 for all the amplifiers in the test schematic. Compare the current consumption and the low frequency gain of the bipolar input vs. the MOS input stages. Explain the observations.