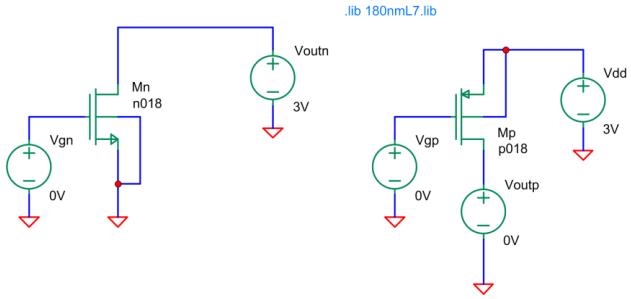
# 1. The simple, one transistor current source

The test schematic (*srs-simpla-MOS.asc*):




**Proposed exercises:**

1. Design the NMOS source for a 40µA output current and the minimum allowed output voltage $V_{omin}$=250mV. The design means to determine all bias voltages and to choose the appropriate operating point for the transistor.

**Hints:**

a. estimate $V_{omin}$ depending on the transistor operating point, specifically on $V_{DSat}$;
b. from $V_{Th}$ and $V_{DSat}$ determine $V_{GS}$;
c. from $V_{DSat}$ and the output current calculate the transistor geometry $W/L$. Use the table with the reference operating point of Lab 1.

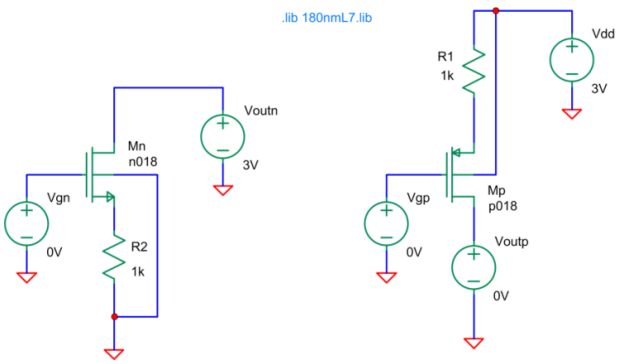
2. Validate the OP through simulation and adjust the circuit to fulfill the design specifications. Fill the following table:

| | $V_{GS}$ | $V_{DS}$ | $V_{Th}$ | $V_{Dsat}$ | $I_D$ | $g_m$ | $r_{DS}$ |
|---|---|---|---|---|---|---|---|
| $M_n$ | | | | | | | |

3. Determine the output resistance of the source.
4. Simulate the output characteristic of the source. Measure the output resistance around the previously set operating point. Estimate the value of $V_{omin}$.
5. Repeat the exercises 1-4 for the similar PMOS source.

# 2. The simple, one transistor current source with resistive degeneration

The test schematic (*srs-degR-MOS.asc*):



**Proposed exercises:**

6. Design the NMOS source for a 40µA output current and $V_{omin}$=350mV. What is the influence of the degeneration resistor on the operating point of the transistor?

**Hints:**

a. from $V_{omin}$ determine $V_{DSmin}$ and the voltage drop across the resistor;
b. considering the above voltages and $V_{Th}$, calculate the $V_{GS}$ of the transistor;
c. from $V_{DSat}$ and the output current determine the transistor geometry $W/L$. Use the parameters of the reference OP found in Lab 1.

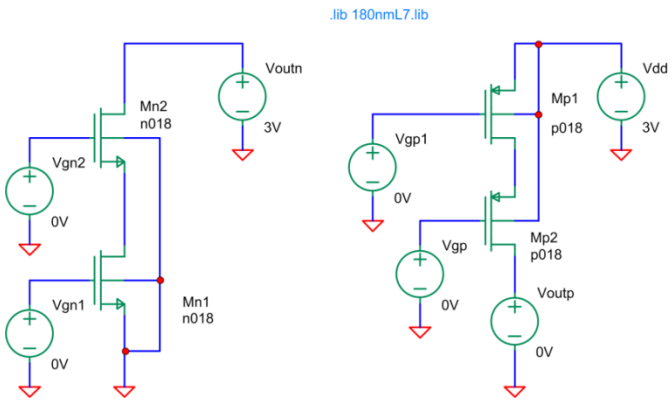
7. Validate the OP through simulation and adjust the circuit to fulfill the design specification. Fill the following table:

| | $V_{GS}$ | $V_{DS}$ | $V_{Th}$ | $V_R$ | $V_{Dsat}$ | $I_D$ | $g_m$ | $r_{DS}$ |
|---|---|---|---|---|---|---|---|---|
| $M_n$ | | | | | | | | |

8. Determine the output resistance of the source.
9. Simulate the output characteristic of the source. Measure the output resistance around the previously set operating point. Estimate the value of $V_{omin}$.
10. Repeat the exercises 6-9 for the similar PMOS source.

## 3. The cascode current source

The test schematic (*srs-cascoda-MOS.asc*):




**Proposed exercises:**

11. Design the NMOS source for a 40µA output current and $V_{omin}$=500mV. How is the $V_{DS}$ voltage of $M_{n1}$ set?

Designing the source means to determine the geometries for both transistors in the circuit and to set the bias voltages $V_{gn1}$ and $V_{gn2}$ in order to meet the design specifications.

*In the first step* the minimum allowed output voltage, $V_{omin}$, is split between the two transistors. The first idea is to divide $V_{omin}$ in two equal parts and set $V_{DS\text{-}n1}$=$V_{DS\text{-}n2}$=250mV. However, in practice $V_{DS\text{-}n1}$ is always chosen to be larger than $V_{DS\text{-}n2}$. The reason for this is that the output current is set by $M_{n1}$ and this transistor must be maintained in saturation as long as possible when the output voltage decreases. Consequently, $V_{DS\text{-}n1}$=300mV and $V_{DS\text{-}n2}$=200mV.

*In the second step* a reasonable value is chosen for $V_{DSat\text{-}n1,2}$, for example 200mV.

*In the third step* the reference operating point parameters are used to determine the transistor geometries. For $I_{D\text{-}n1,2}$=40µA and $V_{od\text{-}n1,2}$=200mV it results that

$$\left(\frac{W}{L}\right)_{n1,2}=\left(\frac{W}{L}\right)_{ref}\cdot\frac{I_{D-n1,2}}{I_{D-ref}}\cdot\left(\frac{V_{od-ref}}{V_{od-n1,2}}\right)^2=\frac{5}{1}\cdot\frac{40}{50}\cdot\left(\frac{240}{200}\right)^2=\frac{5.76\mu}{1\mu}$$

According to this *W*/*L* ratio, the source/drain area and perimeter are

$$\begin{cases}AS=AD=5.76\mu m\cdot 0.2\mu m=1.15\mu m^2\\ PS=PD=2\cdot\left(5.76\mu m+0.2\mu m\right)=11.9\mu m\end{cases}$$

*Finally*, the bias voltages $V_{gn1}$ and $V_{gn2}$ are calculated. The threshold voltage of the cascode transistor, $V_{Th\text{-}n2}$, is always considered to be larger than the value in the reference table due to the non-zero substrate-source voltage $V_{SB}$.

$$V_{gn1}=V_{GS-n1}=V_{od-n1}+V_{Th-n1}=200mV+450mV=650mV$$

$$V_{gn2}=V_{GS-n2}+V_{DS-n1}=V_{od-n2}+V_{Th-n2}+\Delta V_{Th-n2}+V_{DS-n1}=200mV+450mV+100mV+300mV=1050mV$$

12. Validate the OP through simulation and adjust the circuit to fulfill the design specification. Fill the table with the simulated parameters.

In order to validate the transistor operating points, an *.OP* analysis is performed. By reading the returned node potentials and branch currents, it can be observed that $V_{DSat\text{-}n1}$ is only 192mV while the output current is 34.3µA. The $V_{GS1}$ voltage is adjusted by slightly increasing the $V_{gn1}$ voltage. Next, the output current is adjusted by changing the transistor geometry. When the target values for $V_{DSat\text{-}n1}$ and $I_{D\text{-}n1,2}$ have been achieved, the $V_{DS\text{-}n1}$ voltage is also changed through $V_{gn2}$. The iterative changes in the schematic lead to $V_{gn1}$=660mV, $V_{gn2}$=1025mV, $(W/L)_{n1,2}$=6.22µm/1µm. For these values the following parameters can be found:

| | $V_{GS}$ | $V_{DS}$ | $V_{Th}$ | $V_{Dsat}$ | $I_D$ | $g_m$ | $r_{DS}$ |
|---|---|---|---|---|---|---|---|
| $M_{n1}$ | 660mV | 301mV | 446mV | 199mV | 40µA | 309µS | 136kΩ |
| $M_{n2}$ | 724mV | 2.7V | 531mV | 188mV | 40µA | 325µS | 327kΩ |

13. Determine the output resistance of the source.

The output resistance can be approximated from the equation given in the lecture notes:

$$R_{out}\cong g_{m-n2}r_{DS-n2}r_{DS-n1}=325\mu S\cdot 326.8k\Omega\cdot 135.6k\Omega=14.4M\Omega$$

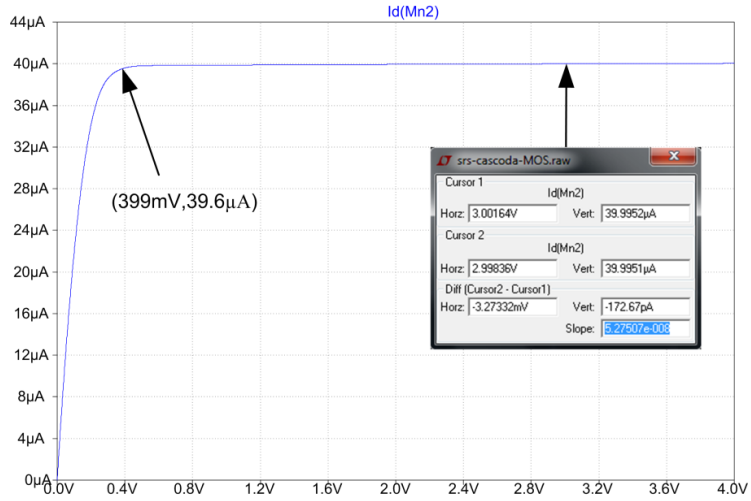
14. Simulate the output characteristic of the source. Measure the output resistance around the operating point. Estimate the value of $V_{omin}$.

The output characteristic is plotted by performing a *.DC* analysis, in which the source $V_{outn}$ is linearly changed between 0V and 3V with a 1mV step size. The corresponding Spice command is *.dc Voutn 0 3 1m*. Once the analysis has been finished, the output current is plotted as Id(Mn2).

The output resistance is measured by placing the cursors at two distinct positions around the operating point and reading the *Slope* from the measurement window. The output resistance is then calculated as 1/*Slope*=$R_{out}$=18.9MΩ.

The minimum allowed output voltage is estimated by placing a cursor to the point on the curve

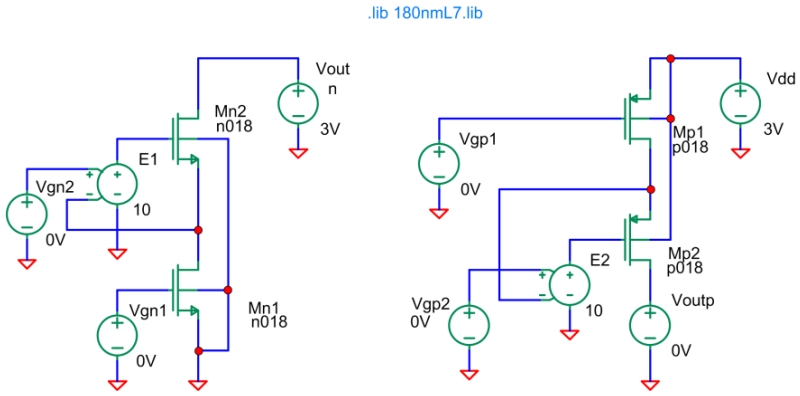
where the transistor $M_{n1}$ is shifted from saturation into the linear region. Reading the cursor coordinates yields approximately $V_{omin}$=399mV.




15. Repeat the exercises 11-14 for the similar PMOS source.

## 4. The cascode current source with enhanced output resistance

The test schematic (*srs-casenhanced-MOS.asc*):




**Proposed exercises:**

16. Design the NMOS source for a 40µA output current and $V_{omin}$=550mV. How is the $V_{DS}$ voltage of $M_{n1}$ set? Which transistor sets the output current?

**Hints:**

a. split $V_{omin}$ between $V_{DS\text{-}n1}$ and $V_{DS\text{-}n2}$ similarly as for the cascode current source;
b. choose $V_{DSat}$ for both transistors;
c. from $V_{DSat}$ and $V_{Th}$ calculate the gate-source voltage of $M_{n2}$;
d. from $V_{DSat}$ and the output current determine the transistor geometries;
e. the voltage $V_{gn2}$ is calculated knowing that, if the gain of the voltage controlled voltage source $E_1$ is sufficiently large, the inputs will tend to settle at the same potential ($V^+$=$V^-$ just like for an opamp).

17. Validate the OP by simulation and adjust the circuit to fulfill the design specification. Fill the following table:

| | $V_{GS}$ | $V_{DS}$ | $V_{Th}$ | $V_R$ | $V_{Dsat}$ | $I_D$ | $g_m$ | $r_{DS}$ |
|---|---|---|---|---|---|---|---|---|
| $M_{n1}$ | | | | | | | | |
| $M_{n2}$ | | | | | | | | |

18. Determine the output resistance of the source.
19. Simulate the output characteristic of the source. Measure the output resistance around the previously set operating point. Estimate the value of $V_{omin}$.
20. Repeat the exercises 16-19 for the similar PMOS source.