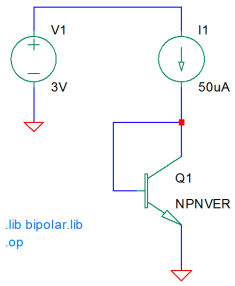
1. Bipolar junction transistors

1.1. The operating point

The test schematic (*tranzistorBJT-psf.asc*):

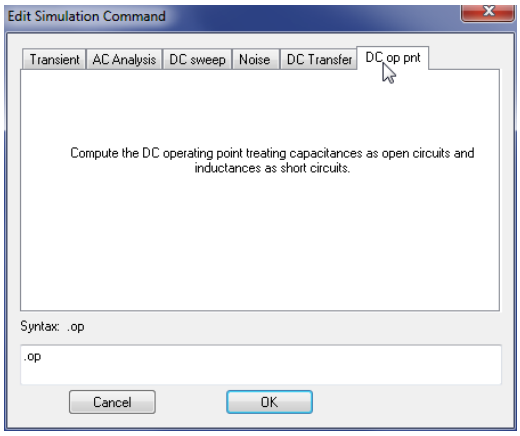


The test bench contains a single bipolar transistor Q_1 connected as a diode (base wired to the collector), which receives a 50µA DC current supplied by the ideal source I_1. The voltage source V_1 represents the 3V supply voltage. The transistors symbol (*npn.asy*) can be found in the root folder of the project. In order to have access to the corresponding Spice model, the transistor must be renamed to *npnver* after the placement onto the schematic sheet. The path to the library containing the specified transistor model must also be specified by placing the Spice command *.lib bipolar.lib* on the schematic sheet.

Proposed exercises:

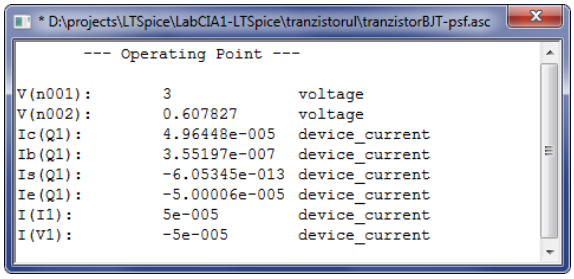
1. Create the appropriate simulation profile and simulate the operating point of the transistor.

From the menu item *Simulate* choose the option *Edit Simulation Cmd*. In the opening window select the *.OP* analysis type by clicking on the *DC op pnt* tab. After accepting the chosen analysis option, the corresponding Spice command *.OP* will be placed on the schematic in order to instruct the simulator to run the operating point analysis. The result of the *.OP* analysis is a set of values including all node potentials relative to the ground, all the branch currents and the typical parameters of all the semiconductor devices in the schematic.

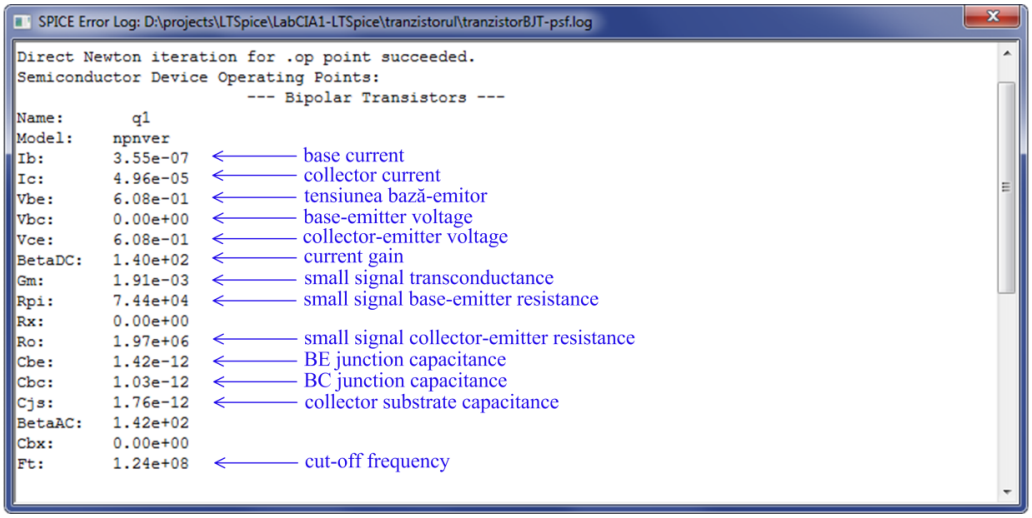


When the selection and the settings of the simulation profile have been finished, the next step is to choose the *Run* command from the menu item *Simulate*. After running the analysis, the simulator displays a window returning all node potentials referenced to the ground and the branch current of the test circuit. The calculated values can also be read directly in the status bar when hovering the mouse cursor over different nets and device terminals in the schematic. The negative signs of the

currents reflect the flowing sense. By convention, currents flowing into circuit nodes will all be positive, while current flowing out of nodes will be negative.



The parameters of the bipolar transistor under test are returned in the simulation output file that can be accessed by clicking on the *View* menu item and the *Spice Error Log* option (or alternatively by hitting the *CTRL+L* key combination).

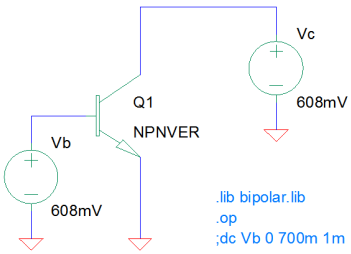


2. Fill the following table:

I_B	I_C	β	V_{BE}	V_{CE}	g_m	r_{BE}	r_{CE}

1.2. The transfer characteristic (*tranzistorBJT-dc.asc*)

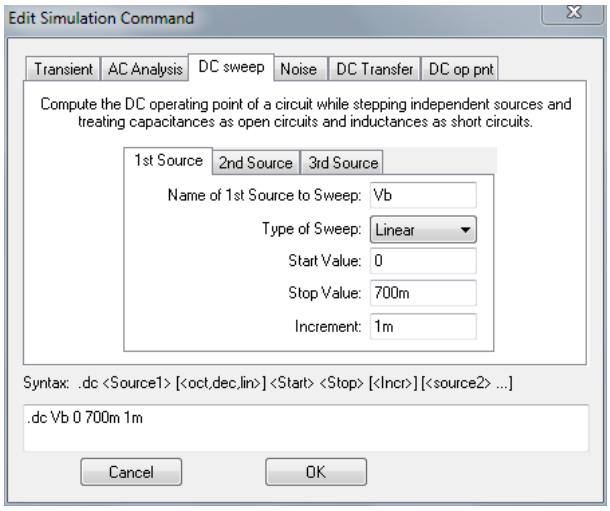
The test schematic:



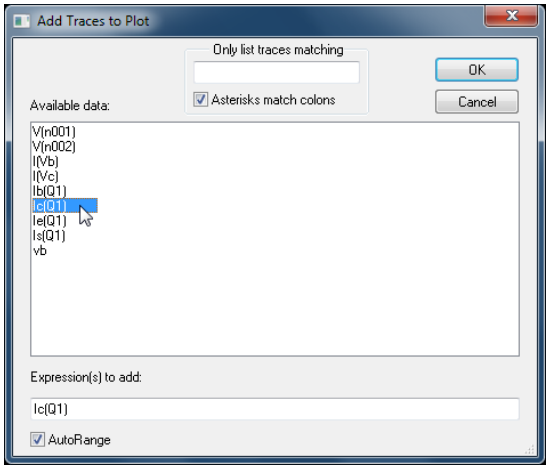
Proposed exercises:

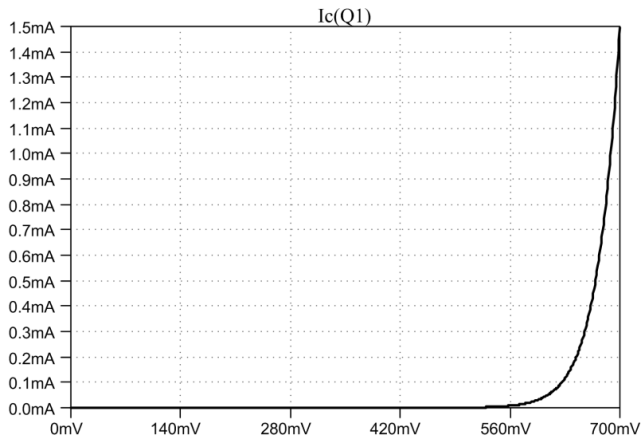
3. Create the appropriate simulation profile and simulate the transfer characteristic of the bipolar transistor.

The simulation the transfer characteristic requires a *.DC* analysis that linearly changes the base voltage V_b between 0V and 700mV with a 1mV increment. The collector-emitter voltage is set by a second DC source V_c. For consistent simulation results, the operating point found in the previous exercise needs to be maintained. Therefore, the nominal voltages V_{BE}=V_{CE}=608mV are read from the table and set on the schematic. A new simulation profile is then created by clicking the *Simulate* menu item and the *Edit simulation cmd* option.



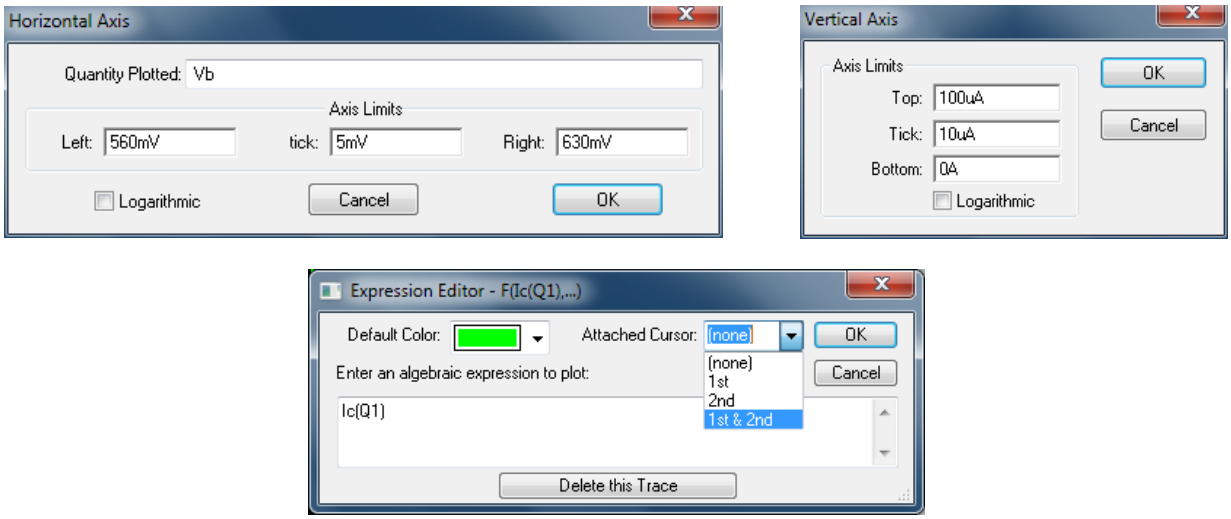
After running the simulation (*Simulate* → *Run*) the simulator displays a plot window. The *Plot Settings* menu item, along with the *Add Trace* option (or alternatively the key combination *CTRL+A*) allows the selection of the voltages and currents to be plotted. Since the *y* axis of the transfer characteristic corresponds to the transistor collector current, the parameter $I_c(Q_1)$ is selected from the list of parameters. As a result, the exponential dependence of the current on the base-emitter voltage is plotted.



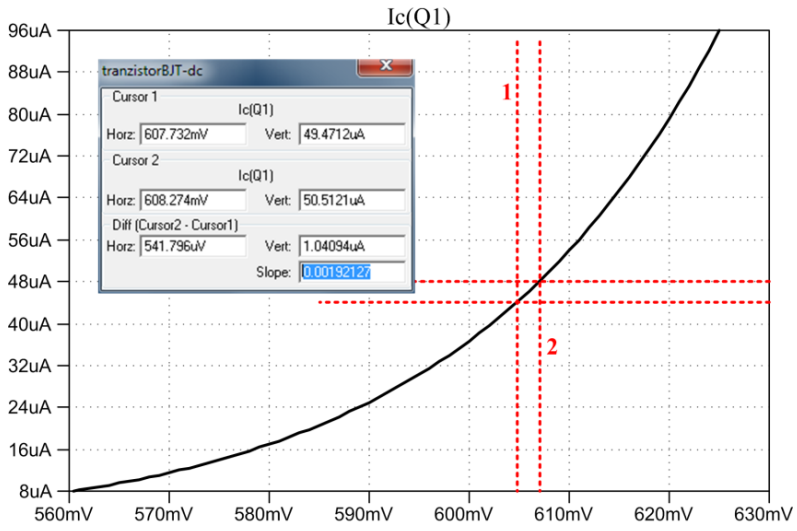


4. Measure the slope of the transfer characteristic around the operating point found in exercise 1 (I_c=50µA, V_{BE}=608mV) and compare the measurement result with the transconductance (g_m) from the small signal parameter table.

Adjust the scales of the *Ox* and *Oy* axes for a detailed view on the region of interest. Hover the mouse cursor over the axes until a small ruler shows up, then a click will open the settings window. The slope of the curve is measured with the two available cursors. For activation right click on the curve expression in the legend above the plot (on Ic(Q1)), then attach both cursors to the plotted transfer characteristic.



The small signal transconductance is measured by positioning the cursors onto distinct points around the operating point and by reading the *Slope* parameter of the measurement window. The resulting measurement is g_m=1.92mS, which corresponds to the transconductance calculated by the operating point analysis.



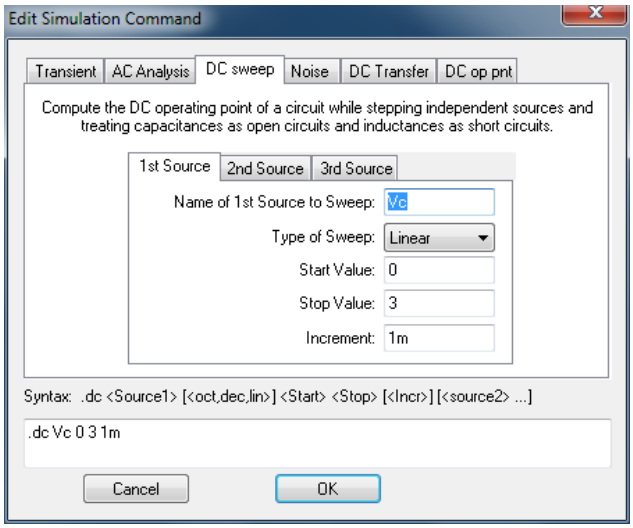
1.3. The output characteristic

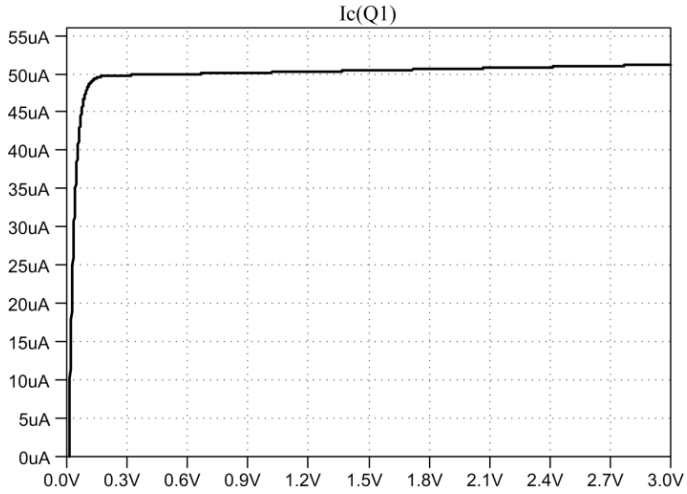
The test schematic is identical to the one used to determine the transfer characteristic, but the changing input variable will be the voltage supplied by V_c. The variation range must be adjusted considering the weak dependence of the collector current on the collector-emitter voltage. The chosen range must also cover both the saturation and the forward active regions.

Proposed exercises:

5. Change the simulation profile for a linear variation of the source V_c between 0V and 3V with a 1mV increment. The base potential defined by V_b is set to 608mV, corresponding to the previously simulated bias point.

Access the *Simulate* menu item and choose the option *Edit Simulation Cmd*. In the settings window change the details concerning the performed *.DC* analysis. The Spice command on the schematic will change to *.dc Vc 0 3 1m*. After running the simulation (*Simulate* → *Run*) plot the collector current Ic(Q1).





6. Measure the slope of the output characteristic around the operating point set in the exercise 1 (I_c=50µA, V_{BE}=608mV, V_{CE}=608mV), calculate its reciprocal and compare the result to the collector-emitter resistance (r_{CE}) from the small signal parameter table.

Attach both cursors to the plotted current and position them onto distinct locations around the operating point. Read the *Slope* parameter directly from the measurement window. The collector-emitter resistance is found to be

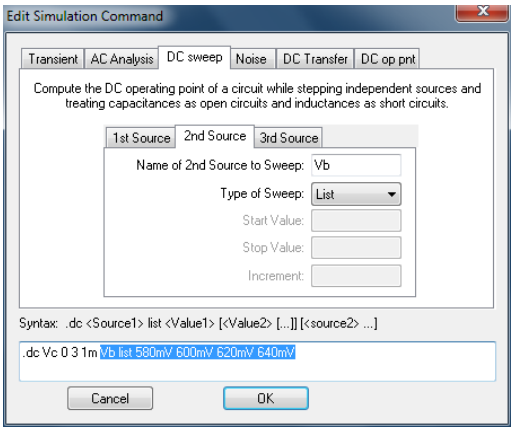
$$r_{CE} = \frac{1}{Slope} = \frac{1}{5.11 \cdot 10^{-7}} \cong 1.96\text{M}\Omega\,,$$

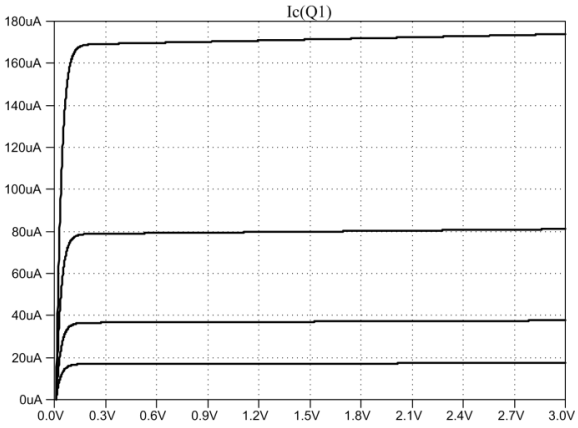
a value consistent with the results of the .OP analysis of exercise 1.

7. Simulate the output characteristic of the bipolar transistor and show its dependence on the base-emitter voltage.

Add a parametric analysis to the *.DC* simulation profile. The main variable is still the source V_c (left unchanged in the simulation profile), while the secondary swept variable is the source V_b that changes according to the following list of values: 580mV, 600mV, 620mV, 640mV. The corresponding Spice command on the schematic will be adjusted to *.dc Vc 0 3 1m Vb list 580mV 600mV 620mV 640mV*.

After running the simulation, plot the collector current Ic(Q1).

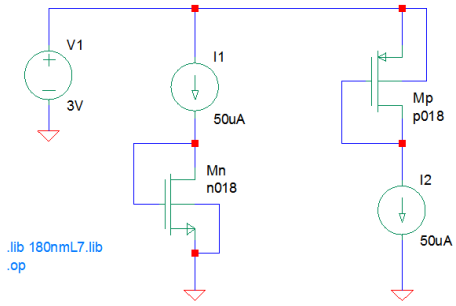




2. The MOS transistor

2.1. The operating point (*tranzistoareMOS-psf.asc*)

The test schematic for simulating both NMOS and PMOS transistors:



The transistor symbols can be found in the root folder of the project (*nmosb.asy* and *pmosb.asy*). After placing the components on the schematic the Spice model name is changed to *n018* or *p018*, depending on the device type. The schematic is similar to the setup used to simulate the operating point of the bipolar transistor. Pay special attention to the PMOS transistor terminal connections – the correct operation requires the source and substrate terminals to be connected to higher voltages then the gate and the drain.

Proposed exercises:

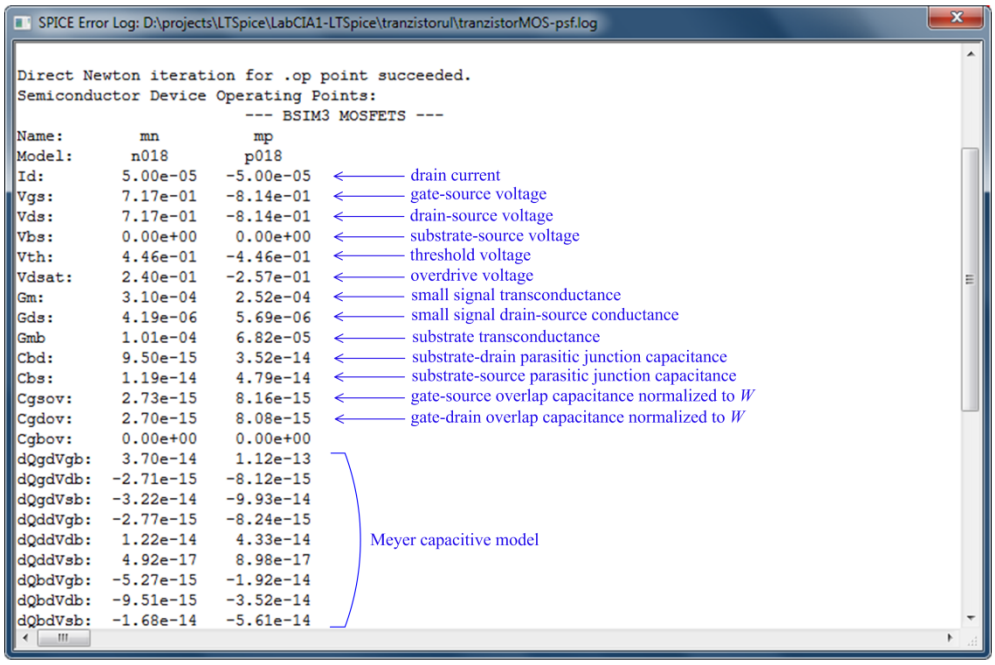
8. Create the appropriate simulation profile that evaluates the operating point and the small signal parameters.

The simulation profile is similar with the one created for the bipolar transistor. The *.OP* analysis returns a window with all node voltages referenced to ground and all branch currents in the circuit. A detailed list with the transistor parameters is found in the output file (*View* → *Spice Error Log*).

Since PMOS and NMOS transistors have complementary structure, voltages and currents associated with the PMOS device will be negative in the parameter table.

9. Use the parameter listing in the output file to fill the following table:

	V_{GS}	V_{DS}	V_{BS}	V_{Th}	V_{DSat}	I_D	g_m	g_{mb}	r_{DS}
NMOS									
PMOS	814mV	814mV	0V	446mV	257mV	50µA	252µS	68.2µS	176kΩ



10. Fill the following reference table (*Important – it will be used for every lab !*):

	I_D	W/L	V_{DSat}	V_{Th} (V_{BS}=0)
NMOS				
PMOS	50µA	15µ/1µ	257mV	446mV

11. Change the transistor geometry and the test schematic in order to adjust the operating point to a current equal to 30µA while V_{DSat} remains constant. Use a scaling procedure and check the hand calculations against the simulation results.

In order to scale the operating point, the current equation is written twice, once for the set of reference parameters (the table of exercise 10) and once for the newly imposed operating point.

$$\begin{cases} I_{D-ref} = \dfrac{\mu C_{ox} W_{ref}}{2L_{ref}} V_{DSat-ref}^2 \\ I_D = \dfrac{\mu C_{ox} W}{2L} V_{DSat}^2 \end{cases}$$

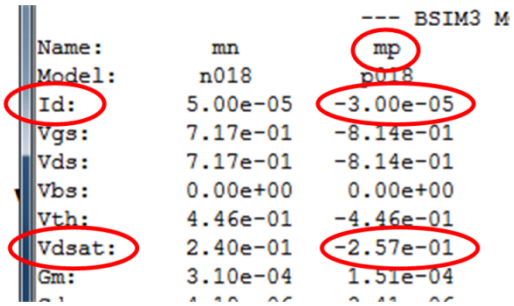
Replace the reference parameters with the values from the table in exercise 10 (*for PMOS*), I_D with 30µA and V_{DSat} with 257mV. Then, dividing the two equations leads to the geometry corresponding to the new operating point.

$$\frac{W}{L} = \frac{W_{ref}}{L_{ref}} \cdot \frac{I_D}{I_{D-ref}} \cdot \left(\frac{V_{DSat-ref}}{V_{DSat}} \right)^2 = \frac{15}{1} \cdot \frac{30}{50} \cdot \left(\frac{240}{240} \right)^2 = \frac{9\mu}{1\mu}$$

The new geometry requires the recalculation of the areas and of the perimeters *AS*, *AD*, *PS*, *PD*:

$$\begin{cases} AS = AD = W \cdot 0.2\mu = 9\mu \cdot 0.2\mu = 1.8\text{pm}^2 \\ PS = PD = 2(W + 0.2\mu) = 2(9\mu + 0.2\mu) = 18.4\mu\text{m} \end{cases}$$

The parameters can be set by right clicking on the PMOS transistor on the test schematic. After the settings have been changed, the simulation must be run again to allow the simulator to update the parameters in the output file. The inspection of the parameter list shows that for the new 30µA current the V_{DSat} voltage has been maintained constant at 257mV.

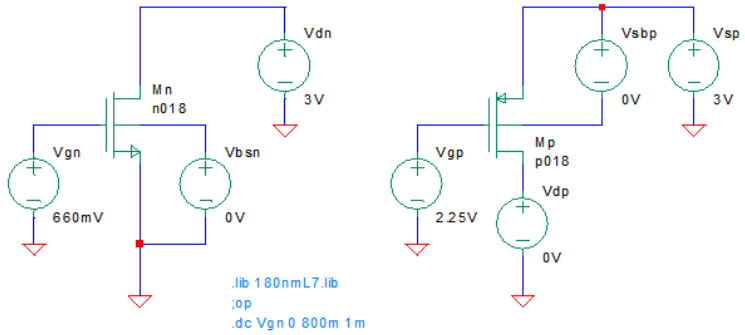


12. Change the transistor geometry and the test schematic in order to adjust the operating point to a current equal to 70µA and a V_{DSat} equal to 200mV. Check the hand calculations against the simulation results.

The scaling procedure of exercise 11 can be used again for calculating the new geometry according to the imposed operating point. After replacing the set of reference parameters, the new current and the new overdrive voltage into the current equations, the width, the length and the diffusion parameters are calculated to be W=34.7µm, L=1µm, AS=AD=6.94pm^2 and PS=PD=69.8µm. The output file shows that the operating point has been adjusted to I_D=70µA and V_{DSat}=204mV.

2.2. The transfer characteristic (*tranzistoareMOS-dc.asc*)

The test schematic:



The voltages $V_{gn,p}$ and $V_{dn,p}$ have the same significance as for the bipolar transistor test schematic. The additional voltage sources V_{bsn} and V_{sbp} represent the substrate-source voltage drop, influencing the transistor threshold voltages.

Proposed exercises:

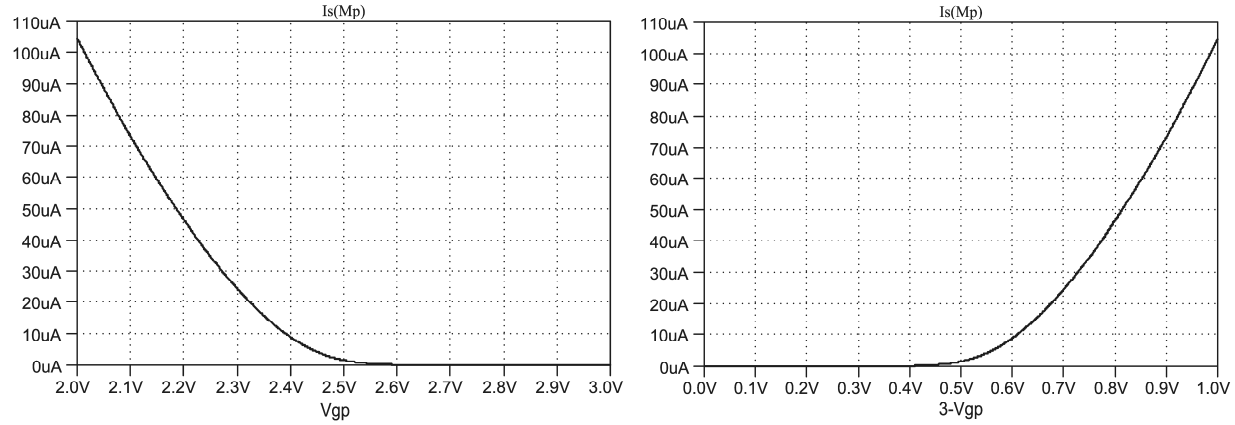
13. Create the simulation profile for plotting the transfer characteristic of the PMOS transistor.

The transfer characteristic can be plotted through a *.DC* analysis that linearly sweeps the gate voltage V_{Gp}. Considering the complementary operation of PMOS transistors, all terminal voltages will be referenced to the supply voltage V_{DD} instead of the ground. Therefore, the source V_{Gp} will be swept between V_{DD}-0V and V_{DD}-800mV with a 1mV step size. Since V_{DD} has been set to 3V and the simulator expects a monotonically increasing input voltage, the parameters *StartValue* and *Stop Value* in the simulation profile will be adjusted to 2.2V and 3V. The resulting Spice command on

the schematic sheet will be *.dc Vgp 2.2 3 1m*. The source-drain voltage V_{SD} of the transistor must be set to the same value as found for the operating point in the exercise 9. Thus, the source V_{dp} setting the drain potential will have the value V_{DD}-814mV=2.19V.

After finishing the simulation, the menu item *Plot Settings* and the option *Add Trace* (or the *CTRL+A*) in the graphical window opens a list of available quantities to plot. The target curve in this list is the drain current Id(Mp). For a PMOS transistor the drain current is always negative due to the sign convention. If only the absolute value of the current is of interest, the curve –Id(Mp) or, alternatively, the source current Is(Mp)= –Id(Mp) can be displayed.

In the plotted characteristic the variable on the *Ox* axis is the gate potential V_{gp} of the transistor. The final transfer characteristic results by changing the *Ox* axis variable to the source-gate voltage. This adjustment is performed by accessing the settings window of the *Ox* axis and by swapping the *Quantity plotted* option *Vgp* with *3-Vgp*.



14. Measure the slope of the transfer characteristic around the operating point of exercise 9. Compare the measurement result with the transconductance g_m found by the .OP analysis.

The scale of the *Ox* axis on the previously plotted drain current is adjusted to the range between 750mV and 850mV with a 20mV tick. Similarly, the scale of the *Oy* is adjusted between 35µA and 65µA with a 5µA tick. Both cursors will be attached to the curve Is(Mp) and positioned around the 50µA nominal current. The transconductance, found by reading the parameter *Slope* in the measurement window is approximately 250µS. This measurement is consistent with the value found by the simulator during the operating point analysis in exercise 9.

15. Simulate the variation the transfer characteristic and of the threshold voltage with V_{bsn}.

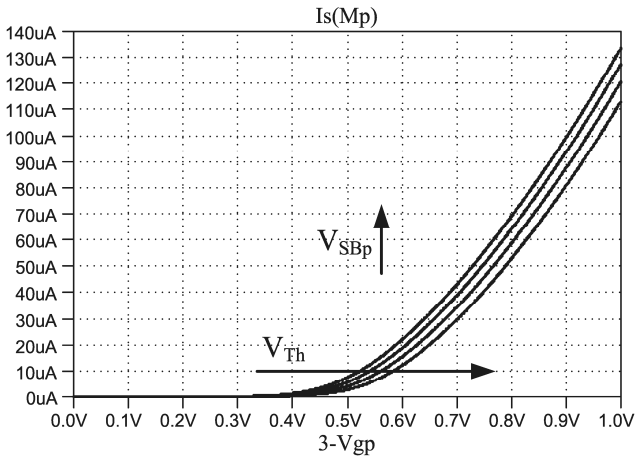
The primary *.DC* sweep, used to find the transfer characteristic, is maintained while a secondary sweep is added to the simulation profile. The secondary sweep varies the voltage supplied by the source V_{sbp}. The parametric simulation is activated in the profile by clicking the *2nd Source* tab and by filling the appropriate fields. The source V_{sbp} will be swept according to the following list of values: 100mV, 200mV, 300mV and 400mV.

2.3. The output characteristic

The test schematic is the same as the one used to obtain the transfer characteristic. The voltage V_{bsn} is set to 0V, while the gate-source voltage is chosen according to the operating point found in the exercise 9 (814mV). The gate potential of the transistor will be $V_{gn}=V_{DD}$-814mV=2.19V.

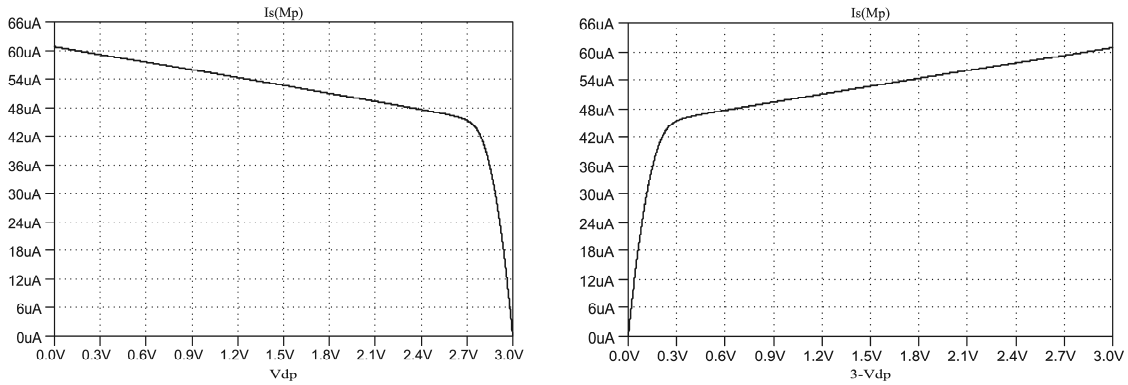
Proposed exercises:

16. Plot the output characteristic of the PMOS transistor.



The output characteristic is simulated by changing the profile of the exercise 13 for a variation of the drain current with the drain-source voltage of the transistor. The main variable swept during the analysis will be the voltage supplied by the source V_{dp} that varies between 0 and 3V with a 1mV step size. The corresponding Spice command placed on the schematic becomes *.dc Vdp 0 3 1m*.

After running the simulation, the source current Is(Mp) is plotted whose absolute value is equal to the drain current but the negative sign is eliminated. The current is now displayed against the variation of the transistor gate potential. The final characteristic results by changing the *Ox* axis variable to *3-V_{dp}*.



17. Determine the drain-source resistance of the transistor by measuring the slope of the output characteristic around the operating point of exercise 9. Compare the measurement result with the resistance calculated by the simulator during the analysis of the operating point.

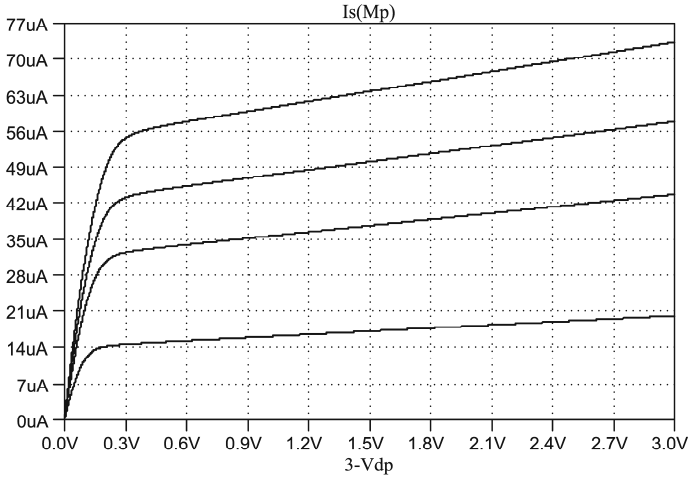
Both cursors will be attached to the plotted source current and placed at two distinct positions around the 50µA value. Read the *Slope* parameter from the measurement window. The slope is equal to the drain source conductance g_{DS}, while its reciprocal gives the drain-source resistance r_{DS}. The measured resistance is consistent with the value from the small signal parameter table.

$$r_{DS} = \frac{1}{Slope} = \frac{1}{g_{DS}} = \frac{1}{5.52 \cdot 10^{-6}} \cong 181\text{k}\Omega$$

18. Add a parametric analysis and plot the family of curves emphasizing the variation of the output characteristic with the source-gate voltage of the transistor.

The main variable V_{dp} remains the same. A secondary sweep is added to the simulation profile that will vary the transistor gate voltage V_{gp} according to the following list of values: 2.15V, 2.2V, 2.25V, 2.35V. The Spice command on the schematic is *.dc Vdp 0 3 1m Vgp list 2.15 2.2 2.25 2.35*.

The family of output characteristics is obtained by plotting the source current Is(Mp) and then changing the variable on the *Ox* axis to *3-V_{dp}*.



Homework:

Repeat all the simulations and measurements for the NMOS transistor.