LUND UNIVERSITY

Department of
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LTH

ETIN25 – Analogue IC Design

Laboratory Manual – Lab 2

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Laboratory 2: Design and Simulation of an Operational Amplifier

The goal of this laboratory is for you to design a two stage operational amplifier (OP-amp) from given specifications, simulate it in Cadence and compare the simulated result with your calculated design.

Introduction

An OP-amp consist of a number of transistors and it can be difficult to know where to start you design. Which transistor or which specification should be the starting point? There is not one correct answer to this question and experience from earlier designs is a great advantage. To help you get started this manual start with a design example of one way to design an OP-amp from a specification. Read it, and the suggested pages from the book, to get a good understanding of what you are doing and how to design the OP-amp. This will help you to prepare for the exam as well. Note that the specification and results used in the example is not the same as in the laboratory.

The finished OP-amp will be connected in a non-inverting configuration with capacitive load and feedback. See the schematic in figure 1, R_1 in the feedback is there to create a DC feedback for the amplifier and it does not interfere in small signal design if chosen large enough, (with large enough analogue designers mean that it has to be at least 10 times larger than the surrounding component values). This will result in small or non-noticeable deviations from the desired result. In this case we want to create a DC feedback that does not influence our small signal behavior, i.e. it needs to be large in comparison with the impedance from the feedback capacitors.

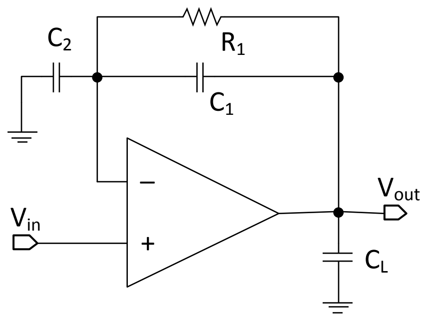

Figure 1: Non-inverting amplifier.

Design example

For the design example below, the body effect is partly ignored, and it is assumed that $\lambda V_{DS} \ll 1$. Long-channel approximations are used. The specifications for the closed-loop circuit of figure 1 are the following:

- $A(s) = 2\ (in - band)$ (closed loop gain)
- $\omega_0 = \omega_{-3dB,CL} = 2\pi \cdot 19 \cdot 10^6\ rad/s$ (unity gain frequency)
- $SR = 30V/\mu s$ (slew rate)
- $\phi_m > 70°$ (phase margin)
- $R_1 > 100M\Omega$
- $C_L = 1.5pF, C_1 = C_2 = 1pF$

Note: The specifications and resulting values are different from the laboratory assignment.

The schematic of the OP-amp is found in figure 2.

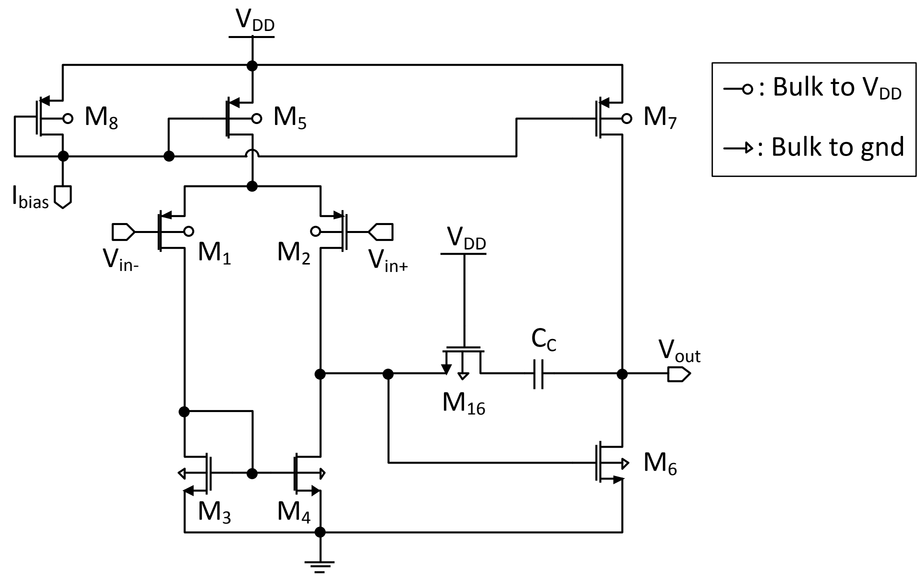

Figure 2: Schematic of the OP-amp

We start by choosing C_C = 2pF, which is approximately the same value as the total capacitance between the OP-amp output and ground. Page 690 in the text book, eq (9.144), discusses the load of an OP-amp. C_C is a compensation capacitor to ensure stability. Compensation is described in section 9.4 page 633-664 and especially sections 9.4.1, 9.4.2 and 9.4.3 is of interest for this laboratory. To give a quick summary:

The goal for compensation is the phase margin, ϕ_m. and it is a measure of the amplifiers stability. The transistors have a frequency dependency due to its parasitic capacitances and at higher frequencies the gain will start to roll of due to poles from these parasitics. The phase will also be affected by the poles, thus the output signals phase is frequency dependent. The frequency where the gain has decreased to 1, or 0dB, is called the unity gain frequency and if the phase shift is 180°, or more, at that frequency the amplifier will be unstable and start to oscillate when the feedback loop is closed. A negative feedback of an amplifier with 180° phase shift results in a positive feedback. The phase margin is the difference between 180° and the phase shift at the unity gain frequency. With the compensation capacitor we create a dominant pole at a low frequency which will move the unity gain frequency down in frequency where the phase shift is smaller. In this way we sacrifice bandwidth for the sake of stability. A phase margin of at least 45° is a good rule of thumb. See figure 9.12 on page 634 in the text book.

C_C needs to be large, a few pF is often enough, but to find the optimal value iterations through simulation need to be done.

Next we will look at the slew rate, section 9.6 pages 681-693 in the text book. The slew rate is a measure of how fast the amplifier is, how much current it can deliver and how fast. A good example of the result of a slew rate limited amplifier is found in figure 9.57 page 693 in the text book. To measure the slew rate, a step function should be applied to the input.

The slew rate will determine the value of the currents in both the input and output stage and it is a good place to start the design. If the first stage is limiting the slew rate we need to determine the maximum current that can be delivered and what capacitance that loads the stage. Looking at the input stage the maximum current that can be delivered is I_{DS5} when a step function is applied (M_1 is turned off and M_2 opened). The output node of the first stage, the drain of M_2, is loaded by C_{gs6} and C_C ($C_{gs6}||C_C \approx C_C$). We now have:

$$SR = I_{DS5}/C_C$$

The same analysis for the output stage gives:

$$SR = I_{DS7}/(C_C + C_L + C_1||C_2)$$

And thus:

$$I_{DS5} > SR \cdot C_C = 30\,V/\mu s \cdot 2pF = 60\mu A$$

$$I_{DS7} > SR \cdot (C_C + C_L + C_1||C_2) = 30\,V/\mu s \cdot (2 + 1.5 + 1||1)pF = 120\mu A$$

Now to find the dimensions of the input and output stage we need the transconductance of M_1, M_2 and M_6.The transconductance can be determined by the bandwidth, gain and phase margin considerations. First we take a look eq. 9.47 on page 648 in the text book which gives us the poles for the compensated amplifier in figure 9.24(a), (this is the same amplifier as in figure 2). In eq. 9.47 all parasitic capacitances except C_{gs} where neglected. To determine the poles of another amplifier you will have to do a small signal equivalent schematic of the transistors in the amplifier and calculate the transfer function. This is a good exercise and you are encouraged to do it on the OP-amp of this laboratory. The poles from eq. 9.47 are:

$$p_1 = -\frac{1}{g_{m6}R_2R_1C_C}$$

$$p_2 = -\frac{g_{m6}}{C_{gs6} + C_L + C_1||C_2}$$

$$p_3 = -\frac{1}{R_{16}C_{gs6}}$$

where

$$R_1 = r_{o2}||r_{o4} \qquad\qquad R_2 = r_{o6}||r_{o7}.$$

We will get back to R_{16} and remember the difference between r_o and R_{ON}. The later is the channel resistance in the linear region and it is V_{GS} dependent; this will be used in R_{16}. r_o is the channel resistance in saturation, or output resistance in saturation, and is described on page 74 in the text book.

Another relation that is used in amplifier design is the Gain-Bandwidth product (GBW). It is a product between the low frequency gain and the frequency of the first pole. In a one pole system the opened and closed loop GBW is constant because the pole is moved up in frequency by the same amount as the gain is lowered. This is explained in section 9.2, pages 624-626, in the text book. Figure 9.2 at page 625 illustrate this well.

If we decide to move the second pole to a frequency higher than ω_0 we can regard the system as a single pole system and because the closed loop gain is just 2 we can approximate that the first pole of the closed loop amplifier will be at ω_0. This approximation works quite well for higher closed loop gain as well but the higher the gain the more careful you have to be.

From above we have the first pole of the open loop amplifier, we also know the unity gain frequency and A(0) from the specification and we need to find the low frequency gain of the open loop amplifier. Page 649 eq. (9.50) gives us the answer; again you are encouraged to do a small signal equivalent circuit and try to find it yourself.

$$a_0 = g_{m1}(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7}) = g_{m1}g_{m6}R_1R_2$$

We can now set up two expressions for the GBW and determine g_m of the input stage.

$$\begin{cases} GBW[Hz] = a_0 f_{p1} = g_{m1}g_{m6}R_1R_2 \cdot \dfrac{1}{2\pi \cdot g_{m6}R_2R_1C_C} = \dfrac{g_{m1}}{2\pi C_C} \\ GBW[Hz] = A_0 f_{p1closed} \approx A_0 \dfrac{\omega_0}{2\pi} \end{cases}$$

$$\frac{g_{m1}}{2\pi C_C} = A_0\frac{\omega_0}{2\pi} \Leftrightarrow g_{m1} = A_0\frac{2\pi C_C\omega_0}{2\pi} = 2\cdot 2pF\cdot 2\pi\cdot 19\cdot 10^6 rad/s \approx 480\mu S$$

Now we can find the dimensions of $M_{1,2}$:

$$(W/L)_{1,2} = \frac{g_{m1,2}^2}{2k_p' I_{DS1,2}} = \frac{g_{m1,2}^2}{2k_p' I_{DS5}/2} = \frac{(480\mu)^2}{2\cdot 100\cdot 10^{-6}\cdot 60\cdot 10^{-6}/2} = 38.4$$

This can be rounded off to $(W/L)_{1,2} = 40$.

To find g_{m6} we look at the phase margin once more. The phase margin can be calculated according to:

$$\phi_m(\omega_0) = 180° - \arctan(\omega_0/\omega_{p1}) - \arctan(\omega_0/\omega_{p2})$$

A pole will turn the phase 90° over 2 decades of frequency and after the first pole we only have 90° left for the phase margin specification of 70° and one pole to go. It is clear that the second pole has an impact on the phase margin and when we looked at the GBW we approximated the system to only have one pole. If we move the second pole high above ω_0 the approximation will be accurate and the phase will be marginal effected by the second pole. If we start with placing the pole at $3\omega_0$ we fulfill the one pole approximation and we get a phase margin of:

$$\phi_m(\omega_0) = 180° - \arctan(\omega_0/\omega_{p1}) - \arctan(\omega_0/\omega_{p2}) = [\omega_{p2} = 3\omega_0] =$$

$$= 180° - 90° - \arctan(1/3) = 71.6° > 70°$$

We then look at eq. 9.47 once again and determine g_{m6} (we approximate C_{gs6} to be in the range of 100fF):

$$p_2 = -\frac{g_{m6}}{C_{gs6} + C_L + C_1||C_2} = 3\omega_0 \Leftrightarrow g_{m6} = 3\omega_0\left(C_{gs6} + C_L + C_1||C_2\right) = 750\mu S$$

And now the dimensions of M_6:

$$(W/L)_6 = \frac{g_{m6}^2}{2k_n^{'} I_{DS6}} = \frac{(750\mu)^2}{2 \cdot 400 \cdot 10^{-6} \cdot 120 \cdot 10^{-6}} = 5.85 \approx 6$$

This is quite a small ratio, and we can afford to increase the above ratios (rather arbitrarily), without loading the output of the differential stage too much. With this, analogue designers, mean that if we increase the dimensions of M_6 the capacitive load of the first stage will increase as the parasitic capacitances, such as C_{gs6}, will increase but that node is already loaded by C_C which is much larger than the parasitic even if we increase M_6 (within reason). So we choose:

$$(W/L)_6 = 50$$

This will of curse increase g_{m6} and a larger g_{m6} will increase the second pole which increases the phase margin so it is a win-win situation. A larger device is also less sensitive to mismatch. The new value of g_{m6} will be 2.2mS.

A short summery of what we done so far:

- We started to choose a value for C_C. We know that we need to compensate the amplifier to ensure stability. Experience tells us that we can use quite a large capacitor when we are aiming for a low unity gain frequency as 19 MHz.
- Next we used the slew rate specification to decide the current needed to be delivered by each stage. This is a good starting point as it set directions for both the input and output stage.
- To get g_m of the input transistors we found the expressions for the poles in the system and the gain bandwidth product and made the assumption that the second pole would be at high enough frequency so we could consider the amplifier to only have one pole. With this we could set the dimensions of the input transistors.
- Last we looked at the phase margin to get g_m of the output transistor. With the assumption that p_2 would be larger than ω_0 we found g_m and then the dimensions of M_6.
- As M_6 turned out to be quite small we increased it in size. This improved the phase margin and minimize mismatch and as we didn't altered the total load the internal node between the input and output-stage we know that this will only affect the earlier results marginally.

We now continue with the active load of the input stage, M_3 and M_4. The drains of M_1 and M_2 should ideally have the same potential and looking at the schematic in figure 2 we see that this will be the same potential as on the gates of M_3 and M_4 as well as of the gate of M_6. Thus we will have the same V_{GS} of all three transistors. This is described more at page 425 and eq. 6.62 and 6.63 in the text book. The relation between the dimensions of the transistors and their I_{DS} is:

$$\frac{(W/L)_6}{(W/L)_{3,4}} = \frac{I_{DS6}}{I_{DS5}/2}$$

from which it follows that

$$(W/L)_{3,4} = (W/L)_6 \frac{I_{DS5}/2}{I_{DS6}} = 50 \cdot \frac{30 \cdot 10^{-6}}{120 \cdot 10^{-6}} = 12.5 \approx 12\,.$$

Now we need to take a step back and look at the frequency dependence and phase margin again. Page 640, figure 9.18 and eq (9.27a) shows that the C_{GD6} together with g_{m6} creates a zero in the right half plane. Due to the low g_m in a MOS-transistor and the fact that our compensation capacitor, C_C, is in parallel with C_{GD6} the zero will appear at a quite low frequency causing instability. Looking at figure 9.20, page 643, in the text book we can see that the zero appears between the two poles before the unity gain is reached. This stops the gain from rolling off, pushing the unity gain frequency up in frequency, as well as shifting the phase -90°, which is totally devastating for the phase margin. (A zero in the left half plane shifts the phase +90°). Our assumptions earlier about a single pole system and placing the second pole at a high frequency will be inaccurate. Section 9.4.3, pages 643-650, address the issue and solutions to the same. We will solve it by moving the zero to infinity with a resistor, R_Z, which we will implement with the transistor M_{16} (we called this resistor R_{16} earlier). This will add a third pole at high frequency, which will not influence the behavior of the amplifier at the frequencies of interest, and change the zero according to:

$$z = \frac{1}{(1/g_{m6} - R_Z)C_C}$$

$$p_3 \approx -\frac{1}{R_Z C_{GS6}}$$

If $R_Z = 1/g_{m6}$ the zero will be at infinity and it is no problem if R_Z deviates a bit from $1/g_{m6}$. As long as the difference is small the zero will appear at a very high frequency, either in the left or right half plane.

We will, as mentioned, use M_{16} to realize R_Z. M_{16} will be working in the linear region so we can easily implement a resistance of desired value as g_{m6} is known.

$$R_{ON,16}^{-1} = g_{m6}$$

In the linear region, we have (see Eq. 2.53 in the textbook)

$$R_{ON,16}^{-1} = k_n^{'}(W/L)_{16}(V_{GS16} - V_{th16})\,.$$

(Here we ignore V_{DS16} as no DC current will flow through the transistor, $V_{DS16} \approx 0$. C_C blocks the DC current). Note that

$$V_{S16} = V_{G6} = V_{th6} + \sqrt{\frac{2I_{DS6}}{k_n^{'}(W/L)_6}} = 0.3 + 0.11 = 0.41V$$

Because we connect the gate of M_{16} to $V_{DD} = 1.2V$ we get a $V_{GS} = 0.79V$ and moreover

$$V_{th16} = V_{th0n} + \gamma\left(\sqrt{2\phi_{fn} + V_{S16}} - \sqrt{2\phi_{fn}}\right) = 0.3 + 0.58\left(\sqrt{0.7 + 0.41} - \sqrt{0.7}\right) = 0.43V\,.$$

Thus,

$$(W/L)_{16} = \frac{g_{m6}}{k_n'(V_{GS16} - V_{th16})} = \frac{2.2 \cdot 10^{-3}}{400 \cdot 10^{-6}(0.79 — 0.43)} = 15.28 \approx 15$$

Finally, the current sources M_5 and M_7 can be designed. Here we are a bit free to do as we like to get the right drain-to-source current. A smaller transistor requires a larger overdrive voltage, V_{ov}, while it occupies a smaller area and vice versa with a larger transistor. A larger transistor is, however, less sensitive to mismatch and the area of a single transistor today is not a big issue (in most cases) and especially in the difference between the two ratios we are talking about here. We choose large transistors for our design and if we set V_{ov} to 0.14V we obtain

$$(W/L)_5 = \frac{2I_{DS5}}{k_p' V_{ov}^2} = \frac{2 \cdot 60 \cdot 10^{-6}}{100 \cdot 10^{-6} \cdot 0.14^2} = 61.22 \approx 60$$

$$(W/L)_7 = \frac{2I_{DS6}}{k_p' V_{ov}^2} = \frac{2 \cdot 120 \cdot 10^{-6}}{100 \cdot 10^{-6} \cdot 0.14^2} = 122.45 \approx 120$$

For convenience we choose $(W/L)_8 = (W/L)_5$ and $I_{bias} = I_{DS5}$. As usual in analogue designs, it is good practice to choose transistor lengths and widths (much) larger than the smallest allowed by the process, since in this way we obtain a better match between transistors, and the transistors behave more in accordance with the long-channel approximation. A possible choice is a common length of 0.5µm, resulting in the following dimensions:

Transistor	W (µm)	L (µm)
M_1	20	0.5
M_2	20	0.5
M_3	6	0.5
M_4	6	0.5
M_5	30	0.5
M_6	25	0.5
M_7	60	0.5
M_8	30	0.5
M_{16}	7.5	0.5

Note that the major loss from using larger transistors, and especially longer, is speed. If we would like to create a circuit for higher frequencies, e.g. a radio receiver in the GHz area, we would have used minimum length transistors.

Now we can try to estimate the DC-gain of the OP-amp and we use the same equation as before, eq. 9.50:

$$a_0 = g_{m1}(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7})$$

From the text book (Eq. 1.163, 1.164 and 1.194) we see that

$$r_o = \frac{dX_d}{dV_{DS}}^{-1} \frac{L_{eff}}{I_D}$$

where the effective transistor length

$$L_{eff} = L - 2L_d - 2X_d$$

Thus,

$$r_{o2} = (0.04 \cdot 10^{-6})^{-1} \frac{0.485 \cdot 10^{-6}}{30 \cdot 10^{-6}} = 404.17k\Omega \approx 404k\Omega$$

$$r_{o4} = (0.08 \cdot 10^{-6})^{-1} \frac{0.485 \cdot 10^{-6}}{30 \cdot 10^{-6}} \approx 202k\Omega$$

$$r_{o6} = (0.04 \cdot 10^{-6})^{-1} \frac{0.485 \cdot 10^{-6}}{120 \cdot 10^{-6}} \approx 101k\Omega$$

$$r_{o7} = (0.08 \cdot 10^{-6})^{-1} \frac{0.485 \cdot 10^{-6}}{120 \cdot 10^{-6}} = 51k\Omega$$

Now we end this example by calculation a_0:

$$a_0 = 480 \cdot 10^{-6} \cdot (404 \cdot 10^3 || 202 \cdot 10^3) \cdot 2.2 \cdot 10^{-3} \cdot (101 \cdot 10^3 || 51 \cdot 10^3) \approx 4.8 \cdot 10^3 = 73.6\ dB$$

Homework

1. Read this manual carefully especially the design example. Read the pages in the book that is referred to in the example. This will give you a better understanding of what you are doing and why.
2. Draw the schematic of your OP-amp in Cadence, see figure 2. Calculate all the bias currents and dimensions for the devices and mark the results in your schematic. You should meet the following specifications (not the same as in the example):

$A(s) = 2\ (in - band)$	(closed loop gain)
$\omega_0 = \omega_{-3dB,CL} = 2\pi \cdot 18 \cdot 10^6\ rad/s$	(unity gain frequency)
$SR = 25V/\mu s$	(slew rate)
$\phi_m > 60°$	(phase margin)
$R_1 > 100M\Omega$	
$C_L = 2pF, C_1 = C_2 = 2pF$	

   Choose M_{16} so that the zero introduced by C_C is at infinity and choose C_C to be 1pf, 2pF or 3pF. The supply voltage, V_{DD}, should be set to 1.2 V.
3. What is the order of magnitude of the input offset voltage, and how does it impact open-loop simulations and measurements?
4. How can the loop gain be measured? Indicate this in fig 5.
5. Try to finish as much of the lab as possible before the lab starts. You should at least have created your schematic of the OP-amp and preferably done a DC simulation to check that the bias currents are correct.

Design and Simulation of an Operational Amplifier

Start by creating a new schematic cell in your laboratory library, as you did in the first laboratory session, and create a schematic according to figure 2. Use the calculated dimensions from the homework exercise for your transistors. Use MIMCAPS_MML130E, from the library umc13mmrf for the compensation capacitor. For the transistors you should use P_12_HSL130E and N_12_HSL130E. Don't forget to add pins to your schematic and use inputOutput pins (p).When you are done create a symbol for your schematic.

Next you should create a test bench for you OP-amp according to figure 3. Use the schematic view and insert your OP-amp together with the other circuit elements. For the test bench you should use capacitors and resistors from analogLib. Use a variable called Voffset in the DC source between the two inputs of the OP-amp. When your test bench is ready you should save it and open Analog Environment to setup the simulations as you did in the first laboratory session.

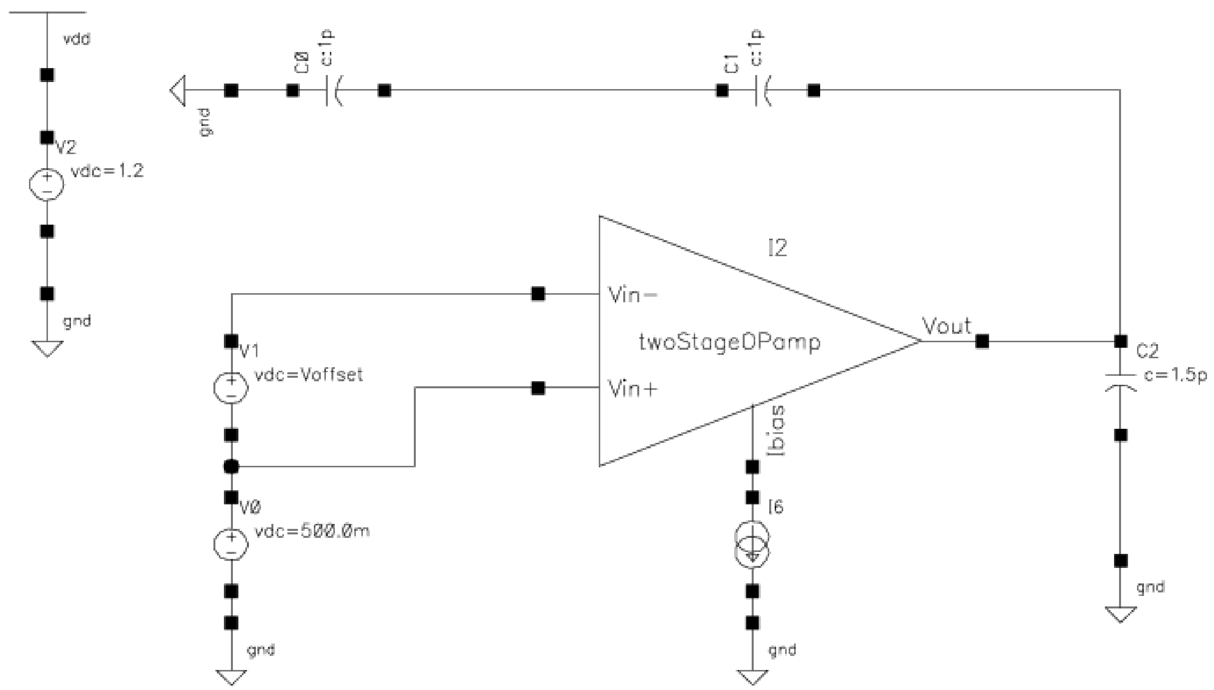

Figure 3. Test bench for open loop simulations.

Start with a DC simulation, "Analyses –> Choose …". Save the DC operating points and select a sweep of Voffset. Choose reasonable values for Voffset and find the value where the DC voltage of the output node is 0.5V. In many applications you would like the output node voltage to be in the middle of the available supply voltage, in our case 0.6V (V_{DD} = 1.2V and ground = 0V). However, here this voltage will also set the common voltage of all our bias sources so to grantee that M_5 is in saturation we choose 0.5V. Use the calculator to see how the DC currents and g_m of the input and output stage varies with Voffset.

When you found the right value for Voffset, write it in Analog Enviroment and turn off the sweep and do a new DC simulation. Do the simulated I_{DS5}, I_{DS7}, $g_{m1,2}$ and g_{m6} match the calculated values? Adjust the dimensions of the transistors if needed.

Now you should investigate the open loop gain, ϕ_m, and ω_0. Add vsin from analogLib as your input source in your test bench and set the AC magnitude to 1 V. You find this parameter in the bottom of the list of all parameters for vsin. The first parameters for frequency and amplitude are used in e.g. transient simulations. Set up the AC simulation in Analog Environment, “Analyses –> Choose … -> ac” and sweep from 10Hz to 1 GHz. See figure 4. When the simulation is done choose “Results -> Direct Plot -> AC Gain & Phase”, click on the output node and then on the input node. A graph of the phase and gain as a function of the frequency should appear, save it for the lab rapport with ϕ_m, and ω_0 marked in the graph. Compare with the homework assignment.

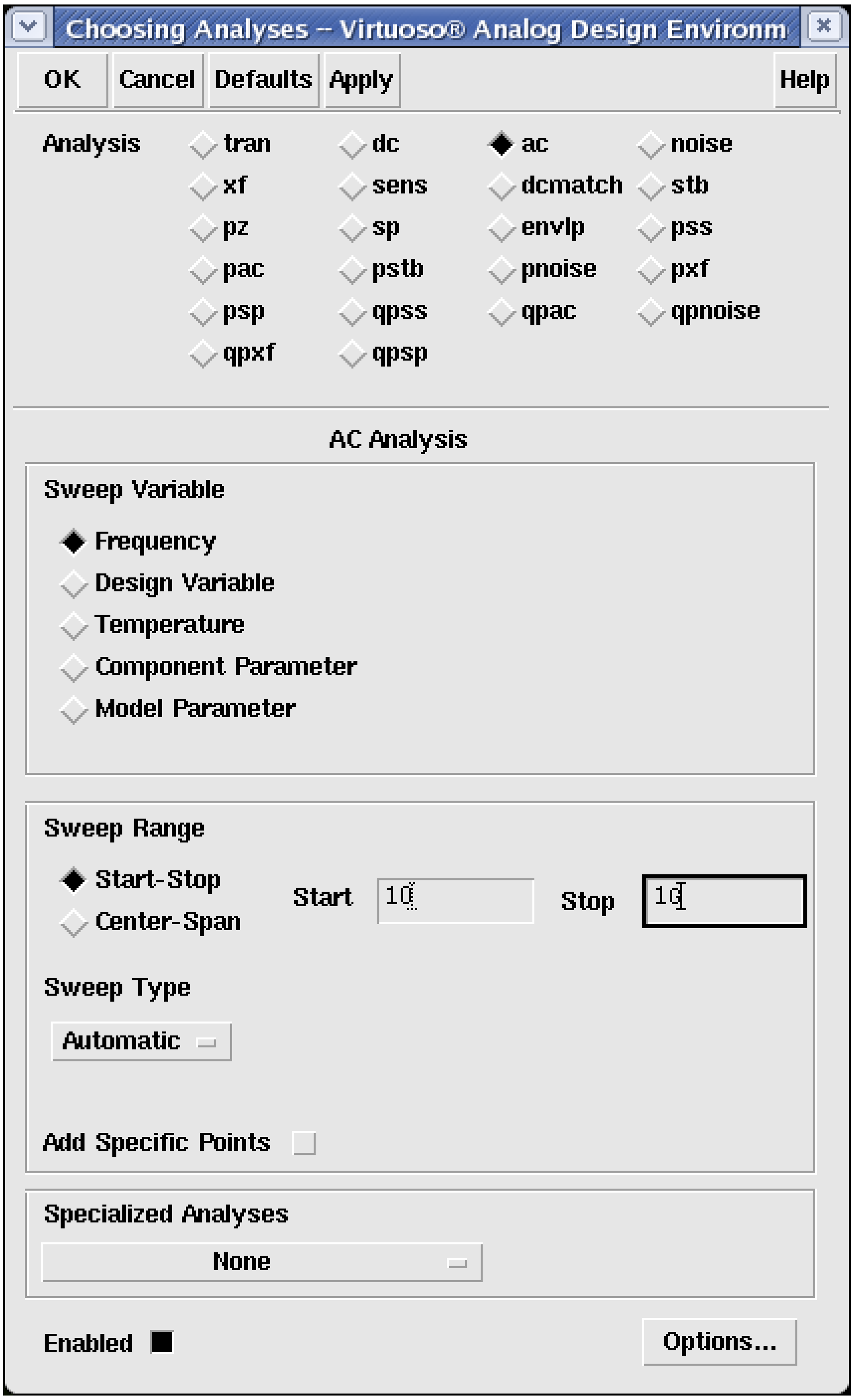

Figure 4. AC-simulation setup.

Do the simulations once more but this time you should remove the compensation capacitor and M_{16}. Just remove the wires and not the actual instances as you will need them again. It is ok to simulate with warnings that appear when you press “Check and save” but if you want to remove the warnings you can add the instance “noConn” from the library “basic” to the non connected nodes. Compare the result with the compensated OP-amp. Are there any differences from the compensated OP-amp? Discuss/ explain in the rapport. Connect the compensation again.

Now it is time to close the loop so the test bench looks like the schematic in figure 5. Do the AC simulation again and measure A(s), the closed loop gain, like you did in the open loop case. Are there any differences from the open loop case? Discuss/ explain in the rapport.

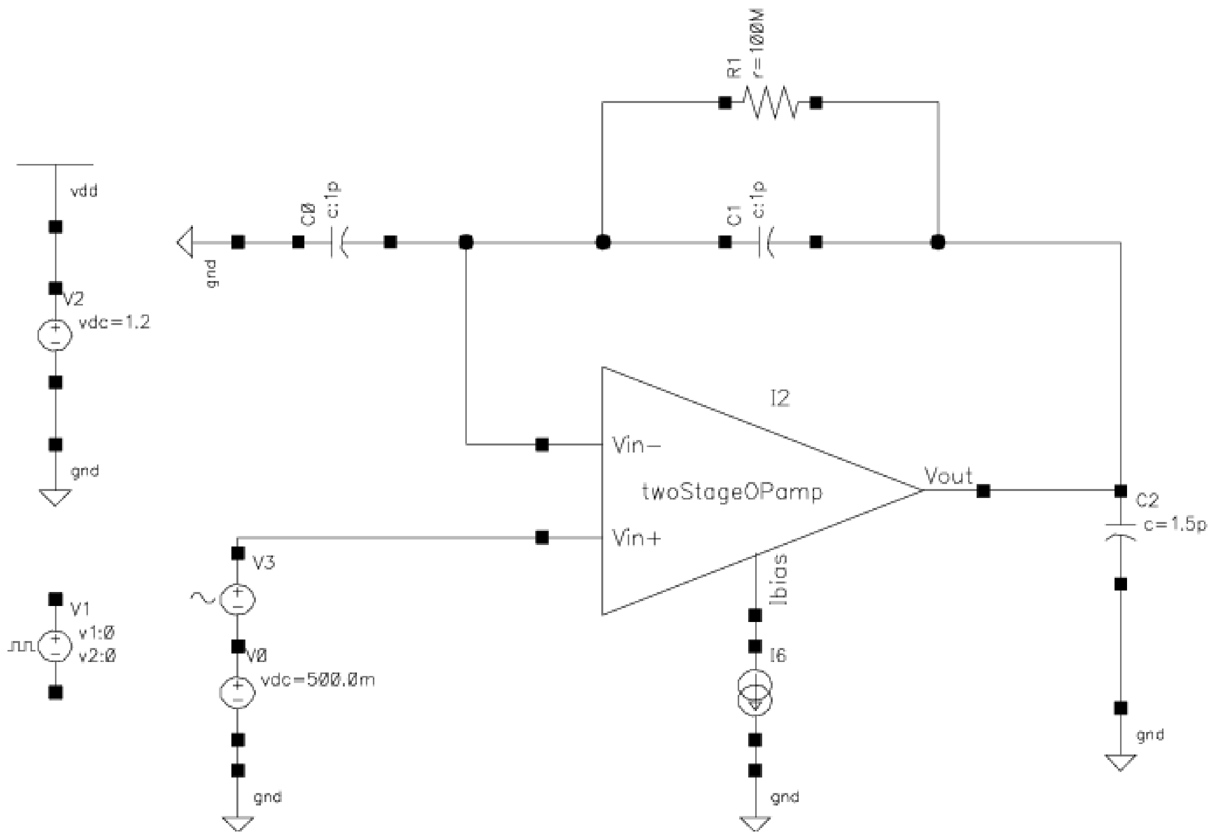

Figure 5. Test bench for closed loop simulations.

Next you should measure the slew rate of the OP-amp. Remove the vsin source for now and add a vpulse from analogLib. Check the properties of the vpulse and change the values to get a symmetrical 0.5V step around your dc input of 500mV. (Hint: -250mV to 250mV). Set up a transient simulation in Analog Environment and choose a reasonable “Stop Time” and “conservative” “Accuracy Defaults”. When the simulation is done go to “Results -> Direct Plot -> Transient signal”, click on the output node and the press the escape button. Zoom in in the graph so you only see one rising or falling edge but make sure that you have some of the flat parts before and after the edge as well. To measure the SR, open the calculator and choose wave and click on the wave in the graph. Then go to “Special Functions” and choose “slewRate …” and fill in the new window appearing. For “Initial Value” and “Final Value” use the “y” option and think of which is your initial and final value. When you are done just click “OK” and the “print” on the calculator and check the “Result Display Window”. See figure 6 for an example, make sure that you don't copy the initial- and final value. Look at you plot to find them!

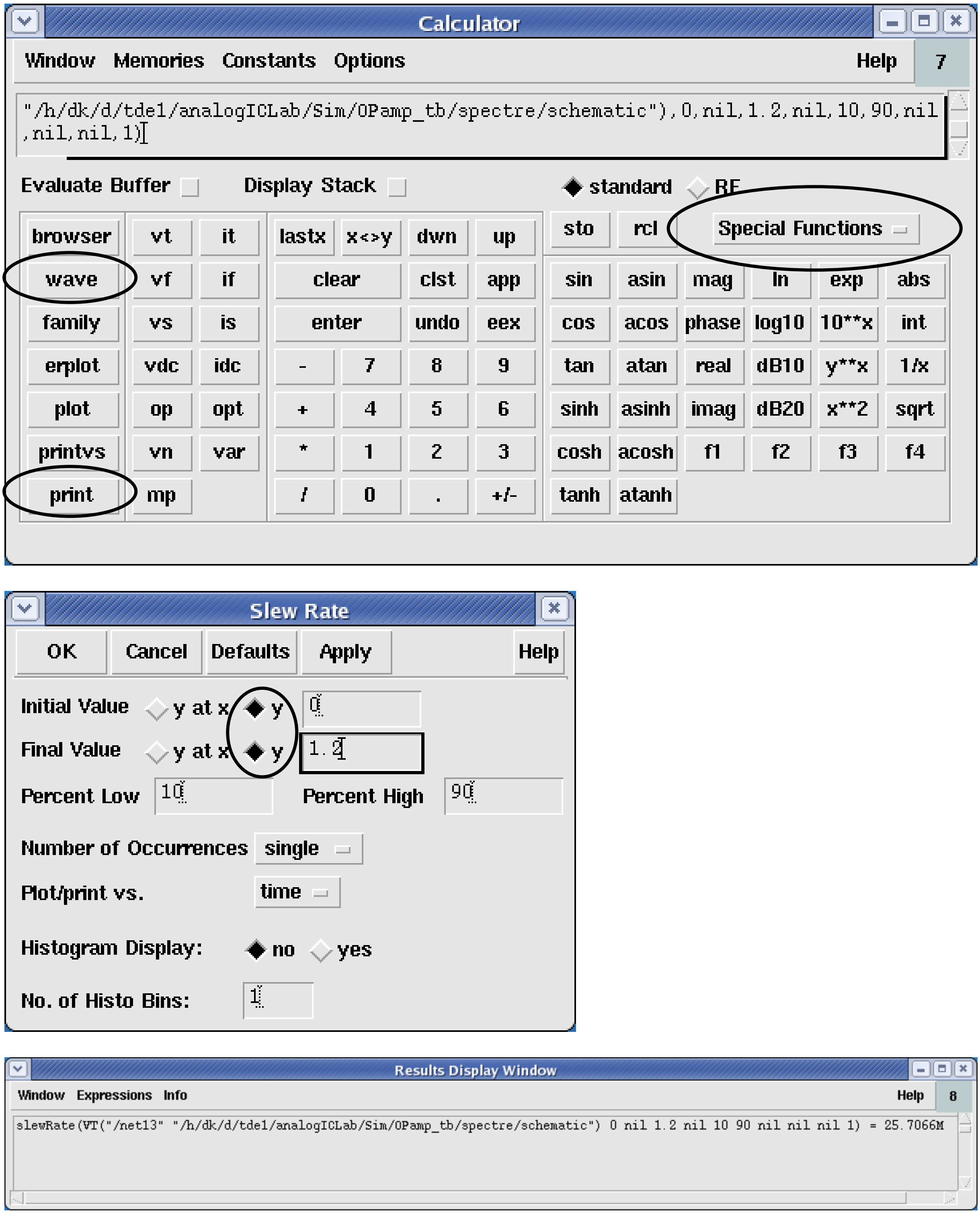

Figure 6. Setup for slew rate measurement.

You can also see page 681-682 in the text book. Does the SR deviate from the specification? Measure the SR both at the positive and negative flank.

Increase and decrease the capacitive load by a factor of 10 and repeat the transient simulation. What happens to the output and why? What is the new SR?

Laboratory Report

Compose a report containing the difference of calculated and simulated values. Include the values of the open loop gain, ϕ_m, ω_0 and SR. The report should also answer the questions in the homework section, and explain the results. Include plots of the simulated figures.