Bumping Design Guide

Revised: May 2009

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1 Contact Information

To start your relationship with FlipChip International, contact the appropriate Sales Representative. Each is an expert at learning the particular needs of your device. In addition, your FlipChip Sales Representative can discuss all aspects of pricing, logistics, cycle time, and answer any other question you may have.

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2 Introduction

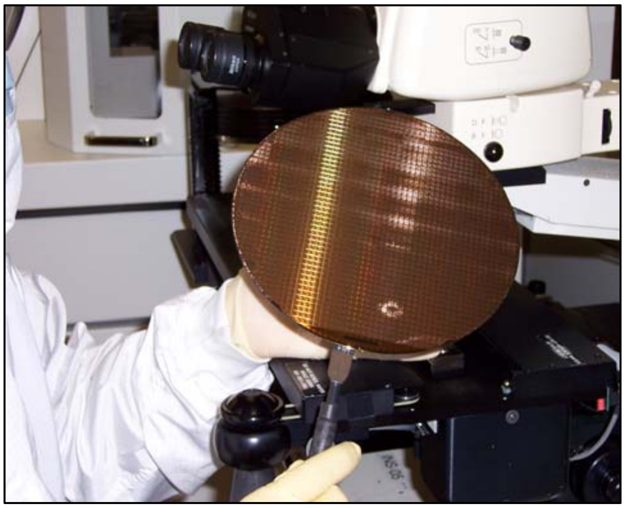
2.1 Overview

Thank you for your interest in FlipChip International, LLC for your wafer bumping needs. This guide will take you through the process of deciding which bumping flow is right for you. In addition, this guide will give you the basics of each process flow, incoming wafer requirements, device requirements, material properties, and a glossary, so you may have a better understanding of FCI's broad bumping technology options.

2.2 History

FlipChip International, LLC (FCI) began in 1996 as Flip Chip Technologies (FCT), a joint venture between Delco Electronics Systems and Kulicke & Soffa Industries (K&S). Delco contributed the patented Flex-On-Cap (or FoC) flip chip process and over 30 years of flip chip experience from the automotive industry to this partnership. K&S added its knowledge and leadership position as the world's largest supplier of semiconductor assembly equipment. The company's Flex-on-Cap (FoC) standard flip chip bumping technology quickly became the industry standard for flip chip bumping.

In 1998, FCT developed and patented the *Ultra*CSP® Wafer Level Chip Scale Package (WLCSP), which quickly became the industry standard for WLCSPs. FlipChip began an aggressive licensing program to bring its unique bumping technology to a broader worldwide market. Today, the semiconductor industry's packaging heavyweights, including Amkor Technology, Advanced Semiconductor Engineering (ASE), Siliconware (SPIL), and STATS ChipPAC have licensed and use FlipChip's bumping technology as the foundation of their bumping capabilities.



In 2001, K&S acquired Delco's remaining interest in FCT and we became the Flip Chip Division of Kulicke & Soffa. In 2004, RoseStreet Labs, LLC, a private research and development company based in Phoenix, completed the acquisition of the assets of the Flip Chip Division from Kulicke & Soffa, through its newly formed subsidiary -- FlipChip International, LLC. In early 2005, FCI acquired IC Services, which became the Die Sales Division of FCI (or FCI-DSD). The Die Sales Division continues its long tradition of providing wafer thinning, dicing, Automated Optical Inspection (AOI), Waffle Pack, and Tape & Reel services.

Since 2005, FCI has been offering its flagship Spheron SFC and Spheron WLCSP product lines which are now widely accepted technologies in the portable handset space.

Also in 2005, FlipChip International licensed the Fraunhofer Institute's Electroless Ni/Au process leading to a new line of low cost flip chip and WLCSP CSP bumping offerings sold under the Elite UBM banner. Target applications of E-less Ni/Au UBMs include high temperature power devices, low cost RFID and WLCSP applications. The new process has been in commercial production since mid-2006 at our FCMS joint venture in Shanghai.

In 2006, FlipChip entered into a joint venture with Millennium Microtech Shanghai (MMS) to form FlipChip Millennium Shanghai (FCMS). FCMS opened in March of 2007 and provides "Full Turn-Key" wafer bumping and die packaging services, focusing on the Asian market. FCI's Elite SFC and Elite WLCSP product offerings were qualified and fully deployed at FCMS during the remainder of 2007. Also in 2007, FlipChip entered into strategic partnerships with select domestic test houses to enable the wafer sort as part of our Full Turn-Key supply strategy.

Since 2007, FCI-Phoenix has further broadened its product portfolio through the implementation of semi-additive Cu electroplating based processes which provide additional RDL and wafer bumping capabilities for WLCSP, embedded die and Cu Pillar Bumping applications on a growing range of substrate technologies including Silicon, Sapphire, and GaAs.

In 2008, FCI entered into an additional Asian joint venture with Unisem called Unisem-Advanpack Technologies (UAT) located in Ipoh, Malaysia. This joint venture provides a mutually beneficial, Asia based second sourcing option for FCI's customers using sputtered and electroplated Cu based wafer level processing technologies for wafer sizes up to 200 mm. In early 2009, FCI entered into a 300 mm wafer bumping partnership with Semiconductor Manufacturing International Corporation (SMIC) located in the Pudong area of Shanghai. This partnership further broadens FCI's abilities to support its wide range of Wafer Level Packaging product offerings across all standard wafer sizes.

In addition to offering the industry's broadest assortment of wafer bumping options, FlipChip has maintained an aggressive program to develop and generate intellectual property for future implementation at FlipChip-Phoenix and in our Asian factory locations. Our commitment to leadership and quality in wafer bumping solutions continues, ensuring that FlipChip remains the leader in developing, and bringing to market the latest in bumping technology.

The primary bumping facility and technology development site for FlipChip is located in the World Headquarters building in Phoenix, Arizona, USA. This facility is a state of the art 16,000-ft^2 (4700 m^2), class 1000 clean room. FlipChip – Phoenix is ISO9001:2000 and ISO14001 certified.

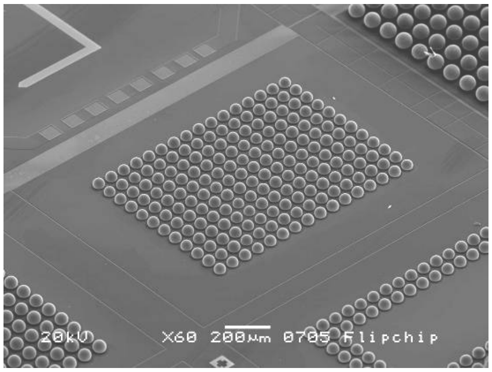
FCI World Headquarters – Phoenix, AZ, USA

Die Sales Division – Tempe, AZ, USA

Unisem / UAT – Ipoh, Malaysia

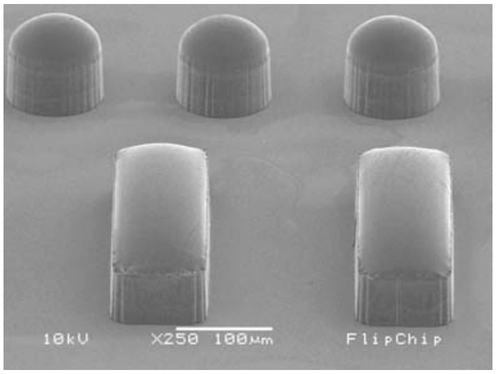
FCMS Bumping Facility – Shanghai, China

2.3 Flagship Product Offerings at a Glance



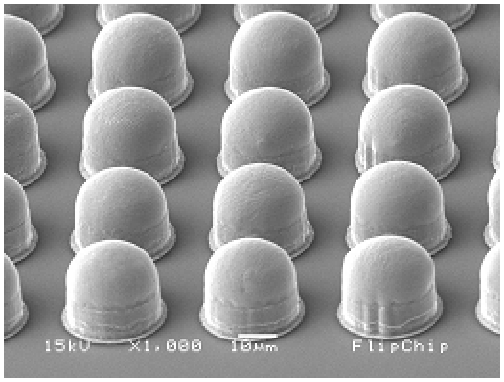
FCI’s Standard Flip Chip Bumping

(See Section 3.1)



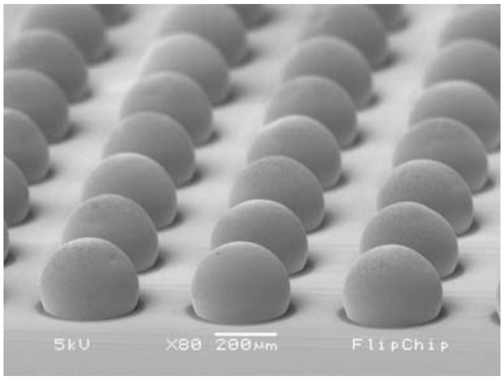
FCI’s Standard Cu Pillar Bumping

(See Section 3.4)



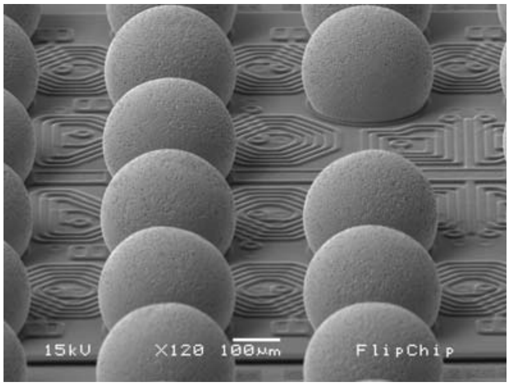
FCI’s NANOPillar Cu Pillar Bumping

(See Section 3.4)



FCI’s Spheron Sputtered RDL WLCSP

(See Section 3.5.1)



FCI’s Electroplated Cu Spheron RDL WLCSP

(See Section 3.5.2)

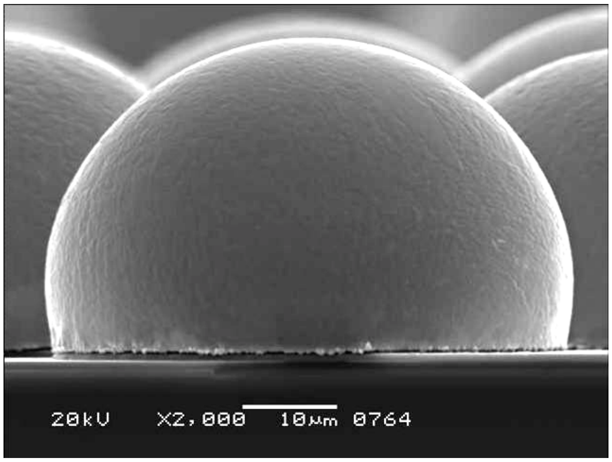
3 Choosing a Bumping Process

Here we look at the different Wafer Level Processing services offered by FlipChip. To make it easy, we have broken our services into the different processes. Each one is recommended for a different bumping situation, from the simplest to the most complex. Look these over and decide which process will meet your needs. If you still can't decide, give us a call! We'll be glad to walk you through our available options and help you select the process that will work best for your application. We are experts at matching up a standard process flow to your device. Keep in mind that we are a development driven engineering organization. For non-standard devices, we can design a custom process flow that will meet your application's specific requirements.

3.1 Standard Flip Chip – Bump on I/O

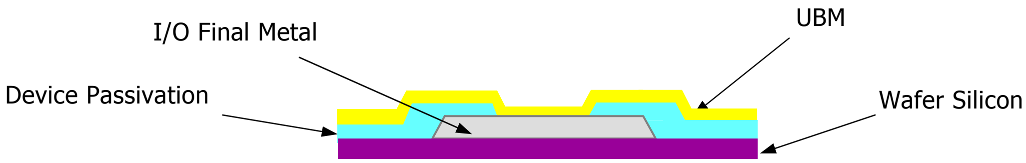
Our Standard Flip Chip (SFC) process, formerly known as the Flex-on-Cap (or FoC) process, was originally developed in the mid-1960's by Delco for use in the automotive industry. Today, the process has unsurpassed industry track record with 40 years and millions of bumped wafers behind it. This is the process to use when you need to place small bumps (less than 130μm in height) directly on the die I/O. Pitch capabilities in this process are typically 150μm or greater for a full array I/O or peripheral I/O design. Typically, the number of bumps per die ranges from 4 to 6000. The SFC process uses premixed solder paste for the solder bumps. This provides for outstanding control of the alloy composition across the entire wafer. Since the process is not limited to the bi-metal constraints of an electroplating process, a wide range of multi-metal solder alloys tailored to your application (such as Sn/Ag/Cu alloys) are available. As with all flip chip die processed with small bumps, these die will require the use of underfilling during packaging in order to achieve acceptable reliability.

To take advantage of this process flow, the device must meet some minimum I/O pad requirements (described below in section 3.1.2). If the device does not meet these minimum I/O pad requirements, refer to section 3.2, which outlines SFC Repassivation alternatives. If you are looking for bump heights greater than 130μm, refer to sections 3.5 and 3.6, and consider the *UltraCSP* and/or Spheron WLCSP flows.



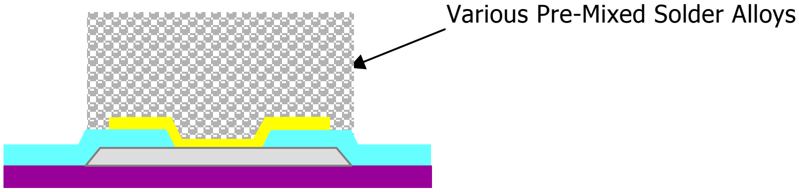
3.1.1 Standard Flip Chip-Bump on I/O Process Summary

The SFC-Bump on I/O process supports fine pitch flip chip applications to pitches well below 100μm. Below is an outline of the flow:

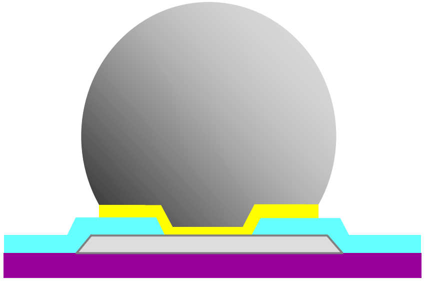


Sputter deposit three layer (Al/NiV/Cu) Under Bump Metallization (or UBM) stack.

Pattern the UBM pads.



Deposit the pre-mixed solder paste (proprietary process).



Reflow the solder.

3.1.2 I/O Requirements for the SFC-Bump on I/O Process

Since the SFC-Bump on I/O process forms a bump directly on the device I/O, certain criteria must be followed to ensure a reliable bump structure. The basic rule is what we call "The Golden Rule of Flip Chip", which is:

The UBM must overlap the I/O passivation opening by at least 8µm and the I/O final metal pad must extend at least 5µm past the end of the UBM.

Figure 1 shows the "Golden Rule" requirements for the UBM in relation to the passivation opening and the I/O metal bond pad. This rule requirement accomplishes several reliability requirements. The overlap of the UBM to the passivation opening provides a seal to the underlying I/O aluminum bond pad. The overlap of the UBM inside the I/O metal bond pad eliminates stresses that can cause silicon cratering.

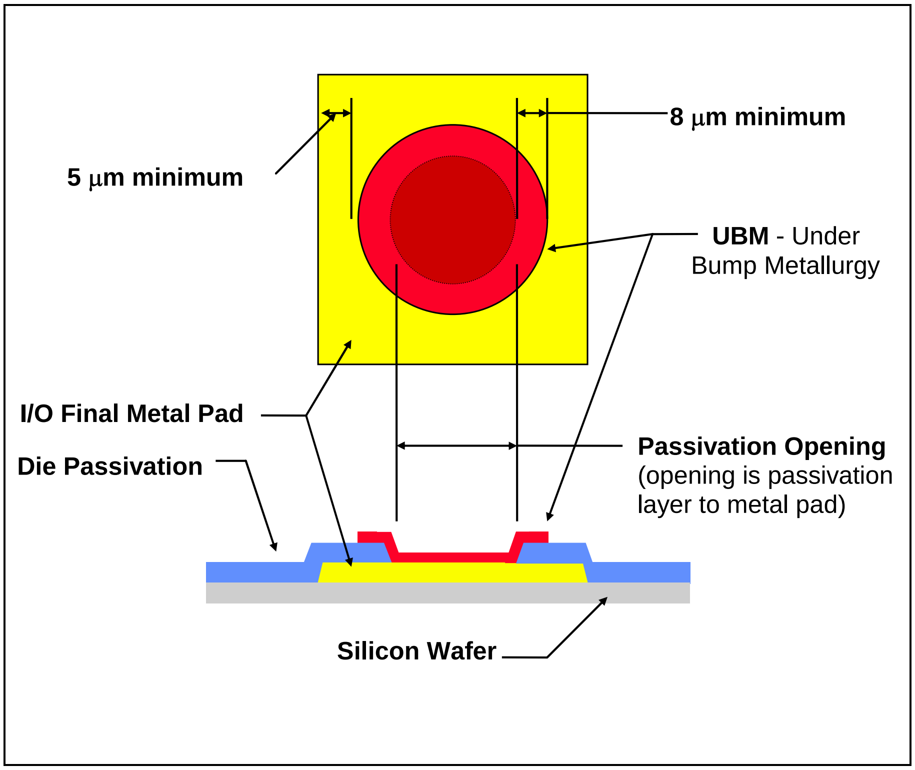


Figure 1: The Golden Rule of Flip Chip

The allowable size of the UBM is directly related to I/O Pitch. The bump height is strongly influenced by both I/O pitch and UBM size. Please see the section 6.1 "Pitch, UBM Size, and Bump Height Relationships" as a guide as to what size your UBM will be.

If your device does not meet the requirements of the Golden Rule, your device will likely be a candidate for one of our SFC-Repassivation process flows, which are outlined in section 3.2.

3.2 Standard Flip Chip - Repassivation

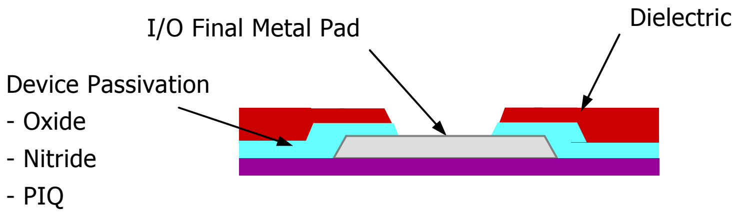
Our SFC-Repassivation process flows are similar to the SFC-Bump on I/O process, but support bumping applications that do not meet all of the I/O final metal pad and passivation opening requirements of SFC-Bump on I/O. In this process, a stress relieving layer of either Benzocyclobutene (BCB) or Spheron™ (an FCI proprietary high performance dielectric repassivation layer) is deposited on the die before bumping. The repassivation layer corrects for the issue of the I/O passivation opening being too small or too large for a standard flip chip bump. It also corrects for the issue of the I/O final metal pad being too small for a standard flip chip bump. The repassivation dielectric layer also planarizes the device surface and gives the bump structure additional strength and robustness.

As with SFC-Bump on I/O, SFC-Repassivation is designed for small bumps (less than 130μm) placed directly on the die I/O. Pitch capabilities in this process are typically 150μm or greater for full array I/O or peripheral I/O design. The number of bumps per die typically can range from 4 to 6000. The SFC-Repassivation process uses premixed solder paste for the solder bumps. This provides for outstanding control of the alloy composition across the entire wafer. Since the process is not limited to the bi-metal constraints of an electroplated solder process, multi-metal alloy (including Sn/Ag/Cu) options are readily available. As with all die processed with small bumps, die bumped with the SFC-Repassivation process will require the use of underfill during packaging.

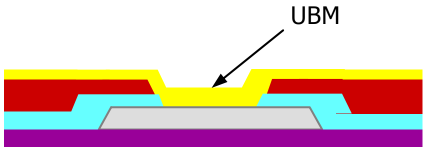
If your device contains bumps that will not be placed directly on the I/O, take a look at the next section 3.3, which describes the SFC-Redistribution flow. If you are looking for bump heights greater than 160μm, take a look at section 3.5 and 3.6, which covers the Spheron and *UltraCSP* WLCSP flows – the industry's standards in Wafer Level Chip Scale Packaging solutions.

3.2.1 SFC-Repassivation Process Summary

The SFC-Repassivation process requires relatively few process steps to complete the flow. Below is an outline of the process flow for BCB or Spheron polymer (none of the drawings are to scale):

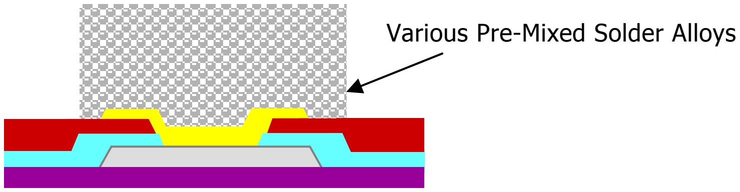


Deposit and pattern a layer of BCB or Spheron dielectric / passivation.

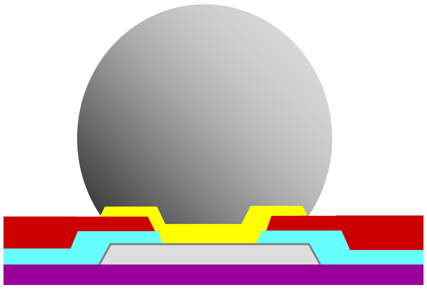


Sputter Deposit Appropriate Under Bump Metalization (or UBM) stack.

Pattern UBM pads.



Deposit pre-mixed solder paste.



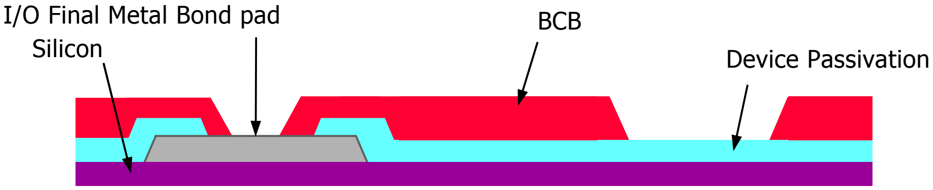
Reflow solder.

3.3 Standard Flip Chip - Redistribution

On some die, the I/O are not located where you need to have the bumps. This is especially true when you take a die originally designed for wire bond packaging applications and need to convert it to be flip chip compatible. The SFC-Redistribution Line (or RDL) process adds "redistribution metallization" (often called "runners' or "traces") that let you re-route the signal path from the die peripheral I/O to an area array of new bump locations, often with significant loosening of effective bump pitches. Although a single RDL layer is most commonly used today, FCI has successfully supported more complex SFC-RDL applications involving up to 3 metal layers. Although FCI's metallization schemes have historically involved subtractive, sputtered metal RDL and UBM options, more recently, FCI has also added semi-additive electroplated Cu based options to its product lineup. Redistribution SFC bumping flows are intended to produce bumps of less than 130μm in height, although the typical bump height is ~100μm. Typical pitch capabilities in this process are 70μm or greater. RDL runners using subtractive sputtered metallization schemes are allowed a minimum of 20um wide lines and 22um wide spaces. For finer pitch, higher aspect ratio RDL requirements, including On Chip Inductor applications, FlipChip also has available semi-additive Cu electroplated metallization schemes which allow a minimum of 8um wide lines and 10um wide spaces if needed. Since the SFC process is not limited to the bi-metal constraints of an electroplated solder process, multi-metal alloys (including Sn/Ag/Cu) are readily available. As with all die processed with small bumps, these die will require the use of underfill during packaging.

3.3.1 BCB SFC-Redistribution Process Summary

The BCB SFC-RDL process requires more process steps than the SFC-Bump on I/O or the SFC-Repassivation flows. Below is an outline of the BCB SFC-Redistribution subtractive, sputtered metallization process sequence with its characteristic Bump on Nitride construction (none of the drawings are to scale):

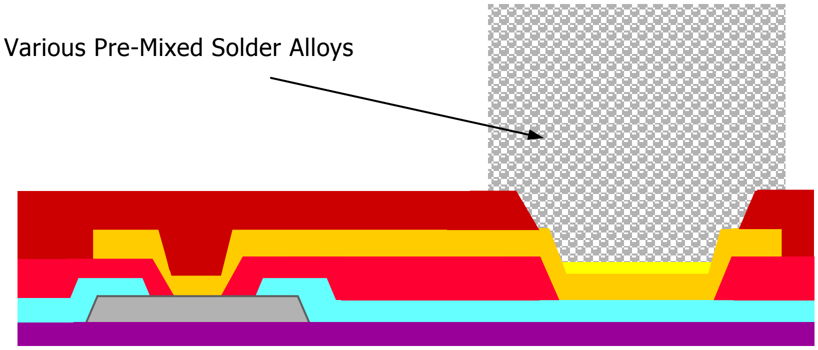


Deposit and pattern first layer of BCB passivation (BCB1).

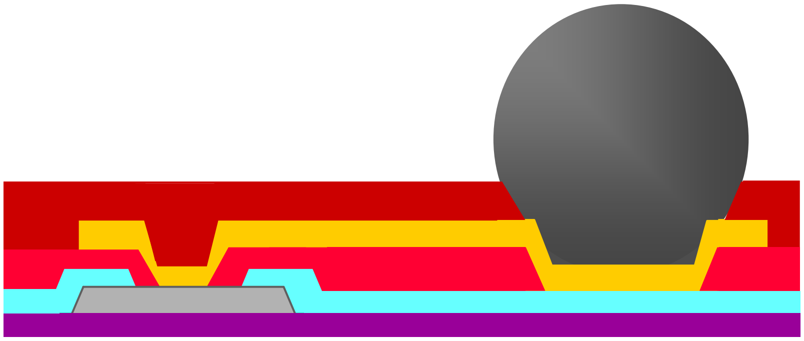
Deposit four layer (Al/NiV/Cu/Ti) RDL / UBM stack.

Photodefine and Etch UBM stack to form redistribution runners and bump pads.

Deposit, pattern, and cross-link second layer of BCB passivation (BCB2).



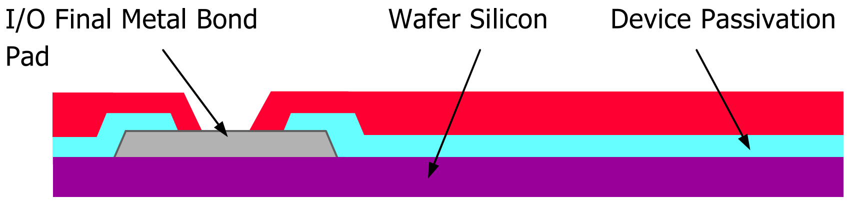
Deposit solder paste (Proprietary Process).



Reflow solder.

3.3.2 Spheron™ SFC-Redistribution Process Summary

The Spheron SFC-RDL process also requires more process steps than the SFC-Bump on I/O or the SFC-Repassivation flows. Below is an outline of the Spheron SFC-Redistribution subtractive, sputtered metallization process sequence with its characteristic Bump on Polymer construction (none of the drawings are to scale):

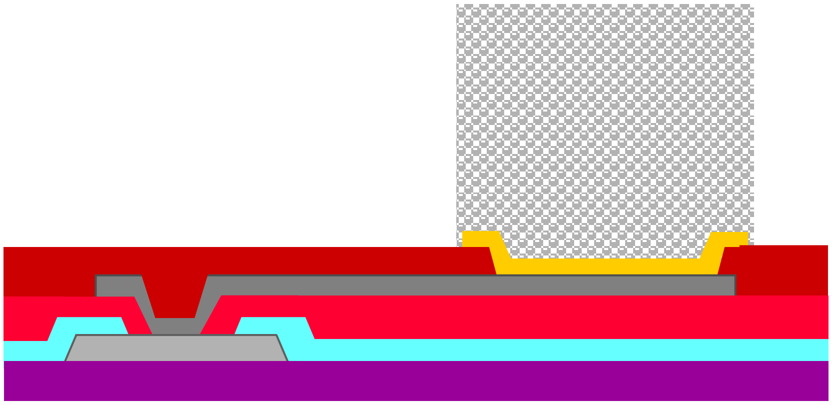


Coat first dielectric layer (Spheron1), expose, develop, and cure.

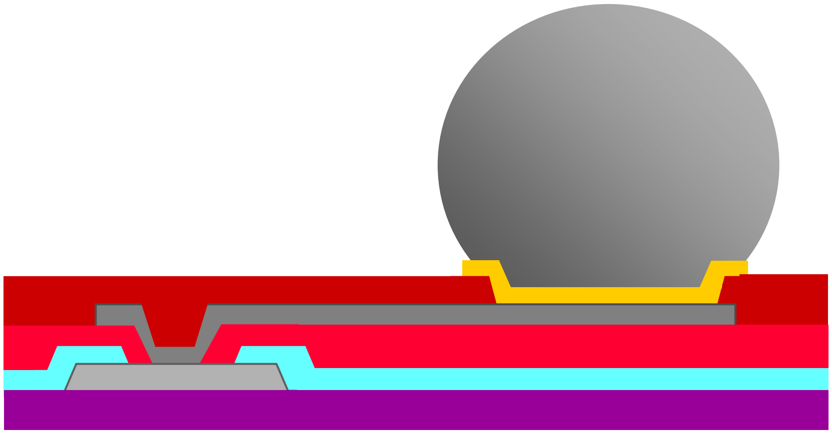
Sputter metal redistribution layer (Ti/Al/Ti). Pattern and etch to form redistribution runners.

Coat second dielectric layer (Spheron2), expose, develop, and cure.

Deposit and pattern three layer sputtered UBM stack (Al/NiV/Cu).



Deposit solder paste (Proprietary Process).



Reflow Solder

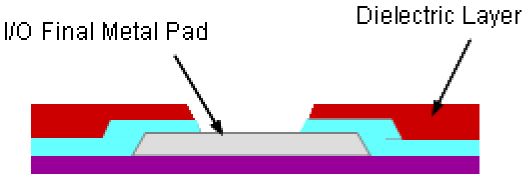
3.4 Cu Pillar & Cu NanoPillar Bump Repassivation

As the industry has continued to drive flip chip applications to bump pitches of 150µm and below, significant assembly challenges related to underfilling flip chip assemblies on laminate substrates has arisen due to associated decreases in chip stand-offs. Cu Pillar Flip Chip bumping has emerged as an attractive option both for high end computing and more recently for wireless flip chip, System in Package (SiP) applications, where the predictable stand-off of a copper post can effectively minimize assembly and underfilling problems. Since FCI is a dominant force in bumping for the wireless electronics space, FCI has developed and qualified a robust Cu Pillar Bump Repassivation technology for use on silicon and GaAs flip chip applications. FCI's Standard Pillar Bump technology targets applications of 100 micron pitch and greater, while the more recent NANOPillar™ Bump alternative supports ultra-fine pitch flip chip applications down to 35 micron pitch. NANOPillar Bumps target flip chip on silicon applications which are becoming increasingly common in an assortment of 3D packaging schemes.

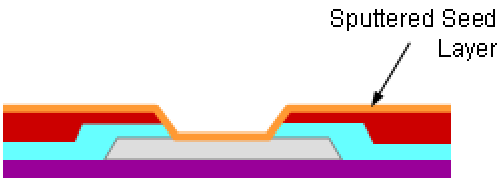
In order to ensure successful deployment of this product offering, FCI opted to take a Cu Pillar Bump license from APS, a well recognized Singaporean technology company. Unlike the rest of the industry however, FCI's Cu Pillar Bump offering involves solder capping of plated Cu posts of definable heights, using a minor variant of its widely accepted, proprietary SFC printed bump process. This flow uses premixed solder paste for formation of the solder cap and as a result is not limited to the bi-metal constraints of an all electroplating Cu Pillar Bump technology. Multi-metal alloys (including a broad assortment of Sn/Ag/Cu alloys) can be selected to match the particular requirements of specific applications. The generous die stand-offs that result from Cu Pillar Bumps enable ease of assembly, particularly at underfill. In the case of Flip Chip SiP applications, the elimination of underfill process steps and dimensional design keep outs enabling vacuum-assisted transfer molding for simultaneous die underfilling and package overmolding is enabled. In this flip chip bumping alternative, a dielectric repassivation layer of either Benzocyclobutene (or BCB) or Spheron can be selected as a localized stress reliever in the bump location on the die before bumping. As with SFC-Bump on I/O and SFC-Repassivation, FCI's Cu Pillar Bump - Repassivation offering is designed for small flip chip bumping applications (less than 130μm in diameter) placed directly on the die I/O. FCI's Cu Pillar Bump can also be readily incorporated with FCI's plated Cu RDL options should it be required.

3.4.1 Cu Pillar Bump - Repassivation Process Summary

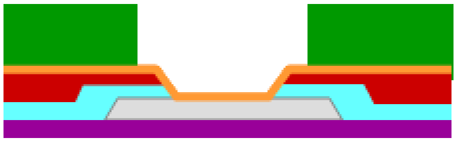
The Cu Pillar Bump - Repassivation process flows were designed to have significant commonality with FCI's other bumping options. Below is an outline of a generic Cu Pillar Bump process flow (none of the drawings are to scale):



Deposit, pattern and cure a layer of BCB or Spheron dielectric.

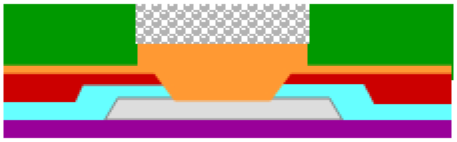


Sputter deposit seed layer.



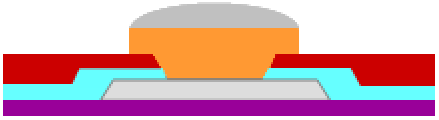
Deposit, expose and develop plating resist.

Electroplate Cu pillar.



Print solder cap.

Reflow solder cap.



Strip resist and etch seed layer.

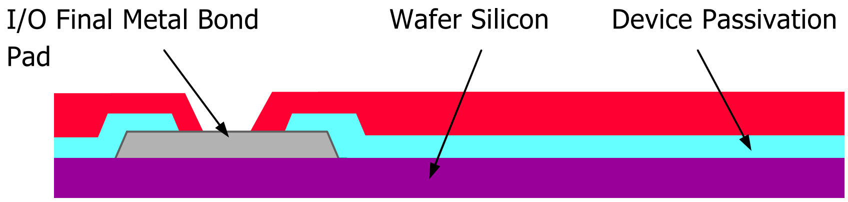
3.5 Spheron™ WLCSP

FlipChip's Flagship Spheron™ WLCSP technology utilizes a proprietary dielectric material, which offers improved electrical performance and reliability over other polymer repassivation options. In addition to its advanced dielectric material, the Spheron WLCSP™ product family incorporates a growing number of subtractive sputtering and semi-additive electroplated Cu based metallization options targeting specific customer needs. For example, some of the Spheron WLCSP product breadth over the past few years has been developed in response to the evolving board level requirements of portable handheld products. Benefits of Spheron WLCSP options include: improved electrical performance, reduced capacitive coupling between UBM/Solder and the underlying IC circuitry, improved solder joint reliability, significant improvement in thermal cycling performance due to die planarization/polymer film characteristics, and elimination of incoming wafer topology issues. In addition, this planarizing polymer film ensures proper UBM step coverage, even over non-planarized devices. Spheron is compatible with silicon nitride and silicon dioxide passivations.

Spheron WLCSPs use pre-formed solder spheres of 200µm to 500µm in diameter to routinely bump device pitches ranging from 0.35 to 0.8 mm pitch and reflowed for final bump heights of 160µm to 400µm. In this process, the bumps can be placed directly on the device I/O's or the bump location may be redistributed to a more desirable die location. For WLCSPs, the number of bumps per die is typically in the range of 4 to 100 with upper array size limitations being based primarily on end-user board level reliability requirements rather than any bumping constraints. Die bumped with Spheron WLCSP typically do not require underfill. Spheron WLCSPs have been demonstrated to be JEDEC Level 1 compliant.

3.5.1 Spheron WLP™ Redistribution – Standard Process Flow

The Spheron WLP process may be used to bump directly on I/O or may be used to redistribute bumps to a more desirable die location. An example of the subtractive sputtered metallization redistributed process options available is shown (none of the drawings are to scale).

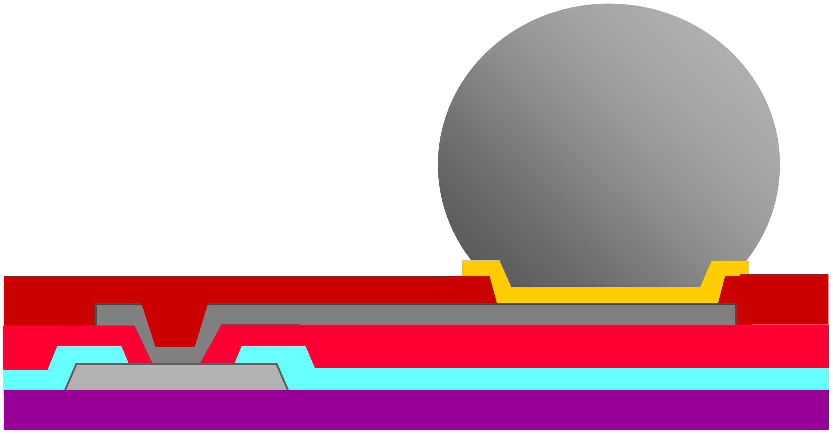


Coat first dielectric layer (Spheron1), expose, develop, and cure.

Sputter metal redistribution layer (Ti/Al/Ti). Pattern and etch to form redistribution runners.

Coat second dielectric layer (Spheron2), expose, develop, and cure.

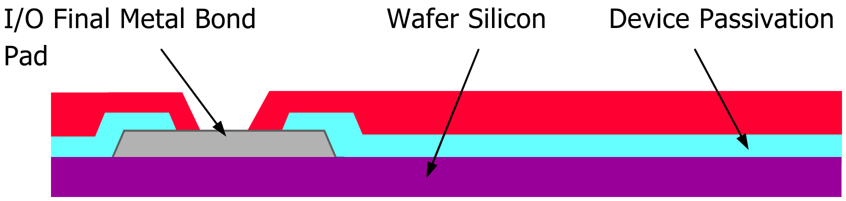
Deposit and pattern three layer sputtered UBM stack (Al/NiV/Cu).



Drop and Reflow Solder Spheres

3.5.2 Spheron WLCSP™ Electroplated Cu Redistribution Process Flow

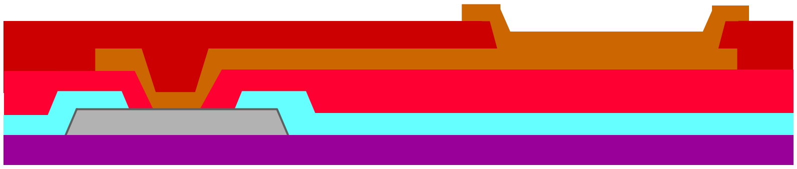
The Spheron WLCSP Electroplated Cu process may be used to bump directly on I/O or may be used to redistribute bumps to a more appropriate die location. A representative flow of FCI’s Semi-Additive Electroplated Cu RDL process is outlined below (none of the drawings are to scale).



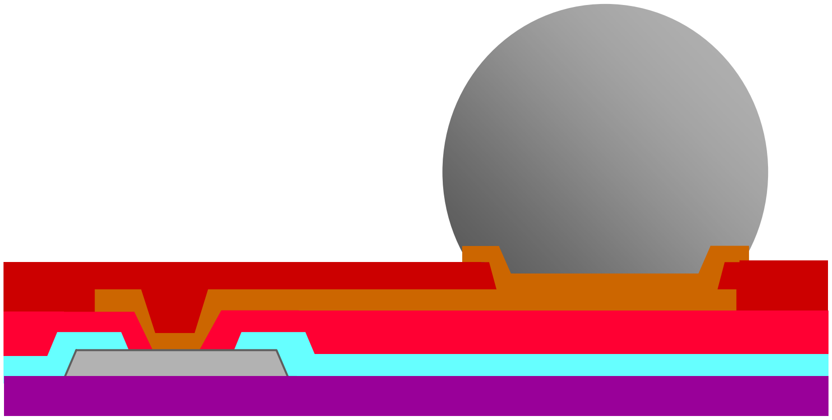
Coat first dielectric layer (Spheron1), expose, develop, and cure.

Sputter deposit plating seed layer. Pattern electroplate Cu RDL layer. Strip resist / etch seed layer.

Coat second dielectric layer (Spheron2), expose, develop, and cure.



Deposit plating seed layer. Pattern plate UBM layer. Strip resist and etch seed layer.



Sphere placement and reflow.

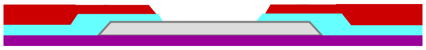
3.6 UltraCSP®

*Ultra*CSP® is our patented Wafer Level Chip Scale Package (or WLCSP) process. Since its introduction in 1998, *Ultra*CSP has become the industry's standard for WLCSP. Bump heights for the process range from 160µm to 400µm depending on pitch. In this process, pre-formed solder spheres of 200µm to 500µm in diameter are placed on the wafer and reflowed. The bumps can be placed directly on the device I/O's or the signal may be redistributed to a more desirable die location. Typically, the number of bumps per die is 4 to 100. Die bumped with *Ultra*CSP do not require underfill until the bump array reaches the 6x6 to 7x7 size. For larger bump arrays underfill may be needed depending on the reliability requirements of the particular application. The lack of underfill makes it easy to migrate TSOP or QFP to *Ultra*CSP. *Ultra* CSP is classified as a JEDEC Level 1 compliant packaging option.

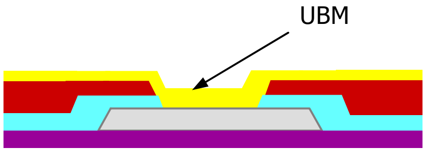
3.6.1 *Ultra*CSP® Process Summary

The *UltraCSP* process may be used to bump directly on I/O or may be used to redistribute bumps to a more desirable die location. Both processes are summarized below (none of the drawings are to scale).

3.6.2 *Ultra*CSP® Bump on I/O - Process Flow

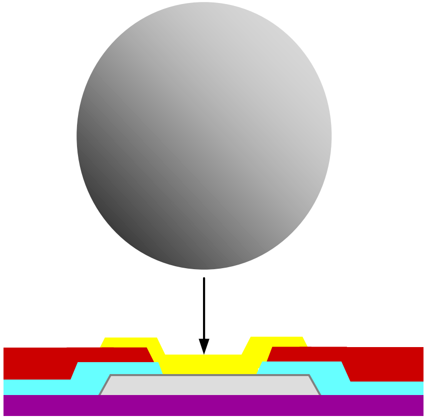


Deposit and pattern a layer of BCB passivation.

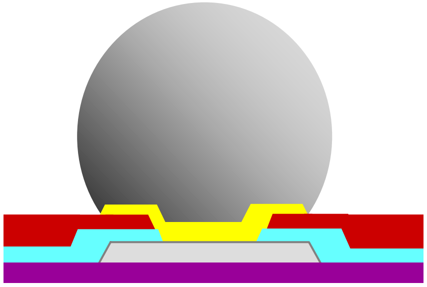


Deposit three layer (Al/NiV/Cu) Under Bump Metalization (UBM) stack.

Pattern UBM pads

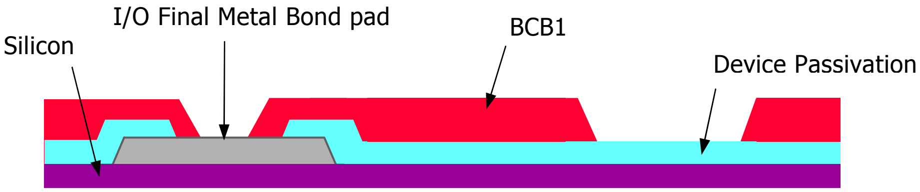


Attach pre-formed solder spheres.



Reflow solder.

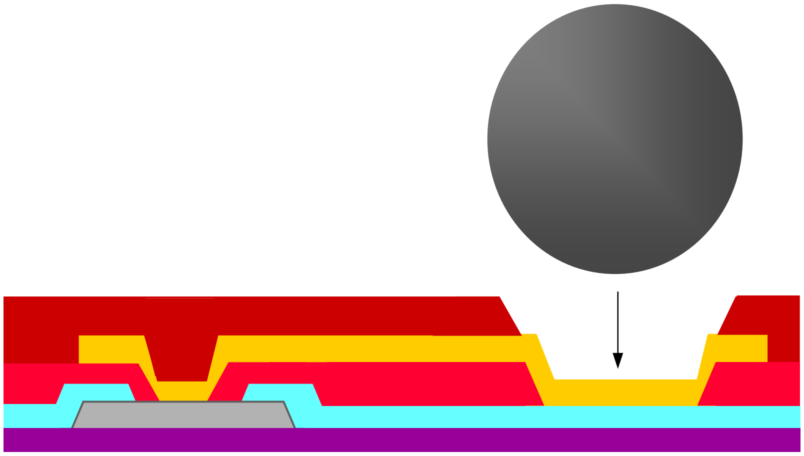
3.6.3 *Ultra*CSP® Redistributed - Process Flow



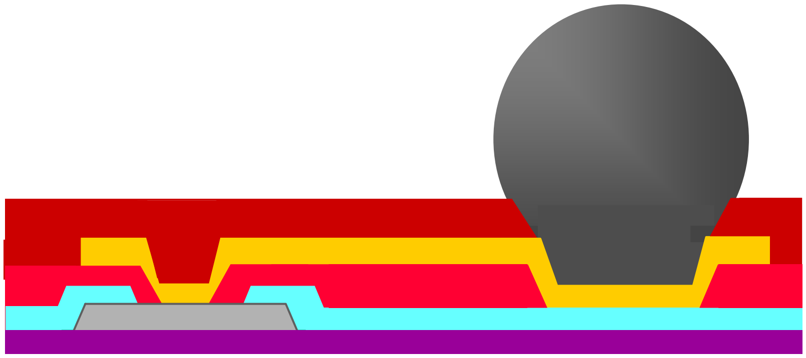
Deposit and pattern first layer of BCB passivation (BCB1).

Sputter deposit three layer (Al/NiV/Cu) RDL / UBM stack and pattern.

Deposit, pattern, and cross-link second layer of BCB passivation (BCB2).



Attach Pre-formed solder spheres.



Reflow solder.

3.7 EliteUBM™, EliteFC™, and EliteCSP™ – Electroless Ni/Au

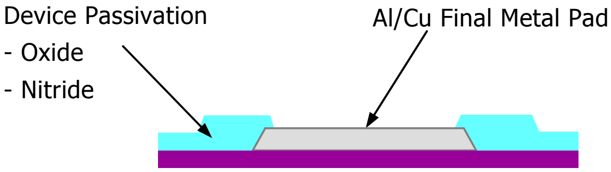
In 2005, FlipChip acquired a license from the Fraunhofer/IZM Institute of Berlin to offer Electroless Ni/Au (E-less Ni/Au) bumping alternatives. E-less Ni/Au is available in three configurations: EliteUBM, EliteFC, and EliteCSP. EliteUBM is simply a Ni/Au pad ranging in thickness from 5µm to 30µm. Typical applications for EliteUBM are low cost RFID tags. *Elite* packages and FlipChip package extensions are JEDEC Level 1 compliant.

EliteFC is a Flip Chip smaller sized bumping technology that uses the low cost E-less Ni/Au UBM. Typical bump heights are 70µm - 130µm depending on bump pitch and configuration. EliteFC can often be used as a lower cost alternative to traditional Standard Flip Chip.

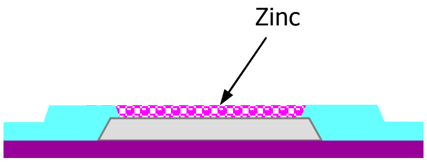
EliteCSP is a Wafer Level-Chip Scale Package (WL-CSP) that uses the E-less UBM structure. As with *Ultra*CSP, pre-formed solder spheres of 200µm to 500µm are placed on the wafer and reflowed for final bump heights of 160µm to 400µm. Typical applications for EliteCSP include very cost sensitive as well as high power / high temperature devices.

Devices that are to be bumped using any of the Elite processes need to have some special requirements met. These requirements are described in Section 4.3.12.

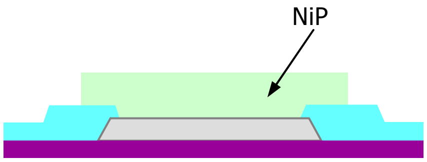
3.7.1 *Elite*UBM™ – Process Flow



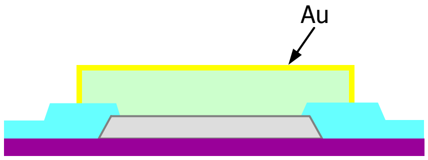
Clean Aluminum/Cu Final Metal Pad.



Apply a thin layer of Zinc to the AlCu Pad.

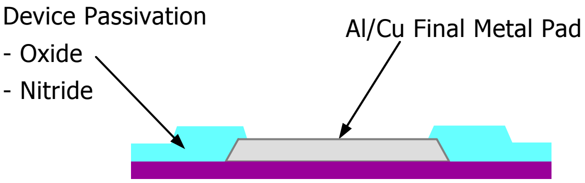


Substitute NiP for the Zinc.

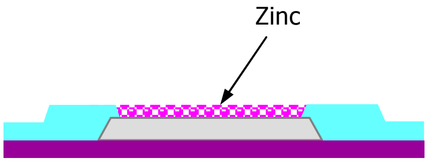


Coat UBM with a thin layer of Au (oxidation protection).

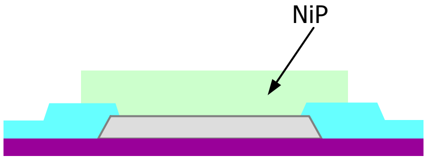
3.7.2 *Elite*FC™ – Process Flow



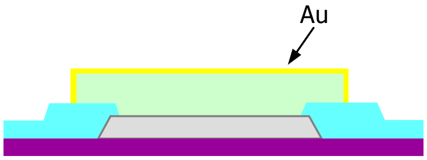
Clean Aluminum/Cu Final Metal Pads.



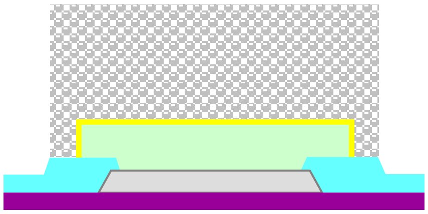
Zincation of AlCu Pads.



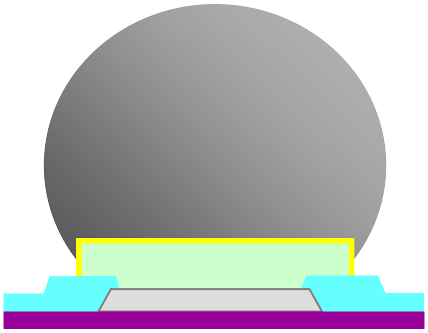
Ni-P Zn displacement.



Coat UBM with a thin layer of Au (oxidation protection).

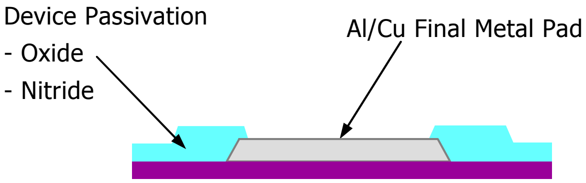


Deposit pre-mixed solder paste.

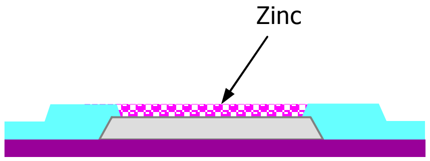


Reflow Solder

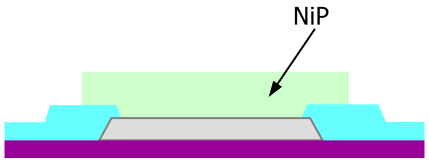
3.7.3 *Elite*CSP™ – Process Flow



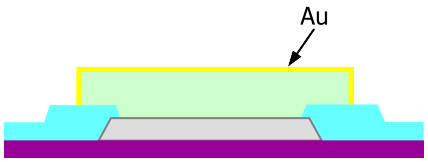
Clean Aluminum/Cu final metal pads.



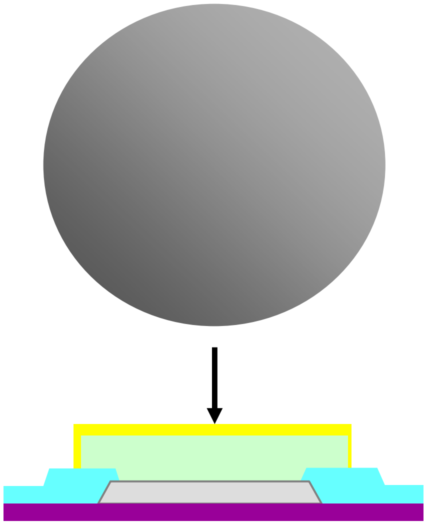
Zincation of AlCu pads.



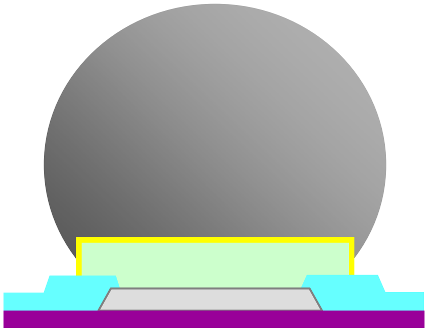
Substitute NiP for the Zinc on pads.



Coat UBM with a thin layer of Gold (oxidation protection).



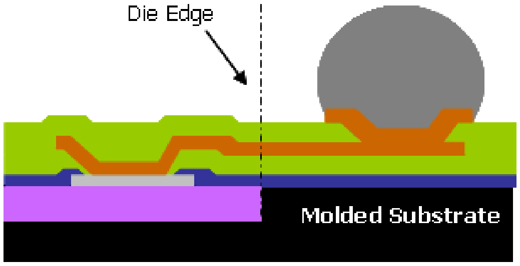
Attach pre-formed solder spheres.



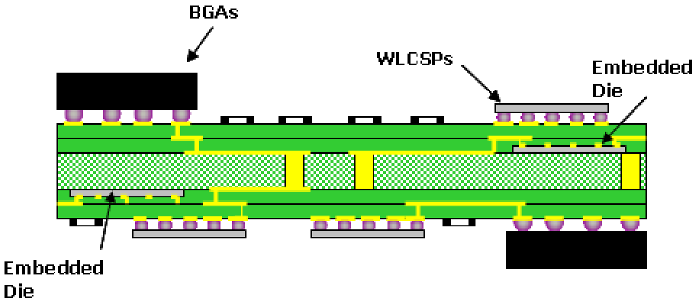
Reflow Solder

3.8 Embeddable Die Customization Technology (EDC™)

Fan-out Chip Scale Packaging technologies are being promoted as a key element of next generation 3D semiconductor packaging schemes. Freescale's Redistribution Chip Package (RCP) and Infineon's Embedded Wafer Level BGA (EWLB) are two examples that have recently been receiving significant industry attention. Additionally, embedding integrated circuits and passive components into printed circuit boards (PCB) for cellular, consumer and other form factor sensitive portable electronics applications is also emerging. In the case of the PCB approach, viable approaches by Imbera and Europe's Hiding Dies consortia have also emerged.



Fan-Out WLCSP RDL structure.



Embedded die in a Build Up PWB.

One of the critical infrastructural requirements for the proliferation of these emerging 3D technologies is the availability of a robust, standardized wafer level die modification technology needed to prepare devices for embedding. FCI's assortment of Pad on I/O - EDC and multilayer RDL-EDC technologies were originally developed by FCI to support flip chip and WLCSP applications but have been modified to address the specific requirements of embedded die technologies. Embeddable Die Customization (EDC^{TM}) is the product name for this recent addition to FCI's broadening portfolio of wafer level technologies. EDC^{TM} allows the conversion of integrated circuits into embeddable ready components. Wafer thinning and stress relief processing to enable die thicknesses of 100 microns and below is also a key requirement of the EDC^{TM} technology.

Cross-section of a typical 2 metal layer RDL-EDC structure.

A broadening range of embedded die applications are currently being supported by FCI's EDC offering. Through its network of established embedded die technology partners, FCI can facilitate your transition into 3D packaging.

4 Choosing Bumping Options

4.1 Available Solder Alloys

FlipChip offers several different solder alloys to match your application's needs. By using pre-mixed solder paste and pre-formed solder spheres, alloy composition is very tightly controlled. This means that your solder bumps have predictable and reliable reflow characteristics.

4.1.1 Basic Physical Properties of Solder Paste Alloys

The SFC-Ball on I/O, SFC-Repassivation, and SFC-Redistribution processes use pre-mixed solder paste to form the final solder bumps. Table 1 summarizes the basic properties of our most common paste alloys.

Table 1: Physical Proprieties of Paste Alloys

Alloy / Property	Sn/Ag/Cu Lead Free (SAC 351)	63Sn37Pb Standard Eutectic / ULA Eutectic
Alloy Composition	Sn 95.5% Ag 3.5% Cu 1.0%	Sn 63% Pb 37%
Melting Point	217°C	183°C
Peak Reflow Temperature	265°C	223°C
Alpha Emissions (counts/cm^2/hr)	<0.01	Not Tested for Standard Eutectic / <0.002 for ULA Eutectic

4.1.2 Basic Physical Properties of Pre-Formed Solder Sphere Alloys

The *Ultra*CSP and Spheron WLCSP processes use pre-formed solder spheres. The standard solder sphere sizes are 0.20mm (200μm), 0.25mm (250μm), 0.3mm (300μm), 0.35mm (350μm), 0.4mm (400μm), and 0.5mm (500μm). The basic physical properties of the pre-formed solder spheres are listed on the table below.

Table 2: Physical Properties of Pre-Formed Solder Ball Alloys

Alloy / Property	Sn/Ag/Cu Lead Free (SAC 266)	Enhanced Lead Free Sn/Ag/Cu (SAC 105)	Eutectic 63Sn37Pb
Alloy Composition	Sn 96.8% Ag 2.6% Cu 0.6%	Sn 98.5% Ag 1.0% Cu 0.5% Dopant	Sn 63% Pb 37%
Melting Point	220°C	218°C	183°C
Peak Reflow Temperature	250°C	250°C	221°C
Alpha Emissions (counts/cm^2/hr)	<0.01	<0.01	Not Tested

4.2 Backside Laser Mark

For die identification and traceability, FlipChip gives the option of using a laser to mark the backside of each die. FlipChip can mark any alphanumeric character down to a minimum character size of 0.25 mm square with a character depth of approximately 4 - 6μm. Simple graphics including circles, squares, triangles, etc. can be used for the optional pin 1 indicator. We can even mark simplified graphics consisting of basic shapes including circles, squares, triangles, etc. for company logos. FlipChip has the capability to mark accurately any die to a minimum die dimension of 0.8 mm. If you need custom designs, give FlipChip a call. We can custom match a laser program to your needs.

4.3 "In Process" Backgrind

Many times wafers need to be thinned to meet final packaging requirements. For *Ultra*CSP, Spheron WLCSP, and EliteCSP, FlipChip has the ability to backgrind wafers, during processing, just before the solder balls are applied. Wafers are coarse ground with a 360 grit wheel and polished ground with a 2000 grit wheel. Below are our high volume backgrinding / processing capabilities. (For thickness requirements on incoming wafers, please see section 5.2.7 "Incoming Wafer Thickness.") Please contact FlipChip if you have thinner backgrinding requirements.

Table 3: Wafer Thickness After "In Process WL-CSP" Backgrinding

Wafer Size	6 inch (150mm)	8 inch (200mm)
Minimum Wafer Thickness After Backgrind for Bump Heights above 160um	12 mil (305μm)	14 mil (350μm)

4.4 “Post Process” Backgrind

For Standard Flip Chip (SFC), Repassivated Standard Flip Chip (RP-SFC) and Redistributed Standard Flip Chip (RDL-SFC), FlipChip has the ability to backgrind wafers after the bumping process is completed. Wafers are coarse ground with a wheel of 360 grit and polished ground with a wheel of 2000 grit. Below are our standard backgrinding / processing capabilities. Please contact FlipChip if you have thinner backgrinding requirements.

Table 4: Wafer Thickness After “Post Process SFC” Backgrinding

Wafer Size	6 inch (150mm)	8 inch (200mm)
Minimum Wafer Thickness After Backgrind for Bump Heights below 130um	6 mil (152µm)	8 mil (203µm)

4.5 Backside Laminate Coating

FCI offers the option of having a 40um thick non-transparent laminate film added to the backside of the processed wafer. This film has been shown to increase die strength, reduce chip-outs during saw, and also make the die look more like a BGA package. Contact FlipChip for details.

4.6 Electronic Wafer Map Yield Reporting

Wafer yield mapping data is either presented on paper (shipped with the wafers) or by electronic wafer maps (transmitted over secure FTP sites) depending on customer preference. FlipChip uses Simplified INF (SINF), the industry standard file format, for all electronic wafer maps. FTP sites can be easily and quickly set up for secure data transfer. Contact FlipChip for details.

4.7 Post Bump Electrical Testing

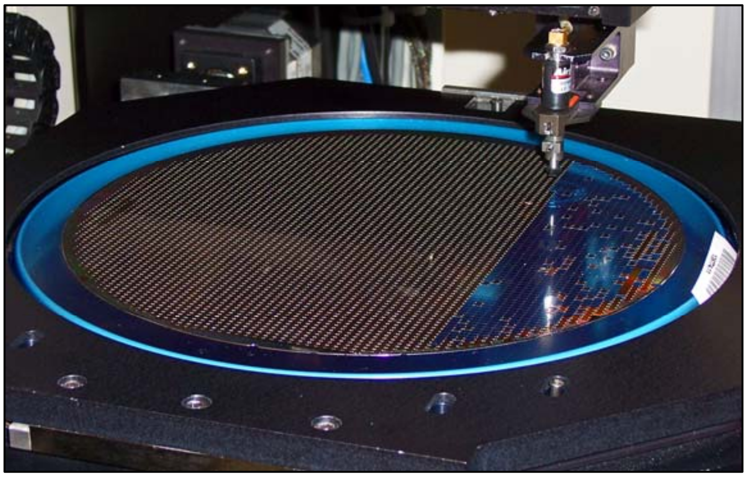
After bumping, FlipChip can have the un-sawn die electrically tested on a variety of test platforms including:

- Advantest
- Agilent / HP
- Credence
- Eagle
- Credence
- Nextest
- LTX
- Teradyne

Contact FlipChip for a complete description of electrical testing capabilities and availability.

4.8 Dicing and Packaging

FlipChip also has the capability to have your finished wafers diced to your specifications. After dicing, visual inspection either by sampling or 100% will be performed. The die will then be packaged in tape-and-reel or waffle pack configurations. For complete dicing and packaging descriptions and capabilities, contact FlipChip.



5 Design Guidelines

5.1 Overview

FlipChip has developed a set of design rules and guidelines to ensure that your wafers will be processed successfully. These rules allow for FlipChip to use standardized process flows using industry standard process equipment The rules presented below represent a generalization of the actual FlipChip Design Specifications, which are subject to revisions and may not apply to all devices. If you have wafers that do not meet these guidelines or if you have any questions, give FlipChip a call. Since we are a development driven engineering organization, we can often create a custom solution for even the most unusual bumping application. FCI is committed to work with you to ensure your total satisfaction.

5.2 Incoming Wafer Requirements

5.2.1 Types of Wafers

FlipChip can process Silicon (all types) and Silicon/Germanium wafers. Contact FlipChip if you have other types of substrates (including Quartz, Sapphire, and GaAs). We will provide feedback on our capabilities.

5.2.2 SEMI Material Requirements

All wafers must meet current SEMI material requirements. These specifications cover major areas including: wafer diameter (dimension and tolerance), polish, edge profile, notches, and major and minor flat sizes, locations, and orientations. It is highly recommended that 8-inch (200 mm) wafers have a notch rather than a flat.

5.2.3 Wafer Scribe Requirements

It is highly recommended that each wafer have a unique scribe number. Typically, the device lot number and the wafer number (within the lot) are scribed on each wafer.

5.2.4 Wafer Backside Requirements

For proper processing, the backside must be smooth, without ridges, bumps, or protrusions. The backsides of incoming wafers ideally should be exposed Silicon or Silicon/Germanium. Some types of backside coatings are acceptable. Contact FlipChip if your wafers are backside coated so that we can determine processing feasibility.

5.2.5 Acceptable Wafer Size

FlipChip-Phoenix accepts wafers of the following sizes: 6 inch (150mm), and 8 inch (200mm). FCI also offers 12” (300 mm) wafer bumping and WLCSP options through SMIC, one of our Asian wafer level manufacturing partners. If you have other wafer size needs, please contact FlipChip.

5.2.6 Wafer Edge Exclusion Requirements

FlipChip uses a standard 3mm edge exclusion for all designs. Edge exclusions less than 3mm can be used under certain circumstances depending on the process flow selected. Please contact FlipChip for more information.

5.2.7 Incoming Wafer Thickness

It is always preferable for FCI to receive “Full Thickness” wafers. If your wafers need to be thinned prior to shipment to FCI, the following table gives the minimum incoming thickness requirements. Wafers thinned before processing must have at least a 2000 grit final polish. It is preferred that the wafers are also “stress relieved”. If you need wafers that are thinner, consider the option of backgrinding the wafers during processing at FlipChip (see sections 4.3 and 4.4).

Table 5. Incoming Wafer Thickness Requirements

Process	6 inch (150 mm)	8 inch (200 mm)
All Product Offerings	22 mil (560um)	26 mil (660um)

5.3 Device Requirements

5.3.1 Die Size

For all processes at FlipChip, there are no limits on die size. For practical reasons, the bump size, the number of bumps, and the required pitch for each bump determine minimum die size. There is no maximum die size.

5.3.2 Number of Sites Bumped Per Die

For all processes at FlipChip, bump pitch is the limiter to the number of bumps per die. For practical reasons, the bump size, the die size, the required pitch for each bump, and the reliability requirements of the device determine the maximum number of bumps per die. There are no requirements for the minimum number of bumps per die.

5.3.3 Die Layout

The devices on the wafer may be stepped to the very edge of the wafer. FlipChip will bump the wafer to a standard edge exclusion of 3.0mm, unless otherwise specified.

5.3.4 Unique Die on Wafer

For initial engineering evaluations, there may be more than one die design per wafer. The only restrictions are that the same process flow (SFC, Repassivation, or Redistribution) and the same solder alloy be used across the entire wafer. For engineering wafers with more than one die design, Automated Optical Inspection (AOI) cannot be performed while laser marking requirements must be reviewed. For production wafers, only one die design is allowed per wafer.

5.3.5 Types of Passivation

For all processes, allowable passivations are nitride, oxide, and oxy-nitride. Please contact FlipChip is your wafers have a different passivation such as polyimide.

5.3.6 Types of Final Metal

For all processes, acceptable types of final metal pads are Aluminum, Aluminum alloys (typically Al/Cu or Al/Cu/Si), Copper with an Aluminum cap, and Copper. If your final metal is Gold, Titanium, or Titanium/Tungsten, contact FlipChip. We will review your requirements and provide a workable solution.

5.3.7 Ink Dots

Incoming wafers with ink dots are not acceptable. Wafers that have been previously ink dotted, then cleaned, can be bumped under certain circumstances. If you have wafers that have been ink dotted, contact FlipChip.

5.3.8 Fuse Links

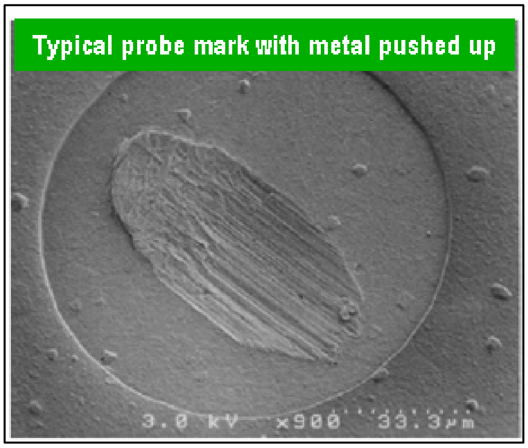
FlipChip can bump devices that contain fuse links provided that the process flow selected uses an added passivation layer (BCB or Spheron). It is important that the UBM layer does not make direct contact with fuse links. The added passivation will be used to insulate the UBM from the fuse pad. The location of fusible links must be supplied to FlipChip as part of design data package.

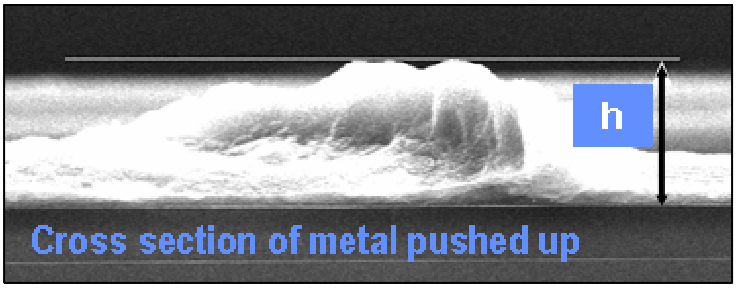
5.3.9 Nitride Passivation Openings Not Bumped

For flows using BCB or Spheron, arrayed I/O pads that are not bumped will be covered with the added passivation. Peripheral I/O pads that are not routed will also be covered with added passivation.

5.3.10 Probing

All FlipChip processes readily accommodate probed wafers and bumping directly over probe marks. Impact of most probe damage on I/O pads has been proven to be negligible, due to the deposition of Aluminum or Titanium as first layer of the three layer metal UBM stack. As a rule of thumb, FCI allows a certain amount of probe tip "over-travel" after touchdown. FlipChip can accept probe damage up to a maximum of 1/3 of the diameter of the I/O pad. FCI will accept single or double probe marks. For redistribution designs (only), the height (h) of the "pushed-up" metal of the probe mark can be a maximum of 3μm. If the pushed up metal is higher than 3μm, it can interfere with FCI routing rules. *Elite*UBM, *Elite*FC, and *Elite*CSP have additional rules on probe marks. These rules are described in section 5.3.12. FlipChip's bumps can also be probed after bump. Please consult with FCI Sales if severe probe damage is inherent to your wafer processing.





5.3.11 Street Width

The street width is defined by the die passivation edge to opposite passivation edge. Since dicing capability is variable, depending on the equipment used to dice the wafer, it is important to ensure that the saw methodology does not damage the BCB or Spheron edge during the saw operation. BCB and Spheron separation across a dicing street is typically greater than 80 microns.

5.3.12 Special *Elite*UBM, *Elite*FC, and *Elite*CSP Device Requirements

There are several special requirements for devices that are to be bumped using the *Elite* E-less Ni/Au process. The following is a partial list of the major requirements. For the complete list, please contact FlipChip.

Preferably, the devices Final Metal pad should be Cu doped Aluminum (Cu≥0.5%). In most circumstances pure Aluminum, Al/Si pad metallizations can also be accommodated.

The top Aluminum layer of the Final Metal Pad must have a thickness of 1um or greater.

The diameter of the device passivation opening should be approximately 8μm smaller than the desired UBM diameter (for the typical Ni/Au thickness of ~5μm).

There can be no exposed probe pads, fuse links, die apron rings, test pads, passivation pinholes or any other exposed metal on the device or in the streets (other than the Final Metal I/O pads) -- these exposed areas will plate with the Ni/Au.

Localized masking options with dielectric and photoresist layers are possible but add processing complexity and cost.

Probe marks must be shallow and must not have dug into underlying layers through the Final Metal pad.

5.3.13 Passivation Opening Sidewalls

Die I/O passivation opening sidewalls should have a slope of 70° or less with the sidewalls not "under-cut" into the passivation. Sidewalls greater than 70° are not recommended due to the possibility of discontinuity in sputtered metal films over such via profiles (see Figure 2C). If the passivation opening sidewalls are greater than 70°, FCI design rules strongly recommend the use of a polymer dielectric layer with termination of the via within the passivation opening prior to sputter deposition of the UBM or RDL metal layer. If you have a device with a passivation opening sidewall slopes greater than 70°, contact FlipChip for further review.

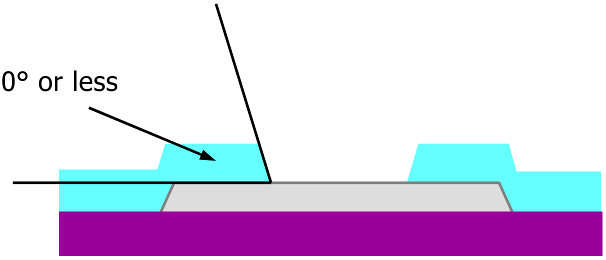


Figure 2A. Passivation Sidewall Requirements

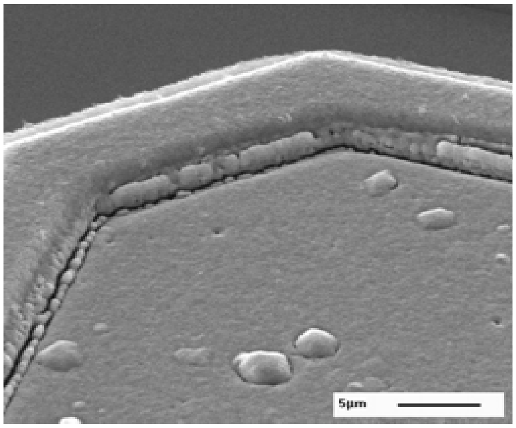


Figure 2B. Poor Sidewall Step Coverage

5.4 Alignment Feature Requirements

Having proper alignment targets present on a wafer is critical to ensure proper bump tooling alignment and processing repeatability. FlipChip prefers to reference alignment features that are only repeated once per reticle step. An example of such a feature would be a Clearfield Cross alignment feature (see figure below) or an equivalent sized feature located with the street or frame data of each reticle step. Alignment features located and repeated within each die are not preferred for bump alignment as this could lead to row / column mis-alignment.

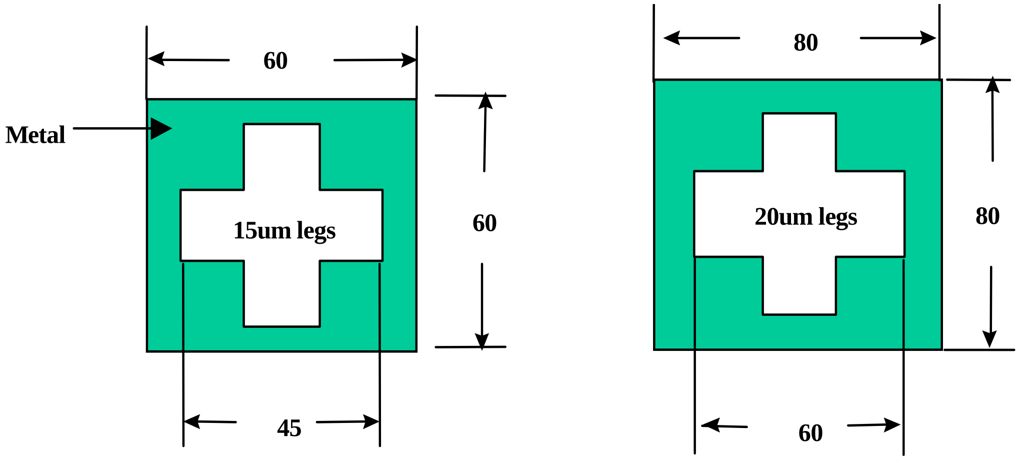


Figure 3. Clearfield Cross Alignment Features

5.5 What Information Does FlipChip Need For New Mask Designs?

FlipChip performs all CAD work using industry standard GDSII software. Data sent to FlipChip for a new design should include at least the device top metal layer and the passivation layer in GDSII format. This data should not be fractured and there should be minimal hierarchy (no more than 10 cells). FlipChip has the capability to receive other formats; however, file format conversions can sometimes be very time consuming. If you have formats other than GDSII, call FlipChip. In addition to the GDSII file, some other basic information will be needed to begin your design. This basic information includes:

- An accurately completed Mask Design Information Form/Statement of Work (MDIF/SOW): The MDIF/SOW asks for a description of the wafer, the die, and how you would like to bump it. A current copy of the MDIF/SOW can be found in the Design Guide section of our web site at:

  http://www.flipchip.com/get_started/
- A Wafer Shot Map showing the array layout / stepping pattern and die orientation relative to the flat or notch location.
- For redistribution designs: A diagram showing the routing requirements between the peripheral bond pads and the array bumps.
- If the product is to be Laser Marked, a completed Laser Marking Specification form.
- A non-disclosure confidentially agreement (for first time customers only).
- A Purchase Order

6 Design Rules and Considerations

6.1 Pitch, UBM Size, and Bump Height Relationships

The maximum allowable size of the UBM is directly related to I/O pitch. The bump height is strongly influenced by both I/O pitch and UBM size. The larger the pitch, the larger the UBM can be, which leads to a larger bump height. Usually, you will want the largest bump height that your pad pitch will allow.

The tables below show typical relationships between pad pitch, UBM size and bump heights. Call FlipChip about your wafers, we will give the exact relationships for your device.

Table 6. Typical Peripheral / Array Pad Pitch, UBM Size and Bump Height Relationships for SFC-Ball on I/O, SFC-Repassivation, SFC-Redistribution, and EliteFC.

Array Pad Pitch (μm)	Typical UBM Diameter (μm)	Typical Bump Height (μm)	Typical Bump Diameter (μm)
70 (2.8 mil)	Customer Specific	Customer Specific	Customer Specific
100 (4 mil)	50	45	57
152 (6 mil)	74	70	89
177 (7 mil)	80	78	99
204 (8 mil)	85	90	114
227 (9 mil)	90	100	127
254 (10 mil)	102	105	133
343 (12 mil)	152	130	165

Table 7: Typical Pad Pitch, Sphere Size, UBM Size and Bump Height Relationships for UltraCSP, Spheron WLCSP, and EliteCSP.

Standard Pad Pitch (μm)	Sphere Size (μm)	Nominal UBM Diameter (Solder Wetable) (μm)	Nominal Bump Height (μm)
350	200	180	160
400	250	235	200
500	300	280	240
650	350	325	300
800	500	450	400

6.2 Packaging Relationships

6.2.1 SFC, Repassivation, and Redistribution Package Stand-Off Height

Package standoff height is the final distance between the die and the board after the die is reflowed.

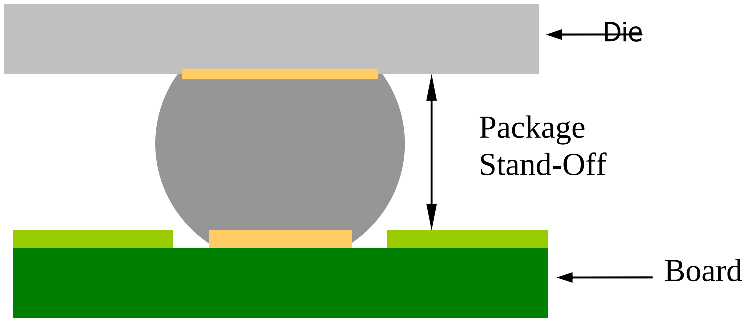


Figure 4. As Assembled Device

For the SFC, Repassivation, Redistribution, and EliteFC processes, package standoff is typically 70% of the bump height. For example, a device with a bump height of 100µm will have a package stand-off height of approximately 70µm.

6.2.2 *UltraCSP*, Spheron WLP, and EliteCSP Package Dimensions

As shown in Figure 5, the critical package dimensions of FlipChip Wafer Level Packages (*UltraCSP*, Spheron, and EliteCSP) include pitch (A), bump height (B), bump diameter (D), die thickness (C), and overall package thickness (B+C).

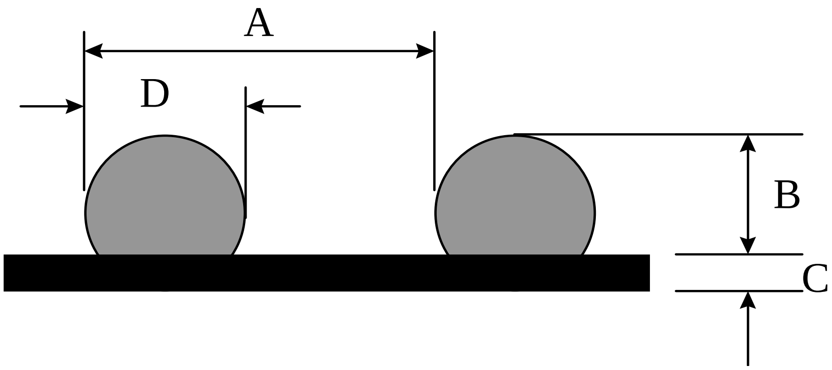


Figure 5. UltraCSP, Spheron WLP, and EliteCSP Package Dimensions

The critical geometric dimensions of FlipChip's WLP's are pitch-dependent. See Table 8 for the dimensional measurements on each package.

Table 8: Typical UltraCSP, Spheron WLP, and EliteCSP Pre-Assembly Package Attributes.

PITCH (mm) (A)	SPHERE SIZE (mm)	PRE-ASSEMBLY DIMENSIONS		DIE THICKNESS * (C)		PACKAGE THICKNESS (mm) (B+C)
		Ball Diameter (mm) (D)	Ball Height (mm) (B)	6″ WAFER (mm)	8″ WAFER (mm)	
0.35	0.20	0.22	0.16	0.30-0.68	0.36-0.73	0.46-0.89
0.4	0.25	0.26	0.20	0.30-0.68	0.36-0.73	0.50-0.93
0.5	0.30	0.33	0.24	0.30-0.68	0.36-0.73	0.54-0.97
0.65	0.35	0.37	0.30	0.30-0.68	0.36-0.73	0.60-1.03
0.8	0.5	0.54	0.40	0.30-0.68	0.36-0.73	0.70-1.13

Note: Lower end of thickness value is after wafer thinning prior to sphere placement.

6.2.3 WLCSP Package Stand-Off Heights

FlipChip recommends assemblers of the *Ultra*CSP, Spheron WLCSP, and EliteCSP technology attempt to target the following stand-off heights and solder volumes during the assembly process, in order to ensure the reliability performance that has been optimized by FlipChip. Critical parameters for stand-off height are indicated in Table 9.

Table 9: UltraCSP, Spheron WLP, and EliteCSP Critical Dimensions: Solder Volume and Stand-Off Height (For Devices with Polymer Defined Wetable Areas)

PITCH:	0.35 mm	0.4 mm	0.5 mm	0.65 mm	0.80 mm
Final Polymer Opening (Wettable Area, μm)	180	235	280	325	450
Nominal Sphere Diameter (μm)	200±10	250±10	300±10	350±20	500±20
UBM Diameter (μm)	225	280	325	350	500
Nominal Ball Height (μm)	160±15	200±15	240±15	300±15	400±15
Nominal Ball Diameter (μm)	220±15	260±15	330±15	380±15	520±15
Nominal Solder Volume of Ball, μm^3 or (mil^3)	3.72×10^6 (375)	8.18×10^6 (500)	1.41×10^7 (860)	2.24×10^7 (1370)	2.24×10^7 (1370)
Nominal Solder Volume of Paste, μm^3 or (mil^3)	2.93×10^6 (137)	3.67×10^6 (226)	6.33×10^6 (390)	9.49×10^6 (580)	9.49×10^6 (580)
Nominal Total Solder Volume, μm^3 or (mil^3)	0.85×10^7 (439)	1.19×10^7 (776)	2.05×10^7 (1250)	1.41×10^7 (1950)	1.41×10^7 (1950)
Recommended PCB Cu Pad (μm)*	180	235	280	325	450

*The wettable area diameter of die side should match the wettable area of the board side (1:1).

6.2.4 Printed-Circuit Board Layout

Two types of land patterns are used for surface-mount packages:

Solder Mask Defined (SMD): Pads have solder-mask openings smaller than the copper pads.

Non-Solder Mask Defined (NSMD): Copper pads are smaller than the solder mask openings.

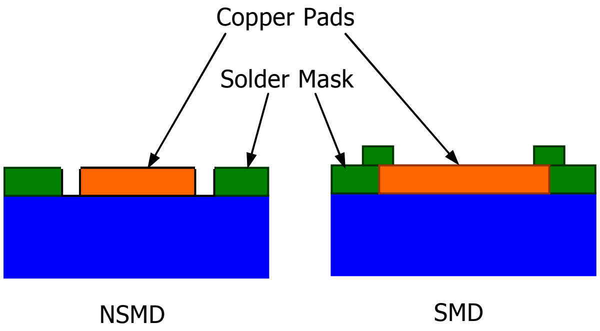


Figure 6. NSMD and SMD Land Pattern

The NSMD configuration is preferred due to its tighter control on copper etch process, as compared to the solder-mask etch process in the SMD pad definition. In addition, the NSMD configuration reduces stress concentration near the solder-mask overlap region, which can result in solder joints cracking. The smaller pad size in the NSMD definition also provides for more room for tight pitch routing on the PCB.

To achieve higher standoff, the copper layer thickness should be 30μm or less. A copper layer greater than 30 μm will result in lowering of the effective stand-off. Lower stand-off may compromise solder joint reliability. Copper pads should be finished with Organic Solderability Preservative coating (OSP). For electroplated nickel-immersion gold-finish pads, the gold thickness must be less than 0.5 micron to avoid making the solder joints brittle.

6.2.5 WLCSP Stencil and Board Design Parameters

FlipChip has achieved target ball standoff height and solder volume by use of the stencil and board-level design parameters as indicated above. The table below gives examples of typical stencil design and construction parameters used to obtain the required standoff height and solder volume.

Table 10: Table of Sample Standoff Calculations

	PARAMETER	300µm SPHERE	350µm SPHERE	500µm SPHERE
PRINTED SOLDER PASTE on BOARD	Metal Loading (%)	50	50	50
	Aperture Shape	Square	Square	Round
	Aperture Size (µm)	375	375	400
	Stencil Thickness (µm)	100	150	150
	Solder Release (%)	90	90	90
	Volume (e06 μm^3)	6.33	9.49	8.48
	Board Pad Size (µm)	280	325	450
SOLDER VOLUME	Sphere (e07 μm^3)	1.41	2.24	6.54
	Paste (e06 μm^3)	6.33	9.49	8.48
	TOTAL (e07 μm^3):	2.05	3.19	7.39
CALCULATED STAND-OFF (µm):		240	306	384

**In general, Thermal Cycling (TC) is improved with smaller array sizes.*

Solder release percentage is greatly influenced by the type of stencil. Below is a summary of the types of stencils and the typical release percentages:

Electroform: 90% – 95% release.

Laser Stencil with Electropolish: 80% – 90% release.

Chemical Etch: 65% – 70% release

7 Material Properties

7.1 Benzocyclobutene (BCB) Dielectric

Benzocyclobutene (BCB) is a high performance photosensitive polymer manufactured under the trade name of Cyclotene® by The Dow Chemical Company. BCB is a high-purity polymer solution that was developed for microelectronics applications. The resins are derived from B-staged bisbenzocyclobutene (BCB) monomers and are formulated as high-solids, low-viscosity solutions.

Notable properties of BCB include:

- Low dielectric constant (2.65)
- Low loss at high frequency
- Low moisture absorption (<0.2%)
- Low cure temperature
- High degree of planarization
- Low level of ionics
- High optical clarity
- Good thermal stability
- Excellent chemical resistance
- Good compatibility with various metallization systems
- Excellent Hydrophobic properties (releases absorbed moisture very quickly)

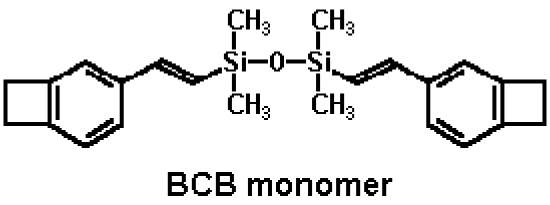


Figure 7. BCB Monomer

The table below gives the physical properties for BCB. For further information on BCB, go to www.cyclotene.com.

7.2 Spheron WLCSP Dielectric

The Spheron advanced polymer was chosen after an exhaustive two-year R&D effort, which evaluated 15 promising microelectronic polymer formulations.

The new polymer was chosen for its outstanding characteristics in the following categories:

- Elasticity
- Elongation
- TCE
- Low moisture content
- Fracture toughness
- Planarization
- Adhesion (>8000 psi) to all adjacent materials
- Enhanced solvent resistance over BCB
- Compatibility to:
    - Passivation layers: organic and inorganic
    - Metals
    - Other layers of the polymer

The new polymer, combined with Spheron WL-CSP's new metal structure, creates a bump structure that offers improved strength and electrical performance over BCB based structures.

Table 11: Comparison of the Spheron Polymer vs. BCB Properties

Property	Spheron Polymer	BCB
Dielectric Constant	2.97	2.65
Dissipation Factor	0.01	0.0008
Glass Transition Temperature, Tg (°C)	284	>350
CTE (T<Tg)	31	52
Tensile Strength (Mpa)	148	87
Young's Modulus (Gpa)	2.8	2.9
Density (at room temperature) g/cm^3	~1.4	~1.6
Elongation %	56	8
Water Absorption %	0.3	0.2

7.3 Solder Alloy Material Properties

Material properties of the common solder Sphere alloys used at FlipChip are presented in the table below. If you need further information on any alloy, please contact FlipChip.

Table 12: Material Properties of Solder Sphere Alloys

Property / Alloy	Sn/2.6Ag/0.6Cu Lead Free	Sn/1.0Ag/0.5Cu Lead Free	63Sn37Pb Eutetic
Liquidious (°C)	220	220	183
Solidous (°C)	218	218	183
Density (g/cm^3)	TBD	TBD	8.4
Young's Modulus (Gpa)	39	39	35
Tensile Strength (Mpa)	35	35	30.6
CTE (ppm/°C)	22	22	25
Elongation (%)	43	43	35 – 53
Electrical Resistively (μΩcm)	TBD	TBD	14.5
Thermal Conductivity (W/m°C)	TBD	TBD	50.9
Alpha Emissions (Counts/cm^2/hr)	<0.002	<0.002	N/A
Poisson Ratio	TBD	TBD	0.4

7.4 UBM Metal Properties

Material properties of the sputtered metals used in Under Bump Metallization (UBM) used at FlipChip are presented in the table below. If you need further information on any metal used in the bumping processes, please contact FlipChip.

Table 13. Material Properties of the UBM Metals

Property / Alloy	Al	NiV*	Cu	Ti
Melting Point (°C)	660	1442	1084	1770
Density (g/cm^3)	2.7	8.9	8.96	4.5
Young's Modulus (Gpa)	69	200 – 210	128 – 130	116
Tensile Strength (Mpa)	47.4	482	351	
CTE (ppm/°C)	23.1	13.4	16.5	8.6
Elongation (%)	10 – 20	2 – 50	10 – 50	20 – 30
Electrical Resistivity (μΩcm)	2.65 – 2.8** 2.65 – 2.8**	7.8** 59.3**	1.7** 1.7**	40** 89.5**
Thermal Conductivity (W/m°C)	235	91	393 – 400	22
Poisson Ratio	0.35	0.31	0.31	0.32

* Values are for Ni (Properties for V doped Ni are very close to pure Ni.)

** Values are for bulk material.

8 Glossary

Al/NiV/Cu	Combination of thin film conductor layers that are sputtered and then etched to form the UBM pads in FlipChip's SFC, Repassivation, *UltraCSP*, and Polymer Collar WLP flows. Also forms the redistribution runners in the *UltraCSP* flow. Also known as one of the combinations of metals used to form the Under-Bump-Metallurgy (UBM).
Array	A pattern of columns and rows. Used to describe bumps that are evenly spaced in rows and columns all across the die surface and not just near the edges.
Array Pattern	Number of rows and columns in a matrix-designed layout of solder balls. Can be a fully formed array or may be partially depopulated, with the absence of bumps toward the center of the array.
BCB	(Benzocyclobutene) Dielectric coating that provides an additional passivation layer on top of the IC passivation for Repassivation, Redistribution, *UltraCSP*, and Polymer Collar WLP designs.
BCB1 Opening (Via)	Opening in the first layer of BCB where IC aluminum pads will be re-routed to facilitate a certain *UltraCSP* designs.
BCB2 Opening (Via)	Opening in the second layer of BCB which will define the metal exposure (wettable area) of the UBM pad. BCB2 will cover all re-distribution traces to protect metal runners from corrosion and physical damage.
Bond Pad	Exposed final metal portion of the device I/O (see also, Pad).
Bump	A small metal alloy deposit on the die that is melted to a pad on the board to form the electrical connection between the board and the die.
Bump Diameter	The widest measurement through the center cross-section of a re-flowed bump.
Bump Height	Vertical measurement from the top of the device passivation to the top of the bump after reflow (not yet attached to PCB substrate). After assembly, the analogous measurement is called "stand-off height".
Bump Shear	Shear value (force measured in grams) and failure mode measured during ball shear test.
Bump Standoff Height	Measurement from FR4 surface to silicon surface
Cu Pad	Solder receiving pad on the substrate that is Cu etch-defined.
Cu Pillar Bump	An integrated circuit flip chip bumping technology involving a Cu pillar that is capped with solder. The Cu pillar provides a built-in, non-collapsing stand-off to facilitate flip chip assembly. Cu pillar bumps are used for finer pitches usually below 150 microns.

Die (Chip)	A square or rectangular piece cut from the wafer that contains the electrical pattern and is repeated in several rows and columns across the top surface of the wafer.
Die (Chip) Size	The active silicon chip area bounded on the outside by the scribe street.
Die (Chip) Stepping Distance	The distance between one point on a die and the same point on an adjacent die. This measurement takes into account both the die size along with the width of the street.
DNP	Distance to neutral point. (The distance from an I/O to the center of the die.) Maximum DNP defines the largest array size for a given process technology that will meet the minimum thermal fatigue performance criteria as established by FlipChip.
Drop Testing	Reliability (REL) test that involves repeatedly dropping a board mounted device to measure continuity. Spheron WLCSP provides outstanding drop test performance.
Electroless Nickel Plating	A chemical reduction process which depends upon the catalytic reduction process of nickel ions in an aqueous solution (containing a chemical reducing agent) and the subsequent deposition of nickel metal without the use of electrical energy.
*Elite*CSP™	A WLCSP product line that is specifically designed for bumping applications that require rapid cycle times, quick time to market, low bumping costs, and high temperature stability. Utilizes an Electroless Ni/Au UBM.
*Elite*FC™	A low cost product that is very similar to the Standard Flip Chip (SFC) product. Utilizes an Electroless Ni/Au UBM.
*Elite*UBM™	A product that consists only of a Electroless Ni/Au UBM. Typically used for low cost RFID applications.
EDC	EDC or Embeddable Die Customization refers to wafer level modification of integrated circuits to prepare them for embedding in printed circuit board or wafer level embedded die applications.
ESD	(Electrostatic discharge) The release of static electricity from one surface to another. Because IC devices and assemblies may be damaged by ESD, precautions are taken to eliminate ESD in IC manufacturing and test areas.
Final Metal	Uppermost metal layer in a device. This layer is usually covered with a thick (~1um) dielectric passivation.
Flip Chip	A die that has bumps to create the electrical connection between the die and the board. So called because the die has to be flipped over in order to be assembled.
I/O	The location of the signal interfaces that contacts to the "outside" world.

I/O Final Metal Bond Pad	Same as I/O
I/O Metal Pad Size	Size of metal bond pad on an I/O, as manufactured during normal IC processing.
Maximum DNP	DNP stands for Distance to Neutral Point. A maximum DNP is the distance from the furthest I/O (solder bump) to the minimum stress point on the die. For a symmetric array pattern, it is also the geometric center of the die.
MDIF/SOW	(Mask Design Information Form / Statement of Work) FlipChip information form that provides FlipChip with a description of the wafer, the die, and how you would like to bump and dice them.
NSMD	(Non-Solder Mask Defined) PCB Copper pads that are smaller than the solder mask openings.
Pad	Metal area on the die that the bump or wire is attached to (see also, Bond Pad).
Partial Die	An incomplete die usually located on the edge of the wafer.
Passivation	Uppermost layer on an IC. Used for circuit protection and cushioning. Typically Nitride, Polyimide, Oxide, PIQ, or Oxi-Nitride.
Peripheral	The edge of the die. Used to describe bumps that are placed near the edges of the die.
PO	(Passivation Opening) Opening in the passivation over the I/O final metal bond pads.
PCB	Printed Circuit Board.
Pitch	The linear distance between the centers of two adjacent I/Os or bumps.
PIQ	(Polyimide Isoindoro Quinazorindione) Non-standard Dielectric polymer material used as a passivation layer in some semiconductor devices.
Repassivation	Layer of Passivation added by FlipChip as part of the bumping process. This layer adds robustness and can correct inappropriate Passivation Openings and Final Metal Pads. The repassivation layer is typically BCB or Spheron Polymer.
RDL	(Re-Distribution Line) Metal deposited at the same time as the UBM pad for the purpose of re-routing I/O sites, for example from edge-distributed bond pads used in wire-bonded applications, to an array layout. Also broadly used to describe the process of rerouting I/O. RDL options at FCI include sputtered metal and plated metal options.
SMD	(Solder Mask Defined) PCB pads that have solder-mask openings smaller than the copper pads.
Solder Mask	A layer of passivation material covered on top of outer-layer conductor (Cu) that has openings to allow solder wet to the Cu pads and prevents

	solder bridging in the rest area. These openings are called Solder Mask Openings.
Solder Paste	Reflowable pre-mixed solder paste that is printed and formed into a solder sphere. Provides the electrical connection between the die and the package substrate or printed circuit board. Since it is premixed, it provides for excellent composition control. Typically made up of two to four metals.
Solder/Flux Ratio	The volume ratio of flux to solder in the solder paste. A 50/50 ratio of solder to flux is recommended.
Sphere Diameter	Diameter of the pre-formed solder sphere used in Wafer Level Packaging. Typical ball diameters are 300, 350, 400, and 500□m.
Spheron™	FlipChip International WLCSP product predominately used in high frequency applications. It uses the proprietary Spheron Polymer to give enhanced performance over BCB in certain circumstances.
Stencil Aperture Opening	The laser-cut, Nickel Additive (E-Fab), Chemically Etched, or Electroform aperture openings on the solder paste stencil.
Stepping Distance	Linear measurements in both the x and y directions comprising die size and to the center of the scribe streets on all four sides. (see die stepping distance)
Street	The non-electrically active area on the wafer in between the die. Also known as the Saw Street.
UBM	(Under-Bump-Metallurgy) The metal stack that is deposited under the bump as part of the solder bumping process. It has the combined features of adhesion layer, diffusion barrier, wetting layer and oxidation protection layer. FlipChip uses Al/NiV/Cu, Ti/NiV/Cu, Al/NiV/Cu/Ti, or Ni/Au as the UBM.
Wafer	A round flat disk most often made of silicon that is patterned with several die by semiconductor thin-films processing. Each wafer has a flat or notch cut into its edge to help with aligning or orienting the wafer.
Wafer Map	A representation of the wafer that notes where all of the defective die are located.
Wire Bond	The electrical connection consisting partially of a wire that bridges the die to the board.
WL-CSP	Wafer Level Chip Scale Package. An advanced semiconductor package consisting only of a die with solder bumps. Final package size is the size of the starting die.

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