DESIGN AND IMPLEMENTATION OF A FULLY DIFFERENTIAL FOLDED-CASCODE OPAMP

Final Project of ELE539- Analog Integrated Circuit Design

Student: Fu Luo

Instructor: Prof. Godi Fischer

Date: 12/11/2008

1 Background

2 Circuit design and simulation

2.1 Folded-Cascode OTA

2.2 Circuit design and implementation

2.3 Simulation results comparison

2.4 Layout Consideration

3 Future work

1. Background

Since there is only capacitive load to be driven in switched capacitor circuits, no voltage buffer is necessary. The opamps can achieve higher speed and wider swing with special designs, like a folded-cascode opamp and a current mirror opamp. They are usually called Operational Transconductance Amplifier because of the importance of their transconductance value. Instead of using a Miller compensation capacitor as in two-stage opamp design, OTAs use the load capacitor to achieve compensation.

The basic idea of the folded-cascode opamp is to apply cascode opamp transistors to the input differential pair but using transistors opposite on type from these used in the input stage. The arrangement of opposite-type transistors allows the output of this single gain–stage amplifier to be taken at the same bias-voltage levels as the input signals.

Most modern high-performance analog integrated circuits make use of fully differential signal paths. With opamps, this technique results in differential output as well as inputs, and hence, they are referred to as fully differential opamps. One of the major driving forces behind the use of fully differential signals is to help reject noise from the substrate as well as from pass-transistor switches turning off in swithed-capacitor applications.

The reason for this noise rejection is that if the circuit is built in a symmetric manner, then the noise will affect both signal paths identically, and will be rejected, since only the difference between signals is of importance. For this reason, fully differential amplifier become more and more popular in microcircuit design.

Due to its wider common mode input range and lower thermal noise, the fully differential folded-cascode OTA architecture is chosen for this project.

2. Circuit design and simulation

Design methodology of fully differential amplifier has 3 steps

Step1: Based on the specifications, design a single-ended amplifier

Step2: Choose a topology of common mode feedback circuit and design the circuit.

Step3: Replace the single-ended amplifier with fully differential amplifier based on the topologies.

Folded-Cascode OTA

Fig.1 shows a folded-cascode opamp. I_{bias1}, I_{bias2}, V_{B1} and V_{B2} are derived from the biasing circuit which will be discussed later. M_3 through M_6 consist of a folded-cascode wide-swing current mirror with opposite-type as the load of differential-input amplifier M_1-$_2$. M_7 and M_9, M_8 and M_{10} consist of two current sources. It has only a capacitive load C_L at output node. V_{C4} and two differential outputs are connected to the common mode feedback circuit which will also be covered later in the next section. And if the Folded-Cascode OTA is a single-ended circuit, the red connection in the figure should be added, if the Folded-Cascode OTA is fully differential, the red connection should disconnect.

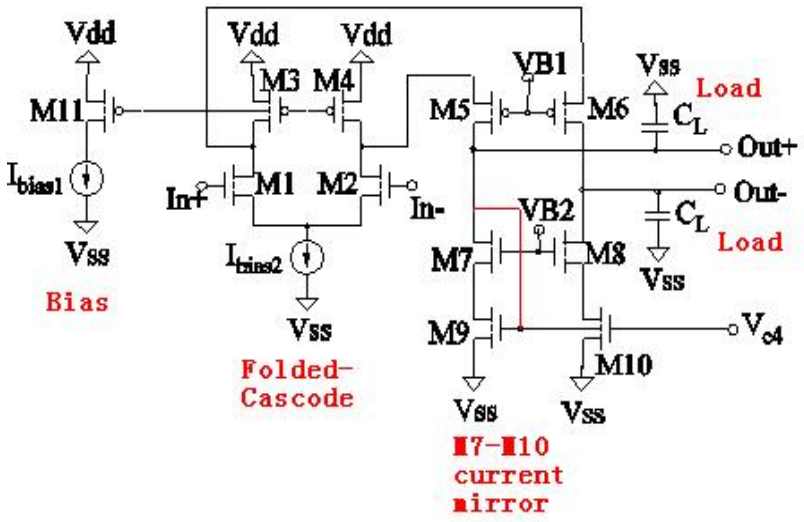

Figure1. Folded-cascode OTA

Common mode input range

$$V_{in-\min} = V_{SS} + 3V_{eff} + V_{th-n}$$

$$V_{in-\max} = V_{dd} - V_{eff} + V_{th-n}$$

Output swing

$$V_{out-swing} = \left(V_{dd} - 2V_{eff}\right) - \left(V_{SS} + 2V_{eff}\right) = V_{dd} - V_{SS} - 4V_{eff}$$

Here we assume that all the transistors have the same effective voltage. In reality, it might not be true.

Output impedance

$$r_{out-1} = g_{m6} r_{ds6} R$$

and

$$r_{out-2} = g_{m8} r_{ds8} r_{ds10}$$

then

$$r_{out} = r_{out-1} // r_{out-2} \approx g_m \frac{r_{ds}^{\ 2}}{2}$$

AC and DC Gain

Since this circuit drives only a capacitive load, in small signal analysis, the differential output current from the drain of differential pair M_1 and M_2 is only applied to the load capacitance C_L. Therefore the circuit can be simplified as a basic differential gain stage. Then the AC gain is given by

$$A_V = g_{m1} Z_{out} = g_{m1}\left(r_{out} // \frac{1}{sC_L}\right) = \frac{g_{m1} r_{out}}{1 + s r_{out} C_L}$$

and the unity-gain frequency

$$\omega_{ta} = \frac{g_{m1}}{C_L}$$

The DC gain of the folded-cascode opamp $A_V(0) = g_{m1} r_{out}$, g_{m1} is the transconductance of the input transistors. The high gain of this single stage opamp stems from the high output impedance of this circuit taking advantage of the cascode technique.Unlike the two-stage opamp, the stability compensation is directly achieved by the output capacitance provided C_L is much larger than any parasitic capacitance. The time constants introduced by the impedance and parasitic capacitances at the sources of M_5 and M_6 dominate the second poles of this opamp.

Slew Rate

$SR = \frac{I_{d4}}{C_L}$, I_{d4} is the current went through M4 which is the bias current of the circuit.

Circuit design and implementation

Biasing circuit:

The wide swing current mirror as shown in Fig.2 has been chosen as bias circuit to provide the necessary current and voltage references. The two biasing current sources, I_{bias1} and I_{bias2}, are derived from the same circuit so as to keep the current of $I_{d5/6}$ independent of any process or environment variation as much as possible.

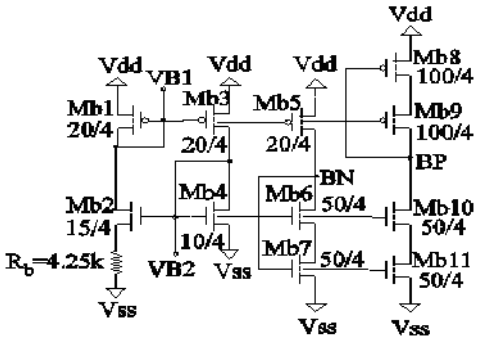

Figure 2 Biasing circuit with wide swing

Moreover, the current mirrors used to derive $I_{bias1/2}$ are composed of transistors realized as parallel combination of unit-sized transistors to guarantee the independency over environment and process variations.

Single-ended folded-cascode Opamp

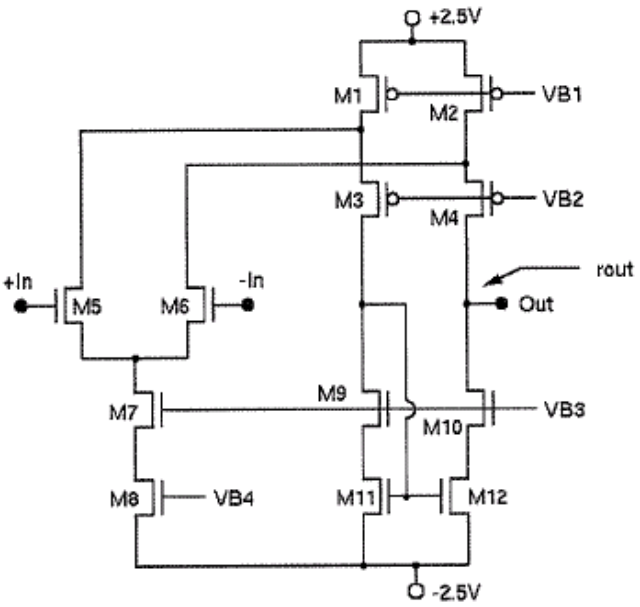

Figure 3. single-ended folded cascade Opamp

As shown in the Figure 3, this is a typical single-ended folded cascade Opamp, and in the next section, we will discuss how to calculate the sizes of the each transistor.

Design Procedure of Single-ended Opamp

The basic specifications for this project are the unity-gain bandwidth (UGB) would be equal or greater than 60Mhz and clock frequency is 10Mhz. Load capacitor is 1pf. Usually the circuit should settle within about half a clock period, so, for a 10Mhz clock frequency, the settling time has to be equal or less than 50ns.

Step1: Based on the bandwidth limitation ω ta, the transconductance of M1 is chosen

$$g_{m1} = 2\pi * \omega_{ta} * C_L$$

Step2: for a 10MHz sampling frequency and 5V supply rail the slew rate should be equal to or greater than

$$SR = \frac{5}{(1/10MHz)/2} = 100V/\mu s$$

$$I_{out} = SR * C_L$$

In this project, I push the slew rate mostly, because slew rate will impact the veracity of ADC which is the future work. The higher slew rate we have, the more veracity we can implement in some degree.

Step 3: The current in the differential branch is given by

$$I_{d1} = \frac{I_{d6}}{2\alpha - 1} \qquad \alpha = \frac{I_{d3}}{I_{bias2}}$$

And α =1 is a good starting point. α =1 means the current go through M5 equal to the current go through M3 and both of them equal the half of the total bias current I_{m1} above analysis are based on Fig.1.

Step 4: The size of transistor M1 and M2 can then be determined by

$$(W/L)_1 = \frac{g_{m1}^2}{2\mu_n C_{OX} I_{d1}}$$

Step5: Veff of output branch M4,6,8,10 is determined to ensure symmetric swing

$$V_{eff\,4} = V_{eff\,6} = V_{eff\,8} = V_{eff\,10} = \frac{V_{dd} - V_{SS} - V_{out-swing}}{4}$$

Using the steps above, we can calculate size of all the transistors. When we replace the single ended amplifier with fully differential amplifier, the performance might change slightly when compares with the original single ended amplifier. The fine tuning should be made here such that the final performance does meet all the design specifications.

Common-Mode Feedback Circuit

The common-mode feedback circuit used to sense the common-mode signal and feed it back to the amplifier for cancellation is shown in Fig.4. The common mode has been set at analog ground.

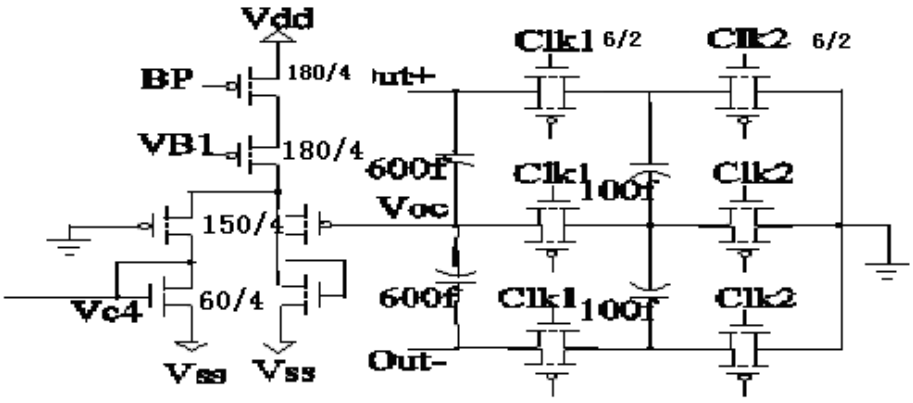

Figure 4. Common Mode Feedback Circuit

the output V_{oc} is the common-mode voltage of V_{out+} and V_{out-}, which is $V_{oc} = \frac{1}{2}\left(V_{out}^{+} + V_{out}^{-}\right)$. Normally, all of the switches would be realized by minimum-size n-channel transistors only, except for the switched connected to the outputs, which might be realized by transmission gates (parallel n-channel and p-channel transistors both having minimum size) to accommodate a wider signal swing. In this project, I use transmission gates for all the switches with W/L=6/2. There are many advantages of transmission gate

1) MOSFET exhibit no DC offset
2) Extremely small leakage currents on off-state
3) Ron variations acceptable over full signal swing
4) 1^{st} order elimination of clock feedthrough

In applications where the opamp is being used to realize switch-capacitor circuits, switch-capacitor CMFB circuits are generally preferred over their continuous-time counterparts since they allow a large output swing. Except the switch capacitor circuit, there is a small sense-amplifier circuit in the CMFB. The sense-amplifier compares V_{OC} with the desired common-mode (analog ground) and provides the control voltages V_{C4} for the current source of the opamp.

The equivalent circuit of the common mode feedback circuit is fig 5.as below:

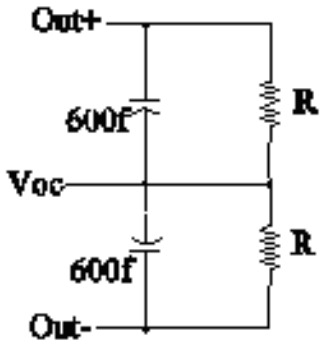

Figure 5. equivalent circuit of the common mode feedback

Req=1/C*Fc, where Fc is switch clock frequency.

Fully differential folded-cascode Opamp

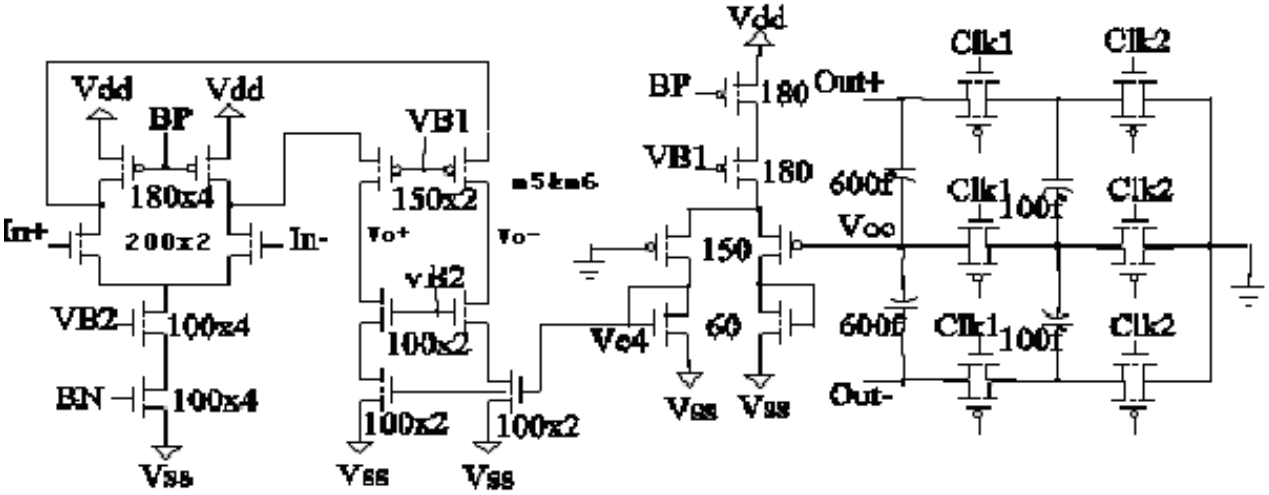

Figure 6. Fully differential folded-cascode opamp

There is one technical problem when using HSPICE to simulate switched-capacitor circuits. Since HSPICE just can simulate linear module and can do nothing about the nonlinear system. Therefore, no AC response could be obtained for a switch-capacitor common-mode feedback circuit. and only the transient analysis is available for verification. But the simulation for the equivalent RC CMFB can be used as a substitute. In short, my way is using RC equivalent circuit to do all the AC analysis and all the transient analysis can be done by the switch capacitor circuit.

Another issue we need pay attention to is that the performance might change slightly when compared with the original single ended amplifier. The fine tuning should be

made here such that the final performance does meet all the design specifications. The final fully-differential OTA is shown in Fig.6.

The most obstinate problem is improving the phase margin, if the phase margin is less than 45 degree, the only way to improve it is to reduce the parasitic capacitor. Since the frequency of the second pole is inverse proportion to the parasitic capacitor. So once the capacitance reduced, the distance between the dominant pole and second pole will be split. Therefore we can get better phase margin.

Test Circuit Set-up for Hspice

Fig 7 is the test circuit set-up for hspice

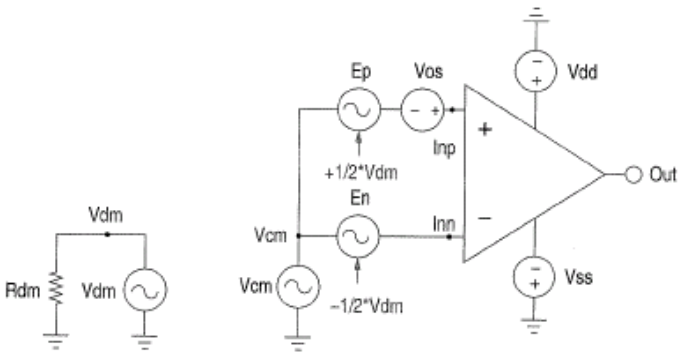

Figure 7 test circuit set-up for hspice

And in Hspice, the MOSFET mode should be described as

MOS D G S B model W L Ad Pd As Ps,

if you do not use Area and Periphery parameters, it is differential to get the right phase margin.

Simulation results comparison

parameters	values
Vdd, Vss，	±2.5V
DC Gain	3411.9
Unity-gain Frequency	170.75MHz
Phase Margin	58 degree
Positive Slew-rate	178.29V/μs
Negative Slew-rate	-160.12V/ μs
Output Swing	7.3V peak-to-peak
Power Dissipation	5.517mW

Table 1. Cl=1.5p,Clock freq of switch=625Khz, Fs=5Mhz

From Figure 8-10, we get all the data in Table1.

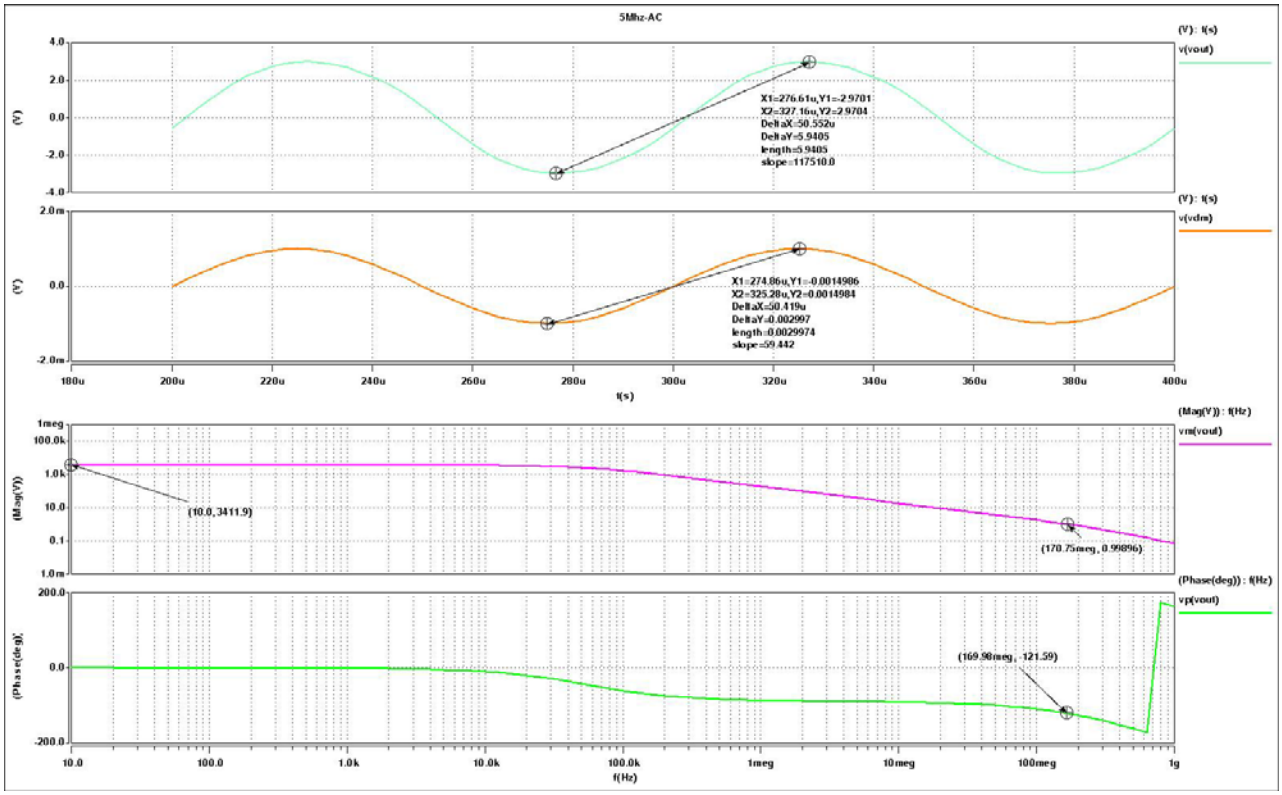

Figure 8. AC analysis - Cl=1.5p,Clock freq of switch=625Khz, Fs=5Mhz

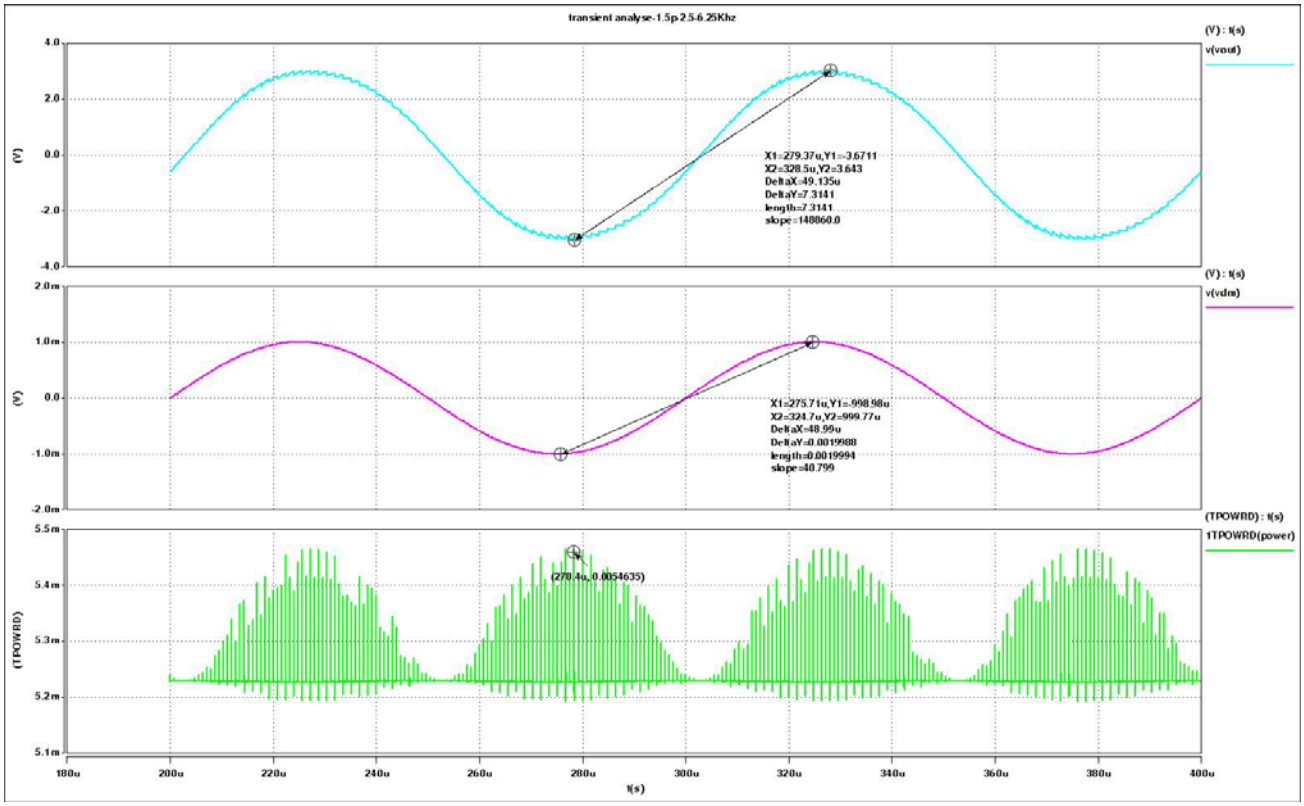

Figure 9. Gain and Power- Cl=1.5p,Clock freq of switch=625Khz, Fs=5Mhz

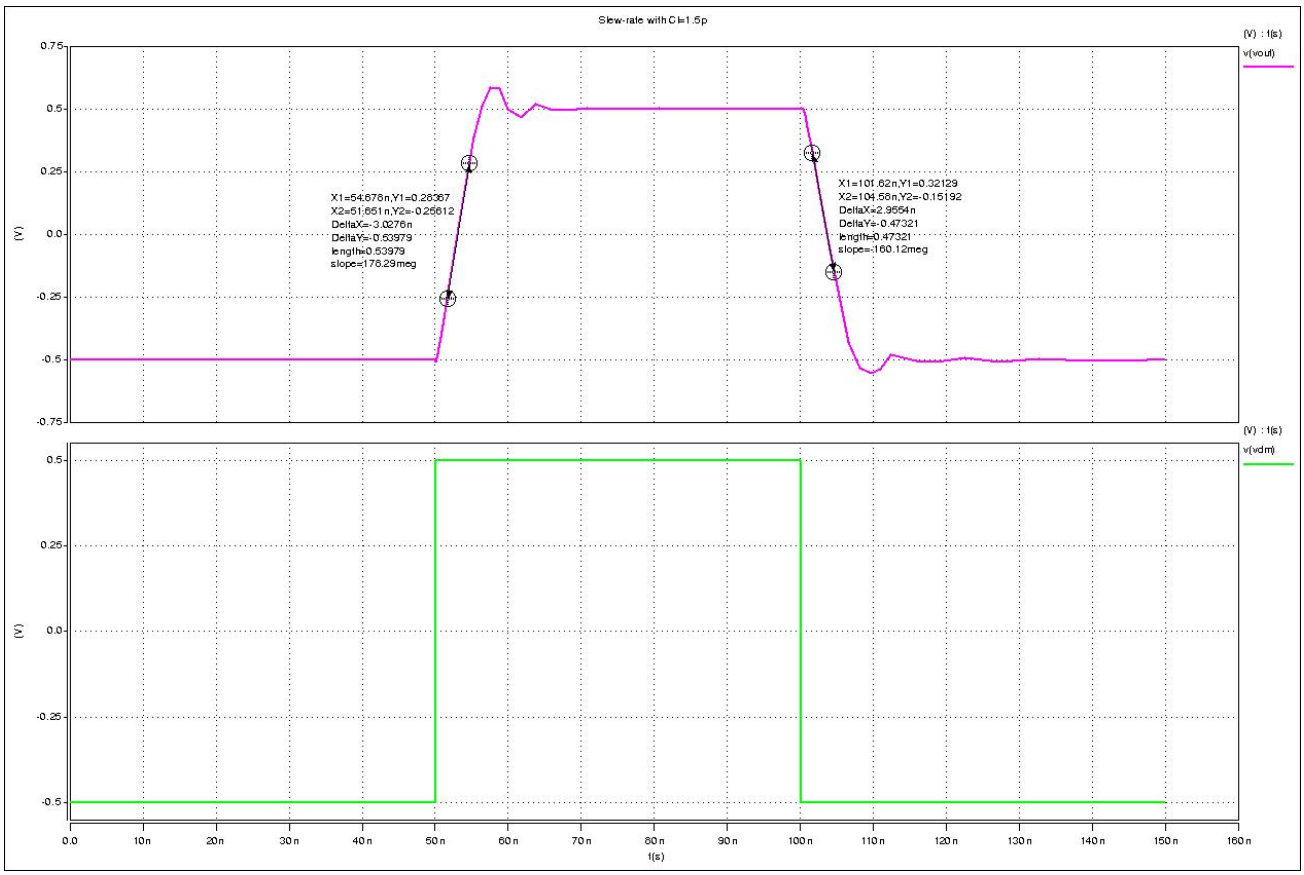

Figure10. Slew rate - Cl=1.5p,Clock freq of switch=625Khz,Fs=5Mhz

parameters	values
Vdd, Vss ,	±2.5V
DC Gain	3159.4
Unity-gain Frequency	169.3MHz
Phase Margin	58 degree
Positive Slew-rate	176.02V/μs
Negative Slew-rate	-160.16V/ μs

Output Swing	7.1V peak-to-peak
Power Dissipation	5.391mW

Table 2. Cl=1.5p, clock of switch=1250Khz, Fs=10Mhz

From Figure 11-13, we get all the data in Table 2.

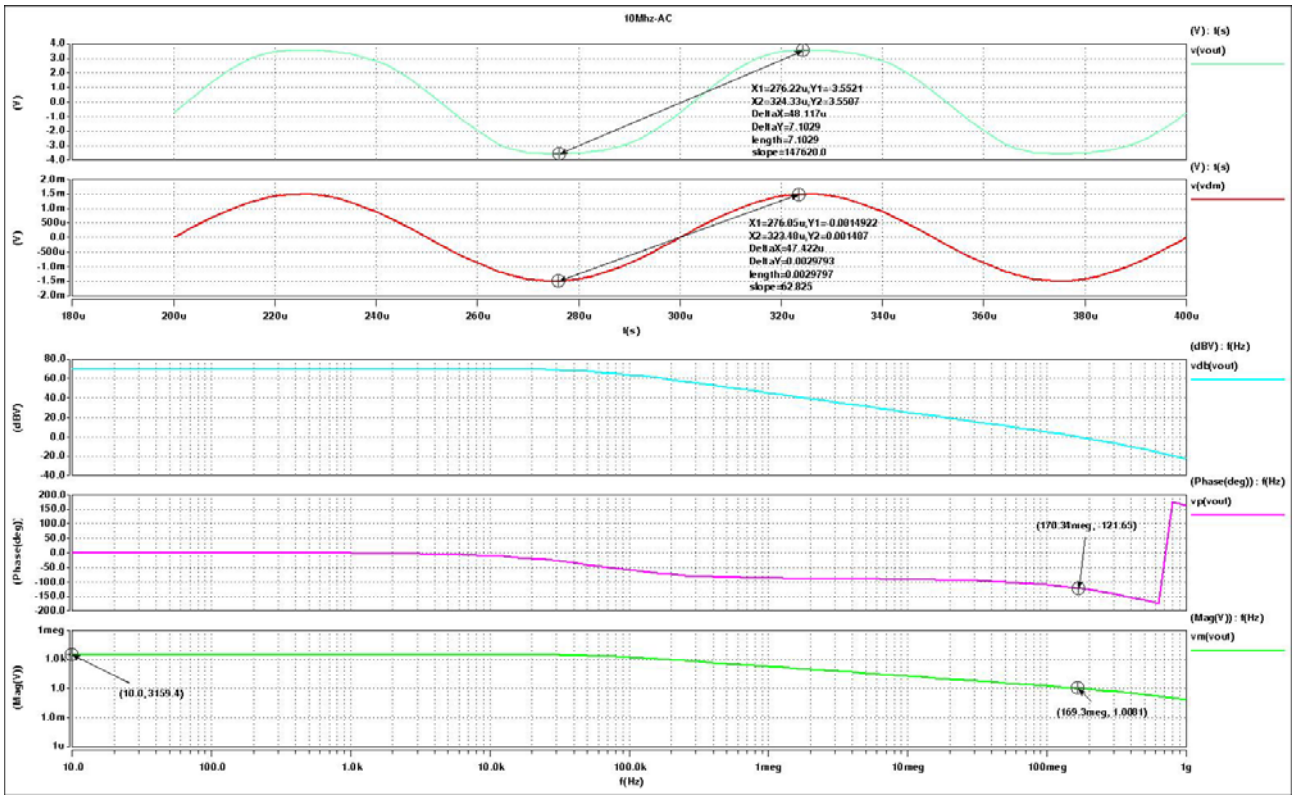

Figure 11. AC analysis-Cl=1.5p, clock of switch=1250Khz, Fs=10Mhz

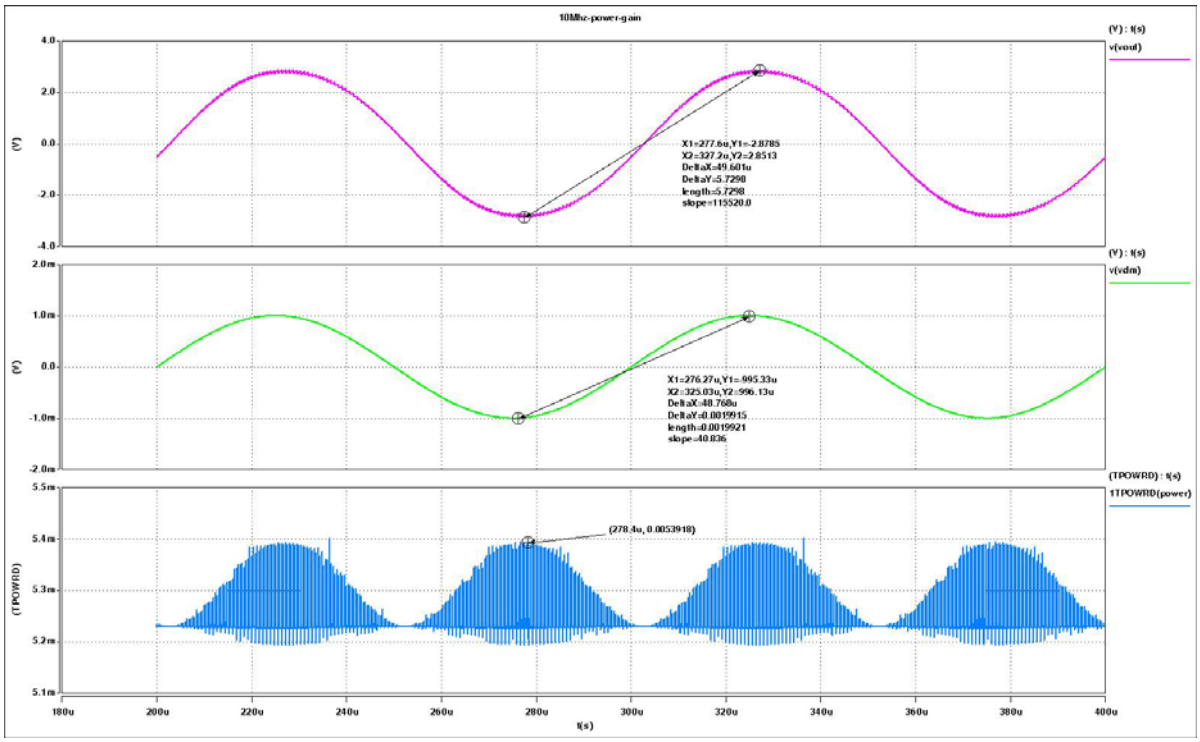

Figure 12. Gain and Power-Cl=1.5p, clock of switch=1250Khz, Fs=10Mhz

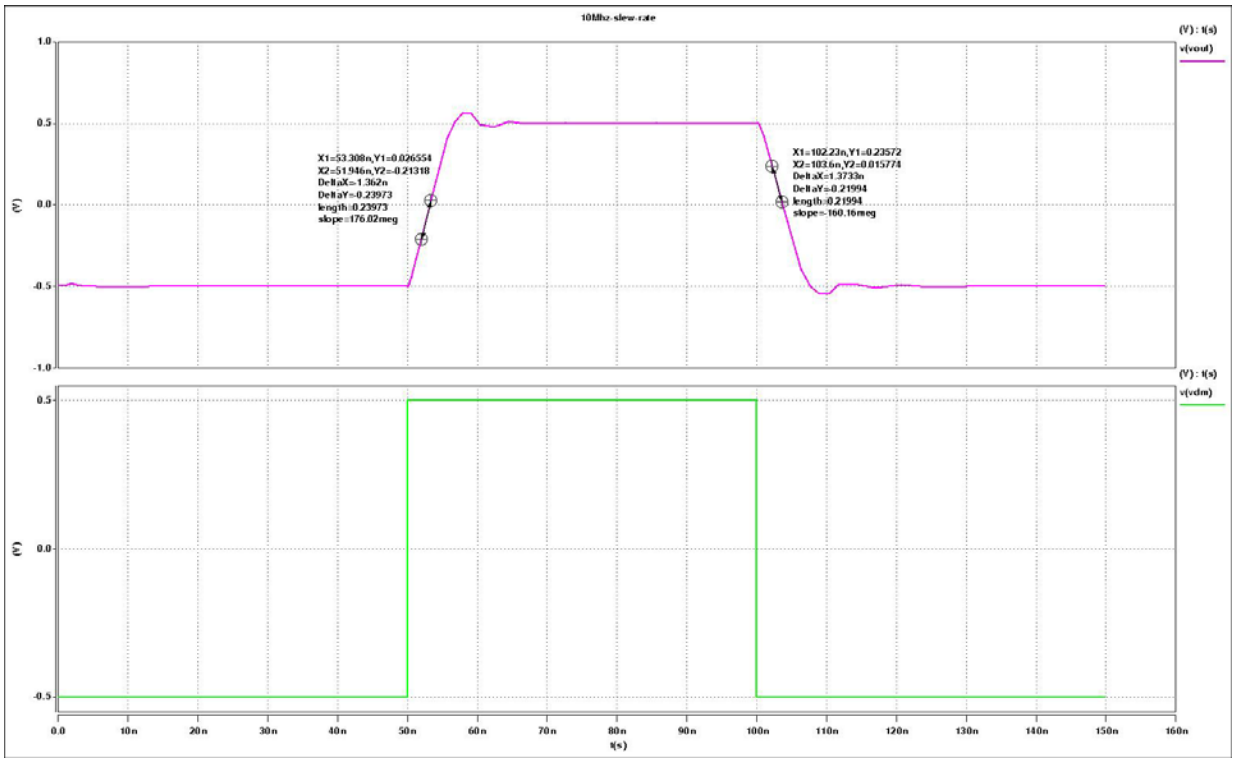

Figure 13. Slew rate-Cl=1.5p, clock of switch=1250Khz, Fs=10Mhz

parameters	Values
Vdd, Vss，	±2.5V
DC Gain	2752.0
Unity-gain Frequency	172.77MHz
Phase Margin	58degree
Positive Slew-rate	176.13V/μs
Negative Slew-rate	-162.56V/ μs
Output Swing	6.8V peak-to-peak
Power Dissipation	5.382mW

Table 3. Cl=1.5p, clock of switch=2500Khz, Fs=20Mhz

From Figure 14-16, we get all the data in Table 3.

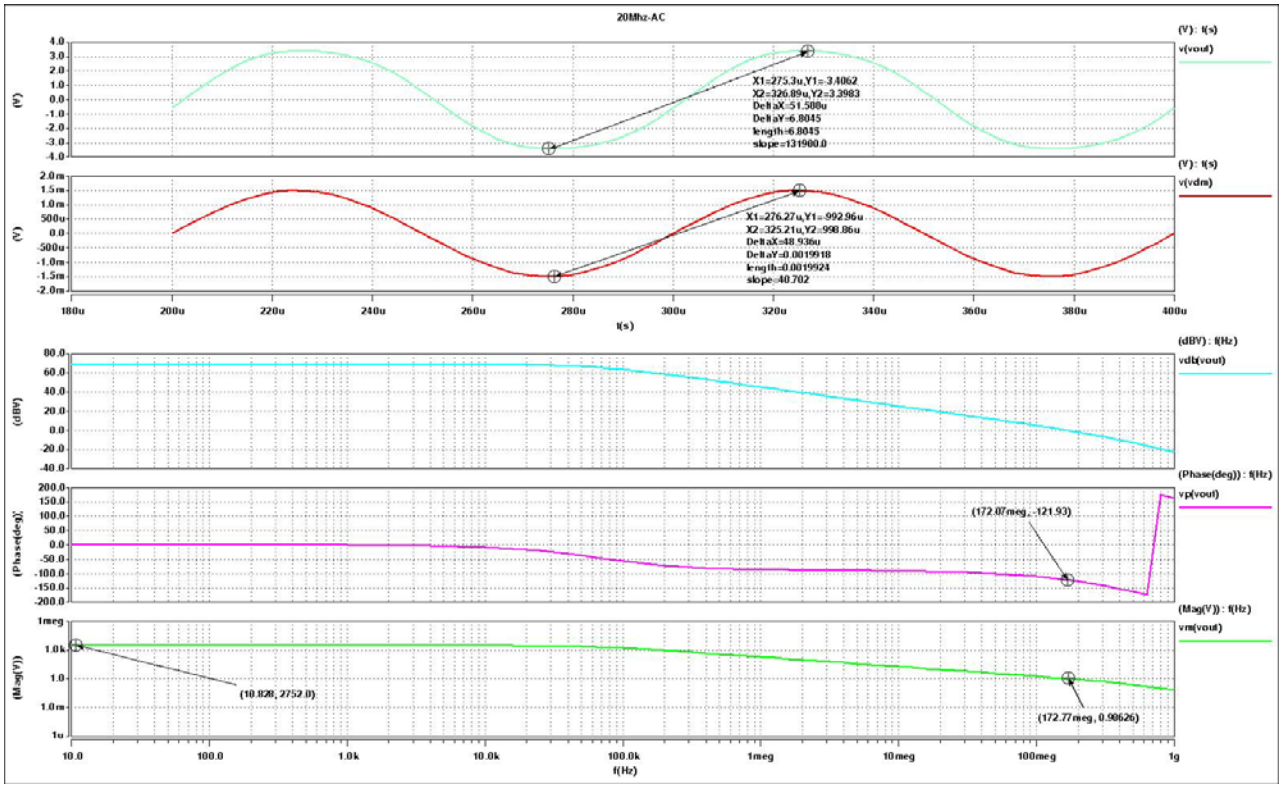

Figure 14. AC analysis-Cl=1.5p, clock of switch=2500Khz, Fs=20Mhz

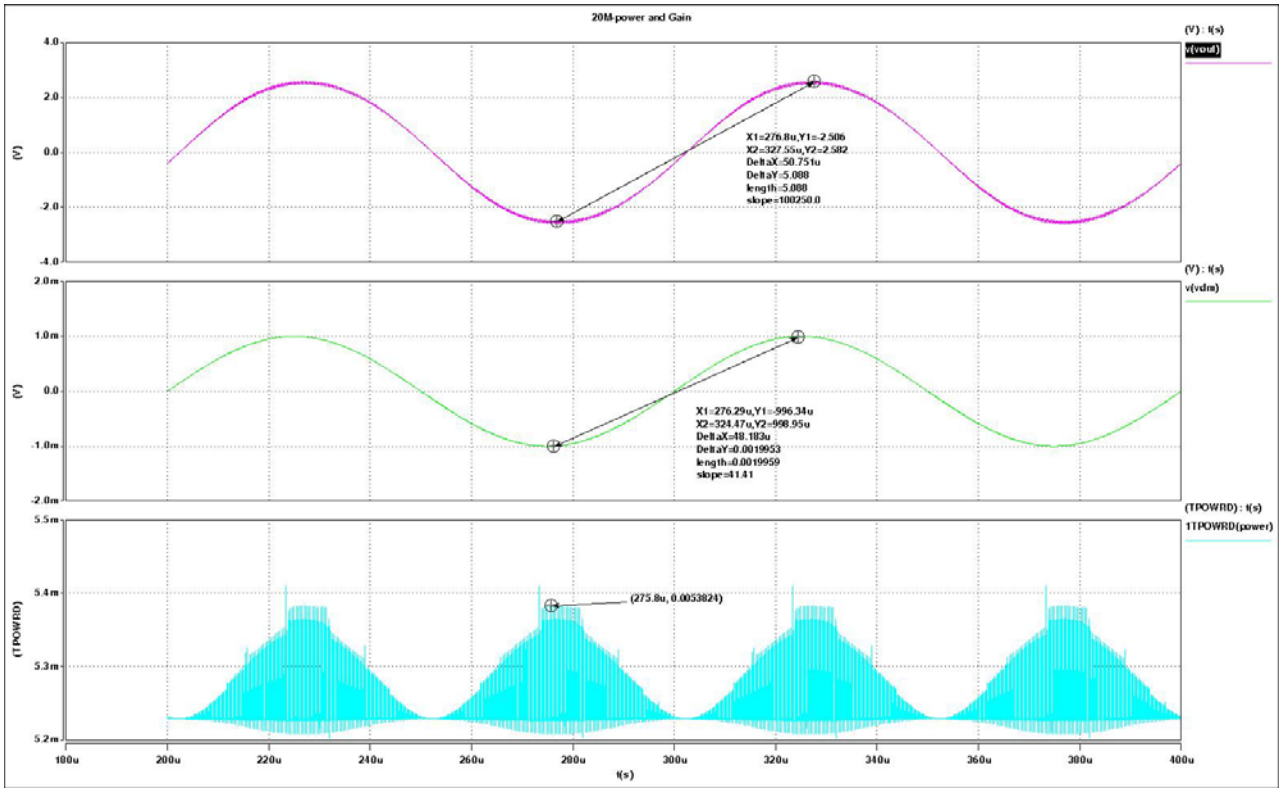

Figure 15. Gain and Power-Cl=1.5p, clock of switch=2500Khz, Fs=20Mhz

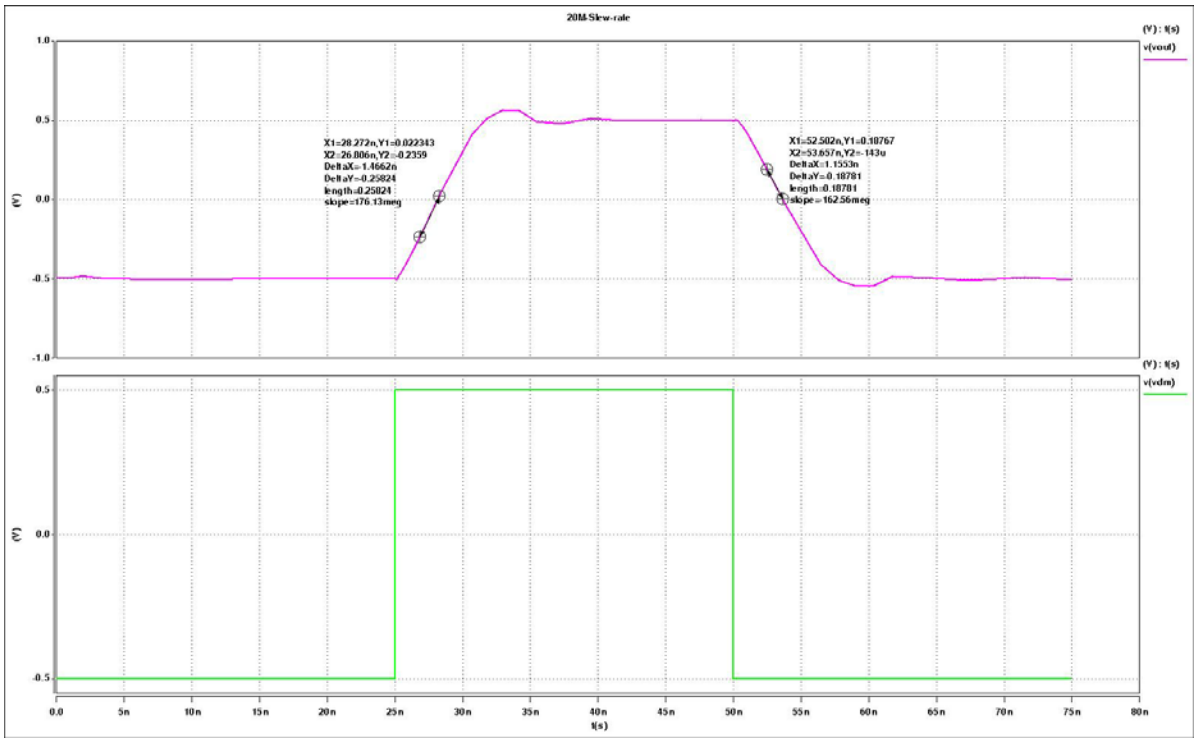

Figure 16. Slew-rate-Cl=1.5p, clock of switch=2500Khz, Fs=20Mhz

From table 1-3, we can see that increasing the switch frequency will reduce DC gain, output swing and the total power dissipation. Increasing the switch frequency will make the output signal more smooth.

parameters	values
Vdd, Vss ,	±2.5V
DC Gain	3411.9
Unity-gain Frequency	193.66MHz
Phase Margin	55 degree
Positive Slew-rate	214.73V/μs
Negative Slew-rate	-199.02V/ μs

Output Swing	7.2V peak-to-peak
Power Dissipation	5.415mW

Table 4. Cl=1p, clock of the switch =625Khz,Fs=5Mhz

From figure 17-19, we can get all the data in table 4.

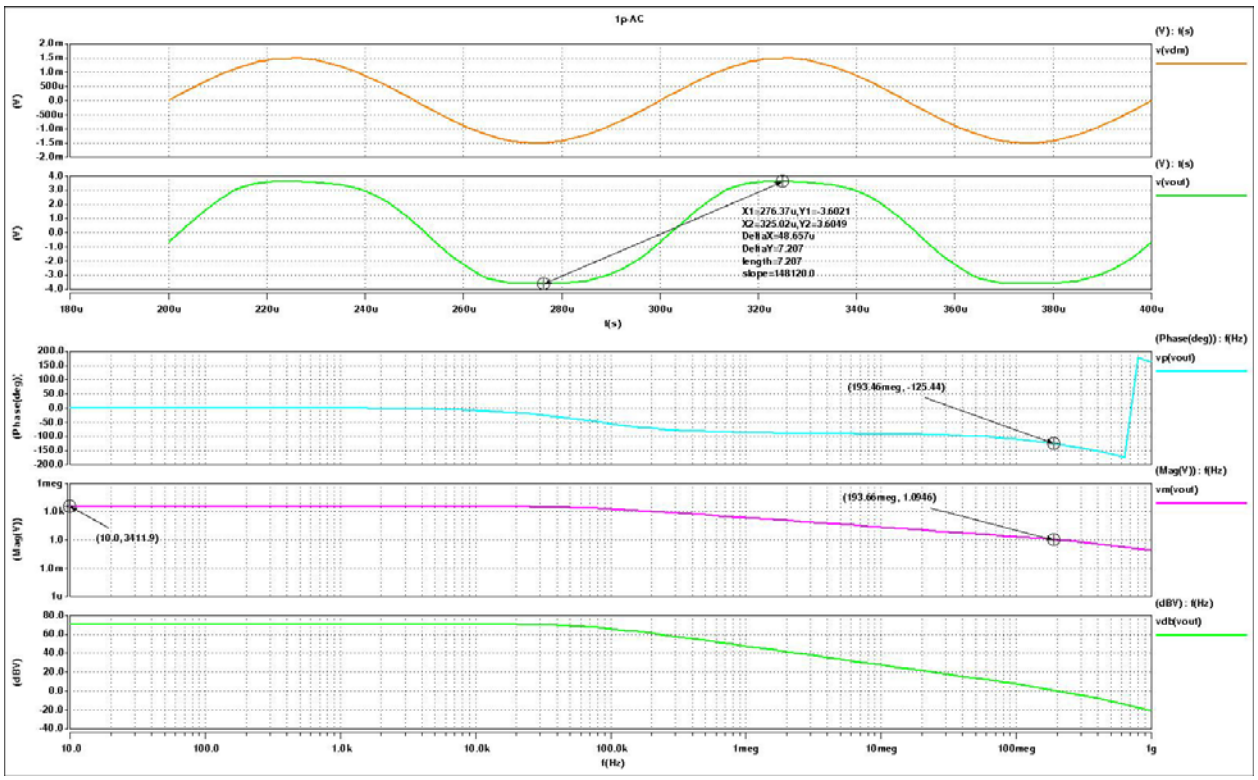

Figure 17. AC analysis-Cl=1p, clock of the switch =625Khz,Fs=5Mhz

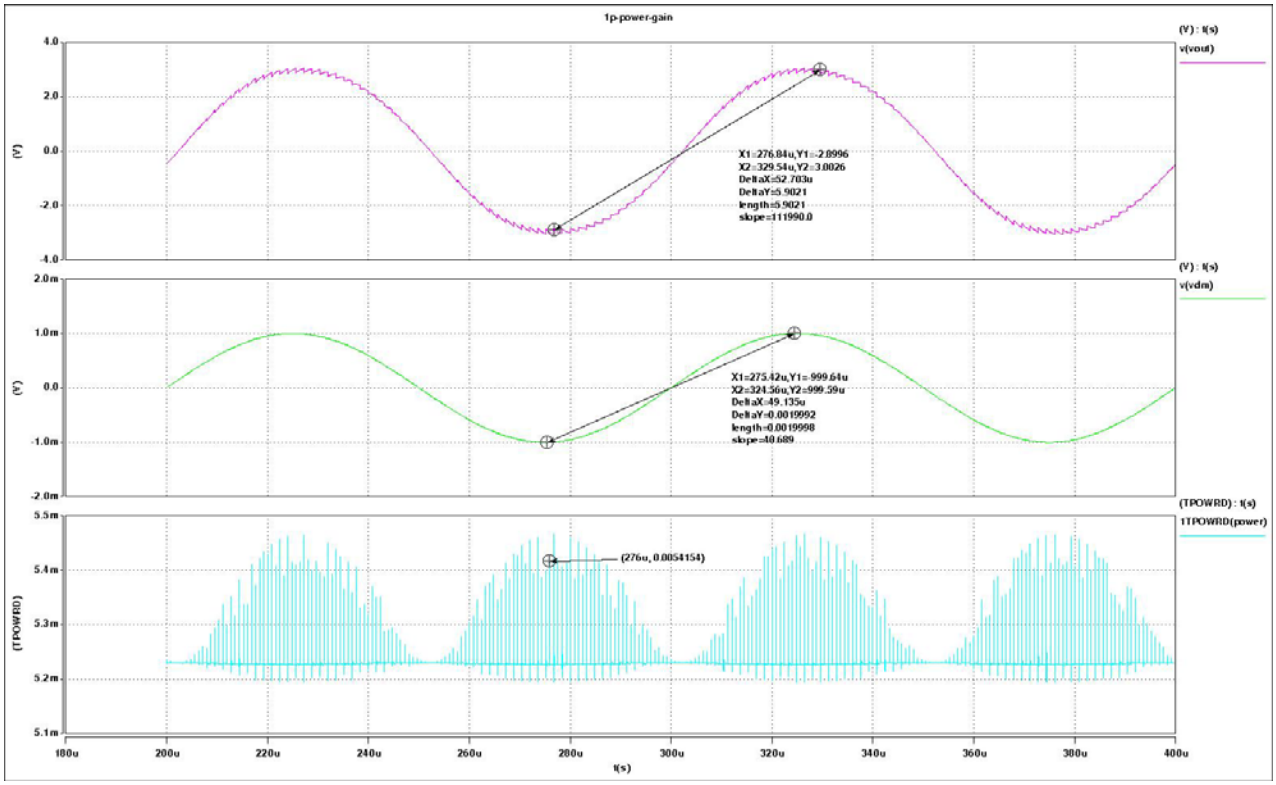

Figure 18. Gain and Power-Cl=1p, clock of the switch =625Khz,Fs=5Mhz

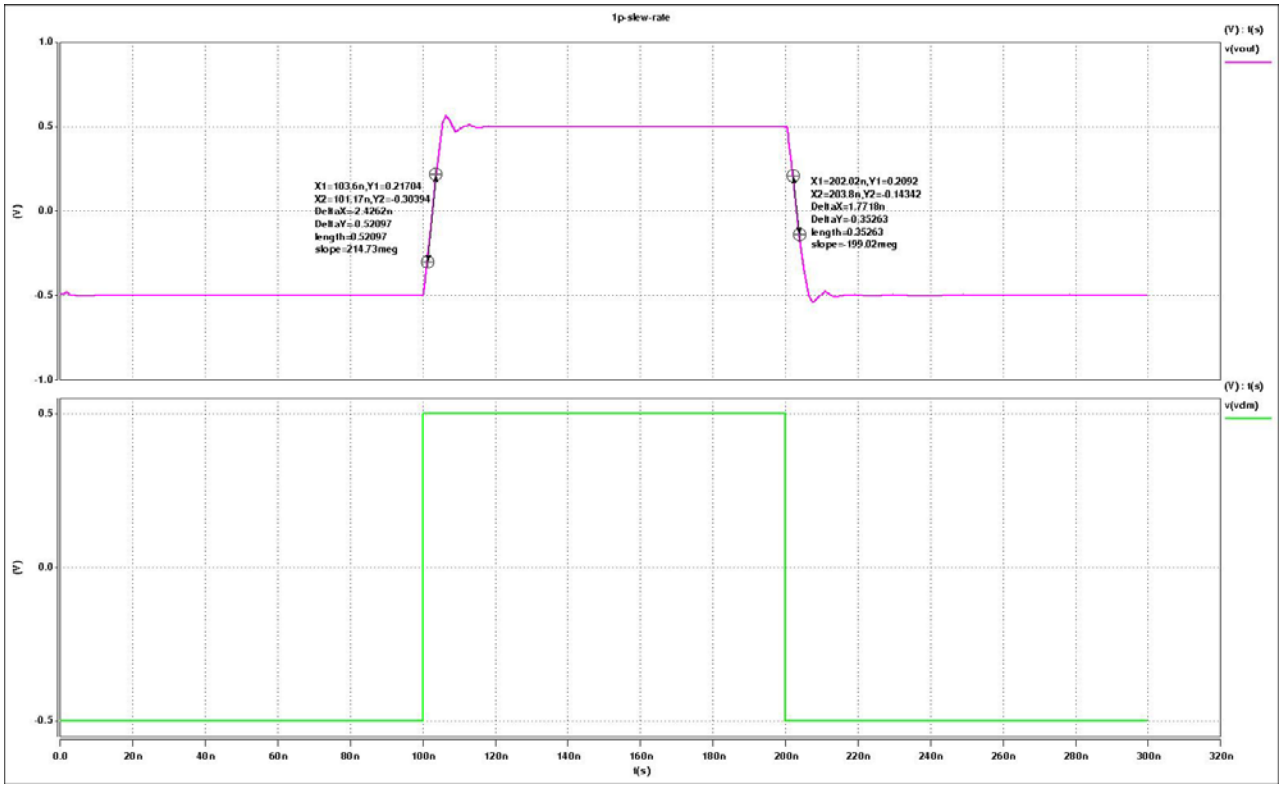

Figure 19. Slew rate-Cl=1p, clock of the switch =625Khz,Fs=5Mhz

Compare table 4 with table 1, we find reducing the Load Capacitor can increase the slew rate sharply, and also can improve the Unit Gain Bandwidth, but phase margin will be lower a little bit.

parameters	values
Vdd, Vss ,	±3.3V
DC Gain	3493.5
Unity-gain Frequency	186.75MHz
Phase Margin	60 degree
Positive Slew-rate	203.5V/μs
Negative Slew-rate	-190.06V/μs
Output Swing	9.2V peak-to-peak
Power Dissipation	8.728mW

Table 5. Cl=1.5p,clock frequency=625Khz,Fs=5mhz

From Figure 20-22, we can get all the data in table 5.

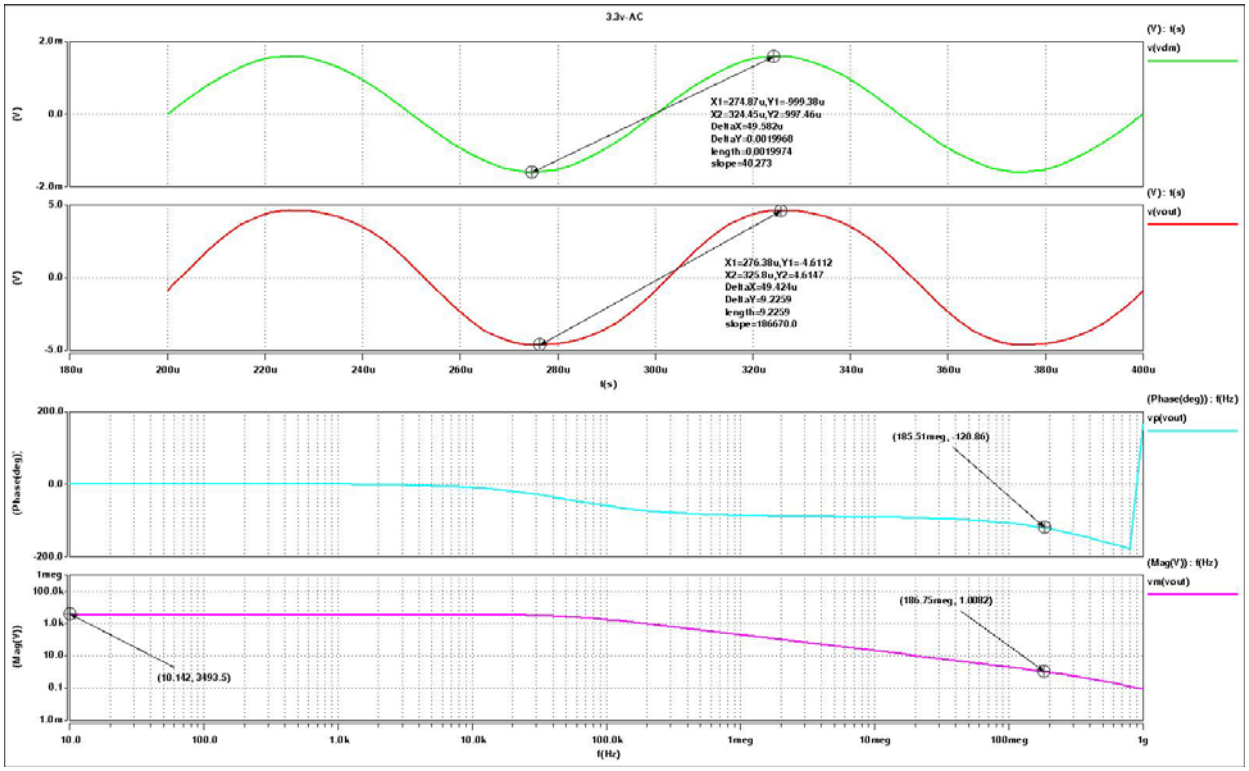

Figure 20. AC analysis-power supply ±3.3V Cl=1.5p,clock frequency=625Khz,Fs=5mhz

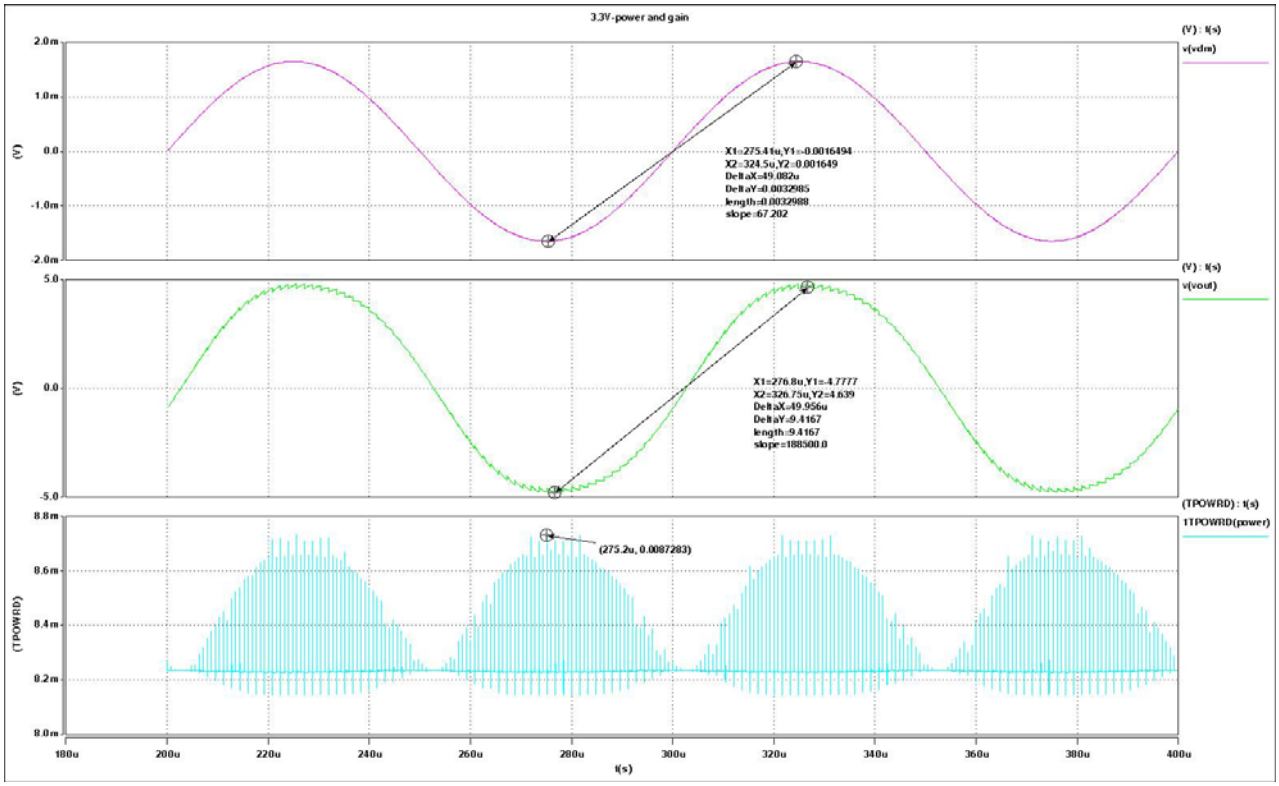

Figure 21. Gain and Power-power supply ±3.3V Cl=1.5p,clock frequency=625Khz,Fs=5mhz

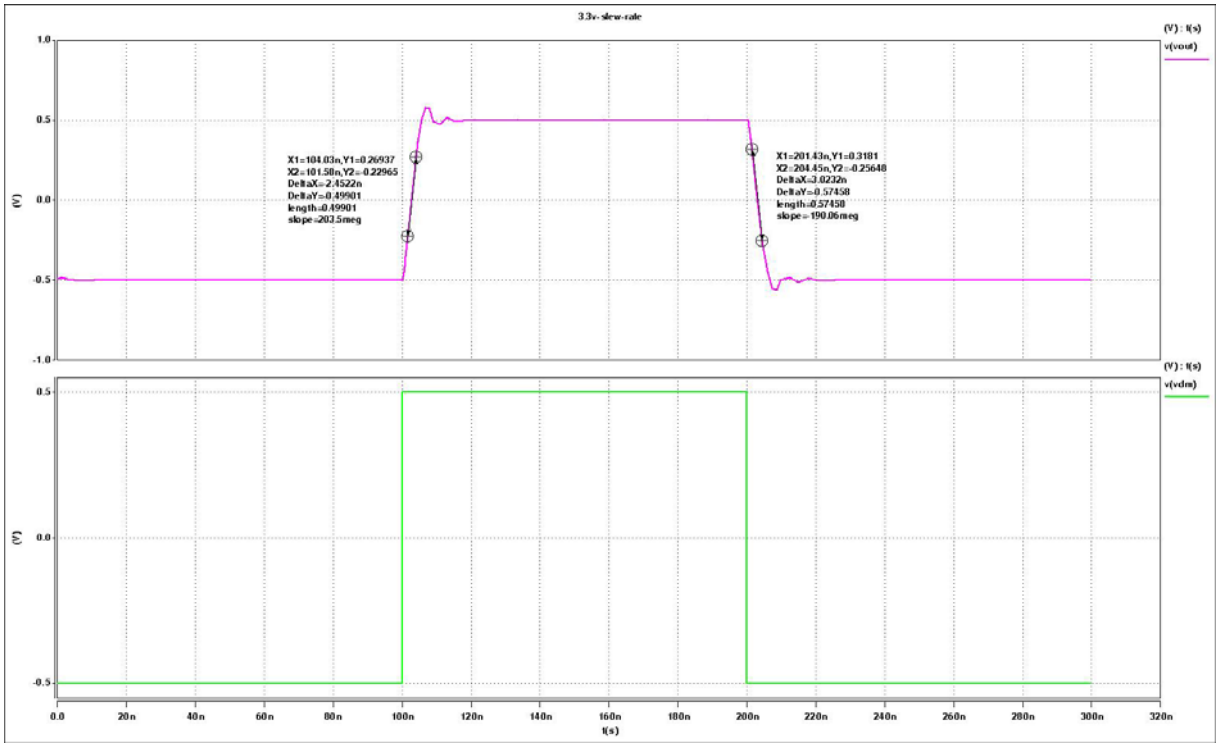

Figure 22. Slew rate-power supply ±3.3V Cl=1.5p,clock frequency=625Khz,Fs=5mhz

Compare table 5 with table1, increasing the rail voltage, the slew rate and phase margin are increased, respectively, and power dissipation is improved significantly. Higher supply voltage can provide higher current. From figure 23, we can see that when rail voltages are ±2.5V, the bias current is 113uA , and ±3.3V rail voltages can drive bias current about 133uA.

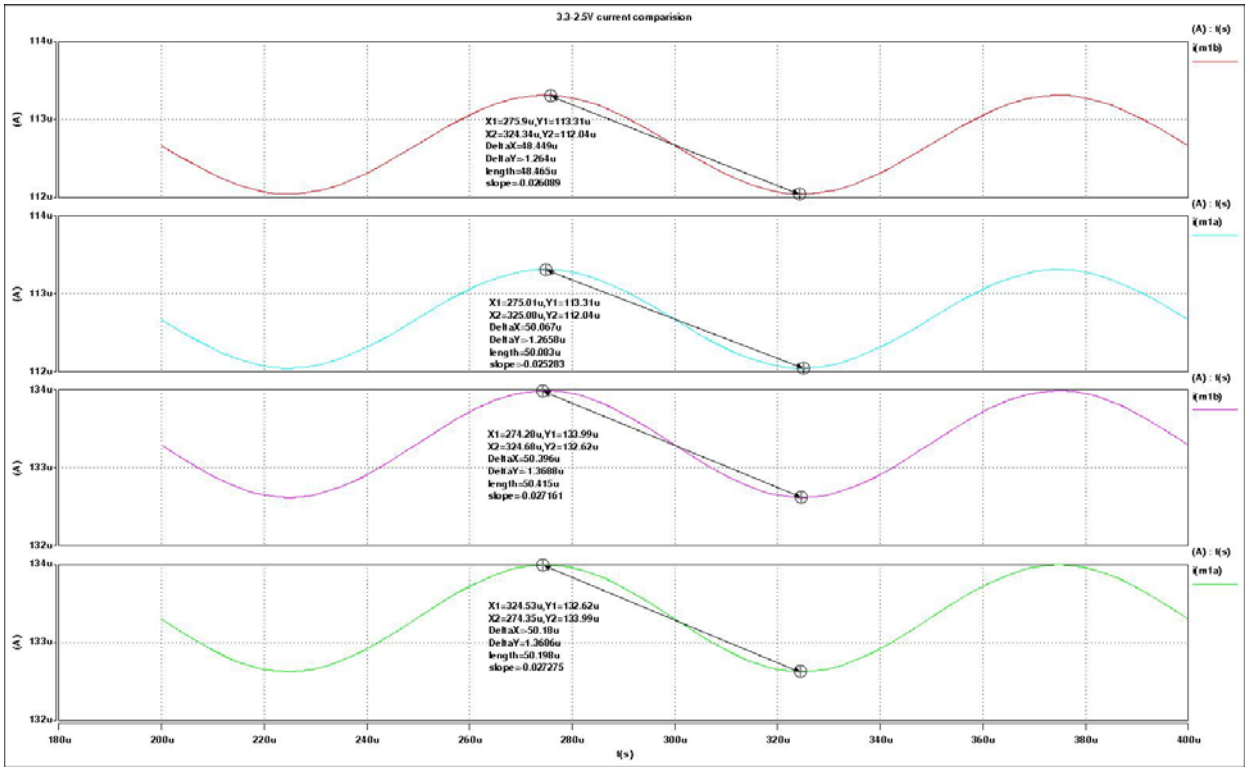

Figure 23. Current comparison for power supply ±2.5V and ±3.3V

For improving the phase margin, reducing the size of input pair transistors is a most effective way, however, we are worry about reducing sizes will amplifier input thermal noise, but from the simulation results, we find that if double the size of input pair, reduction of input noise is not obvious. That is because the equivalent input noise of input pair transistor is $4KT(2/3)(1/g_m)$, increase width of transistor =increase gm, then reduce the noise, but when gm is quite large, the noise bring from the input pair transistors is very small and can not be dominant any more , the infection to the total input noise from input pair transistors is reduced too. So after synthetical analysis, the total noise can not be significantly rejected by reduction $g_{min.}$ From Figure 24, we can easily find out the answer. At 5Mhz, input noise for the (W/L)in=400/4 is 3.7n V/sqrtHz and 3.2nV/sqrtHz for the (W/L)in=800/4.

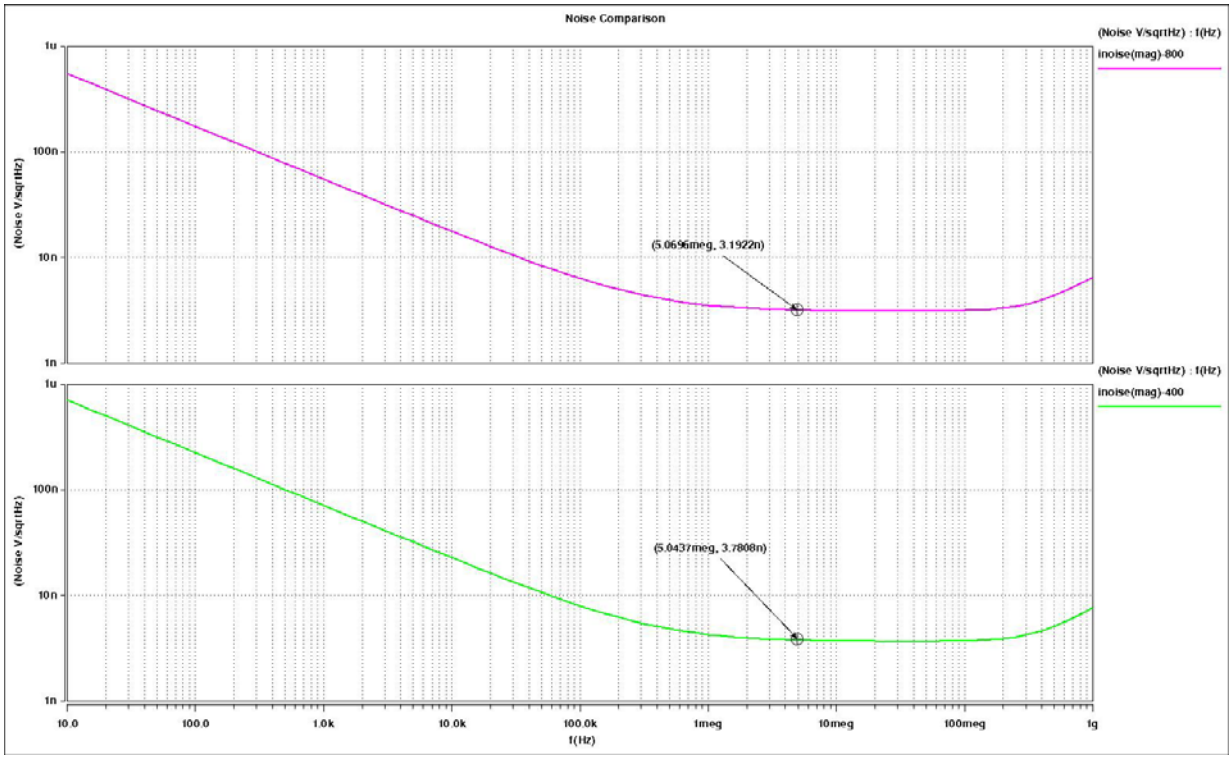

Figure 24. Noise comparison for (W/L)in=400/4 and (W/L)in=800/4

From the analysis above, we can see that there are trade-offs in the Opamp design which is always hardest part during the procedure. Good design is Good compromise among conflicting criteria

Performance Criteria and Design Guidelines

1. Higher Gain

   a.High bias current

   b.Long and wide device

   c.Cascode configuration

2. Higher Bandwidth

   a. High bias current

b. Short channels

3. Higher slew rate

a. High bias current

4. Noise

a.Large devices

b.High bias

Layout Consideration

When one designs analog circuits, several important layout issues should be considered to realize high-quality circuits, These issues can be broadly divided into two categories-noise and matching issues

Power supply noise

Invariably, when signals are routed from one place to another, noise is coupled into the wires. In mixed-signal circuits such as switched-capacitor circuits, this noise coupling problem is more prominent than in pure analog circuits.

- Fully differential architecture
- Separate analog and digital power supplies
- Add contacts on substrate (Vss) and n-well (Vdd)

Substrate Noise

To minimize the effects of substrate noise, wells and guard rings are placed around the analog and digital parts, respectively, to create isolation. This measure helps to prevent the substrate noise from propagating through the resistive substrate.

- Wells

- Guard ring

Matching Issues

The amplifier is the most important block in a ADC design. Precision matching between analog elements, such as transistors and capacitors, is typically required to maximize the effort to improve the ADC performance.

Transistors in analog circuits are usually much wider than those in digital circuits. Therefore, they are commonly laid out using multiple-gate fingers to save space and reduce series resistance in gate.

In switched-capacitor circuits, ratios of capacitors are critical because the accuracy of charge transfer relies on them. Mismatched capacitors might contribute to the failure of the whole circuit. The major error sources in capacitor fabrications are due to over-etching and the oxide-thickness gradient across the surface of the IC.

3. Future work

1) Layout this Opamp

I want to use Magic layout editor to layout it and use HSPICE to do simulation again. Using CSCOPE to observe the results.

2) Design an ADC using this Opamp

ADC as the topic of my thesis, so this Opamp which has very good performance will be used in the ADC core circuit