



Advanced 3D TCAD Simulation of Semiconductor Devices

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Introduction-TCAD

What is TCAD?

- Technology Computer Aided Design for semiconductor devices

Why TCAD?

- TCAD is critical for semiconductor device industry, both discrete and integrated
- It saves time and money, provides deep understanding of the physics

Why 3D TCAD?

- More realistic
- Device nature requires 3D (i.e. Superjunction Power Device, CIS)

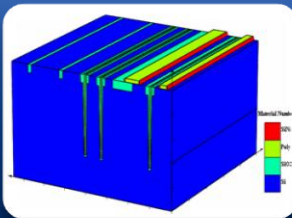
About Crosslight Software, Inc.



A Canadian company with a history of more than 15 years

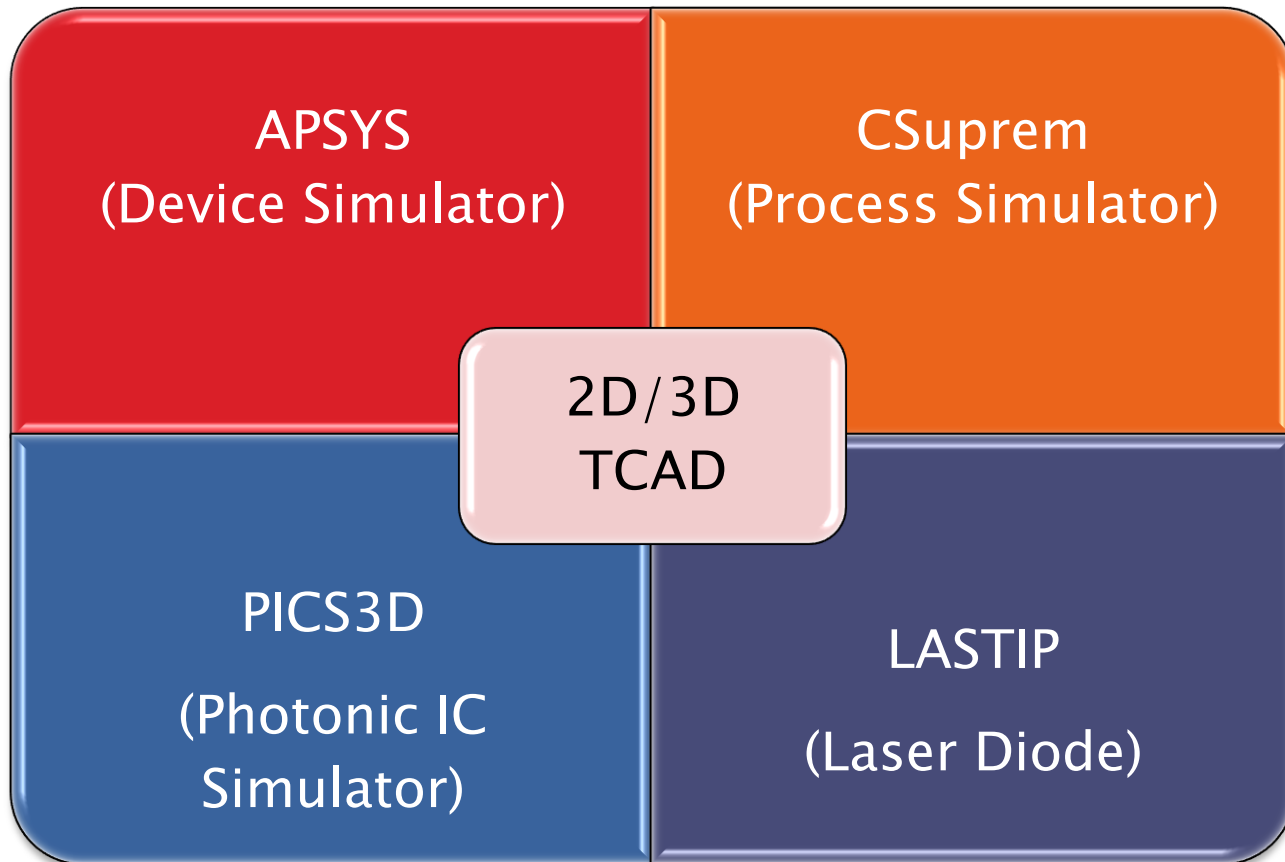


A pioneer and global leader of optics and photonics TCAD



A fast growing TCAD provider for silicon devices

Crosslight TCAD Products Family



Introduction to 3D TCAD Simulation

Time is the Money! Efficiency is the Key!

- Traditionally 3D bulk TCAD is time consuming, may take even longer than real fabrication time
- Not Acceptable for today's semiconductor industry

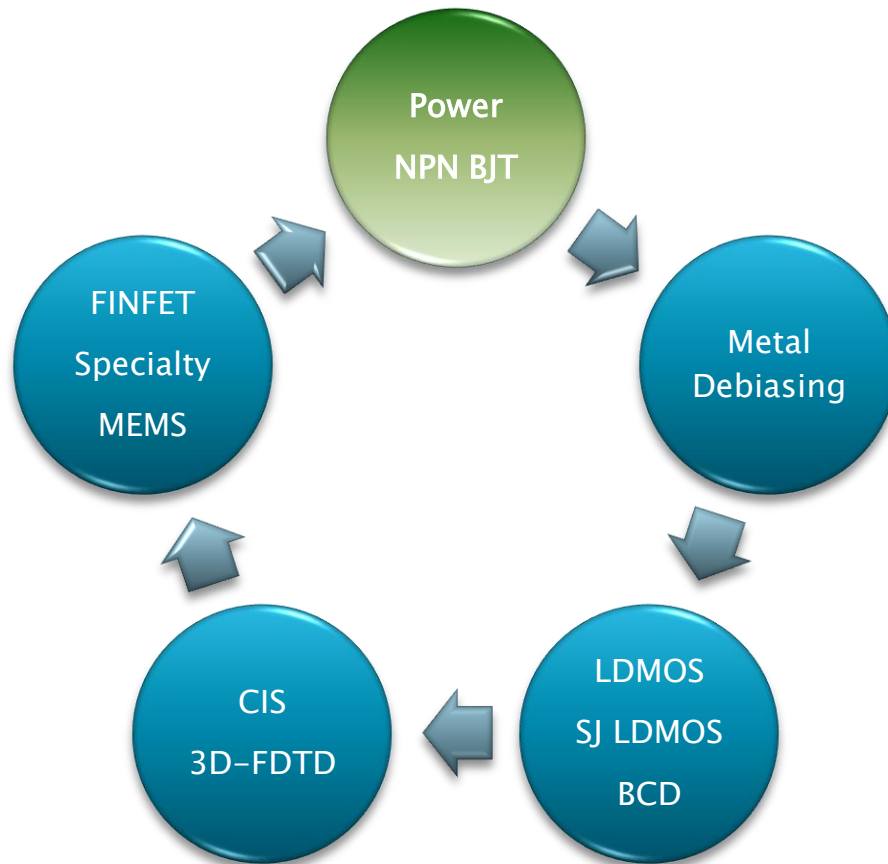
Crosslight's New Approach

- Instead of bulk simulation, Crosslight adopted a new way to stack the 2D planes in the z direction to ensure efficiency and accuracy

Quasi-3D vs. Full 3D

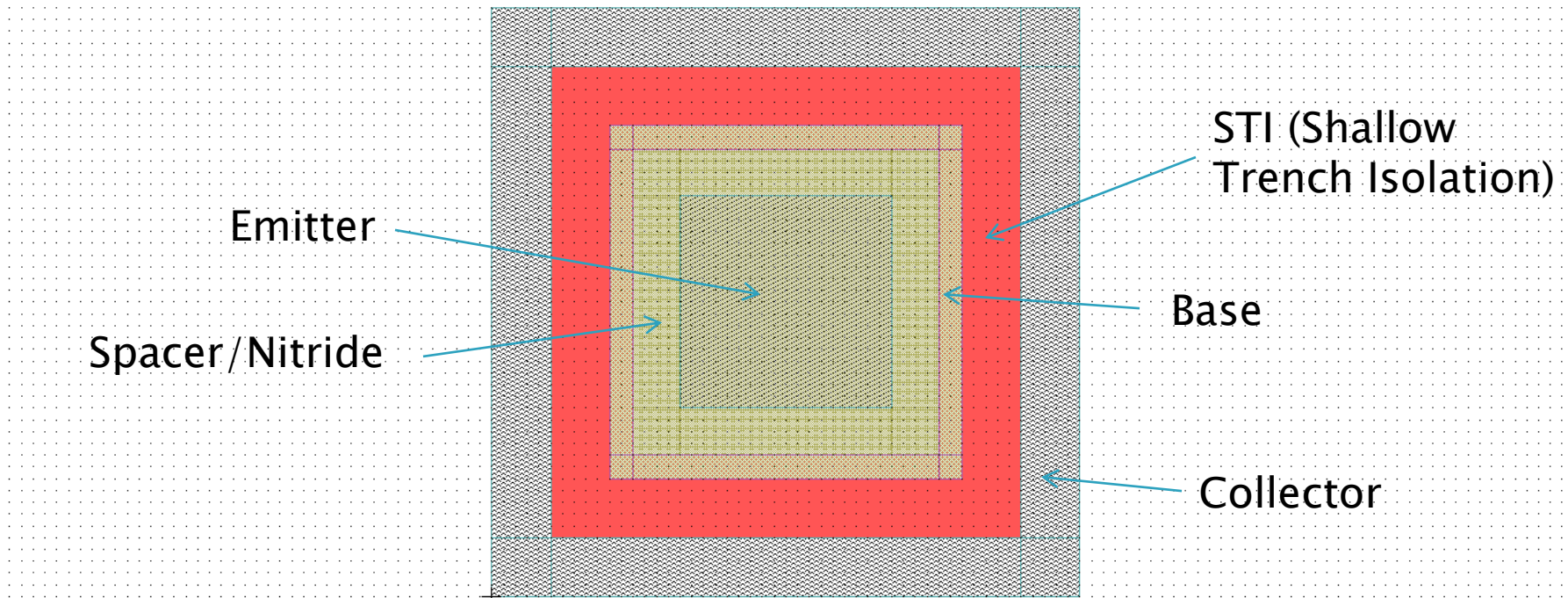
- Quasi-3D neglects the inter-plane dopant diffusion to save time at first, when everything is ok, full 3D will take account all the plane to plane interaction

Examples List: (With a special focus on Power Semiconductor Devices)



3D Simulation Process Build Up

- ▶ We use a vertical power NPN BJT as an example. From layout, generate the GDSII file



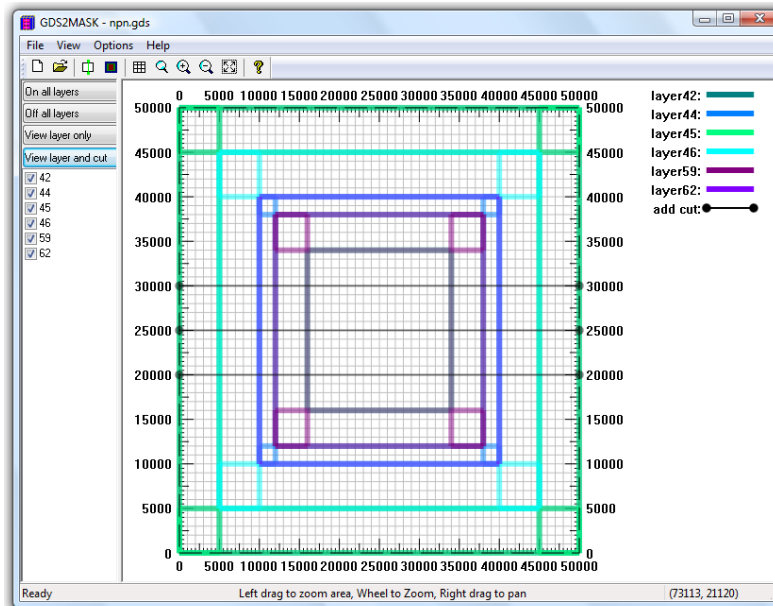
BEOL is neglected for simplicity

3D Build Up: Step 2

Z Direc. Cut(.cut file)



GDS2MASK.exe



1

• Load the GDSII file

2

• Cut the layout in the z direction

3

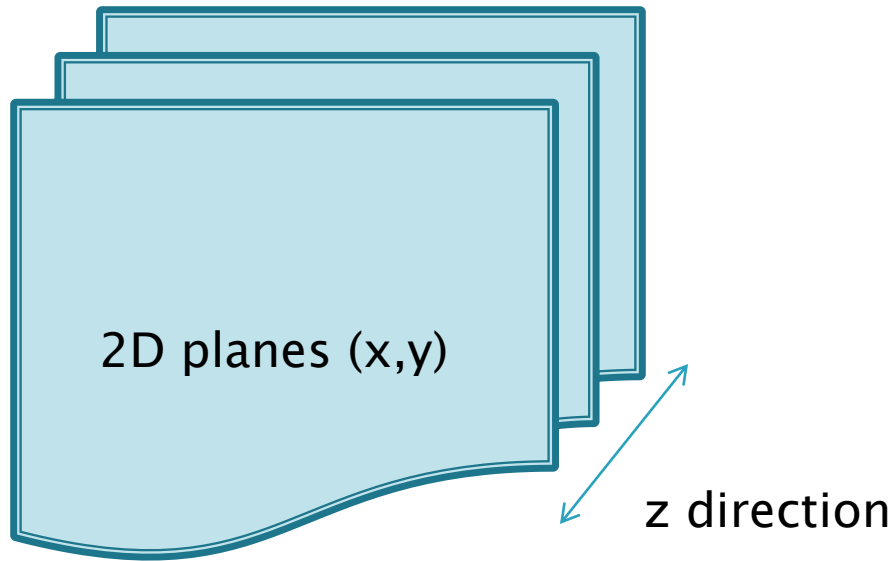
• The .msk and .zst files are automatically generated

Mask Layers (.msk file)

Z structure (.zst file)

Crosslight provides an integrated 3D structure creation tool to simplify the 3D modeling process.

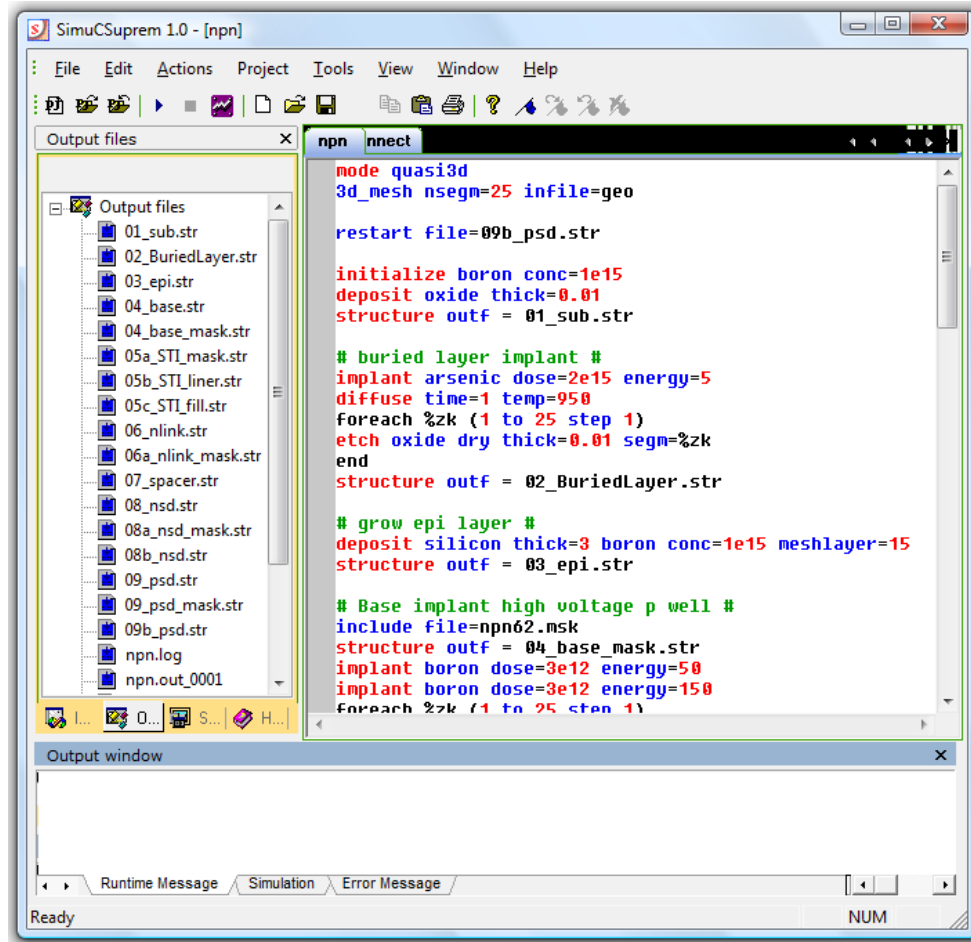
3D Build Up: Step 2 (continued)



The z structure file (.zst file) is used to control the cut location and planes in the z direction

The mask file (.msk file) is used to generate mask layers in the input file for CSuprem

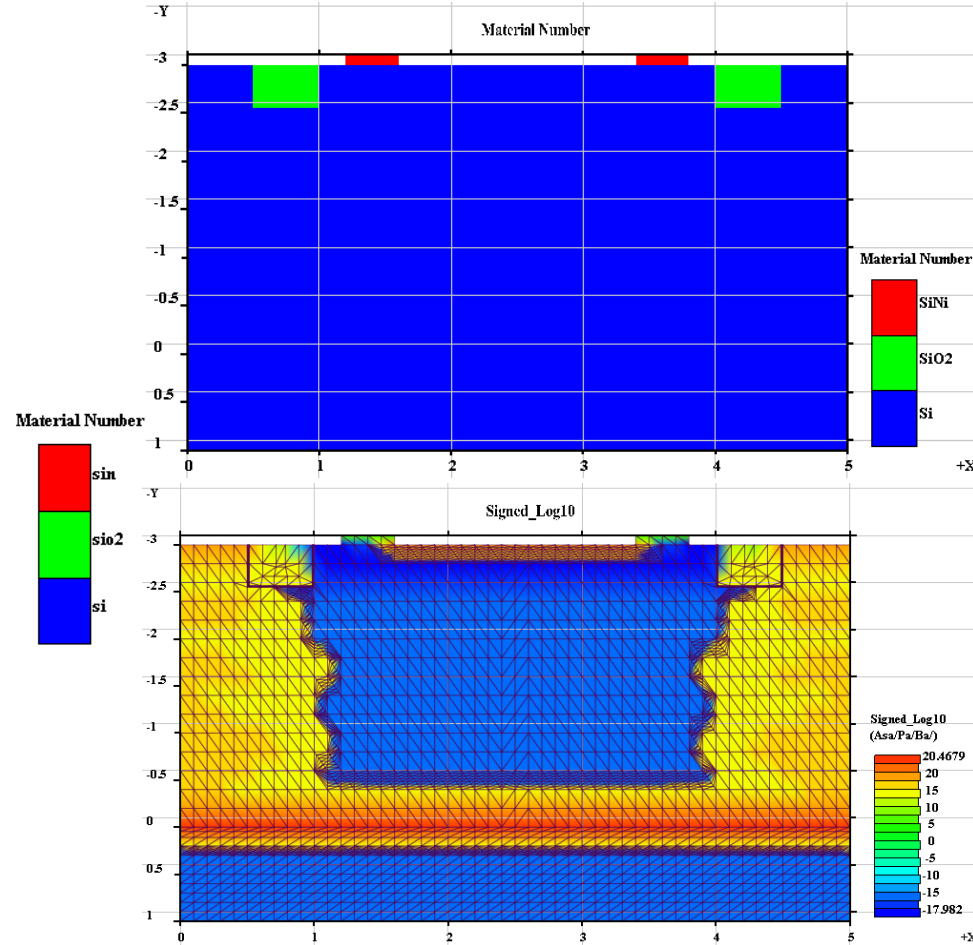
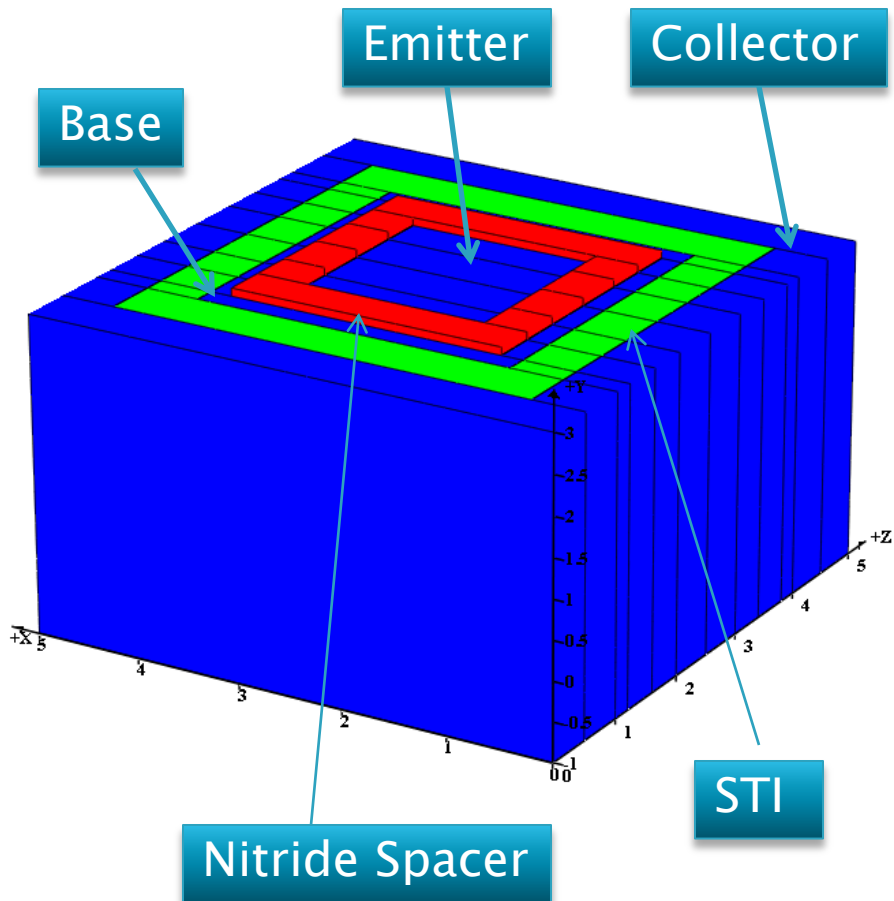
Step 3: Virtual Fabrication using CSuprem



CSuprem is Crosslight's version of SUPREM IV, originally developed by the Stanford University.

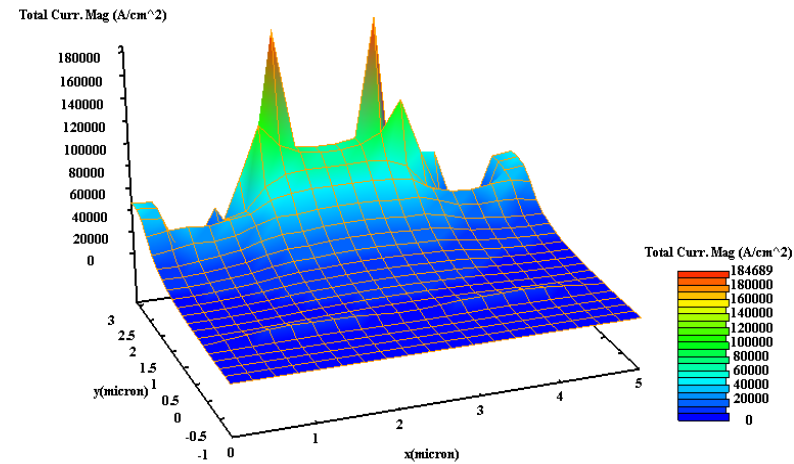
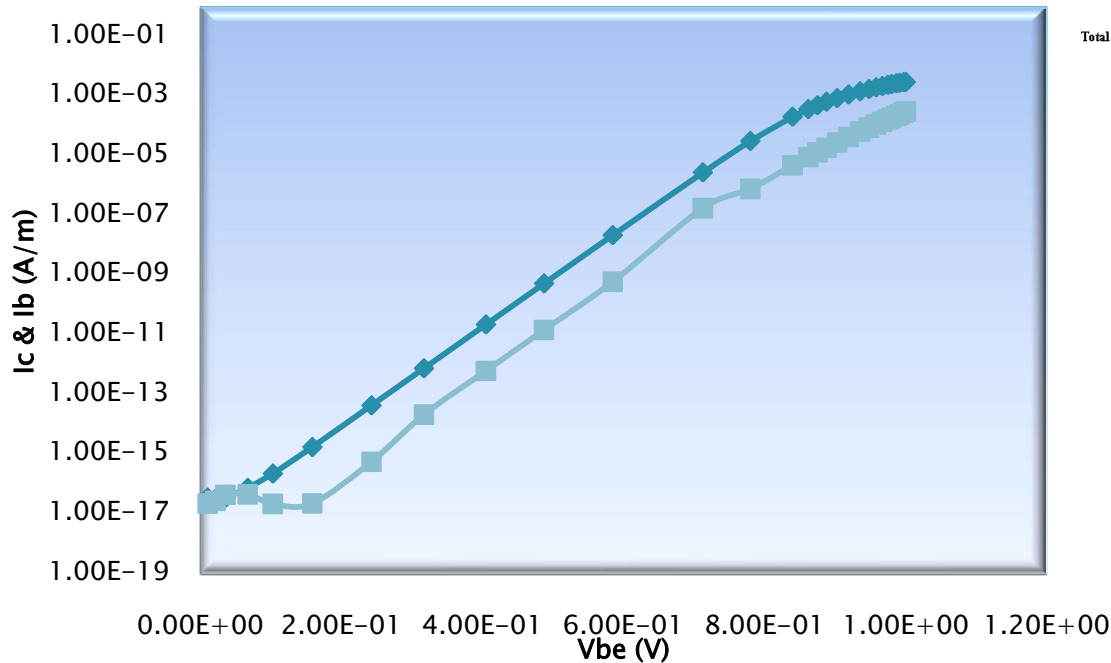
You can choose from quasi 3 dimensional or full 3D simulation, quasi3d means the diffusion between the z planes is not considered to boost up speed

3D NPN BJT Process Simulation



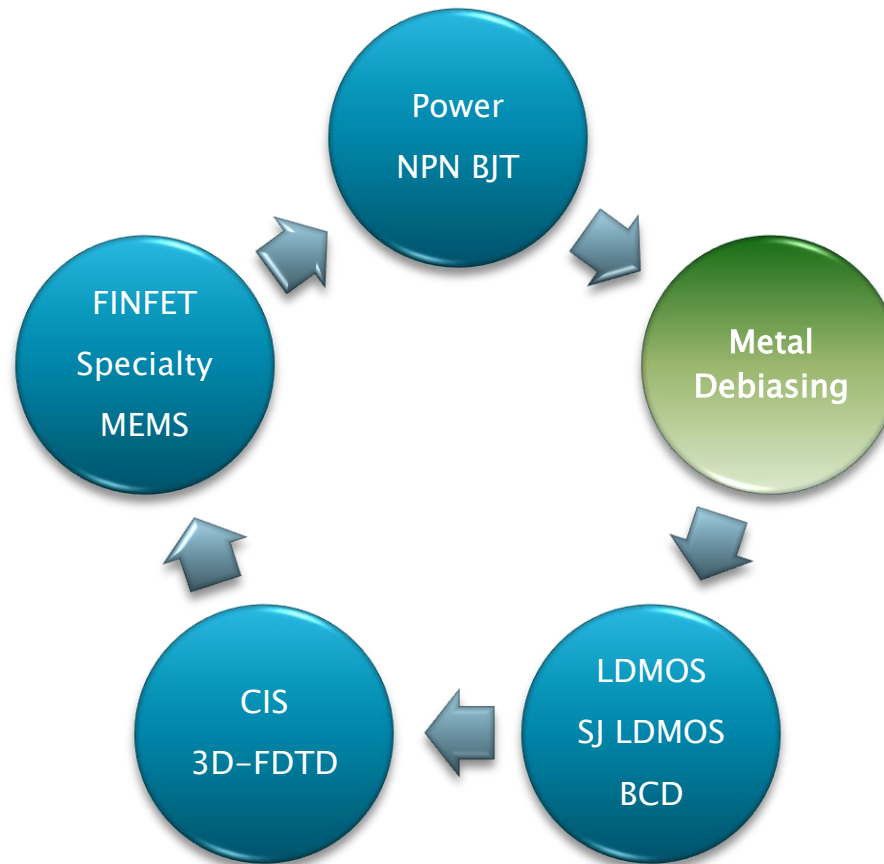
Device Simulation Result of 3D NPN BJT

Gummel Plot



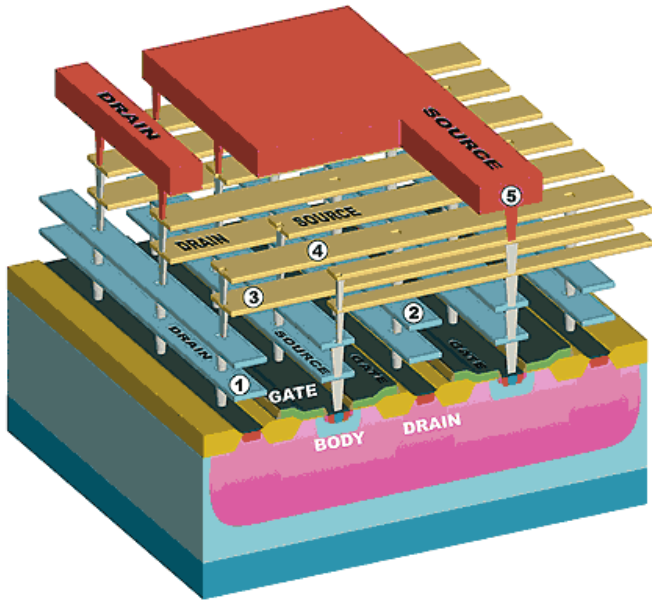
2D center cut: Total
(electron and hole)
Current Contour Plot

Examples List:



Interconnect Metal Debiassing :

A well known problem for the Power IC Industry



The BCD6 high-voltage LDMOS FET uses five interdigitated aluminum/copper metal levels. While the first four layers contact the drain and source fingers, the fifth level carries the current to the pads. Replacing the fifth layer, which is 3 μm thick, with a 5- μm copper layer improved the metal contribution to the on-resistance of the power LDMOS by 60%.

LDMOS from ST

Huge Size! Metal Resistant is no longer negligible

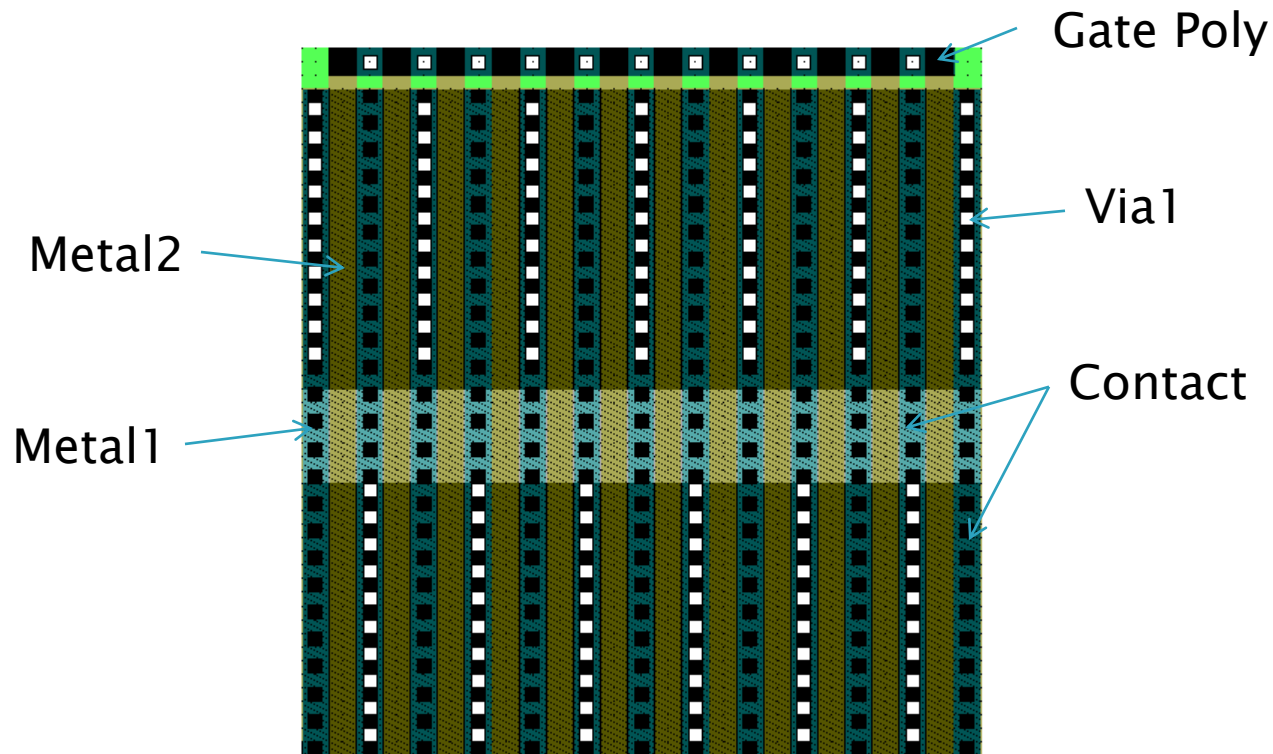
- Metal resistant comparable to device R_{dson}
- Different metal pattern will yield different Res.

Lump model is not good

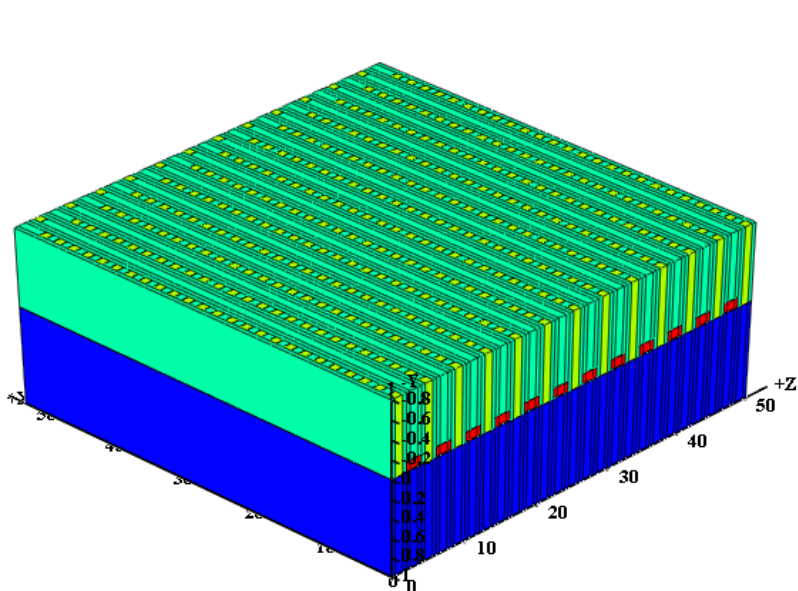
- 3D nature, too complicated to model using lump elements.

Layout of Metal Interconnect

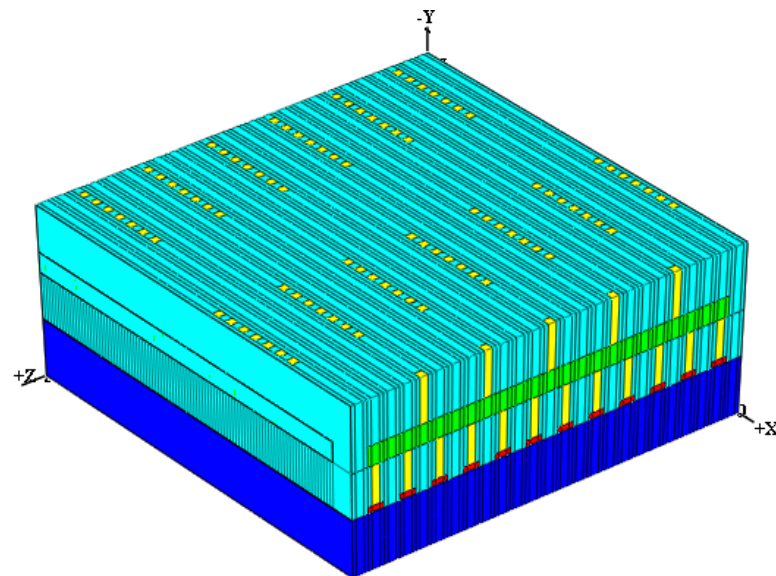
- ▶ The metal interconnect for large sized power MOSFET generally contribute to considerable amount of total resistance, a 3D model is generally necessary to determine the resistance from the metal lines.
- ▶ Layout:



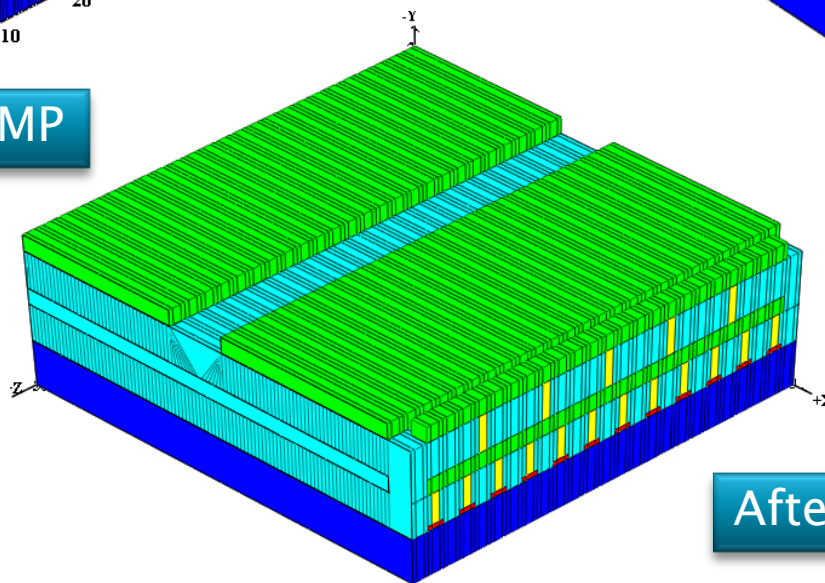
Process Simulation of Metal Interconnect



After Contacts CMP

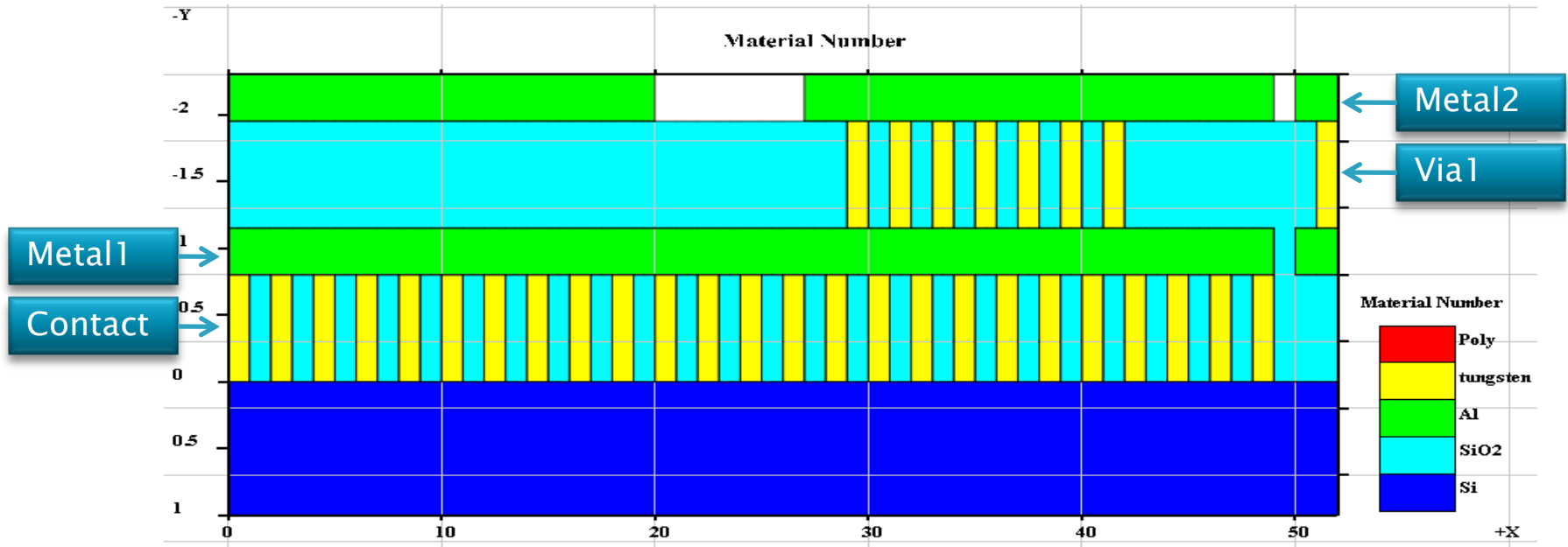


After Via1 CMP

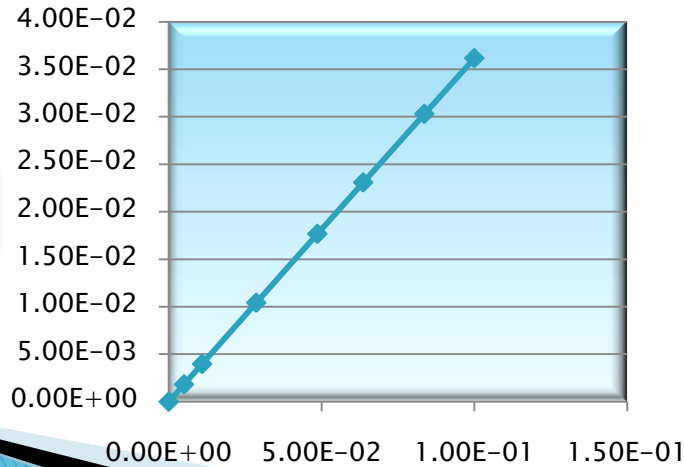


After Metal2 CMP

2D Cut and Device Simulation

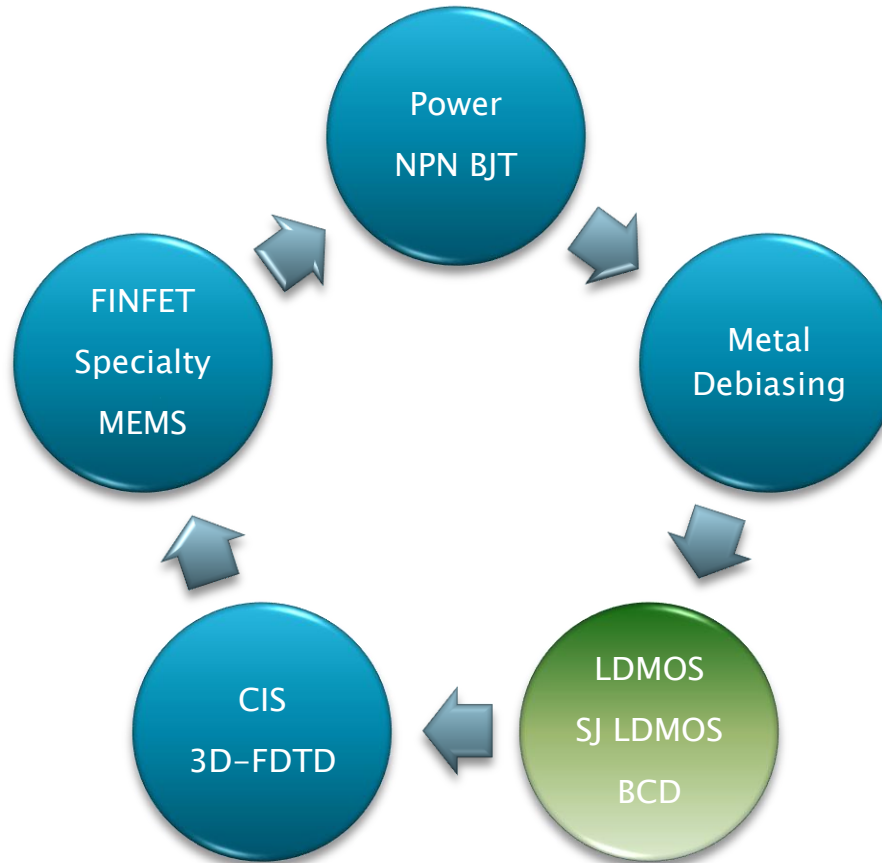


I-V Curve

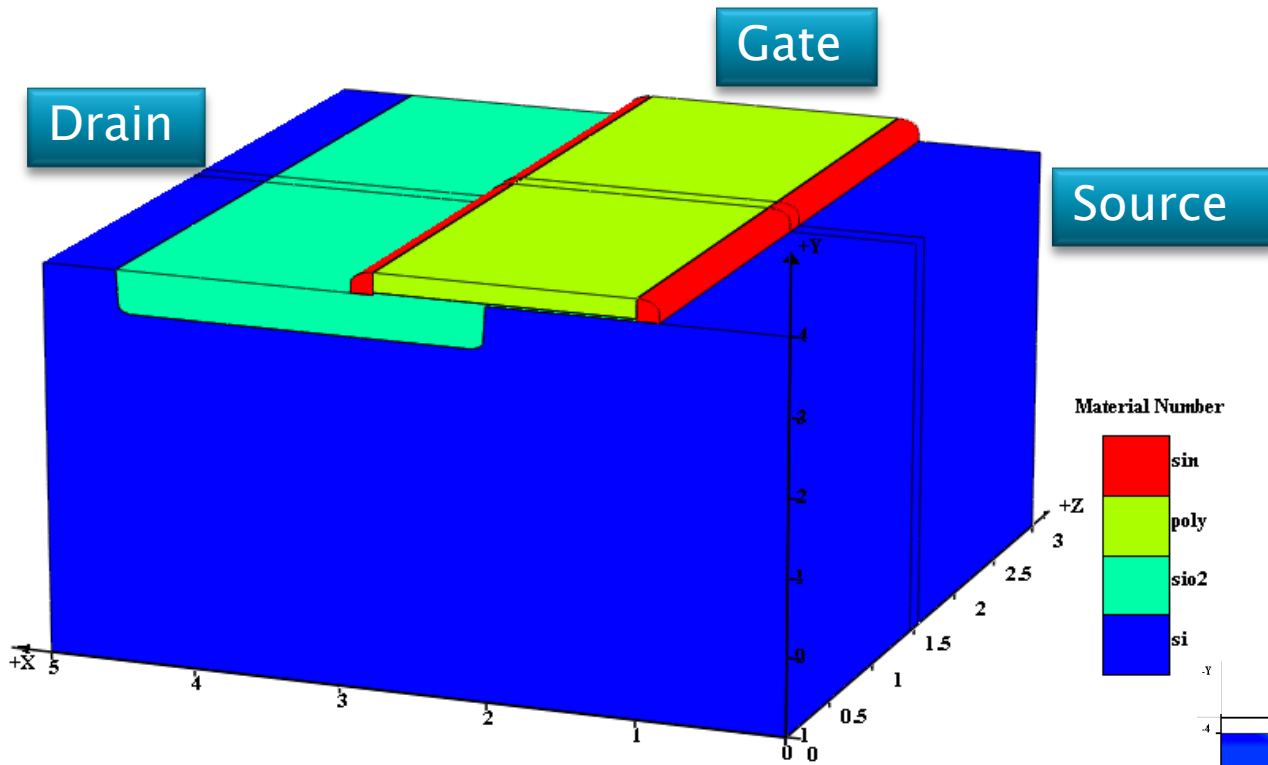


2D cut from center

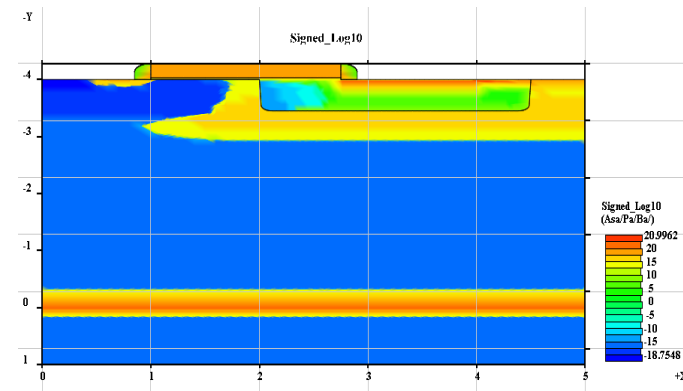
Examples List:



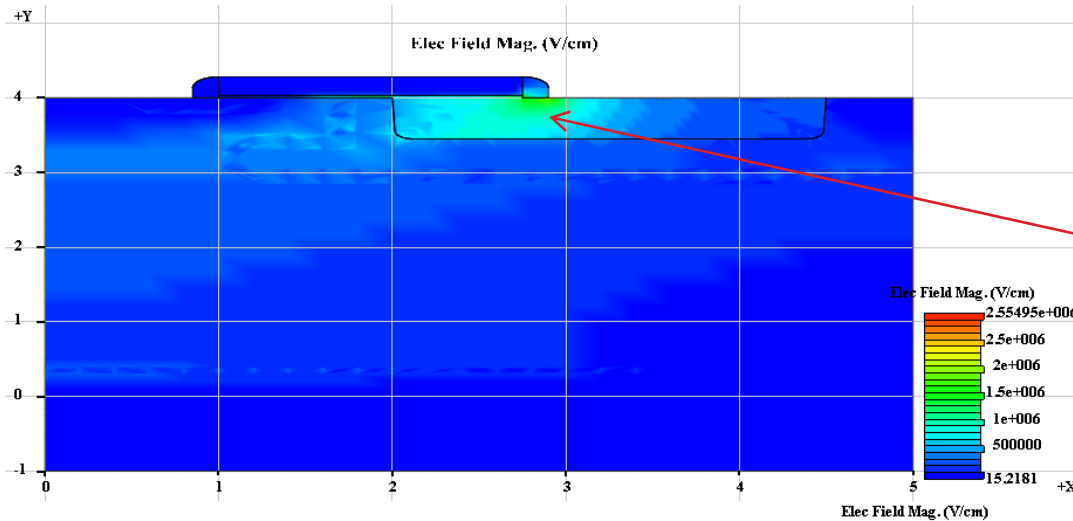
Power LDMOS Process Simulation



2D cut:
Net Doping

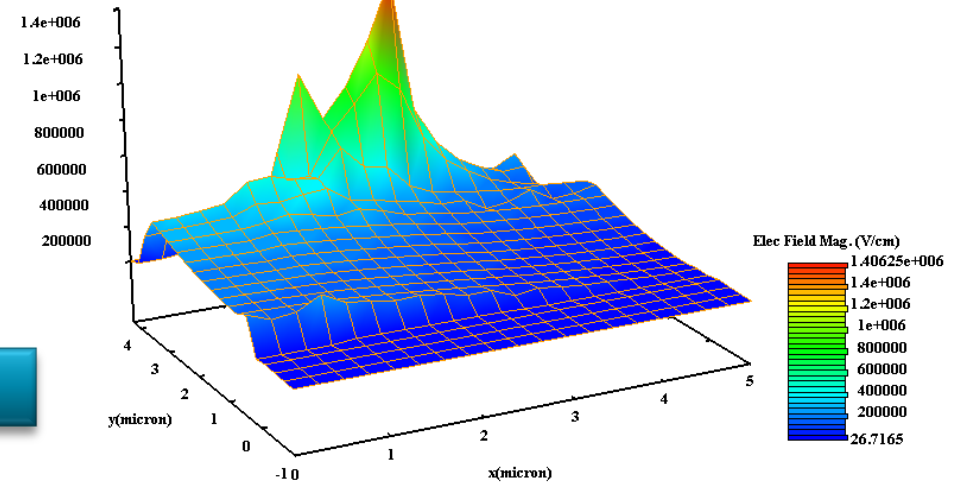


Power LDMOS Device Simulation



Highest Electric Field is located under gate edge in the STI, other areas are pretty flat

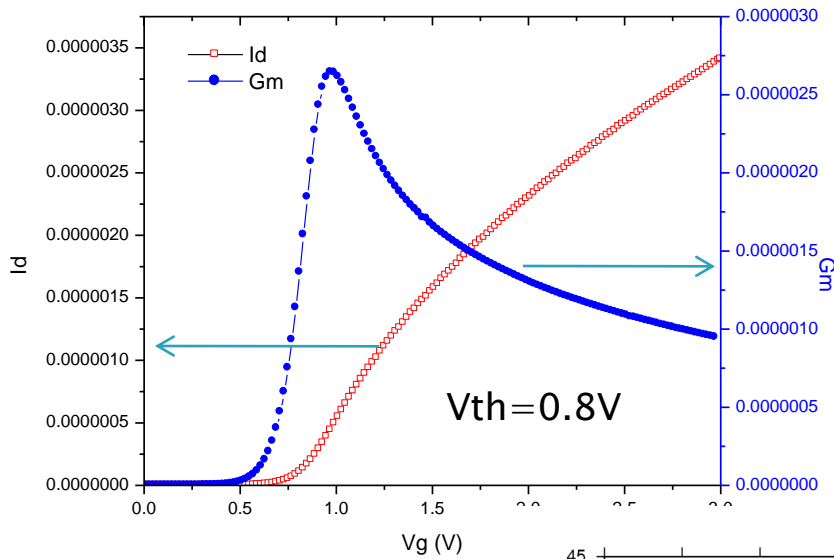
2D cut: Electric Field



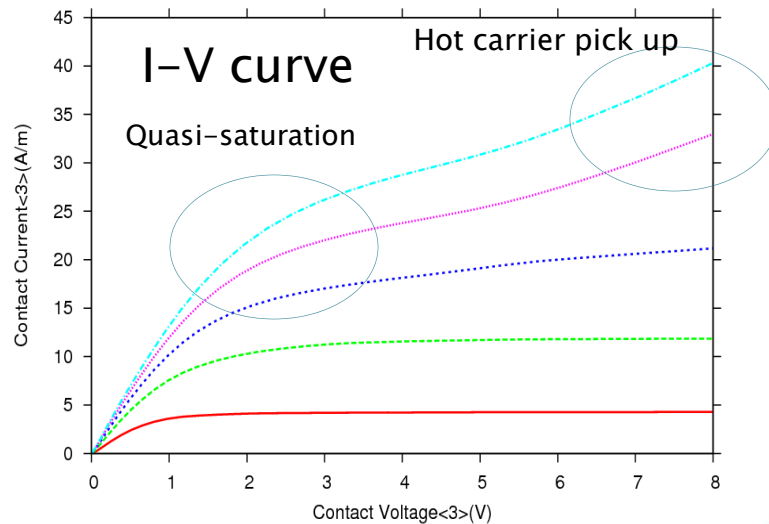
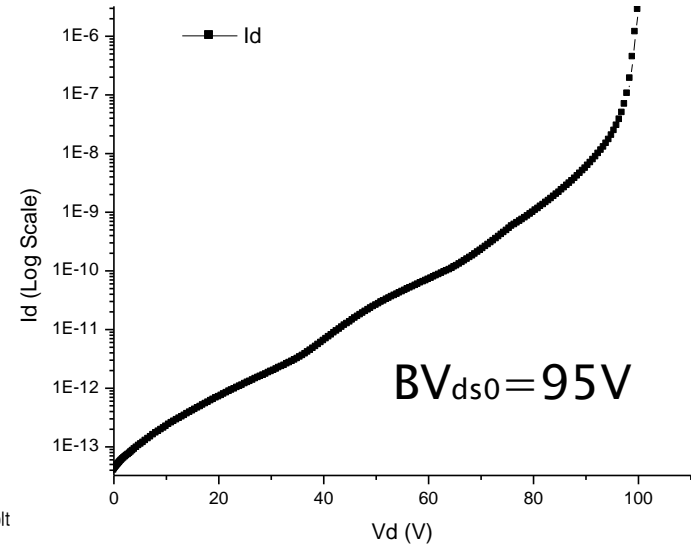
Contour Plot of E. Field

3D Device Simulation of Power LDMOS

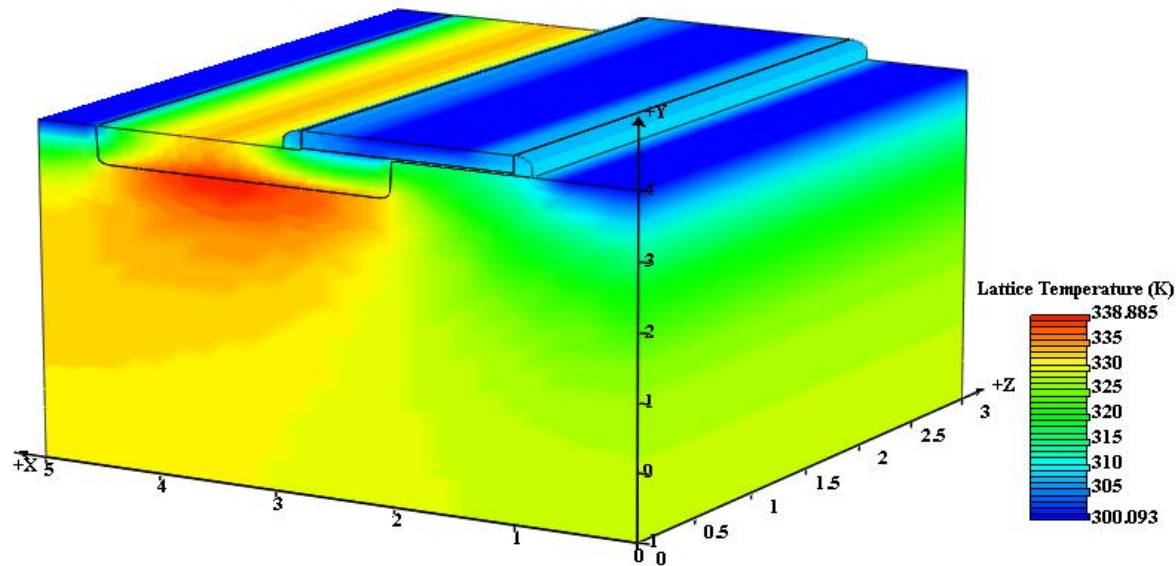
Threshold and Transconductance



Reverse Breakdown



Device Self-Heating and Thermal Simulation

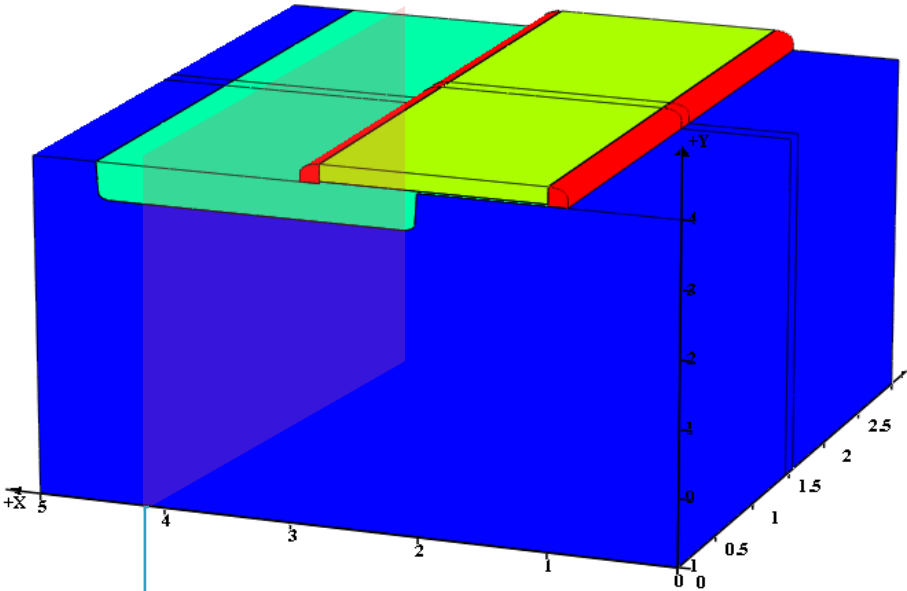


$V_g = 12V$

$V_d = 55V$

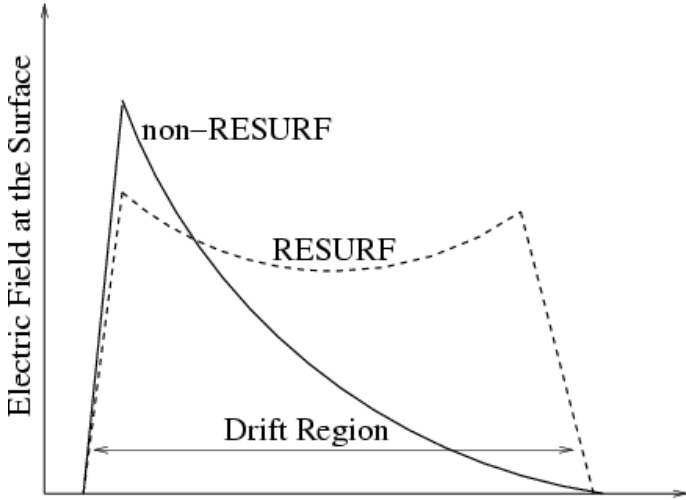
Self Heating with thermal conductance of 0.1 W/mK

3D Superjunction LDMOS Process Simulation

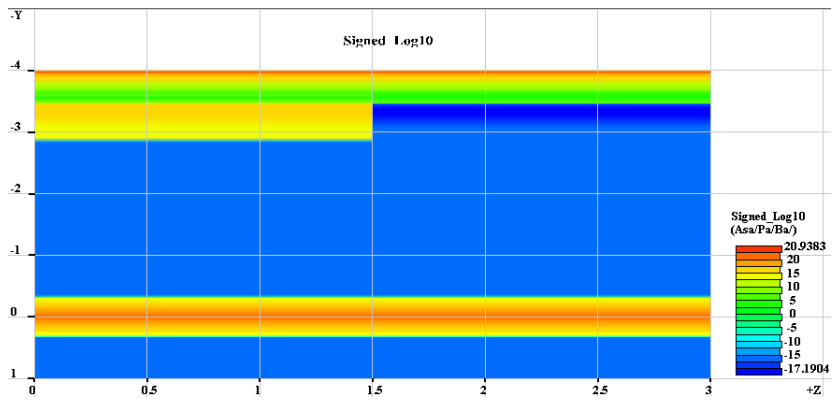


Material Number

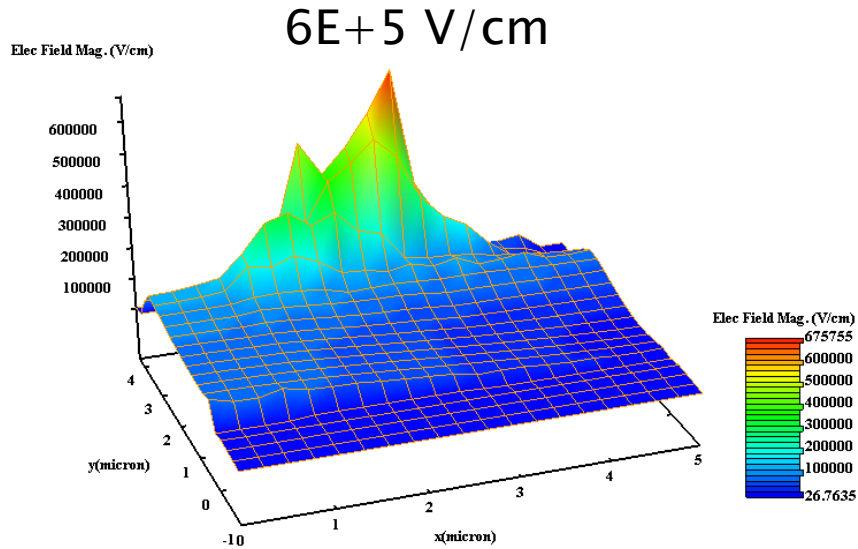
1	sin
2	poly
3	sio2
4	si



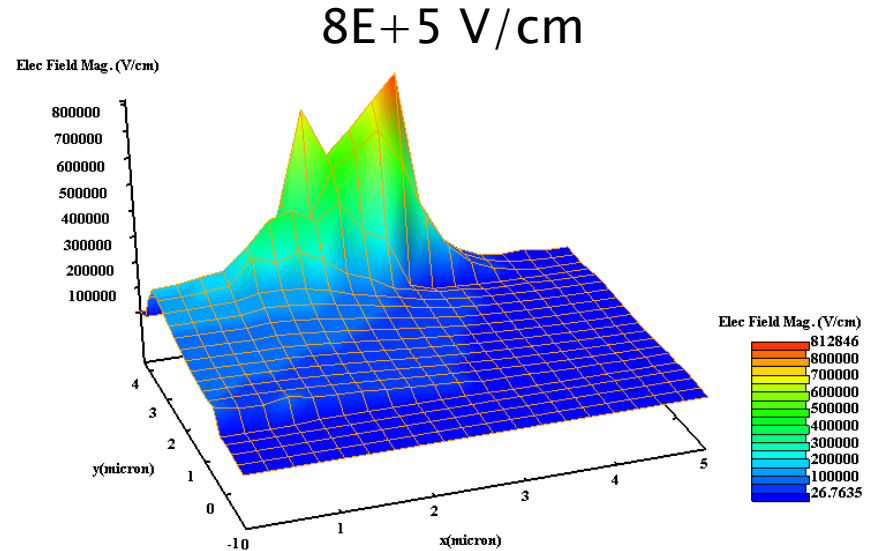
2D cut to Show Net Doping



Comparison of Surface Electric-field



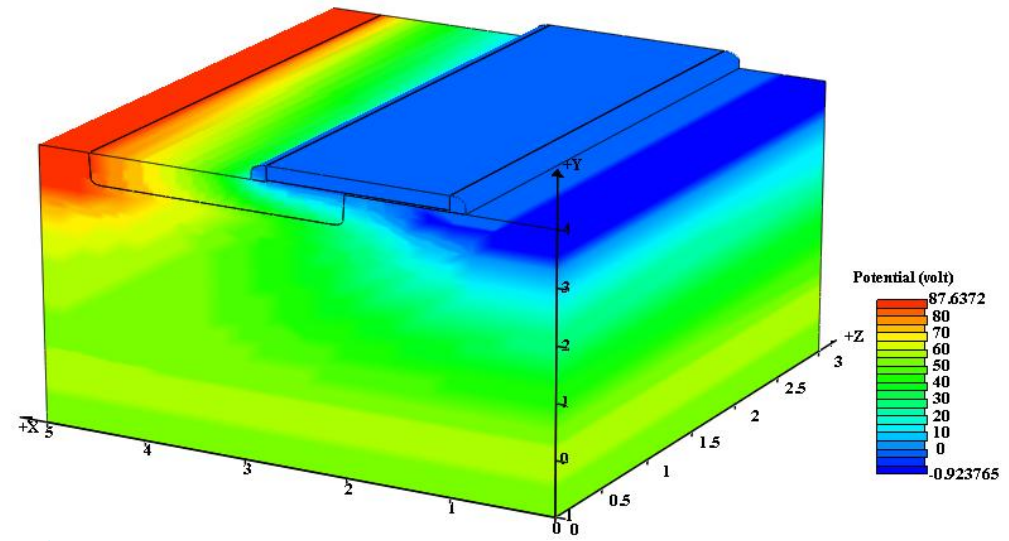
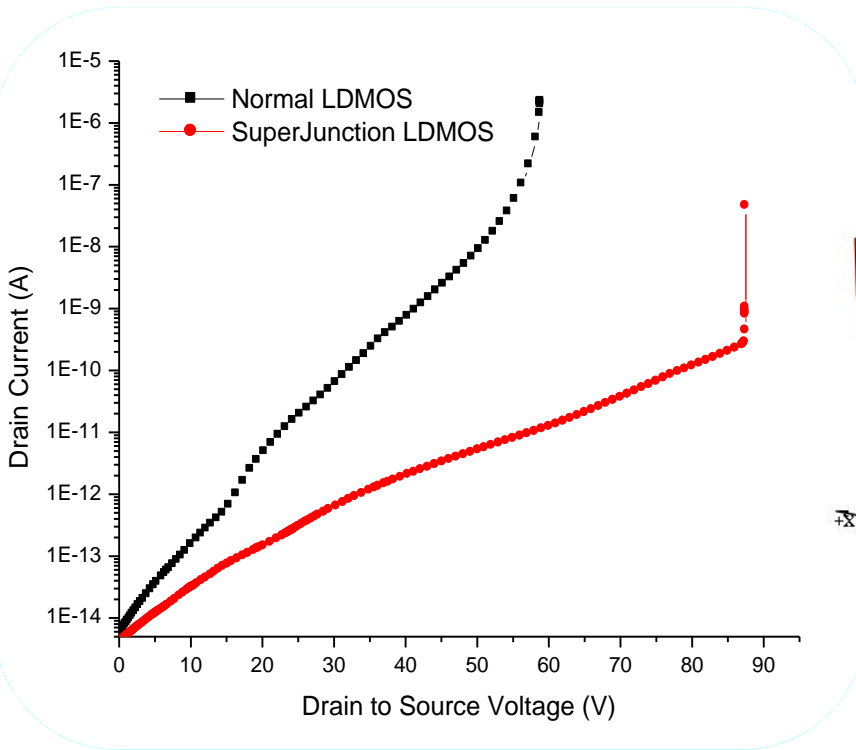
SuperJunction LDMOS



Normal LDMOS

Superjunction has lower Surface field than normal LDMOS with the same drain bias.

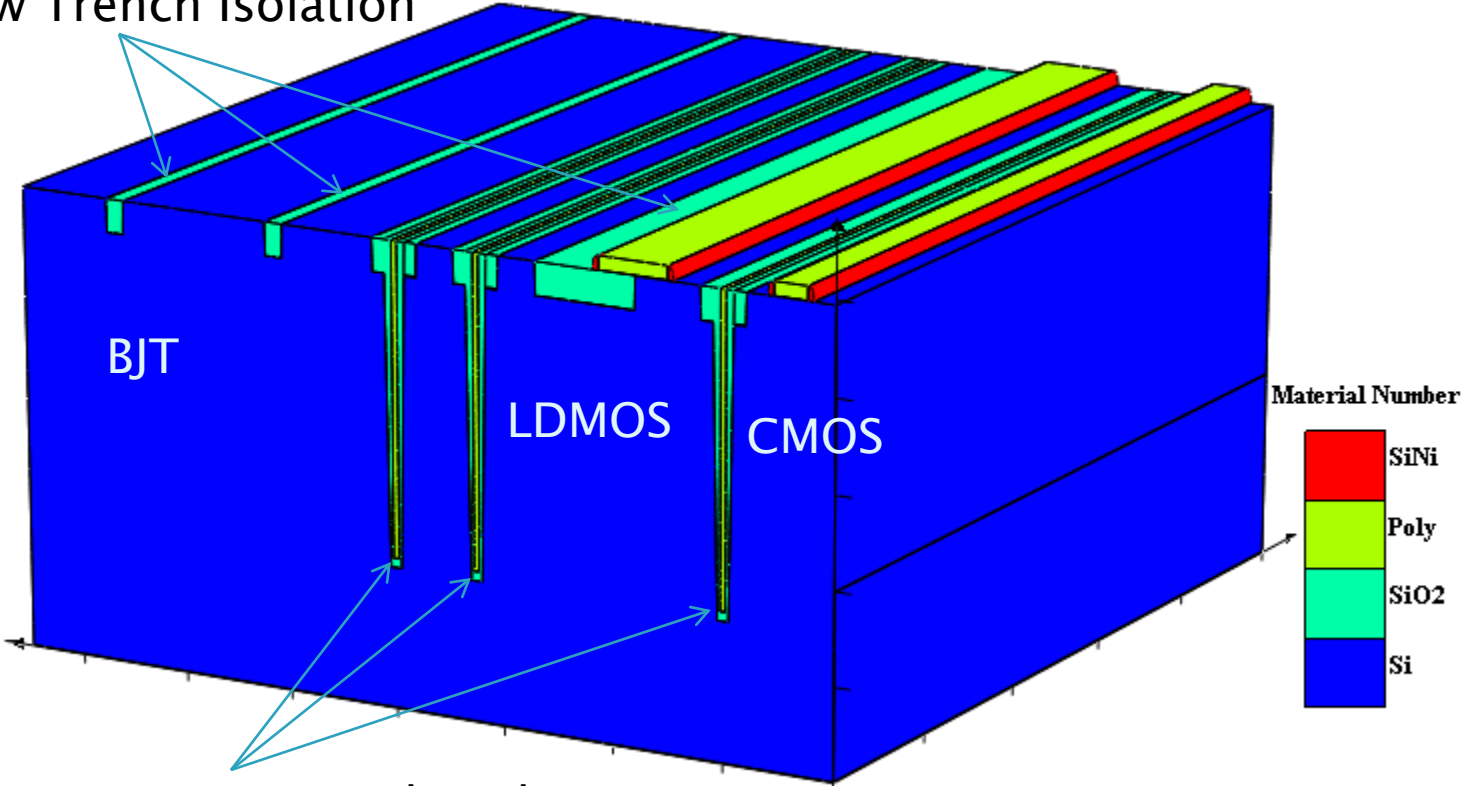
Breakdown Voltage Comparison



Comparison of Breakdown Voltage of SuperJunction LDMOS and normal LDMOS, a clear breakdown voltage increase for Superjunction LDMOS with the same process condition.

BCD Technology Process Simulation

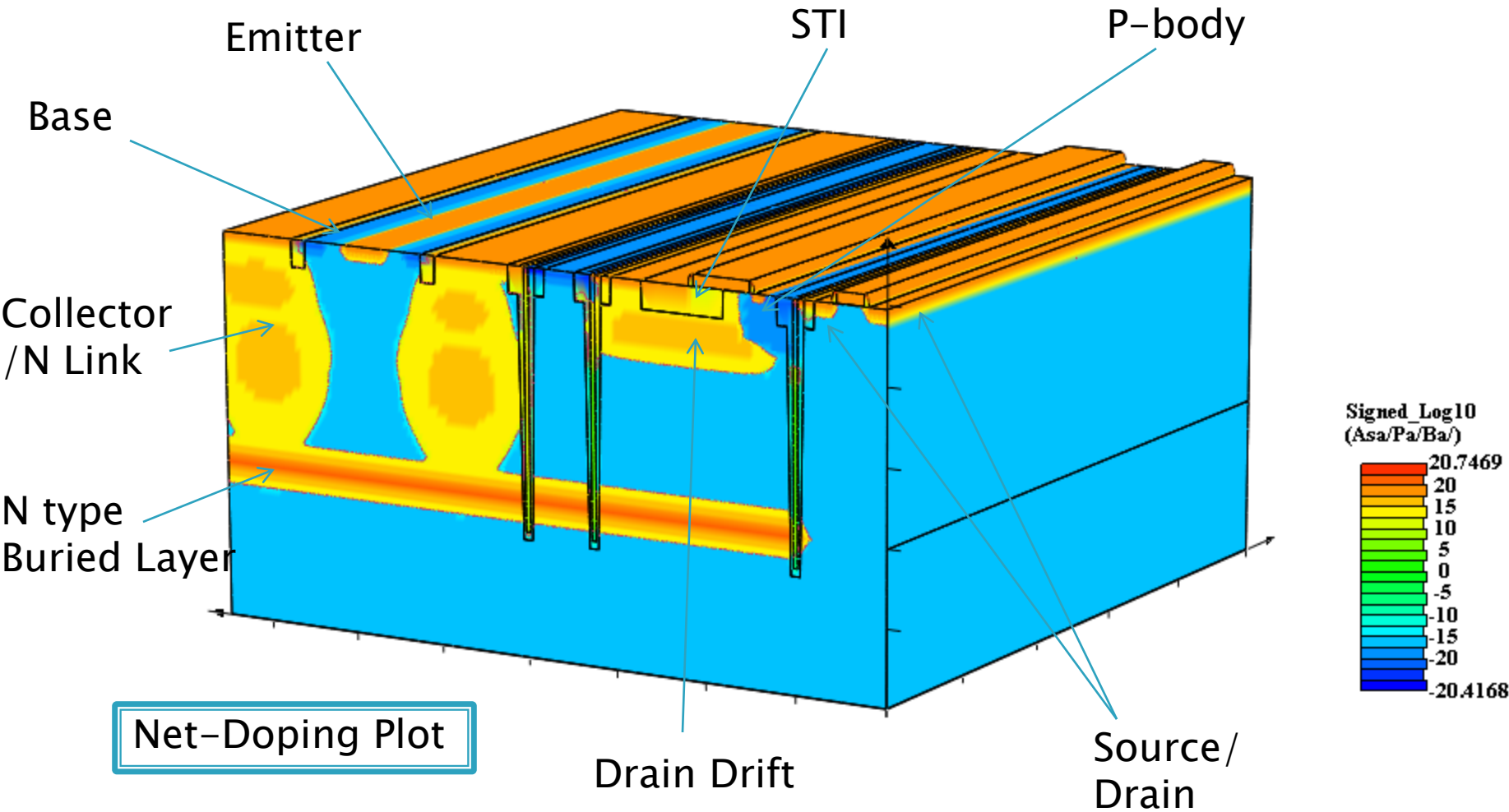
Shallow Trench Isolation



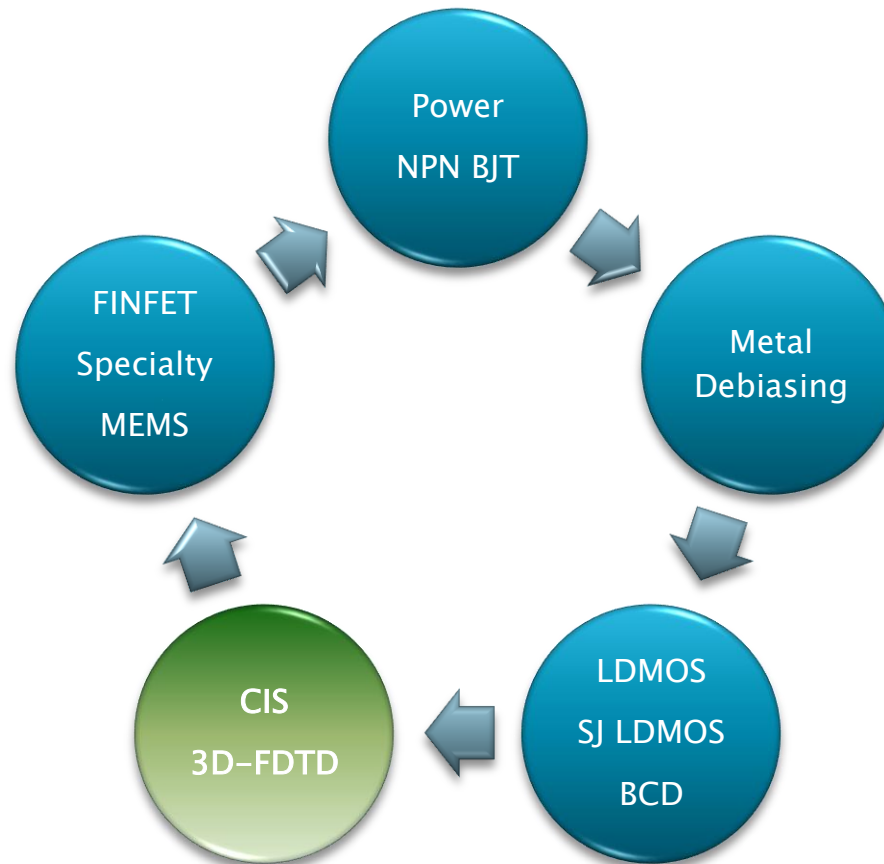
Deep Trench Isolation

BCD Stands for Bipolar-CMOS-DMOS Process

BCD Technology Process Simulation

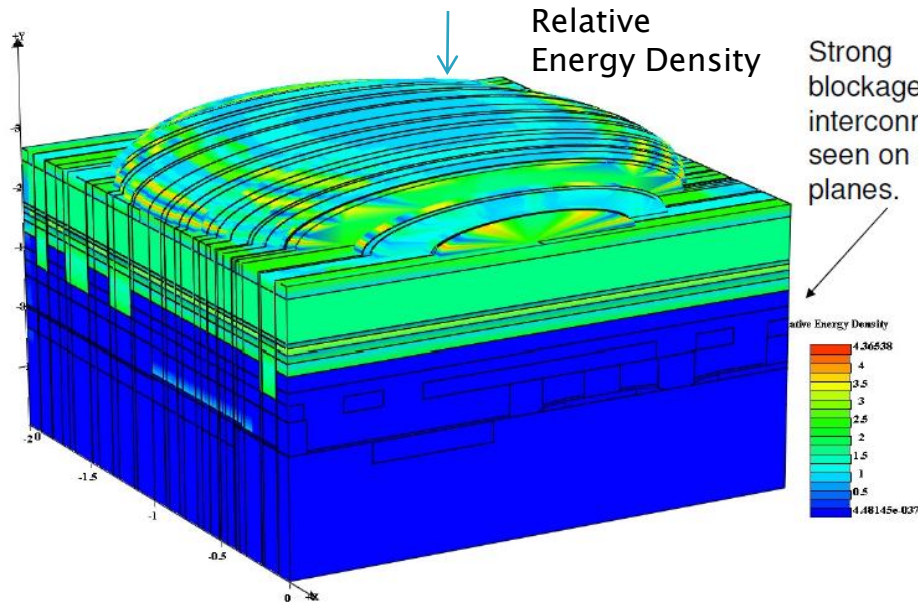


Examples List:



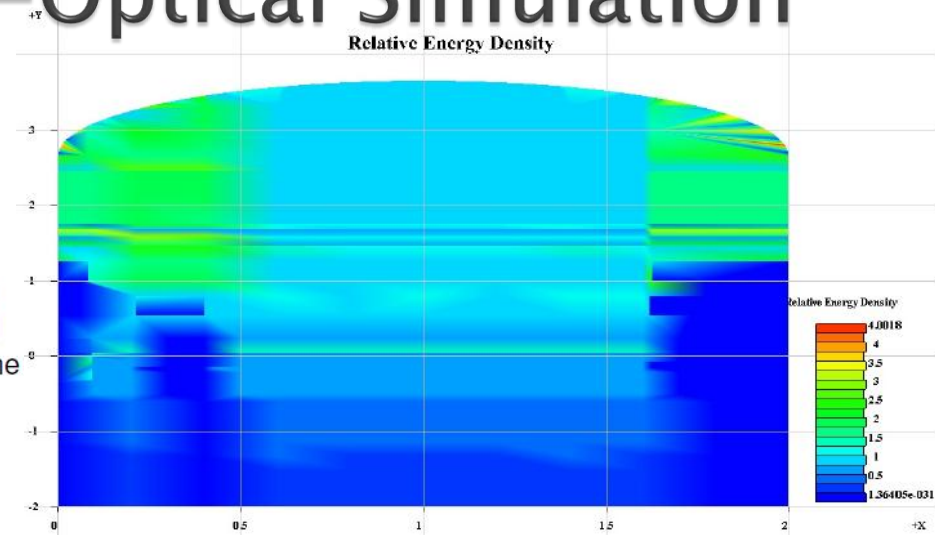
CMOS Image Sensor–Optical Simulation

Optical Simulation
3D–FDTD

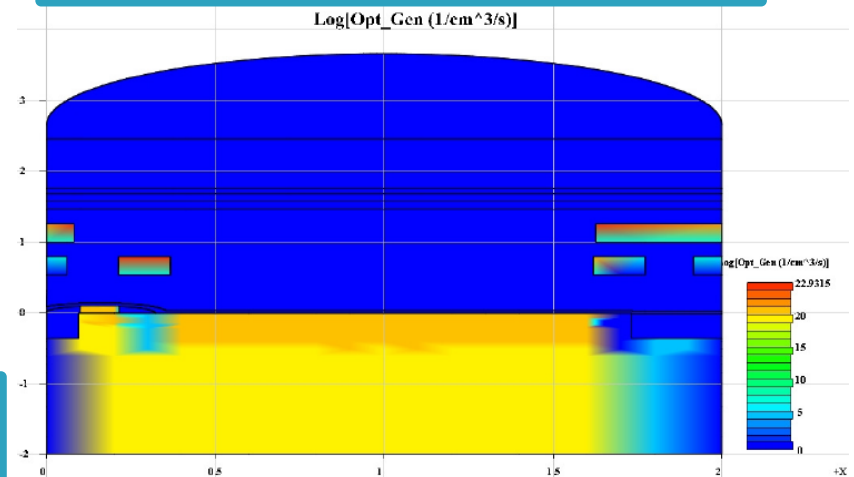


Finite-difference time-domain (FDTD) is a computational electrodynamics modeling technique, dealing with electromagnetic wave interactions with material structures.

2D–Cut of the
Optical Generation

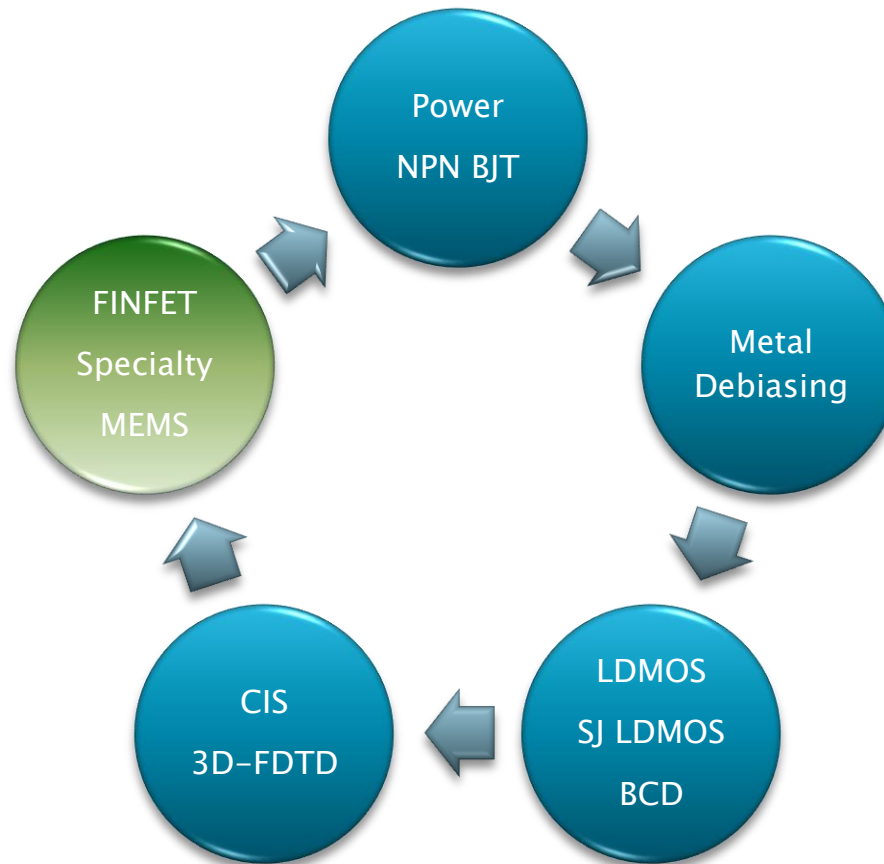


2D–Cut of the Incident Light
relative energy density

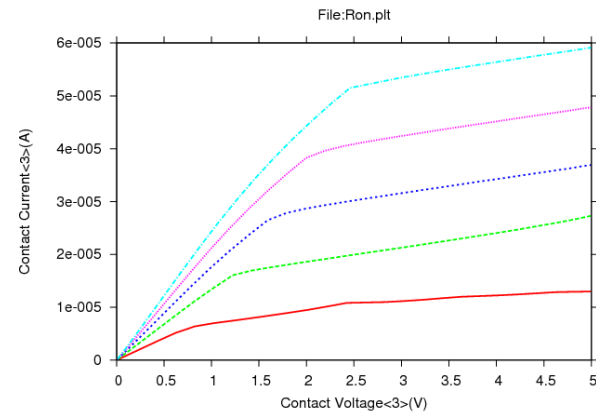
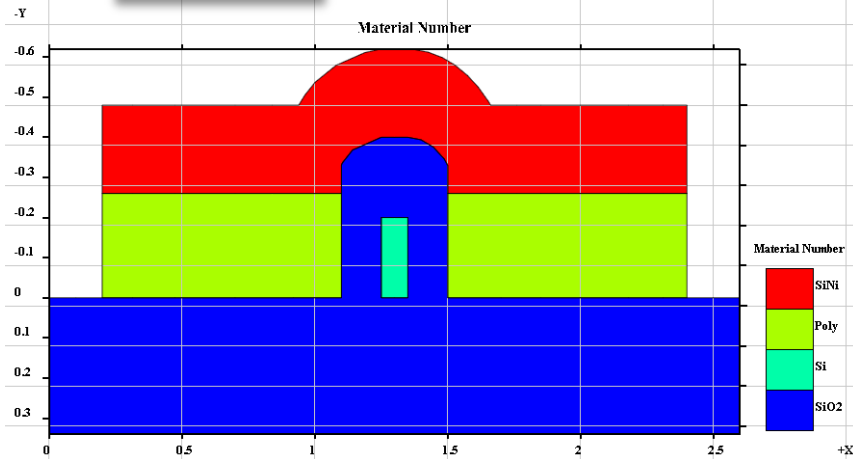
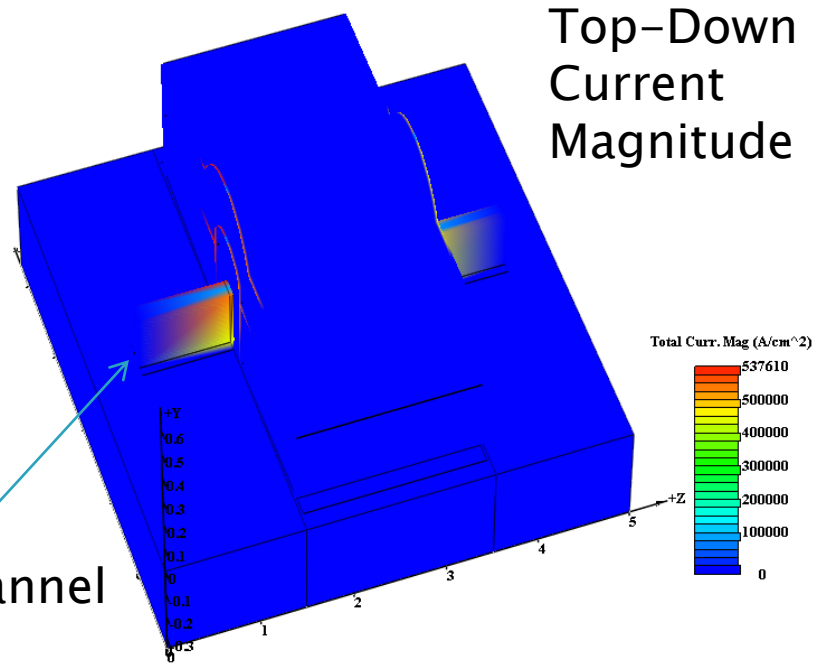
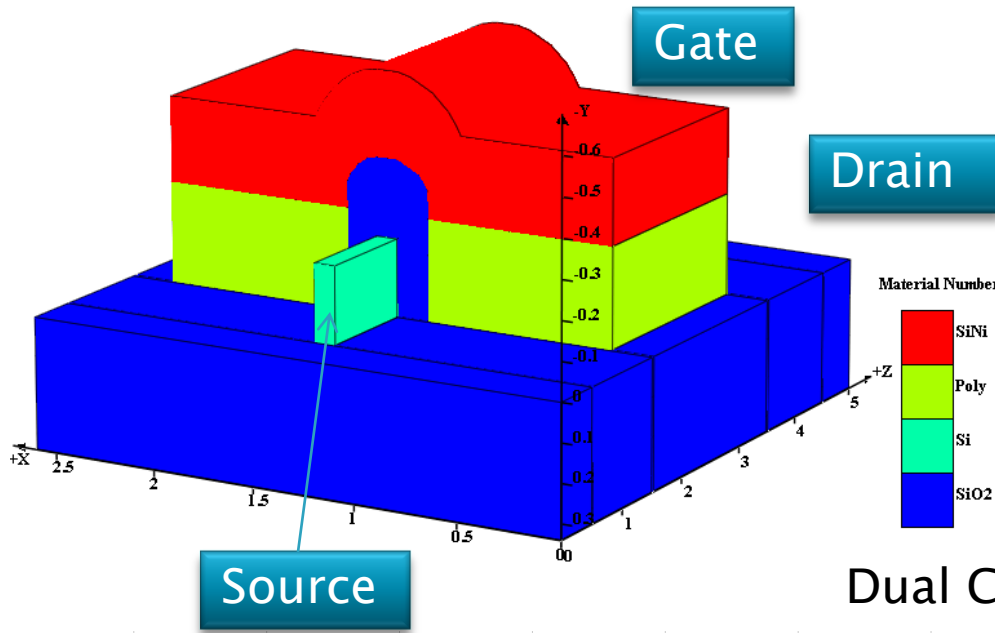


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Examples List:

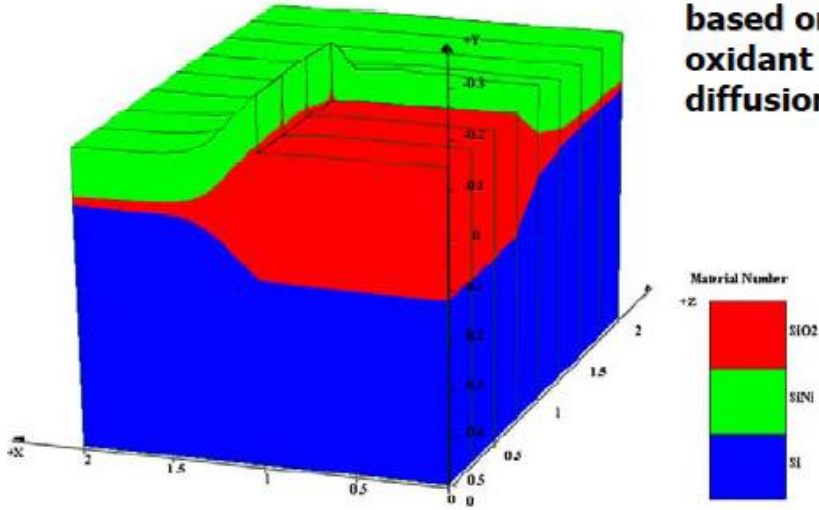


3D Process Simulation of FINFET



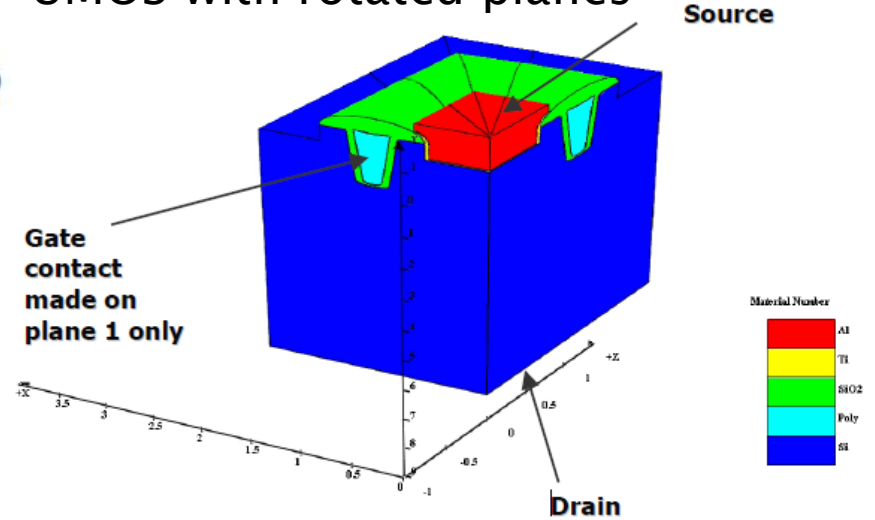
Some Other Specialty Devices

3D LOCOS growth



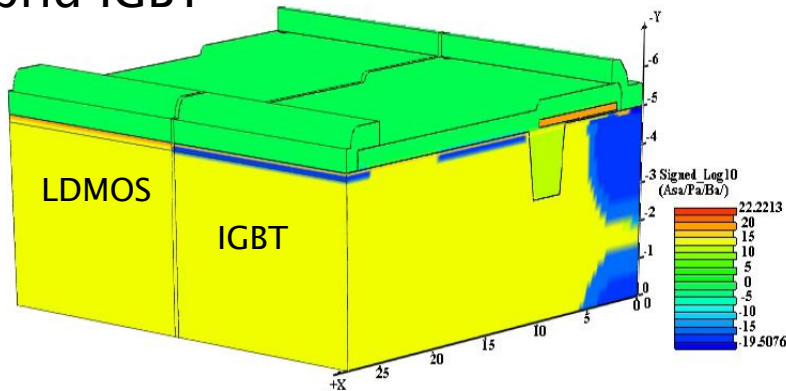
Field oxide growth simulation based on 3D oxidant diffusion.

UMOS with rotated planes

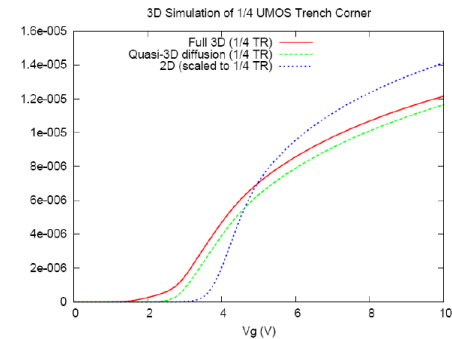


Use rotated mesh planes so that the U-shaped trench/GOX can be accurately defined for all parts of the 3D structure which is to be compared with pure 2D simulation of plane 1.

Hybrid IGBT

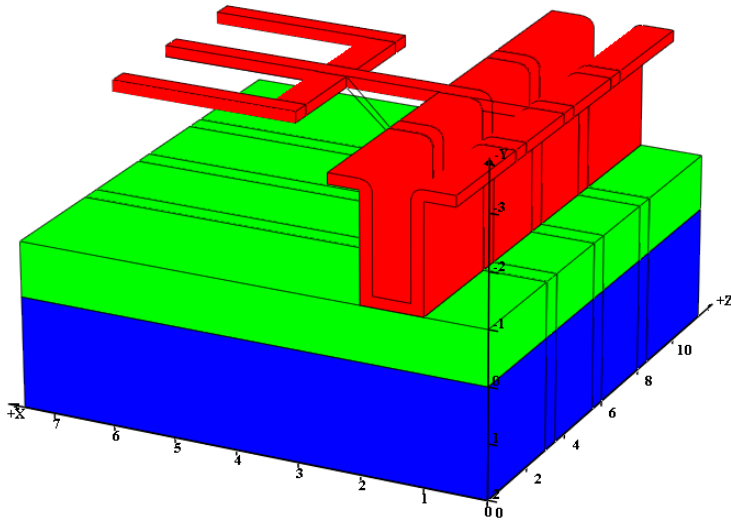


Comparison of Id-Vg

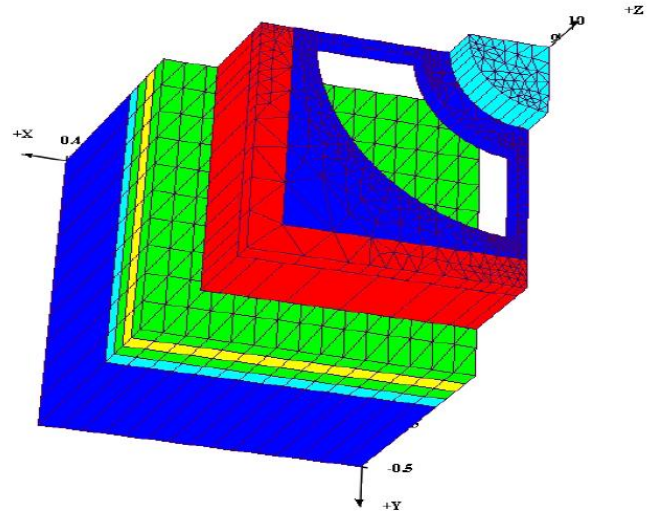
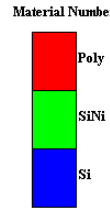


UMOS Id-Vg

3D Process Simulation of MEMS Devices

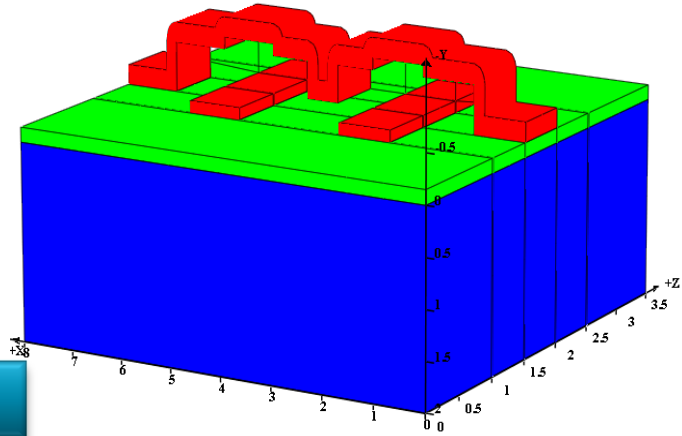
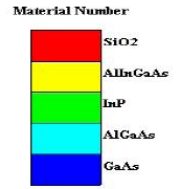


Electro Meter

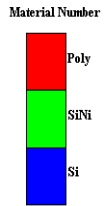


V-MEMS Tunable VCISOs

File Name : 3d_3.ztr
File Type : CSuprem
Variable Name :
Material Number:
3D Cube Contour Parameters :
X Range : 0.1 - 0.4
Y Range : -0.5 - -0.2
Z Range : 0 - 9.5
X Cut Line Num : 15
Y Cut Line Num : 15
Z Cut Line Num : 15



RF Switch



3D CSuprem Process Simulation Summary

- ▶ PC: HP Laptop with Intel Core2 P8600@2.4G Memory 6G, Video card: 512M Nvidia 9600M GT
- ▶ System: Windows Vista 64bit

	MEMS – Electro meter	MEMS– RF Switch	NPN BJT Quasi3D	NPN BJT Full3D	Metal Interconnect	SJ LDMOS Quasi3D	SJ LDMOS Full3D
Time	40s	60s	22m	40m	17m	50m	92m
Mesh	1198	1068	36455	36455	115700	79049	85931
Planes	15	5	25	25	154	33	33

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Thank You!