Senior Layout Contractor Resume

★★★★★ 3.00 /5 (Submit Your Rating)

Austin, TX

SUMMARY

- TEMPPrincipal level layout designer; Extensive expertise and experience in layout floor planning, standard cell planning, hierarchical layout assembly, device matching, place and route of large digital and analog blocks, pad - ring, ESD clamps adjustment, post layout parasitic extraction and re-run timing/ power simulation, shielding and guard ringing, DFM, tape out GDSII format and E-beam mask generation.
- Capable of doing complex analog and digital design, experienced in mixed-signal, RF, digital datapaths, standard cells and place & route
- Enjoy being a leader of new companies or capable of doing stand-alone work or leading a back end team; comfortable being a contractor or a direct hire
- Able to design layouts for entire integrated circuit, construct layout plans, create, debug & document new design flows; deliveries made on-time with minimal area
- Broad knowledge of custom mixed signal design flows with an emphasis on deep submicron analog circuit design and layout
- Passionate about doing teh business development necessary to create companies to innovate and design solutions for complex problems for new markets
- Completed designs in 10nm Finfet, 14nm Finfet, 16nm Finfet, 20nm Finfet, 28nm, and 45nm processes.
- Experienced in layout design of specific components and cells like low noise/low power RF components, ESD structures, large digital and various analog blocks.
- Very strong analytic and problem solving skills to create or debug custom physical design kits or flows.

TECHNICAL SKILLS

Platforms: Unix/Linux Redhat, Netlists, Microsoft Office

Tools: Cadence 7.0/6.1/12.0 Virtuoso VXL, First Encounter, Assura, PVS, Mentor Calibre & Real Time, Laker

Technologies: Samsung 10nm Finfet, TSMC 65-16nm FinFet, Global Foundries 40nm, Jazz SiGe SBC18QTD

PROFESSIONAL EXPERIENCE

Confidential, Austin, TX

Senior Layout Contractor

Responsibilities:

- Layout of Bluetooth bias ldo block in TSMC 40/45 process
- Lead designer on latest chip for team in an ultra-low power RF 40/45 nm ultra-low power TSMC process.
- Responsible for entire analog and digital portion of chip in IBM/Global Foundries SOI process.
- Porting and shrinking analog switches, voltage regulators and LDOs from IBM to TSMC SOI 11 nm process.

Confidential, Santa Clara, CA

Senior Layout Contractor

Responsibilities:

- Layout connections on top level analog block in TSMC 28 nm for 5G RF chip.
- Worked closely with chip lead designer in verifications of DRC, LVS, VMSLAY and interpreting teh results.
- Lead person for LNA RF chips.
- Floor planned and instructed other layout persons on layout.
- Quick turn around on analog blocks and chips in one week.
- Completed very complex high speed 30GHz transmitter block in Samsung 14 nm in just 3 months

Confidential, San Diego, CA

Senior Mask Layout Designer

Responsibilities:

- Lead for DDR 2.0 and 2.5 block currently in Snapdragon 810 processor
- Completed layout of analog LDO and opamps blocks for SerDes
- Main physical designer driving place and route Cadence First Encounter for 10 DDR control blocks
- Layout with TSMC 20nm technology for FIFO blocks
- Created layouts that are matching aware, mitigate deep submicron TEMPeffects, and minimize noise sources
- Led international team of six (6) on advanced bandgaps and PLL transceiver in Samsung FinFet 10nm for Snapdragon 835 processor

Confidential, Plano, TX

Consultant

Responsibilities:

- Consulted on TSMC .65um and Global Foundries .40um complex IO pad design using Laker/ Mentor

software.

- Completed layouts on clock drivers, current calibrator, multiple level shifters, and receivers with driver logic.
- Multiple type voltage devices within guard rings and ESD protection

Confidential, Austin, TX

Founder, VP of Business Development and Director on Board

Responsibilities:

- Bootstrapped a new design group Confidential
- Created concepts for new IP around “smarter” and more efficient solar PV panel technology
- Co-author first patent for smart module for PV panels
- First working proto type for DC to DC converter
- Successfully positioned company for Austin Ventures $6.1M Round A funding

Confidential, Austin, TX

Contractor, ST/NXP Wireless

Responsibilities:

- Completed teh layout on major RF power management unit and accessory detector blocks
- Extensive common centroiding of devices and use of shielding signals to insure best performance and processing in TSMC .65nm process; utilized Cadence VXL for layout and Mentor Calibre for verification
- Successfully completed four (4) different delta-sigma modulators (DSM) in four (4) months for Round A
- DSM designed in SiGe SBC18QTD Jazz fab process with Cadence VXL to run at 900-2.1GHz
- Second version of DSM chip secured $30M C round for final product design
- Simultaneously completed a JAG timing driven block to prove out design flow with First Encounter
- Accomplished complex custom datapath block in TSMC .90nm process for CLX processor
- Assigned to GlobespanViarata, Melbourne, FL for wireless PCI project
- Worked on critical analog circuits and tested mux logic
- Researched multiple vertical markets for new high-speed processor
- Marketing contacts led to funds for spin off division Coherent Logix


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