# A CMOS Voltage Reference with Temperature Sensor using Self-PTAT Current Compensation

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**ABSTRACT**

An all-CMOS circuit for combined voltage reference and temperature sensor is proposed. For voltage reference design, a self-PTAT current is generated for compensating a diode-connected NMOS transistor for achieving temperature-independent purpose. In addition, an ultra linear temperature sensor can be realized and achieved simultaneously. The circuit topology is very suitable for SoC integration. The voltage reference provides a stable voltage for analog circuit. Moreover, the temperature sensor increases the system reliability by predicting eventual faults caused by excessive chip temperatures.

## I. INTRODUCTION

A voltage reference circuit is a key element in the design of many mixed-signal and analog integrated circuits, such as oscillators, PLLs, and data converters. The requirements of such circuits are stable over process, power supply voltage, and temperature variations. Particularly, in the SoC era, a chip often contains several millions of transistors. Its power dissipation increases and consequently the temperature increases. This problem is especially magnified in circuits operating at high frequency. A chip with built-in temperature sensor increases the system reliability by predicting deadly faults caused by excessive chip temperature.

The most widely used schemes of integrated voltage references with low temperature dependency are based on the bandgap approach. With the rapid evolution of CMOS technology, the CMOS bandgap reference was developed [1]. For full CMOS voltage references, mutual compensation of mobility and threshold voltage was used to design a temperature-independent voltage reference, which was biased at the zero temperature coefficient (ZTC) point [2]. Najafizadeh used PTAT current source to bias a diode-connected transistor for achieving temperature-independent voltage reference [3]. Arabi used the relationship of oscillating frequency with temperature to design temperature sensors [4]. Diode-connected MOS transistors were also used to realize temperature sensors [2]. One way for temperature sensor design is the bandgap approach [5].

## II. THE PTAT CURRENT

For a diode-connected NMOS transistor, the I-V characteristics with temperature swept are shown in Fig. 1. The ZTC point is indicated on the figure. The gate-source voltage and drain current are temperature-invariant at ZTC point. Since the drain current cannot be easily kept constant for large temperature variations, the proposed voltage reference is not designed at the ZTC point. Considering the gate-source voltage exactly at 711 mV rather than at the ZTC point, the drain current with respect to temperature is shown in Fig. 2. Obviously, the relation between the drain current and temperature is nearly linear. Based on such concept, if the PTAT current can be generated, the gate-source voltage will be compensated and independent of temperature.

Let the PTAT current, $I_D(T)$, be modeled as

$$I_D(T) \cong I_{D_0}\left[1+\eta\left(T-T_0\right)\right] = I_{D_0}\left[1+\eta \cdot dT\right] \qquad (1)$$

where $\eta$ is the PTAT current temperature coefficient. $I_{D_0}$ is the drain current at $T = T_0$. $T_0$ is the reference temperature in ${}^oK$ (Kelvin). Let the gate-source voltage of the diode-connected NMOS be designed at $V_{GS,Q}$, which is constant and independent of temperature by assumption. Its drain current can be represented as

$$I_D(T) = (1/2)\mu(T)C_{ox}(W/L)\left(V_{GS,Q} - V_{TH}(T)\right)^2$$
$$= \left(\frac{1}{2}\right)\mu(T)C_{ox}\left(\frac{W}{L}\right)\left(V_{GS,Q} - V_{TH0}\right)^2\left(1 - \frac{V_{TH}(T) - V_{TH0}}{V_{GS,Q} - V_{TH0}}\right)^2 \quad (2)$$

where $I_{D0} \triangleq I_D(T_0)$ , $V_{TH0} \triangleq V_{TH}(T_0)$ and $\mu_0 \triangleq \mu(T_0)$.

For the BSIM3v3 MOS model , the mobility, $\mu(T)$ , and the threshold voltage, $V_{TH}(T)$ , are temperature dependent parameters. They are represented as

$$\mu(T) = \mu_0\left(1 + \frac{T - T_0}{T_0}\right)^{U_{TE}} \quad (3)$$

$$V_{TH}(T) = V_{TH0} + \left(K_{T1} + K_{T2}\cdot V_{BS}\right)\left(\frac{T - T_0}{T_0}\right) \quad (4)$$

where $U_{TE}$ is mobility temperature exponent. $K_{T1}$ is temperature coefficient of threshold voltage, and $K_{T2}$ is body bias coefficient of threshold temperature effect. Fortunately, the proposed circuit topology does not suffer from body effect. The body effect term in (4) can be omitted. Using (3) and (4) in (2), we have

$$I_D(T) = I_{D0}\left(1 + \frac{T - T_0}{T_0}\right)^{U_{TE}}\left(1 - \frac{K_{T1}}{V_{GS,Q} - V_{TH0}}\left(\frac{T - T_0}{T_0}\right)\right)^2 \quad (5)$$

Use Taylor series expansion about $T_0$ , then consider the first-order term and neglect the higher-order terms.

$$\left(1 + \frac{T - T_0}{T_0}\right)^{U_{TE}}\Bigg|_{T=T_0} \cong 1 + \frac{U_{TE}}{T_0}dT \quad (6)$$

$$\left(1 - \frac{K_{T1}}{V_{GS,Q} - V_{TH0}}\left(\frac{T - T_0}{T_0}\right)\right)^2\Bigg|_{T=T_0} \cong 1 - \frac{2K_{T1}}{V_{GS,Q} - V_{TH0}}\left(\frac{1}{T_0}\right)dT \quad (7)$$

Substituting (6) and (7) into (5) and neglecting the second order term, yield

$$I_D(T) \cong I_{D0}\left(1 + \left(\frac{U_{TE}}{T_0} - \frac{2K_{T1}}{V_{GS,Q} - V_{TH0}}\left(\frac{1}{T_0}\right)\right)dT\right) \quad (8)$$

Comparing (8) with (1), the PTAT current temperature coefficient, $\eta$ , can be obtained as

$$\eta = \frac{U_{TE}}{T_0} - \frac{1}{V_{OD0}}\left(\frac{2K_{T1}}{T_0}\right) \quad (9)$$

where $V_{OD0} \triangleq V_{GS,Q} - V_{TH0}$ is the overdrive voltage at $T_0$ .

From (9), if $\eta$ can be observed, then the PTAT current will be generated to compensate the diode-connected NMOS transistor. The voltage reference with temperature independency can be achieved.

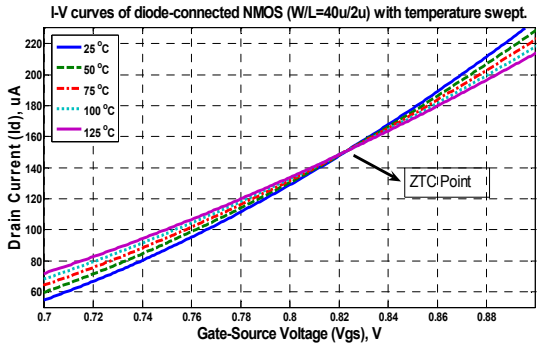


Fig. 1 I-V characteristics of diode-connected NMOS with temperature swept.

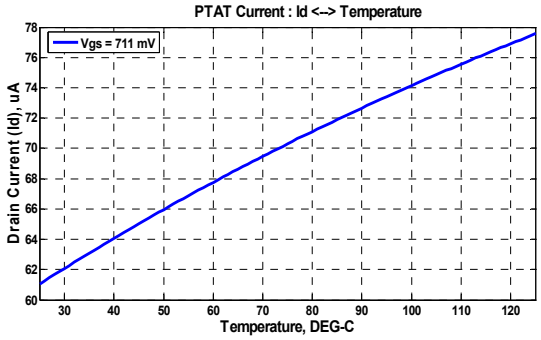


Fig. 2 The PTAT Current

## III. VOLTAGE REFERENCE WITH SELF-PTAT CURRENT COMPENSATION

In Fig. 3, the transistors M1-M4, OP1, and poly-2 resistor R automatically generate the suitable PTAT current to bias the diode-connected M1, and produce stable temperature-independent voltage level.

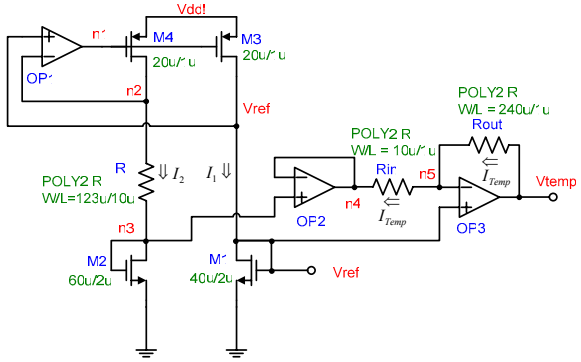


Fig. 3 Voltage Reference and Temperature sensor

To explain the operations of this circuit, we assume that the resistor R is associated with temperature coefficient, $\gamma$, i.e., $R(T) \cong R_0\left[1+\gamma(T-T_0)\right]$. Since nodes of n2 and Vref are connected to the inputs of the OP1, both have the same voltage. The output of the OP1 controls the M3-M4 to generate the suitable PTAT current, and the sizes of M3 and M4 are equal. Namely,

$$I_1(T) = I_2(T) = I_D(T) \tag{10}$$

$$V_{GS1}(T) = V_{GS2}(T) + I_D(T) \times R(T) \tag{11}$$

Therefore, from (11), the drain current, $I_D(T)$, is

$$I_D(T) = (2/C_{ox})\mu(T)^{-1} R(T)^{-2}\left(\sqrt{(L/W)_1} - \sqrt{(L/W)_2}\right)^2 \tag{12}$$

Using Taylor series expansion and considering the first-order approximation only, yields

$$\begin{aligned} I_D(T) &\cong I_{D0}(1+\eta dT) \\ &= (2/C_{0x})\mu_0^{-1}R_0^{-2}\left(\sqrt{(L/W)_1} - \sqrt{(L/W)_2}\right)^2\left(1-\frac{U_{TE}}{T_0}dT\right)(1-2\gamma dT) \\ &\cong I_{D0}\left[1-\left(\frac{U_{TE}}{T_0}+2\gamma\right)dT\right] \end{aligned} \tag{13}$$

That is $\eta = -\dfrac{U_{TE}}{T_0} - 2\gamma$. (14)

Plugging (14) into (9), the important design relation is

$$V_{OD0} = \frac{K_{T1}}{T_0} \Big/ \left(\gamma + \frac{U_{TE}}{T_0}\right) \tag{15}$$

Where $K_{T1}$, $U_{TE}$, and $\gamma$ are available from the simulation model of $0.35-\mu m$ CMOS technology. For the NMOS model with channel length and width in the range of $1.2\mu m \le (L,W) \le 20\mu m$, they are

$U_{TE} = -2.065168$

$K_{T1} = -0.2700492$

$\gamma = 0.00107$

Obviously, $V_{OD0}$ is constant and determined by (15). If $V_{OD0}$ is the overdrive voltage of M1 at $T_0$, the transistor M1 will be biased around $V_{ref} \equiv V_{GS,Q} \equiv V_{GS1} \cong V_{TH0} + V_{OD0}$ and is nearly independent of temperature. The simulation results justify the argument.

Furthermore, the variation of output voltage with respect to power-supply voltage can be described by the sensitivity.

$$S_{V_{DD}}^{V_{Vref}} = \frac{V_{DD}}{V_{Vref}}\frac{\partial V_{Vref}}{\partial V_{DD}} \equiv 0$$

The sensitivity is zero. That means the reference voltage is independent of power-supply voltage variation.

All operational amplifiers in Fig. 3 use two-stage topology with miller compensation. It provides about 76dB gain, and $62^o$ phase margin.

## IV. UTRA LINEAR TEMPERATURE SENSOR

The temperature information can be obtained from nodes of n3 and Vref, as shown in Fig. 3. The OP2 is utilized as a unity-gain buffer for isolation purpose. The other amplifier, OP3, is used to amplify the signal and to improve linearity with respect to temperature. Consider only first-order approximation and assume the open-loop gains of the OP2 and OP3 are infinity. We have

$$I_D(T)R(T) \cong I_{D0}R_0\left[1+(\eta+\gamma)(T-T_0)\right] \tag{16}$$

$$I_D(T)R(T) = V_{GS1}(T) - V_{GS2}(T) = I_{Temp}R_{in}(T) \tag{17}$$

$$V_{Temp}(T) = V_{GS1}(T) + I_D(T)R(T)\cdot\frac{R_{out}(T)}{R_{in}(T)} \tag{18}$$

The closed-loop gain of the OP3 is

$$\left|A_{cl}(T)\right| = \frac{R_{out}(T)}{R_{in}(T)} = \frac{R_{out0}\left[1+\gamma(T-T_0)\right]}{R_{in0}\left[1+\gamma(T-T_0)\right]} = \left|A_{cl}\right| \tag{19}$$

Clearly, if both resistors, $R_{in}$ and $R_{out}$, use the same materials, the closed-loop gain of the OP3 is temperature-independent. (18) can be simplified as

$$V_{Temp}(T) = V_{GS1}(T) + \left|A_{cl}\right| I_0R_0\left[1+(\eta+\gamma)(T-T_0)\right] \tag{20}$$

The sensitivity of $V_{Temp}(T)$ to $V_{GS1}(T)$ is defined as

$$S_{V_{GS1}}^{V_{Temp}} = \frac{V_{GS1}(T)}{V_{GS1}(T) + \left|A_{cl}\right| I_0R_0\left[1+(\eta+\gamma)(T-T_0)\right]} \tag{21}$$

In (21), if the closed-loop gain, $\left|A_{cl}\right|$, of the OP3 goes to infinity, the sensitivity will approach to zero. In other words, the linearity of the temperature sensor can be improved by increasing the closed-loop gain of the OP3.

## V. SIMULATION RESULTS

The circuit topology shown in Fig. 3 is realized by using $0.35-\mu m$ CMOS technology. The sizes of the transistors and resistors are indicated in Fig. 3. The circuit is simulated in the temperature range of $0^oC$ to $150^oC$ by using power supply of 3.3V.

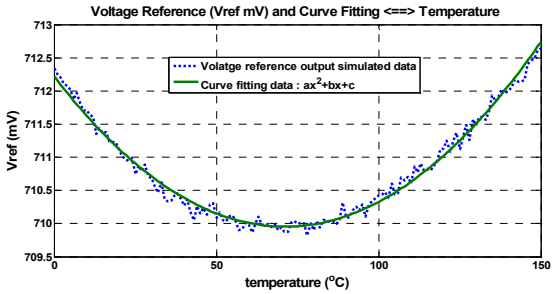


Fig. 4 Voltage Reference with Temperature

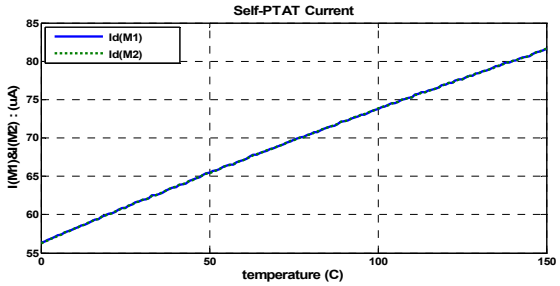


Fig. 5: Self-PTAT Current

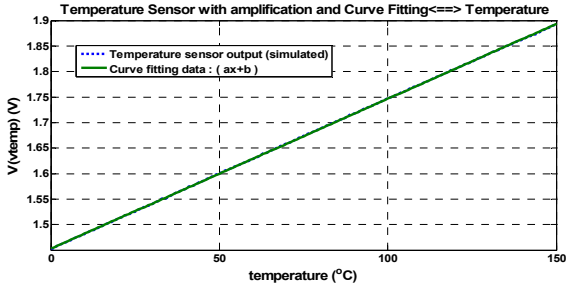


Fig. 6 Temperature sensor Response

Fig. 4 shows the voltage reference with respect to temperature. The transistor M1 is biased by self-PTAT current shown in Fig. 5. Due to excellent-compensation, the voltage reference provides a stable voltage of about 711mV with average temperature coefficient of around 26 ppm/$^oC$. The output voltage can be approximated as

$$V_{ref}(T) = 4.4783 \cdot 10^{-4} \cdot T^2 - 0.0637 \cdot T + 712.2184 \ (mV) \cdot$$

For the temperature sensor, the closed-loop gain of the OP3 is 24. In Fig. 6, the output of the temperature sensor is linear with slope (sensitivity) of *2.9* $mV/^oC$. It is approximated by the linear equation as

$$V_{temp,Fitting}(T) = 0.0029 \cdot T + 1.4528 \ \ (V) \qquad (22)$$

The measurement for the maximum deviation, $\sigma_{\max}$, of the temperature sensor is defined as

$$\sigma_{\max} = \frac{\max\left(\left|Error(T)\right|\right)}{V_{Temp,\max} - V_{Temp,\min}} \times 100\% \qquad (23)$$

Where $Error(T) \triangleq V_{Temp}(T) - V_{Temp,Fitting}(T)$ (24)

The metric of linearity is $L_n = \left(100 - \sigma_{\max}\right)\%$ (25)

The maximum deviation of the temperature sensor is below 0.4%, and the linearity is 99.6%. From (21), if the closed-loop gain of the OP3 increases, the linearity of the temperature sensor will approach to an ideal linear function and the slope (sensitivity) increases.

## IV. CONCLUSION

The proposed circuit topology uses all-CMOS devices. That implies the topology is very suitable for SoCs and mixed-signal circuit design. Furthermore, the system provides not only a voltage reference with temperature and supply-voltage independency, but also a highly linear temperature sensor. The simulation results show the voltage reference provides a stable voltage of 711 mV with mean temperature coefficient of 26 ppm/$^oC$ and the temperature sensor has sensitivity of 2.9 $mV/^oC$ with maximum deviation less than *0.4%*.


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