Concept For Electronic Calibration Of A CMOS Voltage Reference

M. Heinrich #, J. Heidrich #, T. Ussmueller #, R. Weigel #

#University of Erlangen-Nuremberg, Institute of Electronics Engineering, Erlangen, Germany
{heinrich, heidrich, ussmueller, weigel}@lte.eei.uni-erlangen.de

I. Introduction

With growing applications and functionality of small low-power wireless sensors like sensing and localization, the generation of a precise reference voltage becomes ever more important [1]. Reference voltages are usually generated by a bandgap circuit suitable for low-voltage operation [2]-[3]. It employs the different thermal behavior of bipolar diodes and resistors to generate a temperature independent voltage. However, modern CMOS processes do not feature dedicated bipolar devices and make use of parasitic ones. So, new types of voltage reference circuits have been presented that use only MOS devices to generate the desired temperature independent voltage [4]-[6]. Some of these bias cells are capable of low-voltage operation at a current consumption in the range of $1\mu A$. This makes them very desirable for wireless sensors. However, mos references show a strong dependance of process parameters and thus need trimming for accurate output voltage [7]. Also, for use as a reference of an analog-to-digital converter a voltage close to the supply voltage is beneficial for good conversion accuracy.
The goals realized in this concept are therefore a low-voltage low-current circuit with good relative and absolute precision over temperature. The minimum supply voltage has to be close to the reference voltage. A concept for calibration of both temperature behavior and absolute output voltage is presented. This is done via setting configuration bits by either fuses or any kind of external saved calibration data.

II. Basics of MOSFET Voltage References

The circuit of the presented reference cell consists of a proportional to absolute temperature (PTAT) current source which is formed by the transistors M1-M4 and the resistor R1, as can be seen in Fig. 1. The generated PTAT current is mirrored by M5 and the reference voltage is generated by the diode-connected FET M6. A startup circuit is implemented by transistors M13-M15. To achieve a good relative precision of the generated reference voltage in relation to its absolute value M6 should either be a high-V_{th} type or a low-g_m type. According to [2] the PTAT current can be expressed by

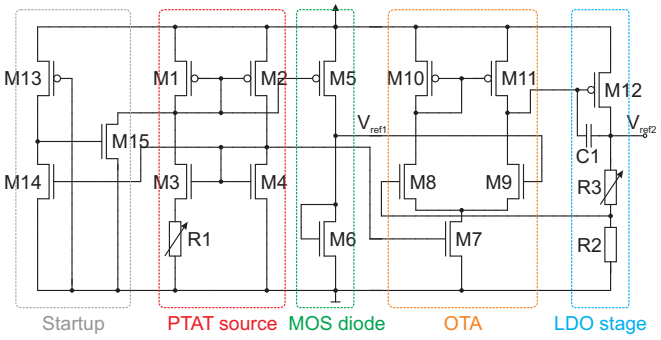

Fig. 1. Schematic view of the proposed adaptable voltage reference circuit.

$$I_{ref} = \frac{2}{\mu_n C_{ox}(W/L)_{M4}} \cdot \frac{1}{R_1^2}\left(1 - \frac{1}{\sqrt{N}}\right)^2, \tag{1}$$

with μ_n the electron mobility in NMOS devices, C_{ox} the area capacitance, W and L width and length of M4 and N the ratio of (W/L) of M3 to M4. The output current of this PTAT source is fed into the diode connected NMOS transistor M6 which generates the desired reference voltage V_{ref1}. A multiplication of the current I_{ref} by M = W(M5)/W(M1)

978-1-4244-7092-1/10/$26.00 ©2010 IEEE

helps to keep a reasonable size for M6. The size of M6 is chosen in a way that the output voltage at the minimum and maximum of the temperature range are equal. The output voltage of the MOS diode is given by

$$V_{ref1} = \sqrt{\frac{I_{ref}}{\mu_n C_{ox} \left(W/L\right)_{M6}}} + V_{th,M6}. \tag{2}$$

The function of the temperature dependence is mainly formed by first, a resistance is approximately proportional to absolute temperature. Second, the threshold voltage of a MOS transistor decreases linearly with temperature [8]. According to [9] this is expressed using the temperature coefficient K_{T1} by

$$V_{th}\left(T\right) = V_{th}\left(T_0\right) - K_{T1}\left(\frac{T}{T_0} - 1\right). \tag{3}$$

Other effects are changes in electron mobility μ as well as other nonlinear effects in the MOSFET that prevent a perfectly constant output voltage over temperature [5]. This results in a PTAT current which can be expressed as

$$I_{ref} = I\left(T_0\right) \cdot \left(1 + k\frac{T - T_0}{T_0}\right). \tag{4}$$

Due to this temperature dependency which counteracts the PTAT behavior of the current source the complete reference circuit shows a nearly constant output voltage over temperature. The remaining deviations can be quantified by a term V_{diff} describing the difference between the maximum and minimum voltage over the entire temperature range of concern as

$$V_{diff} = V_{ref1,max} - V_{ref1,min}. \tag{5}$$

The goal of optimization is to minimize V_{diff}. Therefore, due to the characterisitcs of V_{ref1} over temperature $V_{ref1,max}$ should be equally reached at minimum and maximum temperature. $V_{ref1,min}$ should be reached at the temperature T_M of

$$T_M = \frac{T_{min} + T_{max}}{2}. \tag{6}$$

In the nominal case a V_{diff} of $1.4mV$ is achieved. $V_{ref1,min}$ is $619.2mV$ at $T_M = 48°C$. Due to process variations V_{ref1} can vary by a considerable amount, both in temperature dependance and absolute value. Both effects are shown by the simulation results of five predefined corners in Fig. 2 for the PTAT current and reference voltage. The different temperature characteristics are visible as well as a deviation of $\pm 50mV$ in absolute voltage.

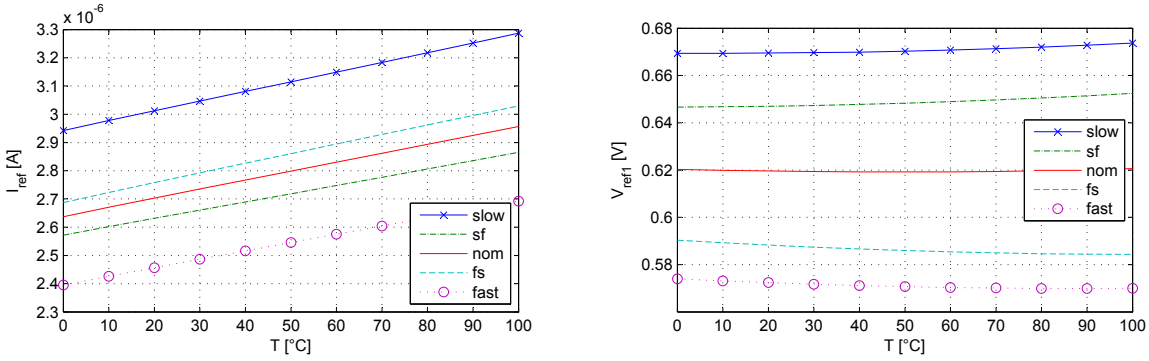

Fig. 2. Simulated PTAT currents I_{ref} and corresponding reference voltages V_{ref1} for five different process corners.

III. Compensation of Behavior versus Temperature

The first step is to correct the temperature characteristic of the output current in the PTAT source. The resistor R_1 is therefore split into a fixed part for the basic feedback and a tunable part for compensation of I_{ref} versus T. The adaptable part is controlled by a number of digital input bits $b_{T,i}$ that switch the PTAT core current either through a resistor or a bypass transistor. A low-V_{th} type transistor is chosen as bypass element due to lowest on-resistance at low supply voltages. For ease of implementation the values of the switched resistors are chosen according to the weight of the corresponding input bit which removes the need for a binary decoder. A schematic illustration of the switched resistor implementation is given in Fig. 3. The focus is to keep the number of bypass transistors as low as possible due to mos transistors showing a temperature dependence that is different to that of the resistors that get bypassed. Thus a larger number of series fets

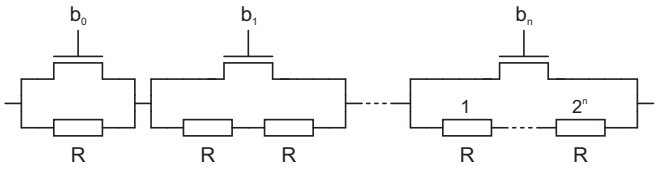

Fig. 3. Schematic illustration of the switchable resistor elements.

introduces new errors in temperature gradient which should actually be corrected in this stage. The nominal design value is implemented as the highest value bit $b_{T,n}$ set to 1 and others to 0 so that the tuning range extends equally up and down from the nominal value. The necessary tuning range is determined by corner analysis of the process variations. The number of bits is a tradeoff between implementation effort and desired precision. A resolution of four bits is sufficient to realize a step size of roughly 7 $°C$ for T_M allowing for a sweep of T_M from $-5°C$ to $100°C$. The step size also determines the remaining error in the calibrated circuit. For the chosen temperature range from $0°C$ to $100°C$, a value of $T_M = 50°C$ gives optimum temperature performance.
The tunable elements are realized as a MOS-transistor in parallel to unity resistors. 2^i unity resistors form a group representing the binary weights of the input control bits. In Fig. 4 the output currents I_{ref} of the PTAT source and the resulting reference voltages V_{ref1} at the diode-connected MOSFET M6 are shown. The simulation parameters for process variations are set to nominal to illustrate the range of temperature tuning possible by the proposed setup. A lower total feedback resistance results in a higher PTAT current as well as a shift of T_M towards higher temperatures. The correction

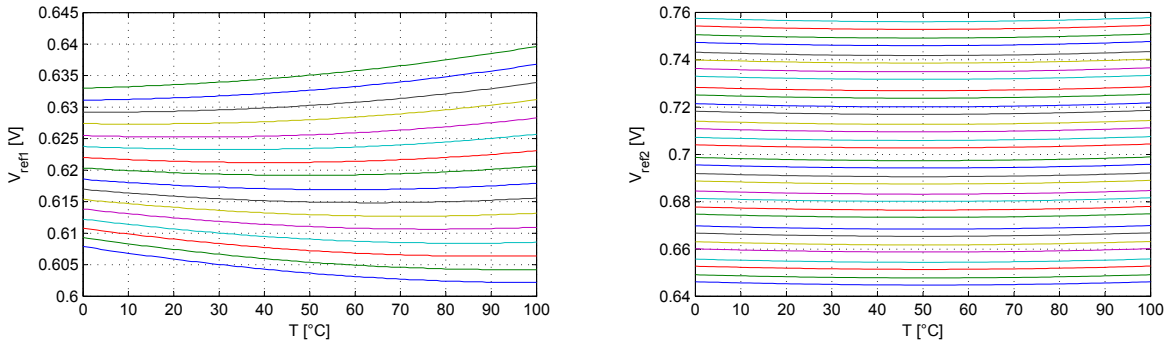

Fig. 4. Tuning ranges for the reference voltages V_{ref1} for all possible input values $b_{T,i}$ and V_{ref2} for all possible input values $b_{abs,i}$ at nominal inputs.

of the temperature curve also has a positive effect on the reference voltage V_{ref2} since a process variation which results in a negative temperature coefficient generally also exhibits a low absolute value for V_{ref2}. The correction procedure results in a higher PTAT current I_{ref} and thus a higher value for V_{ref1} which again relaxes the requirements for correction of the absolute voltage.

IV. Correction of Absolute Output Voltage

The correction of the absolute output voltage is done by a adjustable amplifier with a simple one-stage error amplifier. The error amplifier is implemented as an OTA formed by the devices M7 to M11 whereas M12 is the LDO pass transistor. To ensure stability of the feedback loop the capacitor C1 is inserted exploiting the Miller effect to keep its size small. The design goal of the output stage is to minimize the voltage drop. So, the feedback network of the amplifier consists of a fixed resistor towards ground and a switchable resistor controlled by the input bits $b_{abs,i}$ closing the feedback between the LDO-output and the feedback point. The switchable resistors are designed like the ones used for temperature compensation. At this point, keeping the number of bypass transistors low is very important because a higher number of pass transistors in the feedback network change the temperature gradient while in theory V_{ref1} is simply amplified by

$$V_{ref2} = V_{ref1}\left(1 + \frac{R_{3,i}\sum b_{abs,i}\cdot 2^i}{R_2}\right). \tag{7}$$

Since the output voltage of the LDO directly represents the corrected reference voltage it can be as close to V_{DD} as V_{drop} with V_{drop} as low as a few tens of mV. Fig. 4 illustrates the output voltage V_{ref2} for the different settings of the five input bits $b_{abs,i}$. The implementation allows for $110mV$ adjustment of the output voltage at nominal simulation setup in 31 steps of about $3.5mV$, resulting in an mean output voltage within $\pm 1.75mV$ of the desired value. The nominal value for implementation V_{ref2} is chosen to $700mV$ which gives about $30mV$ headroom to the maximum simulated V_{ref1}. The calibration process is visualized in Fig. 5 showing the uncalibrated and the temperature compensated V_{ref1} and V_{ref2} and fully calibrated voltage V_{ref2}. Using $b_T = 0001$ and $b_{abs} = 01010$, the calibrated values for T_M, V_{diff} and $V_{ref2,min}$ are $51°C$, $1.5mV$ and $699.0mV$, respectively, compared to $-6°C$, $6.9mV$ and $736.8mV$ with the nominal $b_T = 1000$ and $b_{abs} = 10000$. The design was thoroughly simulated, a layout done and the extracted parameters used in a final

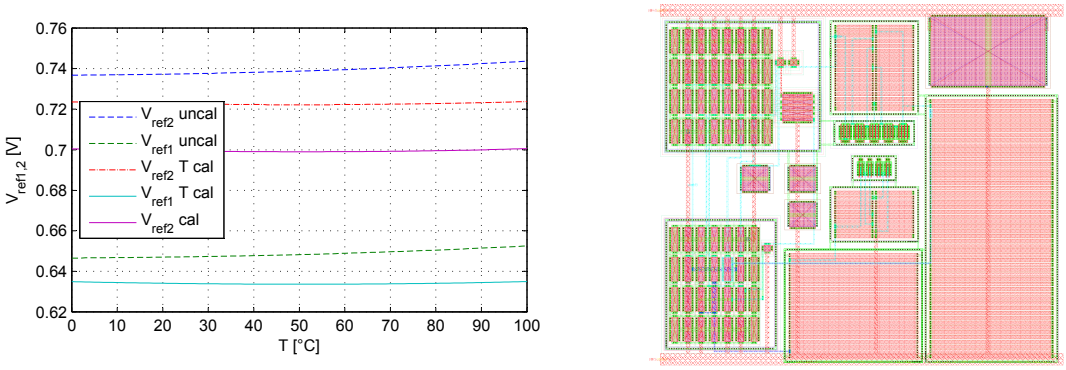

Fig. 5. The voltages V_{ref1} and V_{ref2} in different states of calibration (uncal: uncalibrated, T cal: temperature compensated, cal: temperature and absolute voltage calibrated) and layout of the tunable CMOS voltage reference

verification. The layout shown in Fig. 5 occupies an area of $60\mu m * 66\mu m$ in a 130 nm standard CMOS technology.

V. Conclusion

In this paper an approach for a CMOS voltage reference with the ability to calibrate both voltage over temperature behavior and absolute voltage value is presented. This is achieved by electronic controlled trimming of resistances in the PTAT current source and output amplifier. For the transistors in the PTAT current source, the diode connected reference source and the error amplifier a common size of width $W = 1\mu m$ and length $L = 4\mu m$ was chosen. The design has a nominal total current consumption of $3.4\mu A$ and operates at a minimum supply voltage as low as $800mV$ for the chosen V_{ref2} of $700mV$. The design can be optimized for even lower current consumption by using higher resistances as well as narrower and/or longer transistors. However, such an adaption increases the chip area due to the larger size of both resistors and FETs.

Acknowledgement

The circuit was developed at the Institute of Electronics Engineering within the scope of a research project funded by the German Aerospace Center (DLR) and the Bavarian Ministry for Economy, Traffic, Infrastructure and Technology. The integrated circuits are fabricated by Infineon Technologies.

References

[1] J. Heidrich, D. Brenk, J. Essel, G. Hofer, G. Holweg, G. Fischer, and R. Weigel, "Low voltage reference cells for uhf transponders with advanced features," *Microwaves, Communications, Antennas and Electronics Systems, 2009. COMCAS 2009. IEEE International Conference on*, pp. 1 –8, Nov. 2009.

[2] B. Razavi, *Design of analog cmos integrated circuits*. McGraw-Hill Higher Education, 2001.

[3] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A cmos bandgap reference circuit with sub-1-v operation," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 5, pp. 670–674, May 1999.

[4] L. de Carvalho Ferreira and T. Cleber Pimenta, "A cmos voltage reference based on threshold voltage for ultra low-voltage and ultra low-power," in *Microelectronics, 2005. ICM 2005. The 17th International Conference on*, Dec. 2005, pp. 10–12.

[5] T. Borejko and W. Pleskacz, "A resistorless voltage reference source for 90 nm cmos technology with low sensitivity to process and temperature variations," *Design and Diagnostics of Electronic Circuits and Systems, 2008. DDECS 2008. 11th IEEE Workshop on*, pp. 1 –6, Apr. 2008.

[6] L. Najafizadeh and I. Filanovsky, "A simple voltage reference using transistor with ztc point and ptat current source," *Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on*, vol. 1, pp. I – 909–11 Vol.1, May 2004.

[7] J. Heidrich, D. Brenk, J. Essel, M. Heinrich, G. Hofer, G. Holweg, R. Weigel, and G. Fischer, "Design of an electronically adaptable low-power reference cell for low-cost cmos processes," in *International Conference on Microwave, Radar and Wireless Communications*, Jun 2010, p. to be published.

[8] K. N. Leung and P. Mok, "A cmos voltage reference based on weighted δvgs for cmos low-dropout linear regulators," *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 1, pp. 146–150, Jan 2003.

[9] X. J. Xi, M. Dunga, j. He, W. Liu, K. M. Cao, X. Jin, J. J. Ou, M. Chan, A. M. Niknejad, and C. Hu, *BSIM4.3.0 MOSFET Model - User's Manual*. University of California, Berkley, 2003.