Topic 122

Reliability Challenges in Integrated High Voltage Devices

Peter Moens
AMI Semiconductor
Oudenaarde, Belgium
and
Geert Van den bosch
IMEC
Leuven, Belgium

Integrated medium-to-high voltage transistors with a breakdown voltage between 20 and 100V, are widely used in automotive, industrial and even medical applications. These transistors are used as an interface between the sub-micron digital CMOS and the analog outside world. Often, the transistors have to switch relatively large currents (1-10A), and as such power dissipation is a prime concern.
In this tutorial, the challenges in device reliability for integrated smart power devices are highlighted. An overview of the applications and the resulting quality and reliability requirements is given. The most common types of devices are presented and discussed (DeMOS, LDMOS, VDMOS, IGBT, ...). Their typical device reliability problems are highlighted. These are, amongst others : DC hot carrier, robustness under ESD-like events, switching of different types of loads, operation and failure upon single and multiple power pulsing, thermal modeling, etc… The different measurement techniques used to assess the complete reliability behavior of integrated power devices, are discussed

Peter Moens

Dr. Peter Moens received a M.S. and a Ph.D. in solid state physics from the University of Gent, Belgium, in 1990 and 1993 respectively. From 1993 till 1996, he worked as a post-doctoral fellow in collaboration with Agfa-Gevaert, Mortsel Belgium on the electron capture efficiency of silver halide emulsions. In 1996, he joined AMI Semiconductor, Oudenaarde, Belgium where he is involved in the development of smart power technologies and devices. His present activities are focusing on advanced device concepts and the reliability of integrated power devices. He is author or co-author of over 60 papers in international journals and proceedings and issued several patents. He is vice-chairman of the HV reliability sub-committee of IRPS.

Geert Van den bosch

Dr. Geert Van den bosch received the M. Sc. in electrical and mechanical engineering in 1987 and the Ph. D. in applied sciences in 1993, both from the Katholieke Universiteit Leuven, Belgium.

In 1987, he joined the Interuniversity Microelectronics Center (IMEC) in Leuven, where he did research on basic hot-carrier degradation effects, semiconductor device physics and electrical characterization techniques. From 1993 to 1999 he has been active in the development of several generations of deep submicron mixed-signal CMOS technologies. Since 1999, he has been working as a Senior Reliability Researcher in fields such as plasma and process induced damage, hot-carrier degradation, ultrathin gate oxide integrity, Cu-low-k dielectric back end reliability, and the reliability of high voltage devices and smart power technology.

Dr. Van den bosch has served as a technical program committee member of the Plasma and Process Induced Damage (P2ID) conference, the International Conference on IC Design and Technology (ICICDT) and the International Reliability Physics Symposium (IRPS).

Reliability Challenges in Integrated High Voltage Devices

Peter Moens

AMI Semiconductor BVBA, Belgium

Geert Van den bosch

IMEC, Belgium

Overview

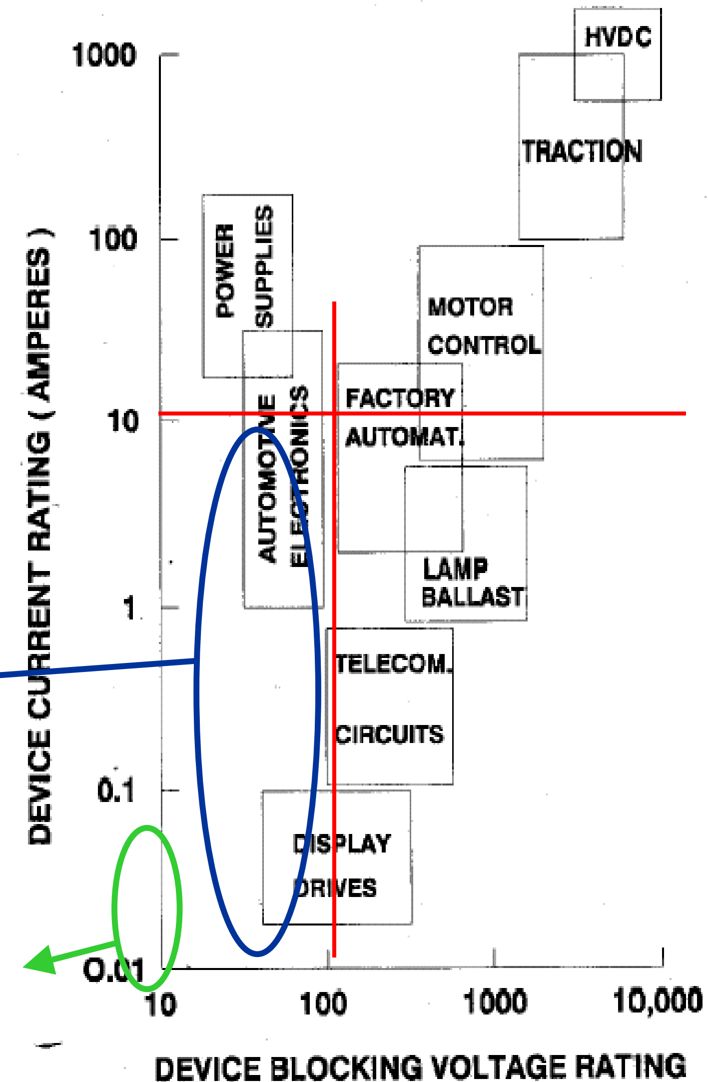
- Introduction
- Q&R Specifications
- Device Overview
- Reliability Measurements and Analysis Techniques
- Reliability Problems in Smart Power Technologies
- Conclusions

Overview

- *Introduction*
- *Q&R Specifications*
- *Device Overview*
- *Reliability Measurements and Analysis Techniques*
- *Reliability Problems in Smart Power Technologies*
- *Conclusions*

Introduction

- *Voltage : ~100 V*
- *Current : ~10 A*
- *Smart : integrated CMOS processing*
- *Trend from discretes to ASICs*
- *Interface with the "real" world*



Smart HV & Power technologies

CMOS technologies

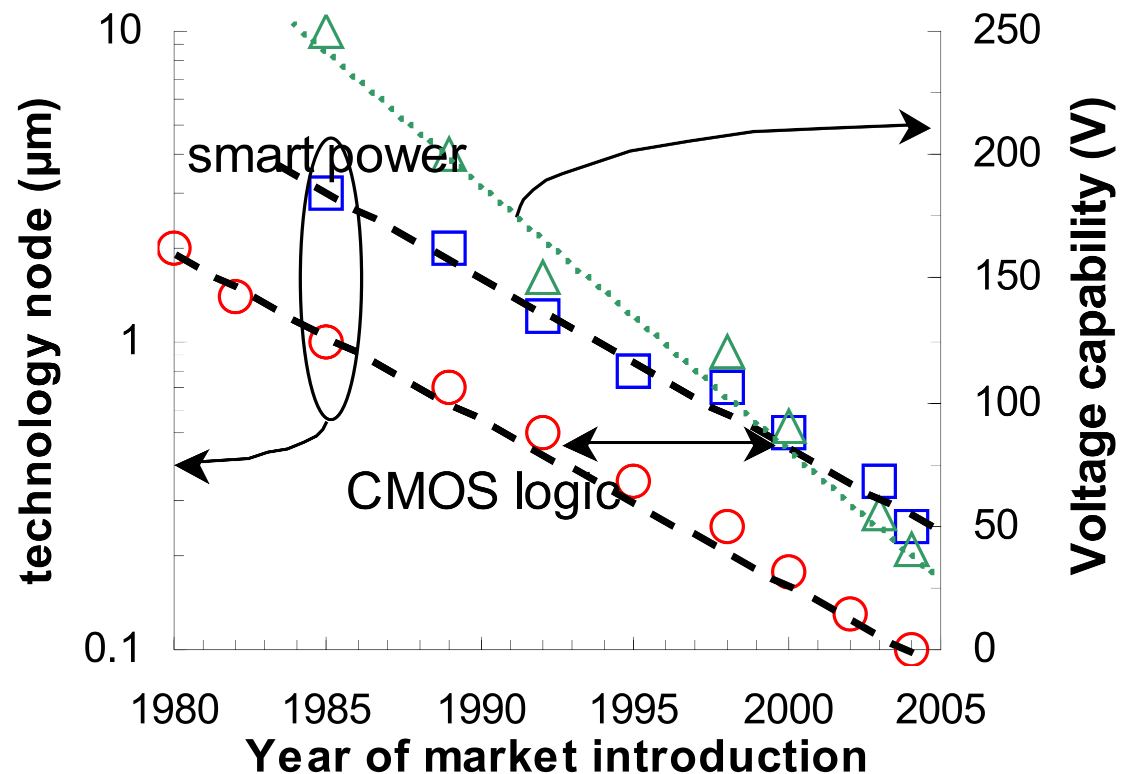
Introduction

- ***Automotive***
- ***Peripherals (printers, …)***
- ***Industrial (washing machines, …)***
- ***Battery management***
- ***Drivers (xDSL, displays)***
- ***Medical (implantables…)***
- ***Consumer (home cinema…)***

See refs [1-5]

Introduction

- ***Smart Power roadmap follows ITRS, but with a delay of ~3 technology nodes.***
- ***V_{bd} drops***
- ***Is there a need to go to lower techno dimensions for HV/power ??***



- ***Smart power challenges***
  - Devices integrated in sub-µm CMOS technos :
    - Low cost (limited number of extra masks, process steps, use as much as possible the standard CMOS flow)
    - Small area (Ron) for a high V_{bd}.
    - Low metal resistance.
  - Flash, EEPROM and OTP
  - Heat generation: must be kept under control and has to be accurately modeled.
  - Isolation and latch-up
  - Reliability

Overview

- Introduction
- **Q&R Specifications**
- Device Overview
- Reliability Measurements and Analysis Techniques
- Reliability Problems in Smart Power Technologies
- Conclusions

Q&R Specifications at product level

- ***Dedicated specifications and criteria at product/technology level (automotive)***
  - All standard CMOS qualifications +
    - AEC-Q100 (Stress Test Qualification for Integrated Circuits)
    - AEC-Q101 (Stress Test Qualification for Discrete Semiconductors)
  - ISO 7637 : immunity to electrical disturbance (Schaffner pulses)
  - ESD : 4 kV HBM, 750V CDM, 400V MM
  - IEC 61000-4-2 : system ESD (8 kV contact discharge ; 15 kV air discharge)
  - High temperature (Tjunc ≥ 175 ^{o}C)

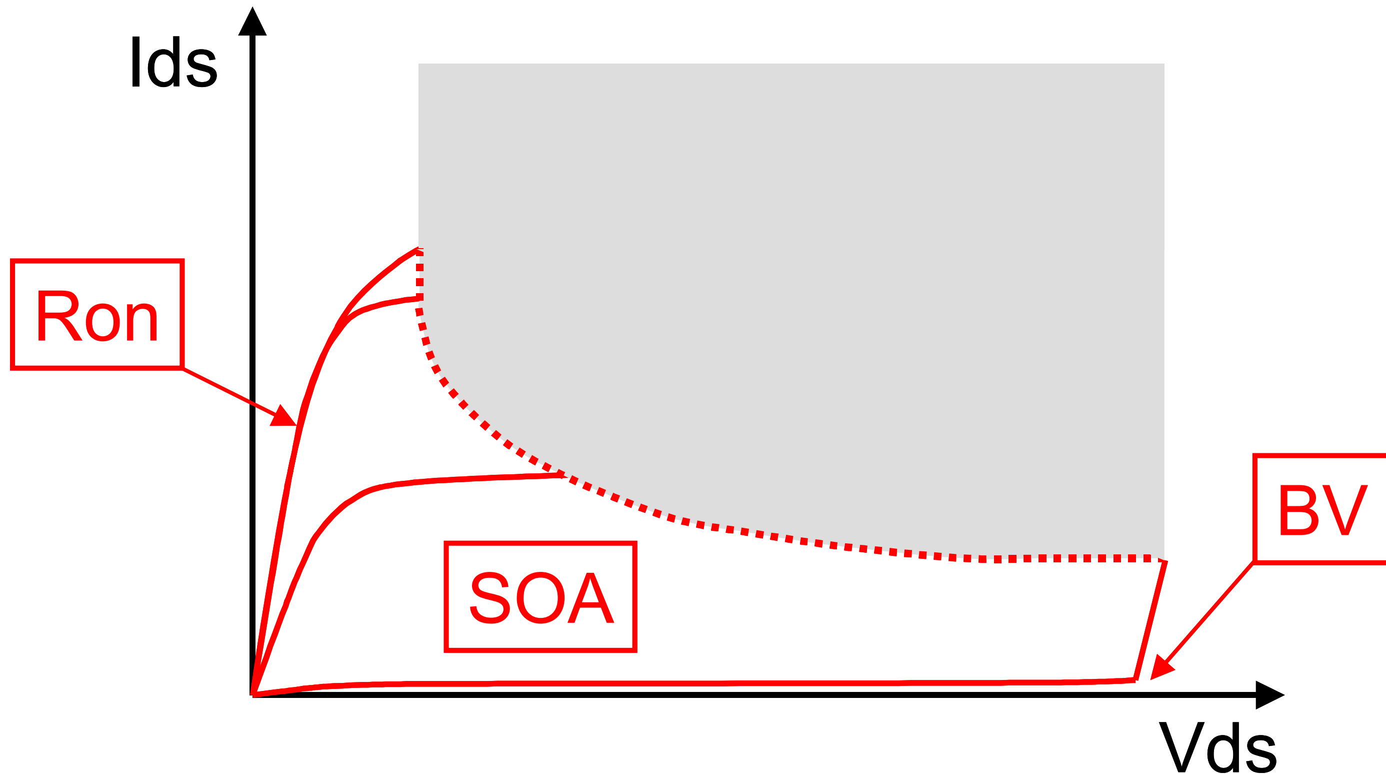
Q&R Specifications at product level

- ***High temperature applications [4,5]***

Mounting zone	Module description	Temperature zones and % of total operation time in each temperature zone			
		T1 (5%)	T2 (20%)	T3 (65%)	T4 (10%)
Engine Compartment	Temperate zone, thermally isolated	- 40 °C	25 °C	60 °C	85 °C
	Splash wall	- 40 °C	25 °C	90 °C	140 °C
	Attached to the engine or attached to the gearbox	- 40 °C	25 °C	95 °C	150 °C
	Throttle valve, close to the exhaust	- 40 °C	25 °C	120 °C	205 °C
Chassis	Locations exposed to heat sources	- 40 °C	25 °C	90 °C	120 °C
	Near breaks or hydraulics	- 40 °C	25 °C	105 °C	175 °C
Cabin	Dashboard, hat rack	- 40 °C	25 °C	60 °C	110 °C
	Roof under strong sun exposure	- 40 °C	25 °C	90 °C	115 °C

Q&R Specifications at device level

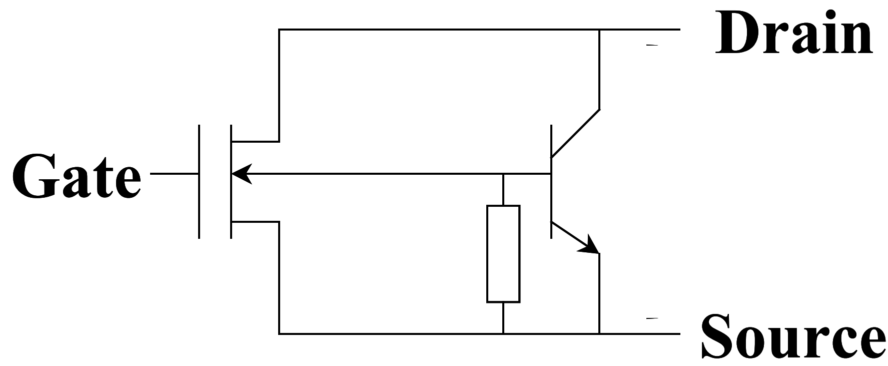
- R_{on} and V_{bd} are prime device parameters



- Trade-off between R_{on}, SOA and V_{bd}.

Q&R Specifications at device level

- **Every n(D)MOS has a parasitic NPN**



$$n_{ie}(T) \sim T^{3/2} \exp(-E_g / 2kT)$$

$$V_{bi}(T) \sim \frac{kT}{q} \ln(\frac{N_B}{n_{ie}(T)})$$

$$V_{bi}(T) = I_h(T).R_{base}(T)$$

- **Bipolar can be triggered :**
  - *Electrical : hole current I_h and/or base resistor R_B are large enough to forward-bias the E-B junction*
  - *Thermal : T is high enough such that $n_{ie} \sim N_B$ → E/B junction is wiped out ($T=T_{crit}(N_B)$), typically $T_{crit} \sim 700$ K).*

Q&R Specifications at device level

- *long-term (s…yrs): limited by hot-carrier degradation [6-21]. Continuous operation e.g. current source.*
- *short-term (ns…µs): limited by electrical bipolar snapback [22-30]. (system) ESD event.*
- *medium-term (µs…ms): limited by electro-thermal breakdown [31-41]. Switching of a load.*

Overview

- Introduction
- Q&R Specifications
- **Device Overview**
- Reliability Measurements and Analysis Techniques
- Reliability Problems in Smart Power Technologies
- Conclusions

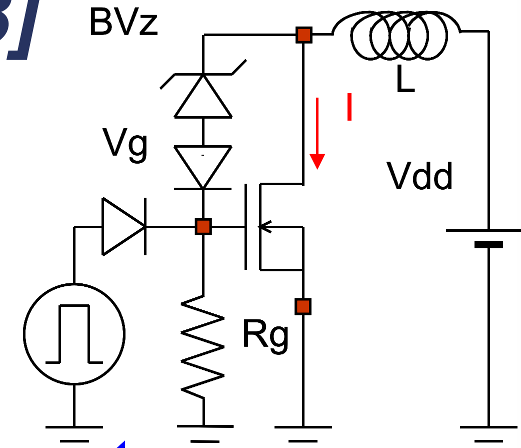
Device Overview

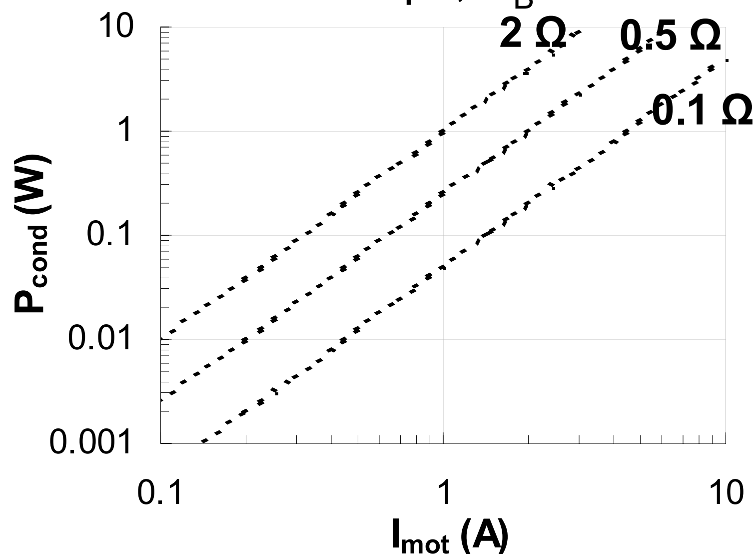
- Figures-of-Merit : R_{on}, V_{bd} and Q_{gd}
- Drain extended MOS (DeMOS)
- Lateral DMOS (LDMOS)
- (quasi)-Vertical DMOS (VDMOS)
- Silicon limit and benchmarking
- Lateral IGBT (L-IGBT)
- SCR's and Thyristors
- Trenchmos
- …

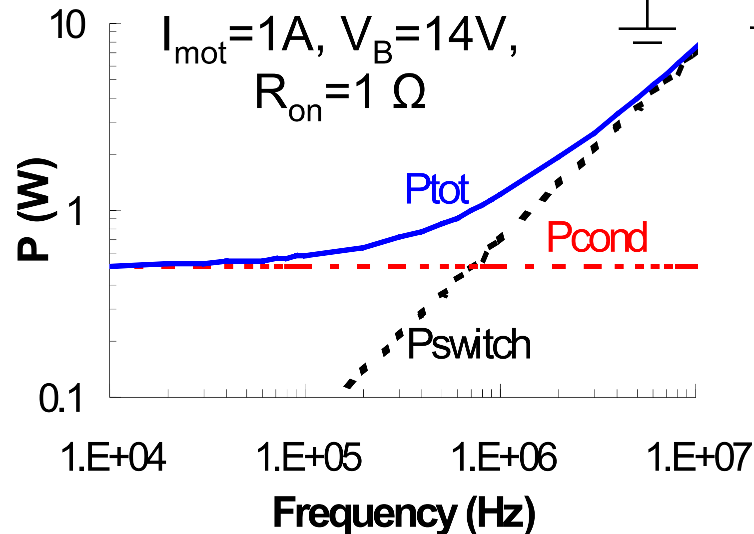
Conduction and switching loss

- R_{on} of a switch must be as low as possible → reduce power dissipation [2,3]

$$P_{tot} = \frac{t_{on}}{t} . I_{mot}^2 . R_{on} + \frac{t_r + t_f}{2t} . V_B . I_{mot}$$



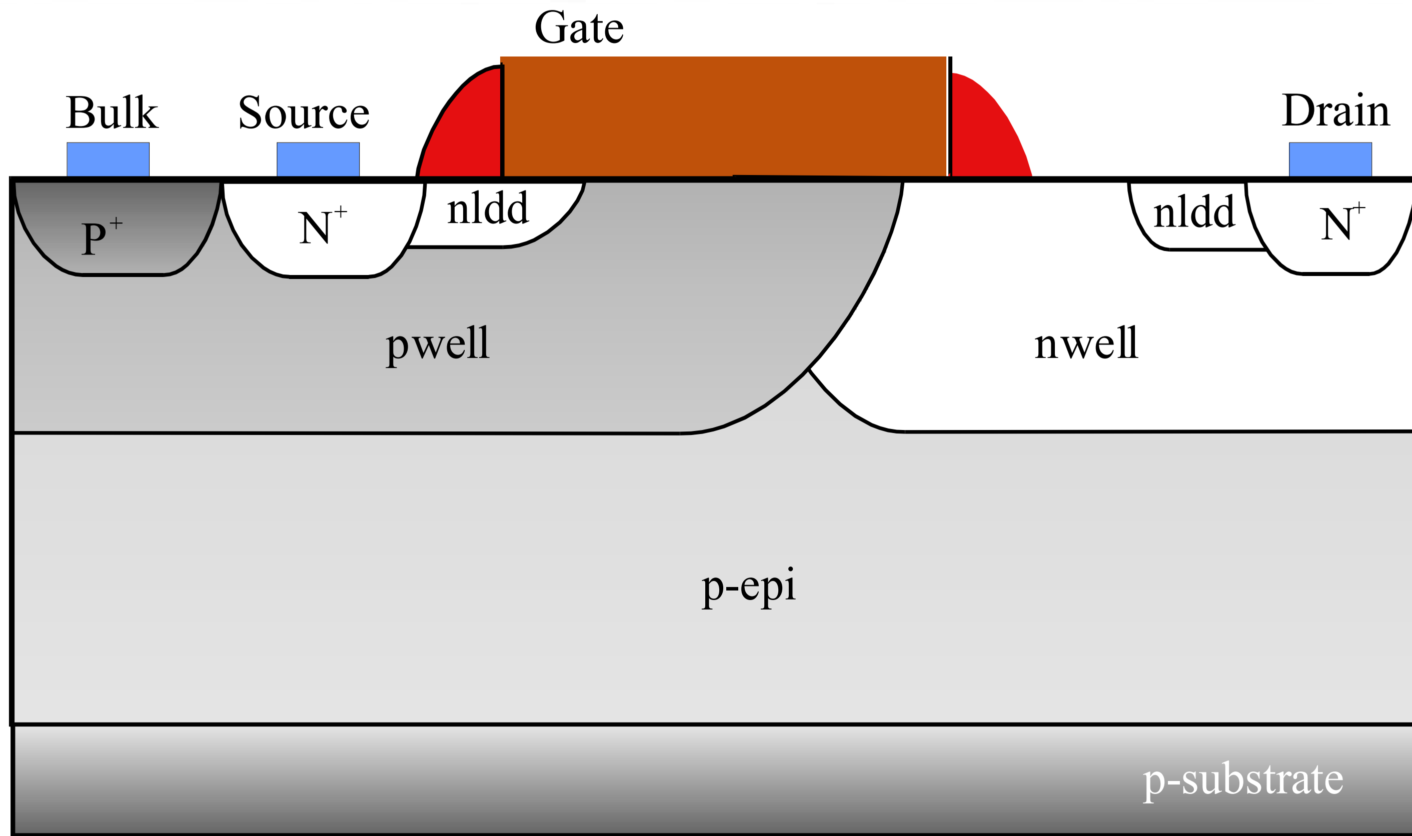




Switching loss

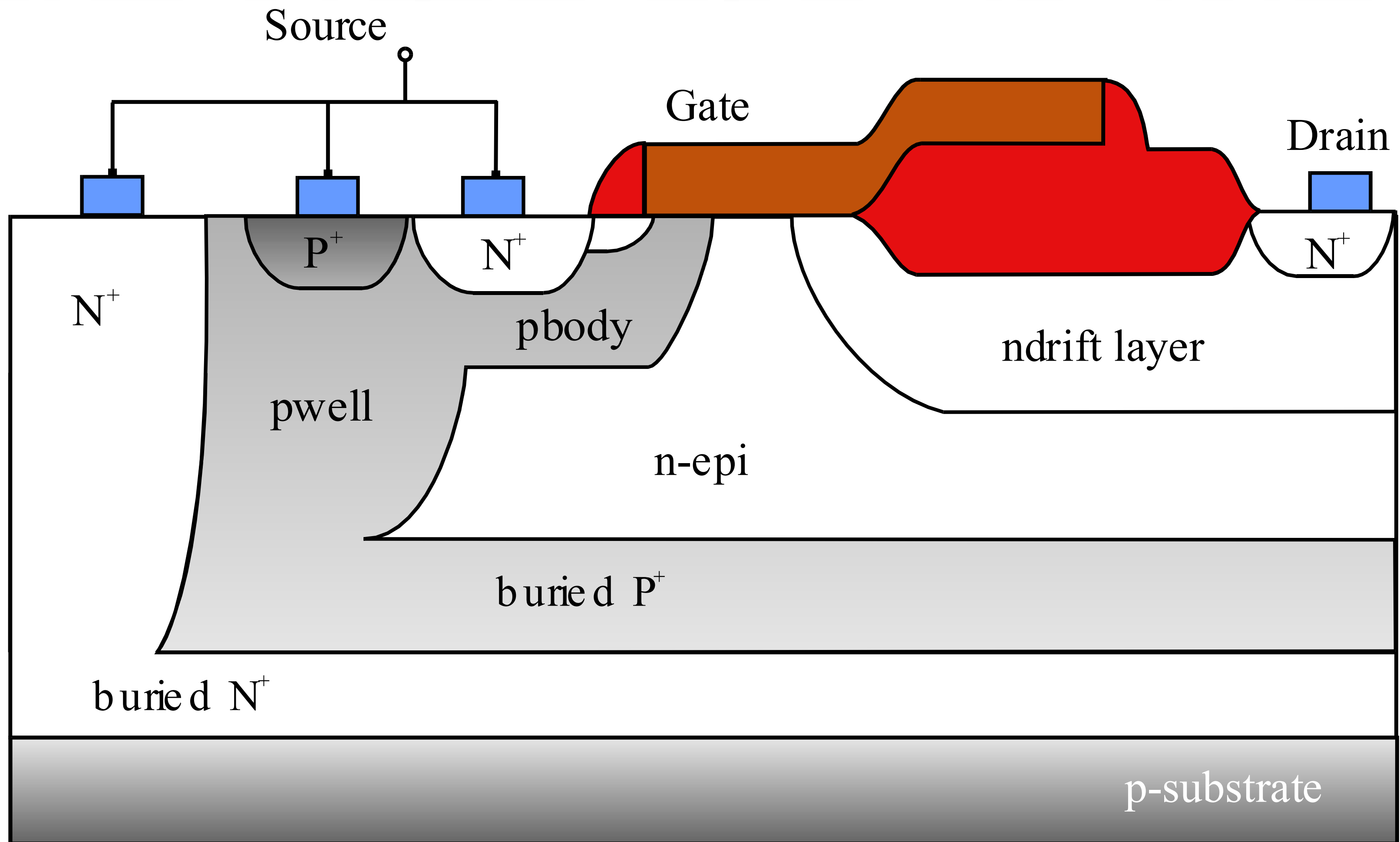
- ***Miller charge and capacitance***
  - Require energy from the gate driver
  - Delays a fast turn-on →enlarges the dissipation
- ***Q_{gd} must be as low as possible in order to reduce switching losses***
- ***Ron* Q_{gd} is an important figure of merit***

DEMOS



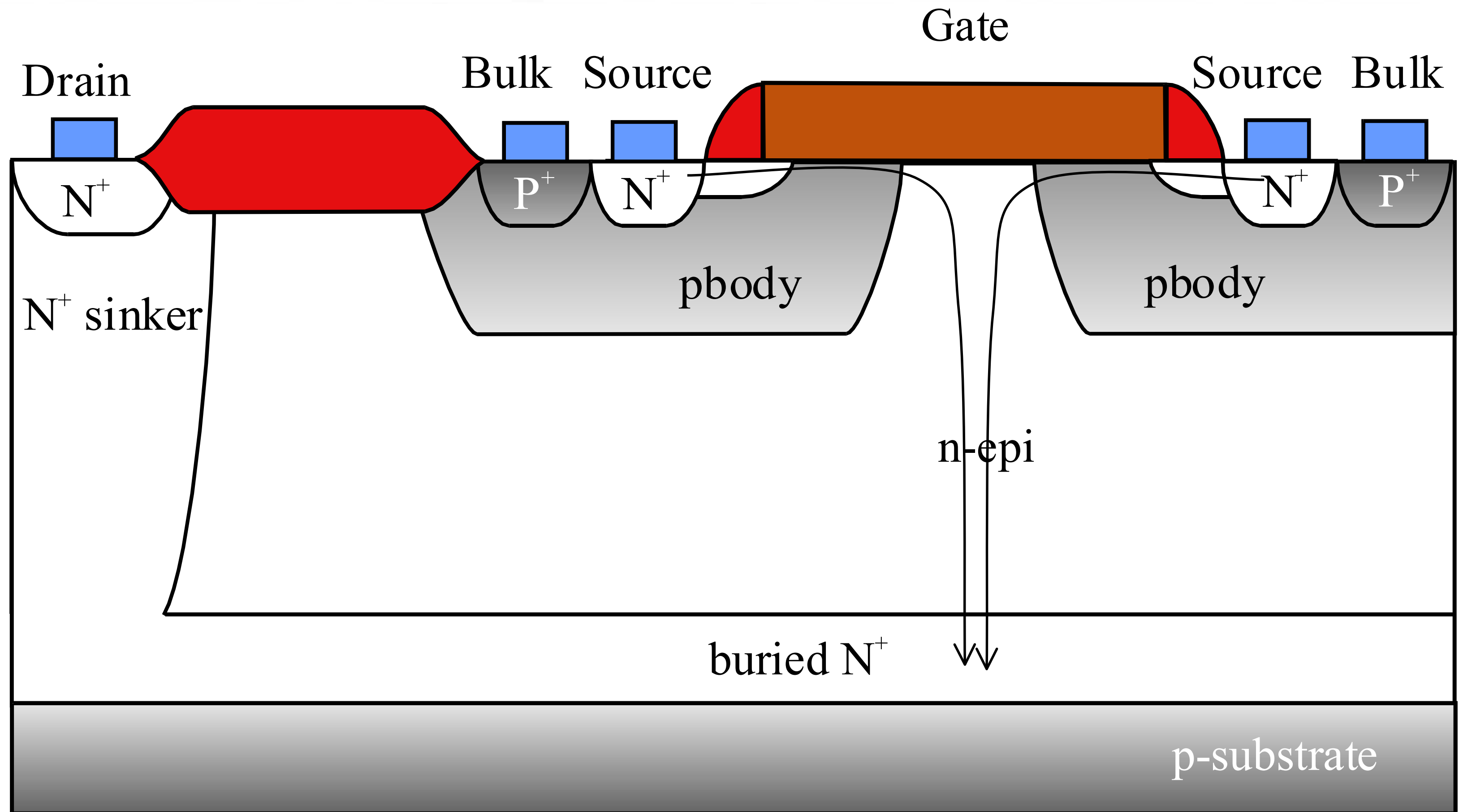
Easy to integrate.

Resurf LDMOS



Floating RESURF LDMOS in n-epi

Q-VDMOS

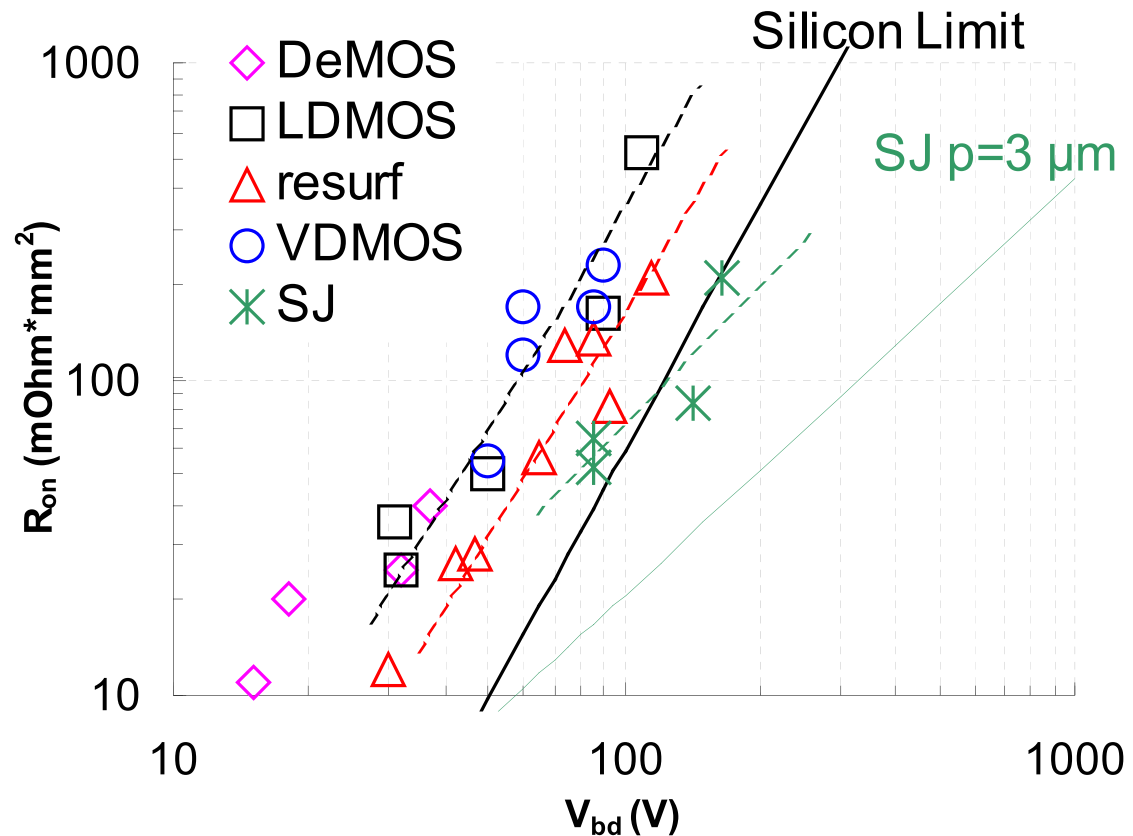


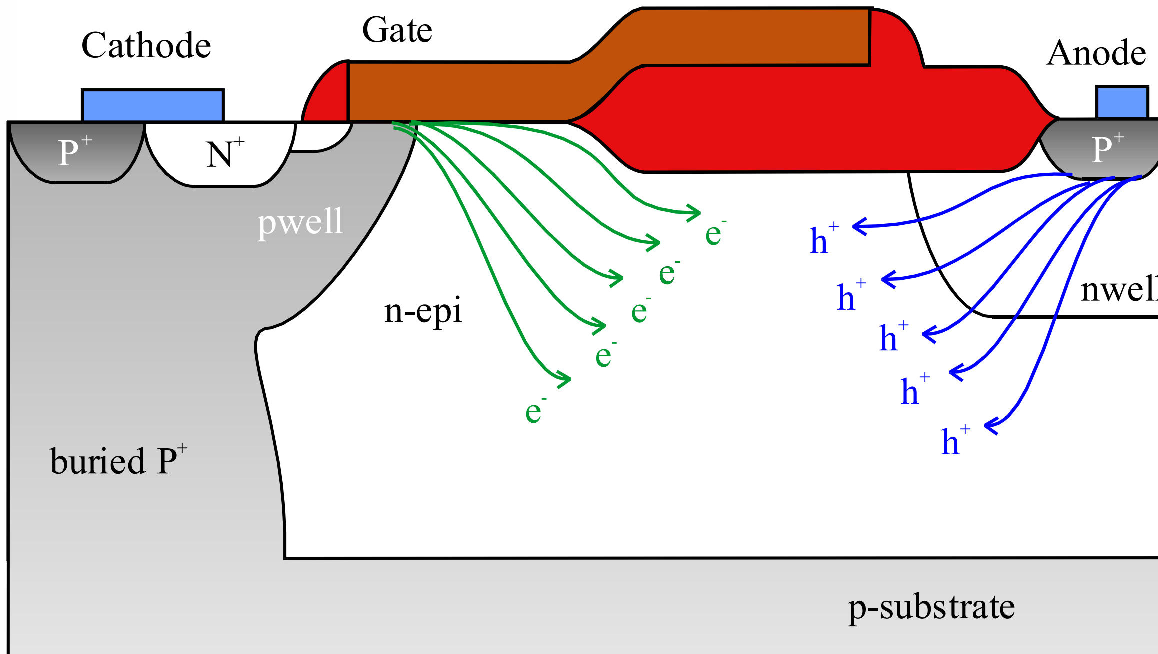
- VDMOS: V_{bd} not scalable, depends on technology
- JFET principle protects the gate ⇒ ROBUST

Silicon limit & Benchmarking

- *Silicon limit expresses the relation between Ron and V_{bd} for an ideal vertical MOS [42]*

$$R_{on} \sim V_{bd}^{2.5}$$





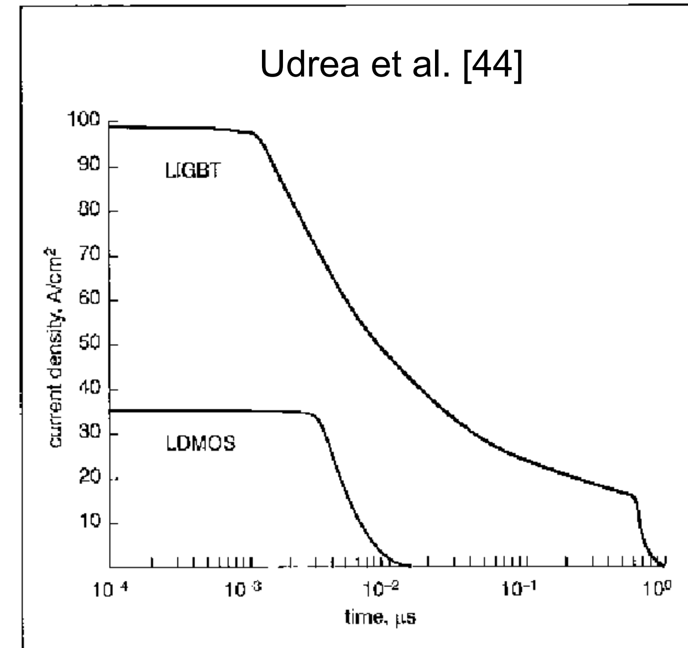


Fig. 9 Turn-off characteristics for 600 V SOI LDMOSFET and LIGBT

Conductivity Modulation ⇒ R_{on} drops

On-State: injection of holes & electrons results in an excess of mobile carriers: "Conductivity Modulation"

Turn-Off: slow due to excess of minority carriers in n-epi [43-45]

Overview

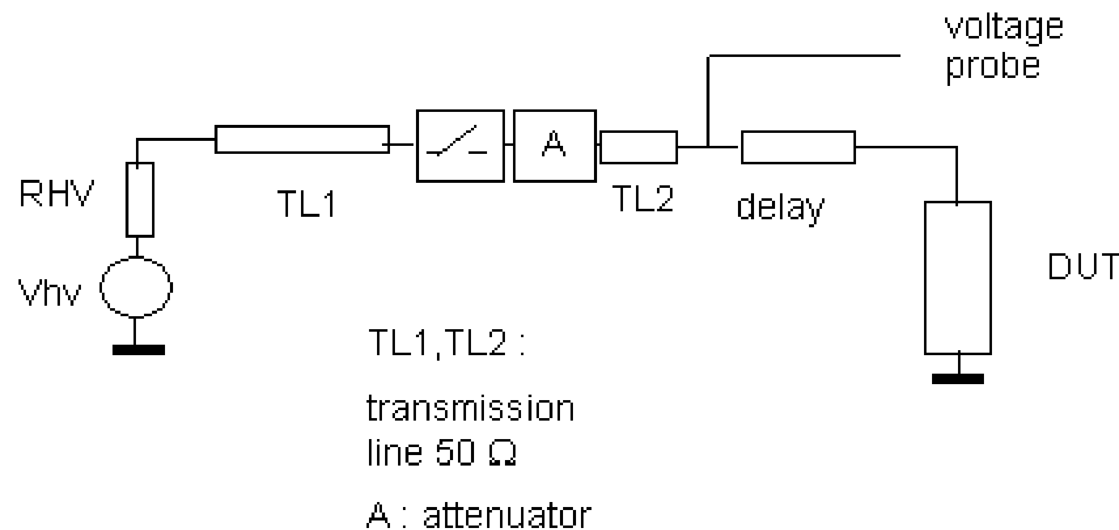
- Introduction
- Q&R Specifications
- Device Overview
- **Reliability Measurements and Analysis Techniques**
- Reliability Problems in Smart Power Technologies
- Conclusions

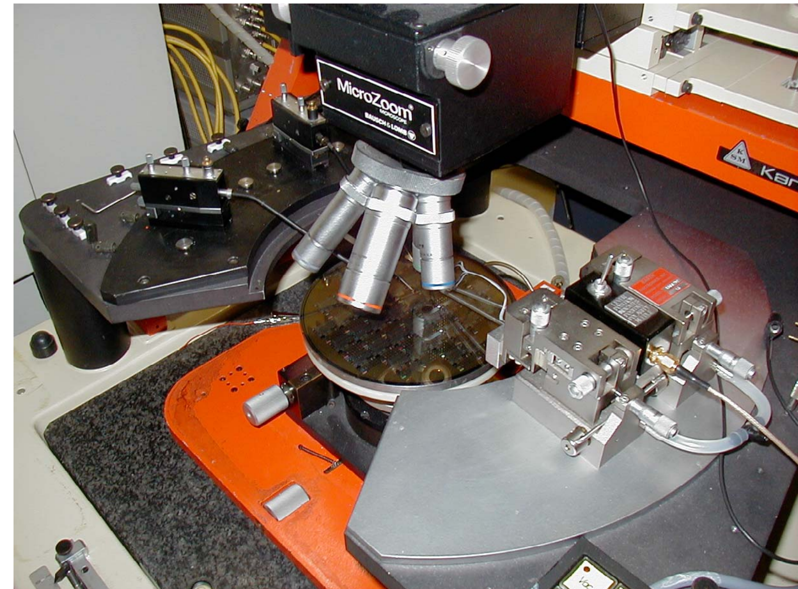
Reliability measurements & Techniques

- Transmission line pulsing (TLP)
- Transmission Interferometric Mapping (TIM)
- Energy Capability (EC)
- Charge Pumping (CP)
- CV measurements

Transmission Line Pulsing

- *Measure the npn turn-on without self-heating of the device. Apply a sufficiently short (5 ns – 200 ns) power pulse [46]*

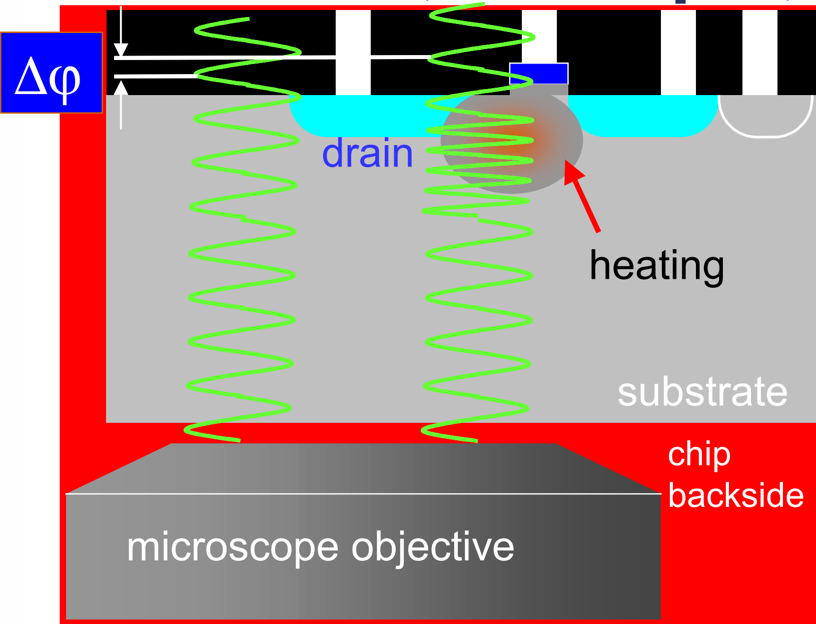




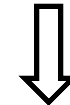
- *On wafer and/or packaged devices*

Transient Interferometric Mapping

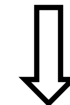
IR laser, λ=1.3 μm, transparent for silicon [47-49]



Temperature and carrier concentration variation



Change in refractive index of the silicon

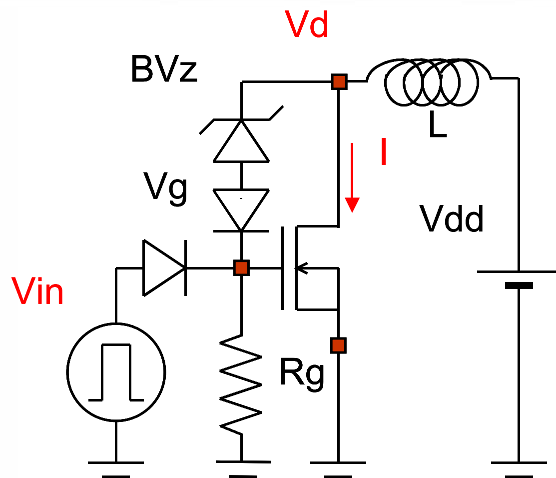


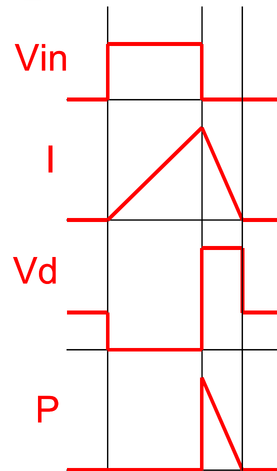
Change in phase shift Δφ

$$\Delta\varphi(t) = \frac{4\pi}{\lambda}\int_{o}^{L}\left(\frac{dn}{dT}\Delta T(z,t) + \left(\alpha_n \Delta n(z,t) + \alpha_p \Delta p(z,t)\right)\right)dz$$

Spatial resolution : 1.5 μm, time resolution : 3 ns.

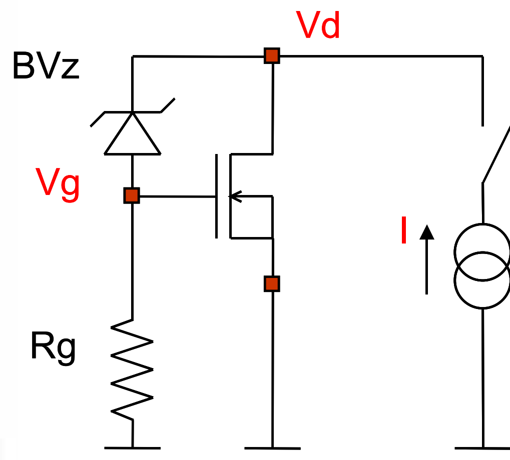
Energy Capability (1)

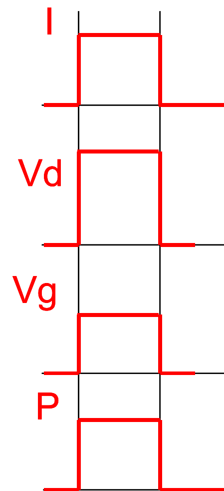




Clamped inductive switching (CIS) : power level and time cannot be controlled independently.

CIS and RPP yield the same results [41] (theory+exp)

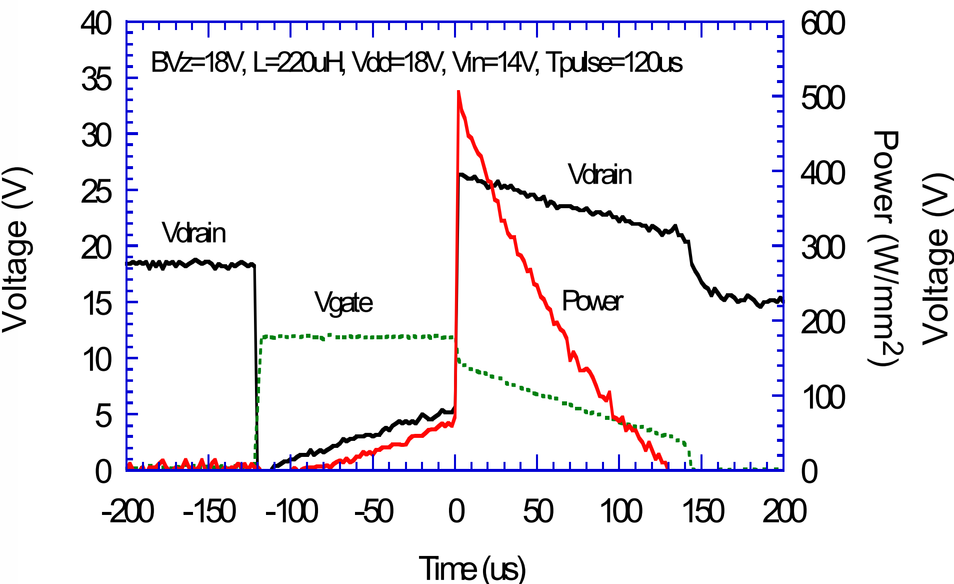


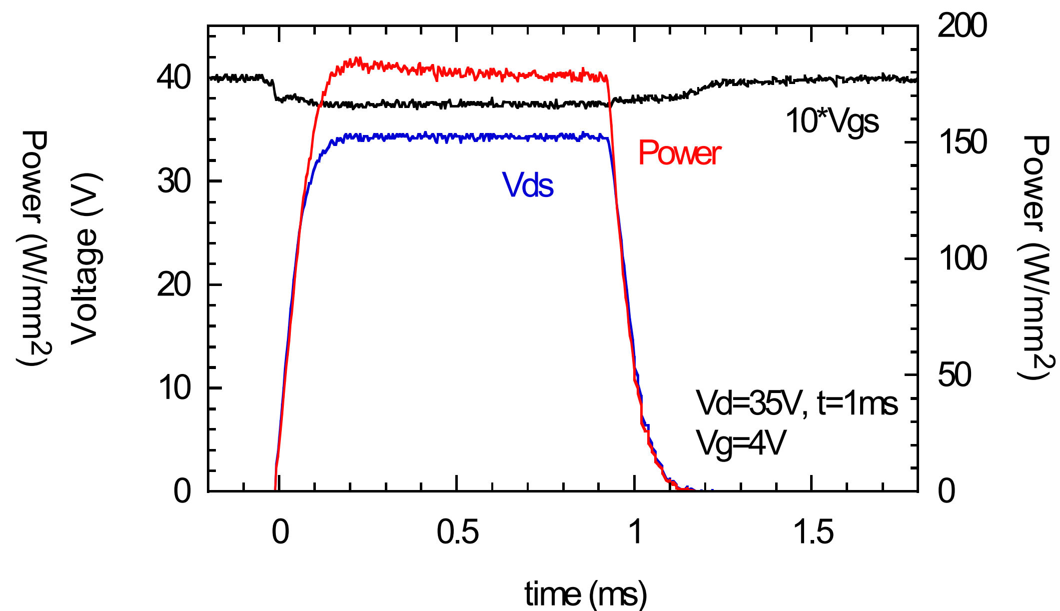


Rectangular power pulsing (RPP) : independent control of Power and time.

Energy Capability (2)

- *For CIS, the power pulse shape is triangular*
- *For RPP, the power pulse is rectangular*



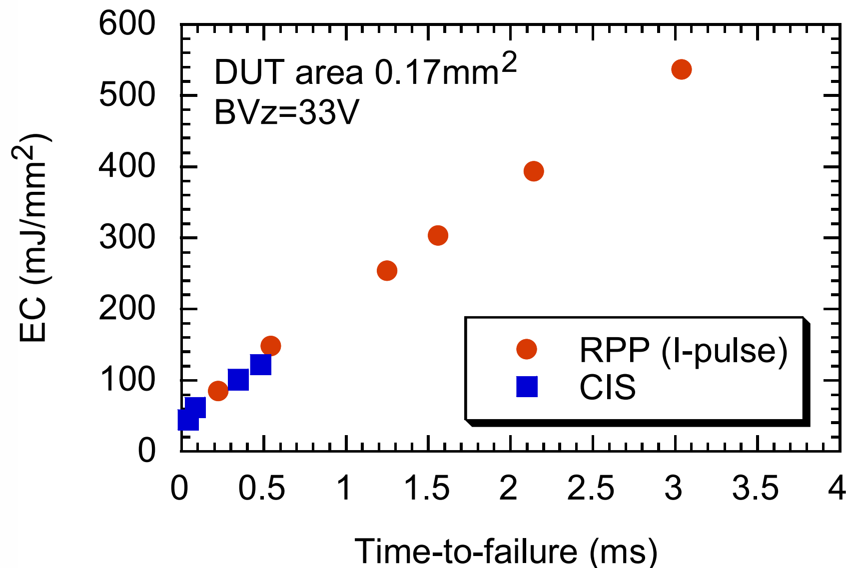


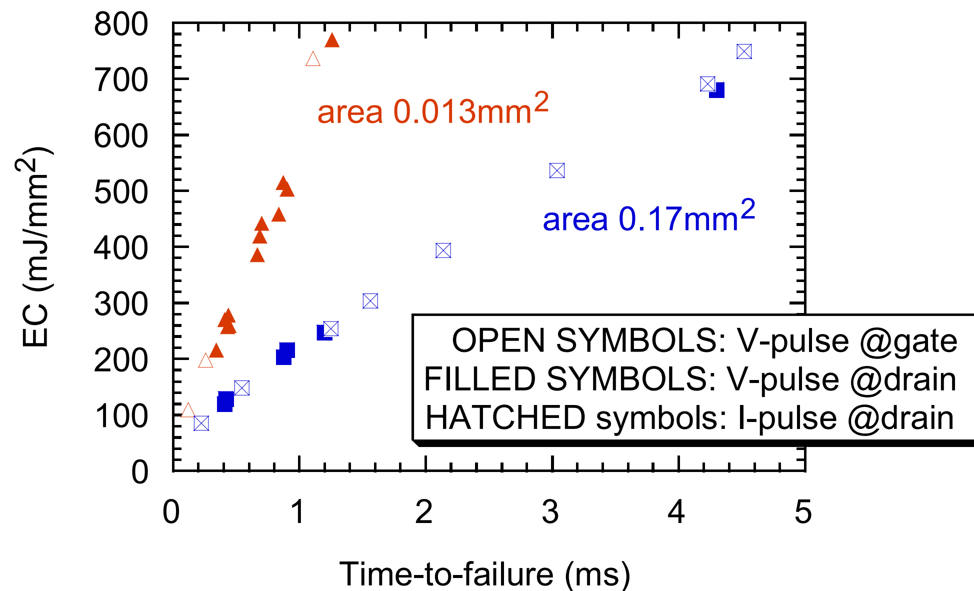
Energy Capability (3)

- ***Theoretical analysis [41]***

$$P_{0,rect} \le P_{0,tr} \le \frac{3}{2} P_{0,rect}$$

$$EC_{rect} \le EC_{tr} \le \frac{9}{8} EC_{rect}$$

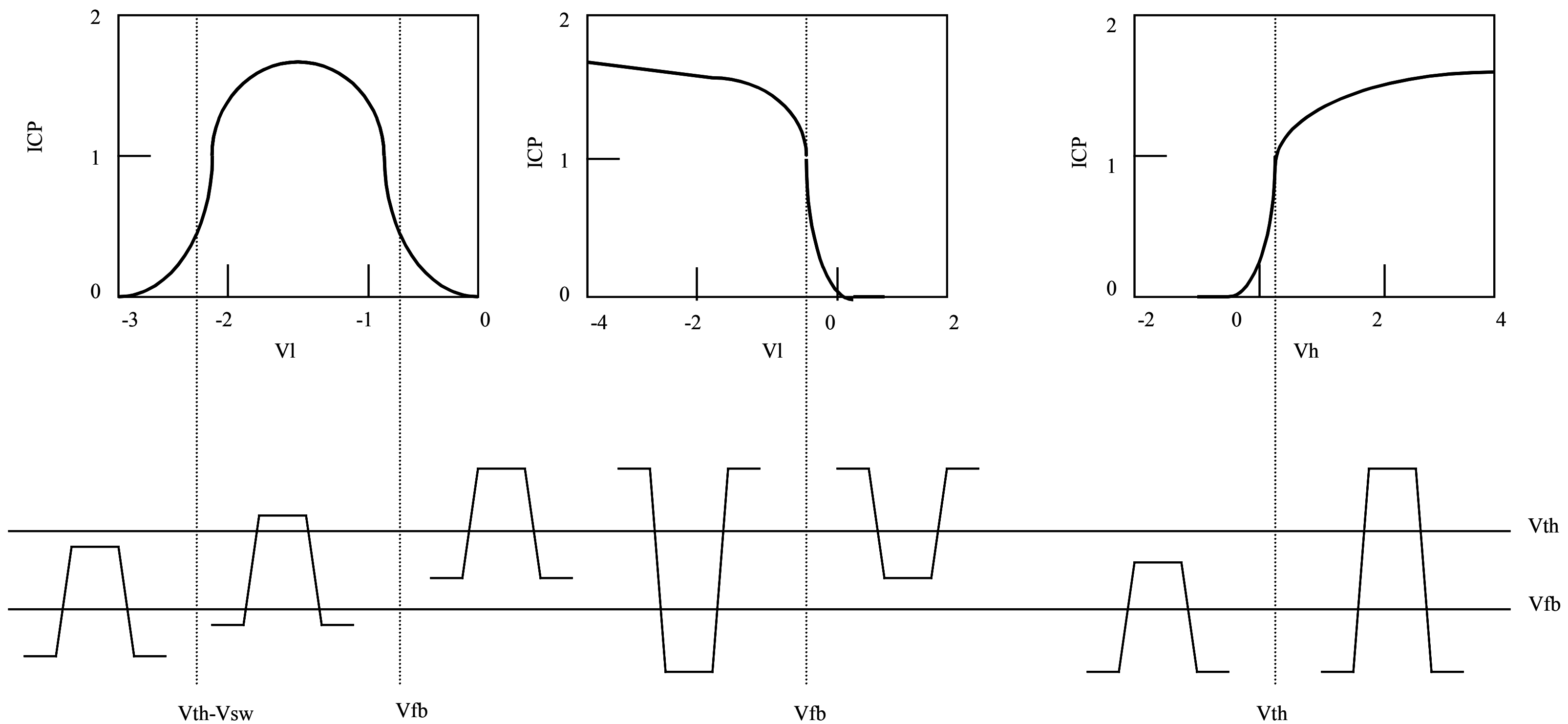




Charge Pumping (1)

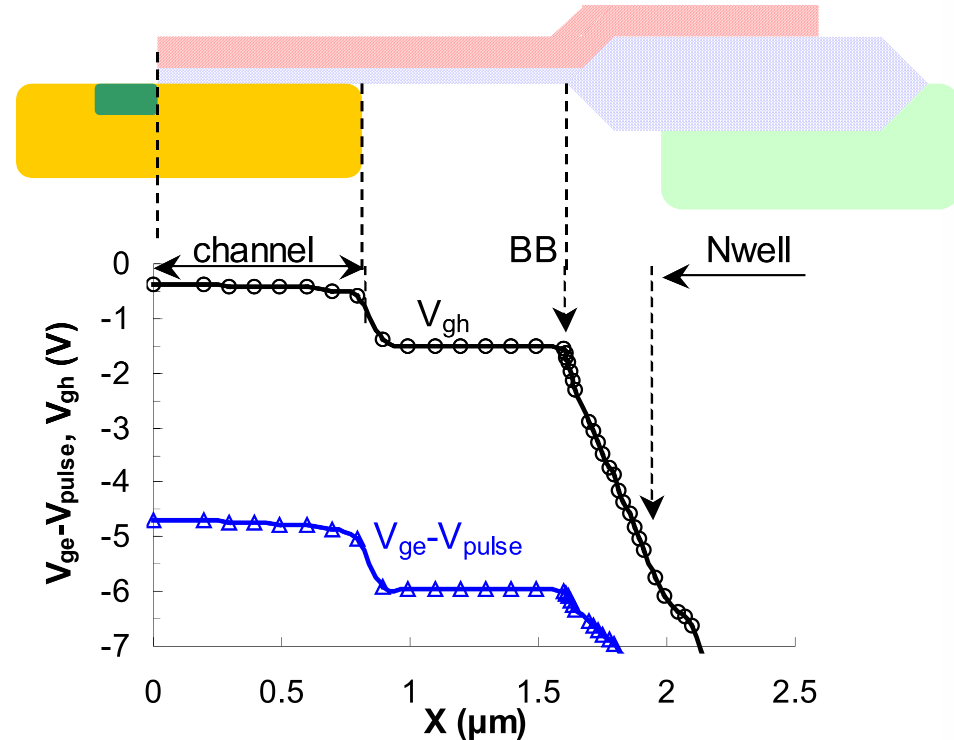
- *To locate and quantify the N_{it} generation [50,51]*

  variable base   variable amplitude



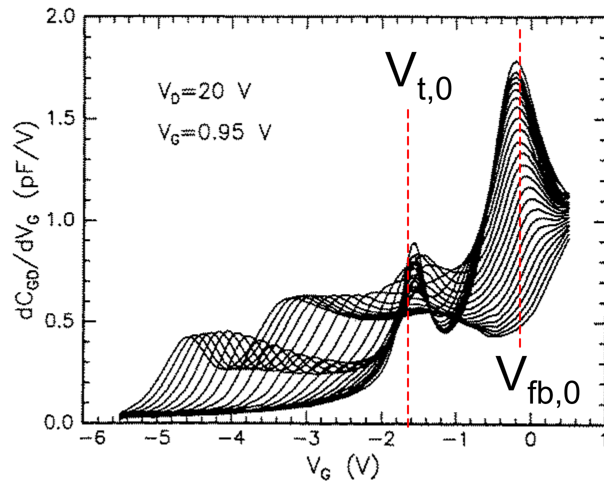
Charge Pumping (2)

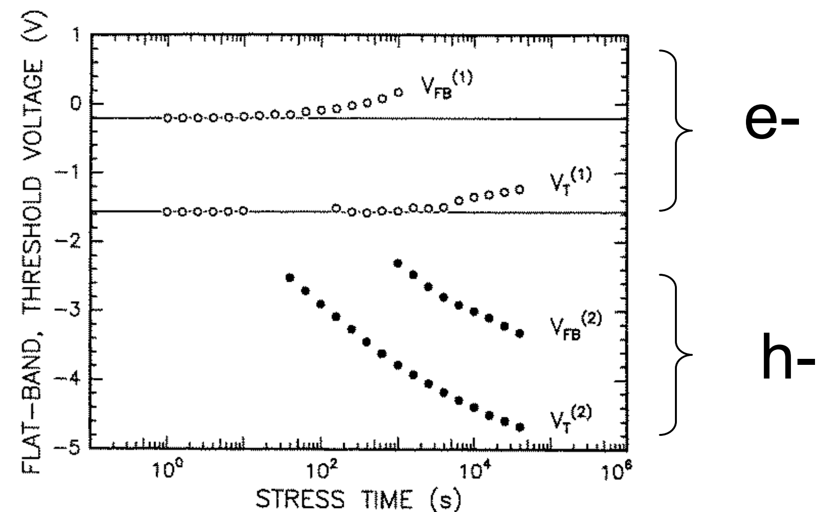
- ***V_{th} (V_{g_e}) and V_{fb} (V_{g_h}) depend on***
  - frequency of the pulse
  - N_d, t_{ox} and N_{ot} at the Si/SiO_2 interface
- **Region that can be probed is dependent on V_{pulse}, hence on t_{ox} thin gate and on N_d.**
- **Very well applicable to DeMOS, LDMOS and VDMOS [19-21]**



CV measurements

- *Assessment of charge trapping in LDMOS using CV measurements [10,16].*
- *C_{gd} monitored at 1 MHZ.*





- *Information on charge trapping is extracted.*
- *Difficult to pinpoint location of trapping.*

Overview

- Introduction
- Q&R Specifications
- Device Overview
- Reliability Measurements and Analysis Techniques
- **Reliability Problems in Smart Power Technologies**
- Conclusions

Reliability Problems in Smart Power

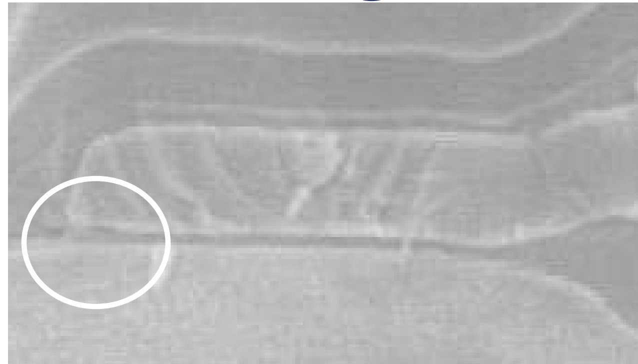
- *DC hot carrier*
- *AC hot carrier (switching of a load)*
- *Electrical SOA (parasitic bipolar turn-on)*
- *Thermal SOA (energy capability)*
- *Simulation of thermal effects*

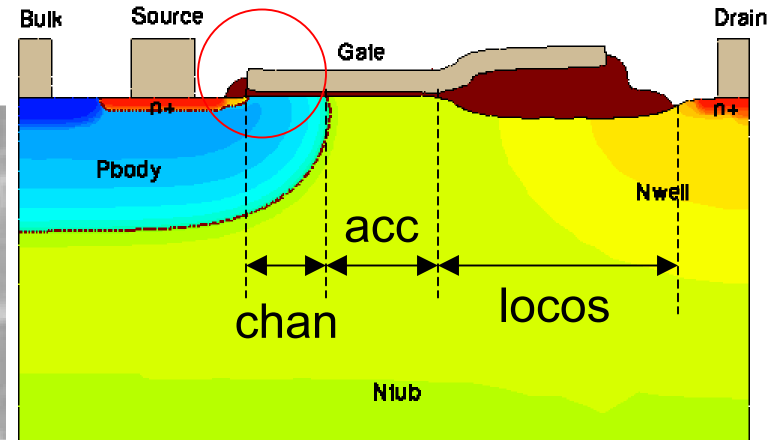
Reliability Problems in Smart Power

- DC hot carrier
- AC hot carrier (switching of a load)
- Electrical SOA (parasitic bipolar turn-on)
- Thermal SOA (energy capability)
- Simulation of thermal effects

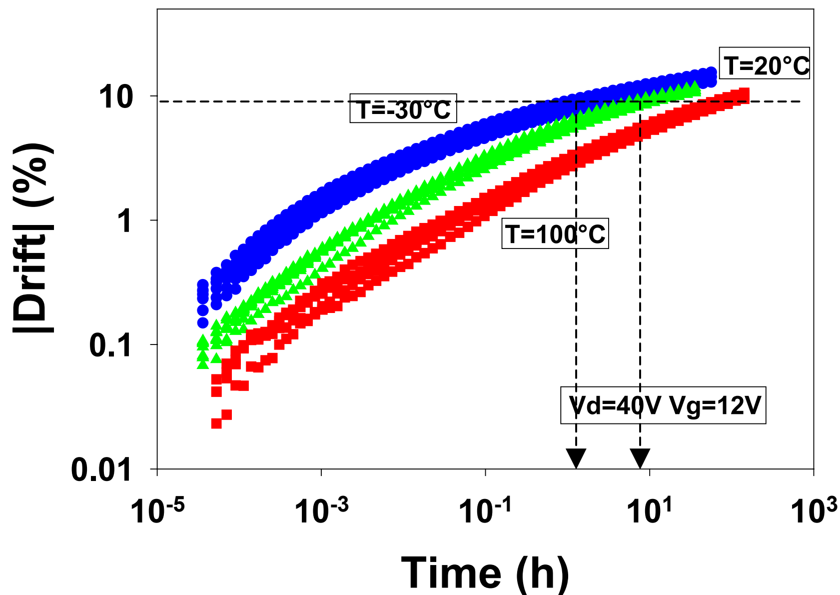
DC hot carrier (1)

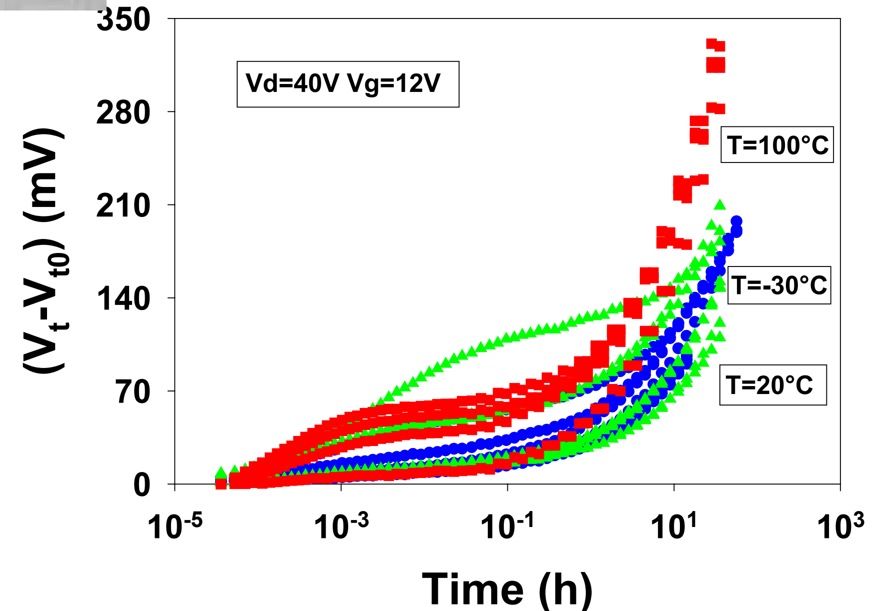
- ***40V LDMOS 12V gate***





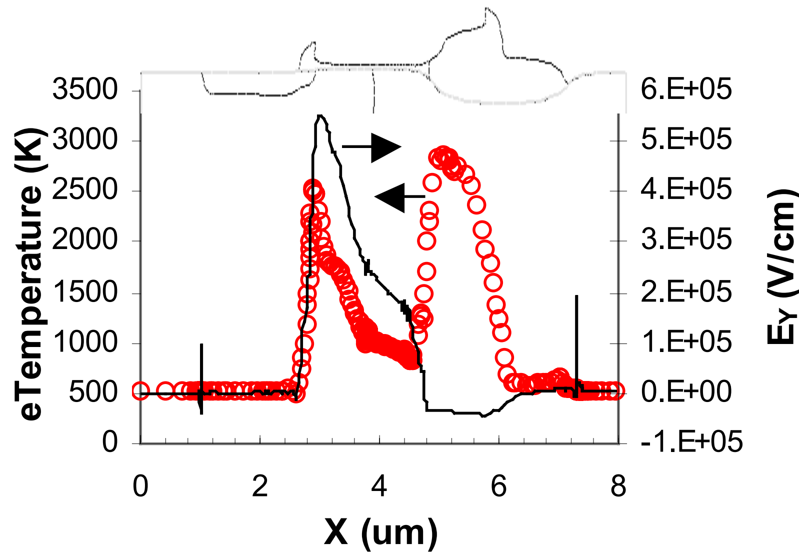
Shift in Ron

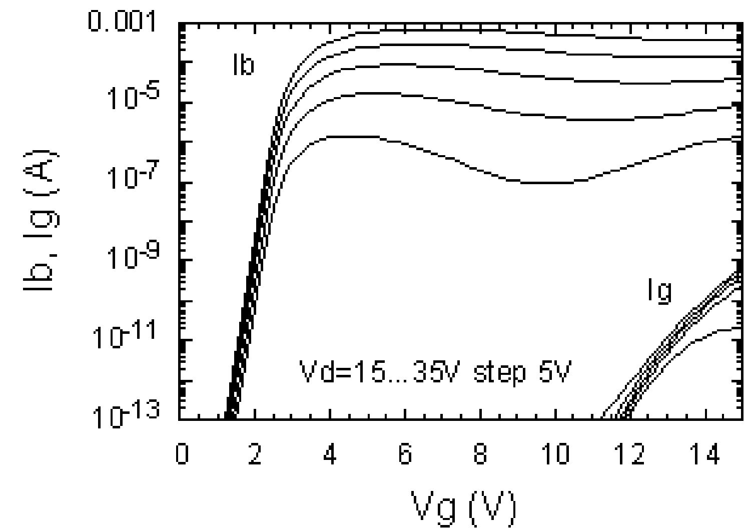




DC hot carrier (2)

- *Source Side Injection (SSI) at high V_{gs}[52,53]*

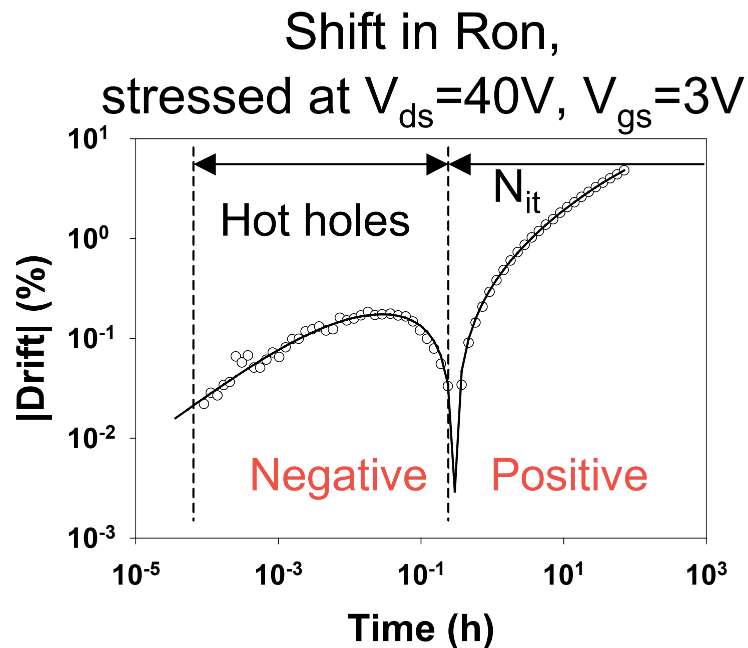


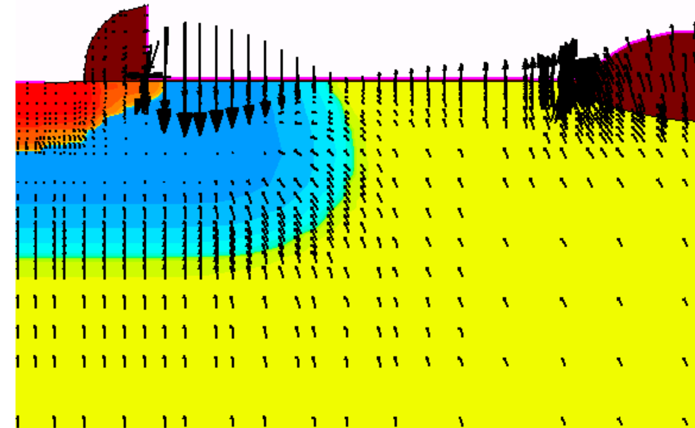


- *nLDD dose is too low for self-aligned p-body dose : E-field build-up at the source*
- *Carrier Injection at the source → V_{th} shift, independent of V_{ds}.*

DC hot carrier (3)

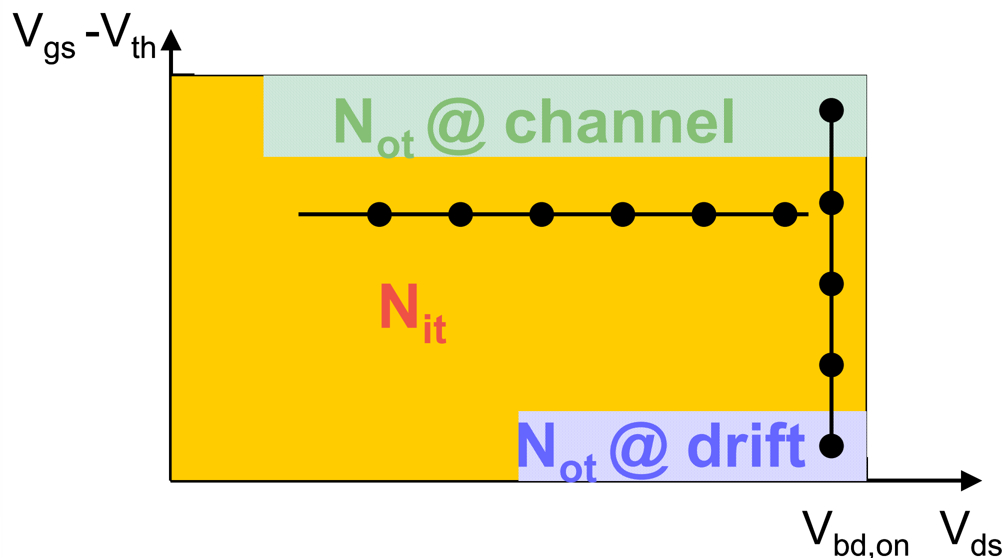
- ***Hole Injection at low V_{gs} and high V_{ds}.***
- ***Occurs at birds beak (E-field direction).***



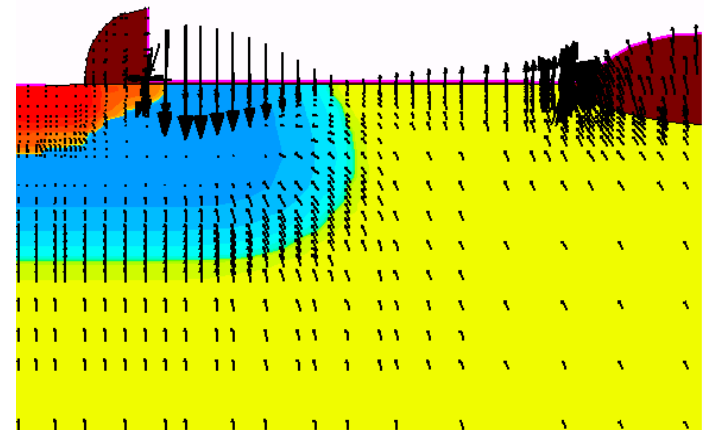


DC hot carrier (4)

- ***V_{gs}/V_{ds} dependency of the degradation***
  - Different degradation mechanisms can occur.
  - Dependent on device specifics (layout, doping, …)
  - At which conditions to stress for worst case ?

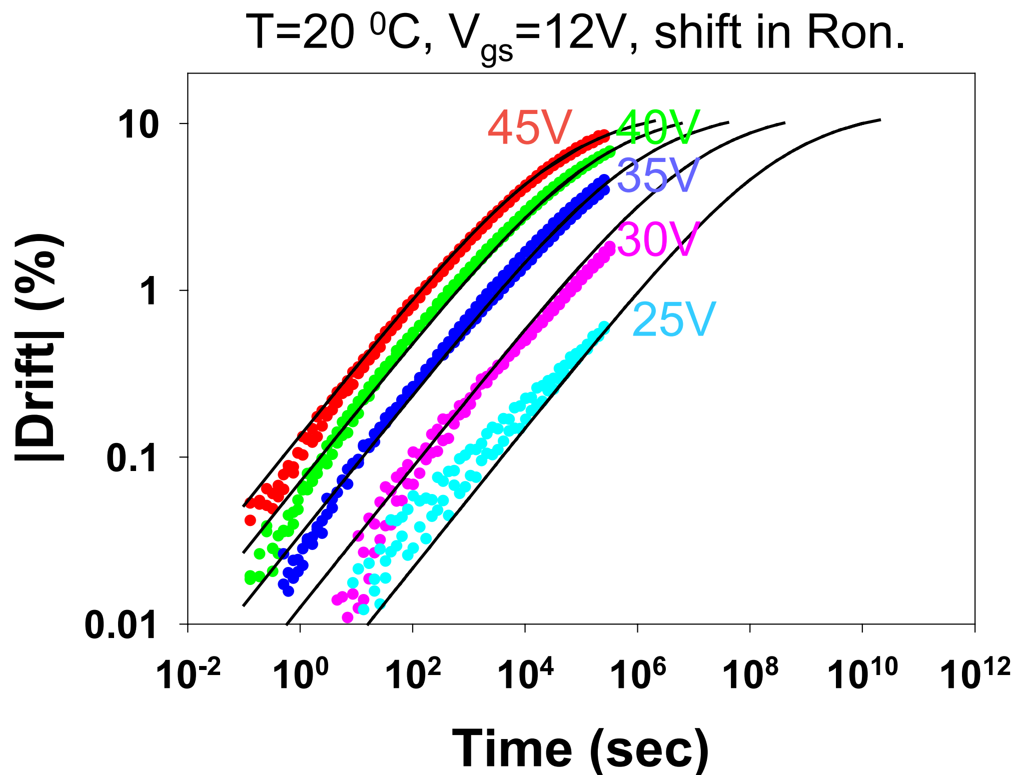


Electric field @ V_{gs}=6V ; V_{ds}=40V



DC hot carrier (5)

- ***V_{ds} dependency : simultaneous fit***



$$\frac{\Delta P}{P_0} = \frac{C_1 \cdot \left[t \cdot \frac{I_d}{W} \left(\frac{I_{sub}}{I_d} \right)^{\varphi_{it}/\varphi_i} \right]^n}{1 + C_2 \cdot \left[t \cdot \frac{I_d}{W} \left(\frac{I_{sub}}{I_d} \right)^{\varphi_{it}/\varphi_i} \right]^n}$$

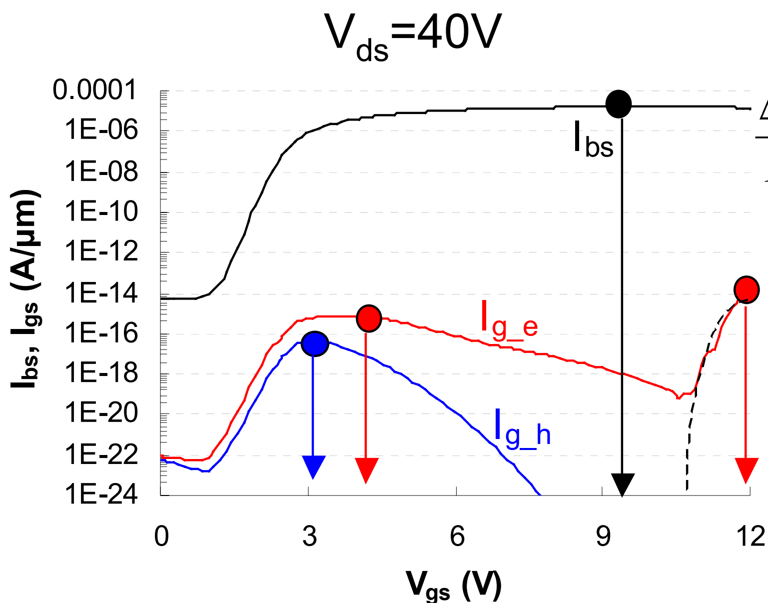
I_{ds}, I_{sub} from experiments

C_1, C_2, φ_{it}/φ_i, n : fitting parameters

3.5 eV (e) 1.3 eV ~0.4-0.6

DC hot carrier (6)

- ***V_{gs} dependency : different mechanisms***
  - Low V_{gs} : hole injection at the birds beak
  - High V_{gs} : electron injection at source side
  - Intermediate V_{gs} : N_{it} formation



$$\frac{\Delta I_d}{I_{d0}} = \frac{C_1 \cdot \left(t \cdot \frac{I_d}{W_{eff}} \cdot \left(\frac{I_{sub}}{I_d} \right)^{\varphi_{it}/\varphi_i} \right)^n}{1 + C_2 \cdot \left(t \cdot \frac{I_d}{W_{eff}} \cdot \left(\frac{I_{sub}}{I_d} \right)^{\varphi_{it}/\varphi_i} \right)^n} + C_3 \cdot \left(t \cdot \frac{I_d}{W_{eff}} \cdot \left(\frac{I_{sub}}{I_d} \right)^{1 + \varphi_{it,h} \cdot \lambda_e / \varphi_i \cdot \lambda_h} \right)^m$$

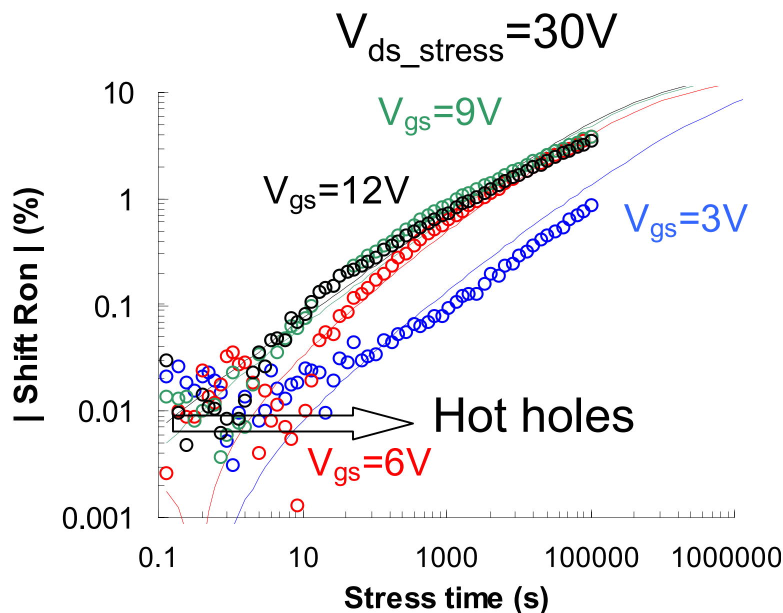
C_3 negative for hole trapping

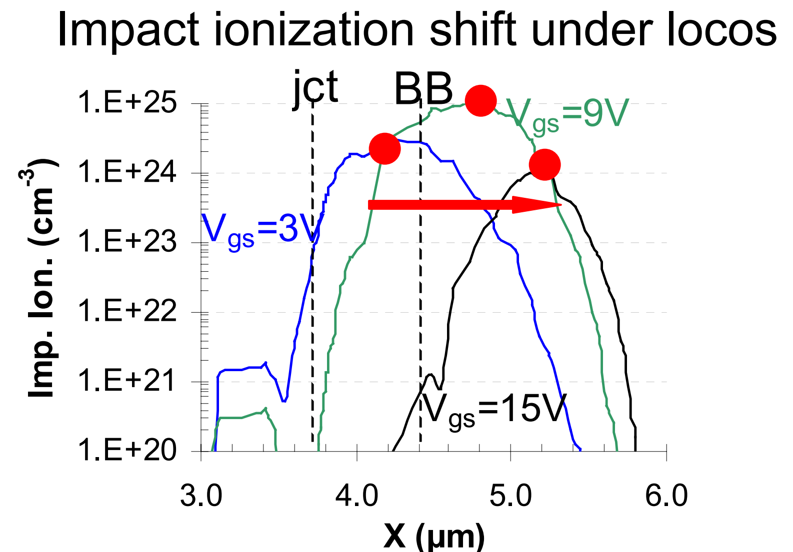
λ_e, λ_h : mean free paths of electrons and holes

$\varphi_{it,h}$: 4.2 eV

DC hot carrier (7)

- ***V_{gs} dependency :***
  - Difficult (if not impossible) to a priori know WC V_{gs}
  - Measure HC degradation for different V_{gs}
  - Difficult to fit different V_{gs} data simultaneously, fitting yields non-physical parameters ($\varphi_{it}/\varphi_{I} < 1$)

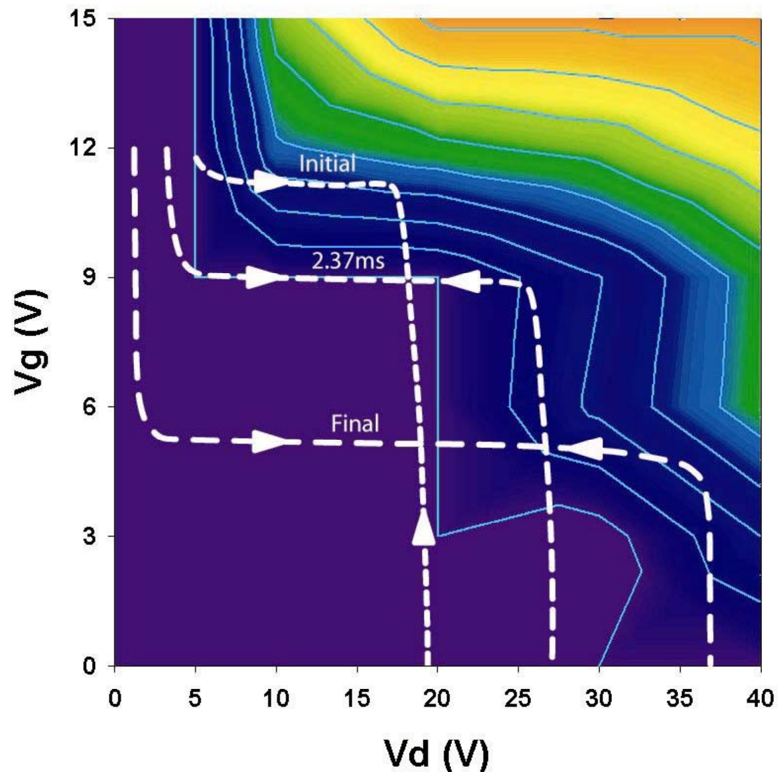




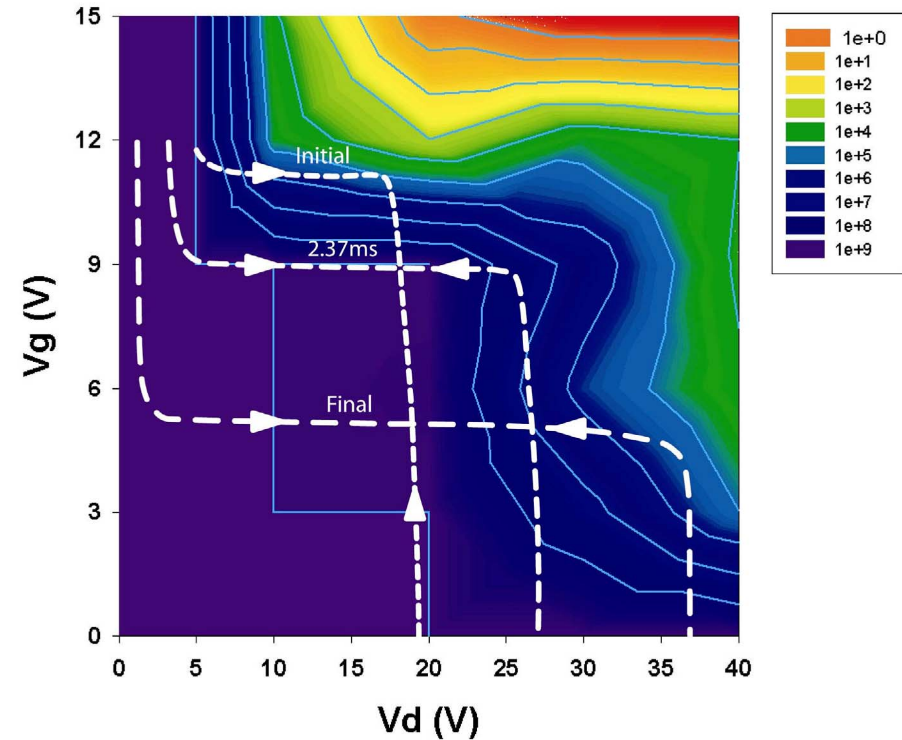
DC hot carrier (8)

- ***LDMOS 40V in a 0.7 µm smart power techno***

T=25 °C

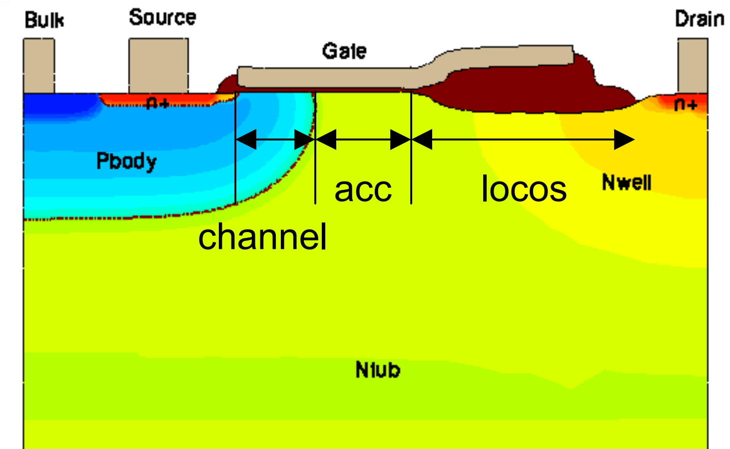


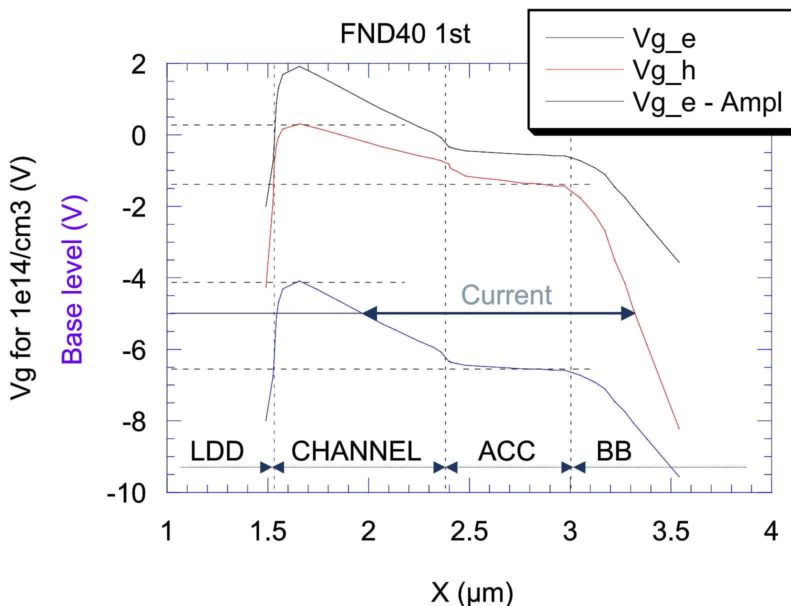
T=-30 °C

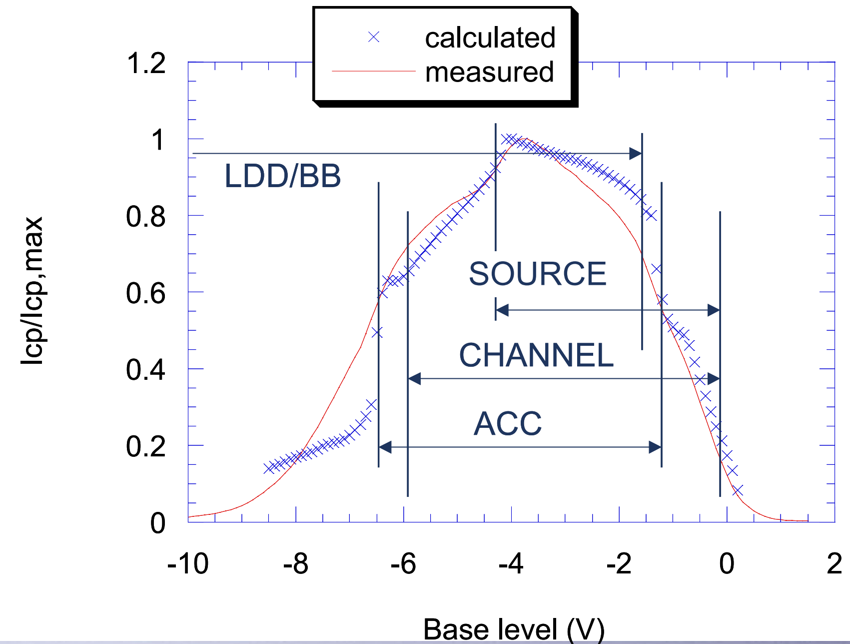


Charge Pumping (1)

- ***40V LDMOS***
- ***V_{ge} and V_{gh} as from TCAD***
- ***Uniform N_{it} in thin oxide***

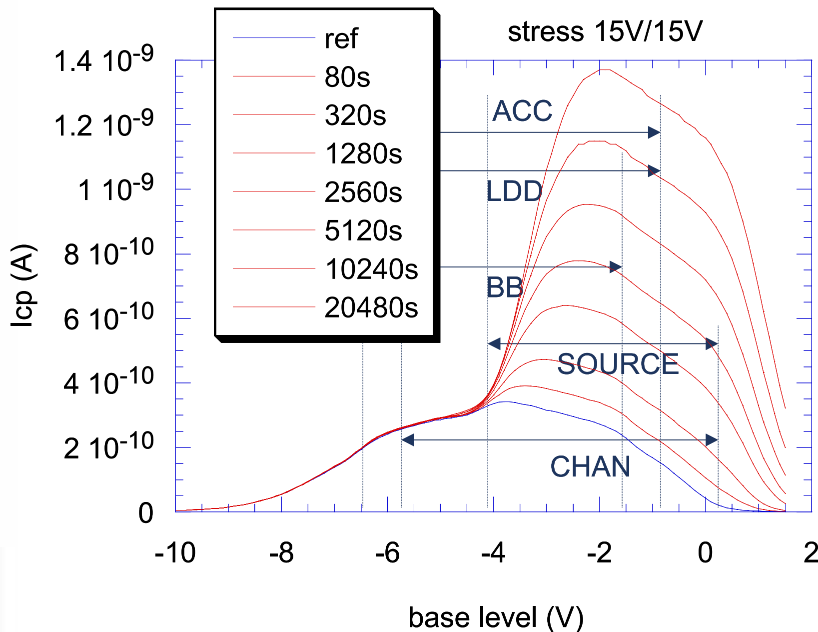


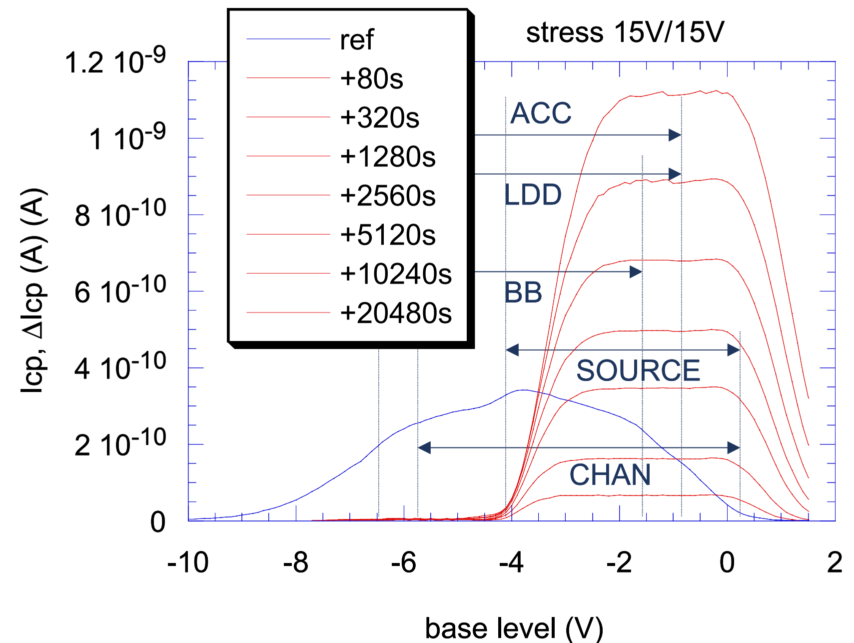




Charge Pumping (2)

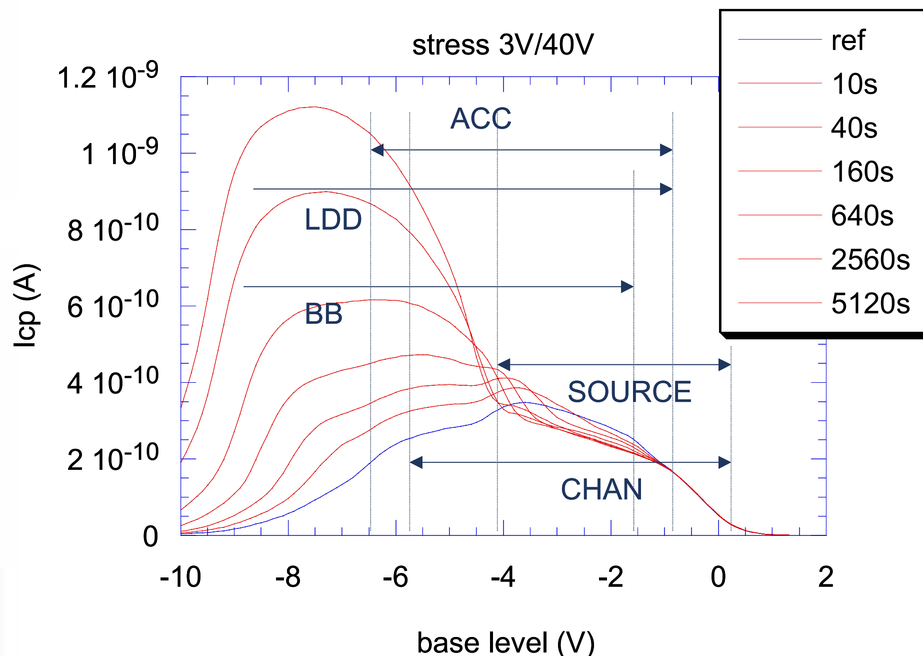
- ***LDMOS stressed at $V_{ds}=V_{gs}=15V$ (low V_{ds}, high V_{gs}) → N_{it} formation at the source.***

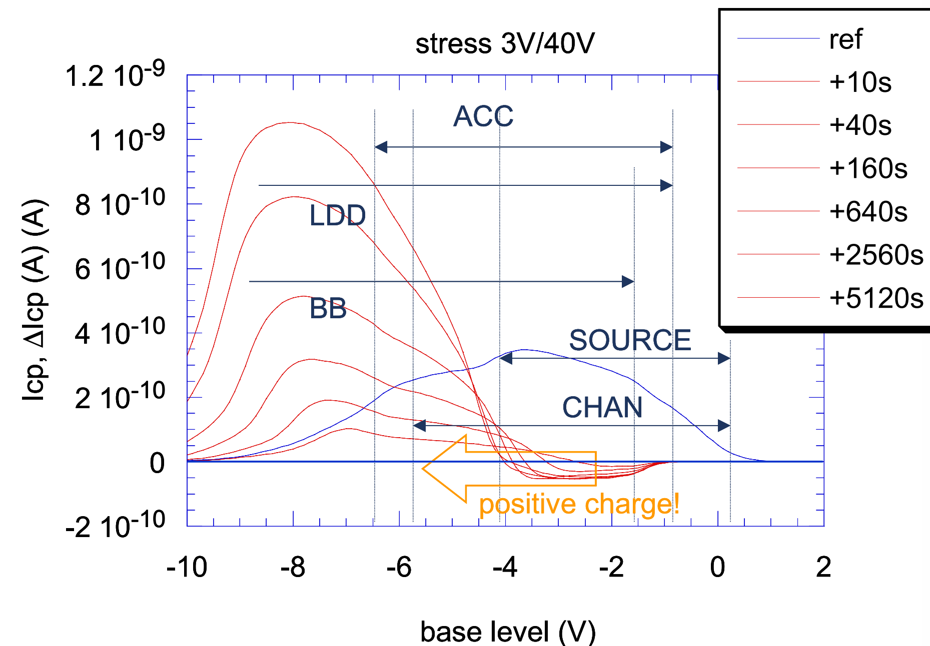




Charge Pumping (3)

- ***LDMOS stressed at V_{ds}=40 V_{gs}=3V (low V_{gs}, high V_{ds}) → N_{it} formation in accumulation region or under the birds beak.***



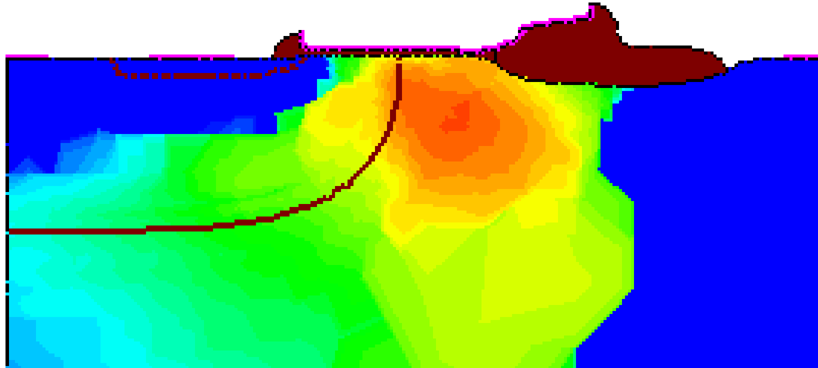


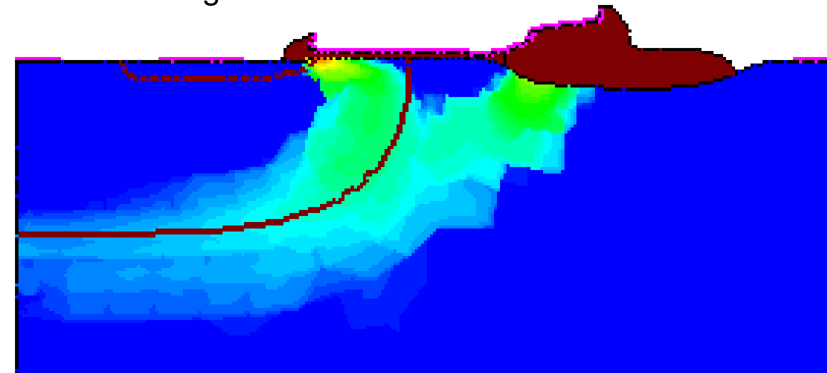
TCAD verification on 40V LDMOS

V_{gs}=3V, V_{ds}=40V

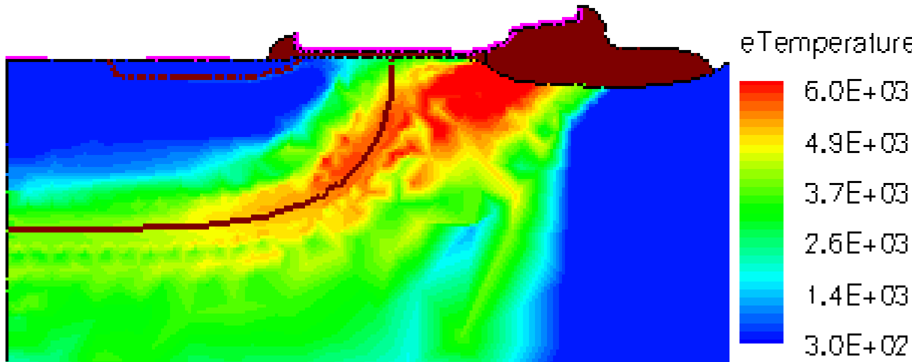
V_{gs}=15V, V_{ds}=15V

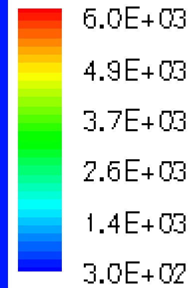
Impact ionization

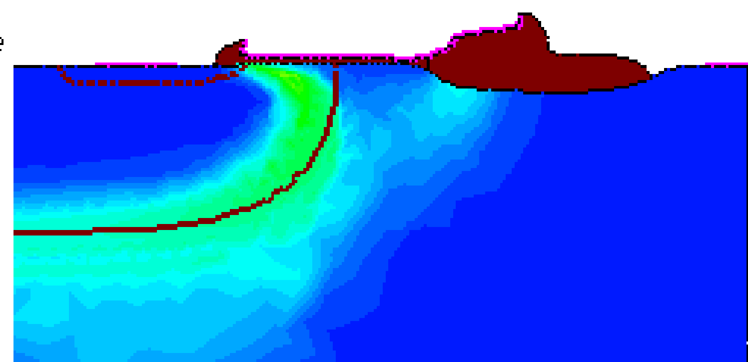




Electron Temperature

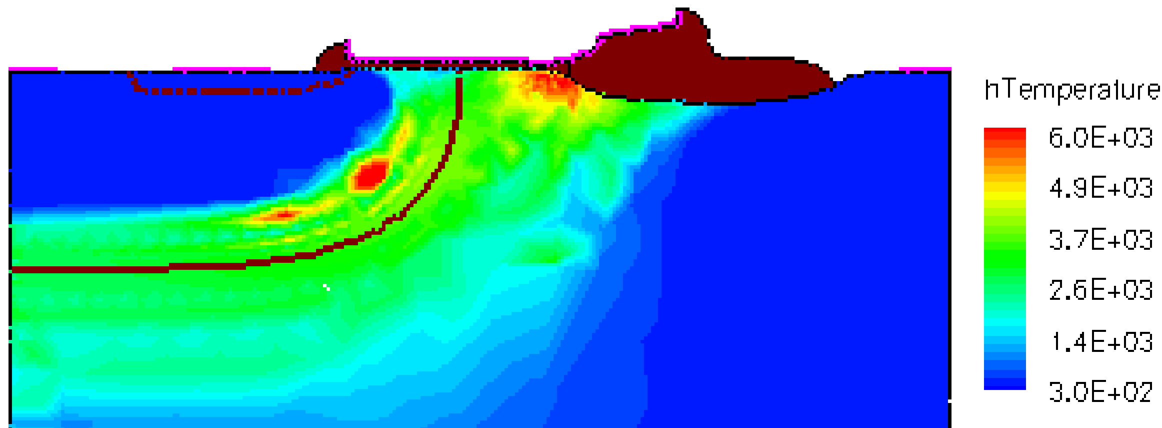






TCAD verification on 40V LDMOS

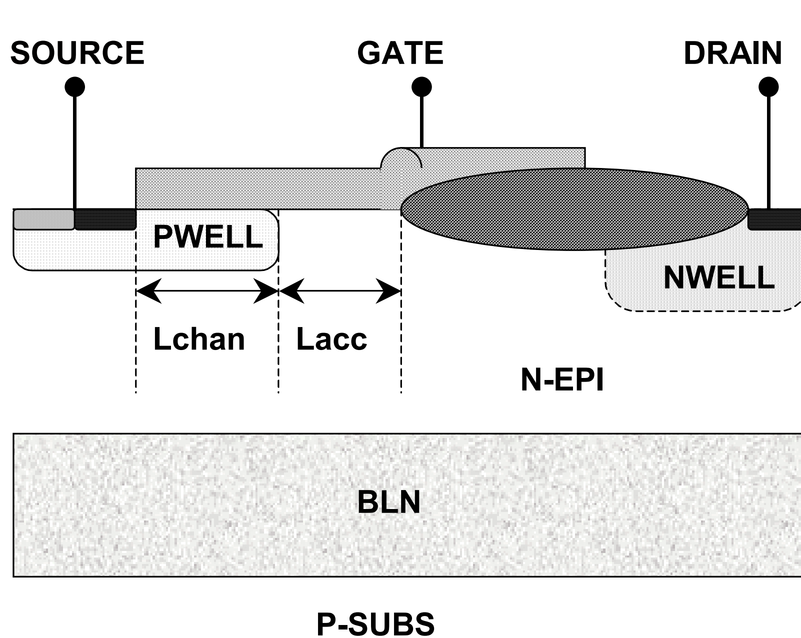
- ***At low V_{gs} (3V) and high V_{ds} (40V) : hot holes are present at the device birds beak.***

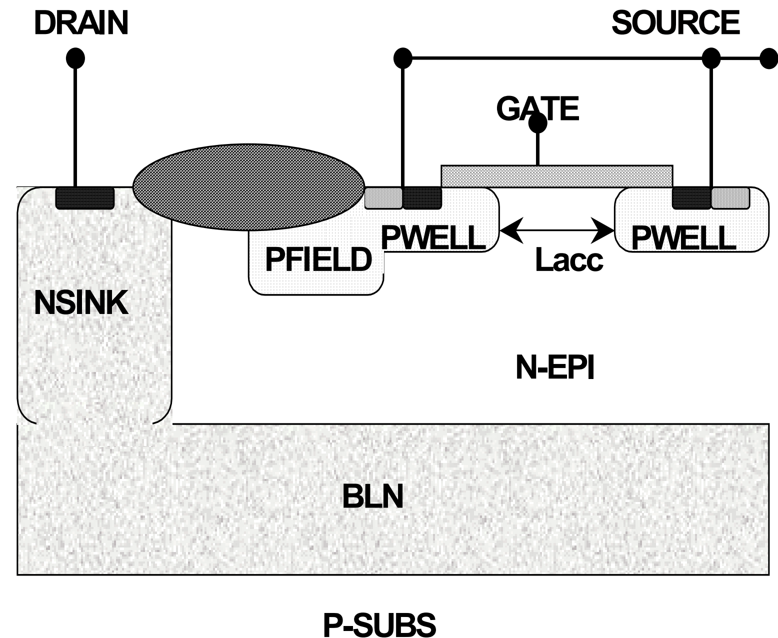


- ***TCAD data confirm analysis results.***

DC hot carrier : LDMOS vs VDMOS (1)

- *80V LDMOS and VDMOS in 0.35 µm SPT [54]*



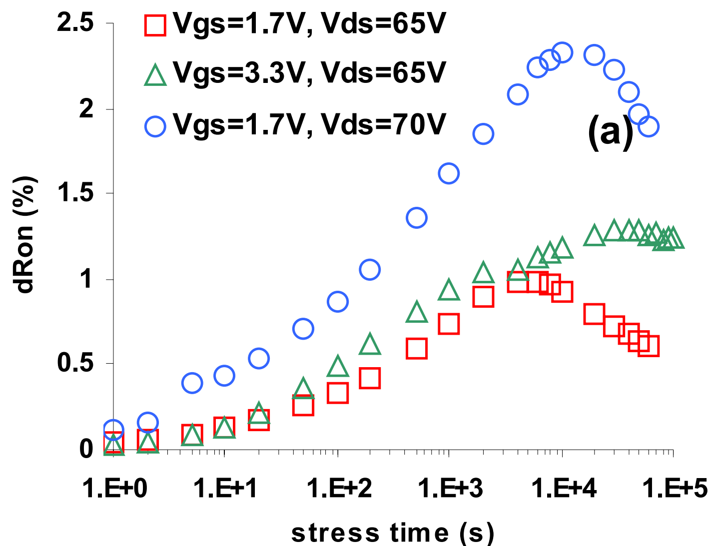


LDMOS *VDMOS*

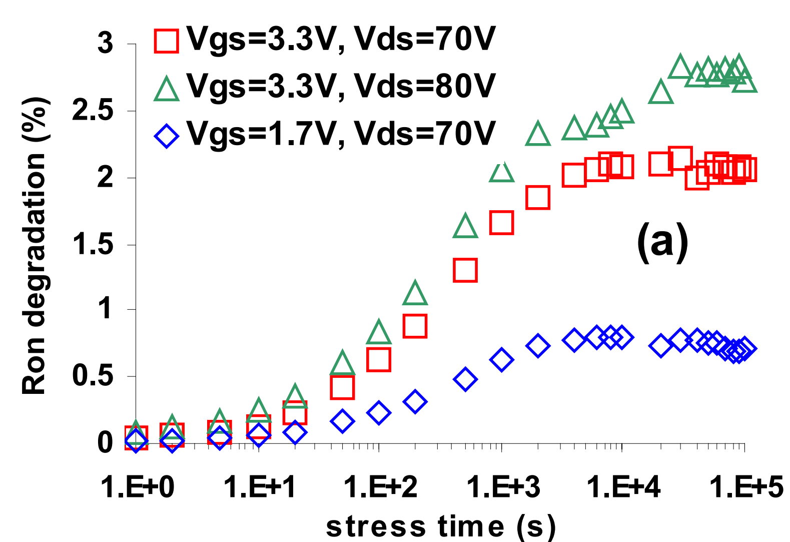
DC hot carrier : LDMOS vs VDMOS (2)

- ***Primary degradation point in LDMOS is birds beak (tip).***
- ***No birds beak is present in VDMOS drift region → expected to yield better for HC.***

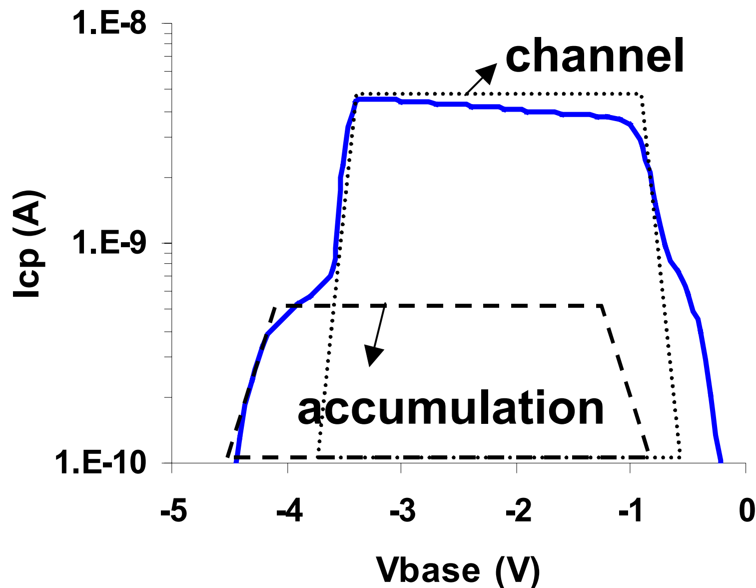
80V LDMOS in 0.35µm SPT

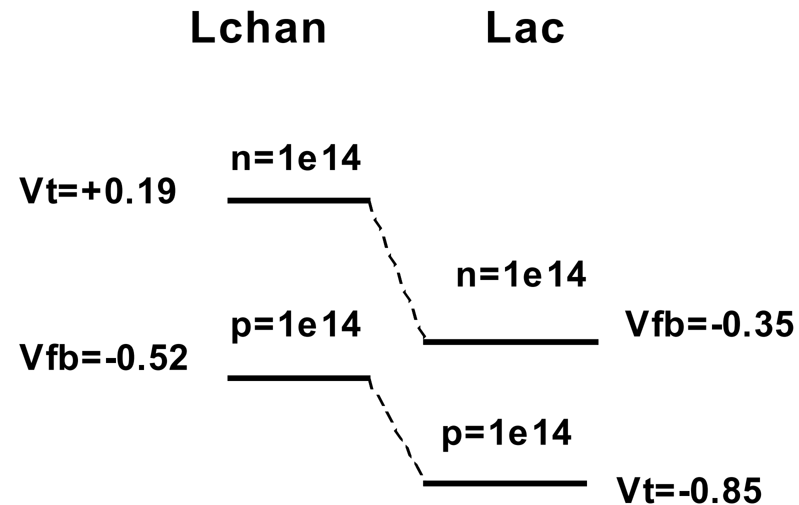


80V VDMOS in 0.35µm SPT



DC hot carrier : LDMOS vs VDMOS (3)



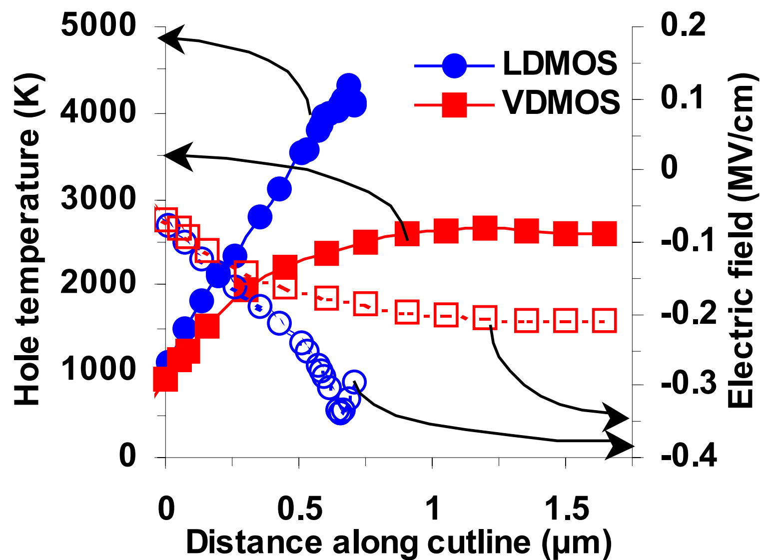


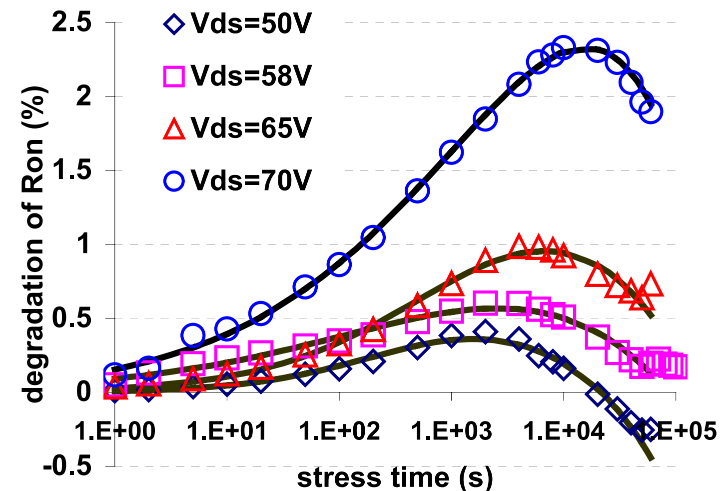
- ***VDMOS : N_{it} formation only in channel***
- ***LDMOS : N_{it} formation in channel and accumulation region (birds beak).***

DC hot carrier : LDMOS vs VDMOS (4)

- ***LDMOS birds beak tip :***
  - Electric field encroachment
  - Impact ionization spot : hot holes injection

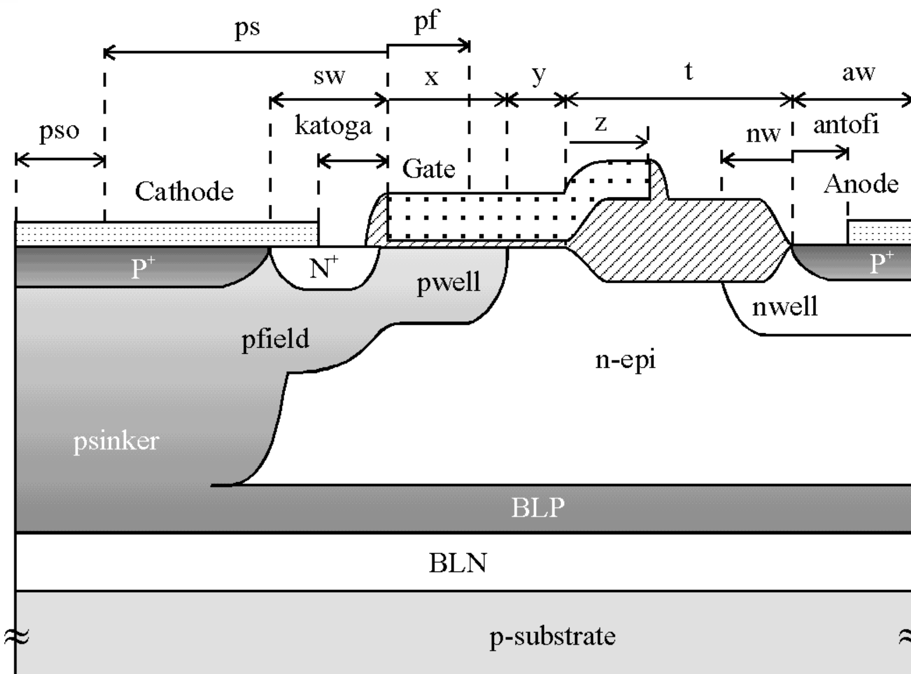
$$\Delta Ron = \frac{A.t^n}{1 + B.t^n} + C.t^m$$

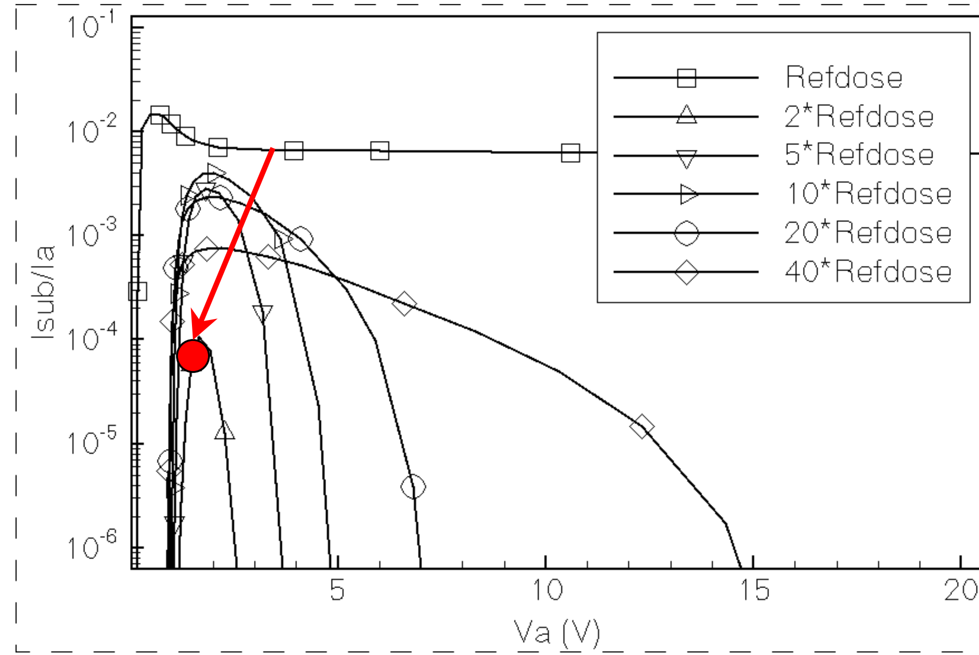




n-type L-IGBT (1)

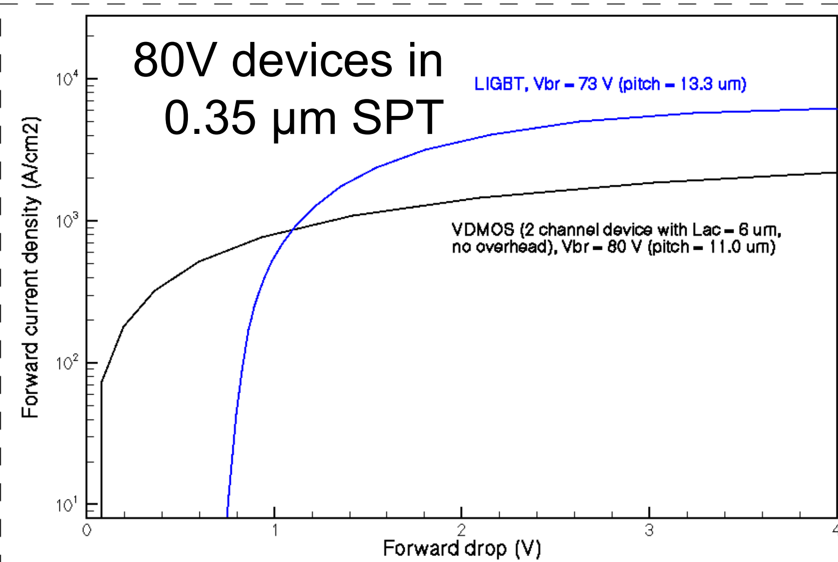
- L-IGBT in JI techno → substrate injection
- Use double isolation : BLN & BLP [45]

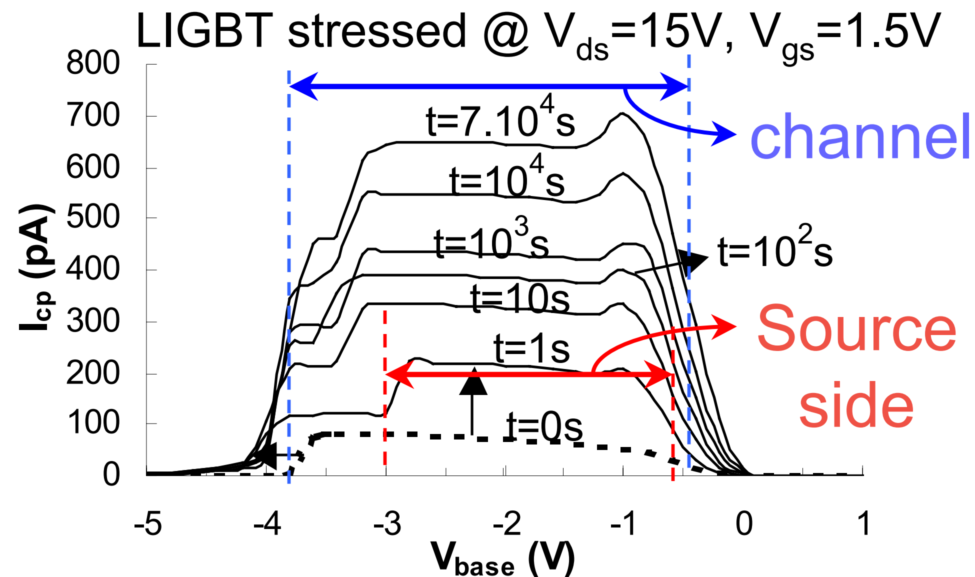




n-type L-IGBT (2)

- ***LIGBT has a much higher current density in on-state compared to MOS → power dissip***
- ***During operation : injection of charges can be monitored with CP***



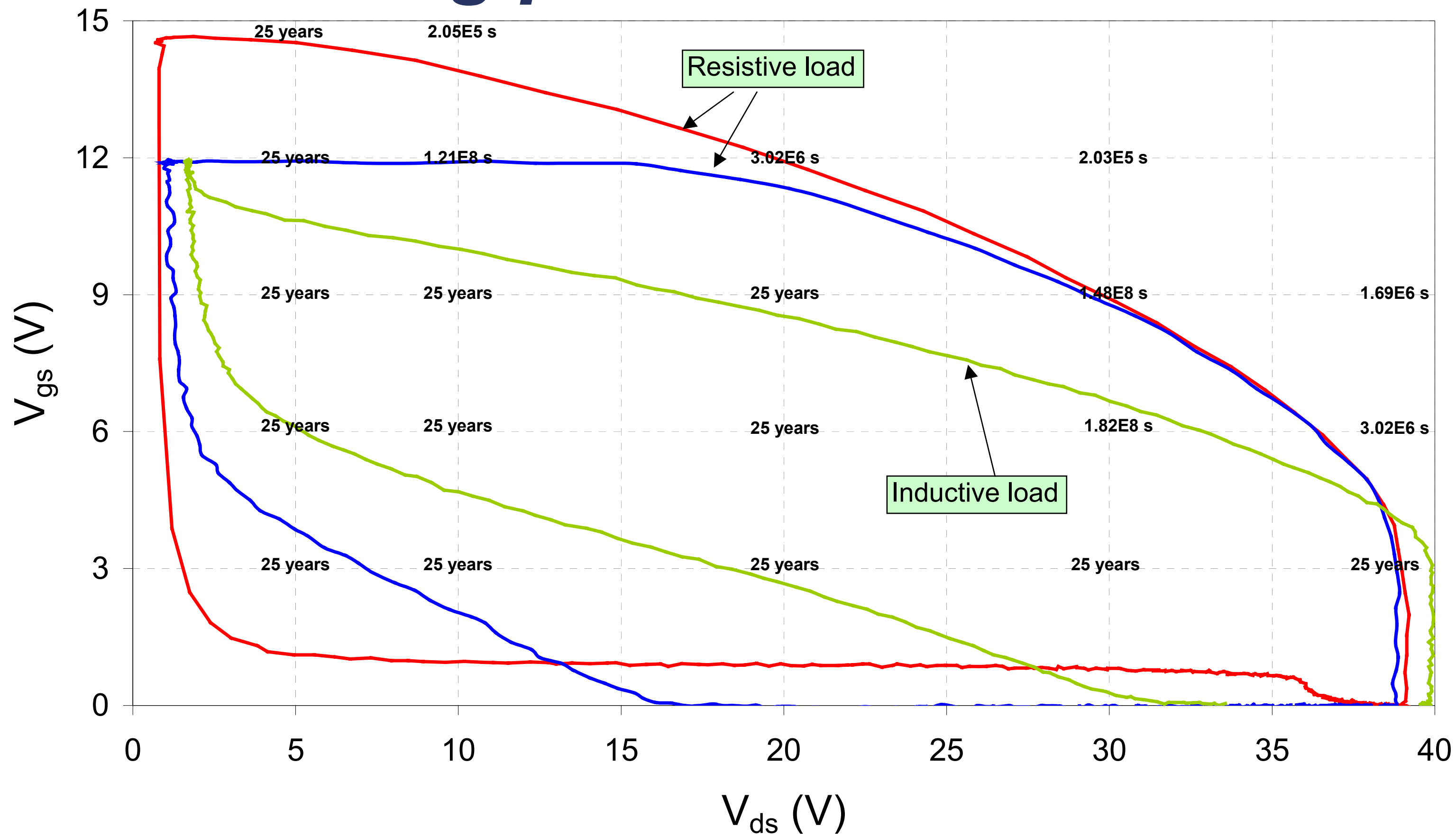


Reliability Problems in Smart Power

- DC hot carrier
- AC hot carrier (switching of a load)
- Electrical SOA (parasitic bipolar turn-on)
- Thermal SOA (energy capability)
- Simulation of thermal effects

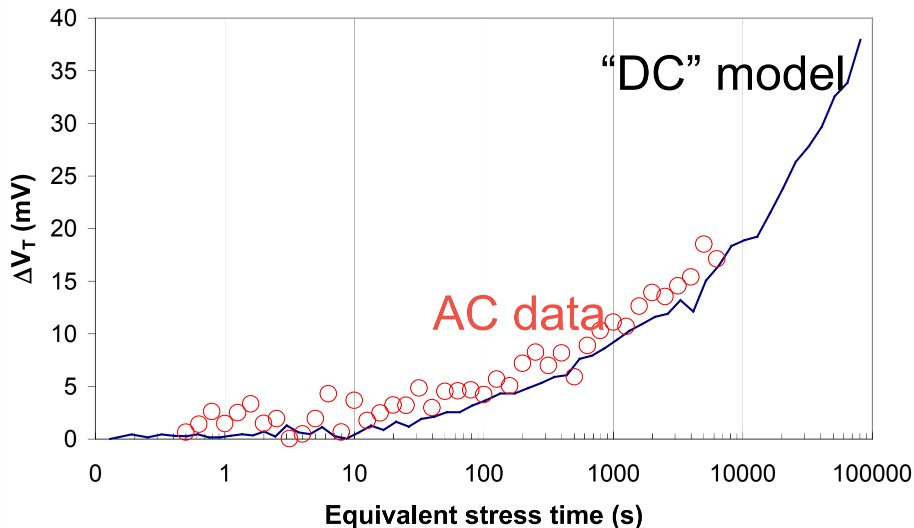
Switching of a load-Link to DC (1)

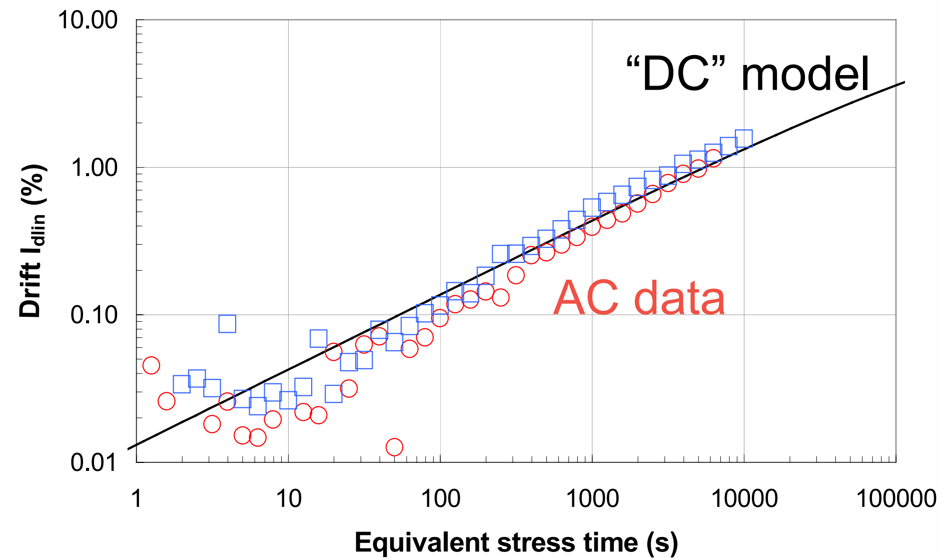
- ***Calculate total equivalent stress time from AC switching path.***



Switching of a load-Link to DC (2)

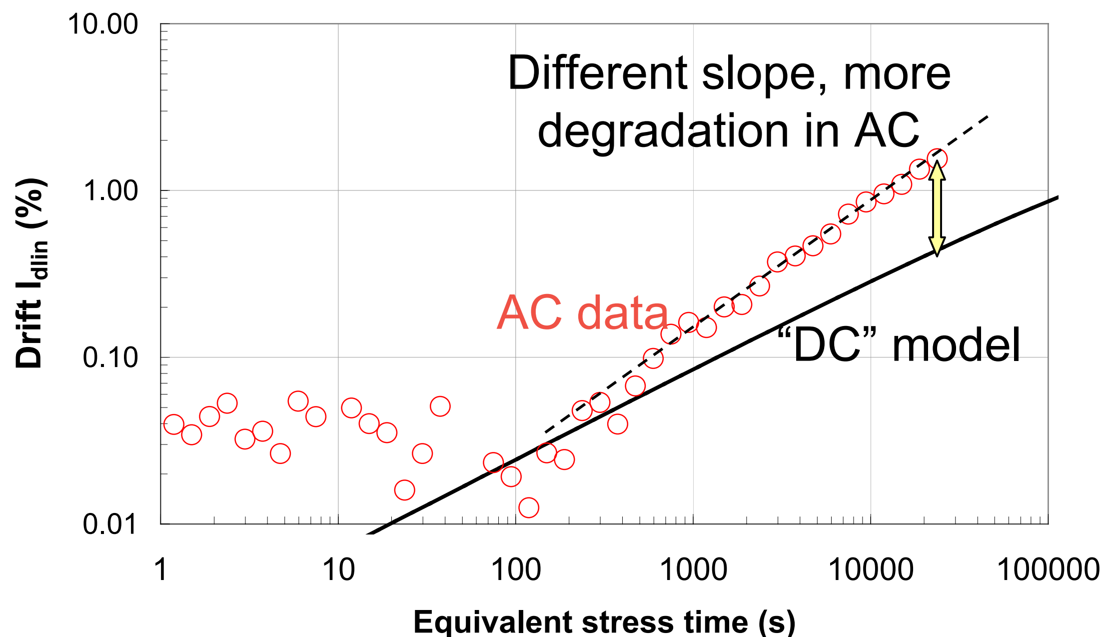
- *Resistive load : good agreement AC-DC*
- *Problem : switching through regions where different parameters are degrading.*

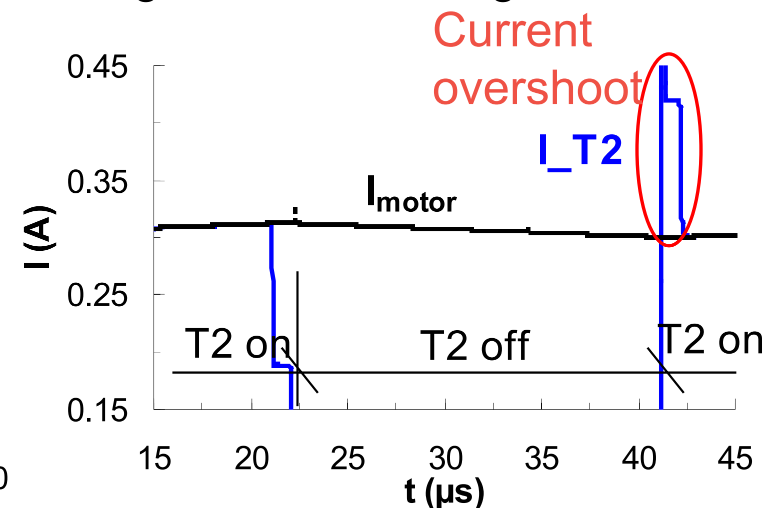




Switching of a load-Link to DC (3)

- *Inductive load : deviation from "DC" model.*
- *Due to overshoots upon switching.*
- *Overshoots to be reduced by design/circuit.*





Reliability Problems in Smart Power

- DC hot carrier
- AC hot carrier (switching of a load)
- **Electrical SOA (parasitic bipolar turn-on)**
- Thermal SOA (energy capability)
- Simulation of thermal effects

Electrical SOA (1)

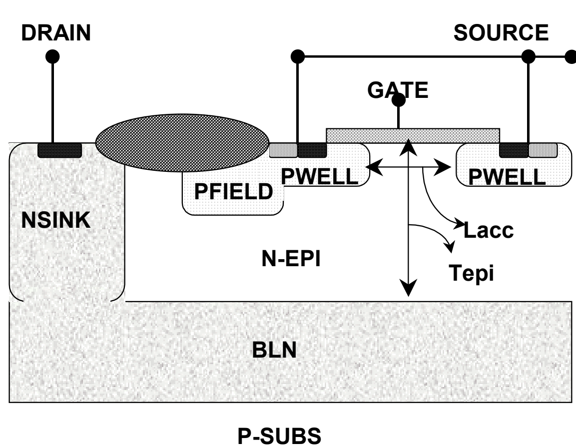
- *LDMOS: bipolar snapback is destructive [26]*
- *Electrical SOA is to a good approximation given by the "flux tube model" [22]*

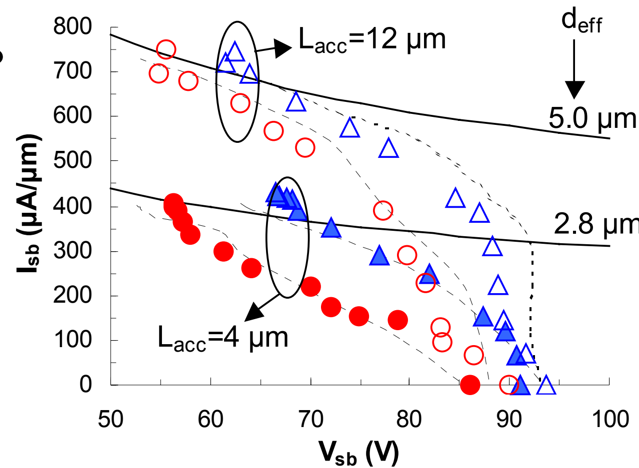
Figure 15: Failure analysis after deprocessing on a ggLDMOS after an ESD stress.

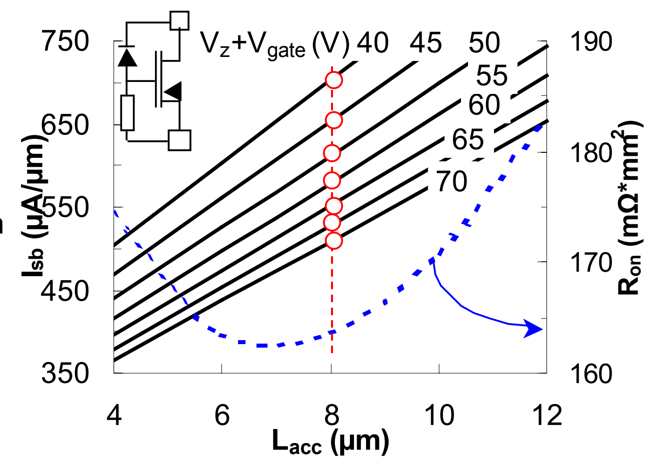
$$\frac{I_{sb}}{W} = d_{eff}.q.v_{sat}.N_d + d_{eff}.\frac{v_{sat}.\varepsilon.E_{sb}^2}{2.V_{sb}}$$

Electrical SOA (2)

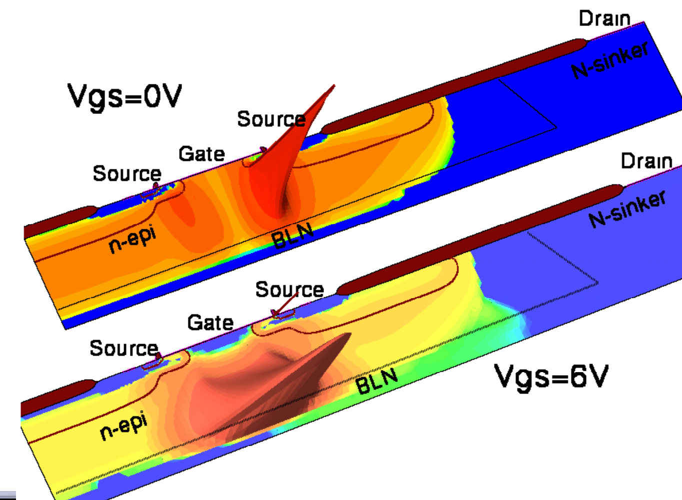
- *Electrical SOA VDMOS [55]*





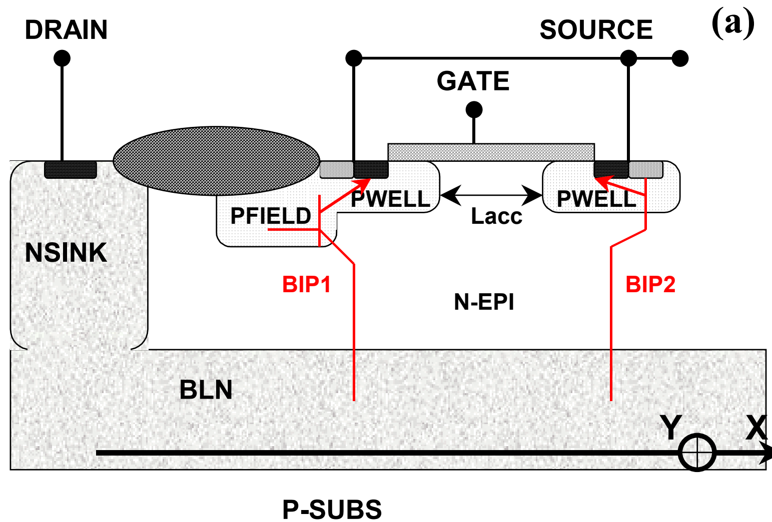


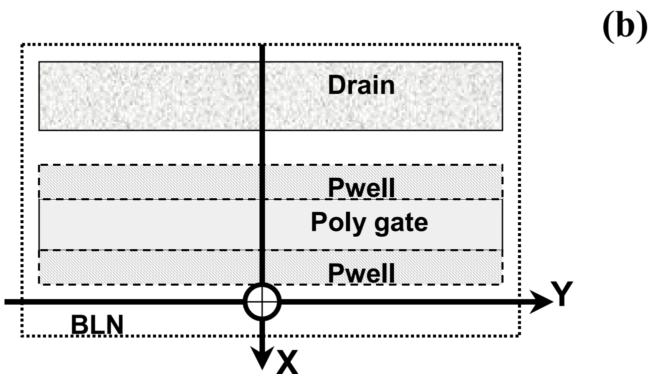
- *Flux tube model predicts well limiting I_{sb}.*
- *Trade-off I_{sb} - R_{on}*

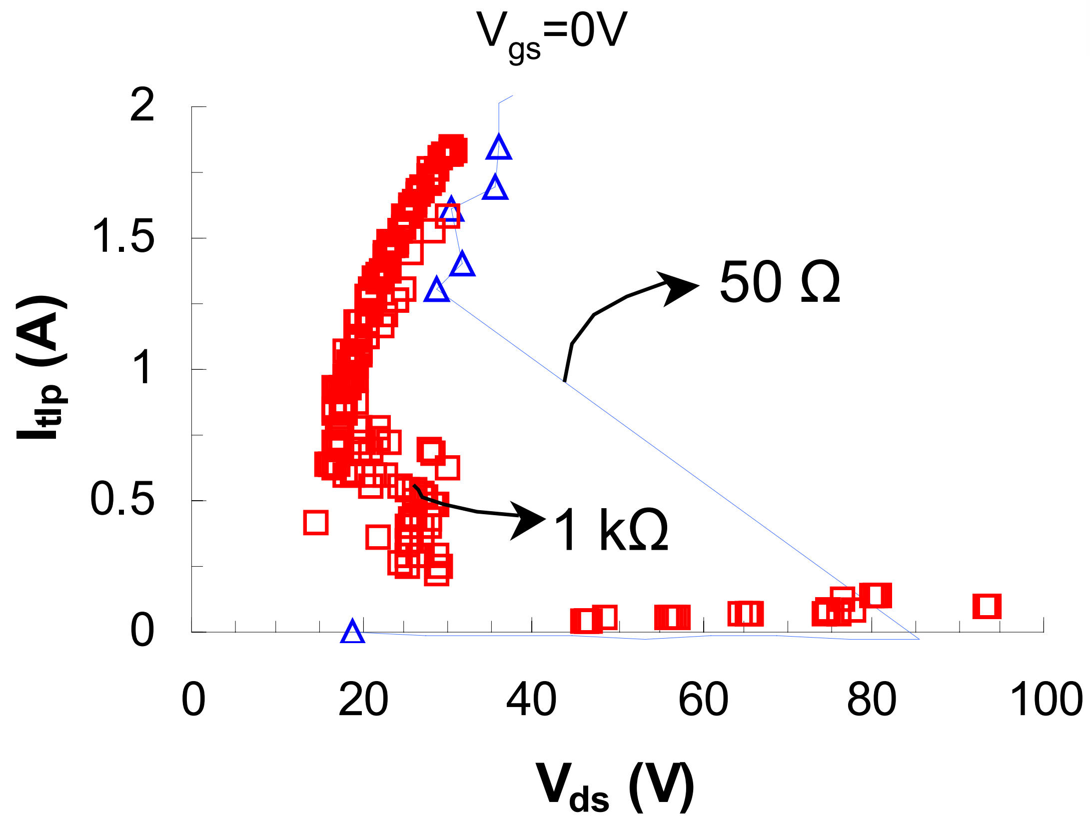


TIM on VDMOS (1)

- ***Hot spot hopping in VDMOS [28,29]***







TIM on VDMOS (2)

I_{tlp}=0.16 A

I_{tlp}=0.27 A

t=19ns, t=41ns, t=61ns, t=81ns, t=113ns

t=20ns, t=40ns, t=62ns, t=82ns, t=114ns

Power density [mW/µm^2]

n+ n-epi p p bln

Position along length, x [µm]

Position along width, y [µm]

- ***Hopping dynamically distributes heat***

Reliability Problems in Smart Power

- DC hot carrier
- AC hot carrier (switching of a load)
- Electrical SOA (parasitic bipolar turn-on)
- **Thermal SOA (energy capability)**
- Simulation of thermal effects

Thermal SOA (1)

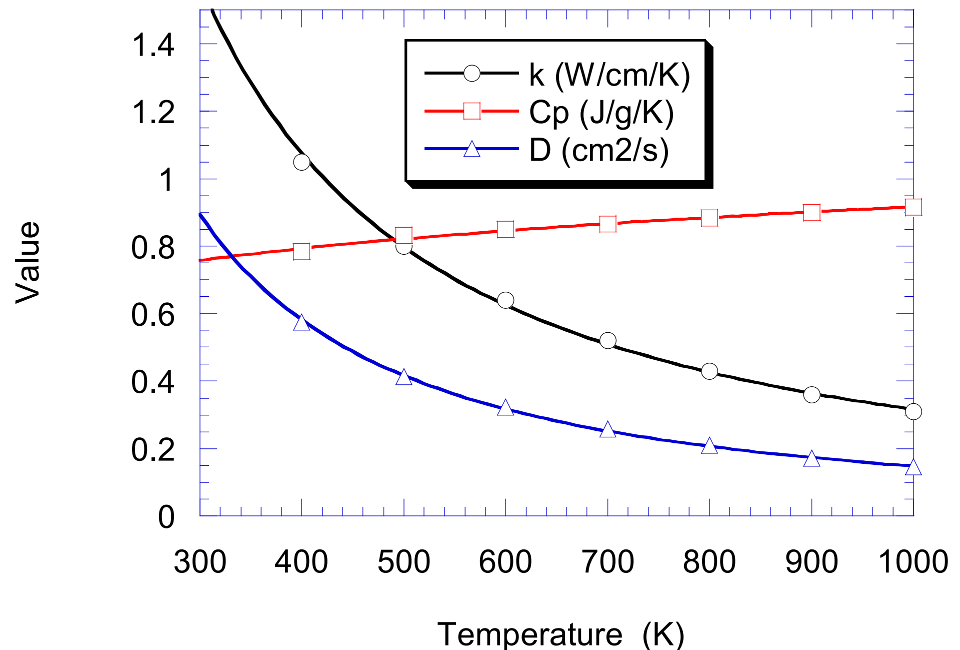
- ***Wunsch-Bell model for a semi-infinite piece of silicon subject to rectangular power pulse P***

$$P(t) = \frac{k\sqrt{\pi}\Delta T_{crit}}{\sqrt{4Dt}}; E(t) = P(t) * t \sim \sqrt{t}$$

Thermal conductivity k in W/cm.K

$D=k/\rho.C_p$, ρ being the density (g/cm^3) and C_p the specific heat (J/gK)

ΔT_{crit} is the critical temperature at thermal failure.



Thermal SOA (2)

- ***Dwyer model for heat source of finite dimensions (a>b>c)***

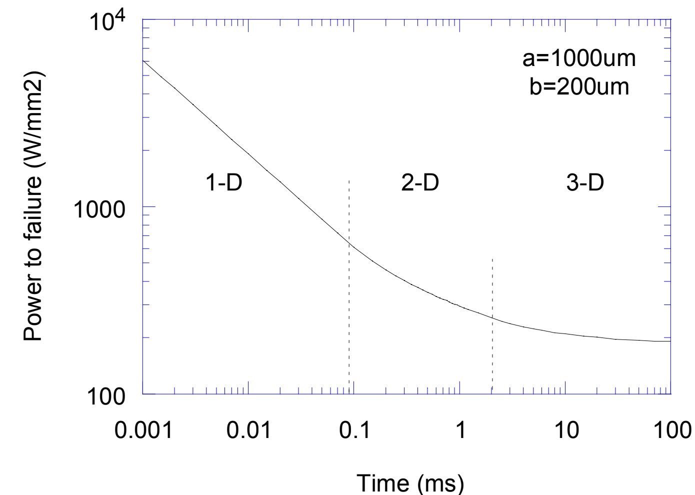
[31,41]

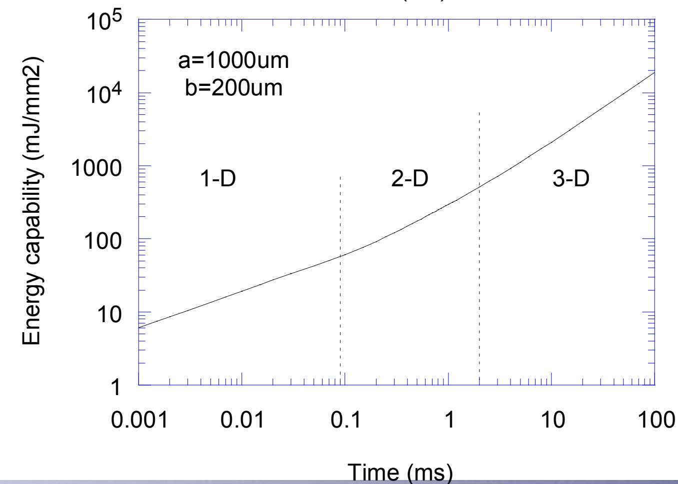
$$P_{1D} = \frac{k\sqrt{\pi}\Delta T_{crit}}{\sqrt{4D}\left(\sqrt{t} - \frac{\sqrt{t_c}}{2}\right)}, \quad t_c < t \le t_b = \frac{b^2}{4\pi D}$$

$$P_{2D} = \frac{2k\pi\Delta T_{crit}}{b\left[\ln\left(\frac{t}{t_b}\right) + 2 - \frac{c}{b}\right]}, \quad t_b \le t \le t_a = \frac{a^2}{4\pi D}$$

$$P_{3D} = \frac{k\pi\Delta T_{crit}}{b\left[\ln\left(\frac{a}{b}\right) + 2 - \frac{c}{2b} - \sqrt{\frac{t_a}{t}}\right]}, \quad t_a \le t$$

$$P_{ss} = \frac{k\pi\Delta T_{crit}}{b\left[\ln\left(\frac{a}{b}\right) + 2 - \frac{c}{2b}\right]}, \quad t \to \infty$$





Thermal SOA (3)

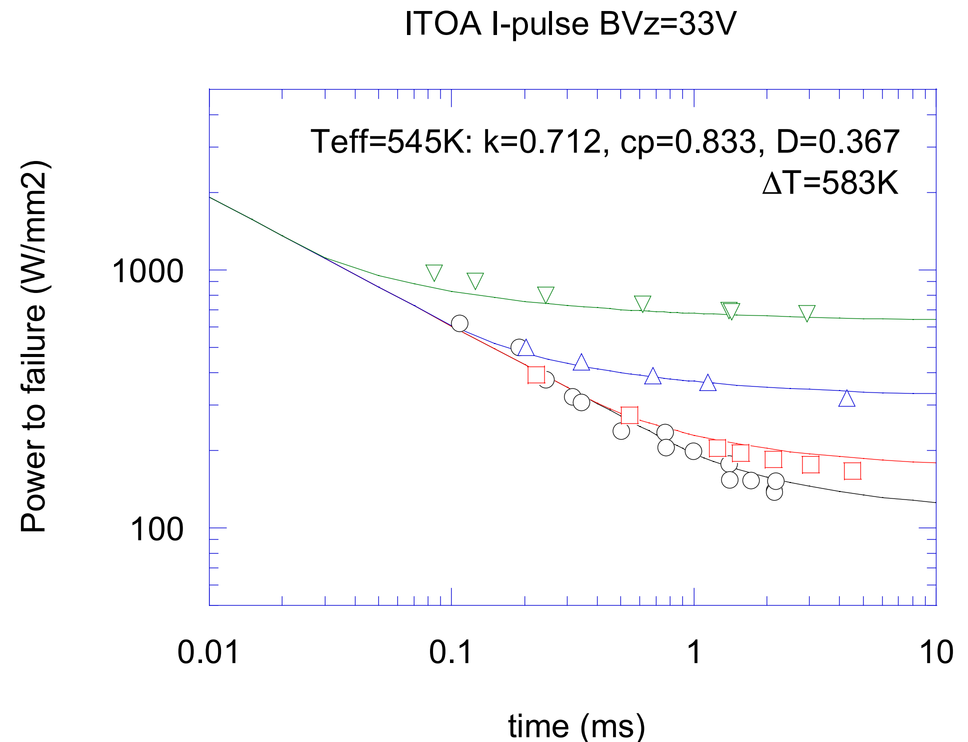
- ***Motivation : construct thermal SOA of 40V square power drivers of different size.***
- ***Measurement data and model fitting.***

•D, k and ΔT_{crit} are not independent

•K and D are dependent on T_{eff}

•T_{eff} and ΔT_{crit} are to be fitted to the data

ΔT_{crit} (~580K) is rather large. From simulations and measurements values between 400-500 are found [39,40]



Thermal SOA (4)

- ***Dependency of P_{fail} on V_{ds}***
  - Pure thermal ?
  - Electro-thermal coupling ?
  - Data for constant time-to-failure ? →Normalize the data to a fixed time (e.g. 1 ms).

$$P_{3D}(t^*) = P_{1D}(t)\frac{\sqrt{4\pi Dt}}{b\left[\ln\left(\frac{a}{b}\right)+2-\sqrt{\frac{t_a}{t^*}}\right]},\quad t \le t_b$$

$$P_{3D}(t^*) = P_{2D}(t)\frac{\left[\ln\left(\frac{t}{t_b}\right)+2\right]}{2\left[\ln\left(\frac{a}{b}\right)+2-\sqrt{\frac{t_a}{t^*}}\right]},\quad t_b \le t \le t_a$$

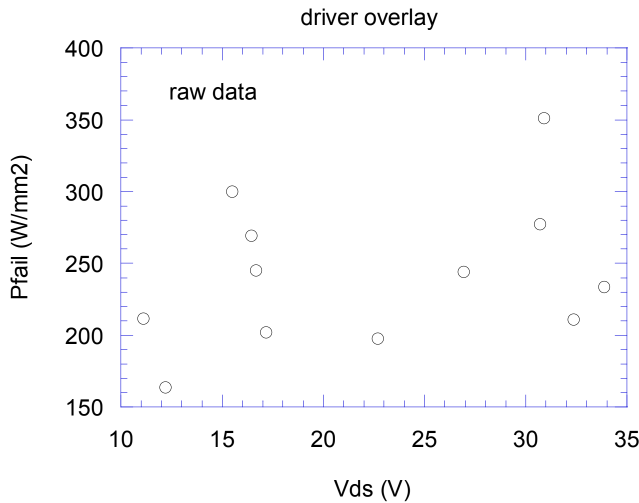
$$P_{3D}(t^*) = P_{3D}(t)\frac{\left[\ln\left(\frac{a}{b}\right)+2-\sqrt{\frac{t_a}{t}}\right]}{\left[\ln\left(\frac{a}{b}\right)+2-\sqrt{\frac{t_a}{t^*}}\right]},\quad t_a \le t$$

Only dependent on D, not on ΔT_{crit}.

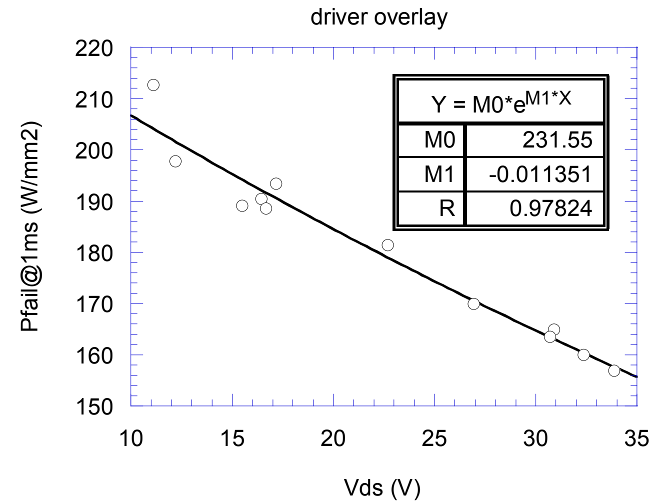
D assumed to be independent of V_{ds}.

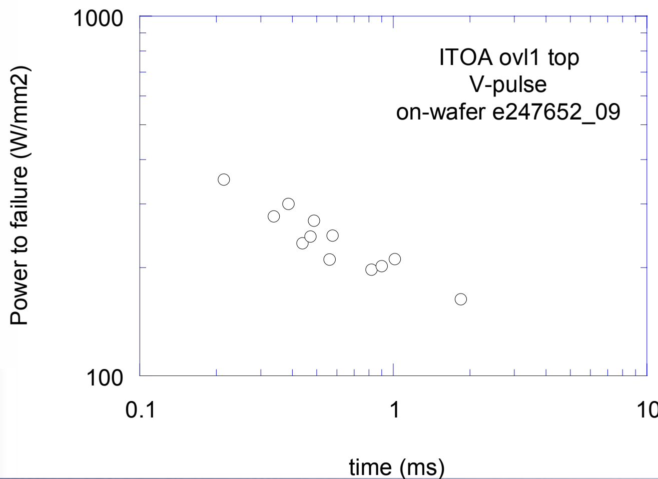
Thermal SOA (5)

Raw data

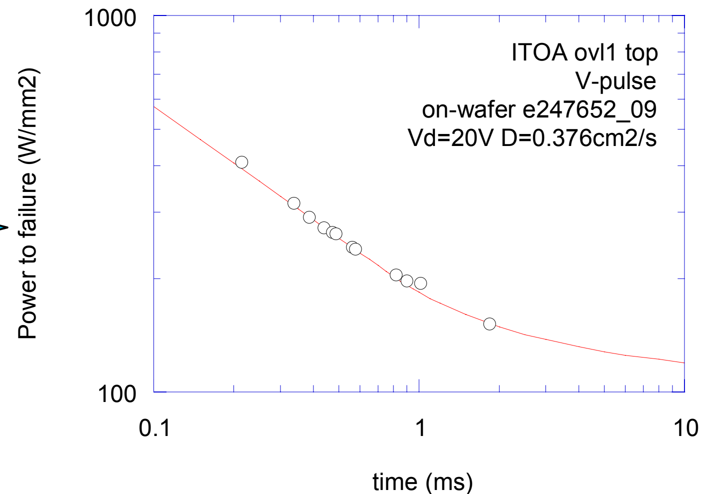


normalized to t*=1ms



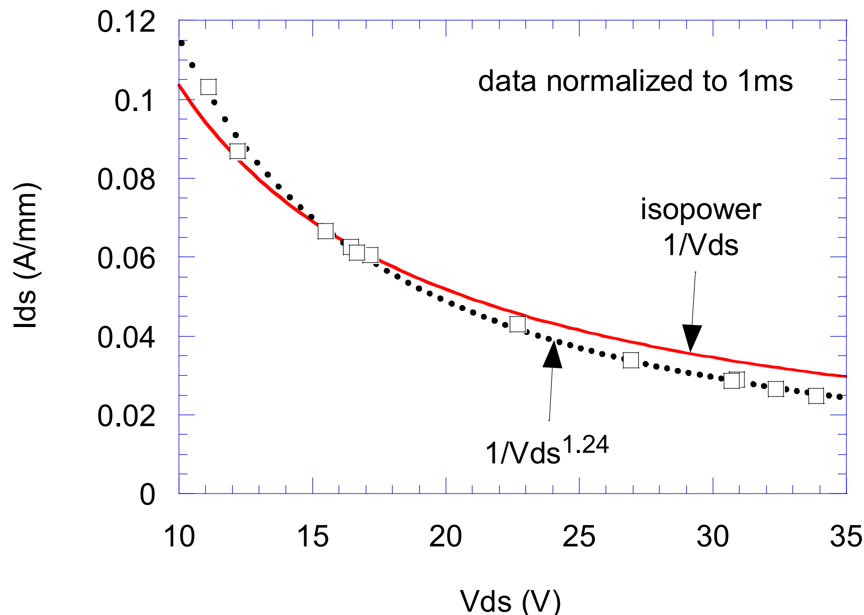


normalized to V_{ds}=20V



Thermal SOA (6)

- ***Thermal SOA***
  - Plot equi-t_{fail} lines in V_{gs}-V_{ds} or I_{ds}-V_{ds} plot.
  - Problem : t_{fail} is not an independent variable.
  - Use normalization procedure.



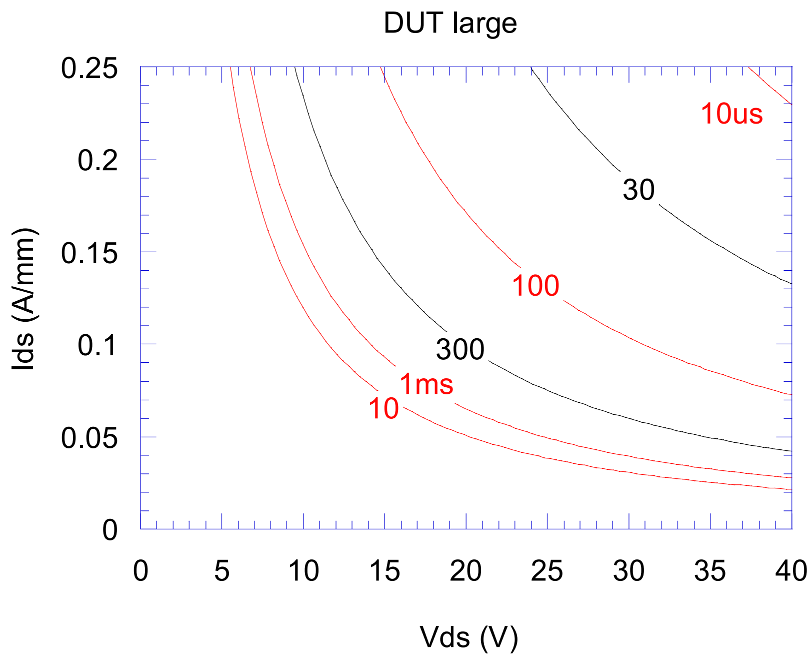
A generalized fit $I_{ds}(V_{ds})$~$1/V_{ds}^{1.24}$ yields the best results, consistent with electro-thermal coupling.

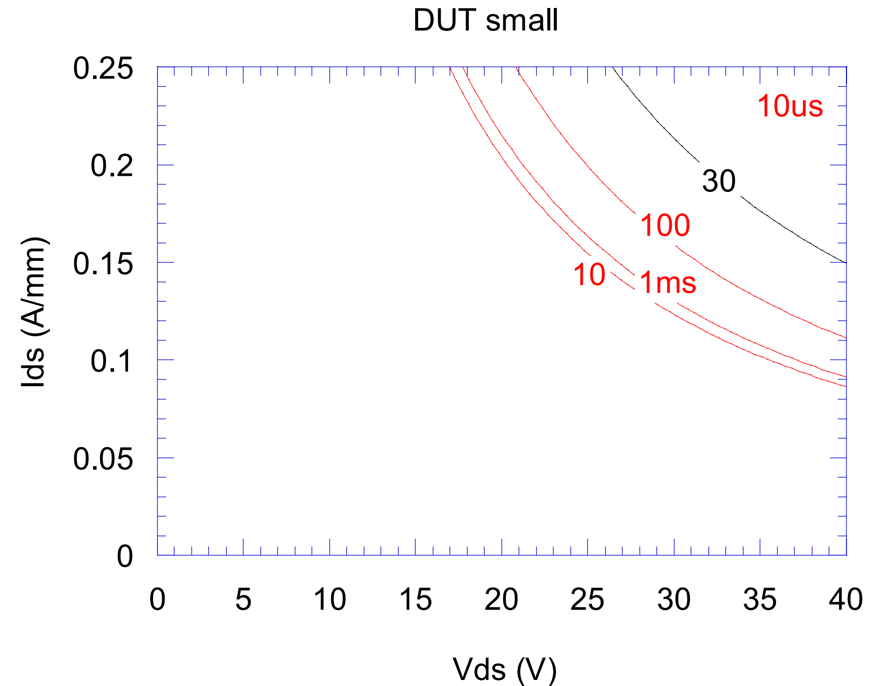
Cross-checked on other sets of data.

Similar results obtained by Krabbenborg et al. [35]

Thermal SOA (7)

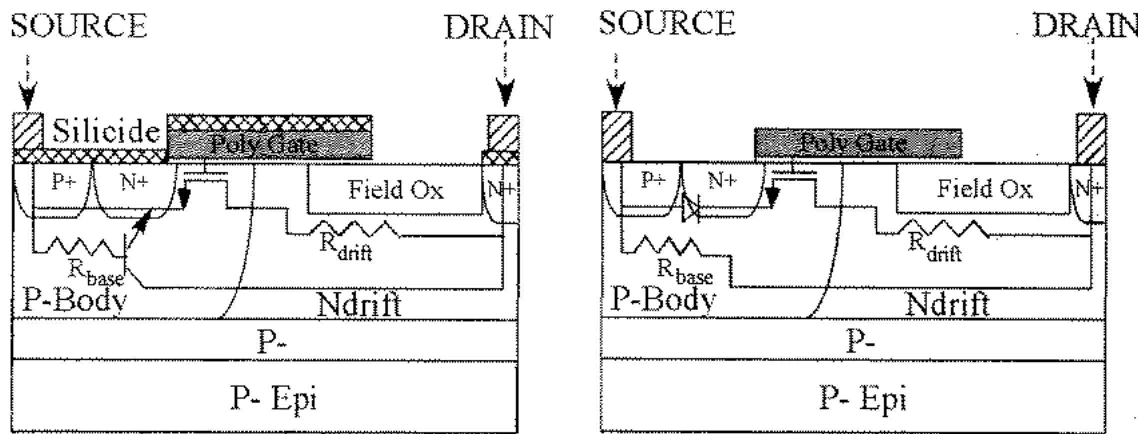
- ***Thermal SOA : equi-t_{fail} as obtained from the Dwyer model.***

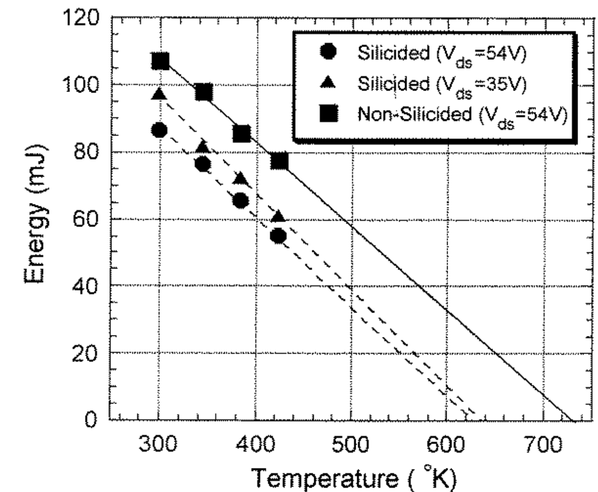




Thermal SOA (8)

- *Electro-thermal interaction : de-activate parasitic NPN [40] to isolate pure thermal effects.*

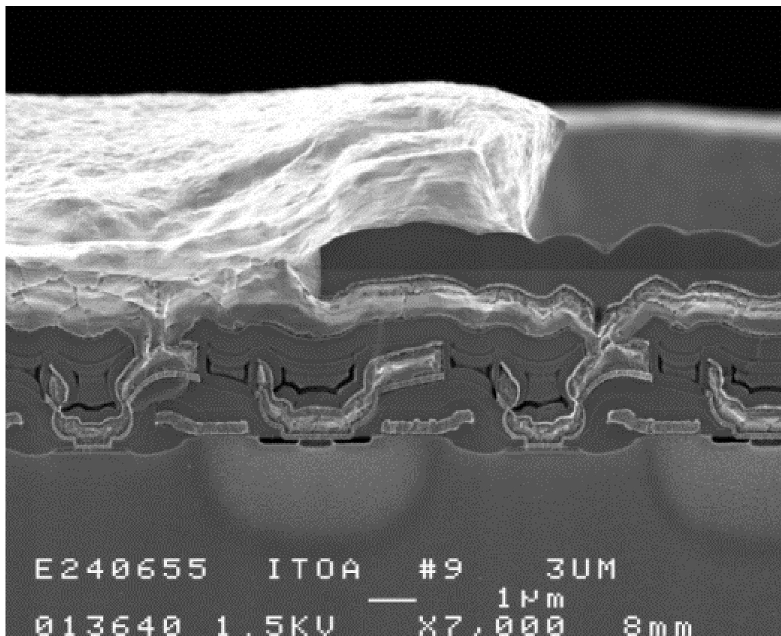


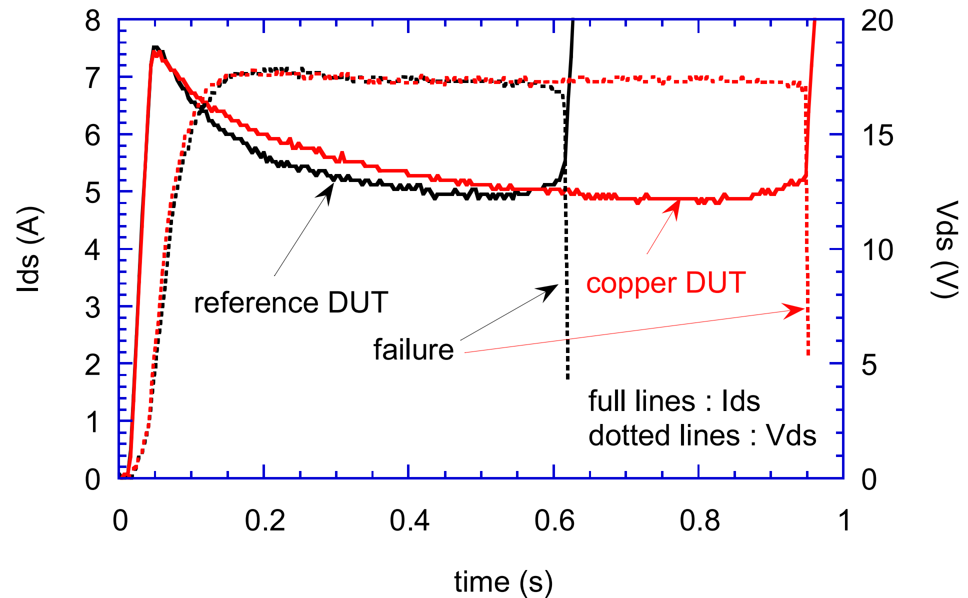


- *Non silicided device yields T_{crit}=730 K*
- *Silicided device : T_{crit}=630 K, due to electro-thermal coupling.*

Thermal SOA (9)

- ***In smart power, an electroplated top Cu layer (3-25 µm) is often used :***
  - To reduce the metal resistance [32]
  - As a heat sink/spreader to reduce T_{max} [38,41]





Reliability Problems in Smart Power

- DC hot carrier
- AC hot carrier (switching of a load)
- Electrical SOA (parasitic bipolar turn-on)
- Thermal SOA (energy capability)
- **Simulation of thermal effects**

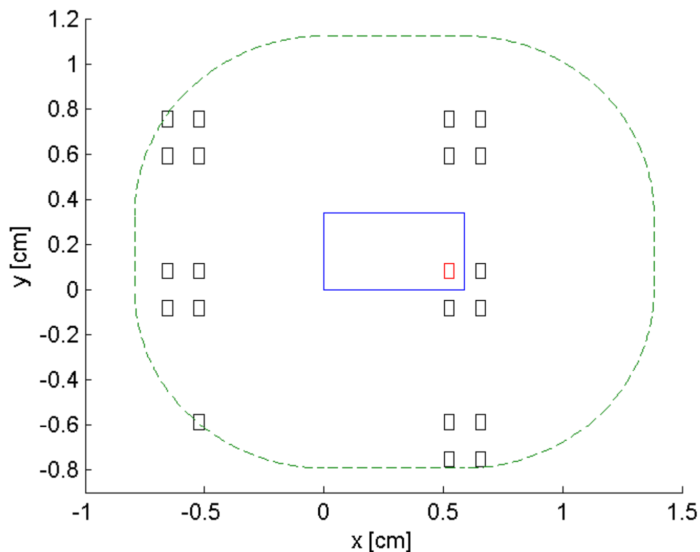
Thermal simulations (1)

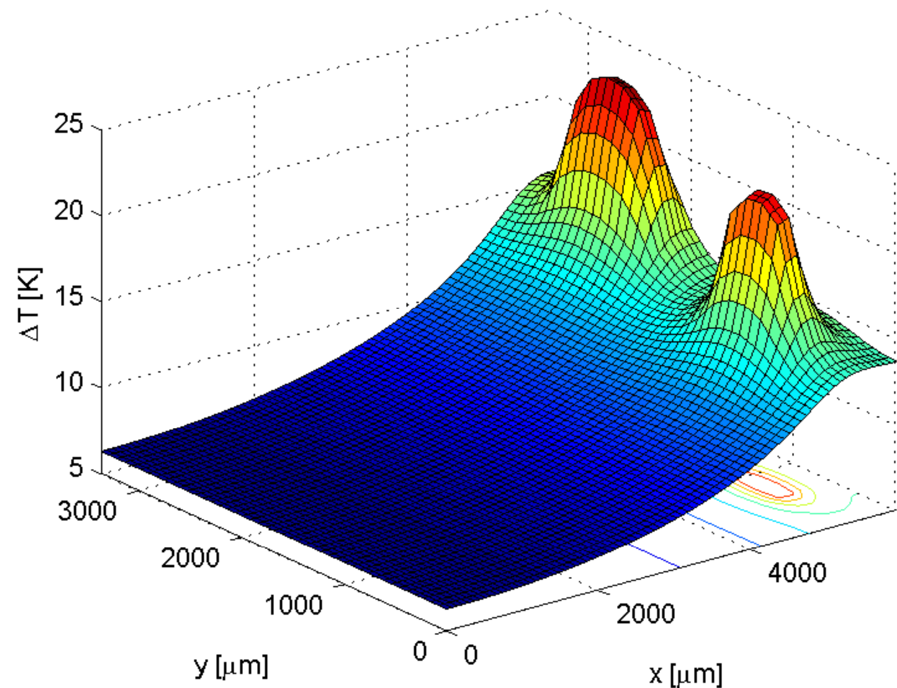
- ***Need for a fast thermal simulation tool as a function of pulse time, bias conditions, device area and chip size.***
  - Green's function solution of the heat diffusion equation [56].
  - Adiabatic boundary conditions using the method of images [57].
  - Thermal boundaries defined by a typical thermal diffusion length.
- ***Calculation of T(x,y,z,t) for any number of power sources and for any power pulse P(t)***

Thermal simulations (2)

- ***Examples of the model (1)***

Images and thermal boundary (100 ms)



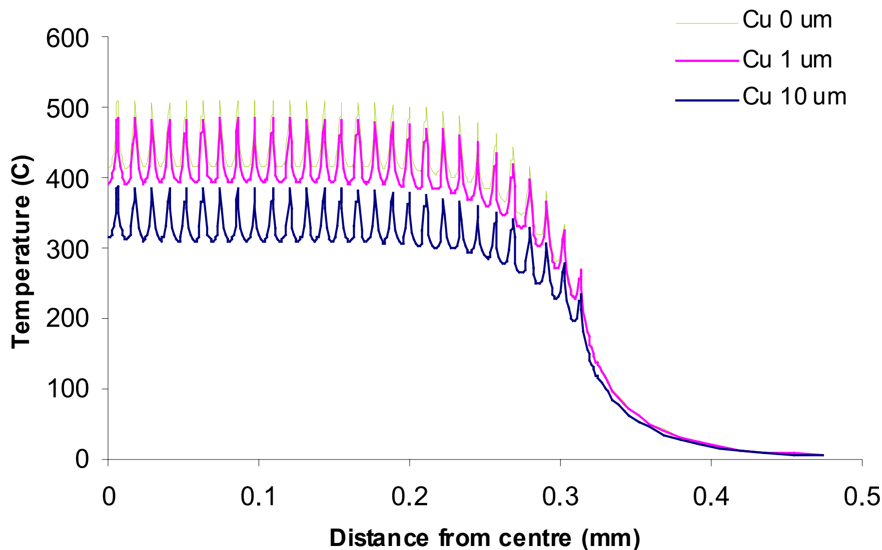


Temperature rise after 1s for 2 DMOS in a H-bridge, each dissipating 2.3 W

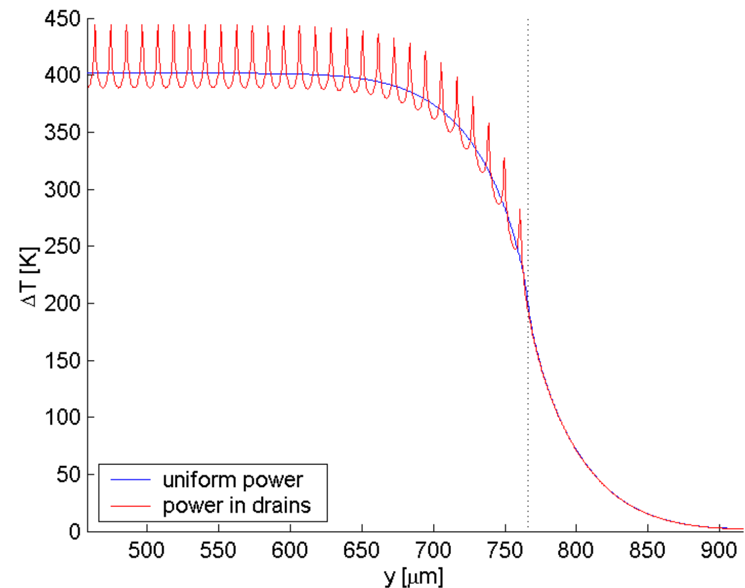
Thermal simulations (3)

- ***Numerical simulations: MSC.Marc software***
- ***Good agreement for small Cu thickness***

commercial software

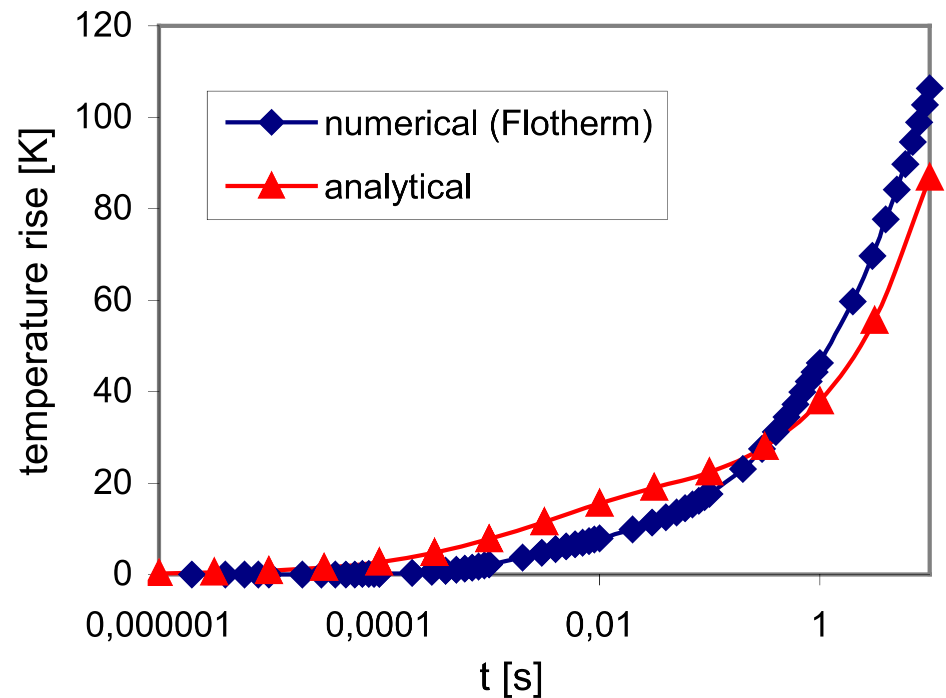


developed tool



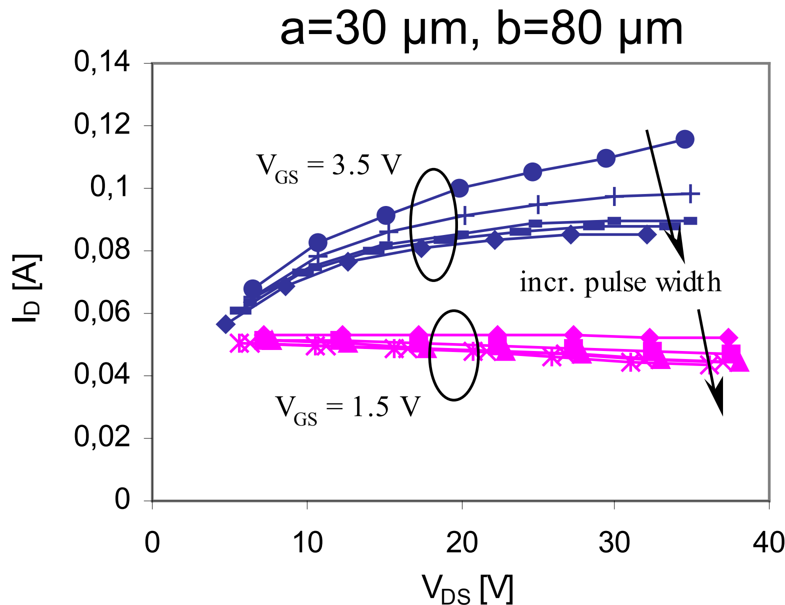
Thermal simulations (4)

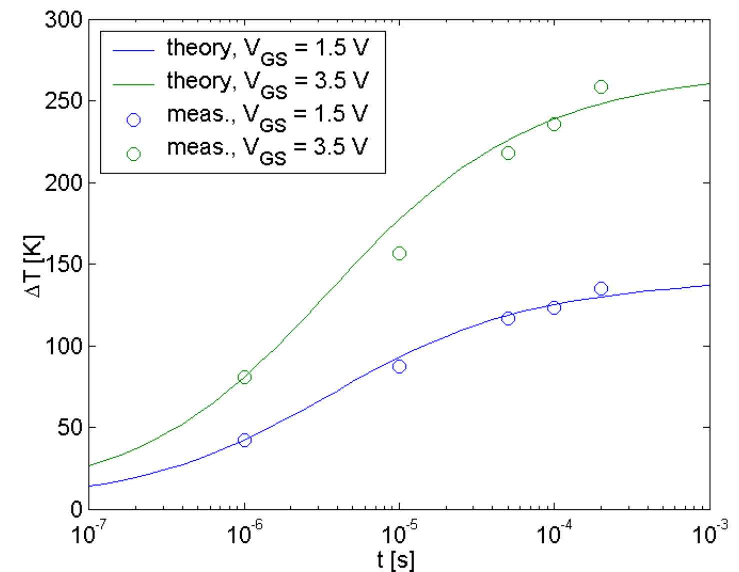
- ***Accuracy of the model : temperature rise in the center of a DMOS, for a 2 W power step function.***
  - Flotherm : 24 hours
  - Matlab : 20 min
- ***Model is :***
  - Fast
  - Reliable
  - Flexible to use



Thermal simulations (5)

- ***Experimental validation of the model :***
  - Mobility reduction [58] : $I_D / I_{D0} = (T/T_0)^{-k}$
  - Integrated temperature sensors [59,39]

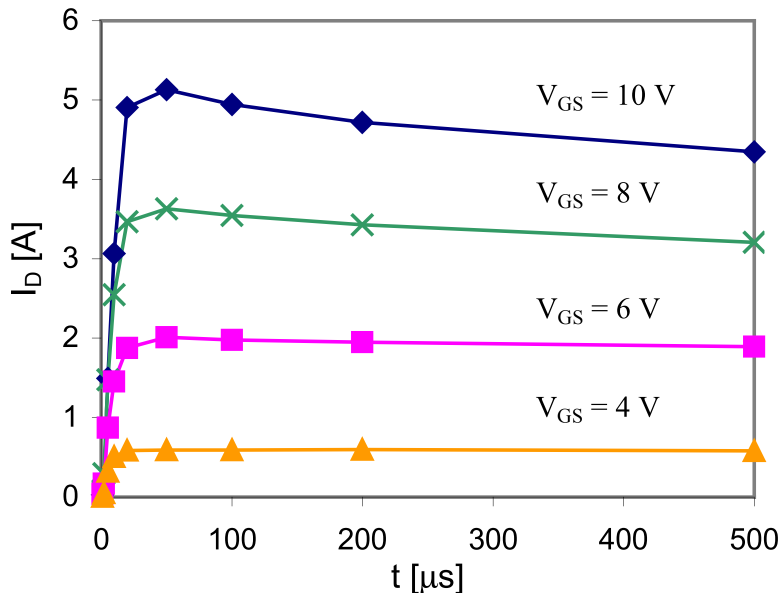


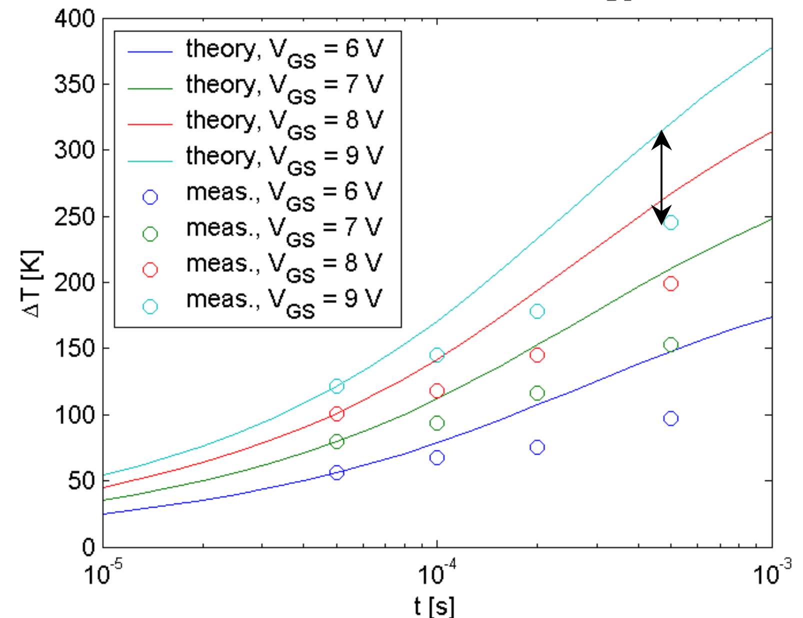


- Works reasonably well for relatively small devices.

Thermal simulations (6)

- ***For large drivers : temperature seems to be overestimated.***
- ***Need for electro-thermal coupling.***

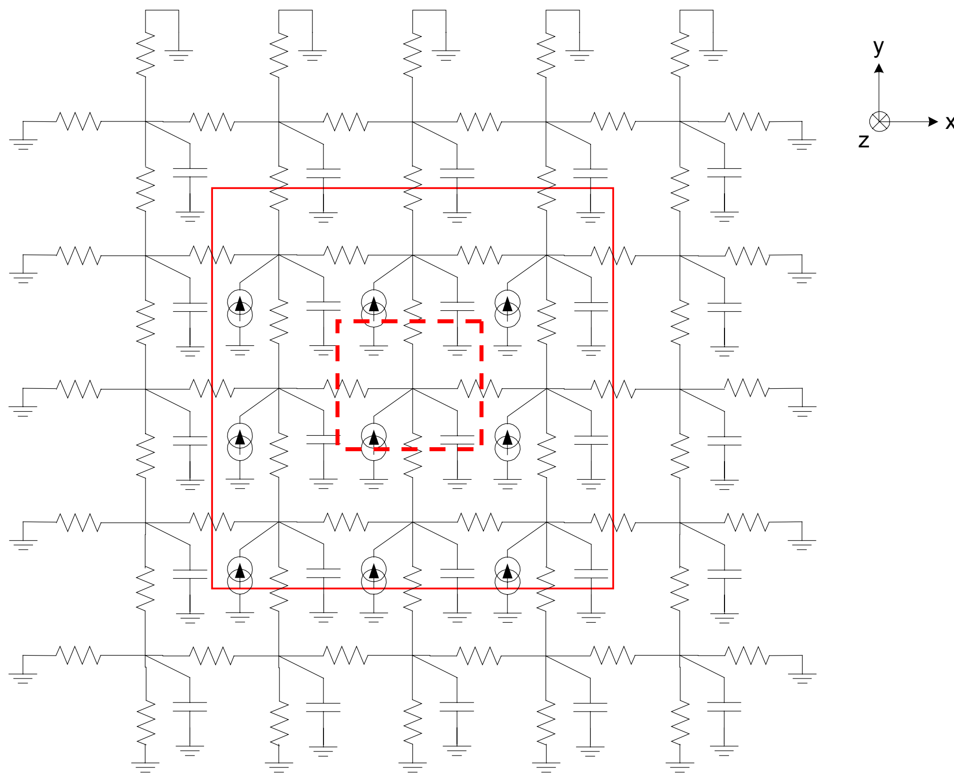


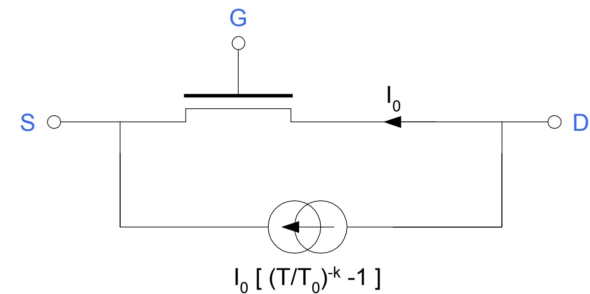


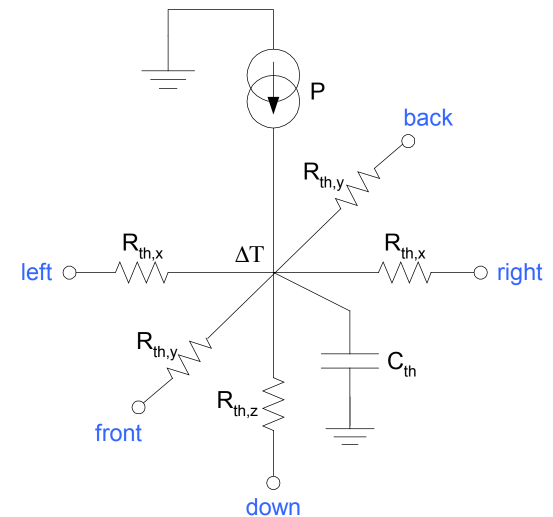
Thermal simulations (7)

- ***Electro-thermal coupling : discretization***

Topview thermal network

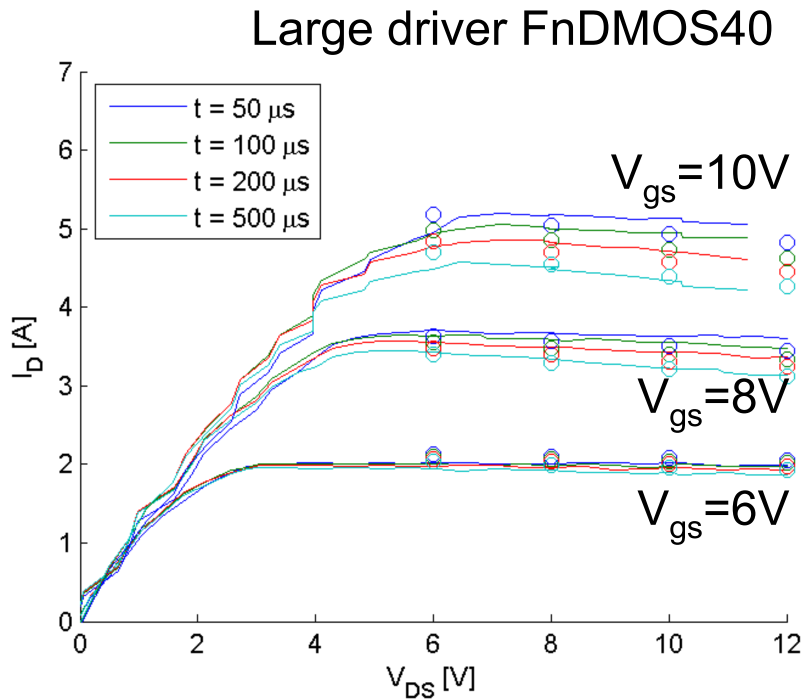


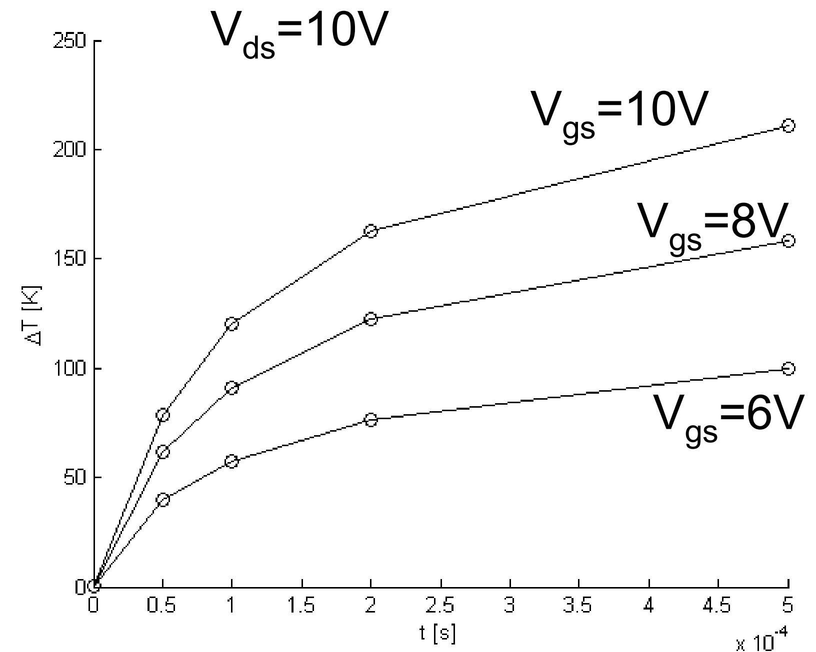




Thermal simulations (8)

- ***Current and temperature versus pulse time***

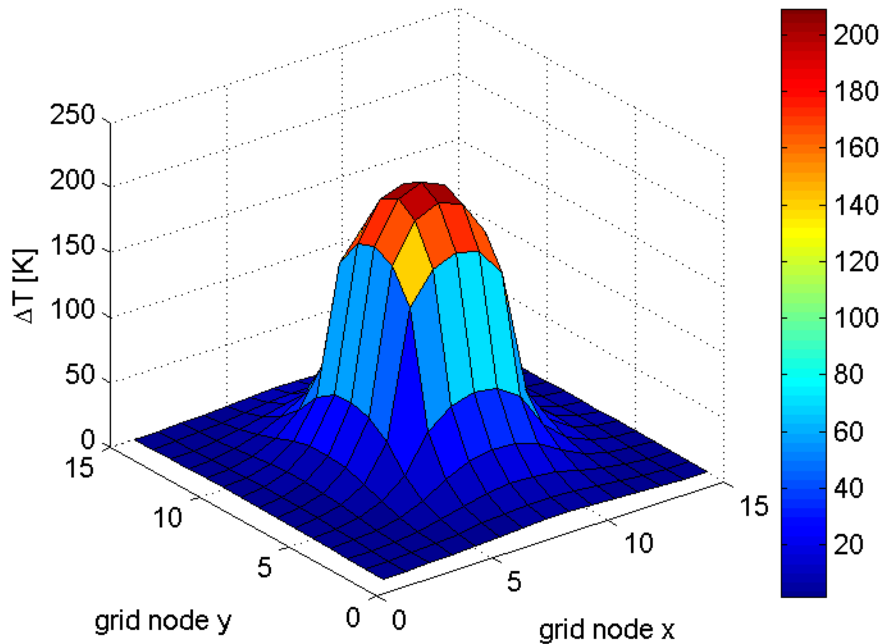


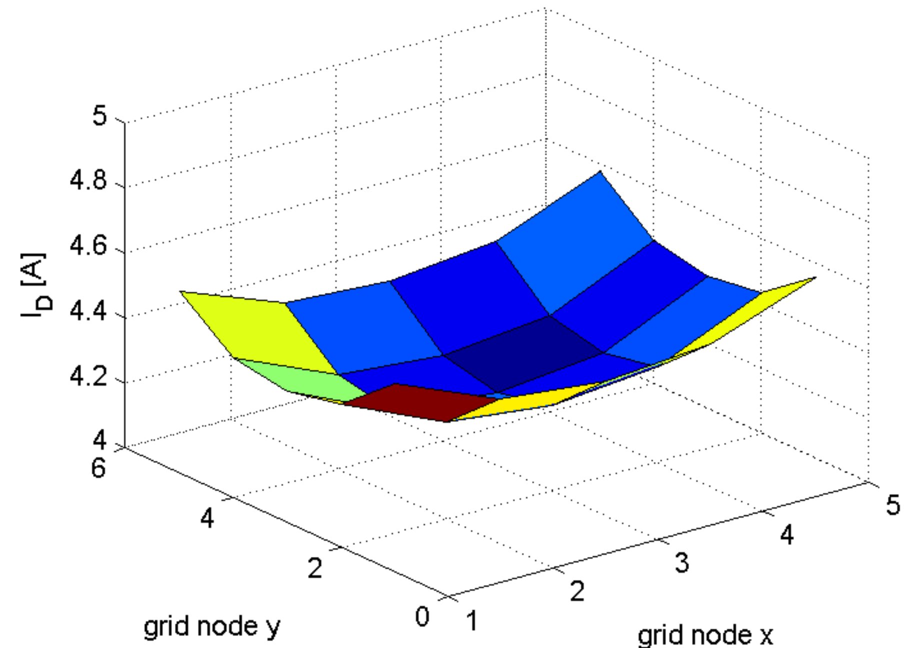


- ***Electro-thermal model yields good agreement with measurements***

Thermal simulations (9)

- **3D temperature and current distribution**



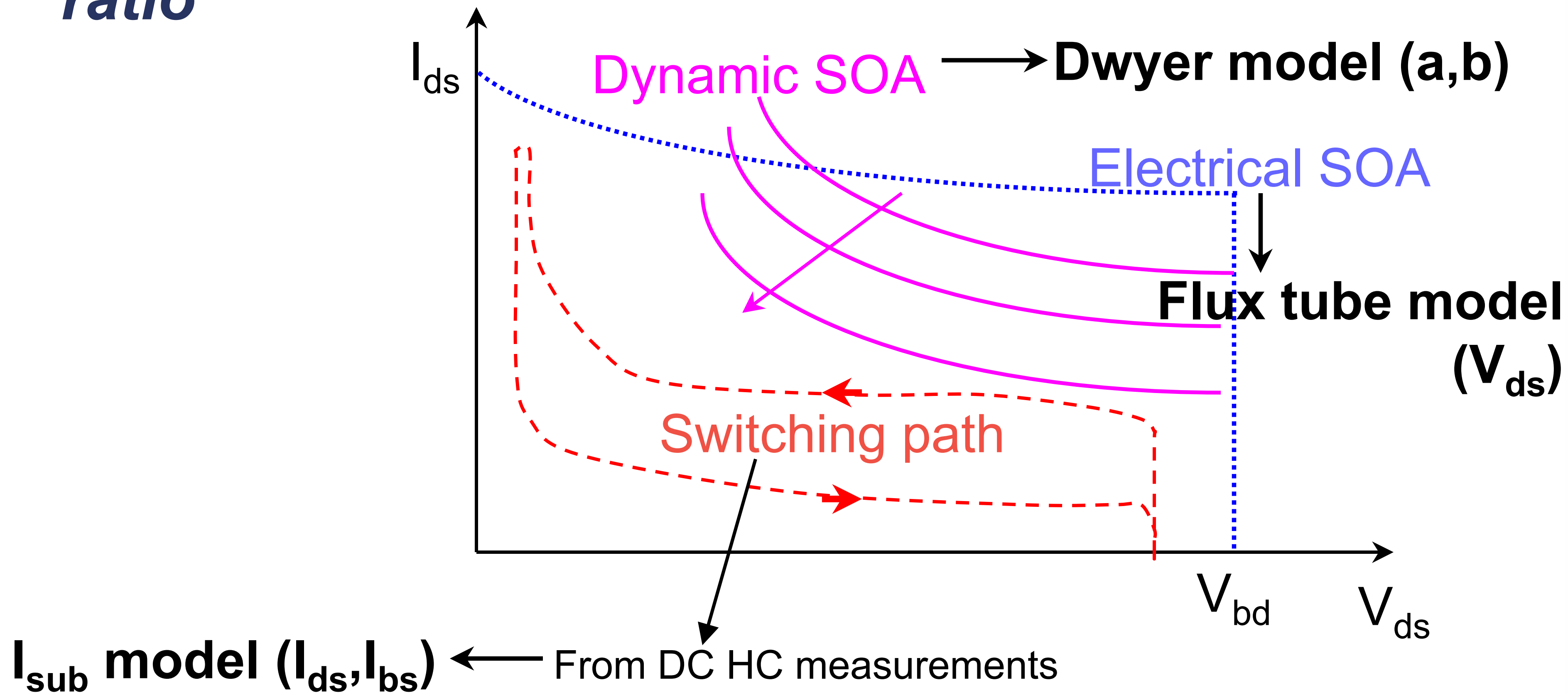


Overview

- Introduction
- Q&R Specifications
- Device Overview
- Reliability Measurements and Analysis Techniques
- Reliability Problems in Smart Power Technologies
- **Conclusions**

Conclusion : Total SOA (1)

- ***Electrical and DC SOA are independent of W***
- ***Dynamic SOA is dependent on area and aspect ratio***



Conclusion : Total SOA (2)

- ***Calculate static and AC HC degradation for a given device. Device must always operate within SOA.***
- ***Thermal SOA will determine ΔT_{device}, to be calculated using electro-thermal model. ΔT_{device} must be within technology specifications ($T_{junction} = T_{ambient} + \Delta T_{device}$). ΔT_{device} is largely dependent on the application.***

Acknowledgment

- G. Groeseneken, B. Elattari and E. Driessen, IMEC, Belgium
- W. Deceuninck, S. Aresu and J. Mertens, IMOMEC, Belgium
- B. Bakeroot, ELIS, Belgium
- D. Pogany and S. Bychikhin, TUV, Austria
- B. Desoete, D. Wojciechowski. F. Bauwens and K. Reynders, AMIS, Belgium
- COMPOSE project, funded by the IWT

References (1)

[1] J.G. Kassakian and D.J. Perrault, “The Future of Electronics in Automobiles”, *Proceedings of the International Symposium on Power Semiconductor Devices & ICs (ISPSD)*, 2001, pp. 15-19.

[2] H. Casier, P. Moens and K. Appeltans, “Technology Considerations for Automotive”, *Proceedings of the European Solid State Device Research Conference (ESSDERC)*, 2004, pp. 37-41.

[3] P. Moens et al.,“Intelligent PowerFET Technologies and Design Implementation Techniques”, *Proceedings of the International Symposium on Power Semiconductor Devices & ICs (ISPSD)*, 2004, pp. 85-88.

[4] A. Blessing, “Passive Components for High Temperatures : Application Potential and Technological Challenges”, *Proceedings of the 9th Annual Automotive Electronic Council (AEC),* 2004.

[5] M. Goroll, R. Pufall, W. Kanert and B. Plikat, “Semiconductors in high Temperature Applications – A Future Trend in Automotive Industry”, *Microelectronics Reliability*, **44**, 2004, pp. 1413-1417.

[6] P. Habas, Z. Prijic, D. Pantic, N.D. Stojadinovic, “Charge-pumping characterization of SiO2/Si Interface in virgin and irridiated power VDMOSFETs”, IEEE Transactions on Electron Devices, **43**, 1996, pp. 2197-2208.

[7] A.W. Ludikhuize, M. Slotboom, A. Nezar, N. Nowlin, R. Brock, “Analysis of hot-carrier-induced degradation and snapback in submicron 50V lateral MOS transistors”, *Proceedings of the International Symposium on Power Semiconductor Devices (ISPSD),* 1997, pp. 53-56.

[8] R. Versari, A. Pieracci, S. Manzini, C. Contiero, B. Ricco, “Hot carrier reliability in submicrometer LDMOS transistors”, *Proceedings of the International Electron Devices Meeting (IEDM),* 1997, pp. 371-374.

[9] M.S. Shekar, R. K. Williams, M. Cornell, M.-Y. Luo, M. Darwish, “Hot electron degradation and unclamped inductive switching in submicron 60-V lateral DMOS”, *Proceedings of the International Reliability Physics Symposium (IRPS)*, 1998, pp. 383-390.

[10] A. Pieracci, B. Ricco, “A new characterization method for hot-carrier degradation in DMOS transistors”, IEEE Transactions on Electron Devices, **45**, 1998, pp.1855-1858.

References (2)

[11] R. Versari, A. Pieracci, “Experimental study of hot-carrier effects in LDMOS transistors”, IEEE Transactions on Electron Devices, **46**, 1999, pp. 1228-1233.

[12] A.J. Mouthaan, C. Salm, M.M. Lunenborg, M.A.R.C. de Wolf, F.G. Kuper, “Dealing with hot-carrier aging in nMOS and DMOS, models, simulations and characterizations, Microelectronics Reliability, **40**, 2000, pp. 909-917.

[13] V.O’Donovan, S. Whiston, A. Deignan, C.N. Chleirigh, “Hot carrier reliability of lateral DMOS transistors”, *Proceedings of the International Reliability Physics Symposium (IRPS),* 2000, pp. 174-179.

[14] D. Brisbin, A. Strachan, P. Chaparala, “Hot-carrier reliability and design of N-LDMOS transistor arrays, *Proceedings of the International Reliability Workshop (IRW),* 2001, pp. 44-48.

[15] E. Landgraf, F. Hofmann, T. Schulz, H. von Philipsborn, “Substrate current and degradation of trench LDD transistors”, Solid State Electronics, **46**, pp. 965-970.

[16] S. Manzini, A. Gallerano, “Avalanche injection of hot holes in the gate oxide of LDMOS transistors”, Solid-State Electronics, **44**, pp. 1325-1330.

[17] D. Brisbin, A. Strachan, P. Chaparala, “Hot carrier reliability of N-LDMOS transistor arrays for power BiCMOS applications, *Proceedings of the International Reliability Physics Symposium (IRPS),* 2002, pp. 105-110.

[18] L. Labate, S. Manzini, R. Rogerro, “Hot-Hole-Induced Dielectric Breakdown in LDMOS transistors”, IEEE Transactions on Electron Devices, **50**, 2004, pp. 372-377.

[19] P. Moens, M. Tack, R. Degraeve and G. Groeseneken, “A Novel Hot-Hole Injection Degradation Mechanism for Lateral nDMOS Transistors”, *Proceedings of the International Electron Devices Meeting (IEDM),* 2001, pp877- 880.

References (3)

[20] P. Moens, G. Van den bosch and G. Groeseneken, “Hot Carrier Degradation Phenomena in Lateral and Vertical DMOS Transistors”, IEEE Transactions on Electron Devices, **51**, 2004, pp623-628.

[21] P. Moens, G. Van den bosch, C. De Keukeleire, R. Degraeve, M. Tack and G. Groeseneken, “Hot Hole Degradation Effects in Lateral nDMOS Transistors”, IEEE Transactions on Electron Devices, **51**, 2004, pp1704-1710.

[22] P.L. Hower, J.Lin, S. Merchant, “Snapback and safe operation area of Ldmos transistors”, *Proceedings of the International Electron Devices Meeting (IEDM),* 1999, pp. 193-196.

[23] K. Esmark, C. Fürböck, H. Gossner, G. Groos, M. Litzenberger, D. Pogany, et al., “Simulation and experimental study of temperature distribution during ESD stress in smart-power technology ESD protection structures”, *Proceedings of the International Reliability Physics Symposium (IRPS),* 2000, pp. 304-309.

[24] C. Fürböck, K. Esmark, M. Litzenberger, D. Pogany, G. Groos, R. Zelsacher, et al., “Thermal and free carrier concentration mapping during ESD event in smart power ESD protection devices using an improved laser interferometric technique”, Microelectronics Reliability, **40**, 2000, pp. 1365-1370.

[25] Y.S. Chung, “Junction temperature induced thermal snapback breakdown of MOSFET device”, IEEE Electron Device Letters, 23, 2002, pp. 615-617.

[26] P. Besse, N. Nolhier, M. Bafleur, M. Zecri, Y. Chung, “Investigation for a smart power and self-protected device under ESD stress through geometry and design considerations for automotive applications”, *Proceedings of the ESD/EOS Symposium*, 2002, pp. 348-353.

[27] R.M. Steinhoff, J.-B. Huang, P.L. Hower, J.S. Brodsky, “Current filament movement and silicon melting in an ESD robust DENMOS transistor”, *Proceedings of the EOS/ESD Symposium*, 2003, pp. 98-107.

[28]]P. Moens et al. “Effects of Hot Spot Hopping and Drain Ballasting in Integrated Vertical DMOS Devices under TLP Stress”, *Proceedings of the International Reliability Physics Symposium (IRPS),* 2004, pp393-398.

References (4)

[29] M. Denison, M. Blaho, P. Rodin, V. Dubec, D. Pogany, D. Silber, et al. “Moving current filaments in integrated DMOS transistors under short-duration current stress“, IEEE Transactions on Electron Devices, **51**, 2004, pp. 1695-1703.

[30] C. Duvvury, F. Carvajal, C. Jones, D. Briggs, “Lateral DMOS design for ESD robustness”, *Proceedings of the International Electron Devices Meeting (IEDM),* 1997, pp. 375-378.

[31] V.M. Dwyer, A.J. Franklin, D.S. Campbell, “Thermal failure in semiconductor devices”, Solid State Electronics, **33**, 1990, pp.553-560.

[32] T. R. Efland, C.-Y. Tsai, S. Pendharkar, “Lateral thinking about power devices (LDMOS)” *Proceedings of the International Electron Devices Meeting (IEDM),* 1998, pp. 679-682.

[33] S. Merchant, R. Baird, P. Bennet, P. Percy, P. Dupuy, P. Rossel, “Energy capability of lateral and vertical DMOS transistors in an advanced automotive smart power technology”, *Proceedings of the International Symposium on Power Semiconductor Devices & ICs (ISPSD),* 1998, pp. 317-320.

[34] P. Hower, C.Y Tsai, S. Merchant, T. Efland, S. Pendharkar, R. Steinhoff et al., “Avalanche-induced thermal instability in Ldmos transistors”, *Proceedings of the International Symposium on Power Semiconductor Devices & ICs (ISPSD),* 2001, pp.153-156.

[35] B.H. Krabbenborg, J. A van der Pol, “Robustness of LDMOS power transistors in SOI-BCD processes and derivation of design rules using thermal simulation”, *Proceedings of International Symposium on Power Semiconductor Devices & ICs (ISPSD),* 2001, pp. 157-160.

[36] S. Pendharkar et al., “Optimization of low voltage n-channel ldmos devices to achieve required electrical and lifetime SOA”, *Proceedings of the International Symposium on Power Semiconductor Devices & ICs (ISPSD),* 2002, pp. 261-264.

[37] V. Khemka, V. Parthasarathy, R. Zhu, A. Bose, T. Roggenbauer, “Experimental and theoretical analysis of energy capability of RESURF LDMOSFETs and its correlation with static electrical safe operating area”, IEEE Transactions on Electron Devices, **49**, 2002, pp. 1049-1058.

References (5)

[38] F. Alagi, L. Labate, A. Andreini, C. Contiero, “Sub-millisecond energy handling capability improvement of IC power devices with thick copper metallization, *Proceedings of the International Symposium on Power Semiconductor Devices (ISPSD),* 2003, pp. 249-252.

[39] V. Khemka, V. Parthasarathy, R. Zhu, A. Bose, T. Roggenbauer, “Detection and optimization of temperature distribution across large-area power MOSFETs to improve energy capability”, IEEE Transactions on Electron Devices, **51**, 2004, pp. 1025-1032.

[40] V. Khemka, V. Parthasarathy, R. Zhu, A. Bose, “A novel technique to decouple electrical and thermal effects in SOA limitation of power LDMOSFET”, IEEE Electron Device Letters, **25**, 2004, pp. 705-707.

[41] G. Van den bosch, P. Moens, P. Gassot, D. Wojciechowski and G. Groeseneken, “Analysis and Application of Energy Capability Methods in Power MOSFETS”, *Proceedings of the European Solid State Device Research Conference (ESSDERC)*, 2004, pp. 453-456.

[42] R. Zingg, “On the Specific On-Resistance of High-Voltage and Power Devices”, IEEE Transactions on Electron Devices, **51**, 2004, pp. 492-499.

[43] B. J. Baliga, “The Future of Power Semiconductor Device Technology”, *Proceedings of the IEEE 2001,* 2001, pp822-832.

[44] G. Amaratunga and F. Udrea, “Power Devices for High Voltage Integrated Circuits : New Device and Technology Concepts”, *Proceedings of the International Symposium on Power Semiconductor Devices (ISPSD),* 2001, pp. 441-448.

[45] B. Bakeroot, J. Doutreloigne and P. Moens, “A new substrate current free nLIGBT for junction isolated technologies”, *Proceedings of the European Solid State Device Research Conference (ESSDERC)*, 2004, pp.461-464.

References (6)

[46] P. Hower, "LDMOS Safe Operating Area", Tutorial ISPSD 2002.

[47] D. Pogany et al., "Extraction of Spatio-temporal Distribution of Power Dissipation in Semiconductor Devices Using Nanosecond Interferometric Mapping Technique", Appl. Phys. Letters, **81**, 2002, pp2881-2883.

[48] D. Pogany et al., Single-Shot Thermal Energy Mapping of Semiconductor Devices with Nanosecond Resolution Using Holographic Interferometry", IEEE Electron Device Letters, **23**, 2002, pp606-608.

[49] D. Pogany et al., "Moving Current Filaments in ESD Protection Devices and Their Relation to Electrical Characteristics", *Proceedings of the International Reliability Physics Symposium (IRPS),* 2003, pp241-248.

[50] C.T. Wang, "Hot carrier design considerations for MOS devices and circuits", New York, Van Nostrand-Reinhold Press, 1992.

[51] P. Heremans et al., "Analysis of the Charge Pumping Technique and Its Applications for the Evaluation of MOSFET Degradation", IEEE Trans. Electron Devices, **36**, 1989, pp1318-1335.

[52] S. Manzini and C. Contiero, "Hot-Electron-Induced Degradation in High-Voltage Submicron DMOS Transistors", *Proceedings of the International Symposium on Power Semiconductor Devices (ISPSD),* 1996, pp. 65-68.

[53] S. Aresu et al., "Evidence for source side injection hot carrier effects on lateral DMOS transistors", Microelectronics Reliability, **44**, 2004, pp1621-1624.

[54] P. Moens et al, "A 0.35 µm Based System-on-Chip Technology for 42V Battery Automotive Applications", *Proceedings of the International Symposium on Power Semiconductor Devices (ISPSD),* 2004, pp225-228.

[55] P. Moens, K. Reynders, S. Bychikhin, D. Pogany and M. Zubeidat, *"Optimization of Integrated Vertical DMOS Transistors for ESD Robustness", Proceedings of the International Symposium on Power Semiconductor Devices (ISPSD),* 2004, pp221-224.

References (7)

[56] N. Rinaldi, ''On the Modeling of the Transient Thermal Behaviour of Semiconductor Devices'', IEEE Trans. Electron Devices, **48**, 2001, pp. 2796-2802.

[57] N. Rinaldi, ''Generalised Image Method with Application to the Thermal Modeling of Power Devices and Circuits'', IEEE Trans. Electron Devices, **49**, 2002, pp. 679-686.

[58] C. Anghel, R. Gillon and A. Ionescu, ''Selfheating Characterization and Extraction Method for Thermal Resistance and Capacitance in HV MOSFETS'', IEEE Electron Device Letters, **25**, 2004, pp. 141-143.

[59] M. Denison, M. Pfost, K-W. Pieper, S. Markl, D. Metzner and M. Stecher, ''Influence of Inhomogeneous Current Distribution on the Thermal SOA of Integrated DMOS Transistors'', *Proceedings of the International Symposium on Power Semiconductor Devices (ISPSD),* 2004, pp. 409-412.