Design Issues and Considerations for Low-Cost 3-D TSV IC Technology

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***Abstract*—In this paper key design issues and considerations of a low-cost 3-D Cu-TSV technology are investigated. The impact of TSV on BEOL interconnect reliability is limited, no failures have been observed. The impact of TSV stress on MOS devices causes Vth shifts, further analysis is required to understand their importance. Thermal hot spots in 3-D chip stacks cause temperature increases three times higher than in 2-D chips, necessitating a careful thermal floorplanning to avoid thermal failures. We have monitored for ESD during 3-D processing and have found no events take place, however careful further monitoring is required. The noise coupling between two tiers in a 3-D chip-stack is 20 dB lower than in a 2-D SoC, opening opportunities for increased mixed signal system performance. The impact on digital circuit performance of TSVs is accurately modeled with the presented *RC* model and digital gates can directly drive signals through TSVs at high speed and low power. Experimental results of a 3-D Network-on-Chip implementation demonstrate that the NoC concept can be extended from 2-D SoC to 3-D SoCs at low area (0.018 mm^2) and power (3%) overhead.**

***Index Terms*—3-D, CU TSV, ESD, mechanical stress, network-on-chip, noise coupling, thermal behavior.**

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I. Introduction

THROUGH Silicon Vias (TSVs) are an essential technology towards higher and more heterogeneous system integration. 3-D TSV (through silicon via) technologies promise increased system integration at lower cost and reduced footprint [1], as well as performance improvement such as increased bandwidth and easier reuse by mixing and matching existing silicon. Variants of 3-D technologies have recently been introduced in application areas such as DRAM stacking [2], imagers [3], [4], SSDs (Solid-StateDrives) [5].

In Fig. 1 the different proposed 3-D integration schemes are categorized by their most important feature, via diameter/pitch and via aspect ratio. Three categories are distinguished. The large size 3-D-WLP (Wafer Level Packaging) TSVs have diameters larger than 10 μm and serve as bondpad I/O interconnect in systems. They are typically manufactured post-foundry and are compatible with both wafer-to-wafer and die-to-wafer stacking schemes. Because of their rather large size (diameter) small aspect ratios around one or two enable integration in wafers with thickness of 70 μm or more, greatly easing wafer and die handling. The medium size 3-D-SIC (3-D Stacked IC) TSVs have diameters between 2 and 10 μm and serve as global interconnect. They are manufactured at the foundry and are compatible with wafer-to-wafer and die-to-wafer stacking schemes. An aspect ratio of 5 or higher leads to wafer thickness between 25 μm to 70 μm, making wafer and die handling challenging. The 3-D-SIC TSVs are an emerging technology and are expected to appear in applications in the coming years. The smallest size 3-D-IC TSVs with diameter size of 2 μm and smaller target intermediate level interconnect. Even with aspect ratio above 20 they require extremely thinned dies. Their stacking scheme is typically wafer-to-wafer to avoid complex and difficult thin die handling. The 3-D-SIC intermediate level interconnect TSVs are considered risk technology at this time. In this paper, we focus on the emerging Cu 3-D SIC TSV technology, as it is well balanced between cost and application flexibility. It is attractive from cost perspective as it leverages existing CMOS process equipment and it supports die-to-wafer stacking. The latter creates the possibility to stack dies of different sizes, and thus not add unnecessary constraints during system partitioning and floorplanning, which may limit die utilization.

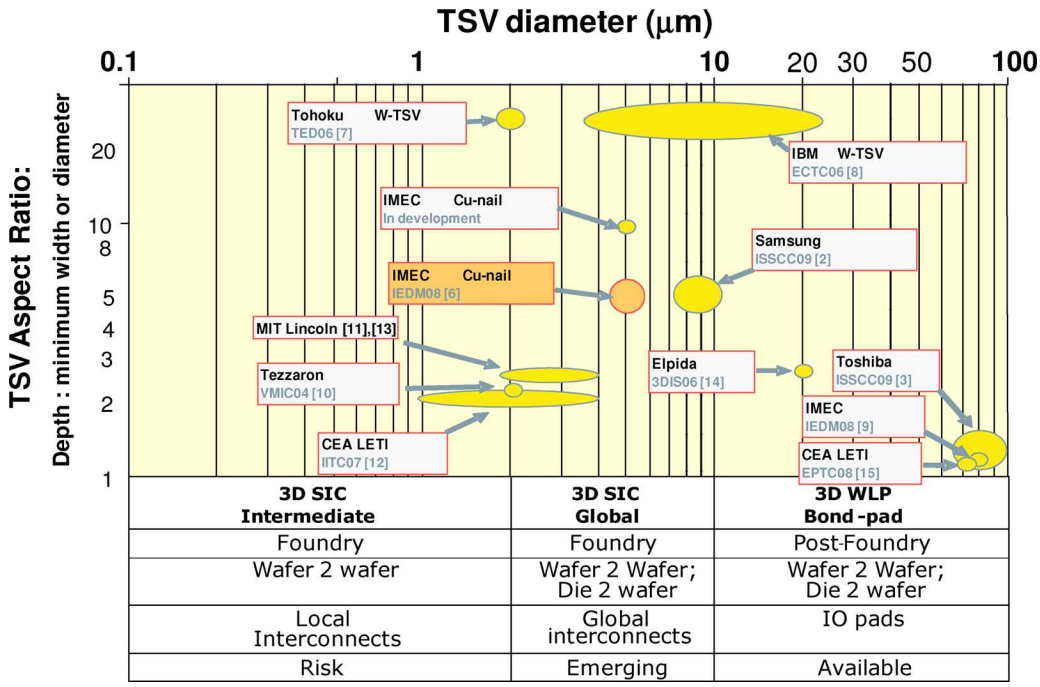


Fig. 1. Overview of 3-D TSV technologies as function of TSV diameter and aspect ratio and classification in 3 categories, 3-D-SIC intermediate and global and 3-D WLP Bondpad with their key attributes.

In this work we investigate in detail the design issues and solutions of a low cost 3-D TSV Stacked-IC technology [16]. The technology we propose offers a 10 μm TSV pitch that enables applications such as logic-on-logic, DRAM-on-logic and RF-on-logic. We present experimental data on key issues such as impact of TSV on MOS devices and back-end-of-line (BEOL), reliability, thermal hot spots, ESD, signal integrity and circuit performance. We point out where changes in current design practices are required to realize the low-cost potential of the technology. We also demonstrate a key circuit for the deployment of the Cu TSV technology: a 3-D Network-on-Chip (3-D-NoC). The 3-D-NoC will serve as the back-bone communication IP for future 3-D-SoC, as it does today in many 2-D SoCs. We show that the NoC concept can easily be extended to 3-D at low area and power overhead.

This paper is structured as follows. In Section II we introduce the low-cost 3-D Cu TSV technology used in this paper and we review the main characteristics of the Cu TSVs. In Section III the mechanical issues of the 3-D technology are discussed, these are the impact of TSVs on the reliability of the BEOL interconnect and TSV stress impact on MOS devices. In Section IV the thermal behavior of 3-D chip-stacks is discussed and a thermal-aware design approach is proposed to avoid hot spots. In Section V the following electrical issues are reviewed: ESD in 3-D chip-stacks, noise coupling level in 3-D compared to 2-D, and digital signaling through TSV in ring oscillators. In Section VI we present a 3-D-NoC demonstrator circuit that shows the 2-D NoC concept used in SoC is compatible with 3-D technology. In Section VII the main results of the paper are summarized.

II. Low Cost 3-D Cu TSV Technology

In this section we briefly describe the 3-D technology and test vehicle that was used in the experiments reported in this paper. Next we review the main characteristics of the Cu TSVs, resistance, capacitance, leakage and yield.

A. Technology Description

The proposed 3-D stacked IC (3-D-SIC) approach leverages existing IC foundry infrastructure to fabricate TSVs after the FEOL processing and prior to BEOL processing [6]. In a 200 mm/130 nm FEOL CMOS technology with Cu/SiO2 BEOL, TSVs are fabricated with 5 μm diameter and a minimum pitch of 10 μm. After the TSV is etched, an isolation layer is deposited followed by the Cu metallization of the TSV, Fig. 2. The wafers then go through the standard BEOL process. To enable interconnections using TSVs, the wafer is thinned down to $\sim$ 25 μm and next TSVs are exposed to a height of $\sim$ 700 nm. The thinned wafers are then diced and the resulting dies are stacked face-up on the regular thickness landing wafer with a collective hybrid bonding process in a die-to-wafer approach [17]. This approach reduces the cycle time by the parallel processing of the relatively long Cu-Cu thermo-compression step and the die-to-wafer configuration allows the selection of Known Good Die prior to stacking, both reducing overall cost of the 3-D processing.

Using this technology we have built a test vehicle as is shown in Fig. 3. The thinned die is stacked face-up on top of the landing wafer (SEM picture of the stack in Fig. 3). A cross section through a TSV array shows the 25 μm high, 5 μm diameter Cu TSVs at a minimum pitch of 10 μm. The electrical and mechanical Cu-Cu bonding is visible at the bottom of the picture, the

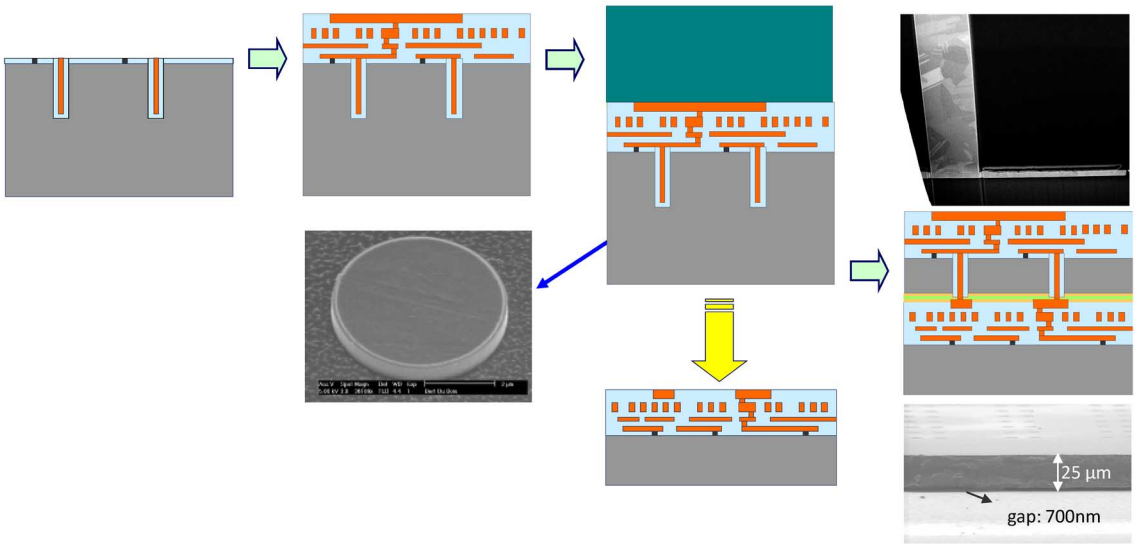
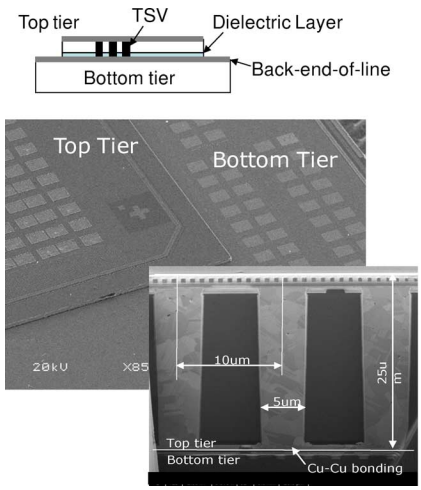


Fig. 2. Process flow of low-cost 3-D Cu TSV technology, Cu TSV are processed after FEOL and before BEOL, next wafers are thinned and dies singulated. Stacking is performed die to wafer with simultaneous Cu-Cu thermo-compression to create mechanical and electrical connections simultaneously.



TSV diameter	5um
Min. TSV pitch	10um
Top tier die thickness	25um
TSV Isolation layer thickness	120n
Dielectric layer thickness	0.7um

Fig. 3. SEM picture of test vehicle with FIB cross section inset (left); summary of dimensions in table (right).

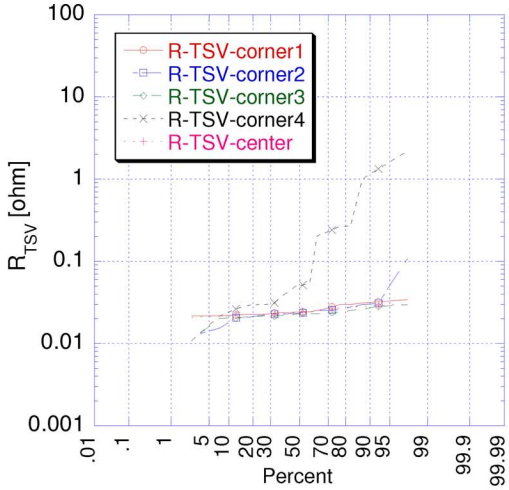
TSV lands on the top metal of the lower tier. The TSV isolation (liner) is 120 nm thick and the dielectric layer isolating the two tiers is 700 nm thick. These geometric parameters are summarized in the table in Fig. 3.

B. Electrical TSV Characteristics and Yield

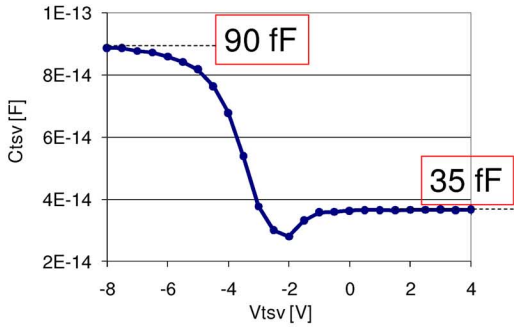
DC Resistance and low frequency capacitance are fundamental electrical parameters of TSVs. Measure of TSV resistance between the top of the TSV and the landing pad provides information on the quality of the vertical electrical connection established by the bonding of the staked dies. With the proposed TSV dimensions, TSV resistance is expected to be in the order of few tens of milliohms in good TSVs. Therefore, the resistance test structure consists of a single TSV in a 4-point or Kelvin configuration. The Kelvin TSV is placed the four corners and in the center of each stacked die. The measured values show $\mathrm{R_{TSV}}$~20 mΩ; the spread over different die locations and over 17 dies is limited (Fig. 4(a)), thus indicating a good quality of 3-D stacking and bonding.

Dense clusters of TSVs, consisting of arrays of 6×6 TSV where each TSV is measured in a 2 point configuration for assessing the 3-D connectivity only, show an evident pitch dependency of the TSV yield. In particular, TSVs in the array periphery do not provide good electrical connections at 15 μm pitch. On the other hand, overall good yield is obtained for 20 μm pitch Fig. 4(c).

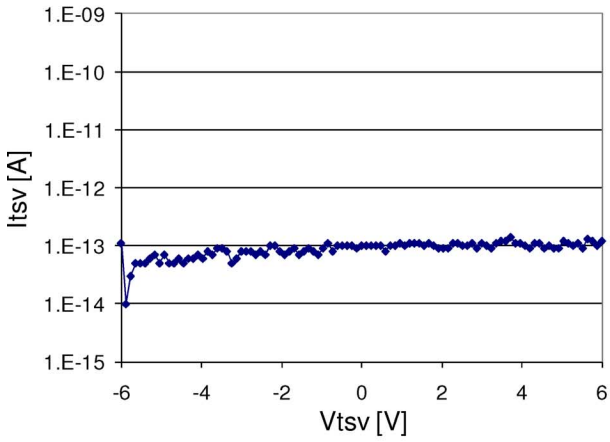
TSV capacitance is an essential parameter for 3-D circuit design. Since the TSV forms a cylindrical MIS (Metal-Insulator-Semiconductor) capacitor with the substrate, it is expected that this capacitance is non-linear and depends on the biasing of the TSV with respect to the substrate. TSV capacitance values are expected to be in the order of $\sim$ 100 fF. These are too low for the accuracy of a standard LCR meter; therefore, arrays of 32 TSVs connected in parallel are used to measure a larger value of capacitance, which is then averaged over the number of TSVs in the parallel array. De-embedding structures are also characterized to reduce the impact of parasitics on the measurements. C-V plots of TSV capacitance @ 1 MHz (Fig. 4(b)), show a



(a)



(b)



(c)

Yield		TSV pitch=15um			
0.35	0.53	0.53	0.71	0.53	0.35
0.65	0.88	1.00	1.00	0.88	0.65
0.71	1.00	1.00	1.00	1.00	0.76
0.71	1.00	1.00	1.00	1.00	0.82
0.47	1.00	1.00	1.00	1.00	0.53
0.29	0.47	0.65	0.35	0.24	0.24

Yield		TSV pitch=20um			
0.76	0.88	0.88	0.82	0.94	0.76
0.94	0.88	1.00	1.00	0.88	0.94
0.94	1.00	1.00	1.00	0.94	1.00
0.94	1.00	1.00	1.00	1.00	1.00
0.82	1.00	1.00	1.00	1.00	1.00
0.65	0.65	0.76	0.82	0.82	0.71

(d)

Fig. 4. Summary of TSV characteristics: (a) cumulative distribution of TSV resistance for different locations on the die, (b) TSV capacitance (C-V) as function of bias voltage shows 90 fF in accumulation and 35 fF in depletion mode, (c) TSV leakage as function of bias voltage is well below 1 pA and (d) TSV yield (1.00 is 100% yield) as function of location of TSV in a 6×6 TSV array with varying pitches, TSVs at the edge of the matrix have lower yield than at center especially at 15 μm pitch.

$C_{TSV} \sim 37$ fF in depletion and a $C_{TSV} \sim 92$ fF in accumulation mode. TSV leakage, measured in the same array used to measure capacitance, is below 1 pA in depletion and accumulation modes (Fig. 4(d)).

Both R_{TSV} and C_{TSV} match well with Raphael™ and Sdevice™ simulations, respectively, performed by using expected TSV dimensions after processing, with the same methodology proposed in [18].

III. Mechanical Issues and Considerations in 3-D TSV Technology

Due to the difference in thermal expansion coefficient of Cu and Si, the TSV induces stress on its surroundings [19], potentially leading to reliability problems. To detect reliability problems, back-end-of-line structures such as vias and serpentine wires have been added next to and on top of TSVs. After stacking the test vehicle these structures were characterized and showed no failures. Next, these test structures have been subjected to thermal cycling. After 1000 cycles of 30 min between $-55°$ and 125°C no failures have been observed on 17 samples. This is a first level of reliability testing of 3-D TSV technology, further reliability tests are needed to confirm these findings, as well as package level reliability tests to assess lifetimes of systems.

The stress generated by TSV potentially impacts the active device electrical performance, to avoid this proximity effect devices can be spaced away from TSV (keep-out-zone, KoZ) at the expense of increased overall area and cost. The TVS proximity influence on active devices has been investigated for a wide range of physical gate lengths. We observed that the transistors figures of merits like the current factor, the saturation voltage and the drive current are slightly affected by the presence of a TSV in the vicinity of the transistors (Fig. 5). The cumulative probability plot of saturation threshold voltage for a short (0.13 μm) and large (1 μm) physical gate length of n-type device measured on thinned (25 μm) and stacked dies. The threshold voltage shows a slight increase for the longer devices (Fig. 5(b)). This variation has also been measured for the current factor, drive current of n-type devices and also for p-type devices. Further modeling and characterization of the stress impact on MOS

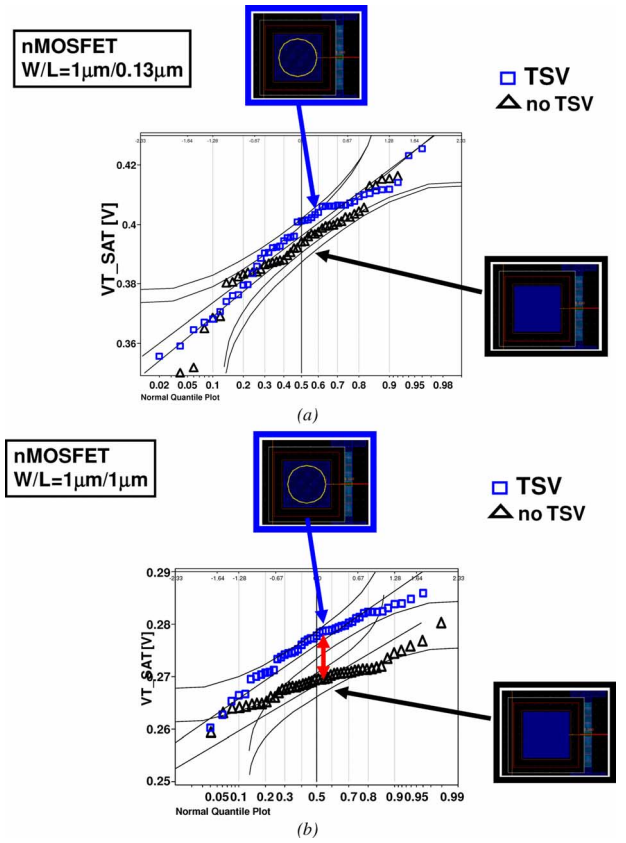


Fig. 5. Impact of TSV proximity on short channel and long channel devices in a 130 nm technology: no Vth shift is visible on 130 nm length device (a), about 10 mV Vth shift is observed on 1 μm length device (b).

devices is needed to gain a better insight and asses the severity of this issue. To avoid large keep out areas (areas in which no devices are placed) and increase cost of the use of 3-D TSV technology, models and tools to design for TSV impact on devices are recommended [20].

IV. Thermal Issues and Considerations in 3-D TSV Technology

Unless the power dissipation is carefully managed across the tiers in a 3-D stack, hot spots may occur. The reduced thermal spreading in the thinned dies and the poorly thermally conductive adhesives used for the vertical integration, lead to high thermal resistances. The same power dissipation in a stacked die package will lead to higher temperatures and a more pronounced temperature spreading compared to a single die package. To study the thermal impact of hot spot size and power density on 3-D stack design, thermal finite element simulations were performed. Two simulation setups have been used. The fine grain simulation of [21] takes into account the complete BEOL and layout structure whereas in the FEM simulation of [22] simplified models are using volume-averaged material properties. These finite element simulations have been calibrated with a test structure that consists of heaters integrated with thermal sensors (diodes). Heaters with a size of 50×50 μm^2 and 100×100 μm^2 are located in the metal 2 layer of the BEOL in the top tier of the 3-D chip-stack, as well as in a 2-D reference die. Both

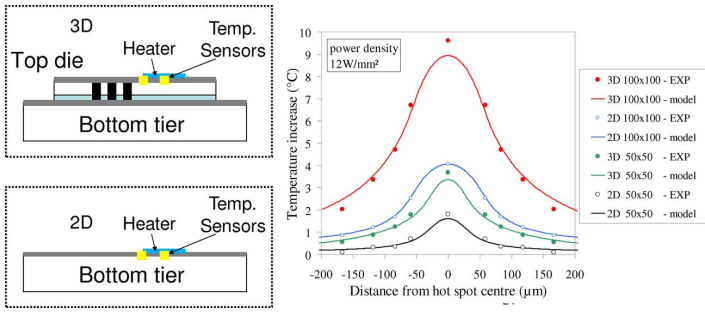


Fig. 6. Temperature increase on the top die in a 3-D chip-stack caused by a 100×100 μm hot spot is approximately three times higher (red curve) than the temperature increase in a 2-D SoC chip (blue curve).

in the top and the bottom die of the stack, a set of five diodes at different distances from the hot spot centre are added are integrated below the heater. This configuration of diodes allows capturing the local temperature peak due to the hot spot power dissipation. The simulation results and experimental validation [23] (Fig. 6) indicate that power dissipation in a 3-D stacked structure approximately has a ~ 3 times higher maximum temperature increase compared to the 2-D reference case, requiring thermal-aware floor-planning to avoid thermal problems in the stack.

To implement the thermal-aware floor-planning in 3-D stacks, a thermal compact model has been developed [24]. With this model, the temperature distribution is calculated in each die, using the power maps of the heat generation in each tier as input. This compact model allows studying the thermal interaction of heat sources in the 3-D stack, both on the same die as well as on other levels of the stack. Furthermore, the compact model allows thermal optimization of the placement of the heat sources as a function of the geometrical and material properties of the interface and interconnects structures. Fig. 7 shows the graphical interface of this thermal compact model.

V. Electrical Issues and Design Considerations in 3-D TSV Technology

A. ESD

During the die to wafer stacking process, the top die can discharge through the TSV's into the bottom wafer, resulting in a Charged Device Model (CDM)-like event. The potential need to protect each TSV for ESD may increase the footprint of 3-D connections and hence increase cost of using 3-D technology. Experimental results in the presented technology indicate that no ESD protection is needed and that standard ESD safe-guarding during 3-D process steps is all that is required. Unprotected transistor gates were chosen as monitor since they are most sensitive to ESD events in advanced CMOS technologies. These are connected to TSV's in various connection schemes (Fig. 8). Statistical DC measurements of the leakage current of all ESD monitor variations were collected across the full wafer with stacked dies. The gate-leakage is observed to monitor ESD events, no increase is found (Fig. 8). In total 420 devices were measured over 2 lots and 2.6% abnormalities

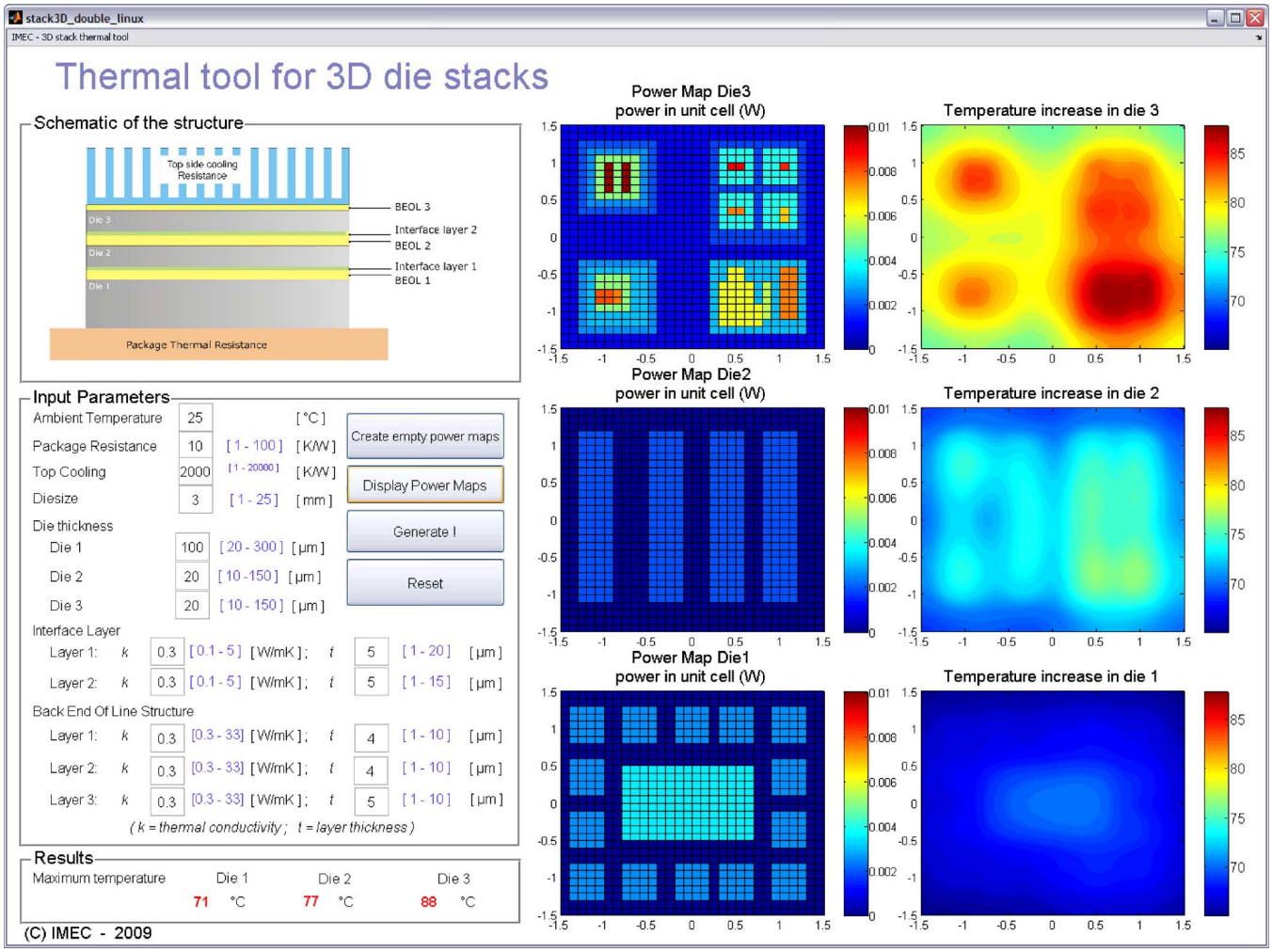


Fig. 7. Graphical interface of the thermal compact model for 3-D stacked structures.

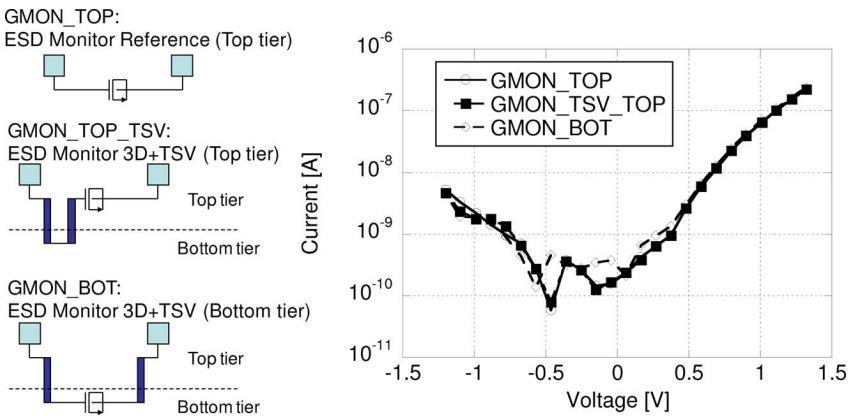


Fig. 8. The leakage currents of ESD monitors (GMON_TOP reference, GMON_TOP_TSV and GMON_BOT) have been measured after stacking: monitors connected through TSVs see no failures (gate shorts) and no significant change versus reference structure GMON_TOP (without TSV).

were detected. These abnormalities resulted consistently in a leakage decrease which excludes gate oxide damage by ESD as a root cause. However, continuous monitoring of future process lots needs to be performed consistently in order to detect possible future ESD occurrences when 3-D technology evolves.

B. Noise Coupling

Experimental results indicate that substrate noise isolation between stacked tiers is 20 dB superior compared to 2-D, creating significant opportunities for mixed-signal and RF applications. A 60 GHz voltage controlled oscillator (VCO) circuit has been implemented both in 2-D and on the top tier in a 3-D stack

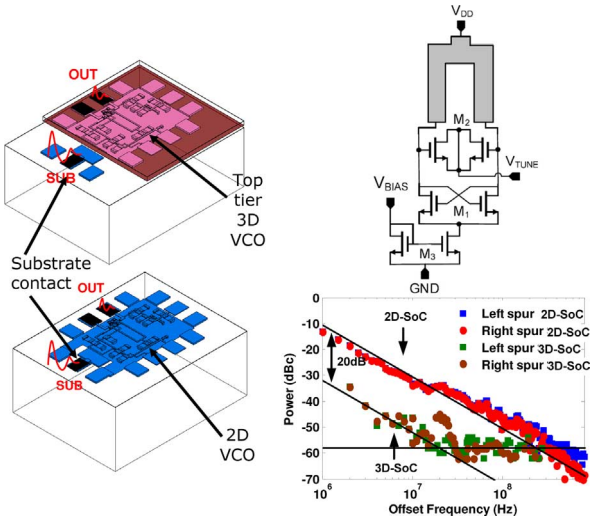


Fig. 9. 2-D SoC and 3-D chip-stack mmWave VCO implementation and schematic: 20 dB reduction of noise coupling in 3-D versus 2-D is observed.

(Fig. 9) to verify the isolation of 3-D versus 2-D. The VCO performance (center frequency, phase noise) is unaffected by the stacking operation. Both on the 2-D chip and the bottom tier of the 3-D stack a controlled "substrate noise" signal is injected to measure noise coupling as in [25]. This substrate noise signal emulates the switching activity of a digital circuit. The emulating waveform is a sine-wave with a frequency that is varied from 1 MHz to 1 GHz, which in practice extracts the coupling in the frequency domain. Due to coupling into the VCO the noise signal appears as unwanted spurs at the output of the VCO at an offset equal to its frequency. The level of the spur power is a measure for the noise coupling, or in other words a lower spur power shows that the isolation is better. The 3-D version exhibits a 20 dB lower level of spur power than the 2-D SoC variant throughout the frequency range of noise from 1 MHz to 30 MHz beyond which the 3-D spur level drops below noise. This indicates isolation is 20 dB better in the lower frequency range up to 30 MHz and noise of 2-D-SoC variant exceeds noise in 3-D up to 300 MHz (Fig. 9). This improved isolation capability of 3-D technology opens up opportunities for high performance mixed-signal system design.

C. Transmitting Digital Signals Through TSVs

Ring Oscillator (RO) is a standard digital circuit to analyze a particular technology and it is used to verify the feasibility of 3-D circuits and the impact of TSV on digital signaling and circuit operation. 2-D and 3-D RO circuits with varying number of stages and inverter sizes are compared. 21 and 41-stage 3-D ring oscillators with 1 TSV/stage and without TSVs are implemented as shown in Fig. 10. All RO configurations have their output connected to 8 stage frequency divider (divide by 256) to enable reliable frequency measurements (0.1–200 MHz). To predict the performance of a 3-D circuit, calibrated device models for the transistors along with lumped "T" *RC* model of the TSV [18] with measured R_{TSV} and C_{TSV} values are used. Simulation results of power-delay characteristics of the functional RO implementation are well in agreement with measurements suggesting that the model with extracted values can also be extended for predicting the performance of more complex 3-D circuits. It can be also seen that because of smaller inverter sizes the delay exhibited by 21 stage 3-D RO is larger when compared to the delay caused by 41 stage 3-D RO. Hence, in real circuit applications, strong driver elements are necessary to limit the delay caused by TSV in 3-D circuits.

VI. 3-D Network on Chip Demonstrator Circuit

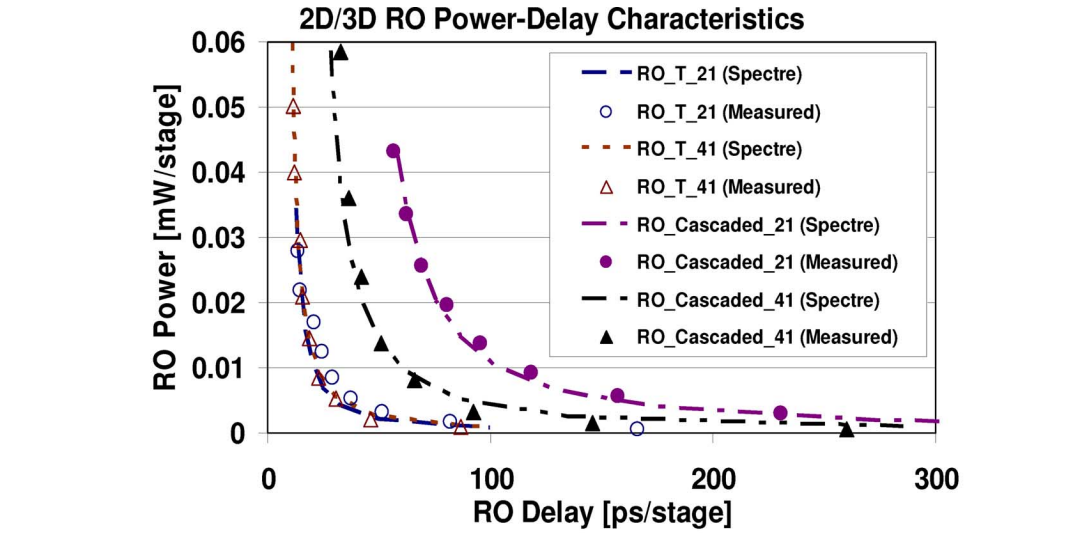
The communication architectures of choice in today's state-of-the-art designs are structured and scalable Networks-on-Chip [26], [27]. The extension of the NoC paradigm to 3-D integrated circuits is very promising, as modularity and scalability are even more critical for future three-dimensional integrated systems [28].

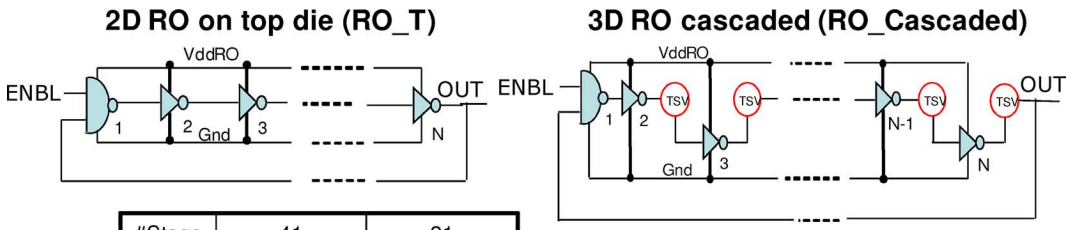
To demonstrate the feasibility of this communication architecture, we designed and manufactured a 16-bit 3-D NoC distributed across two tiers using the iNoCs synthesizable NoC IP and tool chain, with extensions for supporting vertical links (Fig. 11). Each tier consists of a traffic generator, a slave memory, a 3×3 switch and a JTAG controller. The traffic generators mimic logic IP components and can send/receive data packets at NoC speed to and from the memory on each tier. A JTAG controller is inserted on each tier to support Known-Good-Die testing before stacking. It also supports testing of the 3-D link after stacking. Note that the test pads of the bottom tier are no longer accessible after stacking. Therefore, these are replicated on the top tier. The PAD SELECT MUX connects these replicated pads to the JTAG bottom block if the top die is present.

A 2.5D design approach was followed to layout the 3-D NOC, i.e., each tier was independently designed but for the TSVs of which the position was aligned on both tiers during P&R. In total 100 TSVs are used to interconnect both tiers: 12 for 2×6 for VDD/GND, $2 \times (2 \times 16)$ for the 3-D link, 3×8 for the test. Both tiers are manufactured in a the 200 mm/130 nm FEOL CMOS technology with Cu/SiO2 BEOL and 3-D Cu TSV as described in Section I.A. The die-to-wafer configuration allows the selection of KGD prior to stacking, reducing cost of the 3-D processing.

The NoC switches in each tier are connected through a TSV link. Each signal line across the 3-D link is implemented with a standard CMOS buffer (BUFBD2) attached to two TSVs (Fig. 12). TSV duplication per signal is used to protect the link against TSV opens, which is the most frequently occurring fault in our process technology (as described in Section II.B). No ESD protection is used on the 3-D link, as our experimental results indicate that sufficient safe-guarding during 3-D process steps is all that is required (Section V.A).

When activating the NoC, we first enable KGD die testing by ensuring that each 3-D input signal on each tier is driven to a logic value. To this end, we have attached a weak pull down diode to each TSV. The leakage current of the diode in inversion ensures that the input signal of the receiving tier (the TSV_SLECT_MUX) is not floating. Second, we have added the TSV_SLECT_MUX to collect statistics on TSV yield. With this MUX each TSV can be individually tested at boot time through





#Stage	41	21
W_p/L_p	6µm/0.13µm	2µm/0.13µm
W_n/L_n	3µm/0.13µm	1µm/0.13µm

Fig. 10. Ring oscillator schematic (2-D and 3-D), sizing information (21 and 41 stages) and comparison 2-D versus 3-D measurements and simulations.

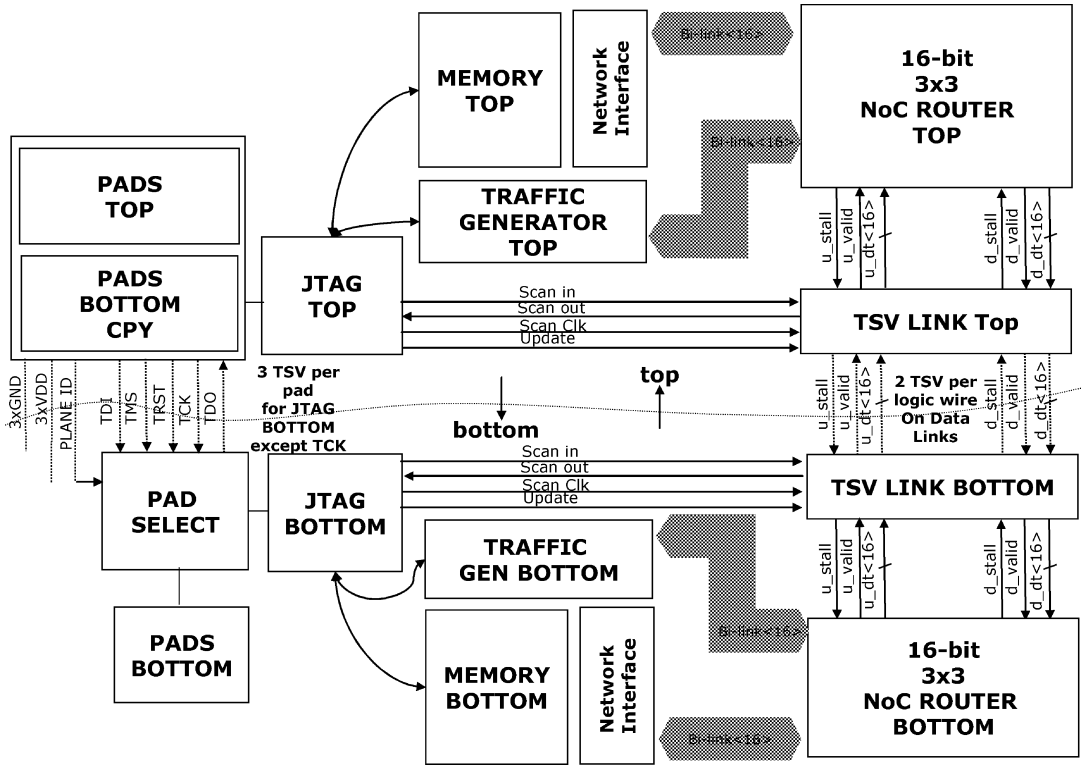


Fig. 11. 3-D NoC schematic, indicated are the circuits embedded in the top tier and the circuits embedded in the bottom tier. The TSVs connecting both circuits are identified and use two or three TSVs per signal to have robustness.

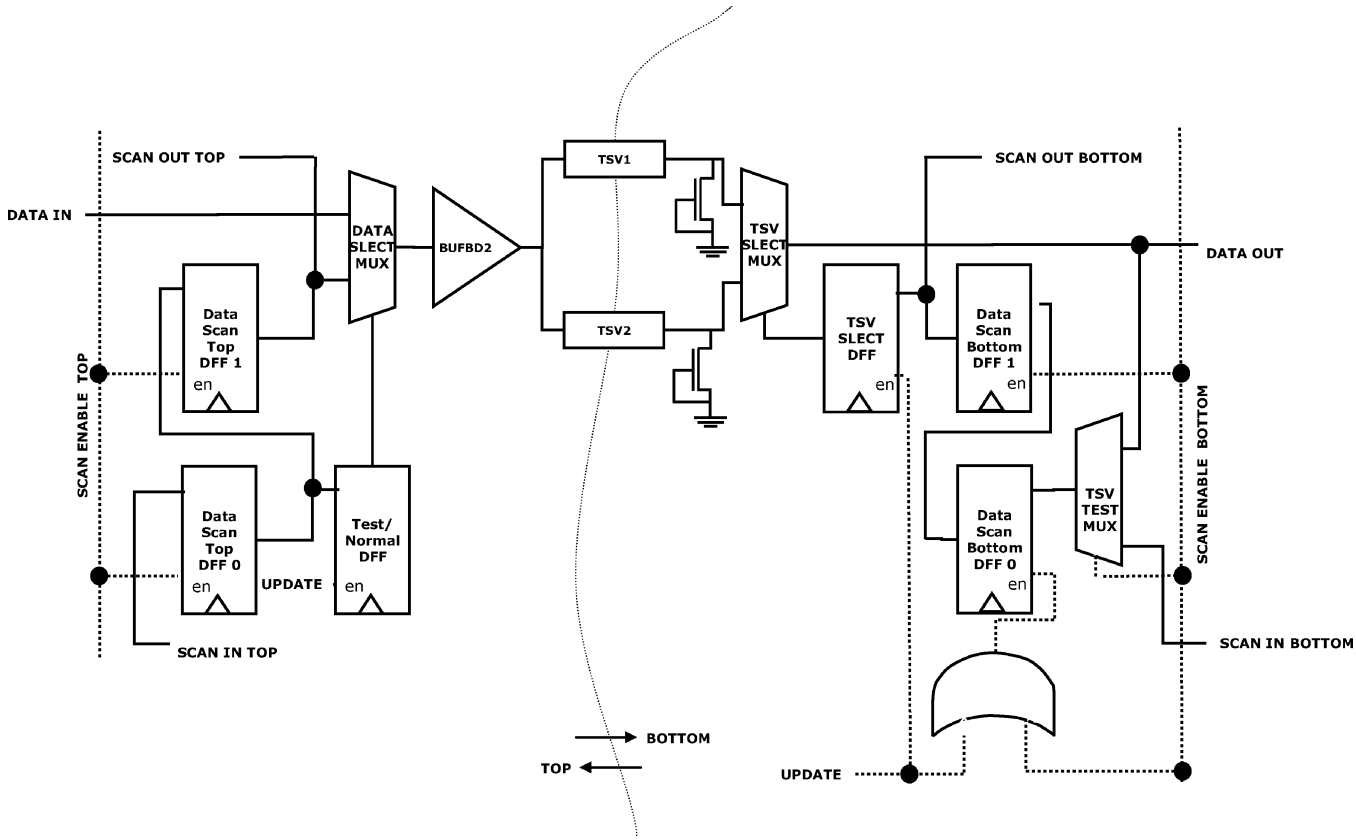


Fig. 12. TSVs for data links are tested using a scan chain and multiplexer. After testing the TSV that functions correctly is selected.

the scan-chain. A test pattern is injected into the scan registers and applied by setting the DATA_SLCT_MUX. After transmitting the data, the receiving register is sampled and scanned in order to detect faulty TSVs. Based on simulation, the redundant TSV and TSV_SLECT_MUX increase the 3-D link delay by 1.6 $\times$, and its power consumption by 1.8 $\times$ with respect to a single CMOS buffer (BUFBD2) driving a single TSV. In case of a TSV process technology where TSV shorts to bulk frequently occur, the above TSV IO scheme can be adapted by replacing the buffer driving both TSVs with a DEMUX, controlled by additional configuration memories. The DEMUX can then disconnect the failing TSVs from the buffers driving them.

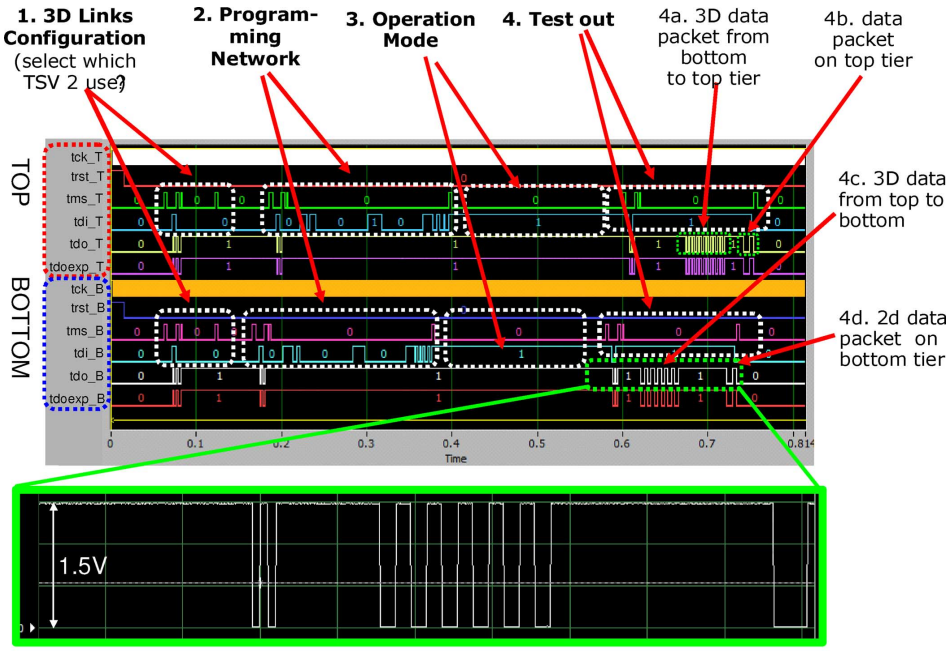
The 3-D NoC operation is depicted in Fig. 13(a). After power on, the design is switched in test mode. First, we program which 32 TSVs out of the total 64 are used for transmitting data on the data link (step 1). Second, we configure what data patterns traffic generators should transmit (step 2). Thereafter, the NoC is switched in operation mode (step 3). In the depicted test-case, short bursts of 32-bits are transmitted in 96-bit network packets. The packets are respectively sent in 3-D across the TSV links from the top(bottom) traffic generator to the bottom(top) memory or in 2-D from the bottom(top) traffic generator to the bottom(top) memory. Finally, the data is scanned out again. The output (tdo) corresponds with the expected output (tdo_exp), confirming a successful operation of the 3-D NoC. Separately, we have tested the 3-D link by transmitted alternating patterns of 0–1/1–0 transitions across the TSV link. So far, we have not found failing TSV on the 3-D NoC link (Fig. 13(b)).

The additional area penalty for the TSVs in the 3-D stack is limited to 0.018 mm^2 (Fig. 14). We have placed the TSV interconnect in a regular array of two columns with a pitch of 13 μm next to the standard cell core area to optimize yield. In this way we avoided TSV proximity impact as discussed in Section III, at the expense of slightly increased overall area. The power penalty for 3-D data transfers is only 3% with respect to sending the same continuous stream of 32-bit data bursts in 2-D, between memory and traffic generator spaced at less than 0.5 mm on the same tier. For 3-D communication at 50 MHz supply 1.39 mW is consumed from a 1.2 V compared to 1.34 mW for 2-D. The delay of the 3-D link is 183 ps, enabling high speed data transfers. The 3-D interconnects in the NoC can be designed to operate at a much higher speed. Characterization of ring oscillators driving TSVs shows that data can be transferred across a TSV in less than 150 ps while consuming less than 2 pJ/bit energy at 1.2 V (Section V.C). TSVs thus enable transferring of data between dies at a similar speed than intra-die data.

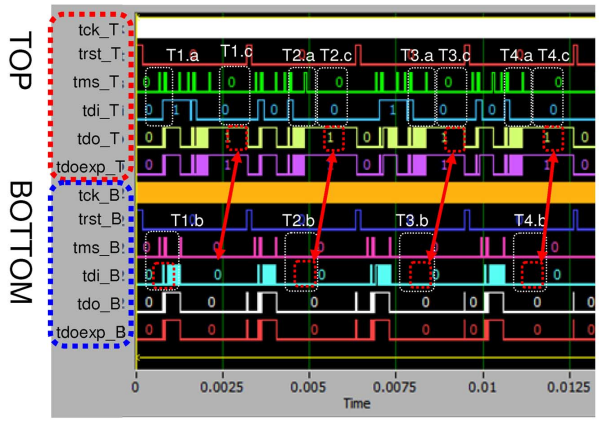
In this section, we have demonstrated a testable 3-D NoC manufactured using a low cost 3-D TSV Stacked-IC technology. This result indicates that modular integration of scalable systems with IP components distributed across multiple dies is feasible.

VII. Summary and Conclusions

In this paper key design issues and considerations of a low-cost 3-D Cu-TSV technology have been investigated.



(a)



	Description	Note
T1a	Select ***TSV1*** TOP	
T1b	TEST	0->1;
T1c	ScanOut BOTTOM	
T2a	Select ***TSV2*** TOP	
T2b	TEST	0->1
T2c	ScanOut BOTTOM	
T3a	Select ***TSV1*** TOP	
T3b	TEST	1->0;
T3c	Scanout BOTTOM	
T4a	Select ***TSV2*** TOP	
T4b	TEST	1->0
T4c	Scanout TOP	

(b)

Fig. 13. Output of scope during wafer-level test; (a) transmission of data burst across TSV links. The expected output (tdo) matches with logic simulation (tdo_exp). Measured maximum performance (25 Mhz@0.4–1.5 V) is limited by wafer-level test setup; (b) JTAG test results of TSVs in d_link (from bottom to top tier); all 38 TSVs in this link are functionally working.

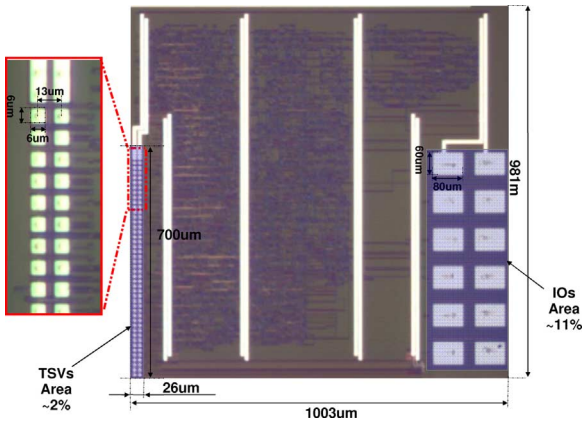


Fig. 14. Microchip photograph of the top tier of the 3-D NoC, indicated are the area consumed by the TSV array ($\sim 2\%$), cell NoC core including drivers ($\sim 87\%$) and I/O area ($\sim 11\%$) of the total 1×1 mm^2 block.

Thermal cycling while carefully monitoring the integrity of BEOL around TSVs has shown 3-D does not compromise reliability of BEOL. The impact of TSV stress on MOS devices causes Vth shifts, to account for this during design further analysis and modeling is advised. Thermal hot spots in 3-D chip stacks cause temperature increases three times higher than in 2-D chips, we have proposed thermal floorplanning to take this into account during design. We have found no ESD events during 3-D processing, however careful further monitoring is required. The noise coupling between two tiers in a 3-D chip-stack is 20 dB lower than in a 2-D SoC, opening opportunities for increased mixed signal system performance. The impact on digital circuit performance of TSVs is accurately modeled with the proposed *RC* model and ring oscillators spanning both tiers in the stack show that digital signals can be driven through TSVs at high speed and low power. Experimental results of a 3-D Network-on-Chip implementation demonstrate that the NoC concept can be extended from 2-D to 3-D SoCs at low area (0.018 mm^2) and power (3%) overhead.

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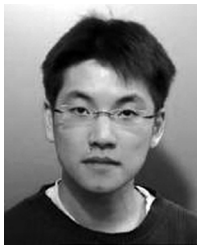

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Dr. Beyne is elected member of the board of governors of the IEEE CPMT society, president of the IMAPS-Benelux committee and member of the IMAPS-Europe Liaison committee.

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