Tutorial 02:

Implementing VHDL design on FPGA board (NEXYS2)

Software:

Xilinx ISE as a software package containing a graphical IDE, design entry tools, a simulator, a synthesizer (XST) and implementation tools.LAB Room-S111 and LAB Room-S241 already contain Xilinx ISE suit 11 but if you want to work on your own computers then a Limited version of Xilinx ISE (WebPack) can be downloaded for free from the Xilinx website.

Basically FPGA design process involves the same sequence of actions for every FPGA design software suite:

i.e.

- First to Create a project (choose a name for your project, an FPGA device (in this case NEXYS2 BOARD), a default language which is VHDL etc.)
- Add files to project (both HDL descriptions of the target device and testbenches for behavioral simulation).
- Do the Behavioral simulation to see if your logic is working (see the Tutorial01 for Behavioral simulation).
- Then you have to run Synthesis (an automatic process to translate HDL description to a netlist).
- Finally Implementation and bitstream generation (*.Bit file).

We will now discuss all above mentioned points step by step.

1.1 Creating a project

To create a project, start a Project Navigator and select File->New Project. You will be asked for project name and folder. Leave "top-level source type" as HDL.

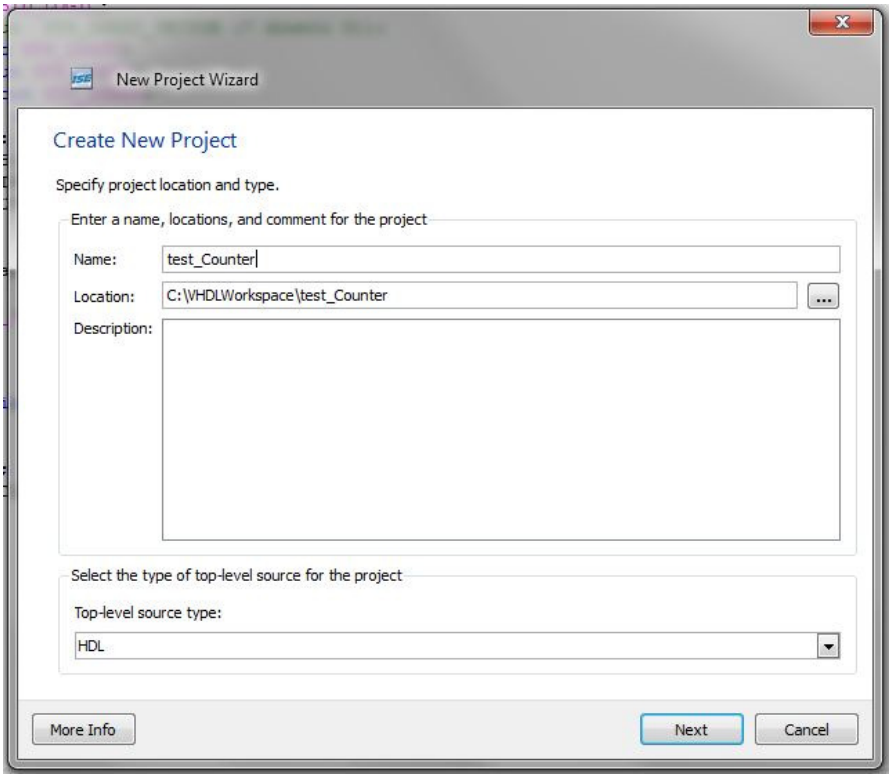

Fig1.1

Now choose a target device (use a Spartan-3E XC3S1200E device (which is Mounted on NEXYS2)) as well as set up some other options, as shown in the figure1.2 below.

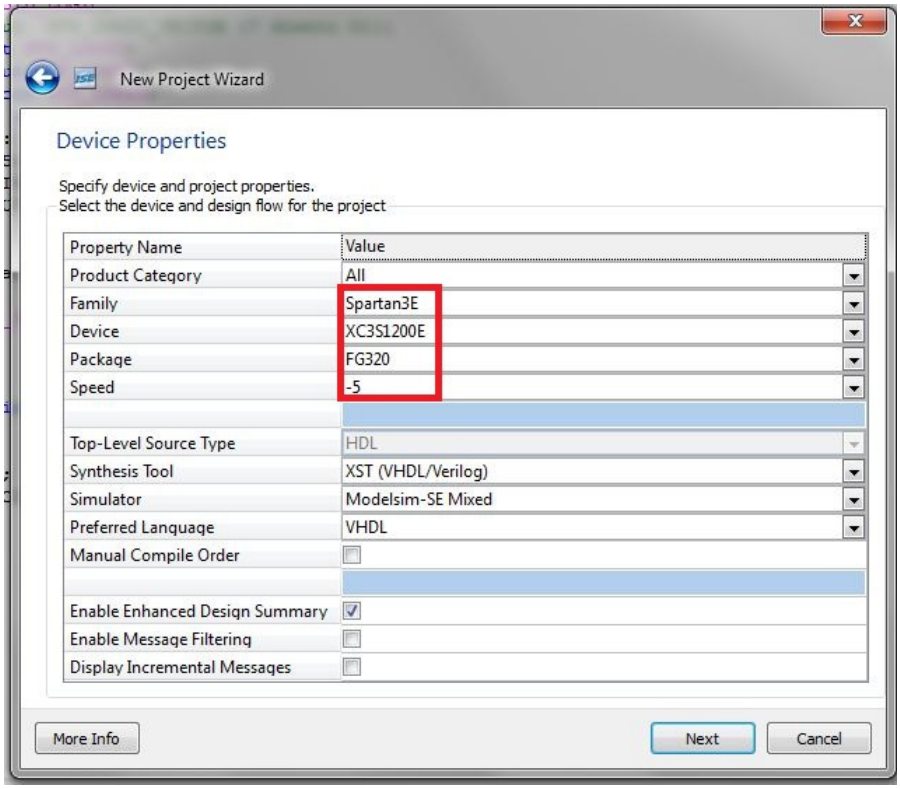

Fig1.2

By pressing ***Next*** to the menu will lead you to create a new VHDL source file as shown in figure 1.3

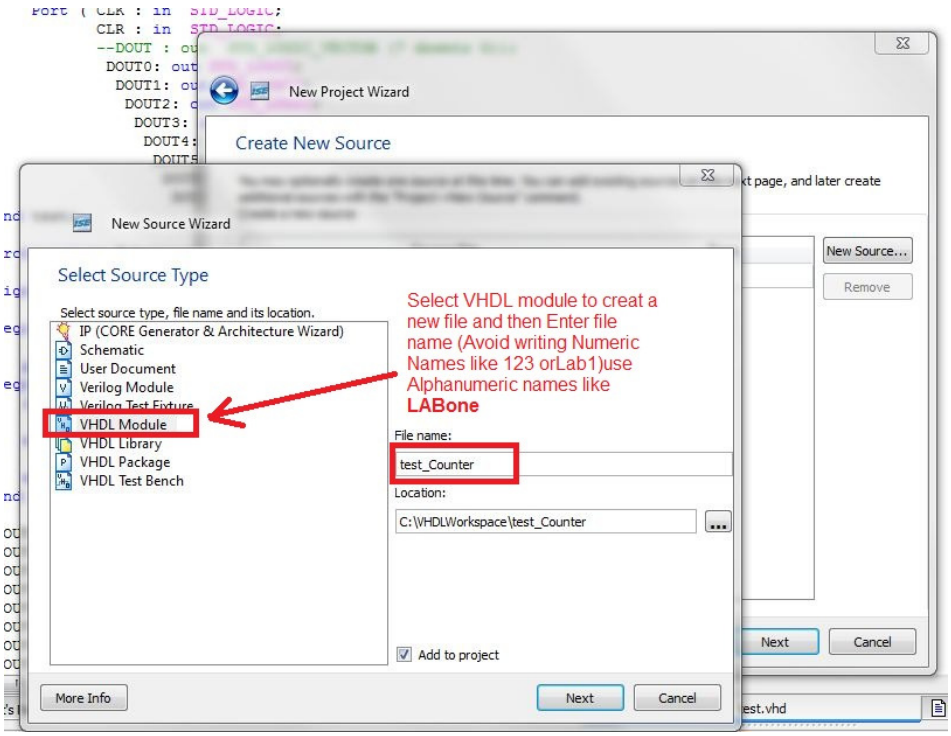

Fig 1.3

1.2 Define a Module:

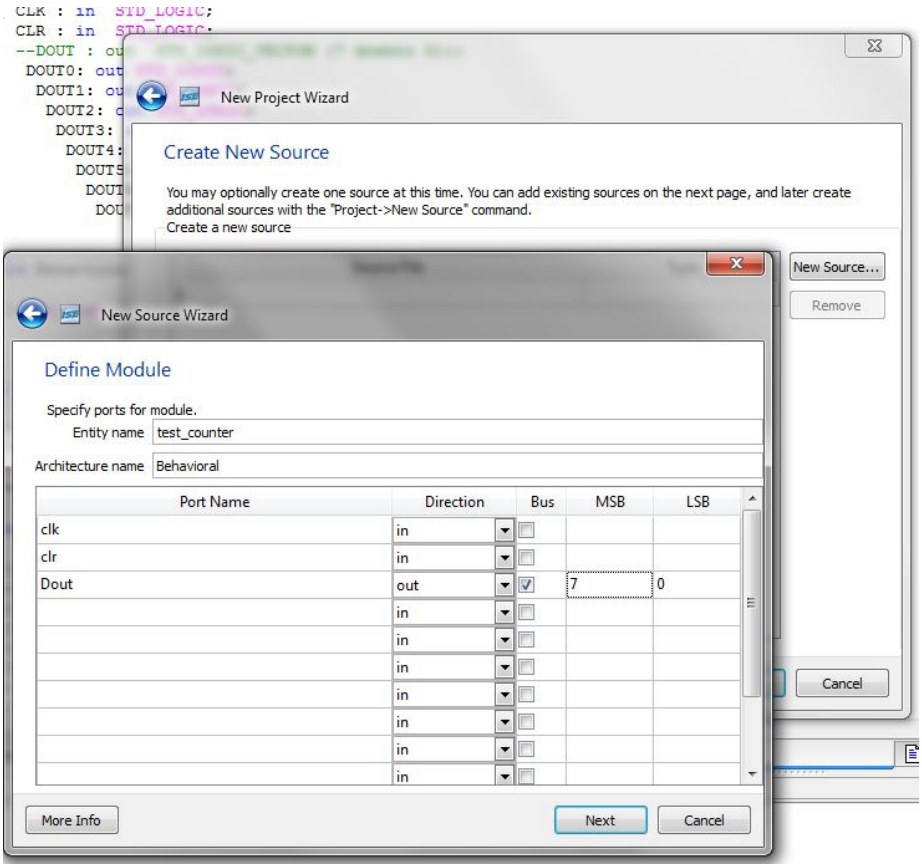

Fig 1.4

1.3 Simulation:

To check that your code works as intended you have to create a *testbench* where you relate all your inputs and outputs to some predefine signals.

Test Bench is written in VHDL, just like a Hardware Description, but the difference is that a testbench can only be use for simulation and is not synthesizable therefore it cannot be used in real Hardware. Testbench are always visible in "*Behavioral Simulation"* mode that can be selected from the combo box in the upper left part of the **Xilinx ISE project Navigator.** For further details check "Tutorial01".

1.4 Synthesis:

For implementing the design you should choose *"Implementation"* mode from the combo box in the upper left part of the **Xilinx ISE Project Navigator,** as shown in figure 1.5.

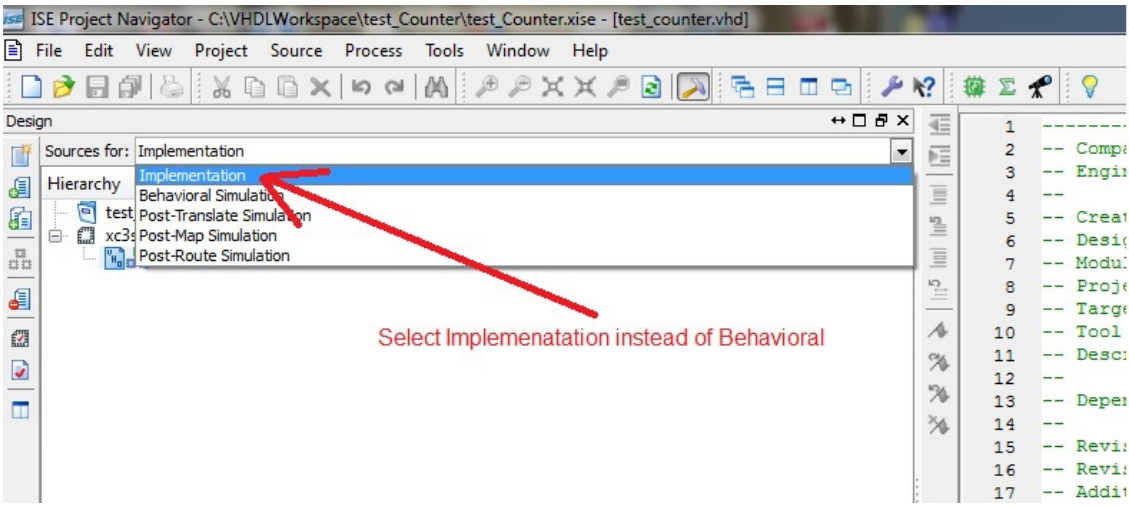

Fig1.6

Before Synthesizing if you have more than one VHDL source files in the project, then select your top design as ***Top Module***, as shown in the figure 1.7.

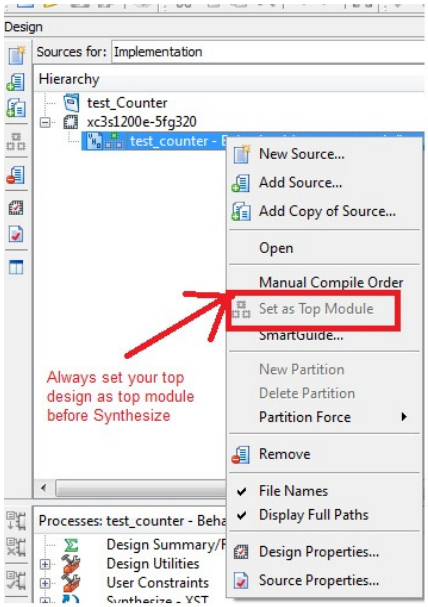

Fig 1.7

Go to the lower menu of the side bar you can see an option *"Synthesize-XST"*. Right click on it and press ***Run*** in order to synthesize your code (as shown in figure 1.8).

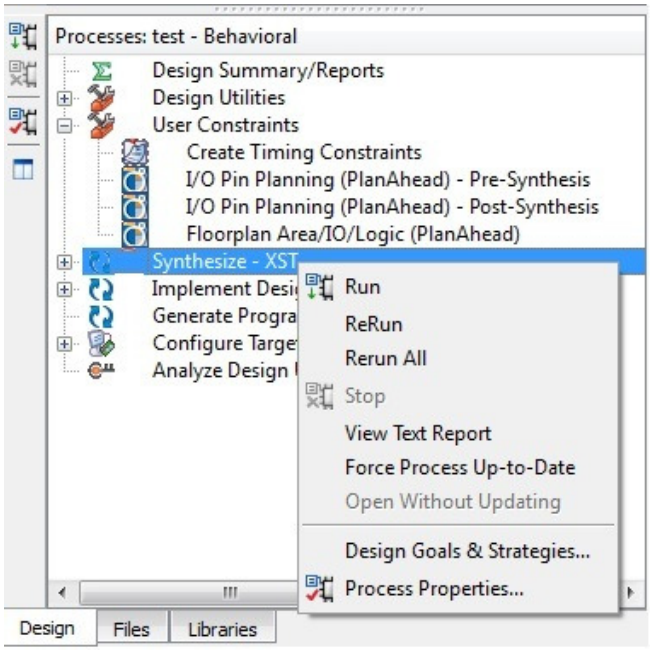

Fig1.8

If the code is correct, there shouldn't be any problems during the synthesis, see figure1.9.

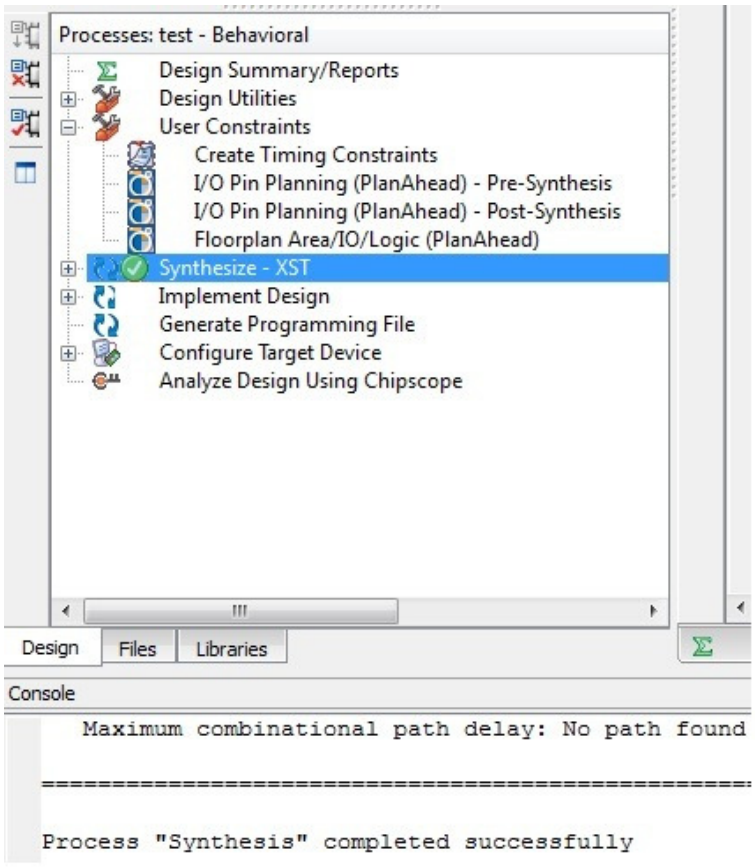

Fig1.9

1.5 Implementation Constraints for NEXYS2 (FPGA Board)

For Implementation of your design to FPGA, you need to add the UCF (User Constraints File) or to create a new UCF file in the project. The user constraints file includes pin assignment for the NEXYS2 (Spartan-3E) device. Figure 1.10 shows how to add the UCF file in your project.

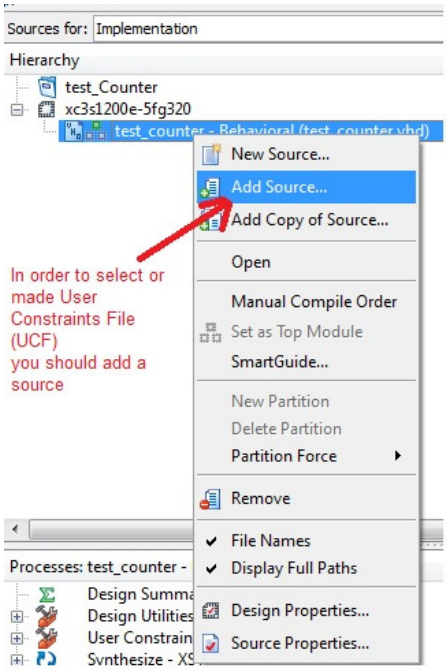

Fig 1.10

In order to add the source one should have the UCF file present in the system. To download that file for particular board (in our case it's NEXYS2) go to http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,789&Prod=NEXYS2 And download the file with a name *"Master UCF file for the Nexys2-1200"* to a folder. And follow the step mentioned in figure 1.10 and figure 1.11.

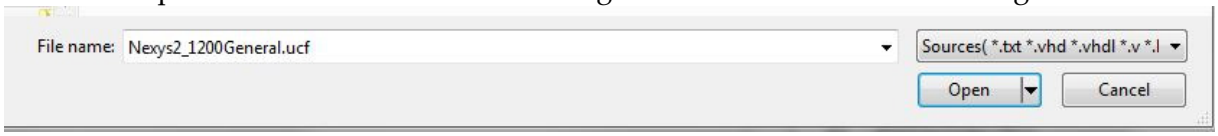

Fig 1.11

After adding the UCF file to your project you need to edit the file according to your project requirements. Figure 1.12 shows how to assign a corresponding pin to your Signal.

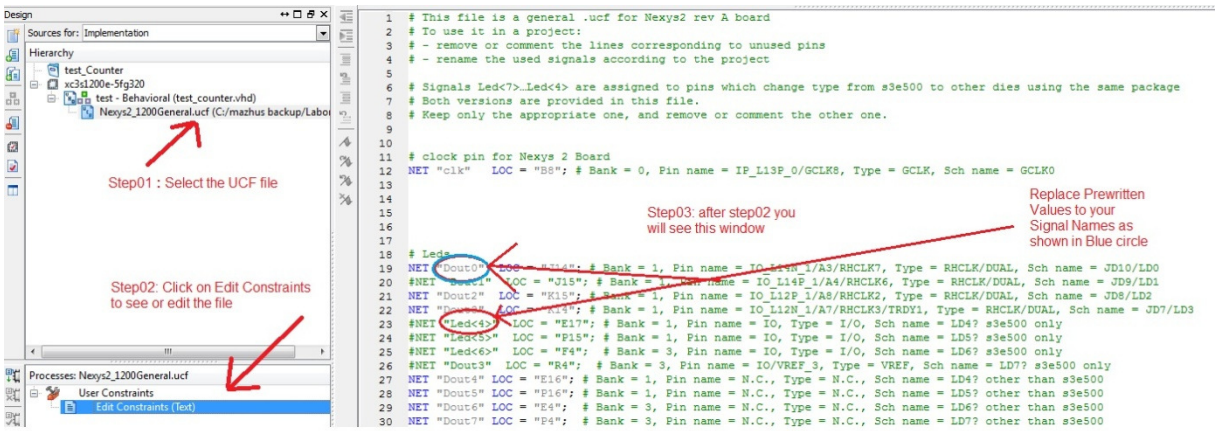

Fig 1.12

1.6 Generate the bit programming file:

After editing the UCF now your program is ready to take the last step which is *Generate Programming File*. Generate Programming File process is to produce a bitstream (.BIT) file for Xilinx device configuration (Shown in figure 1.13).

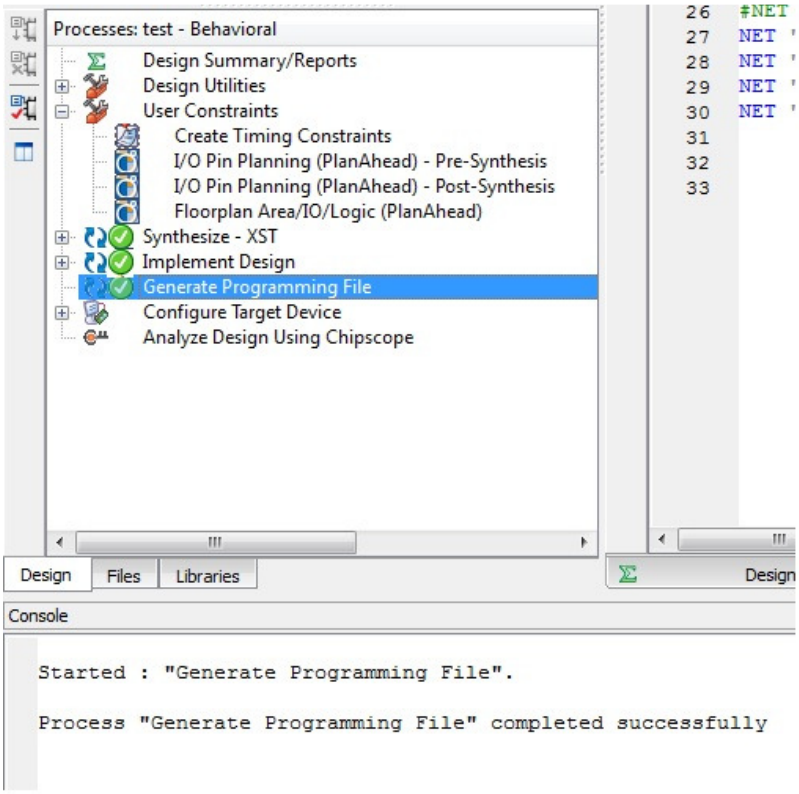

Fig1.13

The (*.BIT) files set switches in a programmable Xilinx FPGA chip to implement the synthesized circuit (Establish gates and connect them) plus device specific information. The binary data in the BIT file can then be downloaded into the FPGA's memory cells.

1.7 Downloading (*.BIT) file to FPGA board (i.e. NEXYS2):

Finally it's time to download the code to FPGA board, in our case its NEXYS2 board equipped with Spartan-3E FPGA (Figure 1.14)

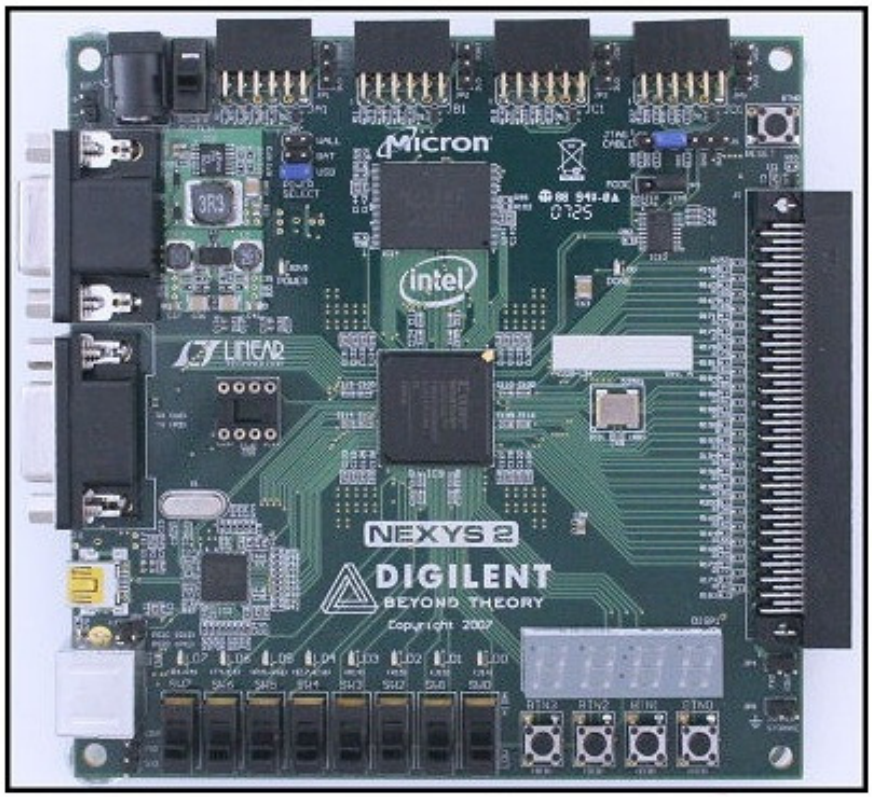

Fig 1.14

- Connect your NEXYS2 Board with Computer via USB cable and load the software from Startmenu>>Programs>> Digilent>>Adept(see figure 1.15)

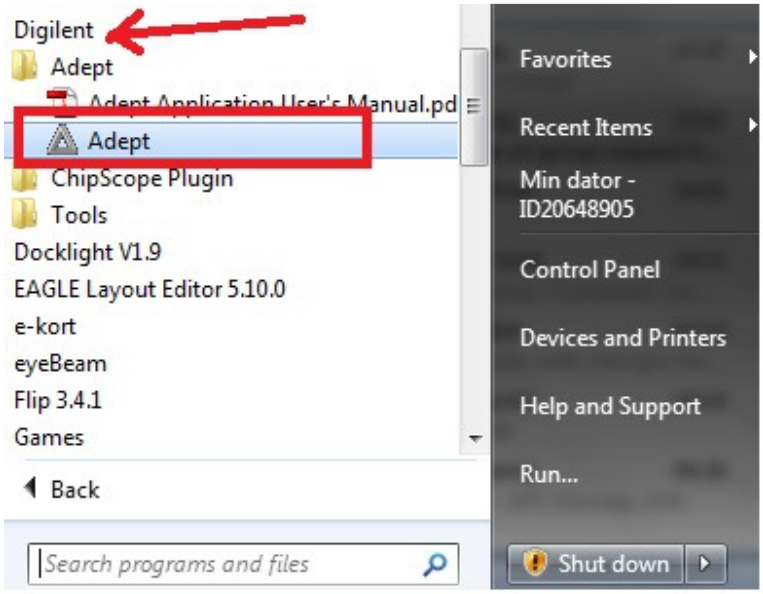

Fig 1.15

- Select the *.*BIT* file from your Project Folder and Click on Program as shown in figure 1.16 and figure 1.17.

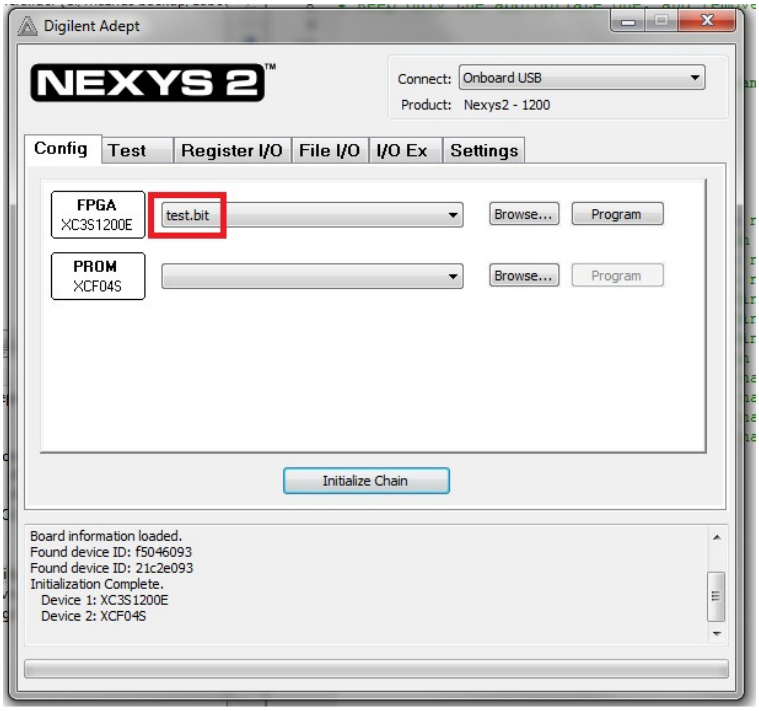

Fig1.16

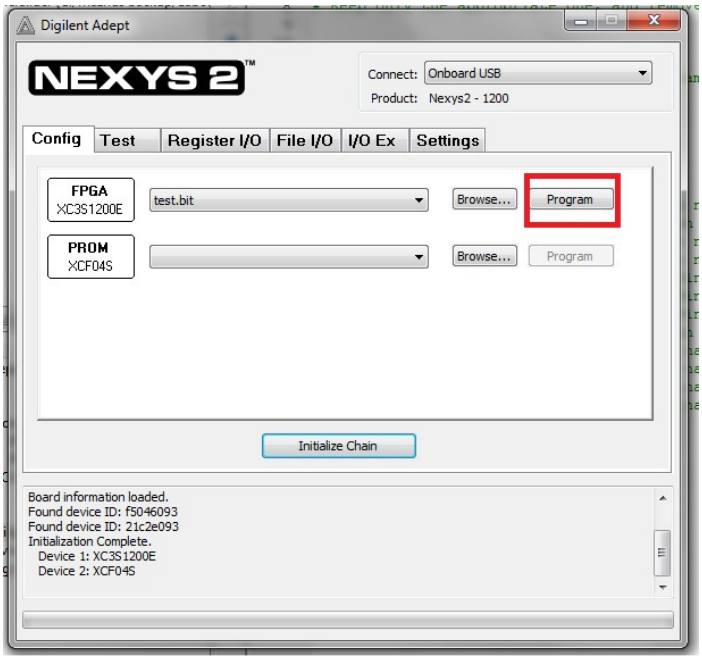

Fig1.17

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