Nexys 2 board tutorial - Counter (Verilog Version)

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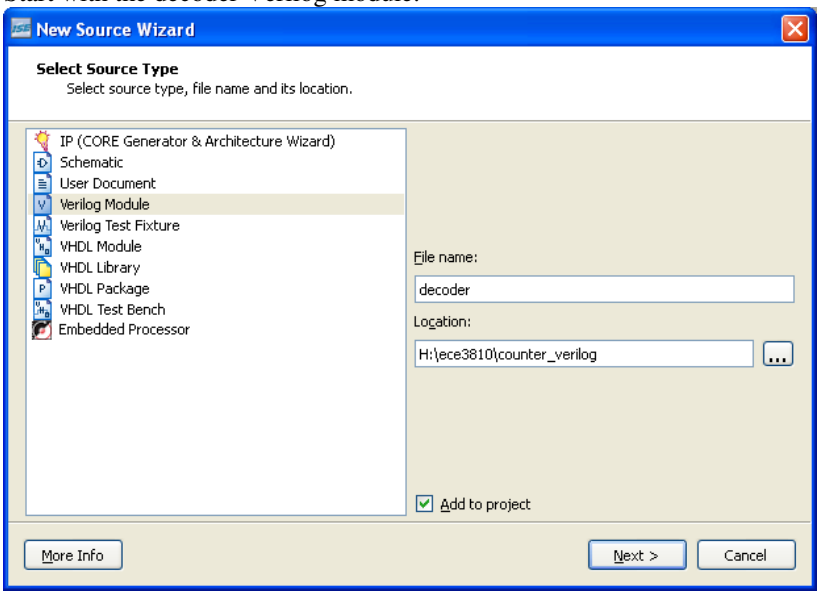
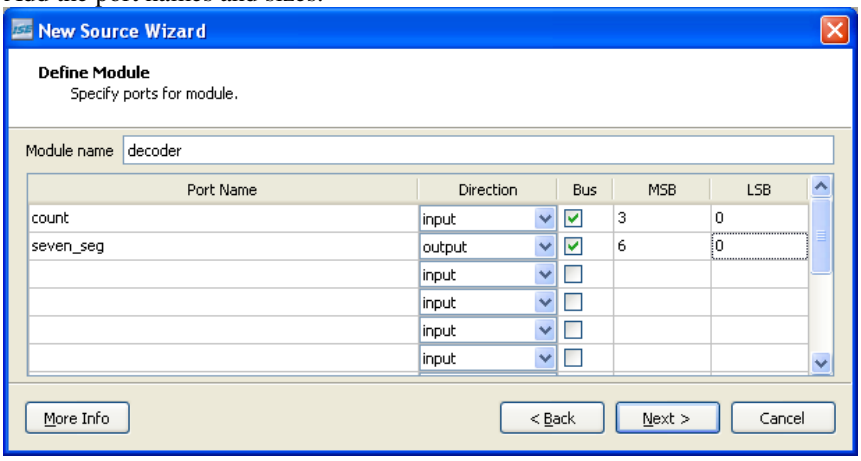
This design shows how to create a simple sequential circuit (a counter) with Verilog HDL.
It also demonstrates hierarchical design by using a separate decoder component that converts a binary count value to a seven segment display.

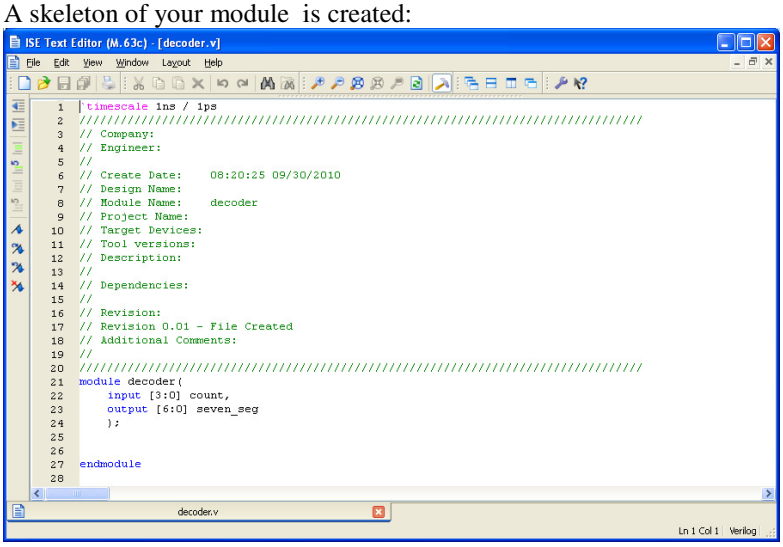
Start with the decoder Verilog module:



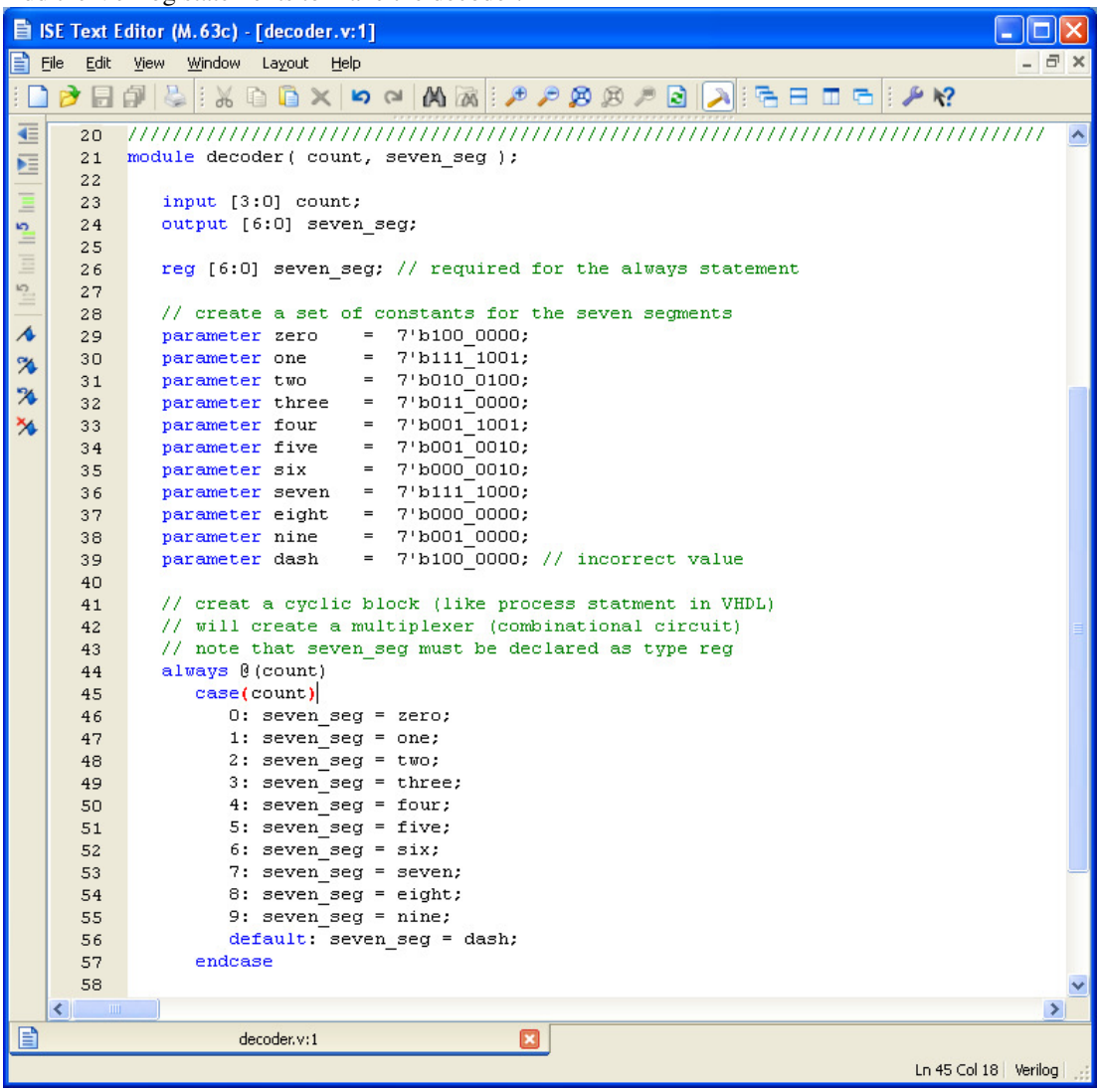
Add the port names and sizes:



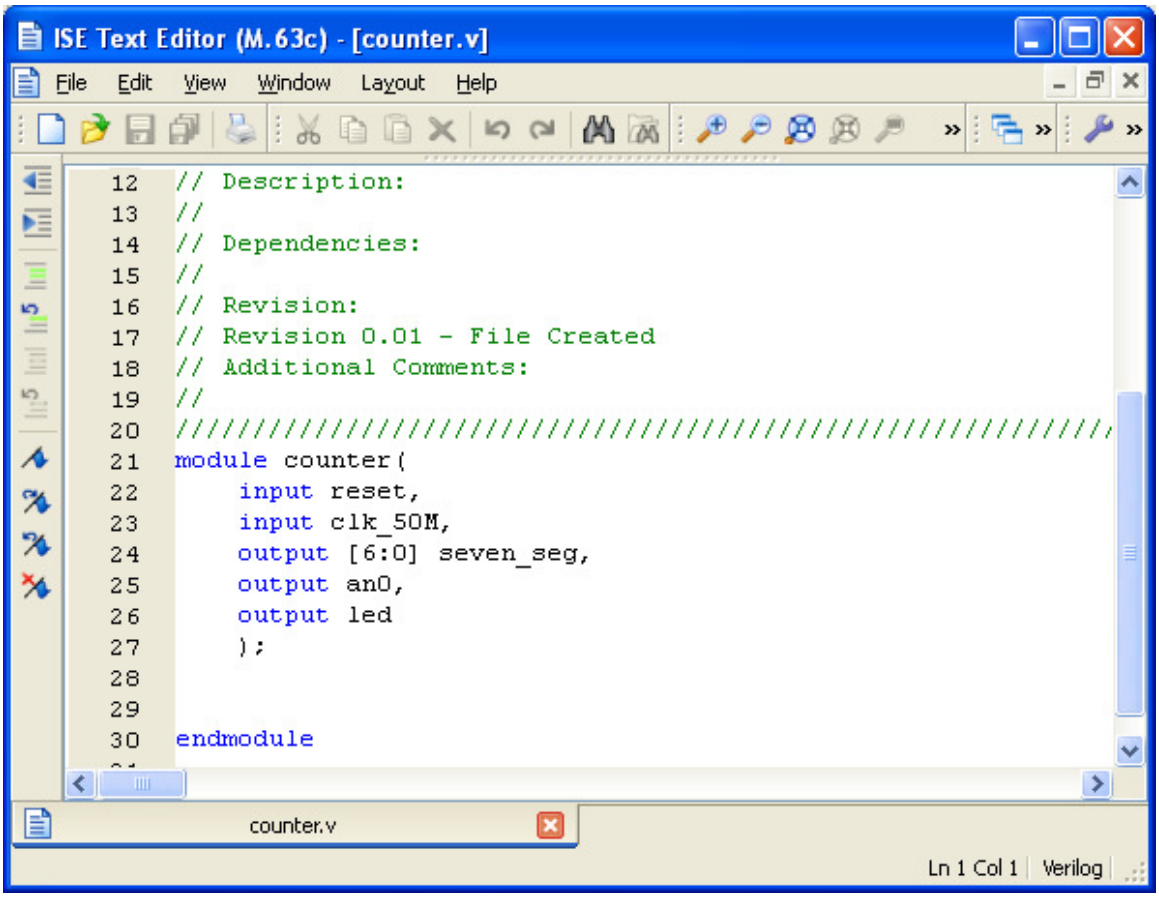
A skeleton of your module is created:



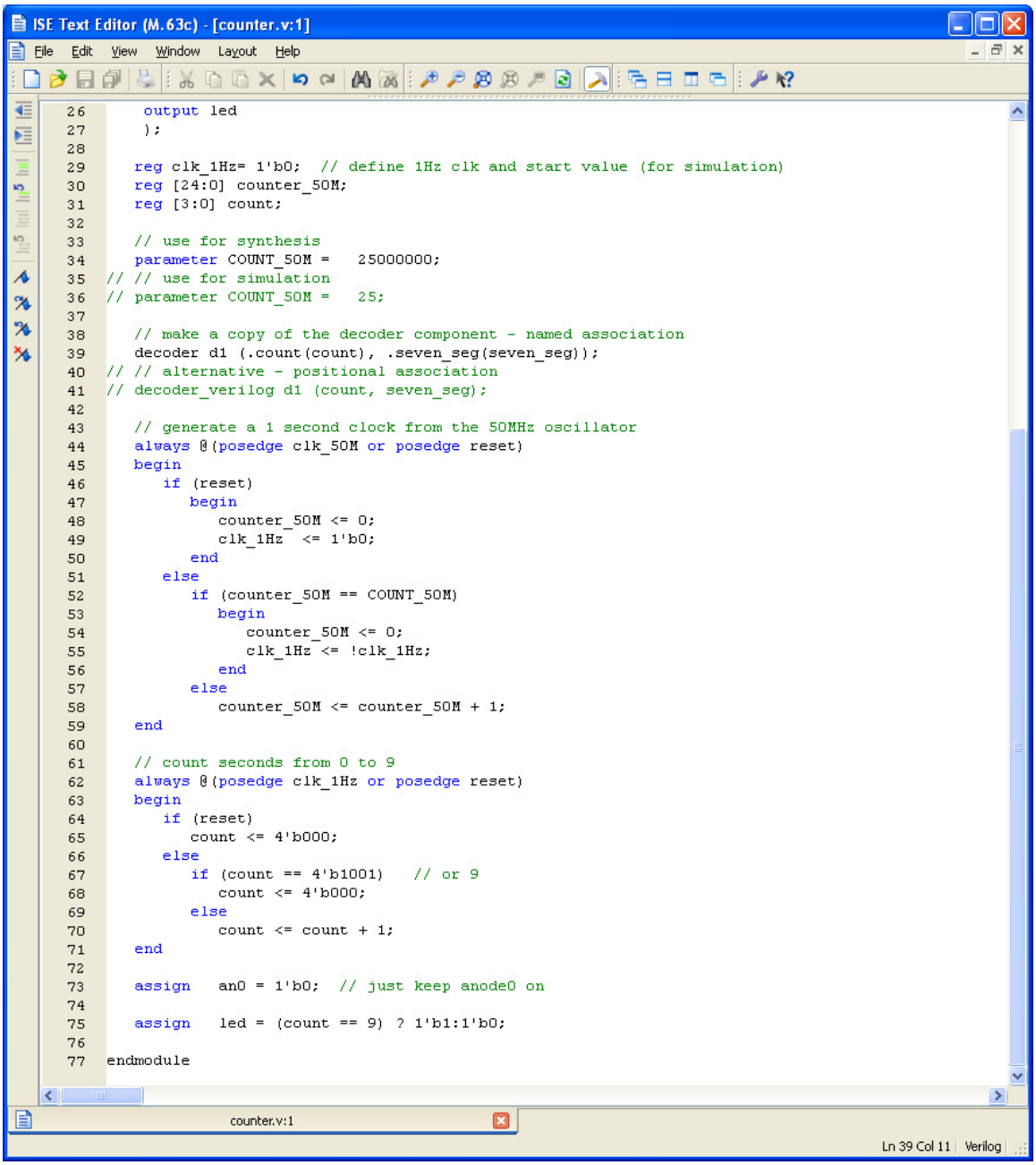
Add the Verilog statements to make the decoder:



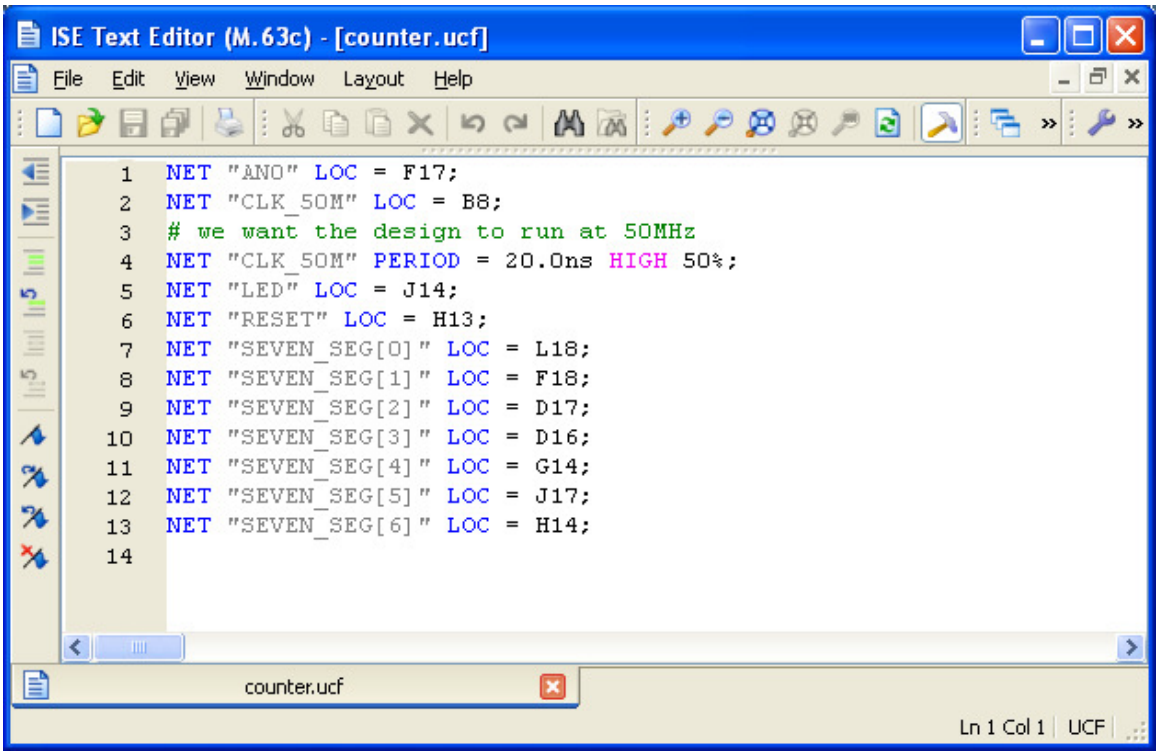
Now create the top level Counter module:



And add the behavioral statements:

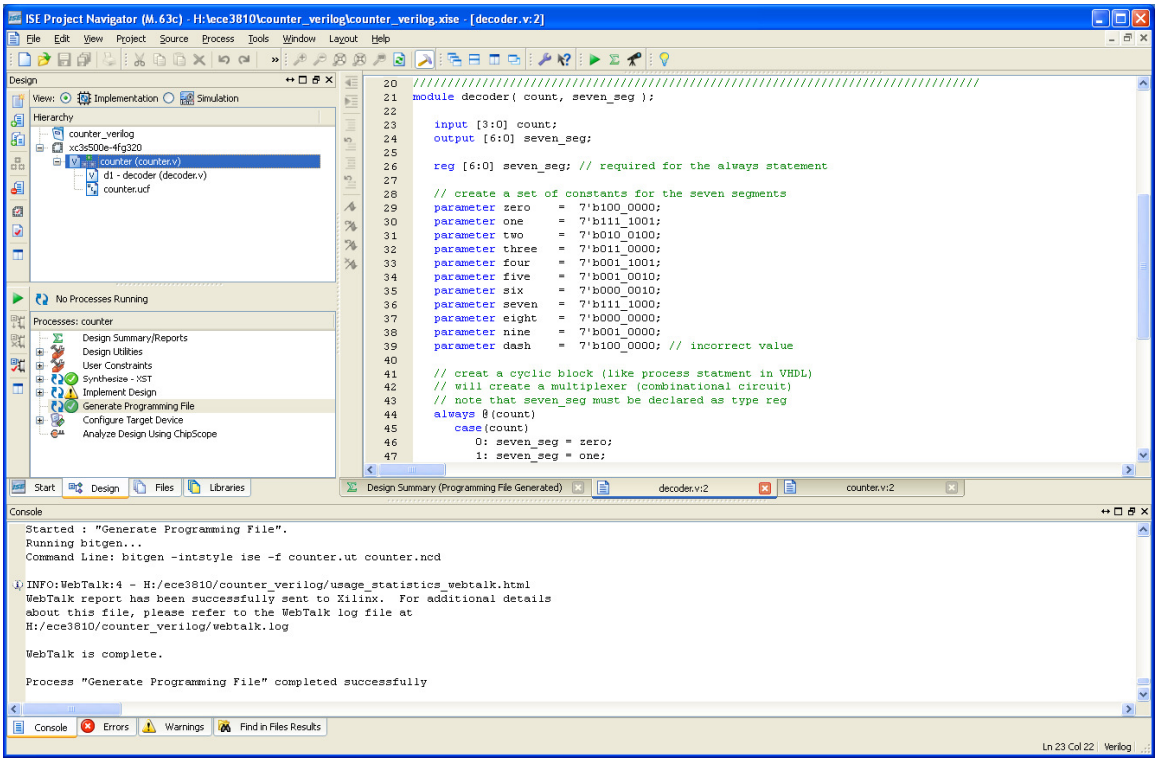


And finally create the UCF file:

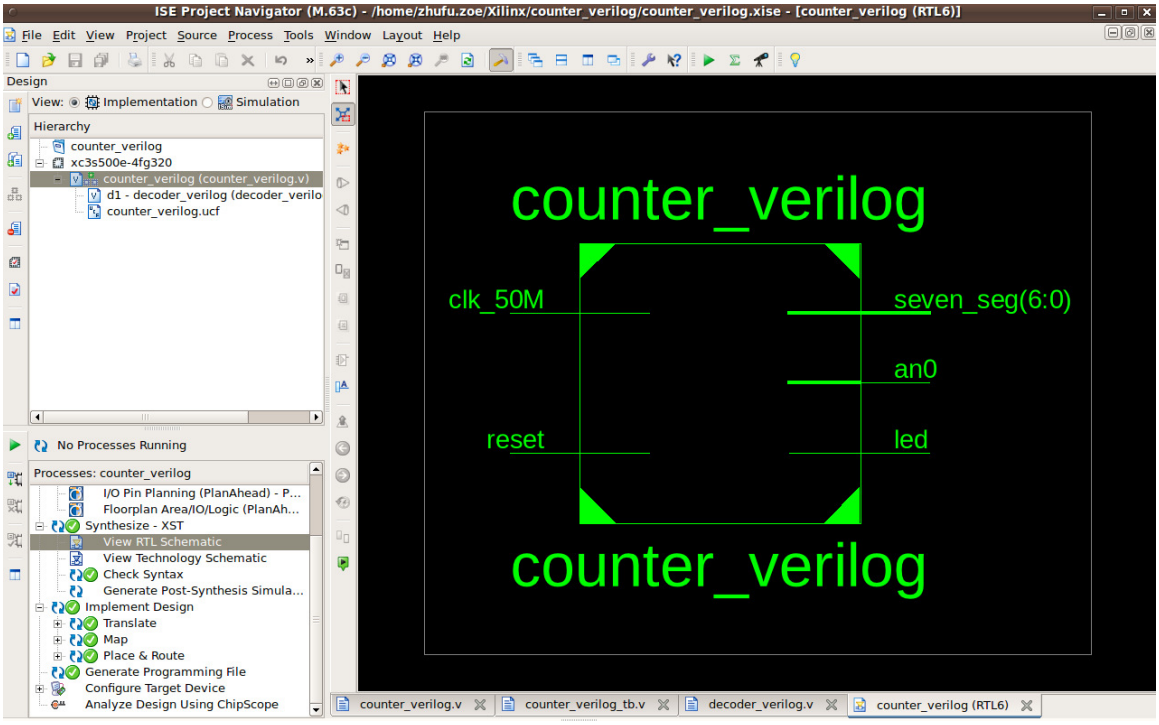


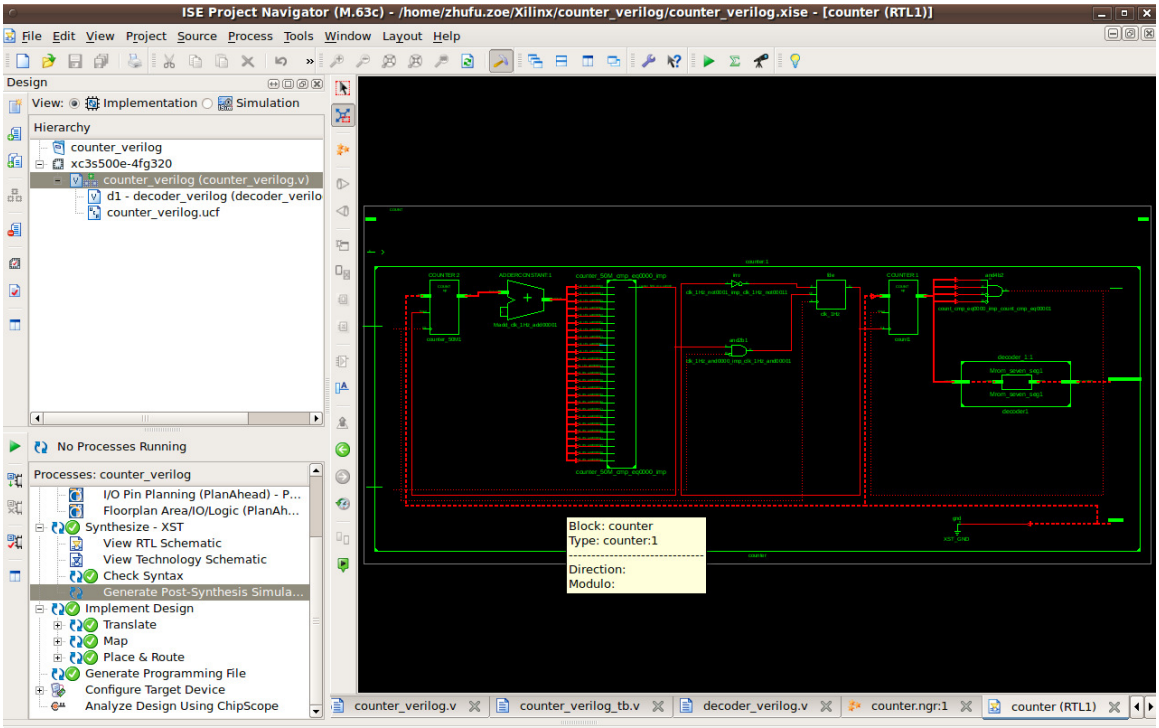
Note: we have added a timing constraint to help guide the synthesis tool

We can now synthesize and implement the design:



Synthesized Results:

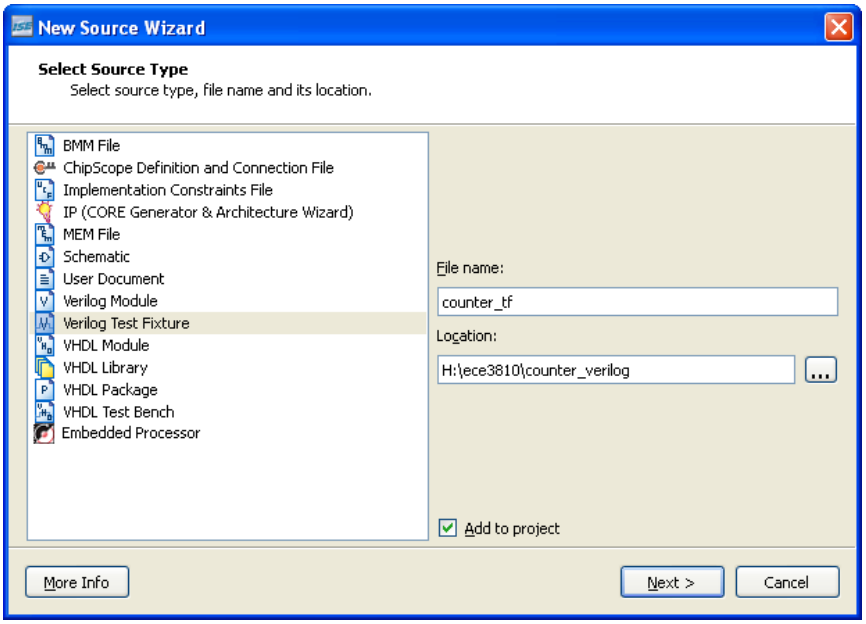




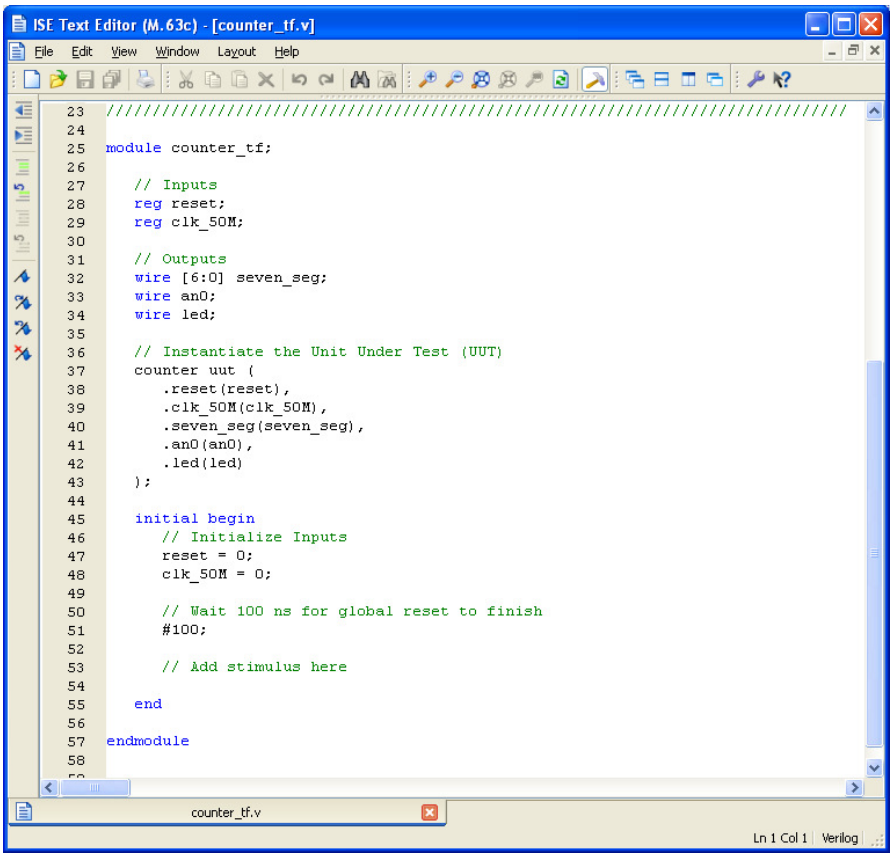
Download the design to the board and test the operation.

We can also create a Test Fixture (test bench to test and simulate the operation).

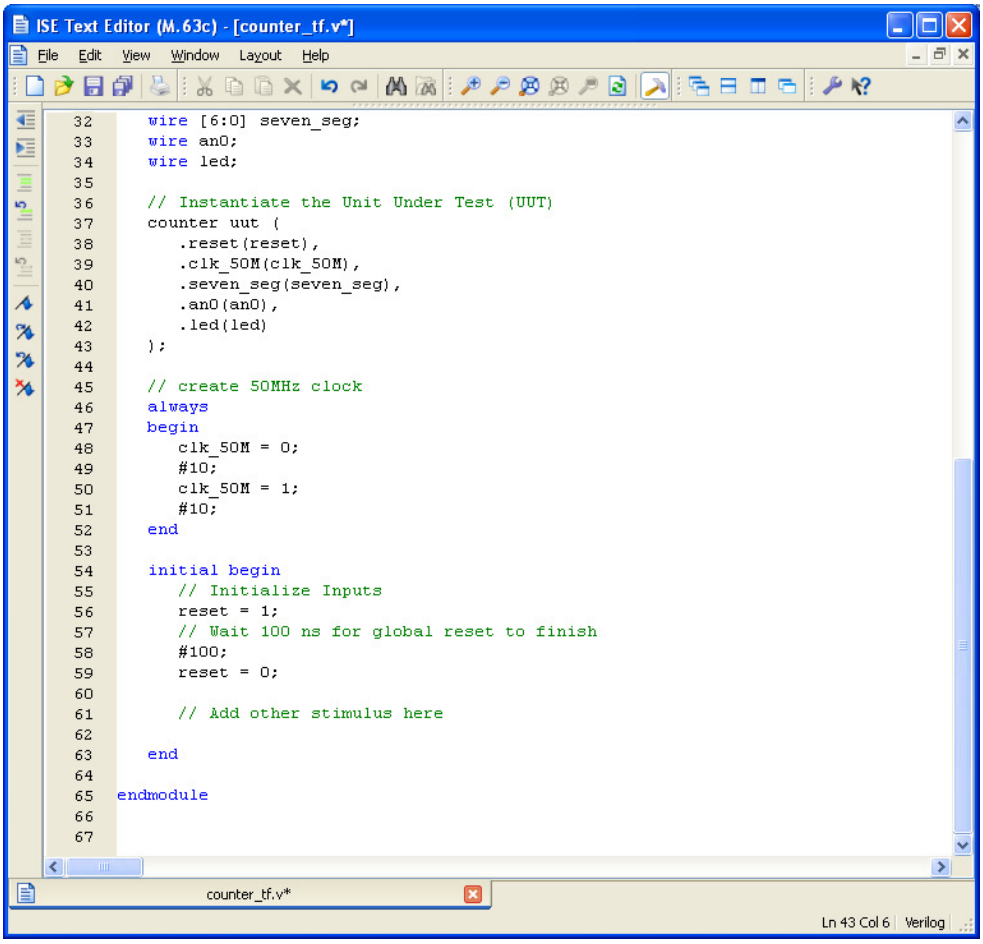
Create a Test Fixture module:



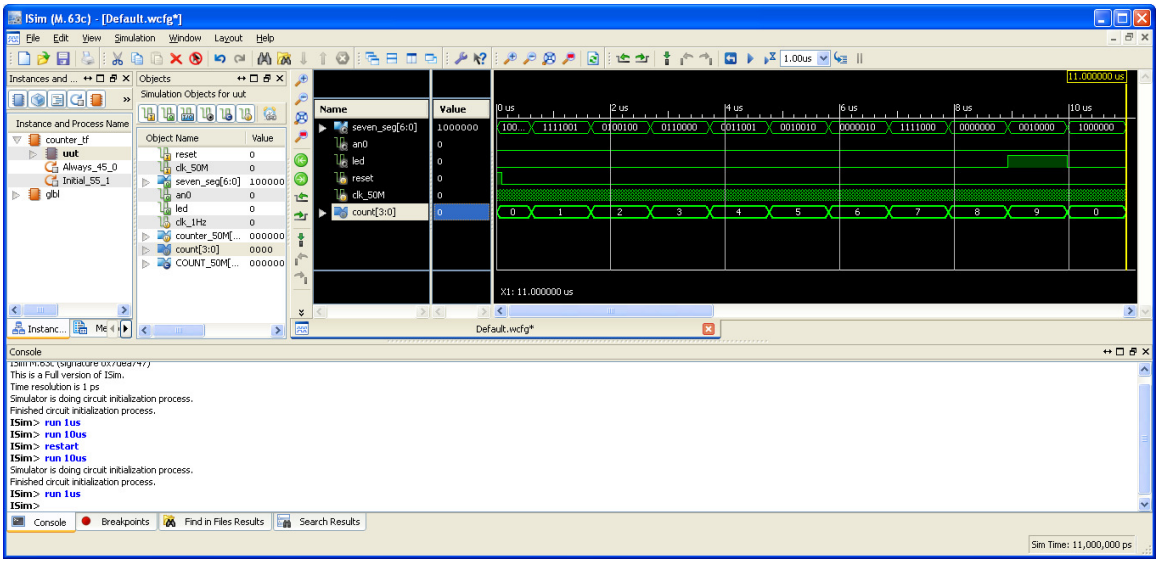
A skeleton of a test fixture to test your counter is produced:



Modify it so it creates a 50MHz clock, and provides the reset signal for 100ns:



Run the simulation (also add the count internal signal) and verify operation.
Note: don't forget to change the PARAMETER COUNT_50M to speed up the simulation



Zoomed in for more detail: