Cadence Transistor Characterization Tutorial

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Unix account and Cadence Setup Instructions

1. Set up a Unix account by visiting the following website.

https://unix.engr.sjsu.edu/wiki/doku.php

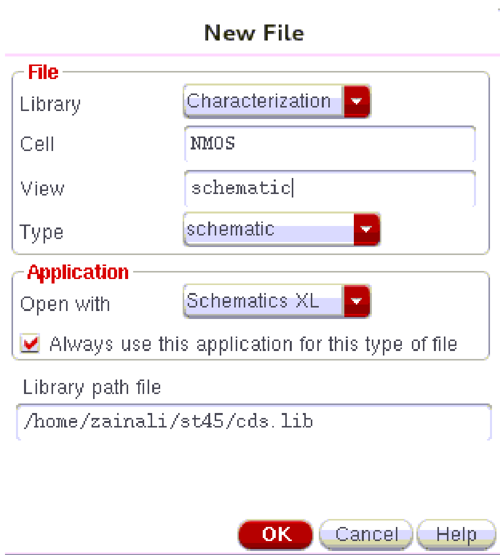
2. Complete the Cadence Tutorial. This will setup cadence on your account and provide you with a general idea on how to use cadence. **Type "csh" in linux terminal to switch to your directory**.

http://www.engr.sjsu.edu/mjones/cadence6.pdf

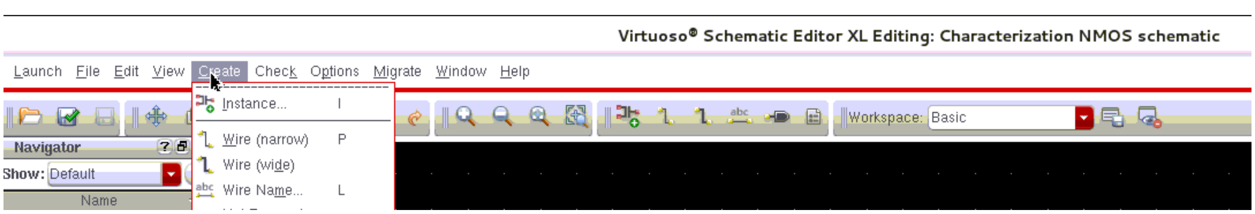
Transistor Characterization - NMOS

The tutorial is adopted from Prof. Murmann's note. You can download them by following this LINK. You can also use EE315 Notes as reference.

1. In the main virtuoso window, click on File-->New-->Library. Name it "characterization" and under "Technology File" select Reference existing technology libraries. Click ok and then select gpdk045 as a reference library.
2. Select File-->New--Cellview. Select the characterization library, name it NMOS and open it with Schematics XL. Hit ok.



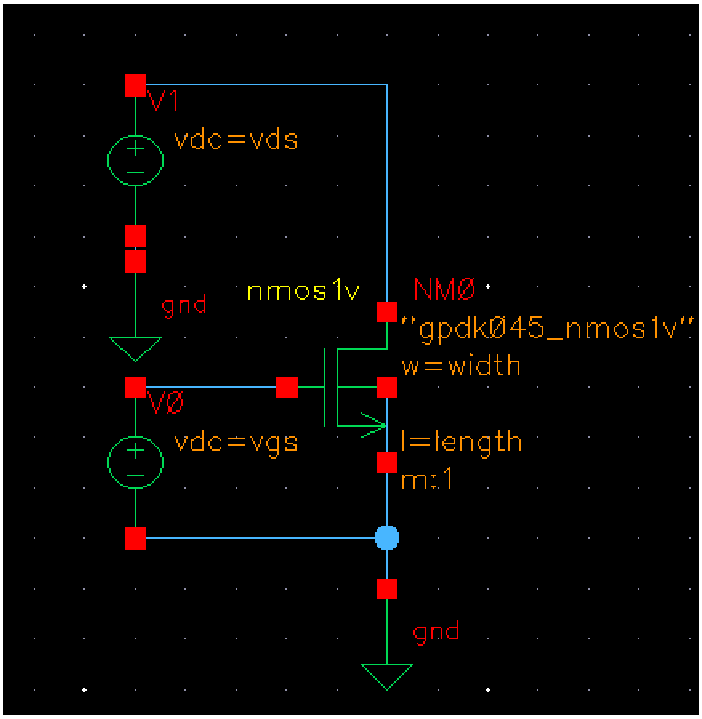
3. Click on Create and then select Instance (alternatively use "I" or shortcut on the toolbar).



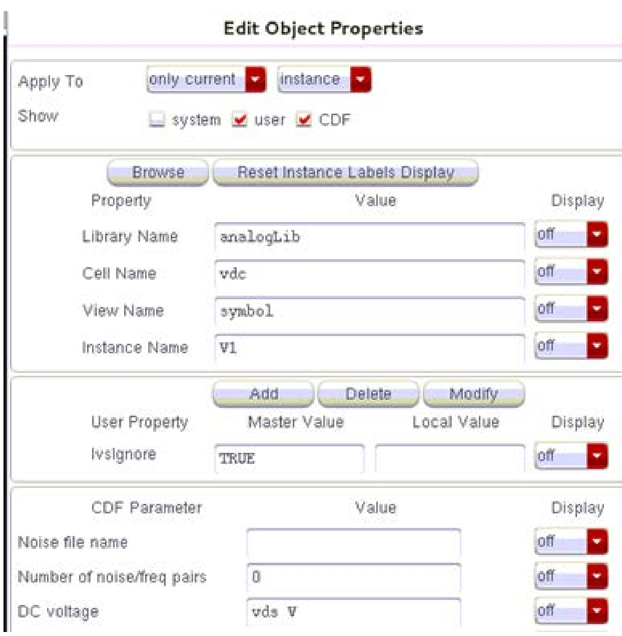
You will need the following parts.

analogLib-->vdc (used as a DC source) //// analogLib-->gnd ////gpdk045--->nmos1v

4. Set up the following test bench for NMOS transistor characterization.



5. Set the voltage for V1 as vds and V0 as vgs. (You can access this click right clicking on the object and selecting properties or selecting an object and pressing "Q" key or by in property editor window in ADE XL.

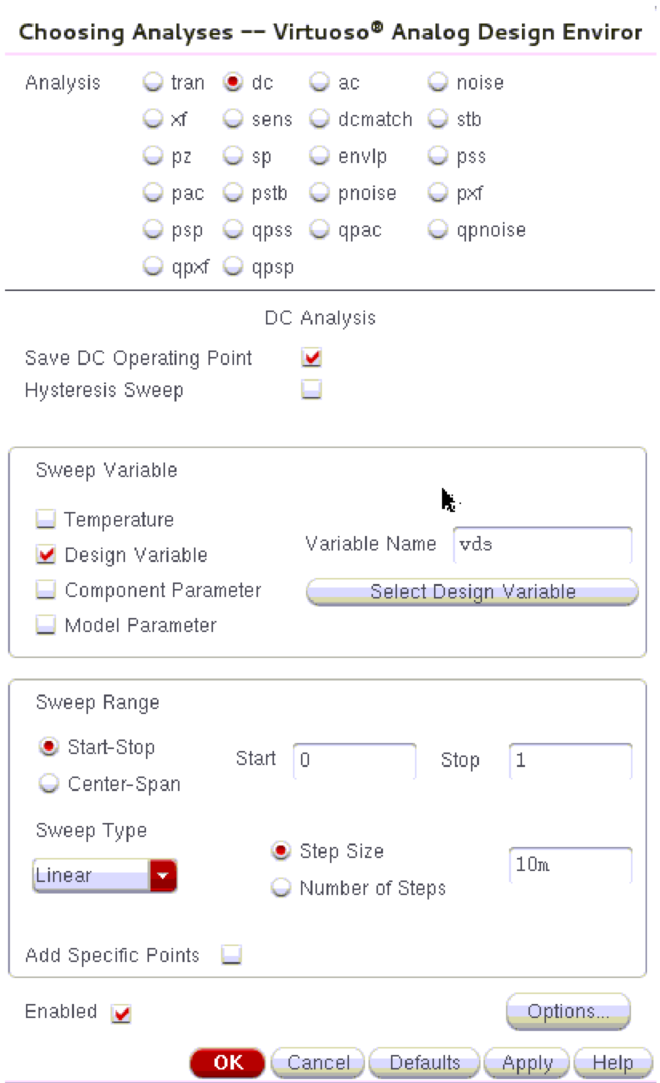


6. For the NMOS transistor, set length as length, width as width and fingers as fing.

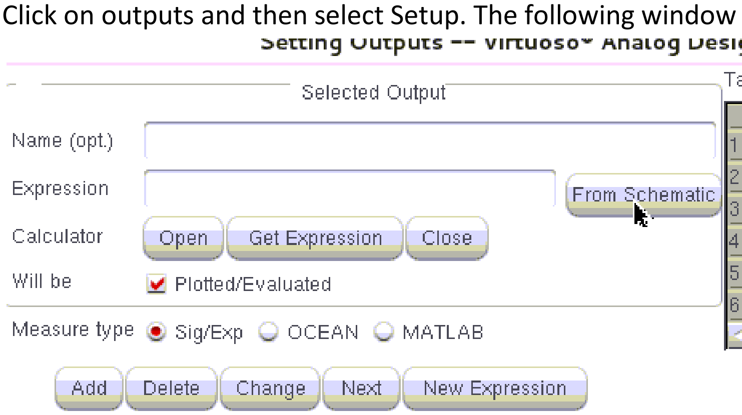
7. Hit F8 or click on  in the toolbars menu. This will check your design for errors and save it.

   Your basic schematic is complete. Now Analog Design Environment will be used to set up various test benches for characterization.

8. Click on launch, select "ADE XL" , select "Create New View" and hit ok.
9. From the Menu Bar, Select "Create" and then select "Test". This will open the ADE XL Test Editor window.
10. Select "Analyses" and then choose under Analysis section select "dc". Check the "save DC Operation point box" and Click Ok. Mirror the following image for a vds sweep.

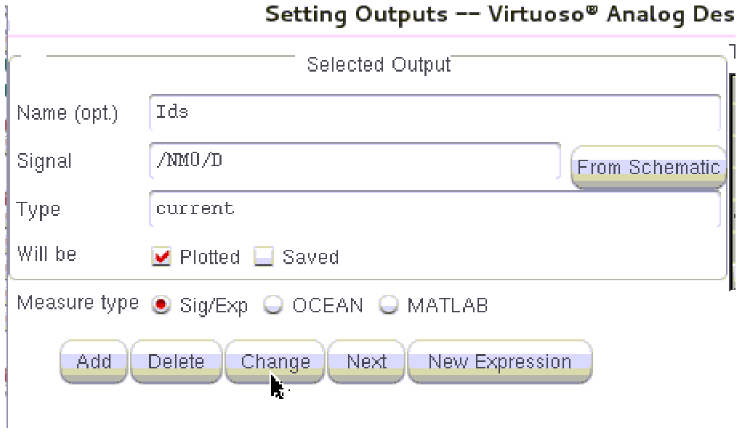


11. Click on outputs and then select Setup. The following window will open.

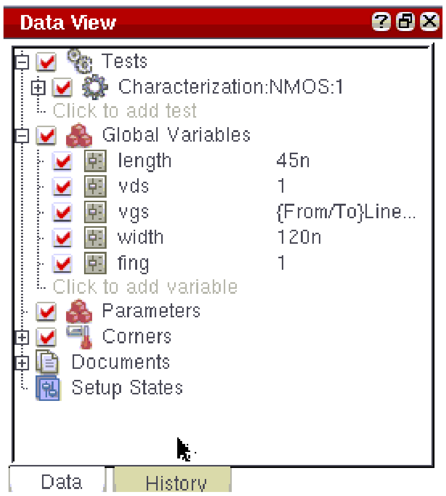


12. Select From Schematic and Click on the drain of the NMOS transistor. If you select a wire, it will plot the voltage. You need to select the node so that current is plotted. Name the signal Ids and

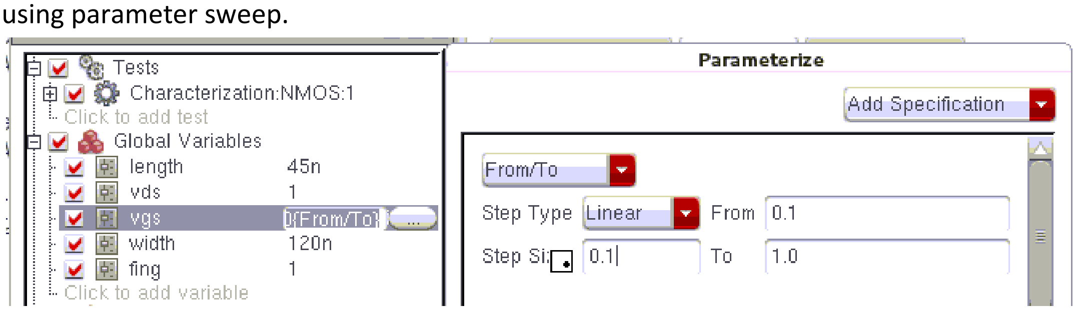
click on Change to update the output.

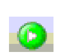


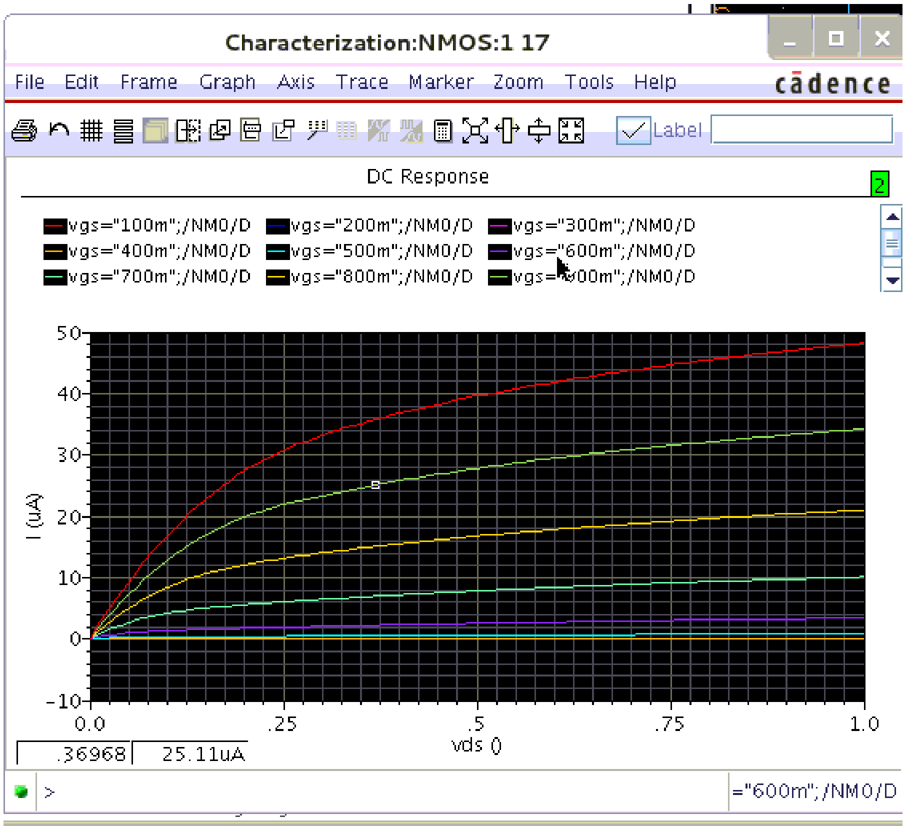
13. Under the data view section, set length to 45n, width to 120n, vds to 1 and fing to 1.



Vgs will be swept from 0.1-1V in 0.1V increments. Just click on the Vgs value tab and set it up using parameter sweep.

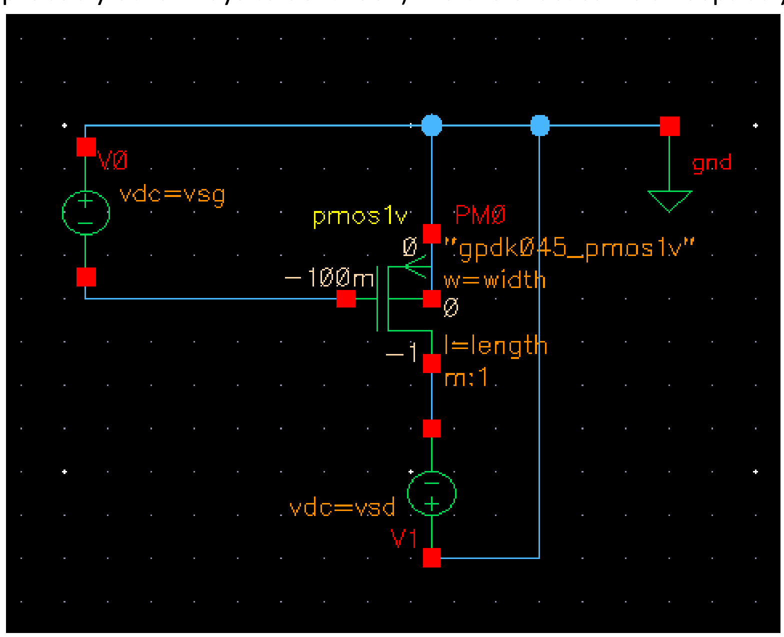


Under Run , select "Single Run, Sweeps and Corners" or hit the  on the main toolbar. You should get the following plot.



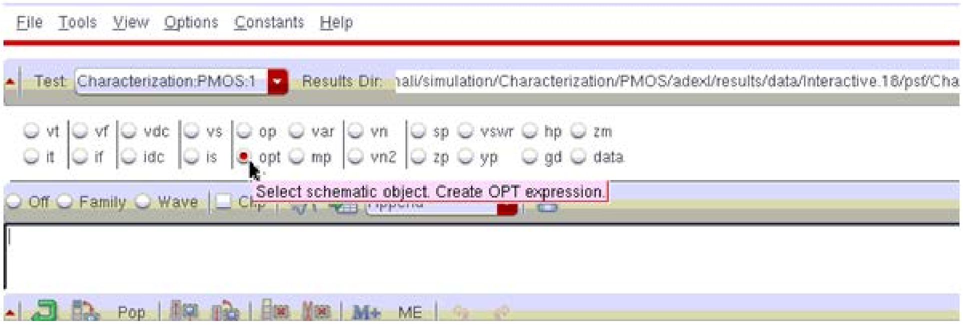
Rerun the simulation by setting the width to 10u. Increase the W/L will increase the amount of current flowing through the transistor.

14. Rerun the same simulation for a pmos1V transistor. Use the following testbench (there are probably other ways to do it too.). Do the exact same sweeps as you did for the NMOS part.

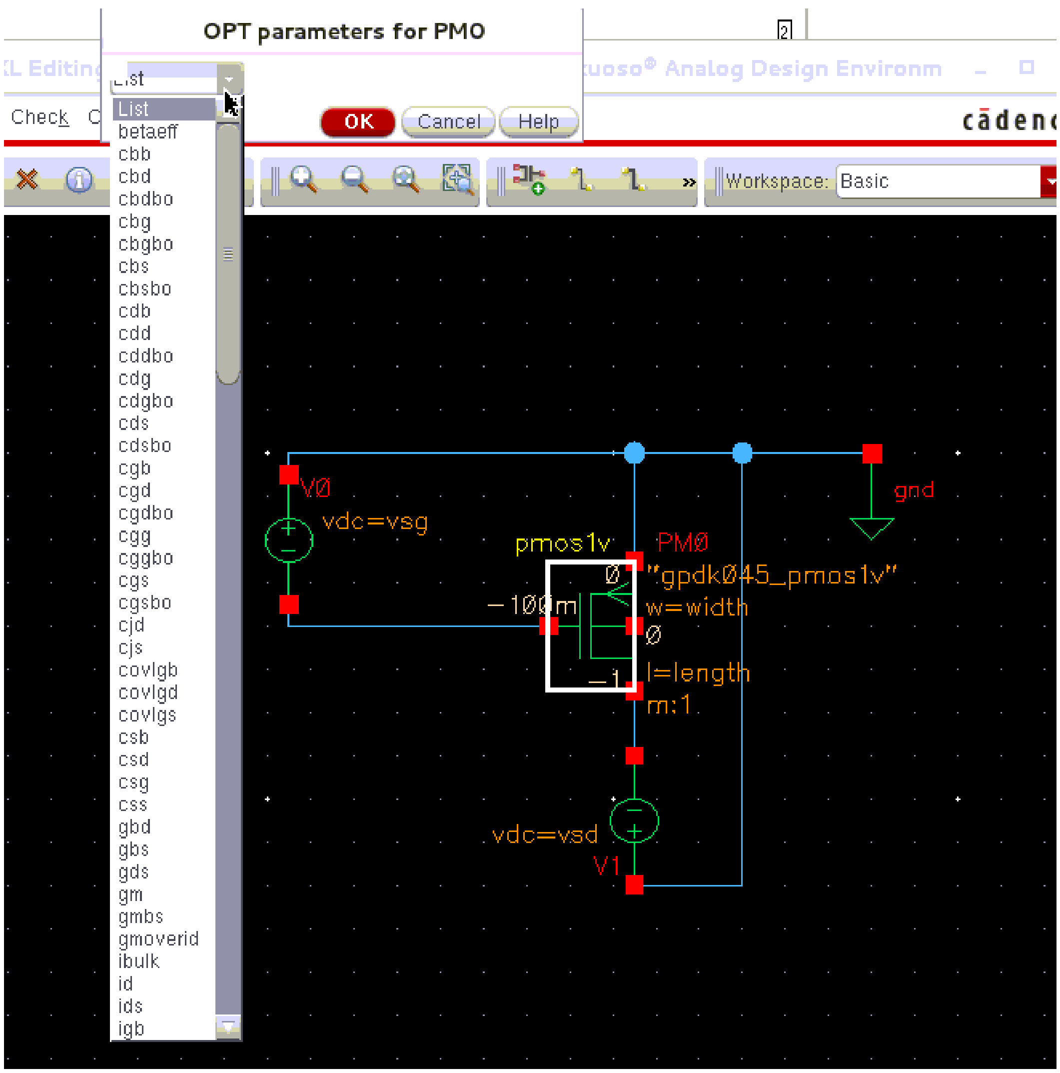


Calculator and gm/Id

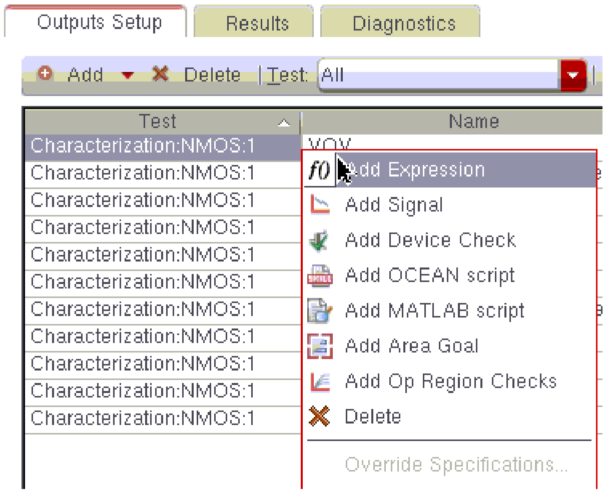
1. In ADE XL , select tools and then calculator. The calculator window will open. Click on opt.



2. This will take you back to your schematic. Select your transistor and it will open a drop down menu.



3. Select gm. It will print an expression ****OPT ("/PM0","gm")**** in the calculator window. In ADE XL window, right click under Outputs Setup and select Add Expression. A new blank expression will be there.



4. Copy and paste the calculator expression under Expression/Signals/File Menu. Under name put gm.

You can plot a variety of different transistor characterization values using the calculator tool. Some of the useful ones are listed below. (Don't forget the name of the transistor)

"(OPT("/NM0" "vgs") - OPT("/NM0" "vth"))" ------------**VOV (Overdrive Voltage)**
"OPT("/NM0" "gmoverid")" ----------------**gmoverid (Transconductor Efficiency)**
"((1 / 6.28) * (OPT("/NM0" "gm") / OPT("/NM0" "cggbo")))" ------------**fT (Transit Frequency)**
"(OPT("/NM0" "gm") / OPT("/NM0" "gds"))" -------- **"gm/gds (gm*rds...Intrinsic Gain)"**
"(OPT("/NM0" "gmoverid") * ((1 / 6.28) * (OPT("/NM0" "gm") / OPT("/NM0" "cggbo"))))" ---------
"gmoverid * ft **("Optimum Point (Murmann))"**

5. Figures of Merit from from Murmann's EE214 Notes. (You already plotted them above. Just listed below for reference.)

gm/Id will provide the highest gain and frequency possible while using the lowest power.

gm/Cgg will provide with the transit frequency for a transistor. As we increase length the transit frequency goes down. Need to minimize the length for highest transit frequency.

gm*rds (gm/go) will provide the highest intrinsic gain. go is equal to λ*Ids. rds id equal to 1/ (λ*Ids). So we need to minimize the Ids to get higher gain.

Figures of Merit for Device Characterization

Square Law

- Transconductance efficiency
  - Want large g_m, for as little current as possible

$$\boxed{\frac{g_m}{I_D}} \quad = \frac{2}{V_{OV}}$$

- Transit frequency
  - Want large g_m, without large C_{gg}

$$\boxed{\frac{g_m}{C_{gg}}} \quad \cong \frac{3}{2}\frac{\mu V_{OV}}{L^2}$$

- Intrinsic gain
  - Want large g_m, but no g_o

$$\boxed{\frac{g_m}{g_o}} \quad \cong \frac{2}{\lambda V_{OV}}$$

B. Murmann EE214 Winter 2010-11 – Chapter 3 16

6. Plot the following (do parameter sweep if you have trouble changing axes). You can also save the dc operating points by following these instructions. You can also export data and plot everything in Matlab/excel. (Note : This is short channel design. Look up Murmann notes for more information)

gm/Id vs Vov
ft vs Vov
gm/Id*ft vs Vov
gm/gds vs Vov
2/(gm/Id) vs Vov (provide estimated Vdsat vs Vov)
ft vs. gm/Id
gm/gds vs gm/Id
Id/W vs gm/Id

7. Repeat procedure for PMOS transistor.