An Introduction to

Mixed-Signal IC Test and Measurement

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Preface

Integrated circuits incorporating both digital and analog functions have become increasingly prevalent in the semiconductor industry. Complex digital circuits are now commonly combined with analog circuits as part of the continuing drive toward higher levels of electronic system integration. For example, complex microprocessors are frequently combined with high-performance analog and mixed-signal circuits to form so-called "system-on-a-chip" devices. An example of this is a single chip modem combining a digital signal processor with precision analog-to-digital and digital-to-analog functions on a single silicon die. Such devices offer the semiconductor customer significant savings in manufacturing costs due to the resulting reduction of chip-to-chip interconnections.

Mixed-signal IC test and measurement has grown into a highly specialized field of electrical engineering. However, test engineering is still a relatively unknown profession compared with IC design engineering. It has become harder to hire and train new engineers to become skilled mixed-signal test engineers. It may take one to two years for a mixed-signal test engineer to develop enough knowledge and experience to develop adequate test solutions. The slow learning curve for mixed-signal test engineers is largely due to the shortage of written materials and university-level courses on the subject of mixed-signal testing. While many books have been devoted to the subject of digital test and testability, the same cannot be said for analog and mixed-signal automated test and measurement.

Training for mixed-signal test engineers has historically started with a sink-or-swim training course covering the use of the test equipment itself, with little or no training on the basics of mixed-signal test and measurement. This equipment-centric approach to training is analogous to teaching a student how to drive by simply explaining the mechanics of the automobile itself (pull this knob, push that pedal, etc.). It would be unwise to assign such an inadequately trained student to drive from L.A. to Pittsburgh without a roadmap and without a working knowledge of trivialities such as stop lights and police sirens. Similarly, a new test engineer is often assigned to develop tests for a complex circuit without training in basic test definitions and common test techniques.

The test engineer is also expected to contribute to the definition of testability circuits that are incorporated into the design of the device to be tested. Again, there is little formal reference material or training on the subject of basic mixed-signal design for test (DfT). As a result, new test engineers often overlook basic deficiencies in the circuit architecture that prevent the device from being tested thoroughly and economically.

This book was written in response to the shortage of basic course material for mixed-signal test and measurement. The book assumes a solid background in analog and digital circuits as well as a working knowledge of computers and computer programming. A background in digital signal processing and statistical analysis is also helpful, though not absolutely necessary. This material is designed to be useful as both a university textbook and as a reference manual for the beginning professional test engineer. Like many specialized technical materials, this book will

most likely become partially outdated before publication. Hopefully, it will at least serve as an amusing historical record of how things were done back in the twentieth century.

The prerequisite for this book is a junior-level course in linear continuous-time and discrete-time systems, as well as exposure to elementary probability and statistical concepts. Fortunately, these two courses are usually required at most universities.

The book is divided into 16 chapters. Chapter 1 presents an introduction to the context in which mixed-signal testing is performed and why it is necessary. Chapter 2 examines the process by which test programs are generated, from device data sheet to test plan to test code. Test program structure and functionality are also discussed in Chapter 2. Chapter 3 introduces basic DC measurement definitions, including continuity, leakage, offset, gain, DC power supply rejection ratio, and many other types of fundamental DC measurements.

Chapter 4 covers the basics of absolute accuracy, resolution, software calibration, standards traceability, and measurement repeatability. In addition, basic data analysis is presented in Chapter 4. A more thorough treatment of data analysis and statistical analysis is delayed until Chapter 15.

Chapter 5 takes a closer look at the architecture of a generic mixed-signal ATE tester. The generic tester includes instruments such as DC sources, meters, waveform digitizers, arbitrary waveform generators, and digital pattern generators with source and capture functionality.

Chapter 6 presents an introduction to both ADC and DAC sampling theory. DAC sampling theory is applicable to both DAC circuits in the device under test and to the arbitrary waveform generators in a mixed-signal tester. ADC sampling theory is applicable to both ADC circuits in the device under test and to waveform digitizers in a mixed-signal tester. Coherent multi-tone sample sets are also introduced as an introduction to DSP based testing. Chapter 7 further develops sampling theory concepts and DSP-based testing methodologies, which are at the core of many mixed-signal test and measurement techniques. FFT fundamentals, windowing, frequency domain filtering, and other DSP-based testing fundamentals are covered in Chapters 6 and 7.

Chapter 8 shows how basic AC channel tests can be performed economically using DSP-based testing. This chapter covers only nonsampled channels, consisting of combinations of op amps, analog filters, PGAs and other continuous-time circuits. Chapter 9 explores many of these same tests as they are applied to sampled channels, which include DACs, ADCs, sample and hold (S/H) amplifiers, etc.

Chapter 10 explains how the basic accuracy of ATE test equipment can be extended using specialized software routines. This subject is not necessarily taught in formal ATE tester classes, yet it is critical in the accurate measurement of many DUT performance parameters.

Testing of DACs is covered in Chapter 11. Several kinds of DACs are studied, including traditional binary-weighted, resistive ladder, pulse-width modulation (PWM), and sigma-delta architectures. Traditional measurements like INL, DNL, and absolute error are discussed. Several kinds of DAC architectures are explored, with an emphasis on their respective weaknesses and common testing methodologies. Chapter 12 builds upon the concepts in Chapter 11 to show how ADCs are commonly tested. Again, several different kinds of ADCs are studied, including binary-weighted, dual-slope, flash, semiflash, and sigma-delta

architectures. The weaknesses of each design are explained, as well as the common methodologies used to probe their weaknesses.

Chapter 13 explores the gray art of mixed-signal DIB design. Topics of interest include component selection, power and ground layout, crosstalk, shielding, transmission lines, and tester loading. Chapter 13 also illustrates several common DIB circuits and their use in mixed-signal testing.

Chapter 14 gives a brief introduction to some of the techniques for analog and mixed-signal design for test. There are fewer structured approaches for mixed-signal DfT than for purely digital DfT. The more common ad hoc methods are explained, as well as some of the industry standards such as IEEE Std. 1149.1 and 1149.4.

A brief review of statistical analysis and Gaussian distributions is presented in Chapter 15. This chapter also shows how measurement results can be analyzed and viewed using a variety of software tools and display formats. Datalogs, shmoo plots, and histograms are discussed. Also, statistical process control (SPC) is explained, including a discussion of process control metrics such as C_p and C_{pk}.

Chapter 16 examines the economics of production testing. The economics of test are affected by many factors such as equipment purchase price, test floor overhead costs, test time, dual-head testing, multisite testing, and time to market. A test engineer's debugging skills heavily impacts time to market. Chapter 16 examines the test debugging process to attempt to set down some general guidelines for debugging mixed-signal test programs. Finally, emerging trends that affect test economics and test development time are presented in Chapter 16. Some or all of these trends will shape the future course of mixed-signal test and measurement.

The preliminary versions of this complete manuscript were reviewed by a number of students and practicing test engineers. We would like to thank those professionals and students who gave us extensive corrections and feedback to improve this textbook: Steve Lyons (Lucent Technologies/Teradyne, Inc.), Jim Larson and Gary Moraes (Teradyne, Inc.), Justin Ewing (Texas A&M University/Texas Instruments, Inc.) Pramodchandran Variyam (Georgia Tech/Texas Instruments, Inc.), and Geoffrey Zhang (Texas Instruments, Inc.). We also thank Juli Boman (Teradyne, Inc.) and Ted Lundquist (Schlumberger Test Equipment) for providing photographs for Chapter 1.

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CHAPTER 1

Overview of Mixed-Signal Testing

1.1 Mixed-Signal Circuits

1.1.1 Analog, Digital, or Mixed-Signal?

Before delving into the details of mixed-signal IC test and measurement, one might first ask a few good questions. Exactly what are mixed-signal circuits? How are they used in typical applications? Why do we have to test mixed-signal circuits in the first place? What is the role of a test engineer, and how does it differ from that of a design engineer or product engineer? Most training classes offered by mixed-signal tester companies assume that the students already know the answers to these questions. For instance, a typical automated test equipment (ATE) training class shows the students how to program the per-pin current leakage measurement instruments in the tester before the students even know why leakage current is an important parameter to measure. This book will answer many of the what's, when's, and why's of mixed-signal testing, as well as the usual how's. Let's start with a very basic question: what is a mixed-signal circuit?

A mixed-signal circuit can be defined as a circuit consisting of both digital and analog elements. By this definition, a comparator is one of the simplest mixed-signal circuits. It compares two analog voltages and determines if the first voltage is greater than or less than the second voltage. Its digital output changes to one of two states depending on the outcome of the comparison. In effect, a comparator is a one-bit analog-to-digital converter (ADC). It might also be argued that a simple digital inverter is a mixed-signal circuit, since its digital input controls an "analog" output which swings between two fixed voltages, rising, falling, overshooting, and undershooting according to the laws of analog circuits. In fact, in certain extremely high-frequency applications the outputs of digital circuits have been tested using mixed-signal testing methodologies.[1]

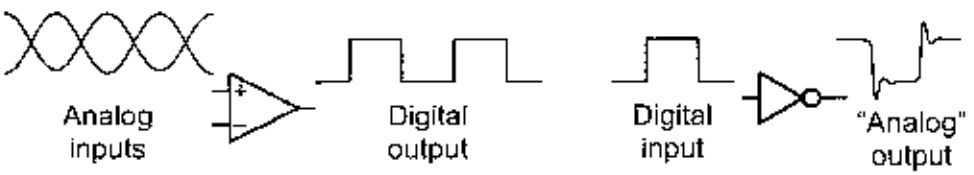

Figure 1.1. Comparator and inverter - analog, digital, or mixed-signal?

Some mixed-signal experts might argue that a comparator and an inverter are not mixed-signal devices at all. The comparator is typically considered an analog circuit, while an inverter is considered a digital circuit (Figure 1.1). Other examples of borderline mixed-signal devices are analog switches and programmable gain amplifiers. The purist might argue that mixed-signal

circuits are those that involve some sort of nontrivial interaction between digital signals and analog signals. Otherwise, the device is simply a combination of digital logic and separate analog circuitry coexisting on the same die or circuit board. The line between mixed-signal circuits and analog or digital circuits is blurry if one wants to be pedantic.

Fortunately, the blurry lines between digital, analog, and mixed-signal are completely irrelevant in the context of mixed-signal test and measurement. Most complex mixed-signal devices include at least some stand-alone analog circuits that do not interact with digital logic at all. Thus, the testing of op amps, comparators, voltage references, and other purely analog circuits must be included in a comprehensive study of mixed-signal testing. This book encompasses the testing of both analog and mixed-signal circuits, including many of the borderline examples. Digital testing will only be covered superficially, since testing of purely digital circuits has been extensively documented elsewhere.[2-4]

1.1.2 Common Types of Analog and Mixed-Signal Circuits

Analog circuits (also known as *linear circuits*) include operational amplifiers, active or passive filters, comparators, voltage regulators, analog mixers, analog switches, and other specialized functions such as Hall effect transistors. One of the very simplest circuits that can be considered to fall into the mixed-signal realm is the CMOS analog switch. In this circuit, the resistance of a CMOS transistor is varied between high impedance and low impedance under control of a digital signal. The off-resistance may be as high as one megaohm or more, while the on-resistance may be 100 Ω or less. Banks of analog switches can be interconnected in a variety of configurations, forming more complex circuits such as analog multiplexers and demultiplexers and analog switch matrices.

Another simple type of mixed-signal circuit is the programmable gain amplifier (PGA). The PGA is often used in the front end of a mixed-signal circuit to allow a wider range of input signal amplitudes. Operating as a digitally adjusted volume control, the PGA is set to high gains for low-amplitude input signals and low gains for high-amplitude input signals. The next circuit following a PGA is thus provided with a consistent signal level. Many circuits require a consistent signal level to achieve optimum performance. These circuits therefore benefit from the use of PGAs.

PGAs and analog switches involve a trivial interaction between the analog and digital circuits. This is why they are not always considered to be mixed-signal circuits at all. The most common circuits that can truly be considered mixed-signal devices are analog to digital converters (A/Ds or ADCs) and digital to analog converters (D/As or DACs). While the abbreviations A/D and ADC are used interchangeably in the electronics industry, this book will always use the term ADC for consistency. Similarly, the term DAC will be used throughout the book rather than D/A. An ADC is a circuit that samples a continuous analog signal at specific points in time and converts the sampled voltages (or currents) into a digital representation. Each digital representation is called a *sample*. Conversely, a DAC is a circuit that converts digital samples into analog voltages (or currents). ADCs and DACs are the most common mixed-signal components in complex mixed-signal designs, since they form the interface between the physical world and the world of digital logic.

Comprehensive testing of DACs and ADCs is an expansive topic, since there are a wide variety of ADC and DAC designs and a wide variety of techniques to test them. For example, an ADC which is only required to sample once per second may employ a dual slope conversion

architecture, whereas a 100-MHz video ADC may have to employ a much faster flash conversion architecture. The weaknesses of these two architectures are totally different. Consequently, the testing of these two converter types is totally different. Similar differences exist between the various types of DACs.

Another common mixed-signal circuit is the phase locked loop, or PLL. PLLs are typically used to generate high-frequency reference clocks or to recover a synchronous clock from an asynchronous data stream. In the former case, the PLL is combined with a digital divider to construct a frequency multiplier. A relatively low-frequency clock, say, 50 MHz, is then multiplied by an integer value to produce a higher-frequency master clock, such as 1 GHz. In the latter case, the recovered clock from the PLL is used to latch the individual bits or bytes of the incoming data stream. Again, depending on the nature of the PLL design and its intended use, the design weaknesses and testing requirements can be very different from one PLL to the next.

1.1.3 Applications of Mixed-Signal Circuits

Many mixed-signal circuits consist of combinations of amplifiers, filters, switches, ADCs, DACs, and other types of specialized analog and digital functions. End-equipment applications such as cellular telephones, hard disk drives, modems, motor controllers, and multimedia audio and video products all employ complex mixed-signal circuits. While it is important to test the individual circuits making up a complex mixed-signal device, it is also important to perform system-level tests. System-level tests guarantee that the circuit as a whole will perform as required in the end-equipment application. Thorough testing of large-scale mixed-signal circuits therefore requires at least a basic understanding of the end-equipment application in which the circuits will be used.

As an example of a mixed-signal application, let us consider a common consumer product using many mixed-signal subcircuits. Figure 1.2 shows a simplified block diagram of a complex mixed-signal application, the digital cellular telephone. It represents an excellent example of a complex mixed-signal system because it employs a variety of mixed-signal components. Since the digital cellular telephone will be used as an example throughout this book, we shall examine its operation in some detail.

A cellular telephone consists of many analog, digital, and mixed-signal circuits working together in a complex fashion. The cellular telephone user interfaces with the keyboard and display to answer incoming calls and to initiate outgoing calls. The control microprocessor handles the interface with the user. It also performs many of the supervisory functions of the telephone, such as helping coordinate the handoff from one base station to the next as the user travels through each cellular area. The control microprocessor selects the incoming and outgoing transmission frequencies by sending control signals to the frequency synthesizer. The synthesizer often consists of several PLLs, which control the mixers in the radio frequency (RF) section of the cellular telephone. The mixers convert the relatively low-frequency signals of the base-band interface to extremely high frequencies that can be transmitted from the cellular telephone's radio antenna. They also convert the very high-frequency incoming signals from the base station into lower-frequency signals that can be processed by the base-band interface.

The voice-band interface, digital signal processor (DSP), and base-band interface perform most of the complex operations. The voice-band interface converts the user's voice into digital samples using an ADC. The volume of the voice signal from the microphone can be adjusted automatically using a programmable gain amplifier (PGA) controlled by either the DSP or the

control microprocessor. Alternatively, the PGA may be controlled with a specialized digital circuit built into the voice-band interface itself. Either way, the PGA and automatic adjustment mechanism form an automatic gain control (AGC) circuit. Before the voice signal can be digitized by the voice-band interface ADC, it must first be low-pass filtered to avoid unwanted high-frequency components that might cause aliasing in the transmitted signal. (Aliasing is a type of distortion that can occur in sampled systems, making the speaker's voice difficult to understand.)

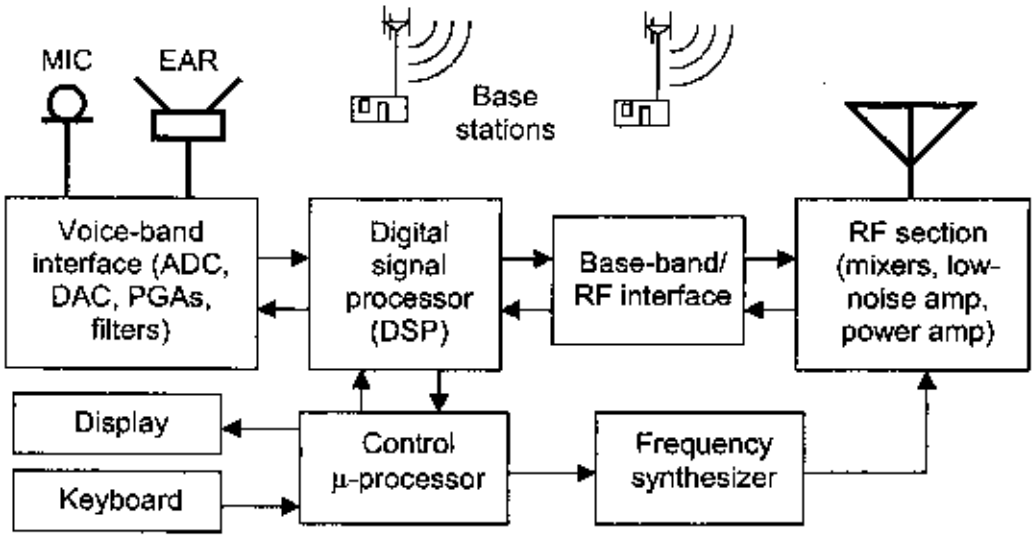

Figure 1.2. Digital cellular telephone.

The digitized samples are sent to the DSP, where they are compressed using a mathematical process called *vocoding*. The vocoding process converts the individual samples of the sound pressure waves into samples that represent the *essence* of the user's speech. The vocoding algorithm calculates a time-varying model of the speaker's vocal tract as each word is spoken. The characteristics of the vocal tract change very slowly compared to the sound pressure waves of the speaker's voice. Therefore, the vocoding algorithm can compress the important characteristics of speech into a much smaller set of data bits than the digitized sound pressure samples. The vocoding process is therefore a type of data compression algorithm that is specifically tailored for speech. The smaller number of transmitted bits frees up airspace for more cellular telephone users. The vocoder's output bits are sent to the base-band interface and RF circuits for modulation and transmission. The base-band interface acts like a modem, converting the digital bits of the vocoder output into modulated analog signals. The RF circuits then transmit the modulated analog waveforms to the base station.

In the receiving direction, the process is reversed. The incoming voice data are received by the RF section and demodulated by the base-band interface to recover the incoming vocoder bit stream. The DSP converts the incoming bit stream back into digitized samples of the incoming speaker's voice. These samples are then passed to the DAC and low pass reconstruction filter of the voice-band interface to reconstruct the voltage samples of the incoming voice. Before the received voice signal is passed to the earpiece, its volume is adjusted using a second PGA. This earpiece PGA is adjusted by signals from the control microprocessor, which monitors the telephone's volume control buttons to determine the user's desired volume setting. Finally, the signal must be passed through a low impedance buffer to provide the current necessary to drive the earpiece.

Several common cellular telephone circuits are not shown in Figure 1.2. These include DC voltage references and voltage regulators that may exist on the voice-band interface or the base-band processor, analog multiplexers to control the selection of multiple voice inputs, and power-on reset circuits. In addition, a watchdog timer is often included to periodically wake the control microprocessor from its battery-saving idle mode. This allows the microprocessor to receive information such as incoming call notifications from the base station. Clearly, the digital cellular telephone represents a good example of a complex mixed-signal system. The various circuit blocks of a cellular telephone may be grouped into a small number of individual integrated circuits, called a *chipset*, or they may all be combined into a single chip. The test engineer must be ready to test the individual pieces of the cellular telephone and/or to test the cellular telephone as a whole. The increasing integration of circuits into a single semiconductor die is one of the most challenging aspects of mixed-signal test engineering.

1.2 Why Test Mixed-Signal Devices?

1.2.1 The CMOS Fabrication Process

Integrated circuits (ICs) are fabricated using a series of photolithographic printing, etching, and doping steps. Using a digital CMOS fabrication process as an example, let us look at the idealized IC fabrication process. Some of the steps involved in printing a CMOS transistor pair are illustrated in Figure 1.3a-f. Starting with a lightly doped P^- wafer, a layer of silicon dioxide (SiO_2) is deposited on the surface (Figure 1.3a). Next, a negative photoresist is laid down on top of the silicon dioxide. A pattern of ultraviolet light is then projected onto the photoresist using a photographic mask. The photoresist becomes insoluble in the areas where the mask allows the ultraviolet light to pass (Figure 1.3b). An organic solvent is used to dissolve the nonexposed areas of the photoresist (Figure 1.3c). After baking the remaining photoresist, the exposed areas of oxide are removed using an etching process (Figure 1.3d). Next, the exposed areas of silicon are doped to form an N-well using either diffusion or ion implantation (Figure 1.3e).

After many additional steps of printing, masking, etching, implanting, and chemical vapor deposition,[5] a complete integrated circuit can be fabricated as illustrated in Figure 1.3f. The uneven surfaces are exaggerated in the diagram to show that the various layers of oxide, polysilicon, and metal are not at all flat. Even with these exaggerations, this diagram only represents an idealized approximation of actual fabricated circuit structures. The actual circuit structures are not nearly as well defined as textbook diagrams would lead us to believe. Cross sections of actual integrated circuits reveal a variety of nonideal physical characteristics that are not entirely under the semiconductor manufacturer's control. Certain characteristics, such as doping profiles that define the boundaries between P and N regions, are not even visible in a cross-section view. Nevertheless, they can have a profound effect on many important analog and mixed-signal circuit characteristics.

1.2.2 Real-World Circuits

Like any photographic printing process, the IC printing process is subject to blemishes and imperfections. These imperfections may cause catastrophic failures in the operation of any individual IC, or they may cause minor variations in performance from one IC to the next. Mixed-signal ICs are often extremely sensitive to tiny imperfections or variations in the printing and doping processes. Many of the fabrication defects that cause problems in mixed-signal devices are difficult to photograph, even with a powerful scanning electron microscope (SEM).

For example, a doping error may or may not cause an observable physical defect. However, doping errors can introduce large DC offsets, distortions, and other problems that result in IC performance failures.

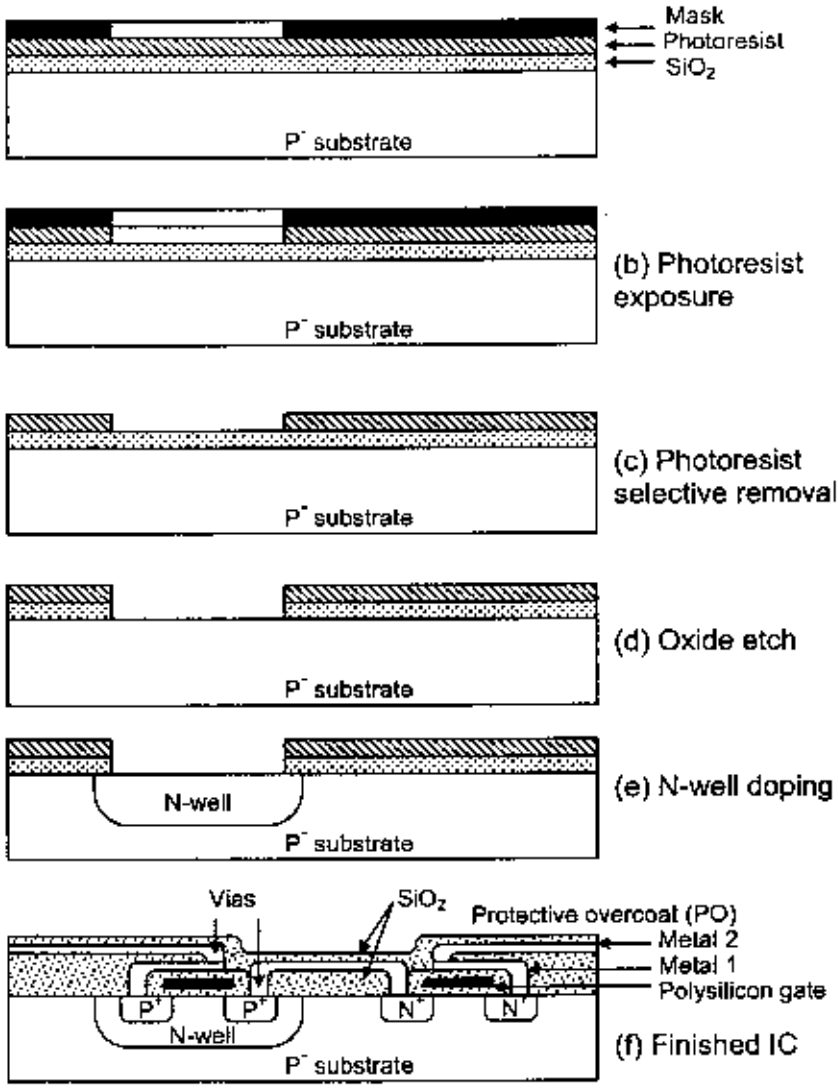

Figure 1.3. CMOS fabrication steps.

Certain types of defects can be photographed quite easily. Figure 1.4 shows a nondefective circuit as photographed using a FIB machine (a device similar to a scanning electron microscope). Compared to the idealized textbook circuit representation, the metal traces are rounded and imperfect.

In digital circuits, such imperfections in shape may be largely unimportant. However, in mixed-signal circuits, the parasitic capacitance between these traces and surrounding structures may represent significant circuit elements. The exact three-dimensional shape of a metal line and its spacing to adjacent layers may therefore affect the performance of the circuit under test. As circuit geometries continue to shrink, these performance sensitivities will only become more exaggerated. Although a mixed-signal circuit may be essentially functional in the presence of

these minor imperfections, it may not meet all its required specifications. For this reason, mixed-signal devices are often tested exhaustively to guard against defects that are not necessarily catastrophic.

Figure 1.4. FIB micrograph of metal traces on an integrated circuit obtained using a Schlumberger AMS 3000 (photo courtesy Schlumberger Test Equipment).

Catastrophic defects such as short circuits and open circuits are often easier to detect with test equipment than the subtler ones common in mixed-signal devices. Not surprisingly, the catastrophic defects are often much easier to photograph as well. Several typical defect types are shown in Figures 1.5–1.8. Figure 1.5 shows a defective metal contact, or via, caused by underetching. Figure 1.6 shows a defective via caused by photomask misalignment. A completely defective via usually results in a totally defective circuit, since it represents a complete open circuit. A more subtle problem is a partially connected via, which may exhibit an abnormally high contact resistance. Depending on the amount of excess resistance, the results of a partially connected via can range from minor DC offset problems to catastrophic distortion problems.

Figure 1.7 shows incomplete etching of the metal surrounding a circuit trace. Incomplete etching can result in catastrophic shorts between circuit nodes. Finally, Figure 1.8 shows a surface defect caused by particulate matter landing on the surface of the wafer or on a photographic mask during one of the processing steps. Again, this type of defect results in a short between circuit nodes. Other catastrophic defects include surface scratches, broken bond wires, and surface explosions caused by electrostatic discharge in a mishandled device. Defects such as these are the reason each semiconductor device must be tested before it can be shipped to the customer.

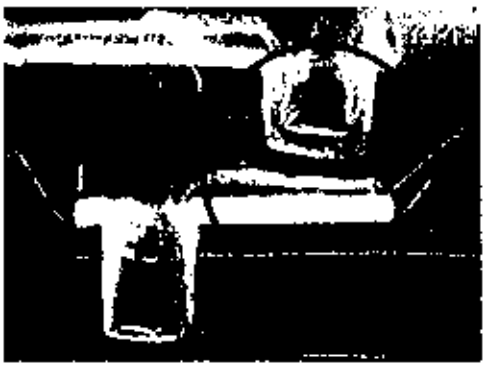

Figure 1.5. Underetched via.

Figure 1.6. Misaligned via.

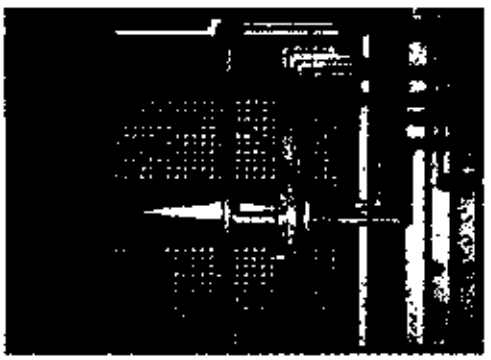

Figure 1.7. Incomplete metal etch.

Figure 1.8. Blocked etch (particulate defect).

It has been said that production testing adds no value to the final product. Testing is an expensive process that drives up the cost of integrated circuits without adding any new functionality. Testing cannot change the quality of the individual ICs; it can only *measure* quality if it already exists. However, semiconductor companies would not spend money to test products if the testing process did not add value. This apparent discrepancy is easily explained if we recognize that the product is actually the entire shipment of devices, not just the individual ICs. The quality of the product is certainly improved by testing, since defective devices are not shipped. Therefore, testing does add value to the product, as long as we define the product correctly.

1.2.3 What Is a Test Engineer?

We have mentioned the term *test engineer* several times without actually defining what test engineering is. Perhaps this would be a good time to discuss the traditional roles of test engineers, design engineers, product engineers, and systems engineers. Although each of these engineering professions is involved in the development and production of semiconductor devices, each profession entails its own set of tasks and responsibilities. The various engineering professions are easiest to define if we examine the process by which a new semiconductor product is developed and manufactured.

A new semiconductor product typically begins in one of two ways. Either a customer requests a particular type of product to fill a specific requirement, or a marketing organization realizes an opportunity to produce a product that the market needs. In either case, systems engineers help define the technical requirements of the new product so that it will operate

correctly in the end-equipment application. The systems engineers are responsible for defining and documenting the customer's requirements so that the rest of the engineering team can design the product and successfully release it to production.

After the systems engineers have defined the product's technical requirements, design engineers develop the corresponding integrated circuit. Hopefully, the new design meets the technical requirements of the customer's application. Unfortunately, integrated circuits sometimes fail to meet the customer's needs. The failure may be due to a fabrication defect or it may be due to a flaw or weakness in the circuit's design. These failures must be detected before the product is shipped to the customer.

The test engineer's role is to generate hardware and software that will be used by automated test equipment (ATE) to guarantee the performance of each device after it is fabricated. The test software directs the ATE tester to apply a variety of electrical stimuli (such as digital signals and sine waves) to the device under test (DUT). The ATE tester then observes the DUT's response to the various test stimuli to determine whether the device is good or bad (Figure 1.9). A typical mixed-signal DUT must pass hundreds or even thousands of stimulus/response tests before it can be shipped to the customer.

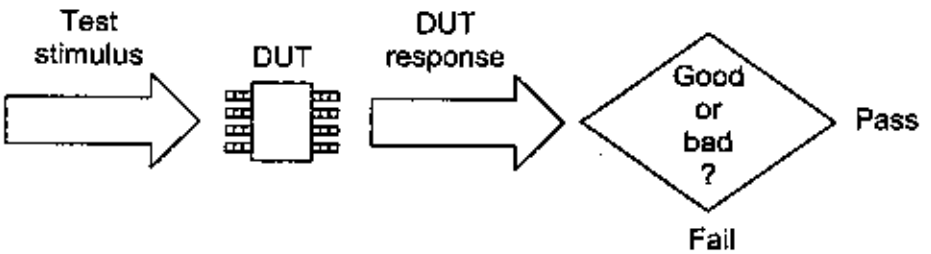

Figure 1.9. Test stimulus and DUT response verification.

Sometimes the test engineer is also responsible for developing hardware and software that modifies the structure of the semiconductor die to adjust parameters like DC offset and AC gain, or to compensate for grotesque manufacturing defects. Despite claims that production testing adds no value, this is one way in which the testing process can actually enhance the quality of the individual ICs. Circuit modifications can be made in a number of ways, including laser trimming, fuse blowing, and writing to nonvolatile memory cells.

The test engineer is also responsible for reducing the cost of testing through test time reductions and other cost-saving measures. The test cost reduction responsibility is shared with the product engineer. The product engineer's primary role is to support the production of the new device as it matures and proceeds to profitable volume production. The product engineer helps identify and correct process defects, design defects, and tester hardware and software defects.

Sometimes the product engineering function is combined with the test engineering function, forming a single test/product engineering position. The advantage of the combined job function is that the product engineering portion of the job can be performed with a much more thorough understanding of the device and test program details. The disadvantage is that the product engineering responsibilities may interfere with the ability of the engineer to become an expert on the use of the complex test equipment. The choice of combined versus divided job functions is highly dependent on the needs of each organization.

1.3 Post-Silicon Production Flow

1.3.1 Test and Packaging

After silicon wafers have been fabricated, many additional production steps remain before a final packaged device is ready for shipment to the customer. The untested wafers (Figure 1.10) must first be probed using automated test equipment to prevent bad dies from passing on to further production steps. The bad dies can be identified using ink dots, which are applied either after each die is tested or after the whole wafer has been tested. Offline inking is a method used to electronically track bad dies using a computer database. Using pass/fail information from the database, bad dies are inked after the wafer has been removed from the test equipment.

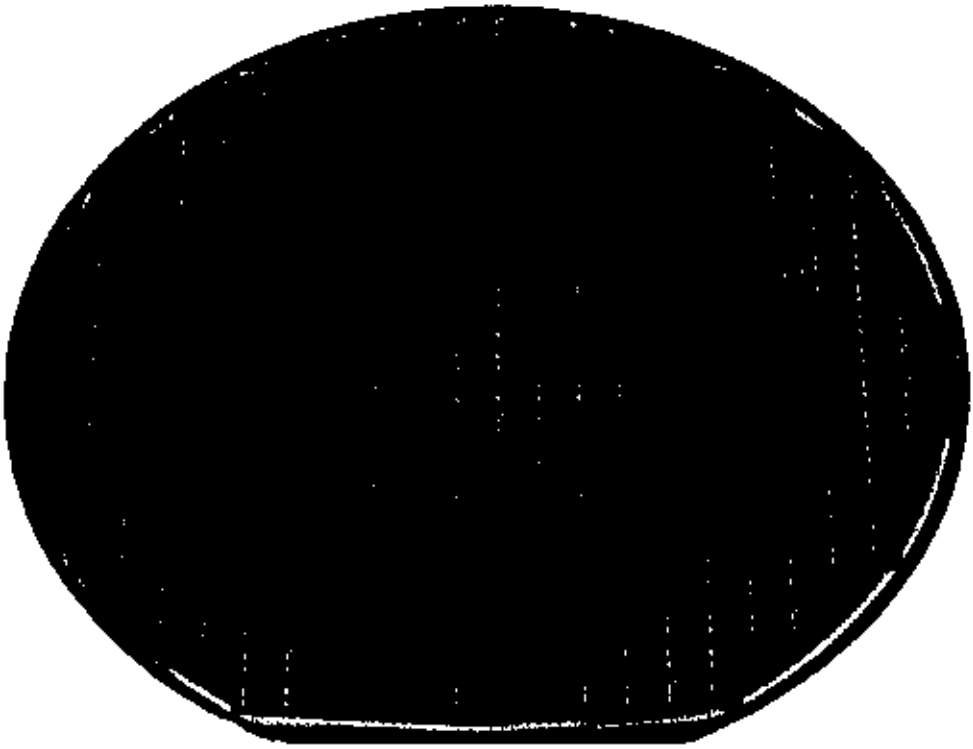

Figure 1.10. Untested wafer.

The wafers are then sawed into individual dies and the good ones are attached to lead frames. Lead frames are punched metal holders that eventually become the individual leads of the packaged device. Bond wires are attached from each die's bond pads to the appropriate lead of the lead frame. Then plastic is injection-molded around the dies and lead frame to form packaged devices. Finally, the individual packaged devices are separated from one another by trimming them from the lead frame.

After the leads have been trimmed and formed, the devices are ready for final testing on a second ATE tester. Final testing guarantees that the performance of the device did not shift during the packaging process. For example, the insertion of plastic over the surface of the die changes the electrical permitivity near the surface of the die. Consequently, trace-to-trace capacitances are increased, which may affect sensitive nodes in the circuit. In addition, the

injection-molded plastic introduces mechanical stresses in the silicon, which may consequently introduce DC voltage shifts. Final testing also guarantees that the bond pads are all connected and that the die was not cracked, scratched, or otherwise damaged in the packaging process. After final testing, the devices are ready for shipment to the end-equipment manufacturer. Figure 1.11 shows a tray of tested quad flat pack (QFP) devices in a plastic carrier tray.

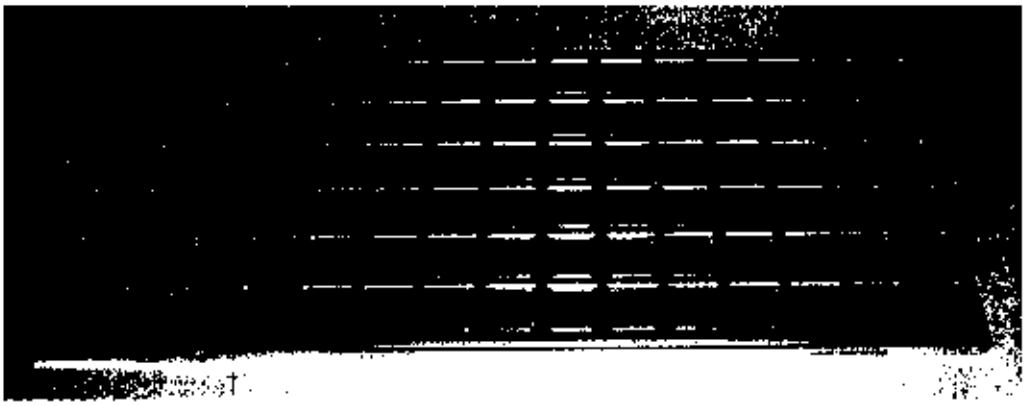

Figure 1.11. Tested QFP devices in a plastic carrier tray.

1.3.2 Characterization versus Production Testing

When prototype devices are first characterized, the ATE test program is usually very extensive. Tests are performed under many different conditions to evaluate worst-case conditions. For instance, the distortion of an amplifier output may be worse under one loading condition than another. All loading conditions must be tested to identify which one represents the worst-case test. Other examples of exhaustive characterization testing would be DC offset testing using multiple power supply voltages and harmonic distortion testing at multiple signal levels. Characterization testing must be performed over a large number of devices and over several production lots of material before the results can be considered statistically valid and trustworthy.

Characterization testing can be quite time consuming due to the large number of tests involved. Extensive characterization is therefore economically unacceptable in high-volume production testing of mixed-signal devices. Once worst-case test conditions have been established and the design engineers are confident that their circuits meet the required specifications, a more streamlined production test program is needed. The production test program is created from a subset of the characterization tests. The subset must be carefully chosen to guarantee that no bad devices are shipped. Product and test engineers must work very closely to make sure that the reduced test list still catches all manufacturing defects.

1.4 Test and Diagnostic Equipment

1.4.1 Automated Test Equipment

Automated test equipment is available from a number of commercial vendors, such as Teradyne, LTX, Agilent Technologies, and Schlumberger, to name a few. The Teradyne, Inc. Catalyst mixed-signal tester is shown in Figure 1.12. High-end ATE testers often consist of three major components: a test head, a workstation, and the mainframe.

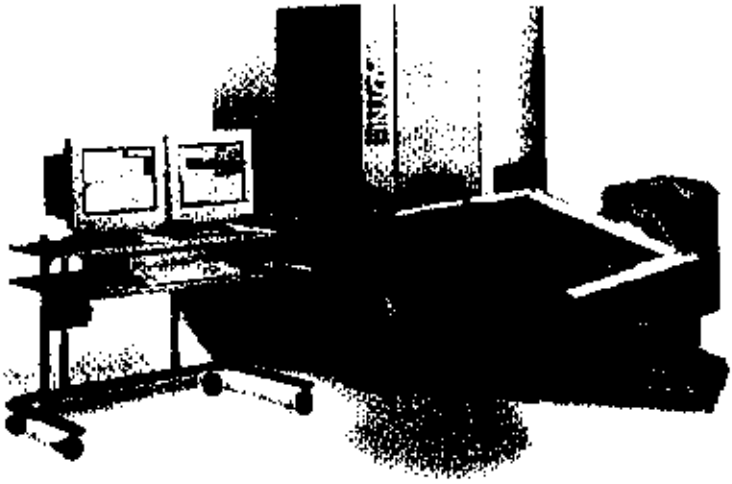

Figure 1.12. Teradyne Catalyst mixed-signal tester (photo courtesy Teradyne, Inc.).

The computer workstation serves as the user interface to the tester. The test engineer can debug test programs from the workstation using a variety of software tools from the ATE vendor. Manufacturing personnel can also use the workstation to control the day-to-day operation of the tester as it tests devices in production.

The mainframe contains power supplies, measurement instruments, and one or more computers that control the instruments as the test program is executed. The mainframe may also contain a manipulator to position the test head precisely. It may also contain a refrigeration unit to provide cooled liquid to regulate the temperature of the test head electronics.

Although much of the tester's electronics are contained in the mainframe section, the test head contains the most sensitive measurement electronics. These circuits are the ones which require close proximity to the device under test. For example, high-speed digital signals benefit from short electrical paths between the tester's digital drivers and the pins of the DUT. Therefore, the ATE tester's digital drivers and receivers are located in the test head close to the DUT.

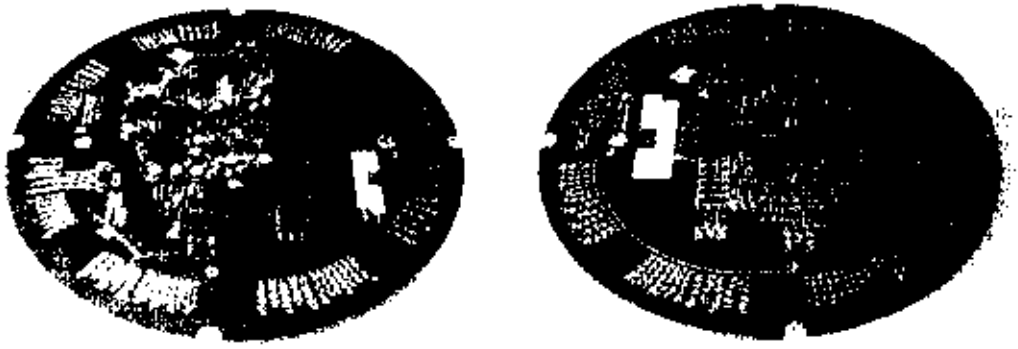

Figure 1.13. Device interface board (DIB) showing local circuits (left) and DUT socket (right).

A device interface board (DIB) forms the electrical interface between the ATE tester and the DUT. The DIB is also known as a *performance board*, *swap block*, or *family board*, depending on the ATE vendor's terminology. DIBs come in many shapes and sizes, but their main function

is to provide a temporary (socketed) electrical connection between the DUT and the electrical instruments in the tester. The DIB also provides space for DUT-specific local circuits such as load circuits and buffer amplifiers that are often required for mixed-signal device testing.

1.4.2 Wafer Probers

Wafer probers are robotic machines that manipulate wafers as the individual dies are tested by the ATE equipment. The prober moves the wafer underneath a set of tiny electrical probes attached to a probe card. The probes are connected to the electrical resources of the ATE tester through a probe interface board (PIB). The PIB is a specialized type of DIB board that may be connected to the probe card through coaxial cables and/or spring-loaded contacts called *pogo pins*. The PIB and probe card serve the same purpose for the wafer that the DIB board serves for the packaged device. They provide a means of temporarily connecting the DUT to the ATE tester's electrical instrumentation while testing is performed.

The prober informs the tester when it has placed each new die against the probes of the probe card. The ATE tester then executes a series of electrical tests on the die before instructing the prober to move to the next die. The handshaking between tester and prober insures that the tester only begins testing when a die is in position and that the prober does not move the wafer in midtest. Figure 1.14 shows a wafer prober manufactured by Electroglas, Inc., and closeup views of a probe card and its probe tips.

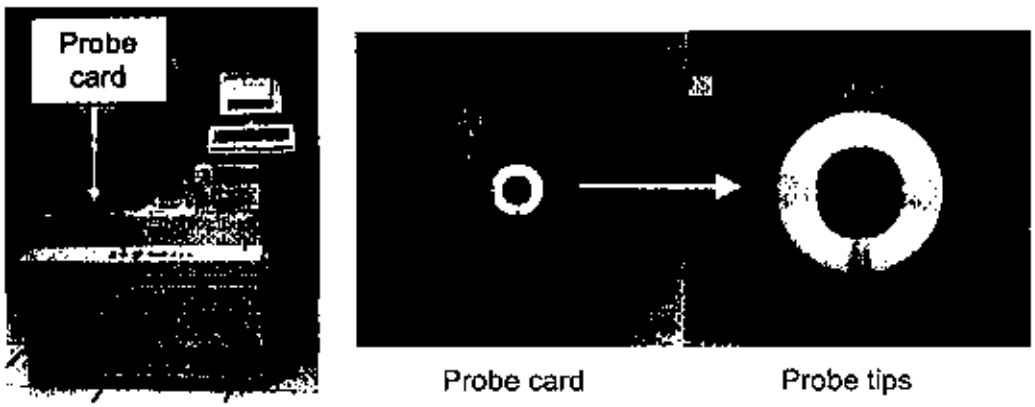

Figure 1.14. Electroglas wafer prober and probe card.

1.4.3 Handlers

Handlers are used to manipulate packaged devices in much the same way that probers are used to manipulate wafers. Handlers fall into two categories: gravity-fed and robotic. Robotic handlers are also known as *pick-and-place* handlers. Gravity-fed handlers are normally used with dual inline packages, while robotic handlers are used with devices having pins on all four sides or pins on the underside (ball grid array packages, for example). Figure 1.15 shows a gravity-fed handler. A robotic handler is shown in Figure 1.16.

Either type of handler has one main purpose: to make a temporary electrical connection between the DUT pins and the DIB board. Gravity-fed handlers often perform this task using a contactor assembly that grabs the device pins from either side with metallic contacts that are in turn connected to the DIB board. Robotic handlers usually pick up each device with a suction arm and then plunge the device into a socket on the DIB board.

In addition to providing a temporary connection to the DUT, handlers are also responsible for sorting the good DUTs from the bad ones based on test results from the ATE tester. Some handlers also provide a controlled thermal chamber where devices are allowed to "soak" for a few minutes so they can either be cooled or heated before testing. Since many electrical parameters shift with temperature, this is an important handler feature.

Figure 1.15. MultiTest gravity-fed handler.

Figure 1.16. Delta robotic handler.

1.4.4 E-Beam Probers

Electron beam probers, or e-beam probers as they are often called, are used to probe internal device signals while the device is being stimulated by the tester. These machines are very similar to scanning electron microscopes (SEMs). Unlike an SEM, an e-beam prober is designed to display variations in circuit voltage as the electron beam is swept across the surface of an operating DUT. Variations in the voltage levels on the metal traces in the IC appear as different shades of gray in the e-beam display (Figure 1.17). e-beam probers are extremely powerful diagnostic tools, since they provide measurement access to internal circuit nodes.

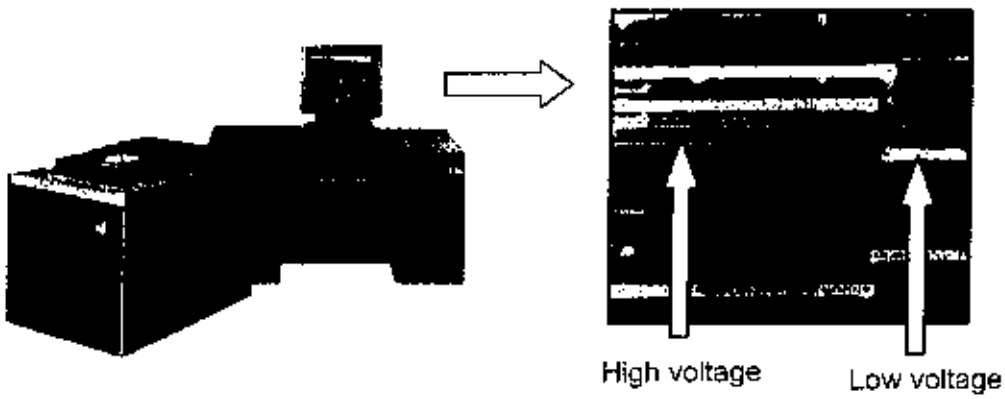

Figure 1.17. Schlumberger IDS-10000 electron beam prober (photo courtesy Schlumberger Test Equipment).

1.4.5 Focused Ion Beam Equipment

Focused ion beam (FIB) equipment is used in conjunction with e-beam probers to modify the device's metal traces and other physical structures. A FIB machine can cut holes in oxide and metal traces and can also lay down new metallic traces on the surface of the device (Figure 1.18). Experimental design changes can be implemented without waiting for a complete semiconductor fabrication cycle. The results of the experimental changes can then be observed on the ATE tester to determine the success or failure of the experimental circuit modifications.

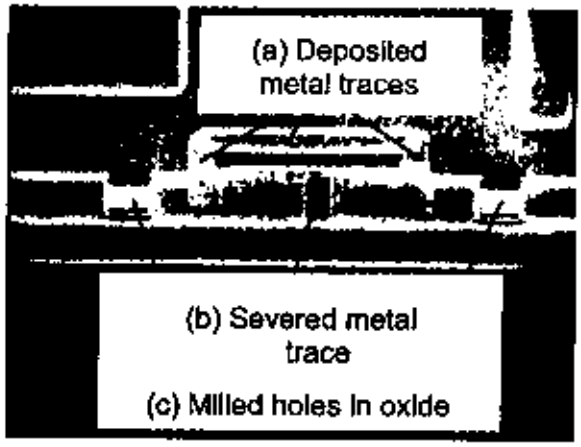

Figure 1.18. Circuit modifications implemented using FIB equipment.

1.4.6 Forced-Temperature Systems

As previously mentioned, a handler's thermal chamber allows characterization and testing of large numbers of DUTs at a controlled temperature. When characterizing a small number of DUTs at a variety of temperatures, a less expensive and cumbersome method of temperature control is needed. Portable forced-temperature systems allow DUT performance characterization

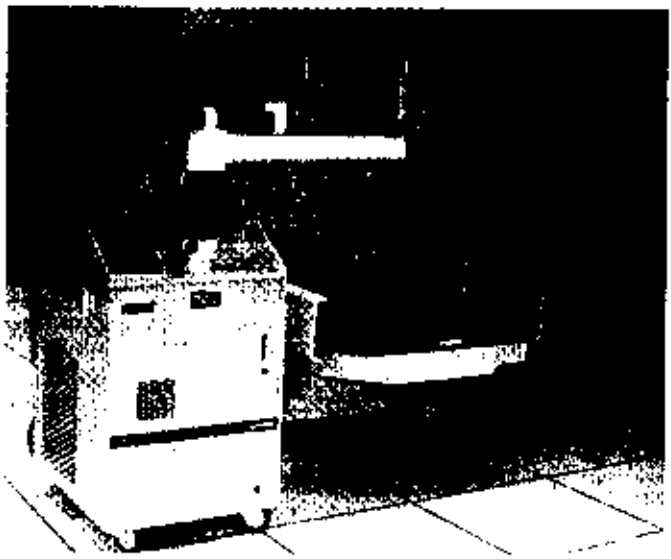

Figure 1.19. Temptronics forced-temperature system.

under a variety of controlled thermal conditions (Figure 1.19). The nozzle of a forced temperature system can be seated against the DIB board or bench characterization board, forming a small thermal chamber for the DUT. Many forced-temperature systems are able to raise or lower the DUT's ambient temperature across the full military range (–55 to +125°C).

1.5 New Product Development

1.5.1 Concurrent Engineering

On a poorly managed project, the test engineer might not see the specifications for a device to be tested until after the first prototype devices arrive. The devices must be screened as soon as possible to ship good prototypes to the customer even if they were never designed with testability in mind. In this case, the test engineer's role is completely reactive.

By contrast, the test engineer's role on a well-managed project is proactive. The design engineers and test engineers work together to add testability functions to the design that make the device easier and less expensive to test. The test engineer presents a test plan to the design engineers, explaining all the tests that are to be performed once the device is in production. The design engineers can catch mistakes in the test engineer's understanding of the device operation. They can help eliminate unnecessary tests or point out shortfalls in the proposed test list. This proactive approach is commonly called *concurrent engineering*. True concurrent engineering involves not only design and test engineering personnel, but also systems engineering, product engineering, and manufacturing personnel. Figure 1.20 shows a simplified concurrent engineering flow for the development and production release of a new semiconductor product.

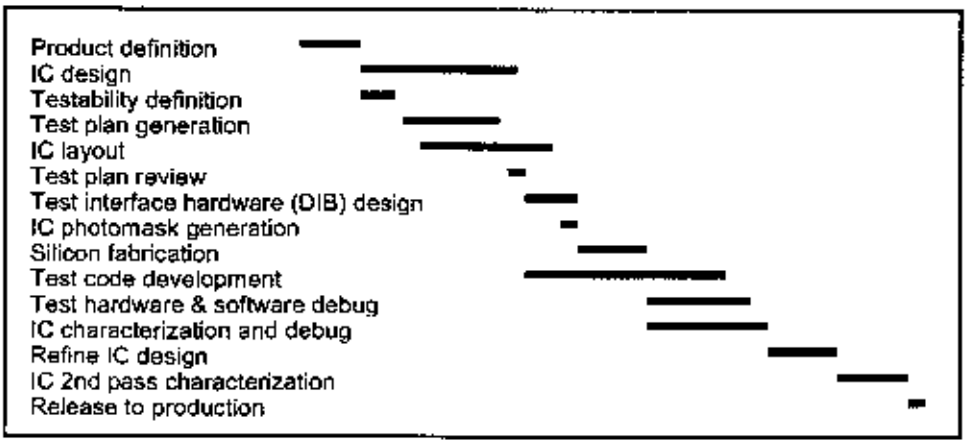

Figure 1.20. Concurrent engineering project flow.

The flow begins with a definition of the device requirements. These include product features, electrical specifications, power consumption requirements, die area estimates, etc. Once the device requirements are understood, the design team begins to design the individual circuits. In the initial design meetings, test and product engineers work with the design engineers to define the testability features that will make the device less expensive to test and manufacture. Test modes are added to the design to allow access to internal circuit nodes that otherwise would be unobservable in production testing. These observability test modes can be very useful in diagnosing device design flaws.

After the test modes are defined, the test engineer begins working on a test plan while the design process continues. Initially, the main purpose of a test plan is to allow design engineers and test engineers to agree upon a set of tests that will guarantee the quality of a product once it is in production. Eventually, the test plan will serve as documentation for future test and product engineers that may inherit the test program once it is complete. A well-written test plan contains brief background information about the product to be tested, the purpose of each test as it relates to the device specification, setup conditions for each test, and a hardware setup diagram for each test. Once the test plan is complete, all engineers working on the project meet to review the proposed test plan. Last-minute corrections and additions are added at this time. Design engineers point out deficiencies in the proposed test coverage while product engineers point out any problems that may arise on the production floor.

Once the test plan has been approved, the test engineer begins to design the necessary test interface hardware that will connect the automated test equipment to the device under test. Once the initial test hardware has been designed, the test engineer begins writing a test program that will run on the ATE tester. In modern ATE equipment, the test engineer can also debug many of the software routines in the test program before silicon arrives, using an offline simulation environment running on a stand-alone computer workstation.

After the design and layout of the device is complete, the fabrication masks are created from the design database. The database release process is known by various names, such as tape-out or pattern generation. Until pattern generation is complete, the test engineer cannot be certain that the pinout or functionality of the design will not undergo last-minute modifications. The test interface hardware is often fabricated only after the pattern generation step has been completed.

While the silicon wafers and the DIB board are fabricated, the test engineer continues developing the test program. Once the first silicon wafers arrive, the test engineer begins debugging the device, DIB hardware, and software on the ATE tester. Any design problems are reported to the design engineers, who then begin evaluating possible design errors. A second design pass is often required to correct errors and to align the actual circuit performance with specification requirements. Finally, the corrected design is released to production by the product engineer, who then supports the day-to-day manufacturing of the new product.

Of course, the idealized concurrent engineering flow is a simplification of what happens in a typical company doing business in the real world. Concurrent engineering is based on the assumption that adequate personnel and other resources are available to write test plans and generate test hardware and software before the first silicon wafers arrive. It also assumes that only one additional design pass is required to release a device to production. In reality, a high-performance device may require several design passes before it can be successfully manufactured at a profit. This flow also assumes that the market does not demand a change in the device specifications in midstream - a poor assumption in a dynamic world. Nevertheless, concurrent engineering is consistently much more effective than a disjointed development process with poor communication between the various engineering groups.

1.6 Mixed-Signal Testing Challenges

1.6.1 Time to Market

Time to market is a pressing issue for semiconductor manufacturers. Profit margins for a new product are highest shortly after it has been released to the market. Margins begin to shrink as

competitors introduce similar products at lower prices. The lack of a complete, cost-effective test program is often the main bottleneck preventing the release a new product to profitable volume production.

Mixed-signal test programs are particularly difficult to produce in a short period of time. Surprisingly, the time spent writing test code is often significantly less than the time spent learning about the device under test, defining the test plan, designing the test hardware, and debugging the ATE test solution once silicon is available. Much of the time spent in the debugging phase of test development is actually spent debugging device problems. Mixed-signal test engineers often spend as much time running experiments for design engineers to isolate design errors as they spend debugging their own test code. Perhaps the most aggravating debug time of all is the time spent tracking down problems with the tester itself or the tester's software.

1.6.2 Accuracy, Repeatability, and Correlation

Accuracy is a major concern for mixed-signal test engineers. It is very easy to get an answer from a mixed-signal ATE tester that is simply incorrect. Inaccurate answers are caused by a bewildering number of problems. Electromagnetic interference, improperly calibrated instruments, improperly ranged instruments, and measurements made under incorrect test conditions can all lead to inaccurate test results.

Repeatability is the ability of the test equipment and test program to give the same answer multiple times. Actually, a measurement that never changes at all is suspicious. It sometimes indicates that the tester is improperly configured, giving the same incorrect answer repeatedly. A good measurement typically shows some variability from one test program execution to the next, since electrical noise is present in all electronic circuits. Electrical noise is the source of many repeatability problems.

Another problem facing mixed-signal test engineers is correlation between the answers given by different pieces of measurement hardware. The customer or design engineer often finds that the test program results do not agree with measurements taken using bench equipment in their lab. The test engineer must determine which answer is correct and why there is a discrepancy. It is also common to find that two supposedly identical testers or DIB boards give different answers or that the same tester gives different answers from day to day. These problems frequently result from obscure hardware or software errors that may take days to isolate. Correlation efforts can represent a major portion of the time spent debugging a test program.

1.6.3 Electromechanical Fixturing Challenges

The test head and DIB board must ultimately make contact to the DUT through the handler or prober. There are few mechanical standards in the ATE industry to specify how a tester should be docked to a handler or prober. The test engineer has to design a DIB board that not only meets electrical requirements, but also meets the mechanical docking requirements. These requirements include board thickness, connector locations, DUT socket mechanical holes, and various alignment pins and holes.

Handlers and probers must make a reliable electrical connection between the DUT and the tester. Unfortunately, the metallic contacts between DUT and DIB board are often very inductive and/or capacitive. Stray inductance and capacitance of the contacts can represent a major problem, especially when testing high-impedance or high-frequency circuits. Although

several companies have marketed test sockets that reduce these problems, a socketed device will often not perform quite as well as a device soldered directly to a printed circuit board. Performance differences due to sockets are yet another potential source of correlation error and extended time to market.

1.6.4 Economics of Production Testing

Time is money, especially when it comes to production test programs. A high-performance tester may cost two million dollars or more, depending on its configuration. Probers and handlers may cost five hundred thousand dollars or more. If we also include the cost of providing floor space, electricity, and production personnel, it is easy to understand why testing is an expensive business.

One second of test time can cost a semiconductor manufacturer three to five cents. This may not seem expensive at first glance, but when test costs are multiplied by millions of devices a year the numbers add up quickly. For example, a five-second test program costing four cents per second times one million devices per quarter costs a company $800,000 per year in bottom-line profit. Testing is perhaps the fastest-growing portion of the cost of manufacturing a mixed-signal device. Continuous process improvements and better photolithography allow the design engineers to add more functions on a single semiconductor chip at little or no additional cost. Unfortunately, test time (especially data collection time) cannot be similarly reduced by simple photolithography. A 100-Hz sine wave takes 10 ms per cycle no matter how small we shrink a transistor. The only hope of salvation from photolithography is the addition of test features into the design itself that aid in the testing of the DUT.

Mainframe ATE equipment is designed to minimize test time and maximize overall product throughput. For example, many testers can be equipped with two test heads that share the mainframe instruments in a multiplexing fashion (Figure 1.21). The purpose of the second head is to allow the tester to simultaneously test a device on one head while a second handler or prober is moving and sorting devices on the other head. Dual-head testing is especially important when the handler index time (the time it takes to remove one DUT from the tester and insert the next one) is significant compared to the test time. When a handler or prober is docked to each test head, the tester can run almost continuously. Thus dual-head testing allows a more efficient use of the expensive tester hardware.

Another feature common in mainframe testers is multisite capability. Multisite testing is a process in which multiple devices are tested on the same test head simultaneously with obvious savings in test cost. The word "site" refers to each socketed DUT. For example, site 0 corresponds to the first DUT; site 1 corresponds to the second DUT, etc. Multisite testing is primarily a tester operating system feature, although duplicate tester instruments must be added to the tester to allow simultaneous testing on multiple DUT sites.

Clearly, production test economics is an extremely important issue in the field of mixed-signal test engineering. Not only must the test engineer perform accurate measurements of mixed-signal parameters, but the measurements must be performed as quickly as possible to reduce production costs. Since a mixed-signal test program may perform hundreds or even thousands of measurements on each DUT, each measurment must be performed in a small fraction of a second. The conflicting requirements of low test time and high accuracy will be a recurring theme throughout this book.

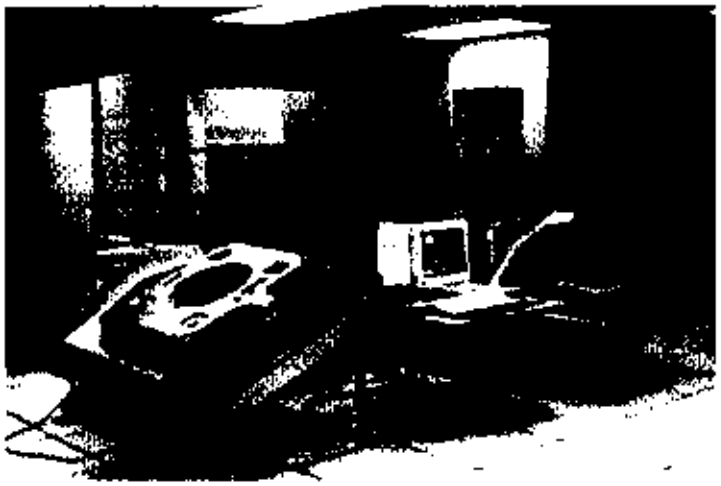

Figure 1.21. Teradyne A575 with dual test heads.

Problems

1.1. List four examples of analog circuits.

1.2. List four examples of mixed-signal circuits.

1.3. Questions 1.3–1.6 relate to the cellular telephone in Figure 1.2. Which type of mixed-signal circuit acts as a volume control for the cellular telephone earpiece?

1.4. Which type of mixed-signal circuit converts the speaker's voice into digital samples?

1.5. Which type of mixed-signal circuit converts incoming modulated voice data into digital samples?

1.6. Which type of digital circuit vocodes the speaker's voice samples before they are passed to the base-band interface?

1.7. When a PGA is combined with a digital logic block to keep a signal at a constant level, what is the combined circuit called?

1.8. Assume a particle of dust lands on a photomask during the photolithographic printing process of a metal layer. List at least one possible defect that might occur in the printed IC.

1.9. Why does the cleanliness of the air in a semiconductor fabrication area affect the number of defects in IC manufacturing?

1.10. List at least four production steps after wafers have been fabricated.

1.11. Why would it be improper to draw conclusions about a design based on characterization data from one or two devices?

1.12. List three main components of an ATE tester.

1.13. What is the purpose of a DIB board?

1.14. What type of equipment is used to handle wafers as they are tested by an ATE tester?

1.15. List three advantages of concurrent engineering.

1.16. What is the purpose of a test plan?

1.17. List at least four challenges faced by the mixed-signal test engineer.

1.18. Assume a test program runs on a tester that costs the company 3 cents per second to operate. This test cost includes tester depreciation, handler depreciation, electricity, floor space, personnel, etc. How much money can be saved per year by reducing a 5-s test program to 3.5 s, assuming 5 million devices per year are to be shipped. Assume that only 90% of devices tested are good, and that the average time to find a bad device drops to 0.5 s.

1.19. Assume the profit margin on the device in problem 1.18 is 20% (i.e., for each $1 worth of devices shipped to the customer, the company makes a profit of 20 cents). Assume the profits are taxed at 36%. How many dollars worth of product would have to be shipped to make an after-tax profit equal to the savings offered by the streamlined test program in Problem 1.18? If each device sells for $1.80, how many devices does this represent? Considering the fact that a dollar saved is an untaxed dollar earned, what obvious conclusion can we draw about the importance of test time reduction versus the importance of selling and shipping additional devices?

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CHAPTER 2

The Test Specification Process

2.1 Device Data Sheets

2.1.1 Purpose of a Data Sheet

Beginning test engineers often spend a great deal of time learning how to generate test plans for mixed-signal devices. A test plan is a written list of tests and test procedures that will be used to verify the quality of a particular device under test (DUT). The definition of a production test plan usually begins with a device *data sheet* or *specification sheet*, as it is often called. Unfortunately, the data sheet does not directly translate into a finite list of all required production tests. For example, a low-pass filter ripple specification of ±1.0 dB states that gain variation is guaranteed at each and every frequency in the passband of the filter. Of course, semiconductor manufacturers do not test every possible frequency in production. Test plan generation sometimes seems like more of an art than a science, especially when one tries to define exactly how a data sheet is translated into a test plan. Before exploring the art and science of mixed-signal test plan generation, let us look at the function and structure of a data sheet in detail.

The data sheet serves many purposes. When development of a new device begins, the data sheet serves as the design specification. Design engineers refer to the data sheet as a blueprint to make sure they design the functions that the marketing and systems engineering organizations have specified. As the project progresses, the test and product engineers refer to the data sheet to define the test list. The test list must be comprehensive enough to guarantee that the manufactured devices meet the data sheet specifications. Throughout the design process, the customer refers to the data sheet while designing the device into the system level end application. The data sheet thus serves as the formal communication channel between the marketing and engineering personnel engaged in a project.

The test engineer often detects data sheet mistakes and ambiguities while writing the test plan or developing the test program. In effect, the test engineer is the first customer for a new design. Likewise, the tester and device interface board (DIB) can be considered the new device's first application. Data sheet errors should be promptly corrected to prevent further mistakes. For instance, if an inappropriate measurement is specified in the initial data sheet, it is the test engineer's responsibility to make sure the error gets corrected or clarified so that a sensible test plan can be defined. For this reason it is important to know which organization is responsible for controlling the data sheet's contents.

The answer to the ownership question depends somewhat on the type of device being developed. There are two kinds of devices: catalog and custom. A catalog device is one that is defined by the semiconductor manufacturer or by an IC design house. Once defined, a catalog

device is offered to multiple customers for use in their end applications. A custom device, by contrast, is defined by a specific customer. It must meet that customer's exact requirements.

In the case of a catalog device, the systems engineering or marketing organization controls the data sheet. The test engineer only needs to get agreement from the design and systems engineers to make a data sheet change. In the case of a custom device, the customer and systems engineer share responsibility for the contents of the data sheet. In addition to approvals from the marketing or systems engineering team, the customer's approval is also required before the data sheet can be modified.

Depending on the customer's requirements, data sheet changes may be very easy to implement or they may be impossibly difficult. Regardless of the customer's needs, though, specification changes requested at the last minute give the appearance of a poorly run organization. For this reason, it is a good idea for the test engineer to get involved very early in the definition of a device so that specification changes can be suggested in a timely manner. Suggestions made early in the new product development cycle give a customer more confidence that the testing process is under control.

2.1.2 Structure of a Data Sheet

Data sheets may contain any of the following sections: a feature summary and description, principles of operation, absolute maximum ratings, electrical characteristics, timing diagrams, application information, characterization data, circuit schematic, and die layout. The sections that are most pertinent to test engineering are the device description, principles of operation, electrical characteristics, timing diagrams, and package/pinout information. Before we can understand the process by which the production test list is developed, we must first understand the purpose of each of these data sheet sections.

Figure 2.1 shows an example data sheet for a digital-to-analog converter (DAC). This data sheet is taken from a Texas Instruments data acquisition circuits data book.[1] The first page of the data sheet provides a quick device summary. The feature summary allows the customer to quickly gauge the device's fit to a particular application. The test engineer can generally ignore this section since the same information is typically called out in subsequent sections of the data sheet. The pinout and package information is much more relevant to test engineering. The test engineer refers to the pinout and package information to design the DIB for each package type.

The device description gives a quick overview of the device's functionality. Together with the principles of operation (Figure 2.2), the device description defines the various operations of the device in detail. The test program must guarantee all these functions, though not necessarily in a straightforward manner. For instance, the device description may depict a circuit that divides an externally generated 1-MHz reference clock by one million, producing a 1-s timebase. Since straightforward testing would represent an unacceptably long test time of 1 s, this function might be tested in an indirect manner.

There are many indirect ways to guarantee the operation of a 1-s timebase counter without spending 1 s of test time. For example, a special test mode might split the divider into two separate stages that each count to one thousand in only 1 ms. The two divider stages could then be tested simultaneously to guarantee the functionality of the whole. Total test time would be only 1 ms (plus overhead introduced by the tester). This is an example of a design for test (DfT) test mode. It serves no purpose in the system-level end application. The customer does not need

to split the divider into two halves and may not even need to know that it can be placed in this test mode at all. Therefore, test modes may or may not be documented in the data sheet.

TLC7524C, TLC7524E, TLC7524I
8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

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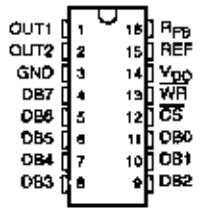
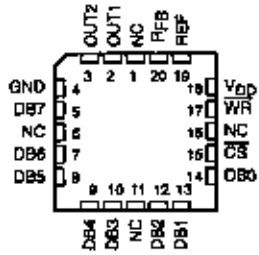
- Easily Interfaced to Microprocessors
- On-Chip Data Latches
- Monotonic Over the Entire A/D Conversion Range
- Segmented High-Order Bits Ensure Low-Glitch Output
- Interchangeable With Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524
- Fast Control Signaling for Digital Signal-Processor Applications Including Interface With TMS320
- CMOS Technology

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	1/2 LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Setting time	100 ns Max
Propagation delay time	80 ns Max

D OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TLC7524C, TLC7524E, and TLC7524I are CMOS, 8-bit, digital-to-analog converters (DACs) designed for easy interface to most popular microprocessors.

The devices are 8-bit, multiplying DACs with input latches and load cycles similar to the write cycles of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, which produce the highest glitch impulse. The devices provide accuracy to 1/2 LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 mW typically.

Featuring operation from a 5-V to 15-V single supply, these devices interface easily to most microprocessor buses or output ports. The 2- or 4-quadrant multiplying makes these devices an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC7524C is characterized for operation from 0°C to 70°C. The TLC7524I is characterized for operation from –25°C to 85°C. The TLC7524E is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGE		
	SMALL OUTLINE PLASTIC DIP (D)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC7524CD	TLC7524CFN	TLC7524CN
–25°C to 85°C	TLC7524ID	TLC7524IFN	TLC7524IN
–40°C to 85°C	TLC7524ED	TLC7524EFN	TLC7524EN

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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1

Figure 2.1. Data sheet for 8-bit multiplying DAC: features, description, and pinout.

TLC7524C, TLC7524E, TLC7524I
8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

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PRINCIPLES OF OPERATION

The TLC7524C, TLC7524E, and TLC7524I are 8-bit multiplying DACs consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary-weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded. These decoded bits, through a modification in the R-2R ladder, control three equally-weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 2. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source I/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 2. Analysis of the circuit for all digital inputs high is similar to Figure 2; however, in this case, I_{ref} would be switched to OUT1.

The DAC on these devices interfaces to a microprocessor through the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, analog output on these devices responds to the data activity on the DB0–DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0–DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

These devices are capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 3 and 4. Tables 1 and 2 summarize input coding for unipolar and bipolar operation respectively.

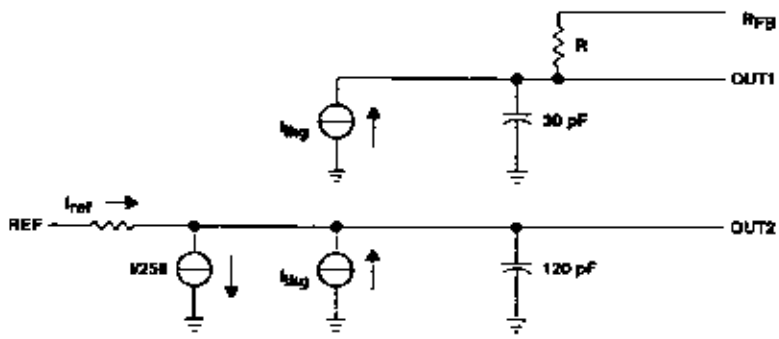

Figure 2. TLC7524 Equivalent Circuit With All Digital Inputs Low

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Figure 2.2. Eight-bit multiplying DAC: principles of operation.

Consider a second example of indirect testing which is more applicable to mixed-signal circuits. A data sheet states that a programmable gain amplifier (PGA) can be set to gains from 0 to 30 dB in 2-dB steps. It may or may not be necessary to test each and every gain step. If the PGA is designed with a binary weighted resistor structure, it might be possible to measure only four of the sixteen gain steps, corresponding to the four gain setting paths of the binary architecture. The other twelve gain steps might be calculated mathematically depending on the accuracy requirements of the test and the robustness of the design.

It is up to the test engineer and design engineer to work through all the required functionality in the principles of operation and determine what series of tests and test modes constitute an acceptable balance between test thoroughness and costly test time. The astute design engineer will make architectural decisions based not only on circuit performance but also on test efficiency. The experienced test engineer serves a critical role in helping to define what kinds of circuits can be most efficiently tested.

Many of the features listed in the device description and principles of operation do not result in measurements of electrical parameters. These features are verified using what is often referred to as a go/no-go test or functional test. Functional tests result in a simple pass/fail result with no numerical reading. Parametric tests, by comparison, are those that return a value that must be compared against one or more test limits to determine pass/fail results.

The 1-s timer is a good example of a circuit that can be tested with a functional test. It is not necessary to measure the exact countdown period in seconds and fractions of a second. The digital counter circuit either divides by one million or it does not. This type of digital logic verification is known as a *functional pattern test*.

The only way the 1-s period of time could be in error is if the divider circuits are not functional or if the 1-MHz external reference clock is not set to the correct frequency. An incorrect external frequency setting does not need to be tested during IC production, since it is not a function of device performance. Only a functional pattern test is required to guarantee the 1-s interval. An automated software process is often used to generate functional pattern tests. The test engineer should verify that all digital functionality has been guaranteed by either automatically generated patterns or by hand-coded functional pattern tests.

In highly customized mixed-signal devices, the test engineer needs to understand the end application of the device. Otherwise, the concurrent engineering process described in Chapter 1 will be impeded and the test engineer will not be able to contribute to the design definition and debug. The device description and principles of operation provide the test engineer with much of the information needed to understand the system into which the device will be placed.

2.1.3 Electrical Characteristics

Electrical characteristics (or electrical specifications) provide the test limits and test conditions for many of the parametric tests in a mixed-signal test program. Figures 2.3 and 2.4 show the electrical characteristics for the 8-bit multiplying DAC. While the format of the electrical characteristics section may vary widely from one manufacturer to another, there are some common features. There are generally parameter names to the left side of the chart, followed by test conditions. Often, a series of notes are listed below the electrical characteristics that give more complete background information for some of the specifications.

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recommended operating conditions

		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
CS setup time, $t_{su(CS)}$		40			40			ns
CS hold time, $t_{h(CS)}$		0			0			ns
Data bus input setup time, $t_{su(D)}$		25			25			ns
Data bus input hold time, $t_{h(D)}$		10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		40			40			ns
Operating free-air temperature, T_A	TLC7524C	0		70	0		70	°C
	TLC7524I	−25		85	−25		85	
	TLC7524E	−40		85	−40		85	

electrical characteristics over recommended operating free-air temperature range, V_{ref} = ±10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$			10			10	µA
I_{IL}	Low-level input current		V_I = 0			−10			−10	µA
I_{lkg}	Output leakage current	OUT1	DB0–DB7 at 0 V, $\overline{WR}$, $\overline{CS}$ at 0 V, V_{ref} = ±10 V			±400			±200	nA
		OUT2	DB0–DB7 at V_{DD}, $\overline{WR}$, $\overline{CS}$ at 0 V, V_{ref} = ±10 V			±400			±200	
I_{DD}	Supply current	Quiescent	DB0–DB7 at V_{IH}min or V_{IL}max			1			2	mA
		Standby	DB0–DB7 at 0 V or V_{DD}			500			500	µA
k_{SVS}	Supply voltage sensitivity, $\Delta gain/\Delta V_{DD}$		ΔV_{DD} = ±10%		0.01	0.16		0.005	0.04	%FSR/%
C_I	Input capacitance, DB0–DB7, $\overline{WR}$, $\overline{CS}$		V_I = 0			5			5	pF
C_o	Output capacitance	OUT1	DB0–DB7 at 0 V, $\overline{WR}$, $\overline{CS}$ at 0 V			30			30	pF
		OUT2				120			120	
		OUT1	DB0–DB7 at V_{DD}, $\overline{WR}$, $\overline{CS}$ at 0 V			120			120	
		OUT2				30			30	
	Reference input impedance (REF to GND)			5		20	5		20	kΩ

Figure 2.3. Recommended operating conditions and electrical characteristics.

TLC7524C, TLC7524E, TLC7524I
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operating characteristics over recommended operating free-air temperature range, V_{ref} = ±10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error				±0.5			±0.5	LSB
Gain error	See Note 1			±2.5			±2.5	LSB
Settling time (to 1/2 LSB)	See Note 2			100			100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80			80	ns
Feedthrough at OUT1 or OUT2	Vref = ±10 V (100-kHz sinewave) $\overline{WR}$ and $\overline{CS}$ at 0 V, DB0–DB7 at 0 V			0.5			0.5	%FSR
Temperature coefficient of gain	T_A = 25°C to MAX		±0.004			±0.001		%FSR/°C

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal full scale range (FSR) = V_{ref} – 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0 – DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

operating sequence

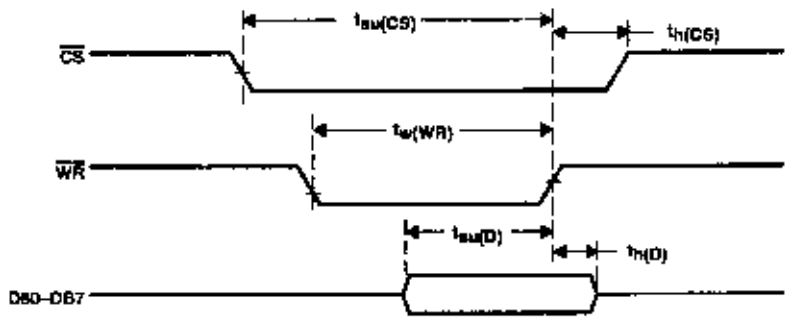

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Figure 2.4. Electrical specifications and timing diagram.

In the example in Figure 2.4, Note 1 states that the "Gain error is measured using the internal feedback resistor..." This piece of information is vital, since the gain error specification is ambiguous without it. Data sheet ambiguities can lead to frustrating correlation efforts. For instance, if Note 1 was missing, the test engineer might use the internal resistor to measure gain error while the customer uses an external resistor. The two engineers might waste days trying to agree upon the correct value of gain error for a particular group of DUTs. Unfortunately, the data sheet seldom lists all possible test conditions for each measurement in complete detail. The test plan must fill in the gaps as needed. The test engineer should also suggest that clarifications be added to the data sheet wherever serious ambiguities might cause the customer problems at a later time.

On the right side of the electrical specification table are the test limits. These are divided into three categories: MIN, TYP, and MAX. The MIN column and MAX column represent the minimum and maximum values allowed for a passing device. These may or may not all be tested in production on every single device. Nevertheless, all specifications should be tested in an extended characterization version of the test program. The extended test program verifies that the device design meets all of the specifications listed in the electrical characteristics section of the data sheet.

The TYP column represents the typical reading expected from a good device. If a TYP value is specified at all, it is often just the average of the MIN and MAX test limits. The production test program does not generally guarantee the TYP value. For example, it is not necessary to verify that the average reading for a large number of tested devices is equal to the TYP value. Since the TYP value has no guaranteed correlation to the devices tested, it has much less value to the customer than the guaranteed MIN and MAX specifications.

The TYP column is sometimes used to specify parameters that are guaranteed by design and/or process. For example, an 8-bit DAC has 8 bits of resolution by definition. Resolution is sometimes listed as a typical specification, but only as a means of formally communicating the number of DAC input bits. The TYP column is also used to list characterization data for parameters that are difficult or impossible to measure in a cost-effective manner. For example, input capacitance is often listed as a typical specification because it is largely dominated by the design layout and by the device package. In cases such as this, characterization data can be collected from many devices to prove that the parameter never fails and therefore does not need to be tested in production.

Sometimes the data sheet lists a parameter with a note stating that it is "guaranteed, not tested" or "guaranteed by design." This is a formal way to notify the customer that this specification has been characterized and shown to be good by design, and is therefore not tested in production. However, the lack of such a notice should not be taken as a guarantee that the parameter is tested in production. Most data books contain a notification that parameters may or may not be tested in production, but that they are nevertheless guaranteed by the manufacturer to meet minimum and maximum specifications.

In addition to electrical characteristics, Figure 2.4 also shows the timing diagram for the example 8-bit DAC. Timing diagrams are critical to test program development. The digital patterns used in mixed-signal tests are sometimes generated manually due to frequency synchronization issues that will become more apparent in subsequent chapters. At present there are few if any good automation schemes that allow the design engineer to specify mixed-signal tests in a way that allows automatic translation into a debugged test program. The mixed-signal

test generation process is still largely manual. Thus timing diagrams are still very pertinent to mixed-signal test engineers.

Application information is often added to the data sheet to aid the customer in designing the end application. Figure 2.5 shows the application diagram for the example 8-bit DAC. This particular application diagram shows the customer how to use the DAC in voltage mode rather than current mode. Application information is often very helpful to the test engineer, as well as the customer. Often the application information helps the test engineer understand the intended application for the device or helps in designing a thorough test list. Application information can also be helpful in the design of circuitry located on the automated test equipment's device interface board (DIB).

Figure 2.6 shows a functional block diagram for the example DAC. The functional block diagram is extremely important on complex devices since it provides a top-level representation of all the device functions in a single diagram. Like the application information section, the functional block diagram helps the customer (and the test engineer) understand the overall functionality of a complex mixed-signal device. Figure 2.6 also shows the absolute maximum and recommended operating conditions for the example 8-bit DAC. Absolute maximum ratings are not intended for production testing. These are specified limits beyond which device damage may occur. The recommended operating conditions, by contrast, list production test conditions such as minimum and maximum supply voltage under which all test limits must be met. The recommended operating conditions are therefore quite important to the test engineer, since they define the permutations of test conditions under which all the specifications must be met.

Figure 2.7 shows characterization data for a low-offset JFET op amp. Characterization data may or may not be included in a data sheet. If it is included, it does not necessarily represent guaranteed data. It is analogous to the TYP data column and is not necessarily guaranteed by the production test program. Certain characterization plots such as statistical histograms may be collected using the production tester simply because it is the easiest way to generate the data. However, characterization plots are more often generated using bench equipment such as oscilloscopes and spectrum analyzers.

2.2 Generating the Test Plan

2.2.1 To Plan or Not to Plan

Strictly speaking, test plans are not absolutely necessary. A test engineer can certainly generate a test program by simply sitting down at the tester computer and entering code based on the device data sheet. There are several problems with this type of undisciplined approach. First, device testability will probably not be identified early enough to allow the addition of test features to the design. Test plans force the design engineers and test engineers to work through all the details of testing at an early stage in the design cycle. Second, the test engineer may create test-to-test compatibility problems if the details of all tests are not known up front. For example, a clocking scheme that works well for one test may be incompatible with the clocking scheme required for a subsequent test. The first test may then need to be rewritten from scratch so that the clocking schemes mesh properly.

If a test plan is not clearly documented before coding begins, then the test engineer lacks the necessary overview of the test program that allows all the tests to fit together efficiently.

APPLICATION INFORMATION

voltage-mode operation

It is possible to operate the current-multiplying DAC in these devices in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output terminal. The analog output voltage is then available at the reference voltage terminal. Figure 1 is an example of a current-multiplying DAC, which is operated in voltage mode.

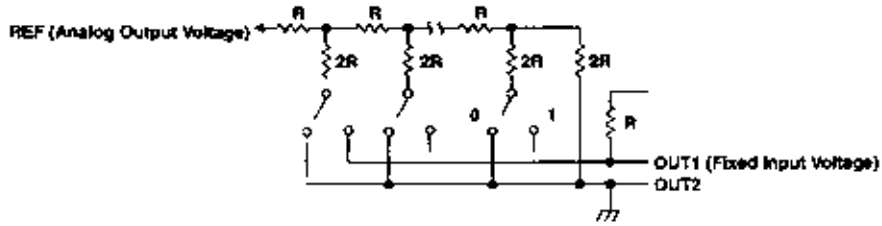

Figure 1. Voltage Mode Operation

The relationship between the fixed-input voltage and the analog-output voltage is given by the following equation:

$$V_O = V_I (D/256)$$

where

V_O = analog output voltage
V_I = fixed input voltage
D = digital input code converted to decimal

In voltage-mode operation, these devices meet the following specification:

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Linearity error at REF	V_{DD} = 5 V, OUT1 = 2.5 V, OUT2 at GND, T_A = 25°C		1	LSB

Figure 2.5. Eight-bit multiplying DAC: application information.

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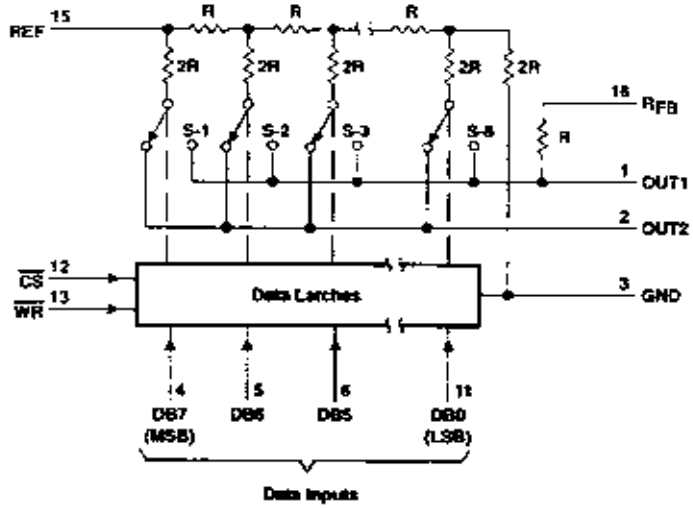
functional block diagram



Terminal numbers shown are for the D or N package

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{DD}		−0.3 V to 16.5 V
Digital input voltage range, V_I		−0.3 V to V_{DD} + 0.3 V
Reference voltage, V_{ref}		±25 V
Peak digital input current, I_I		10 μA
Operating free-air temperature range, T_A:	TLC7524C	0°C to 70°C
	TLC7524I	−25°C to 85°C
	TLC7524E	−40°C to 85°C
Storage temperature range, T_{stg}		−65°C to 150°C
Case temperature for 10 seconds, T_C: FN package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260°C

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Figure 2.6. Eight-bit multiplying DAC: functional block diagram and absolute maximum ratings.

TL05x, TL05xA, TL05xY
ENHANCED-JFET LOW-OFFSET
OPERATIONAL AMPLIFIERS
SLOS171 – FEBRUARY 1997

TYPICAL CHARACTERISTICS

TL051
EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

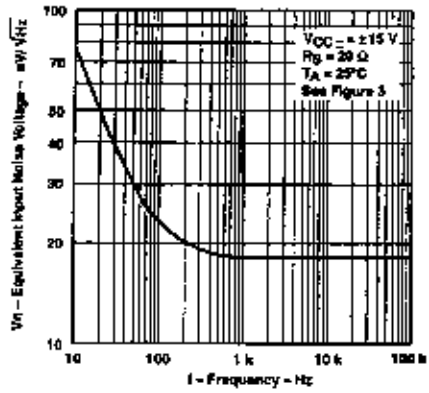

Figure 51

TL052 AND TL054
EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

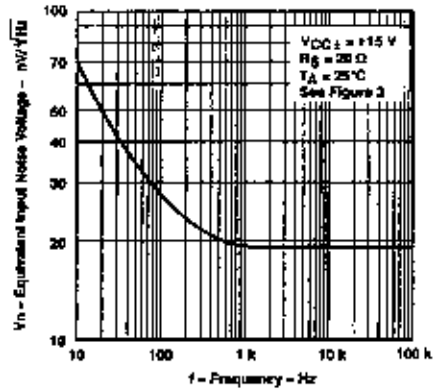

Figure 52

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

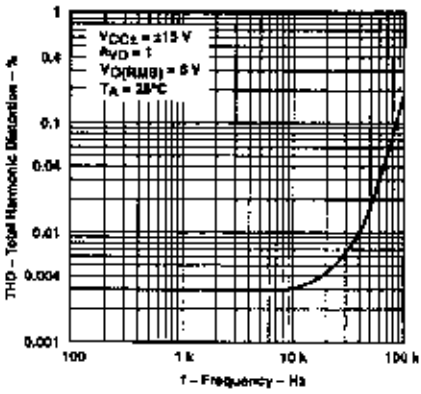

Figure 53

TL051
UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

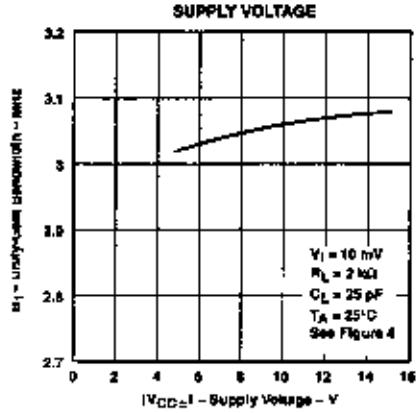

Figure 54

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Figure 2.7. Low-offset JFET op amp: characterization data.

Similarly, test hardware such as DIBs and probe interface hardware cannot be properly designed until all test details are known. Finally, the test plan helps to identify shortfalls in the target tester's capabilities. Early identification of tester deficiencies allows the test engineer time to find acceptable work-arounds. Sometimes, the design engineer can even modify the IC design to accommodate tester deficiencies. This is another example of design for test (DfT).

2.2.2 Structure of a Test Plan

The structure of a mixed-signal test plan varies from one engineer to the next and from company to company. Since test plans are not generally published outside a company, they tend to be less formal and less structured than device data sheets. The primary purpose of a test plan is to serve as a roadmap for the test engineer while the test program is being generated. However, it is also used as the official communication channel between test engineers, design engineers, product engineers, and even customers. Depending on the needs and tastes of the person or organization generating a test plan, it might include any of a number of sections. The following are some suggestions for a well-written test plan.

A thorough test plan includes device background information that cannot be found in the data sheet. For example, a device may have test modes that are not documented in the data sheet. The test plan is an ideal place to list all test modes and how they are utilized. The test plan is also a good place to explain special test requirements that relate to the end application of the device. For example, a data sheet might list a parameter called error vector magnitude that is documented more completely in a separate telecommunication standard. It is a good idea to explain some of the details of a test like this so that a new engineer does not have to spend hours researching the purpose and meaning of the test.

When reading another person's test program, it can sometimes be difficult to understand why a particular test is being performed. A test plan should explain the purpose of each test and how it relates to a data sheet specification. It should also explain any assumptions the test engineer is making about a particular test. For example, an amplifier's absolute gain may be specified from 0 to 10 kHz. If the test engineer plans to test absolute gain at only three frequencies, then the test plan should explain why those frequencies were chosen. Was it an arbitrary choice, or does it relate to expected weaknesses in the design? It should also answer other questions: What was the input signal level? What typical level is expected from the output of the device? Are other tests like signal-to-noise ratio tested at the same time as absolute gain?

Another very useful addition to a test plan is hardware setup diagrams for each test. A hardware diagram can include as much or as little detail as needed to explain the test. If too much detail is included, then the diagram becomes too cluttered to clearly explain the test conditions. It would probably be unnecessary, for example, to show the full schematic for an op amp gain stage having a gain of 10. It would be perfectly acceptable to simply draw a triangular buffer with the label "x10 gain." Likewise, it is unnecessary to draw an entire 256-pin DUT if only three pins of the DUT are relevant to a given test.

Consider the simple diagram in Figure 2.8, showing a test diagram for a DAC full-scale output test. This diagram looks simple, but it may actually represent a test for a small portion of a much more complicated device. Since most of the other pins of the DUT are irrelevant during this test, they can be eliminated from the diagram for clarity. Simplified block diagrams such as this are often more useful in test plan diagrams than fully detailed schematic representations. Another way to eliminate clutter is to document default conditions. Default conditions such as

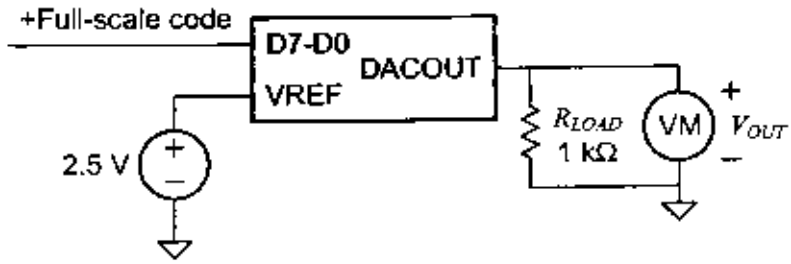


Figure 2.8. Test plan hardware setup diagram.

nominal power supply settings and nominal digital timing can be documented in a "defaults" section at the beginning of the test plan. Unless otherwise specified, these defaults are assumed to apply to all remaining test descriptions.

Test descriptions should be documented in a tester-independent manner if possible. This makes it easier for all engineering team members to understand the purpose of the test and how it should ideally be implemented. If the test plan describes each test in a tester-independent manner, it also makes it easier to convert test programs from one tester to another. Tester-specific information such as digitizer sampling rates and meter range settings can be added to the test plan, but they should perhaps be set aside in a separate subsection after the generic tester-independent description.

2.2.3 Design Specifications versus Production Test Specifications

Since the data sheet is initially used as a design specification, it may contain parameters that either cannot be tested or do not need to be tested in production. These internal specifications are meant for the design engineers only, and should probably be removed from the final data sheet. Consider a very simple example of an on-chip resistor specification of 100 kΩ plus or minus 10%. A resistance test would normally be performed by forcing current across the resistor, measuring the voltage drop, and applying Ohm's law to calculate resistance. However, if the resistor is permanently connected into the feedback path of an op amp gain stage, then resistance may not be directly measurable.

Beginning test engineers sometimes agonize over how to measure an internal parameter such as this without realizing that it is only an internal design specification. Such parameters do not necessarily need to be tested in production. The experienced test engineer knows to verify with the design engineer whether or not the specification is a design specification or a production specification. If it is indeed a production specification and the test engineer has no access to measure the parameter, then something must be done to make the parameter measurable. A design for test (DfT) structure might be added to the design early in the design cycle to allow the necessary test access.

In the on-chip resistor example the resistance and its tolerance is specified only to remind the design engineer of the requirements necessary to support another parameter such as absolute gain. Absolute gain of a simple op amp inverting gain stage is the result of several parameters including two resistance values. The op amp gain stage will probably require an absolute gain specification, which can be measured directly without pulling the resistor out of the gain circuit. If absolute gain performance is the driving force behind the resistance specification, there is no

reason to measure the resistance values in production. Measuring the important parameter, absolute gain in this example, is sufficient. No DfT structure would be required to test the resistors' values in production.

2.2.4 Converting the Data Sheet into a Test Plan

One of the most difficult things to teach a new test engineer is how to convert a data sheet into a corresponding test plan. The difficulty arises from the infinite permutations of possible tests implied by the data sheet. Unlike many digital devices, mixed-signal circuits have an obnoxious habit of interacting with one another in unexpected ways. For example, the signal-to-noise ratio of an amplifier may change depending on the operating mode of a completely separate digital circuit on the opposite side of the die.

This effect may worsen with varying power supply voltage setting, die temperature, etc. How does a test engineer know which operating modes should be tested when there are so many possible permutations of test conditions? Obviously, the production test program must consist of a small subset of possible test conditions but it is difficult to define the pruning process in a scientific manner. There is really no fixed series of steps that can reliably convert a data sheet into a test plan. Nevertheless, a few suggestions are listed in the following paragraphs as a starting point.

For each sentence in the device description and principles of operation, make sure a test is defined that guarantees the device can perform the described operation. For example, if the description states that a DAC can operate in either of two digital interface modes, make sure there is a test that verifies both interface modes. Perhaps the DAC has to be tested in both modes, or perhaps the DAC can be tested in only one mode and a much faster digital test can be executed to verify the other mode. These details must be discussed with the design engineers and systems engineers.

The central function of a mixed-signal test program is the measurement of each of the electrical specifications listed in the device data sheet. For each electrical parameter, make sure that a test is defined to measure the parameter in all modes of operation. For example, a DAC might have a particular linearity specification, but it may operate in two different modes with three different voltage ranges and two possible power supply voltages.

Unfortunately, the permutations of possible test conditions will often grow to an unrealistic test list. If the permutations of modes and test conditions are too large, then discuss the problem with the design engineers and try to identify which permutations are likely to cause the most problems. These so-called *worst-case conditions* are commonly used to prune an infinite test list down to a more manageable subset of critical tests.

Each electrical specification should raise a series of questions. If the device includes internal control registers, how should they be set during each test? What loading should be applied to the output pins of the device? Should an external voltage reference be supplied to the device or should an internal voltage reference be enabled? Can the device drive the capacitive load presented by the tester instruments or will a voltage follower need to be added to the device interface hardware? Are there important electrical specifications that have not been included in the data sheet? Asking detailed questions like this can save the test engineer many headaches later in the project.

In the early stages of device development, some parameters may be listed as TBD (to be determined). Make sure that the innocent-looking TBD placeholder for a simple DC offset test does not become an unexpected nightmare like "offset = 1 pV MAX" at the last minute. There is a huge difference in test methodology between a 100-mV DC offset test and 1-pV offset test. Asking for rough estimates of expected performance is a good idea, even if the exact specification is not known.

After considering all these questions, a limited set of tests must be specified. In the end, it may be impossible to predict what modes of operation represent worst-case test conditions. To be safe, the test engineer usually specifies as many permutations as is reasonable. The initial test program has to be written so that the test list and test conditions can be easily modified. In this manner, worst-case conditions can be determined through empirical characterization of the device performance. After thorough characterization of many lots of production devices, the test list can be pruned down to an optimum set of tests that most efficiently probe the DUT's weaknesses.

2.3 Components of a Test Program

2.3.1 Test Program Structure

The test program is a detailed, tester-specific version of the test plan, written in the target tester's native language. It may at times deviate from the test plan if the target tester is incapable of performing tests exactly as specified by the test plan. In these cases, comments should be added to the program to make this discrepancy clear. Major deviations should be approved by the other members of the engineering team.

Tester languages vary from low-level C routines to very sophisticated graphical user interface environments. Despite wide differences in their details, tester languages often share some basic structural components. Test programs typically consist of all or most of the following sections: waveform creation and other tester initializations, calibrations, continuity, DC parametric tests, AC parametric tests, digital patterns (also known as *functional tests*), digital timing tests, test sequence control, test limits, and binning control.

Well-written test programs often contain extensive characterization code to perform tests not specifically required by the data sheet. These characterization tests allow the design engineers to better evaluate the quality and robustness of the IC design. A thorough test program may also contain code that allows offline simulation of the tests so that certain portions of the program can be debugged without a tester or device. Let us take a more detailed look at some of the structural components commonly found in a mixed-signal test program.

2.3.2 Test Code and Digital Patterns

Test code and digital patterns make up the bulk of mixed-signal test programs. Test code controls the order and timing of instrument settings, signal generation, and signal measurements that make up each measurement in the test program. Test code typically does not control the real-time details of each instrument, though.

For example, the data generated from the digital subsystem of a tester are not clocked out one bit at a time by the test code. Instead, the test code simply calls for the tester's digital subsystem

to begin exercising the desired digital pattern at the appropriate time. The digital subsystem then takes care of the details of generating the individual ones and zeros. Thus the test code for a DAC full-scale output test might look something like this in pseudocode:

```
dac_full_scale_voltage( )
{
        set VH = 2.5 V; /* Set the DAC's voltage reference to 2.5 volts */
        start digital pattern = "dac_full_scale"; /* Set the DAC output to +full scale (2.5 V) */
        connect meter: DAC_OUT /* Connect the DAC voltmeter to the DAC output */
        fsout = read_meter( ); /* Read the voltage level at the DAC_OUT pin */
        test fsout; /* Compare the DAC full scale output to the data sheet limits */
}
```

Digital patterns consist of groups of data bits called *vectors*. Each vector represents the drive and expect data that are to be sent out on each of the tester's digital pins at a specific time. Drive data specifies the desired state at the input to the DUT (HI, LOW, or HIZ). Compare data (also called *expect data*) specifies the required digital output from the device. Vectors are usually sent out at a regular rate, called the *bit cell rate*. Digital patterns usually contain not only the 1/0 drive and expect data, but also the sequencing information for the vectors. The digital pattern sequencing commands allow branching, looping, and other vector sequencing operations that make the pattern more compact. To generate a pair of clocks at two different frequencies from digital pins CLK1 and CLK2, one might write the following pseudocode pattern:

```
label       pattern control   CLK1  CLK2
-------------------------------------------
START                         0     0 /* Vector one */
                              1     0 /* Vector two, etc. */
                              0     1
            Jump START        1     1 /* Infinite loop */
```

This pattern would continue in an infinite loop, producing two frequencies. The CLK1 frequency would be twice that of the CLK2 frequency.

The test code and the digital pattern must operate in stepped synchronization for mixed-signal tests. It would be unfortunate in the DAC test above if the digital pattern "dac_full_scale" did not execute until 50 ms after the meter measurement had already been performed. For this reason, mixed-signal testers include handshaking functions in both the test code and digital pattern control that allow the tester computer and digital pattern subsystem to keep in step with one another.

Another pattern issue unique to mixed-signal testing is that the pattern often must be executed at a very precise frequency. It is not acceptable to round off the period of the vector rate to the nearest nanosecond as is often done in purely digital test programs. The reason for this will become more apparent in Chapters 6 and 7, "Sampling Theory" and "DSP-Based Testing."

2.3.3 Binning

One of the functions of a test program is to sort each device into one of several categories, called *bins*, depending on the outcome of the various tests. The most obvious bins are "pass" and "fail," but there are several others that might be added. For example, a continuity test is usually inserted at the beginning of the test program.

The purpose of the continuity test is to verify that all the electrical contacts between the tester and the DUT have been successfully connected. If a large percentage of devices fail the continuity test, this indicates a probable error in the tester hardware. It is therefore a good idea to use separate bins for continuity failures and data sheet failures so that the production staff can more easily recognize tester hardware problems.

Binning is not always a pass/fail operation. Sometimes there are different grades of passing devices. If a device is designed to operate at 100 MHz but some of the manufactured devices are actually able to operate at 120 MHz, then the test program might be set up to split these devices into two quality grades, "good" and "great." Bin 1 might represent the 120-MHz devices, while Bin 2 might represent the devices that could only operate up to 100 MHz. The-120 MHz devices would be labeled differently than the 100-MHz devices. They would also be priced differently, of course. We are all familiar with higher prices for faster PC microprocessors and memory chips.

Fast binning is a term used to describe a tester's ability to bin a bad device as soon as it fails any test. This is done to prevent a bad device from wasting valuable tester time after it has already produced a failing result. The test and product engineers should work together to ensure that the most commonly failed tests are placed near the beginning of the test program. This allows the tester to sort bad devices as quickly as possible.

The tester generates a binning signal that tells the handler or prober what to do with the various categories of devices. Until recent years, bad die on a wafer were often squirted with red ink dots to designate them as failures. Now this inking is commonly performed offline or is done in a purely virtual manner using pass/fail databases and production lot ID numbers. At final test, different grades of packaged devices are sorted into separate plastic tubes or trays by the handler.

2.3.4 Test Sequence Control

Test sequence may be controlled in a number of ways, depending on the sophistication of the tester's software environment. In older testers, the order of the various tests was simply determined by the order of test routine execution. Comparisons of measured results against test limits were performed after each measurement. Test limits were therefore scattered all through the test program along with the instrument setups and measurement code. Such a scattered arrangement made it difficult to identify which test limits were applied to a device in a given version of the test program. This made it difficult to verify that the test program limits matched the data sheet limits.

As tester software environments matured, a new type of test code module evolved to allow a more convenient summary of test flow, test limits, and binning information. The new code module, called a *sequencer* by some vendors, contains the test routine function calls, the test limits, and the binning information for each test result. The sequencer code allows the programmer to order the tests and group all the test limits into a central location in the test code,

separate from the test routines themselves. The sequencer code thus provides a convenient summary of the test list, test order, and pass/fail limits for each test. This makes it easier to audit the program for compliance with data sheet test limits. Depending on the tester's software environment, the sequencer modules may be coded as text or they may consist of graphical interface objects linked together with arrows to indicate program flow and binning decisions.

2.3.5 Waveform Calculations and Other Initializations

Mixed-signal test programs use many precomputed waveforms. A 1-kHz gain test requires a sinusoidal waveform that does not change from one program execution to the next. Waveforms that do not need to change are precomputed and stored either in arrays or directly into memory banks in the tester instruments themselves. Digital waveforms are also precomputed and stored in the digital subsystem of the tester. Many of the required initializations such as waveform computations are performed only once when the test program is first loaded. Performing these initializations only once saves a large amount of test execution time.

Other operations, such as resetting tester instruments to a default state, must be performed each time the program is run. The details of initializations are very specific to each tester, but most testers involve some type of first-run initialization code. One major class of first-run code is focused calibrations and checkers.

2.3.6 Focused Calibrations and DIB Checkers

Sometimes the instrumentation in a tester does not have sufficient accuracy for a given test. If not, a special routine called a *focused calibration* is required when the program first runs. The focused calibration routine determines the inaccuracy of the instrument using slower, more accurate instrumentation as a reference. The inaccuracies of the faster instrument can then be corrected in a process known as *software calibration*.

Software calibrations must also be performed on circuitry placed on the device interface board. Assume an op amp voltage follower is placed on the DIB to buffer a weak device output. The gain and offset of the voltage follower adds errors into any measured results. The test engineer must calibrate the gain and offset of the voltage follower using focused calibrations to achieve maximum accuracy. Sometimes focused calibrations can be as difficult to develop as the device measurements themselves, especially when extreme accuracy is required in the final test result.

Fortunately, many software calibrations are hidden from the user in the tester's operating system. These calibrations are performed automatically when the program is first loaded. Other calibrations are performed on a regular basis, such as once per week. Software calibration is discussed in greater detail in Chapter 10, "Focused Calibrations."

Electromechanical relays, op amp circuits, comparators, and other active circuits are commonly placed on the DIB to extend the tester's functionality and accuracy. These circuits are subject to failure. The test program should include DIB checker code to verify the functionality of any circuitry placed on the device interface board. This allows production personnel to avoid running thousands of good devices through a bad DIB before discovering the error. DIB checker routines are usually run along with focused calibrations when the program is first loaded.

2.3.7 Characterization Code

Characterization tests are often added to a test program to allow thorough evaluation of the first few lots of production material. Thorough characterization of a new device is critical, since it allows the design engineers to identify and correct the marginal portions of the design. An example of a characterization test would be a filter response test implemented at each frequency from 100 Hz to 10 kHz in 100-Hz increments. Such a test would never be cost-effective in a production test program, but it would provide thorough information about the filter's gain versus frequency characteristics.

2.3.8 Simulation Code

Simulation code is sometimes added to a mixed-signal test program to allow some of the mathematical routines to be verified. For example, the ideal output of a DAC might be simulated and stored into an array for use by a DAC linearity calculation routine. Offline code debugging techniques like this are a good way to reduce debug time and avoid wasting valuable tester time. However, such simulations are not entirely effective in uncovering errors such as incorrect DUT register settings or improper tester instrument range settings.

A more advanced type of simulation, known as *test simulation* or *virtual test* allows true closed-loop simulation of the tester and device. Using test simulation, a software model of the tester stimulates a model of the DUT according to the instructions in the test program. The tester model and tester operating system then capture the responses from the DUT model and compare them to test limits. Test simulation is explained in more detail in Chapter 16, "Test Economics."

2.3.9 "Debuggability"

It is said that the three most important things in real estate are location, location, and location. It might be said of test program structure that the three most important things are debuggability, debuggability, and debuggability (despite the fact that "debuggability" is not a real word). A study at Texas Instruments showed that the test program debugging process takes about 20% of an average test engineer's week. The debugging time was found to be roughly twice the time spent writing test code.

Debugging is not only a matter of finding and fixing test code bugs. It is also a matter of locating measurement correlation errors, intermittent failures, and hardware problems including bad DIB layout and broken tester modules. More important, test debugging often turns into design debugging.

Design debugging activities account for a large portion of the test program debugging time. One of a mixed-signal test engineer's most valuable roles is to help the design engineers isolate design problems. A good test engineer with a well-structured test program can quickly modify the program and run experiments for design engineers or customers. These experiments are critical to reducing the time it takes to get the problems worked out of a new mixed-signal design. The success or failure of a mixed-signal product often depends on how well the design engineers, test engineers, and product engineers work together to resolve design problems.

2.4 Summary

In this chapter, we have reviewed the basic structure of a data sheet, and we have seen how tabular entries and comments in a data sheet translate first into a test plan and then into a test program. The translation is not a simple one-to-one process, with each data sheet entry corresponding to one clearly defined test. Rather, the process requires a great deal of thought, experience, and common sense to guarantee the intent of the data sheet specifications without literally performing millions of possible tests in a production test program.

In Chapter 3, we will begin looking at the test development process, starting with the definitions of some of the most basic tests in a mixed-signal test program, the analog DC tests. Since these tests require very simple hardware and software, we will study DC tests first to gain some familiarity with the language and methodology of analog and mixed-signal testing. Our study of true mixed-signal tests, involving a mixture of analog and digital signals, will be delayed until later chapters so that we can first develop a fundamental understanding of issues such as accuracy and repeatability.

Problems

2.1. (a) List at least three purposes of a data sheet. (b) List at least six types of information that can be found in a data sheet. (c) In which section of the data sheet are the maximum, minimum, and typical specification limits listed?

2.2. What is a test plan? Is there a rigorous method to convert any given data sheet into a test plan? Do the electrical characteristics listed in the tables of a data sheet correspond one-to-one with individual DUT measurements?

2.3. Do the absolute maximum ratings need to be verified during production testing?

2.4. Problems 2.4–2.8 refer to the TLC7524C data sheet in Figures 2.1–2.6. What output load resistance should be attached to the DAC output (OUT1) during the settling time test? What capacitance should be attached in parallel with the load resistance?

2.5. What is the ideal relationship between the output voltage and the input voltage and digital input code when the DAC is operated in voltage mode?

2.6. What state must be applied to the $\overline{\text{WR}}$ and $\overline{\text{CS}}$ signals to allow the DAC output voltage to change according to the data at DB0-DB7? If the $\overline{\text{CS}}$ signal is high and the $\overline{\text{WR}}$ signal is low, what will happen to the DAC output when the data signals DB0-DB7 change from 00000000 to 11111111?

2.7. When the TLC7524C is packaged in the FN package, what device signal is attached to pin 16? What signal is attached to pin 9? What pin is connected to the positive power supply?

2.8. When the TLC7524C is powered with a 5-V supply, what is the maximum power dissipated by the device? If a TLC7524C draws 1.5 mA from the V_{DD} supply, would it pass the power dissipation specification?

2.9. At what frequency does the total harmonic distortion for a TL051 JFET op amp exceed 0.004%? Is the distortion at this frequency guaranteed to be less than 0.004% on every device?

2.10. Can a DUT's specifications be measured under all possible test conditions?

2.11. Which section of a test program tells the handler or prober whether a device is good or bad?

2.12. What is the purpose of the DIB checker section of a test program?

2.13. What is the purpose of focused calibrations?

References

1. Data Book, *Data Acquisition Circuits - Data Conversion and DSP Analog Interfaces*, Texas Instruments, Inc., P.O. Box 809066, Dallas, TX 75380-9066

CHAPTER 3

DC and Parametric Measurements

3.1 Continuity

3.1.1 Purpose of Continuity Testing

Before a test program can evaluate the quality of a device under test (DUT), the DUT must be connected to the ATE tester using a test fixture such as a device interface board (DIB). A typical interconnection scheme is shown in Figure 3.1. When packaged devices are tested, a socket or handler contactor assembly provides the contact between the DUT and the DIB. When testing a bare die on a wafer, the contact is made through the probe needles of a probe card. The tester's instruments are connected to the DIB through one or more layers of connectors such as spring-loaded pogo pins or edge connectors. The exact connection scheme varies from tester to tester, depending on the mechanical/electrical performance tradeoffs made by the ATE vendor.

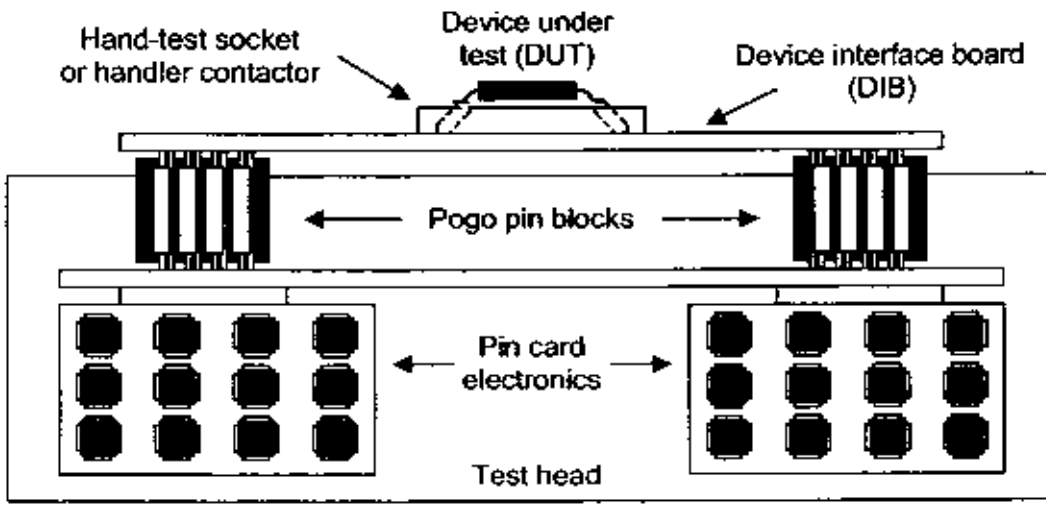


Figure 3.1. ATE test head to DUT interconnections.

In addition to pogo pins and other connectors, electromechanical relays are often used to route signals from the tester electronics to the DUT. A relay is an electrical switch whose position is controlled by an electromagnetic field. The field is created by a current forced through a coil of wire inside the relay (Figure 3.2). Relays are used extensively in mixed-signal testing to modify the electrical connections to and from the DUT as the test program progresses from test to test.

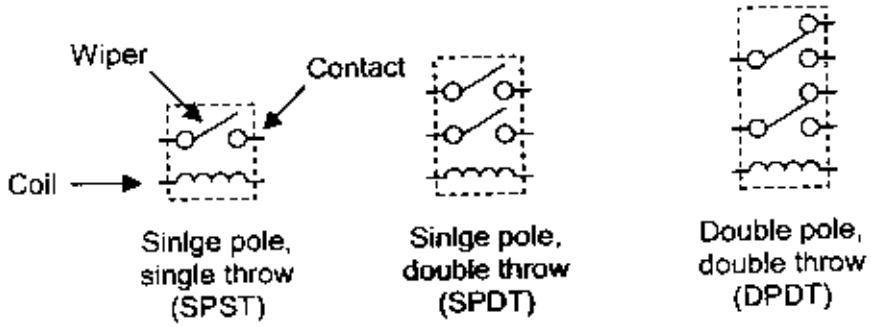


Figure 3.2. Electromechanical relays.

Any of the electrical connections between a DUT and the tester can be defective, resulting in open circuits or shorts between electrical signals. For example, the wiper of a relay can become stuck in either the open or closed position after millions of open/close cycles. While interconnect problems may not pose a serious problem in a lab environment, defective connections can be a major source of tester down time on the production floor. Continuity tests (also known as *contact tests*) are performed on a device to verify that all the electrical connections are sound. If continuity testing is not performed, then the production floor personnel cannot distinguish between bad lots of silicon and defective test hardware connections. Without continuity testing, thousands of good devices could be rejected simply because a pogo pin was bent or because a relay was defective.

3.1.2 Continuity Test Technique

Continuity testing is usually performed by detecting the presence of on-chip protection circuits. These circuits protect each input and output of the device from electrostatic discharge (ESD) and other excessive voltage conditions. The ESD protection circuits prevent the input and output pins from exceeding a small voltage above or below the power supply voltage or ground. Diodes and silicon-controlled rectifiers (SCRs) can be used to short the excess currents from the protected pin to ground or to a power terminal.

An ESD protection diode conducts the excess ESD current to ground or power any time the pin's voltage exceeds one diode drop above (or below) the power or ground voltage. SCRs are similar to ESD protection diodes, but they are triggered by a separate detection circuit. Any of a variety of detection circuits can be used to trigger the SCR when the protected pin's voltage exceeds a safe voltage range. Once triggered, an SCR behaves like a forward-biased diode from the protected pin to power or ground (Figure 3.3). The SCR remains in its triggered state until the excessive voltage is removed. Since an SCR behaves much like a diode when triggered, the term "protection diode" is used to describe ESD protection circuits whether they employ a simple diode or a more elaborate SCR structure. We will use the term "protection diode" throughout the remainder of this book with the understanding that a more complex circuit may actually be employed.

DUT pins may be configured with either one or two protection diodes, connected as shown in Figure 3.4. Notice that the diodes are reverse-biased when the device is powered up, assuming normal input and output voltage levels. This effectively makes them "invisible" to the DUT circuits during normal operation.

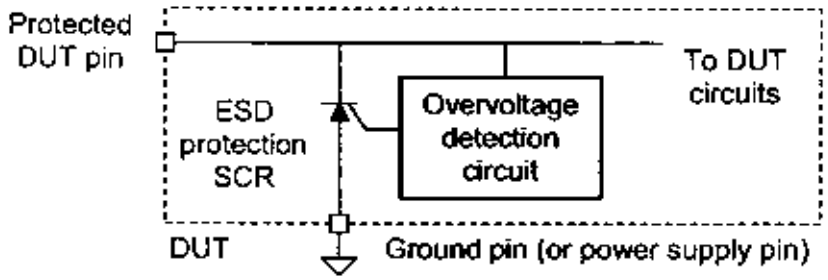


Figure 3.3. SCR-based ESD protection circuit.

To verify that each pin can be connected to the tester without electrical shorts or open circuits, the ATE tester forces a small current across each protection diode in the forward-biased direction. The DUT's power supply pins are set to zero volts to disable all on-chip circuits and to connect the far end of each diode to ground. ESD protection diodes connected to the positive supply are tested by forcing a current I_{CONT} into the pin as shown in Figure 3.5 and measuring the voltage, V_{CONT}, that appears at the pin with respect to ground. If the tester does not see the expected diode drops on each pin, then the continuity test fails and the device is not tested further. Protection diodes connected to the negative supply or ground are tested by reversing the direction of the forced current.

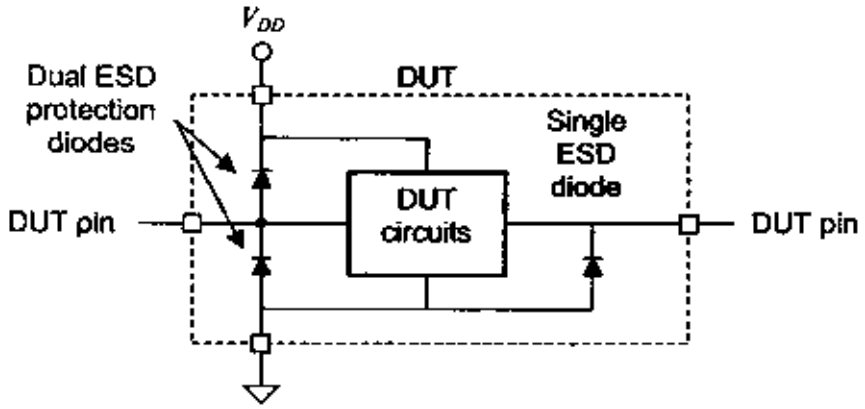


Figure 3.4. Dual and single protection diodes.

In the case of an SCR-based protection circuit, the current source initially sees an open circuit. Because the current source output tries to force current into an open circuit, its output voltage rises rapidly. The rising voltage soon triggers the SCR's detection circuit. Once triggered, the SCR accepts current from the current source and the voltage returns to one diode drop above ground. Thus the difference between a diode-based ESD protection circuit and an SCR-based circuit is hardly noticeable during a continuity test.

The amount of current chosen is typically between 100 μA and 1 mA, but the ideal value depends on the characteristics of the protection diodes. Too much current may damage the diodes, while too little current may not fully bias them. The voltage drop across a good protection diode usually measures between 550 and 750 mV. For the purpose of illustration, we shall assume that a conducting diode has voltage drop of 0.7 V. A dead short to ground will

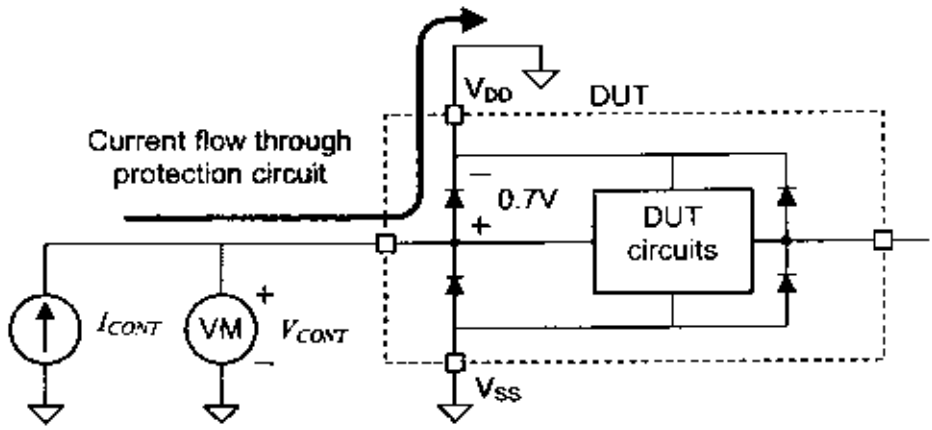


Figure 3.5. Checking the continuity of the diode connected to the positive supply. The other diode is tested by reversing the direction of the forced current.

result in a reading of 0 V, while an open circuit will cause the tester's current source to reach a programmed clamp voltage.

Many mixed-signal devices have multiple power supply and ground pins. Continuity to these power and ground connections may or may not be testable. If all supply pins or all ground pins are not properly connected to ground, then continuity to some or all of the nonsupply pins will fail. However, if only some of the supply or ground pins are not grounded, the others will provide a continuity path to zero volts. Therefore, the unconnected power supply or ground pins may not be detected. One way to test the power and ground pins individually is to connect them to ground one at a time, using relays to break the connections to the other power and ground pins. Continuity to the power or ground pin can then be verified by looking for the protection diode between it and another DUT pin.

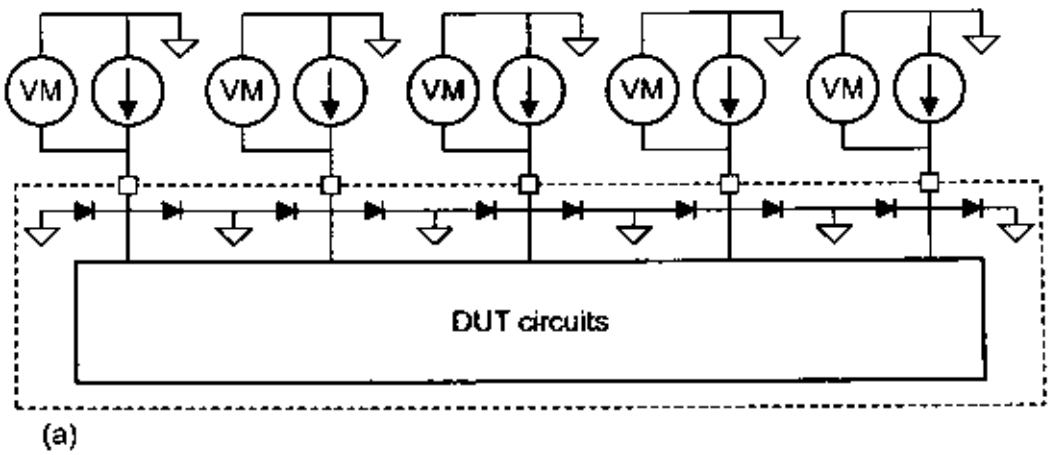
Occasionally, a device pin may not include any protection diodes at all. Continuity to these unprotected pins must be verified by an alternative method, perhaps by detecting a small amount of current leaking into the pin or by detecting the presence of an on-chip component such as a capacitor or resistor. Since unprotected pins are highly vulnerable to ESD damage, they are used only in special cases.

One such example is a high-frequency input requiring very low parasitic capacitance. The space-charge layer in a reverse-biased protection diode might add several picofarads of parasitic capacitance to a device pin. Since even a small amount of stray capacitance presents a low impedance to very high-frequency signals, the protection diode must sometimes be omitted to enhance electrical performance of the DUT.

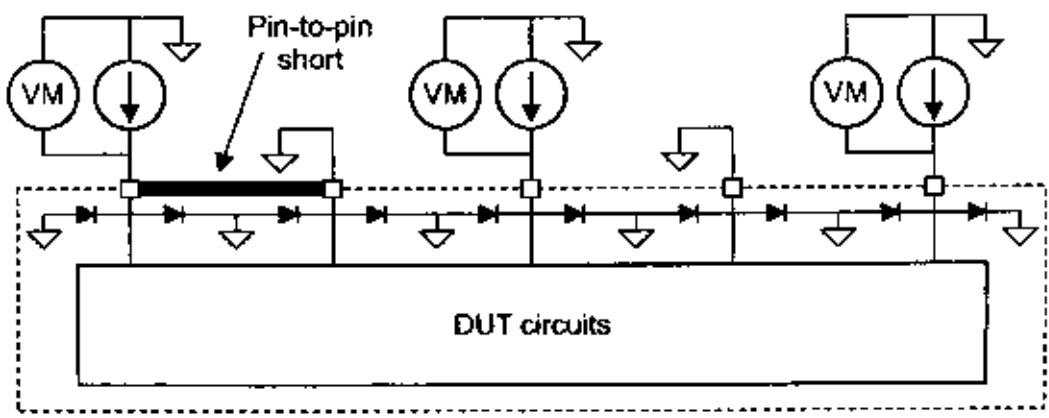
3.1.3 Serial versus Parallel Continuity Testing

Continuity can be tested one pin at a time, an approach known as *serial continuity testing*. Unfortunately, serial testing is a time-consuming and costly approach. Modern ATE testers are capable of measuring continuity on all or most pins in parallel rather than measuring the protection diode drops one at a time. These testers accomplish parallel testing using so-called *per-pin measurement instruments* as shown in Figure 3.6(a).

Clearly it is more economical to test all pins at once using many current sources and voltage meters. Unfortunately, there are a few potential problems to consider. First, a fully parallel test of pins may not detect pin-to-pin shorts. If two device pins are shorted together for some reason, the net current through each diode does not change. Twice as much current is forced through the parallel combination of two diodes. The shorted circuit configuration will therefore result in the expected voltage drop across each diode, resulting in both pins passing the continuity test. Obviously, the problem can be solved by performing a continuity test on each pin in a serial manner at the cost of extra test time. However, a more economical approach is to test every other pin for continuity on one test pass while grounding the remaining pins. Then the remaining pins can be tested during a second pass while the previously tested pins are grounded. Shorts between adjacent pins would be detected using this dual-pass approach, as illustrated in Figure 3.6(b).



(a)



(b)

Figure 3.6. Parallel continuity testing: (a) full parallel testing with possible adjacent fault masking; (b) minimizing potential adjacent fault masking by exciting every second pin.

A second, subtler problem with parallel continuity testing is related to analog measurement performance. Both analog pins and digital pins must be tested for continuity. On some testers the per-pin continuity test circuitry is limited to digital pins only. The analog pins of the tester

may not include per-pin continuity measurement capability. On these testers, continuity testing on analog pins can be performed one pin at a time using a single current source and voltmeter. These two instruments can be connected to each device pin one at a time to measure protection diode drops. Of course, this is a very time-consuming serial test method, which should be avoided if possible.

Alternatively, the analog pins can be connected to the per-pin measurement electronics of digital pins. This allows completely parallel testing of continuity. Unfortunately, the digital per-pin electronics may inject noise into sensitive analog signals. Also, the signal trace connecting the DUT to the per-pin continuity electronics adds a complex capacitive and inductive load to the analog pin, which may be unacceptable. The signal trace can also behave as a parasitic radio antenna into which unwanted signals can couple into analog inputs. Clearly, full parallel testing of analog pins should be treated with care. One solution to the noise and parasitic loading problems is to isolate each analog pin from its per-pin continuity circuit using a relay. This complicates the DIB design but gives high performance with minimal test time. Of course, a tester having per-pin continuity measurement circuits on both analog and digital pins represents a superior solution.

3.2 Leakage Currents

3.2.1 Purpose of Leakage Testing

Each input pin and output pin of a DUT exhibits a phenomenon called *leakage*. When a voltage is applied to a high-impedance analog or digital input pin, a small amount of current will typically leak into or out of the pin. This current is called *leakage current*, or simply *leakage*. Leakage can also be measured on output pins that are placed into a nondriving high-impedance mode. A good design and manufacturing process should result in very low leakage currents. Typically the leakage is less than 1 μA, although this can vary from one device design to the next.

One of the main reasons to measure leakage is to detect improperly processed integrated circuits. Leakage can be caused by many physical defects such as metal filaments and particulate matter that forms shorts and leakage paths between layers in the IC. Another reason to measure leakage is that excessive leakage currents can cause improper operation of the customer's end application. Leakage currents can cause DC offsets and other parametric shifts. A third reason to test leakage is that excessive leakage currents can indicate a poorly processed device that initially appears to be functional but which eventually fails after a few days or weeks in the customer's product.[1] This type of early failure is known as *infant mortality*.

3.2.2 Leakage Test Technique

Leakage is measured by simply forcing a DC voltage on the input or output pin of the device under test and measuring the small current flowing into or out of the pin. Unless otherwise specified in the data sheet, leakage is typically measured twice. It is measured once with an input voltage near the positive power supply voltage and again with the input near ground (or negative supply). These two currents are referred to as I_{IH} (input current, logic high) and I_{IL} (input current, logic low), respectively.

Digital inputs are typically tested at the valid input threshold voltages, V_{IH} and V_{IL}. Analog input leakage is typically tested at specific voltage levels listed in the data sheet. If no particular input voltage is specified, then the leakage specification applies to the entire allowable input voltage range. Since leakage is usually highest at one or both input voltage extremes, it is often measured at the maximum and minimum allowable input voltages. Output leakage (I_{OZ}) is measured in a manner similar to input leakage, though the output pin must be placed into a high-impedance (HIZ) state using a test mode or other control mechanism.

3.2.3 Serial versus Parallel Leakage Testing

Leakage, like continuity, can be tested one pin at a time (serial testing) or all pins at once (parallel testing). Since leakage currents can flow from one pin to another, serial testing is superior to parallel testing from a defect detection perspective. However, from a test time perspective, parallel testing is desired. As in continuity testing, a compromise can be achieved by testing every other pin in a dual-pass approach.

Continuity tests are usually implemented by forcing DC current and measuring voltage. By contrast, leakage tests are implemented by forcing DC voltage and measuring current. Since the tests are similar in nature, tester vendors generally design both capabilities into the per-pin measurement circuits of the ATE tester's pin cards. Analog leakage, like analog continuity, is often measured using the per-pin resources of digital pin cards. Again, a tester with per-pin continuity measurement circuits on both analog and digital pins represents a superior solution, assuming the extra per-pin circuits are not prohibitively expensive.

3.3 Power Supply Currents

3.3.1 Importance of Supply Current Tests

One of the fastest ways to detect a device with catastrophic defects is to measure the amount of current it draws from each of its power supplies. Many gross defects such as those illustrated in Figures 1.5–1.8 result in a low-impedance path from one of the power supplies to ground. Supply currents are often tested near the beginning of a test program to screen out completely defective devices quickly and cost effectively.

Of course, the main reason to measure power supply current is to guarantee limited power consumption in the customer's end application. Supply current is an important electrical parameter for the customer who needs to design a system that consumes as little power as possible. Low power consumption is especially important to manufacturers of battery operated equipment like cellular telephones. Even devices that draw large amounts of current by design should draw only as much power as necessary. Therefore, power supply current tests are performed on most if not all devices.

3.3.2 Test Techniques

Most ATE testers are able to measure the current flowing from each voltage source connected to the DUT. Supply currents are therefore very easy to measure in most cases. The power supply is simply set to the desired voltage and the current from its output is measured using one of the tester's ammeters.

When measuring supply currents, the only difficulties arise out of ambiguities in the data sheet. For example, are the analog outputs loaded or unloaded during the supply current test? Is digital block XYZ operating in mode A, mode B, or idle mode? In general, it is safe to assume that the supply currents are to be tested under worst-case conditions.

The test engineer should work with the design engineers to attempt to specify the test conditions that are likely to result in worst-case test conditions. These test conditions should be spelled out clearly in the test plan so that everyone understands the exact conditions used during production testing. Often the actual worst-case conditions are not known until the device has been thoroughly characterized. In these cases, the test program and test plan have to be updated to reflect the characterized worst-case conditions.

Supply currents are often specified under several test conditions, such as power-down mode, standby mode, and normal operational mode. In addition, the digital supply currents are specified separately from the analog supply currents. I_{DD} (CMOS) and I_{CC} (bipolar) are commonly used designations for supply current. I_{DDA}, I_{DDD}, I_{CCA}, and I_{CCD} are the terms used when analog and digital supplies are measured separately.

Many devices have multiple power supply pins that are connected to a common power supply in normal operation. Design engineers often need to know how much current is flowing into each individual power supply pin. Sometimes the test engineer can accommodate this requirement by connecting each power supply pin to its own supply. Other times there are too many DUT supply pins to provide each with its own separate power supply. In these cases, relays can be used to temporarily connect a dedicated power supply to the pin under test.

Another problem that can plague power supply current tests is settling time. The supply current flowing into a DUT must settle to a stable value before it can be measured. The tester and DIB circuits must also settle to a stable value. This normally takes 5–10 ms in normal modes of DUT operation. But in power-down modes, the specified supply current is often less than 100 µA. Since the DIB usually includes bypass capacitors for the DUT, each capacitor must be allowed to charge until the average current into or out of the capacitor is stable.

The charging process can take hundreds of milliseconds if the current must stabilize within microamps. Some types of bypass capacitors may even exhibit leakage current greater than the current to be measured. A typical solution to this problem is to connect only a small bypass capacitor (say 0.1 µF) directly to the DUT and then connect a larger capacitor (say 10 µF) through a relay as shown in Figure 3.7. The large bypass capacitor can be disconnected temporarily while the power-down current is measured.

3.4 DC References and Regulators

3.1.1 Voltage Regulators

A voltage regulator is one of the most basic analog circuits. The function of a voltage regulator is to provide a well-specified and constant output voltage level from a poorly specified and sometimes fluctuating input voltage. The output of the voltage regulator would then be used as the supply voltage for other circuits in the system. Figure 3.8 illustrates the conversion of a 6- to 12-V ranging power supply to a fixed 5-V output level.

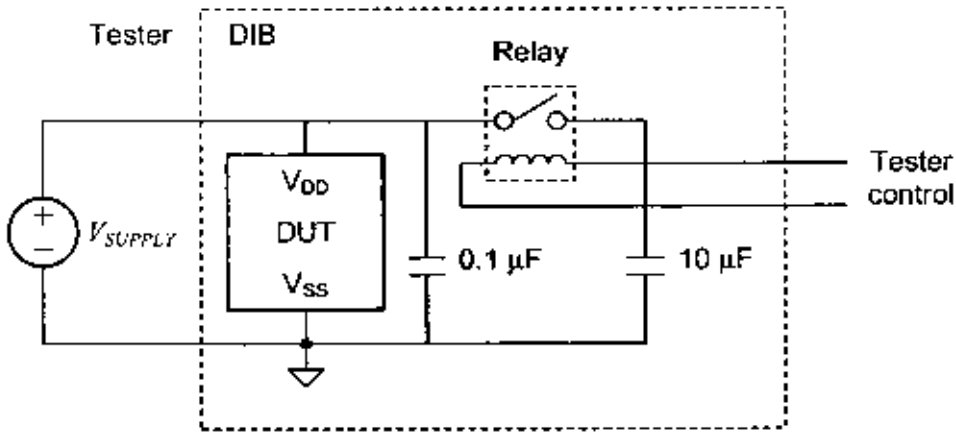


Figure 3.7. Arranging different-sized bypass capacitors to minimize power supply current settling behavior.

Voltage regulators can be tested using a fairly small number of DC tests. Some of the important parameters for a regulator are output no-load voltage, output voltage or load regulation, input or line regulation, input or ripple rejection, and dropout voltage.

Output no-load voltage is measured by simply connecting a voltmeter to the regulator output with no load current and measuring the output voltage V_O.

Load regulation measures the ability of the regulator to maintain the specified output voltage V_O under different load current conditions I_L. As the output voltage changes with increasing load current, one defines the output voltage regulation as the percentage change in the output voltage (relative to the ideal output voltage, $V_{O\text{-}NOM}$) for a specified change in the load current. Load regulation is measured under minimum input voltage conditions

$$\text{load regulation} \equiv 100\% \times \left. \frac{\Delta V_O}{V_{O\text{-}NOM}} \right|_{\max\{\Delta I_L\},\ \text{minimum } V_I} \tag{3.1}$$

The largest load current change, $\max\{\Delta I_L\}$, is created by varying the load current from the minimum rated load current (typically 0 mA) to the maximum rated load current.

Load regulation is sometimes specified as the absolute change in voltage, ΔV_O, rather than as a percentage change in V_O. The test definition will be obvious from the specification units (i.e. volts or percentage).

Line regulation or *input regulation* measures the ability of the regulator to maintain a steady output voltage over a range of input voltages. Line regulation is specified as the percentage change in the output voltage as the input line voltage changes over its largest allowable range. Like the load regulation test, line regulation is sometimes specified as an absolute voltage change rather than a percentage. Line regulation is measured under maximum load conditions

$$\text{line regulation} \equiv 100\% \times \left. \frac{\Delta V_O}{V_{O\text{-}NOM}} \right|_{\max\{\Delta V_I\},\ \text{maximum } I_L} \tag{3.2}$$

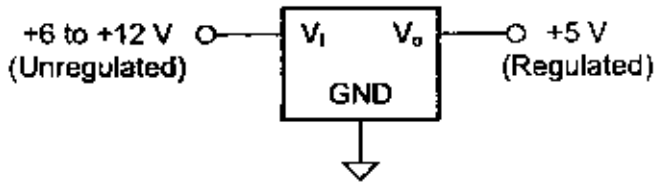


Figure 3.8. 5-V DC voltage regulator.

For the regulator shown in Figure 3.8, with the appropriate load connected to the regulator output, the line regulation would be computed by first setting the input voltage to 6 V, measuring the output voltage, then readjusting the input voltage to 12 V, and again measuring the output voltage to calculate ΔV_O. The line regulation would then be computed using Eq. (3.2).

Input rejection or *ripple rejection* is the ratio of the maximum input voltage variation to the output voltage swing, measured at a particular frequency (commonly 120 Hz) or a range of frequencies. It is a measure of the circuit's ability to reject periodic fluctuations of rectified AC voltage signals applied to the input of the regulator. Input rejection can also be measured at DC using the input voltage range and output voltage swing measured during the line regulation test.

Dropout voltage is the lowest voltage that can be applied between the input and output pins without causing the output to drop below its specified minimum output voltage level. Dropout voltage is tested under maximum current loading conditions. It is possible to search for the exact dropout voltage by adjusting the input voltage until the output reaches its minimum acceptable voltage, but this is a time-consuming test method. In production testing, the input can simply be set to the specified dropout voltage plus the minimum acceptable output voltage. The output is then measured to guarantee that it is equal to or above the minimum acceptable output voltage.

Exercises

3.1. The output of a 5-V voltage regulator varies from 5.10 V under no-load condition to 4.85 V under a 5 mA maximum rated load current. What is its load regulation?

Ans. 250 mV or 5%.

3.2. The output of a 5-V voltage regulator varies from 5.05 to 4.95 V when the input voltage is changed from 14 to 6 V under a maximum load condition of 10 mA. What is its line regulation?

Ans. 100 mV or 2%.

3.3. A 9-V voltage regulator is rated to have a load regulation of 3% for a maximum load current of 15 mA. Assuming a no-load output voltage of 9 V, what is the worst-case output voltage at the maximum load current?

Ans. 8.73 V.

3.4.2 Voltage References

Voltage regulators are commonly used to supply a steady voltage while also supplying a relatively large amount of current. However, many of the DC voltages used in a mixed-signal device do not draw a large amount of current. For example, a 1-V DAC reference does not need to supply 500 mA of current. For this reason, low-power voltage references are often incorporated into mixed-signal devices rather than high-power voltage regulators.

The output of on-chip voltage references may or may not be accessible from the external pins of a DUT. It is common for the test engineer to request a set of test modes so that reference voltages can be measured during production testing. This allows the test program to evaluate the quality of the DC references even if they have no explicit specifications in the data sheet. The design and test engineers can then determine whether failures in the more complicated AC tests may be due to a simple DC voltage error in the reference circuits. DC reference test modes also allow the test program to trim the internal DC references for more precise device operation.

3.4.3 Trimmable References

Many high-performance mixed-signal devices require reference voltages that are trimmed to very exact levels by the ATE tester. DC voltage trimming can be accomplished in a variety of ways. The most common way is to use a programmable reference circuit that can be permanently adjusted to the desired level. One such arrangement is shown in Figure 3.9. The desired level is programmed using fuses, or a nonvolatile digital control mechanism such as EEPROM or flash memory bits. Fuses are blown by forcing a controlled current across each fuse that causes it to vaporize. Fuses can be constructed from either metal or polysilicon. If EEPROM or flash memory is added to a mixed-signal device, then this technology may offer a superior alternative to blown fuses, as EEPROM bits can be rewritten if necessary.

There are various algorithms for finding the digital value that minimizes reference voltage error. In the more advanced trimming architectures such as the one in Figure 3.9, the reference can be experimentally adjusted using a bypass trim value rather than permanently blowing the

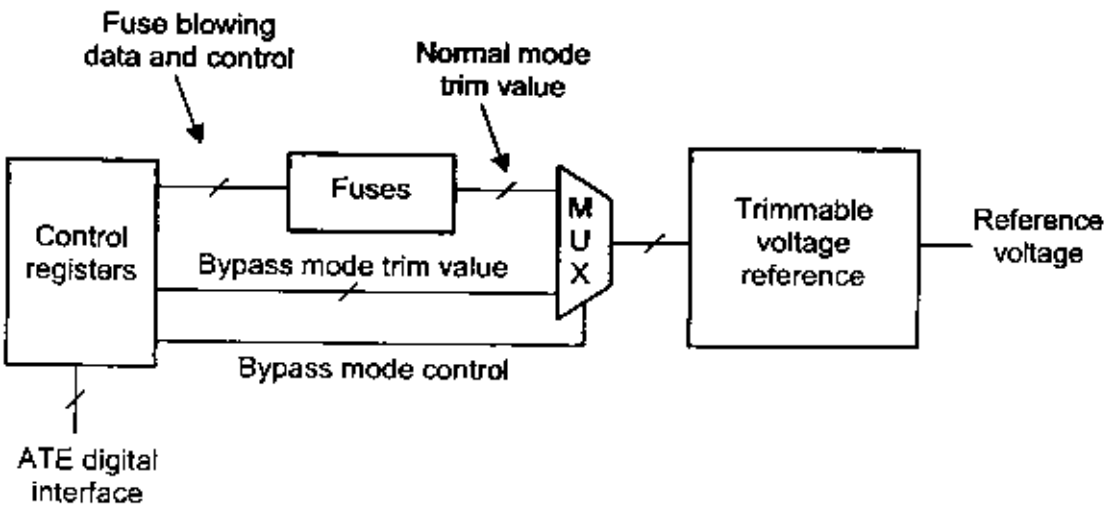


Figure 3.9. Trimmable reference circuit.

fuses. In this example, the bypass trim value is enabled using a special test mode control signal, bypass mode control. Once the best trim value has been determined by experimental trials, the fuses are permanently blown to set the desired trim value. Then, during normal operation, the bypass trim value is disabled and the programmed fuses are used to control the voltage reference.

Trimming can also be accomplished using a laser trimming technique. In this technique, a laser is used to cut through a portion of an on-chip resistor to increase its resistance to the desired value. The resistance value in turn adjusts the DC level of the voltage reference. The laser trimming technique can also be used to trim gains and offsets of analog circuits. Laser trimming is more complex than trimming with fuses or nonvolatile memory. It requires special production equipment linked to the ATE tester.

Laser trimming must be performed while the silicon wafer is still exposed to open air during the probing process. Since metal fuses can produce a conductive sputter when they vaporize, they too are usually trimmed during the wafer probing process. By contrast, polysilicon fuses and EEPROM bits can be blown either before or after the device is packaged.

There is an important advantage to trimming DC levels after the device has been packaged. When plastic is injected around the silicon die, it can place slight mechanical forces on the die. This in turn introduces DC offsets. Because of these DC shifts, a device that was correctly trimmed during the wafer probing process may not remain correctly trimmed after it has been encapsulated in plastic. Another potential DC shift problem relates to the photoelectric effect. Since light shining on a bare die introduces photoelectric DC offsets, a bare die must be trimmed in total darkness. Of course, wafer probers are designed with this requirement in mind. They include a black hood or other mechanism to shield bare die from light sources.

3.5 Impedance Measurements

3.5.1 Input Impedance

Input impedance (Z_{IN}), also referred to as *input resistance*, is a common specification for analog inputs. In general, impedance refers to the behavior of both resistive and reactive (capacitive or inductive) components in the circuit. As the discussion in this chapter is restricted to DC, inductors and capacitors have zero reactance, and as such, make no contribution to impedance. Hence, impedance and resistance refer to the same quantity at DC.

Input impedance is a fairly simple measurement to make. If the input voltage is a linear function of the input current (i.e., if it behaves according to Ohm's law), then one simply forces a

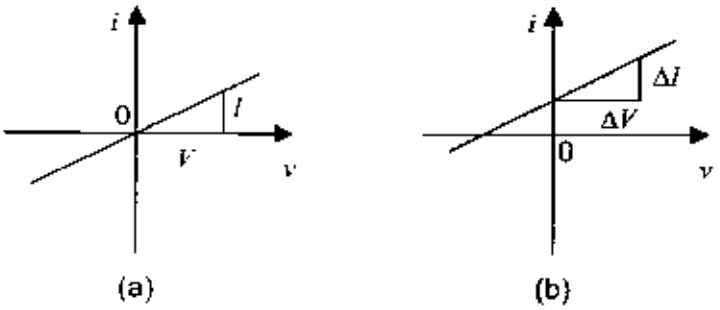


Figure 3.10. Input i–v characteristic curves for (a) linear impedance and (b) nonlinear impedance.

voltage V and measures a current I, or vice versa, and computes the input im
to

$$Z_{IN} = \frac{V}{I}$$

Figure 3.10(a) illustrates the input i-v relationship of a device satisfying Ohm
that the i-v characteristic is a straight line passing through the origin with a
In many instances, the i-v characteristic of an input pin is a straight line
through the origin as shown in Figure 3.10(b). Such situations typically
considerations where the input terminal of a device is biased by a constant cu
that shown in Figure 3.11 or the input impedance is terminated with an unkn
other than ground.

In cases such as these, one cannot use Eq. (3.3) to compute the input impe
lead correctly to the slope of the i-v characteristic. Instead, one measures the
current (ΔI) that results from a change in the input voltage (ΔV) and
impedance using

$$Z_{IN} = \frac{\Delta V}{\Delta I}$$

If the input impedance is so low that it would cause excessive currents t
another approach is needed. The alternative method is to force two con
measure the resulting voltage difference. This is often referred to as a *for*
voltage method. Input impedance is again calculated using Eq. (3.4).

ple 3.1

In the input impedance test setup shown in Figure 3.11, voltage source SR
current flowing into the pin is measured at 0.055 mA. Then SRC1 is set
current is measured again at 0.021 mA. What is the input impedance?

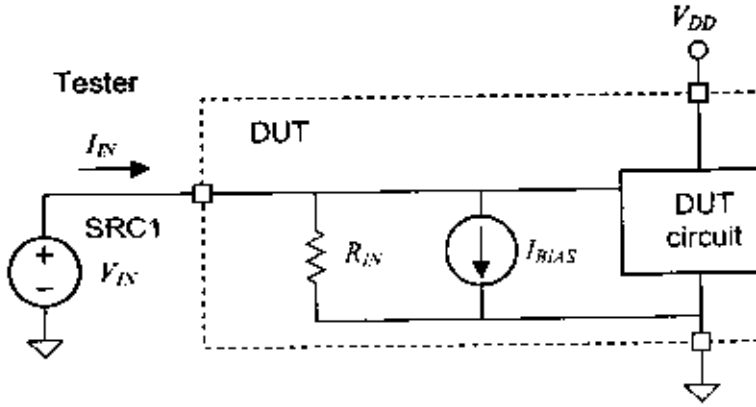


Figure 3.11. Input impedance test setup.

voltage V and measures a current I, or vice versa, and computes the input impedance according to

$$Z_{IN} = \frac{V}{I} \tag{3.3}$$

Figure 3.10(a) illustrates the input i-v relationship of a device satisfying Ohm's law. Here we see that the i-v characteristic is a straight line passing through the origin with a slope equal to Z_{IN}^{-1}. In many instances, the i-v characteristic of an input pin is a straight line but does not pass through the origin as shown in Figure 3.10(b). Such situations typically arise from biasing considerations where the input terminal of a device is biased by a constant current source such as that shown in Figure 3.11 or the input impedance is terminated with an unknown voltage source other than ground.

In cases such as these, one cannot use Eq. (3.3) to compute the input impedance, as it will not lead correctly to the slope of the i-v characteristic. Instead, one measures the change in the input current (ΔI) that results from a change in the input voltage (ΔV) and computes the input impedance using

$$Z_{IN} = \frac{\Delta V}{\Delta I} \tag{3.4}$$

If the input impedance is so low that it would cause excessive currents to flow into the pin, another approach is needed. The alternative method is to force two controlled currents and measure the resulting voltage difference. This is often referred to as a *force-current/measure-voltage* method. Input impedance is again calculated using Eq. (3.4).

Example 3.1

In the input impedance test setup shown in Figure 3.11, voltage source SRC1 is set to 2 V and current flowing into the pin is measured at 0.055 mA. Then SRC1 is set to 1 V and the input current is measured again at 0.021 mA. What is the input impedance?

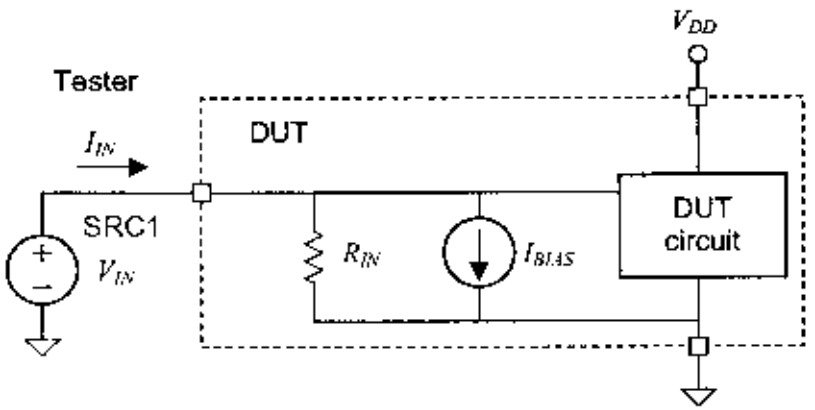


Figure 3.11. Input impedance test setup.

Solution:

Input impedance, Z_{IN}, which is a combination of R_{IN} and the input impedance of the block labeled "DUT Circuit," is calculated using Eq. (3.4) as follows

$$Z_{IN} = \frac{2\text{ V} - 1\text{ V}}{0.055\text{ mA} - 0.021\text{ mA}} = 29.41\text{ k}\Omega$$

Note that the impedance could also have been measured by forcing 0.050 and 0.020 mA and measuring the voltage difference. However, the unpredictable value of I_{BIAS} could cause the input voltage to swing beyond the DUT's supply rails. For this reason, the forced-current measurement technique is reserved for low values of resistance.

In Example 3.1, the values of the excitation consisting of 2 and 1 V are somewhat irrelevant. We could just as easily have used 2.25 and 1.75 V. However, the larger the difference in voltage, the easier it is to make an accurate measurement of current change. This is true throughout many types of tests. Large changes in voltages and currents are easier to measure than small ones. The test engineer should beware of saturating the input of the device with excessive voltages, though. Saturation could lead to extra input current resulting in an inaccurate impedance measurement. The device data sheet should list the acceptable range of input voltages.

3.5.2 Output Impedance

Output impedance (Z_{OUT}) is measured in the same way as input impedance. It is typically much lower than input impedance; so it is usually measured using a force-current/measure-voltage technique. However, in cases where the output impedance is very high, it may be measured using the force-voltage/measure-current method instead.

Example 3.2

In the output impedance test setup shown in Figure 3.12, current source SRC1 is set to 10 mA and the voltage at the pin is measured, yielding 1.61 V. Then SRC1 is set to −10 mA and the output voltage is measured at 1.42 V. What is the total output impedance (R_{OUT} plus the amplifier's output impedance)?

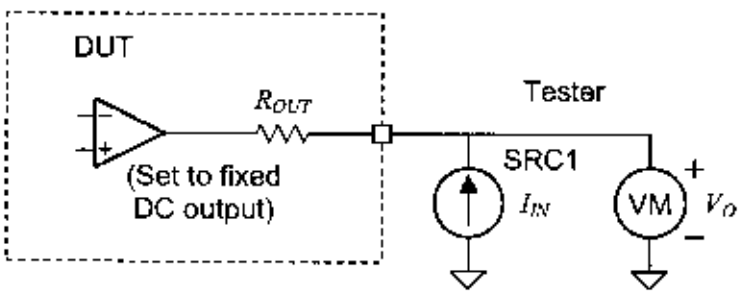


Figure 3.12. Output impedance test setup.

Solution:

Using Eq. (3.4) with Z_{IN} replaced by Z_{OUT}, we write

$$Z_{OUT} = \frac{1.61\ \text{V} - 1.42\ \text{V}}{10\ \text{mA} - (-10\ \text{mA})} = 9.5\ \Omega$$

3.5.3 Differential Impedance Measurements

Differential impedance is measured by forcing two differential voltages and measuring the differential current change. Example 3.3 illustrates this approach. Differential input impedance would be measured in a similar manner.

Example 3.3

In the differential output impedance test setup shown in Figure 3.13 current source SRC1 is set to 10 mA, SRC2 is set to −10 mA and the differential voltage at the pins is measured at 201 mV. Then SRC1 is set to −10 mA, SRC2 is set to 10 mA, and the output voltage is measured at −199 mV. What is the differential output impedance?

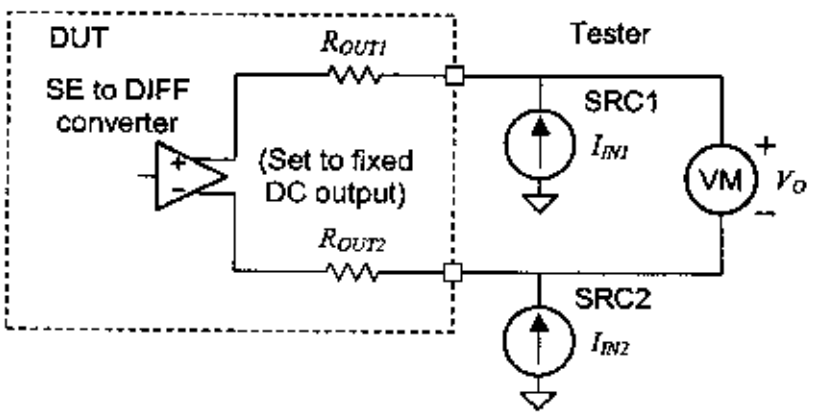


Figure 3.13. Differential output impedance test setup.

Solution:

The output impedance is found using Eq. (3.4) to be

$$Z_{OUT} = \frac{201\ \text{mV} - (-199\ \text{mV})}{20\ \text{mA} - (-20\ \text{mA})} = 10\ \Omega$$

3.6 DC Offset Measurements

3.6.1 V_{MID} and Analog Ground

Many analog and mixed-signal integrated circuits are designed to operate on a single power supply voltage (V_{DD} and ground) rather than a more familiar bipolar supply (V_{DD}, V_{SS}, and ground). Often these single-supply circuits generate their own low-impedance voltage between V_{DD} and ground that serves as a reference voltage for the analog circuits. This reference voltage, which we will refer to as V_{MID}, may be placed halfway between V_{DD} and ground or it may be placed at some other fixed voltage such as 1.35 V. In some cases, V_{MID} may be generated off-chip and supplied as an input voltage to the DUT.

To simplify the task of circuit analysis, we can define any circuit node to be 0 V and measure all other voltages relative to this node. Therefore, in a single-supply circuit having a V_{DD} of 3 V, a V_{SS} connected to ground, and an internally generated V_{MID} of 1.5 V, we can redefine all voltages relative to the V_{MID} node. Using this definition of 0 V, we can translate our single-supply circuit into a more familiar bipolar configuration with V_{DD} = +1.5 V, V_{MID} = 0 V, and V_{SS} = −1.5 V (Figure 3.14).

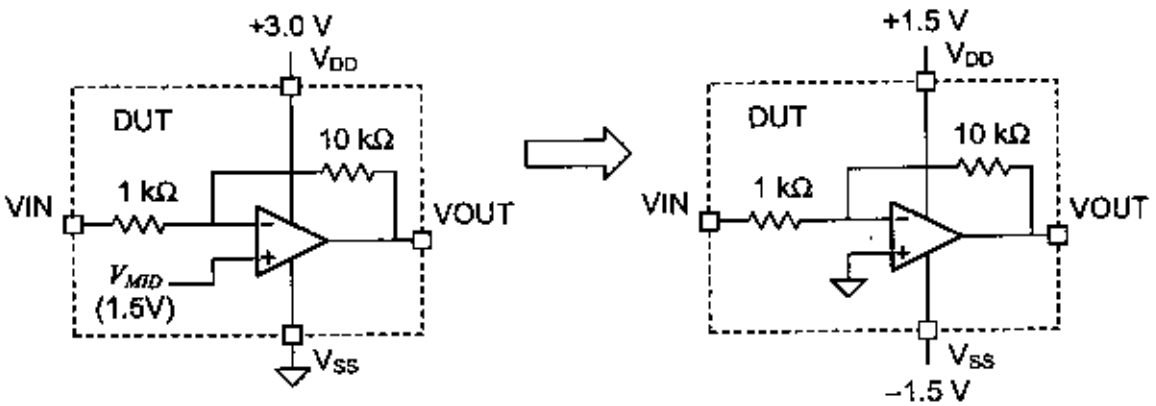


Figure 3.14. Redefining V_{MID} as 0 V to simplify circuit analysis.

Several integrated circuit design textbooks refer to this type of V_{MID} reference voltage as analog ground, since it serves as the ground reference in single-supply analog circuits. This is an unfortunate choice of terminology from a test engineering standpoint. Analog ground is a term used in the test and measurement industry to refer to a high-quality ground that is separated from the noisy ground connected to the DUT's digital circuits. In fact, the term "ground" has a definite meaning when working with measurement equipment since it is actually tied to earth ground for safety reasons. In this textbook, we will use the term analog ground to refer to a quiet 0 V voltage for use by analog circuits and the term V_{MID} to refer to an analog reference voltage (typically generated on-chip) that serves as the IC's analog "ground."

3.6.2 DC Transfer Characteristics (Gain and Offset)

The input-output DC transfer characteristic for an ideal amplifier is shown in Figure 3.15. The input-output variables of interest are voltage, but they could just as easily be replaced by current

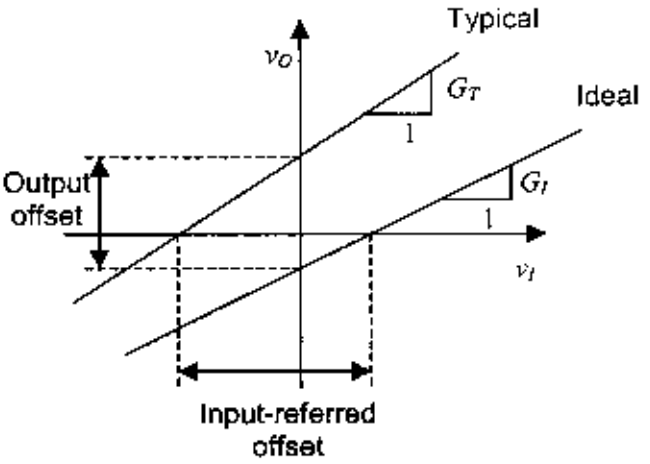


Figure 3.15. Amplifier input-output transfer characteristics in its linear region.

signals. As the real world is rarely accommodating to IC and system design engineers, the actual transfer characteristic for the amplifier would deviate somewhat from the ideal or expected curve. To illustrate the point, we superimpose another curve on the plot in Figure 3.15 and label it "Typical."

In order to maintain correct system operation, design engineers require some assurance that the amplifier transfer characteristic is within acceptable tolerance limits. Of particular interest to the test engineer are the gain and offset voltages shown in the figure. In this section we shall describe the method to measure offset voltages (which is equally applicable to current signals as well) and the next section will describe several methods used to obtain amplifier gain.

3.6.3 Output Offset Voltage (V_O)

The output offset (V_O) of a circuit is simply the difference between its ideal DC output and its actual DC output when the input is set to some fixed reference value, normally analog ground or V_{MID}. Output offset is depicted in Figure 3.15 for an input reference value of 0 V. As long as the output is not noisy and there are no AC signal components riding on the DC level, output offset is a trivial test. If the signal is excessively noisy, the noise component must be removed from the DC level in one of two ways. First, the DC signal can be filtered using a low-pass filter. The output of the filter is measured using a DC voltmeter. ATE testers usually have a low-pass filter built into their DC meter for such applications. The low-pass filter can be bypassed during less demanding measurements in order to minimize the overall settling time. The second method of reducing the effects of noise is to collect multiple readings from the DC meter and then mathematically average the results. This is equivalent to a software low-pass filter.

Sometimes sensitive DUT outputs can be affected by the ATE tester's parasitic loading. Some op amps will become unstable and break into oscillations if their outputs are loaded with the stray capacitance of the tester's meter and its connections to the DUT. An ATE meter may add as much as 200 pF of loading on the output of the DUT depending on the connection scheme chosen by the test engineer. The design engineer and test engineer should evaluate the possible effects of the tester's stray capacitance on each DUT output. It may be necessary to add a buffer amplifier to the DIB to provide isolation between the DUT output and the tester's instruments.

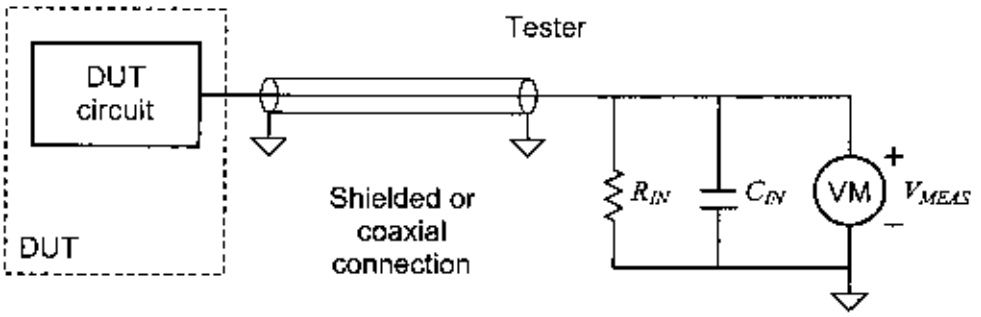


Figure 3.16. Meter impedance loading.

The input impedance of the tester can also shift DC levels when very high-impedance circuit nodes are tested. Consider the circuit in Figure 3.16 where the DUT is assumed to have an output impedance R_{OUT} of 100 kΩ. The DC meter in this example has an input impedance R_{IN} of 1 MΩ. According to the voltage divider principle with two resistors in series, the voltage that appears across the meter V_{MEAS} with respect to the output V_O of the DUT is

$$V_{MEAS} = \frac{R_{IN}}{R_{IN} + R_{OUT}} V_O = \frac{1\ \text{M}\Omega}{1\ \text{M}\Omega + 100\ \text{k}\Omega} V_O$$
$$= 0.909 V_O$$

It is readily apparent that a relative error of

$$\text{relative error} = \frac{V_O - V_{MEAS}}{V_O} = \frac{(1 - 0.909)}{1} = 0.091$$

or 9.1% is introduced into this measurement. A unity gain buffer amplifier may be necessary to provide better isolation between the DUT and tester instrument.

3.6.4 Single-Ended, Differential, and Common-Mode Offsets

Single-ended output offsets are measured relative to some ideal or expected voltage level when the input is set to some specified reference level. Usually these two quantities are the same and are specified on the data sheet. Differential offset is the difference between two outputs of a differential circuit when the input is set to a stated reference level. For simplicity sake, we shall use V_O to denote the output offset for both the single-ended and differential case. It should be clear from the context which offset is being referred to. The output common-mode voltage $V_{CM\text{-}O}$ is defined as the average voltage level at the two outputs of a differential circuit. Common-mode offset $V_{O\text{-}CM}$ is the difference between the output common-mode voltage and the ideal value under specified input conditions.

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ample 3.4

Consider the single-ended to differential converter shown in Figure 3.17. The two outputs of the circuit are labeled OUTP and OUTN. A 1.5-V reference voltage V_{MID} is applied to the input of

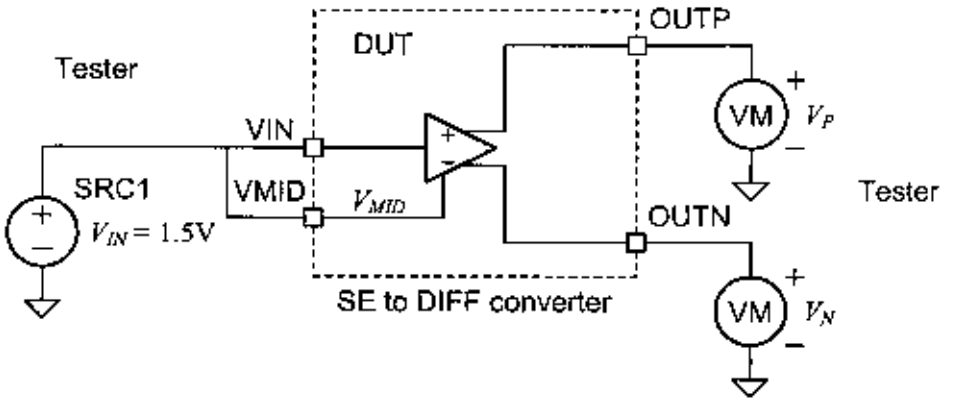

Figure 3.17. Differential output offset test setup.

the circuit and ideally, the outputs should both produce V_{MID}. The voltages at OUTP and OUTN denoted V_P and V_N, respectively, are measured with a meter, producing the following two readings:

$$V_P = 1.507 \text{ V} \quad \text{and} \quad V_N = 1.497 \text{ V}$$

With an expected output reference level of $V_{MID} = 1.50$ V, compute the differential and common-mode offsets.

Solution:

OUTP single-ended offset voltage, $V_{O\text{-}P} = V_P - V_{MID} = +7$ mV

OUTN single-ended offset voltage, $V_{O\text{-}N} = V_N - V_{MID} = -3$ mV

differential offset, $V_O = V_P - V_N = +10$ mV

Output common-mode voltage, $V_{CM\text{-}O} = (V_P + V_N) / 2 = 1.502$ V

Common-mode offset, $V_{O\text{-}CM} = V_{CM\text{-}O} - V_{MID} = 2$ mV

In the preceding example, V_{MID} is provided to the device from a highly accurate external voltage source. But what happens when the V_{MID} reference is generated from an on-chip reference circuit which itself has a DC offset? Typically there is a separate specification for the V_{MID} voltage in such cases; the input of the DUT should be connected to the V_{MID} voltage, if it is possible to do so and the output offsets are then specified relative to the V_{MID} voltage rather than the ideal value.

Thus the inputs and outputs are treated as if V_{MID} was exactly correct. Any errors in the V_{MID} voltage are evaluated using a separate V_{MID} DC voltage test. In this manner, DC offset errors caused by the single-ended to differential converter can be distinguished from errors in the V_{MID} reference voltage. This extra information may prove to be very useful to design engineers who must decide what needs to be corrected in the design.

3.6.5 Input Offset Voltage (V_{OS})

Input offset voltage (V_{OS}) refers to the negative of the voltage that must be applied to the input of a circuit in order to restore the output voltage to a desired reference level, that is, analog ground or V_{MID}. If an amplifier requires a +10 mV input to be applied to its input to force the output level to analog ground, then V_{OS} = -10 mV. It is common in the literature to find V_{OS} defined as the output offset V_O divided by the measured gain G of the circuit

$$V_{OS} \equiv \frac{V_O}{G} \tag{3.5}$$

If an amplifier has a gain of 10 V/V and its output has an output offset of 100 mV, then its input offset voltage is 10 mV. This will always be true provide the values used in Eq. (3.5) are derived from the circuit in its linear region of operation. In high-gain circuits, such as an open-loop op amp, it is not uncommon to find the amplifer in a saturated state when measuring the output offset voltage. As such, Eq. (3.5) is not applicable.

Exercises

3.4. For a x10 amplifier characterized by $V_{OUT} = 10V_{IN} + 5$, what are its input and output offset voltages?

Ans. +0.5 V (input), 5 V (output).

3.5. For a x10 amplifier characterized by $V_{OUT} = 10V_{IN} - V_{IN}^2 + 5$ over a 10-V range, what is its input and output offset voltages?

Ans. +0.477 V (input), 5 V (output).

3.6. A voltmeter with an input impedance of 100 kΩ is to measure the DC output of an amplifier with an output impedance of 500 kΩ. What is the expected relative error made by this measurement?

Ans. 16.6%.

3.7. A differential amplifier has an output OUTP of 3.3 V and an output OUTN of 2.8 V with its input set to a V_{MID} reference level of 3 V. What are the single-ended and differential offsets? The common-mode offset?

Ans. 0.3 V and –0.2V (SE), 0.5 V (DIFF), 50 mV (CM).

3.8. A perfectly linear amplifier has a measured gain of 5.1 V/V and an output offset of –3.2 V. What is the input offset voltage?

Ans. –0.627 V.

3.7 DC Gain Measurements

3.7.1 Closed-Loop Gain

Closed-loop DC gain is one of the simplest measurements to make, as the input-output signals are roughly comparable in level. Closed-loop gain, denoted G, is defined as the slope of the amplifier input-output transfer characteristic, as illustrated in Figure 3.15. We refer to this gain as closed-loop as it typically contrived from a set of electronic devices configured in a negative feedback loop. It is computed by simply dividing the change in output level of the amplifier or circuit by the change in its input

$$G = \frac{\Delta V_O}{\Delta V_I} \tag{3.6}$$

DC gain is measured using two DC input levels that fall inside the linear region of the amplifier. This latter point is particularly important, as false gain values are often obtained when the amplifier is unknowingly driven into saturation by poorly chosen input levels. The range of linear operation should be included in the test plan.

Gain can also be expressed in decibels (dB). The conversion from volt-per-volt to decibels is simply

$$G(\text{dB}) = 20\log_{10}\left|G(\text{V/V})\right| \tag{3.7}$$

The logarithm function in Eq.(3.7) is a base-10 log as opposed to a natural log.

Example 3.5

An amplifier with an expected gain of -10 V/V is shown in Figure 3.18. Both the input and output levels are referenced to an internally generated voltage V_{MID} of 1.5 V. SRC1 is set to 1.4 V and an output voltage of 2.51 V is measured with a voltmeter. Then SRC1 is set to 1.6 V and an output voltage of 0.47 V is measured. What is the DC gain of this amplifier in V/V? What is the gain in decibels?

Solution:

The gain of the amplifier is computed using Eq. (3.5) as

$$G = \frac{2.51\text{ V} - 0.47\text{ V}}{1.4\text{ V} - 1.6\text{ V}} = -10.2\text{ V/V}$$

or, in terms of decibels

$$G = 20\log_{10}\left|-10.2\right| = 20.172\text{ dB}$$

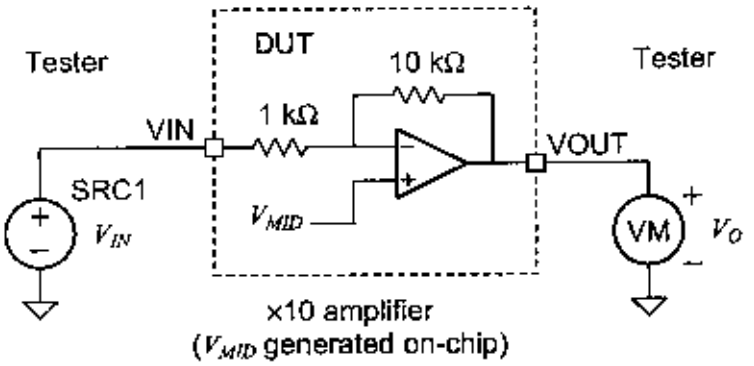

Figure 3.18. A ×10 amplifier gain test setup.

Gain may also be specified for circuits with differential inputs and/or outputs. The measurement is basically the same.

Example 3.6

A fully differential amplifier with an expected gain of +10 V/V is shown in Figure 3.19. SRC1 is set to 1.6 V and SRC2 is set to 1.4 V. This results in a differential input of 200 mV. An output voltage of 2.53 V is measured at OUTP and an output voltage of 0.48 V is measured at OUTN. This results in a differential output of 2.05 V. Then SRC1 is set to 1.4 V and SRC2 is set to 1.6 V. This results in a differential input level of –200 mV. An output voltage of 0.49 V is measured at OUTP and an output voltage of 2.52 V is measured at OUTN. The differential output voltage is thus -2.03 V. Using the measured data provided, compute the differential gain of this circuit.

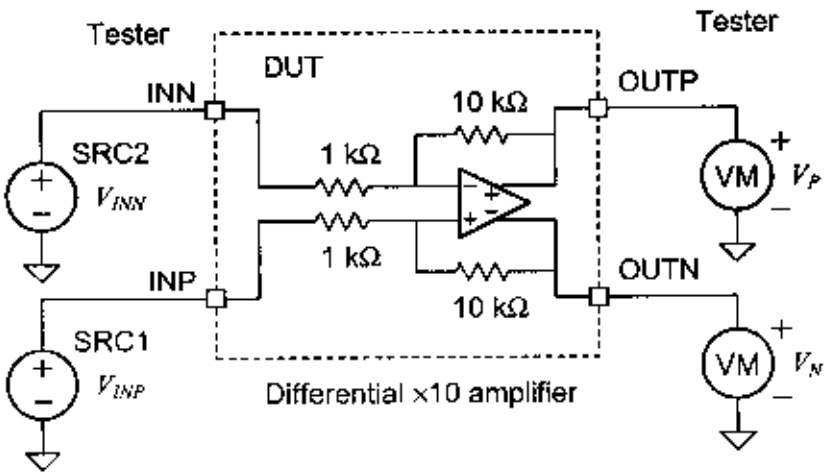

Figure 3.19. Differential ×10 amplifier gain test setup.

Solution:

The differential gain is found using Eq. (3.5) to be

$$G = \frac{2.05\ \text{V} - 2.03\ \text{V}}{200\ \text{mV} - (-200\ \text{mV})} = +10.2\ \text{V/V}$$

Differential measurements can be made by measuring each of the two output voltages individually and then computing the difference mathematically. Alternatively, a differential voltmeter can be used to directly measure differential voltages. Obviously the differential voltmeter approach will work faster than making two separate measurements. Therefore, the use of a differential voltmeter is the preferred technique in production test programs. Sometimes the differential voltage is very small compared to the DC offset of the two DUT outputs. A differential voltmeter can often give more accurate readings in these cases.

In cases requiring extreme accuracy, it may be necessary to measure the input voltages as well as the output voltages. The DC voltage sources in most ATE testers are well calibrated and stable enough to provide a voltage error no greater than 1 mV in most cases. If this level of error is unacceptable, then it may be necessary to use the tester's high-accuracy voltmeter to measure the exact input voltage levels rather than trusting the sources to produce the desired values. The gain equation in the previous example would then be

$$G = \frac{2.05\ \text{V} - 2.03\ \text{V}}{V_1 - V_2}$$

where V_1 and V_2 are the actual input voltages measured using a differential voltmeter.

Exercises

3.9. Voltages of 0.8 and 4.1 V appear at the output of a single-ended amplifier when an input of 1.4 and 1.6 V is applied, respectively. What is the gain of the amplifier in V/V? What is the gain in decibels?

Ans. –16.5 V/V, 24.35 dB.

3.10. An amplifier is characterized by $V_{OUT} = 2.5\ V_{IN} + 1$ over an output voltage range of 0 to 10 V. What is the amplifier output for a 2-V input? Similarly for a 3-V input? What is the corresponding gain of this amplifier in V/V over the 1-V swing? What is the gain in decibels?

Ans. 6 V, 8.5 V, +2.5 V/V, 7.96 dB.

3.11. An amplifier is characterized by $V_{OUT} = 2.5\ V_{IN} + 0.25\ V_{IN}^2 + 1$ over an output voltage range of 0 to 12 V. What is the amplifier output for a 2-V input? Similarly for a 3-V input? What is the corresponding gain of this amplifier in V/V over the 1-V swing? What is the gain in decibels? Would a 4-V input represent a valid test point?

Ans. 7 V, 10.75 V, +3.75 V/V, 11.48 dB, No – the output would exceed 12 V.

The astute reader may have noticed that the gain and impedance measurements are fairly similar, in that they both involve calculating a slope from a DC transfer characteristic pertaining to the DUT. Moreover, they do not depend on any value for the offsets, only that the appropriate slope is obtained from the linear region of the transfer characteristic.

3.7.2 Open-Loop Gain

Open-loop gain (abbreviated G_{ol}) is a basic parameter of op amps. It is defined as the gain of the amplifier with no feedback path from output to input. Since many op amps have G_{ol} values of 10,000 V/V or more, it is difficult to measure open-loop gain with the straightforward techniques of the previous examples. It is difficult to apply a voltage directly to the input of an open loop op amp without causing it to saturate, forcing the output to one power supply rail or the other. For example, if the maximum output level from an op amp is ±5 V and its open-loop gain is equal to 10,000 V/V, then an input-referred offset of only 500 μV will cause the amplifier output to saturate. Since many op amps have input-referred offsets ranging over several millivolts, we cannot predict what input voltage range will result in unsaturated output levels.

We can overcome this problem using a second op amp connected in a feedback path as shown in Figure 3.20. The second amplifier is known as a *nulling amplifier*. The nulling amplifier forces its differential input voltage to zero through a negative feedback loop formed by resistor string R_2 and R_1, together with the DUT op amp. This loop is also known as a servo loop[2]. By doing so, the output of the op amp under test can be forced to a desired output level according to

$$V_{O-DUT} = 2V_{MID} - V_{SRC1} \tag{3.8}$$

where V_{MID} is a DC reference point (grounded in the case of dual-supply op amps, non-grounded for single-supply op amps) and V_{SRC1} is the programmed DC voltage from SRC1. The nulling amplifier and its feedback loop compensate for the input-referred offset of the DUT amplifier. This ensures that the DUT output does not saturate due to its own input-referred offset.

The two matched resistors, R_3, are normally chosen to be around 100 kΩ as a compromise between source loading and op amp bias induced offsets. Since the gain around the loop is extremely large, feedback capacitor C is necessary to stabilize the loop. A capacitance value of 1 to 10 nF is usually sufficient. R_{LOAD} provides the specified load resistance for the G_{ol} test.

Under steady-state conditions, the signal that is fed back to the input of the DUT amplifier denoted V_{IN-DUT} is directly related to the nulling amplifier output V_{O-NULL} according to

$$V_{IN-DUT} = V_{DUT}^{+} - V_{DUT}^{-} = \frac{R_1}{R_1 + R_2}\left(V_{O-NULL} - V_{MID}\right) \tag{3.9}$$

where V^{+}_{DUT} and V^{-}_{DUT} are the positive and negative inputs to the DUT amplifier, respectively. Subsequently, the open-loop voltage gain of the DUT amplifier is found from Eqs. (3.6), (3.8), and (3.9) to be given by

$$G_{ol} = \frac{\Delta V_{O-DUT}}{\Delta V_{IN-DUT}} = -\left(\frac{R_1 + R_2}{R_1}\right)\frac{\Delta V_{SRC1}}{\Delta V_{O-NULL}} \tag{3.10}$$

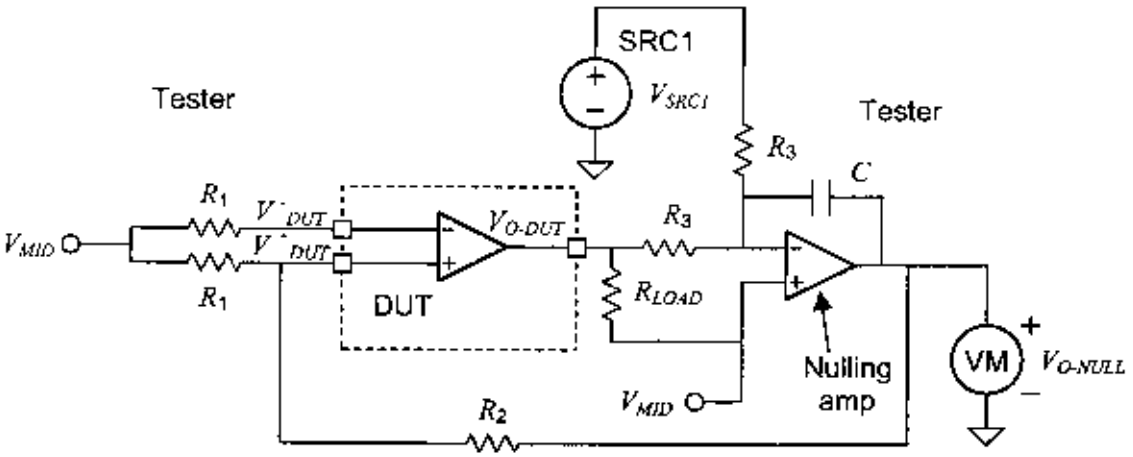

Figure 3.20. Open-loop gain test setup using nulling amplifier.

The nulling loop method allows the test engineer to force two desired outputs and then indirectly measure the tiny inputs that caused those two outputs. In this manner, very large gains can be measured without measuring tiny voltages. Of course the accuracy of this approach depends on accurately knowing the values of R_1 and R_2, and on matching the two resistors, labeled as R_3.

In order to maximize the signal handling capability of the test setup shown in Figure 3.20, and avoid saturating the nulling amplifer, it is a good idea to set the voltage divider ratio to a value approximately equal to the inverse of the expected open-loop gain of the DUT op amp

$$\frac{R_1}{R_1 + R_2} \approx \frac{1}{G_{ol}} \tag{3.11}$$

from which we can write $R_2 \approx G_{ol} R_1$.

Example 3.7

For the nulling amplifier setup shown in Figure 3.20 with R_1=100 Ω, R_2=100 kΩ and R_3=100 kΩ, together with V_{MID} set to a value midway between the two power supply levels (its actual value is not important as all signals will be referenced to it), SRC1 is set to V_{MID} + 1 V and a voltage of V_{MID} + 2.005 V is measured at the nulling amplifier output. SRC1 is set to V_{MID} − 1 V and a voltage of V_{MID} + 4.020 V is measured at the nulling amplifier output. What is the open-loop gain of the amplifier?

Solution:

Open loop gain is calculated using the following procedure. First the change or swing in the nulling amplifier output $\Delta V_{O\text{-}NULL}$ is computed

$$\Delta V_{O\text{-}NULL} = 2.005 \text{ V} - 4.020 \text{ V} = -2.015 \text{ V}$$

then, using Eq. (3.9) the voltage swing at the input of the DUT amplifier, $\Delta V_{IN\text{-}DUT}$, is calculated

$$\begin{aligned}\Delta V_{IN-DUT} &= \frac{R_1}{R_1+R_2}\Delta V_{O-NULL} \\ &= \frac{100}{100+100k}(-2.015\text{ V}) \\ &= -2.013\text{ mV}\end{aligned}$$

Making use of the fact that ΔV_{SRC1} is 2 V, which forces $\Delta V_{O\text{-}DUT} = -2$ V, the open-loop gain of the amplifier is found to be

$$G_{ol} = \frac{\Delta V_{O-DUT}}{\Delta V_{IN-DUT}} = \frac{-2\text{ V}}{-2.013\text{ mV}} = 993.5\text{ V/V}$$

If the op amp in the preceding example had an open-loop gain closer to 100 V/V instead of 1000 V/V, then the output of the nulling amplifier would have produced a voltage swing of 20 V instead of 2 V. The nulling amplifier would have been dangerously close to clipping against its output voltage rails (assuming ±15-V power supplies). In fact, if a 5-V op amp were used as the nulling amplifier, it would obviously not be able to produce the 20-V swing.

In the example, the nulling amplifier should have produced two voltages centered around V_{MID}. Instead, it had an average or common-mode offset level of approximately 3 V from this value. A detailed circuit analysis reveals that this offset is caused exclusively by the input-referred offset of the DUT. Hence, the offset that appears at the output of the nulling amplifier, denoted $V_{O\text{-}NULL\text{-}Offset}$, can be used to compute the input-referred offset of the DUT, $V_{OS\text{-}DUT}$.

Exercises

3.12. For the nulling amplifier setup shown in Figure 3.20 with R_1=100 Ω, R_2=100 kΩ, and R_3=100 kΩ, an SRC1 voltage swing of 1 V results in a 2.3-V swing at the output of the nulling amplifier. What is the open-loop gain in V/V of the DUT amplifier? What is the gain in decibels?

Ans. 435.2 V/V, 52.77 dB.

3.13. For the nulling amplifier setup shown in Figure 3.20 with R_1=1 kΩ, R_2=100 kΩ, and R_3=100 kΩ, an offset of 2.175 V + V_{MID} appears at the output of the nulling op amp when the SRC1 voltage is set to V_{MID}. What is the input offset of the DUT amplifier?

Ans. 21.5 mV.

3.14. For the nulling amplifier setup shown in Figure 3.20 with R_1=100 Ω, R_2=500 kΩ and R_3=100 kΩ, and the DUT op amp having an open-loop gain of 4,000 V/V, what is the output swing of the nulling amplifier when the SRC1 voltage swings by 1 V?

Ans. 1.25 V.

Input-referred offset would then be calculated using

$$V_{OS-DUT} = \frac{R_1}{R_1 + R_2} V_{O-NULL-Offset} \tag{3.12}$$

As this method involves the same measured data used to compute the open-loop gain, it is a commonly used method to determine the op amp input-referred offset. For the parameters and measurement values described in Example 3.7, the input-referred offset voltage for the DUT is

$$V_{OS-DUT} = \frac{100}{100+100k}\left(\frac{4.020\text{ V} + 2.005\text{ V}}{2}\right)$$
$$= 3.0\text{ mV}$$

3.8 DC Power Supply Rejection Ratio

3.8.1 DC Power Supply Sensitivity

Power supply sensitivity (PSS) is a measure of the circuit's dependence on a constant supply voltage. Normally it is specified separately with respect to the positive or negative power supply voltages and denoted PSS^+ and PSS^-. PSS is defined as the change in the output over the change in either power supply voltage with the input held constant

$$PSS^+ \equiv \left.\frac{\Delta V_O}{\Delta V_{PS^+}}\right|_{V_{in}\text{ constant}} \quad \text{and} \quad PSS^- \equiv \left.\frac{\Delta V_O}{\Delta V_{PS^-}}\right|_{V_{in}\text{ constant}} \tag{3.13}$$

In effect, PSS is a type of gain test in which the input is one of the power supply levels.

Example 3.8

The input of the ×10 amplifier in Figure 3.21 is connected to its own V_{MID} source forcing 1.5 V. The power supply is set to 3.1 V and a voltage of 1.5011 V is measured at the output of the amplifier. The power supply voltage is then changed to 2.9 V and the output measurement changes to 1.4993 V. What is the PSS of the amplifier in V/V? What is the PSS in decibels?

Solution:

As the positive power supply (V_{DD}) is being changed by SRC1, the positive power supply sensitivity is

$$PSS^+ = \frac{\Delta V_O}{\Delta V_{SRC1}} = \frac{1.5011\text{ V} - 1.4993\text{ V}}{3.1\text{ V} - 2.9\text{ V}} = 9\text{ mV/V} = -40.92\text{ dB}$$

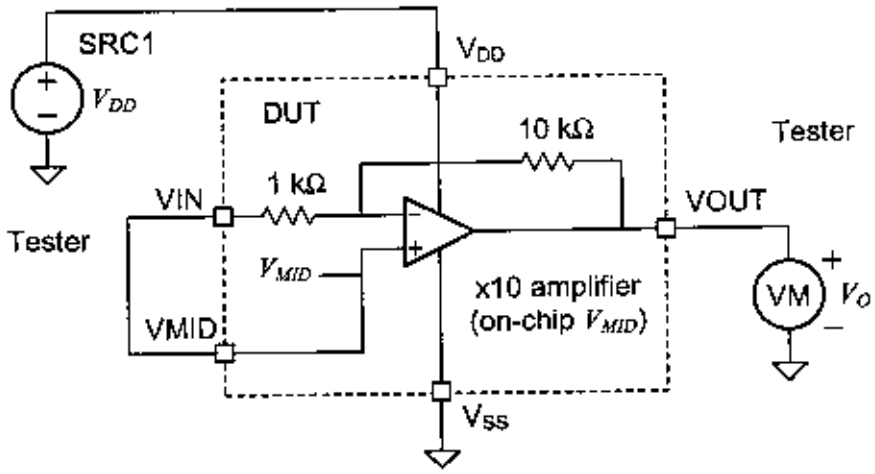

Figure 3.21. Power supply sensitivity test setup.

3.8.2 DC Power Supply Rejection Ratio

Power supply rejection ratio (PSRR) is defined as the power supply sensitivity of a circuit divided by the magnitude of the closed-loop gain of the circuit in its normal mode of operation. Normally it is specified separately with respect to each power supply voltage. Mathematically, we write

$$\text{PSRR}^{+} \equiv \frac{\text{PSS}^{+}}{|G|} \quad \text{and} \quad \text{PSRR}^{-} \equiv \frac{\text{PSS}^{-}}{|G|} \tag{3.14}$$

In Example 3.8, we found PSS^{+}=0.009 V/V. In Example 3.5, the DC gain of this same circuit was found to be −10.2 V/V. Hence the PSRR^{+} would be

$$\text{PSRR}^{+} = \frac{\text{PSS}^{+}}{|G|} = \frac{0.009\ \text{V/V}}{10.2\ \text{V/V}} = 882\ \mu\text{V/V}$$

Power supply rejection ratio is often converted into decibel units

$$\text{PSRR}^{+}\big|_{\text{dB}} = 20\log_{10}(882\ \mu\text{V/V}) = -61.09\ \text{dB}$$

3.9 DC Common-Mode Rejection Ratio

3.9.1 CMRR of Op Amps

Common-mode rejection ratio (CMRR) is a measurement of a differential circuit's ability to reject a common-mode signal V_{CM} at its inputs. It is defined as the magnitude of the common-mode gain G_{CM} divided by the differential gain G_D, given by

$$\text{CMRR} \equiv \left|\frac{G_{CM}}{G_D}\right| \tag{3.15}$$

This expression can be further simplified by substituting for the common-mode gain $G_{CM} = \Delta V_O / \Delta V_{CM}$, together with the definition for input-referred offset voltage defined in Eq. (3.5), as follows

$$CMRR = \left|\frac{\Delta V_O / \Delta V_{CM}}{G_D}\right| = \left|\frac{\Delta V_O / G_D}{\Delta V_{CM}}\right| \simeq \left|\frac{\Delta V_{OS}}{\Delta V_{CM}}\right| \tag{3.16}$$

The rightmost expression suggests the simplest procedure to measure CMRR; one simply measures ΔV_{OS} subject to a change in the input common-mode level ΔV_{CM}. One can measure ΔV_{OS} directly or indirectly, as the following two examples illustrate.

Example 3.9

Figure 3.22 shows a simple CMRR test fixture for an op amp. The test circuit is basically a difference-amplifier configuration with the two inputs tied together. V_{MID} is set to 1.5 V and an input common-mode voltage of 2.5 V is applied using SRC1. An output voltage of 1.501 V is measured at the output of the op amp. Then SRC1 is changed to 0.5 V and the output changes to 1.498 V. What is the CMRR of the op amp?

Solution:

As the measurement was made at the output of the circuit, we need to infer from these results the ΔV_{OS} for the op amp. This requires a few steps: The first is to find the influence of the op amp input-referred offset voltage V_{OS} on the test circuit output. As in Section 3.7.2, detailed circuit

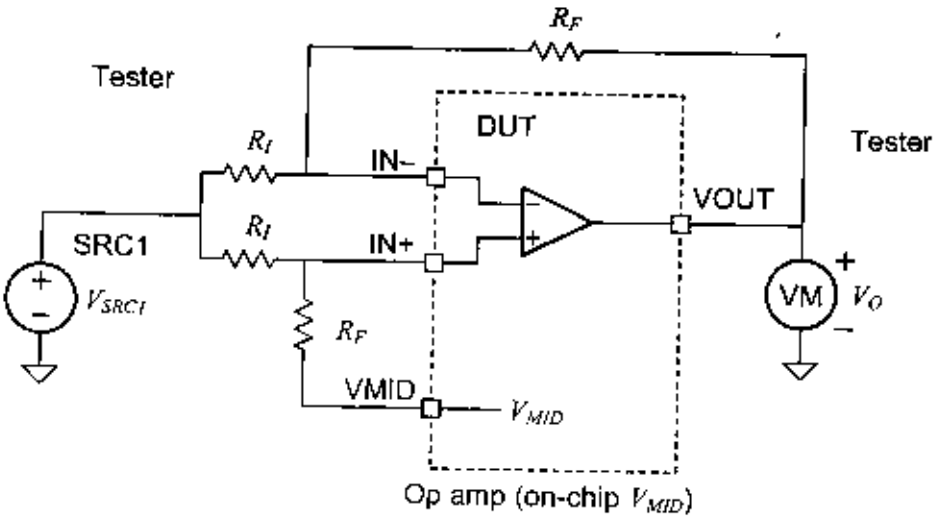

Figure 3.22. Op amp CMRR test setup.

analysis reveals

$$V_O = \frac{R_I + R_F}{R_I} V_{OS}$$

With all resistors equal and perfectly matched, $V_O = 2\ V_{OS}$. Hence, $\Delta V_O = 2\ \Delta V_{OS}$, or when rearranged, $\Delta V_{OS} = 0.5\ \Delta V_O$. Subsequently, substituting measured values $\Delta V_O = 1.501$ V–1.498 V = 3 mV, we find $\Delta V_{OS} = 1.5$ mV. This result can now be substituted into Eq. (3.16), together with $\Delta V_{CM} = \Delta V_{SRC1} = 2.5$ V – 0.5 V = 2.0 V, leading to a CMRR = 750 μV/V or –62.5 dB.

There is one major problem with this technique for measuring op amp CMRR: the resistors must be known precisely and carefully matched. A CMRR value of –100 dB would require resistor matching to 0.0001%, an impractical value to achieve in practice. A better test circuit setup is the nulling amplifier configuration shown in Figure 3.23. This configuration is very similar to the one used previously to measure the open-loop gain and input offsets of Section 3.7. The basic circuit arrangement is identical, only the excitation and the position of the voltmeter are changed. With this test setup, one can vary the common-mode input to the DUT and measure the differential voltage between the input SRC1 and the nulling amplifier output, which we shall denote as $V_{O\text{-}NULL}$. This in turn can then be used to deduce the input-referred offset for the DUT amplifier according to

$$V_{OS\text{-}DUT} = \frac{R_1}{R_1 + R_2} V_{O\text{-}NULL} \tag{3.17}$$

Subsequently, the CMRR of the op amp is given by

$$CMRR = \frac{R_1}{R_1 + R_2} \left| \frac{\Delta V_{O\text{-}NULL}}{\Delta V_{SRC1}} \right| \tag{3.18}$$

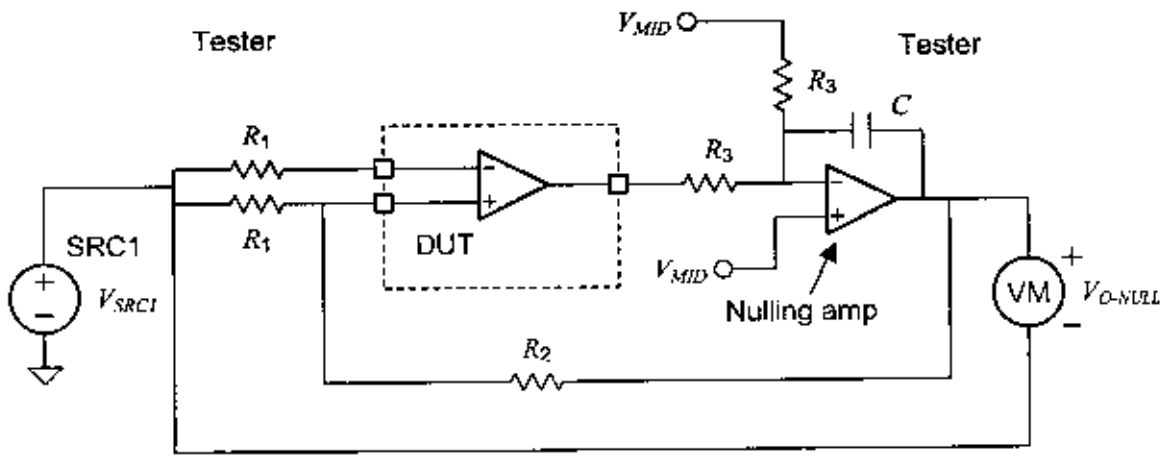

Figure 3.23. Op amp CMRR test setup using nulling amplifier.

Example 3.10

For nulling amplifier setup shown in Figure 3.23 with R_1=100 Ω, R_2=100 k Ω, and R_3=100 k Ω, together with V_{MID} set to a value midway between the two power supply levels, SRC1 is set to +2.5 V and a differential voltage of 10 mV is measured between SRC1 and the output of the nulling amplifier. Then SRC1 is set to 0.5 V and the measured voltage changes to –12 mV. What is the CMRR of the op amp?

Solution:

Using Eq. (3.17), we deduce

$$\begin{aligned}\Delta V_{OS-DUT} &= \frac{R_1}{R_1+R_2}\Delta V_{O-NULL} \\ &= \frac{100}{100+100\text{k}}\left[10\text{ mV}-(-12\text{ mV})\right] \\ &= 22\,\mu\text{V}\end{aligned}$$

for a corresponding ΔV_{SRC1} = 2.5 V – 0.5 V, or 2.0 V. Thus the CMRR is

$$\text{CMRR} = \frac{22\,\mu\text{V}}{2.0\text{ V}} = 11\frac{\mu\text{V}}{\text{V}} = -99.17\text{ dB}$$

3.9.2 CMRR of Differential Gain Stages

Integrated circuits often use op amps as part of a larger circuit such as a differential input amplifier. In these cases, the CMRR of the op amp is not as important as the CMRR of the circuit as a whole. For example, a differential amplifier configuration such as the one in Figure 3.22 may have terrible CMRR if the resistors are poorly matched, even if the op amp itself has a CMRR of –100 dB. The differential input amplifier CMRR specifications include not only the effects of the op amp, but also the effects of on-chip resistor mismatch. As such, we determine the CMRR using the original definition given in Eq. (3.15). Our next example will illustrate this.

Example 3.11

Figure 3.24 illustrates the test setup to measure the CMRR of a differential amplifier having a nominal gain of 10. No assumption about resistor matching is made. Both inputs are connected to a common voltage source SRC1 whose output is set to 2.5 V. A voltage of 1.501 V is measured at the output of the DUT. Then SRC1 is set to 0.5 V and a second voltage of 1.498 V is measured at the DUT output. Next the differential gain of the DUT circuit is measured using the technique described in Section 3.7.1. The gain was found to be 10.2 V/V. What is the CMRR?

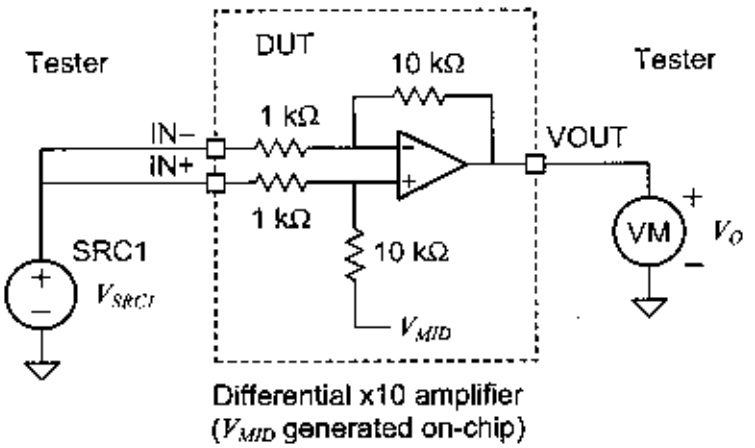

Figure 3.24. A ×10 Differential amplifier CMRR test setup.

Solution:

Since $\Delta V_O = 1.501\ \text{V} - 1.498\ \text{V} = 3\ \text{mV}$ corresponding to a $\Delta V_{CM} = \Delta V_{SRC1} = 2.0\ \text{V}$, the common-mode gain G_{CM} is calculated to be equal to 0.0015 V/V. In addition, we are told that the differential gain G_D is 10.2 V/V; thus we find the CMRR from the following

$$CMRR = \left|\frac{G_{CM}}{G_D}\right| = \left|\frac{0.0015\text{V/V}}{10.2\text{V/V}}\right| = 0.000147 = -76.65\ \text{dB}$$

Exercises

3.15. An amplifier has an expected CMRR of -100 dB. For a 1-V change in the input common-mode level, what is the expected change in the input offset voltage of this amplifier?

Ans. 10 μV.

3.16. For the nulling amplifier CMRR setup in Figure 3.23 with R_1=100 Ω, R_2=500 kΩ, and R_3=100 kΩ, SRC1 is set to +3.5 V and a differential voltage of 210 mV is measured between SRC1 and the output of the nulling amplifier. Then SRC1 is set to 0.5 V and the measured voltage changes to –120 mV. What is the CMRR of the op amp in decibels?

Ans. 21.99 μV/V, -93.15 dB.

3.10 Comparator DC Tests

3.10.1 Input Offset Voltage

Input offset voltage for a comparator is defined as the differential input voltage that causes the comparator to switch from one output logic state to the other. The differential input voltage can be ramped from one voltage to another to find the point at which the comparator changes state. This switching point is, however, dependent on the input common-mode level. One usually tests for the input offset voltage under worst-case conditions as outlined in the device test plan.

Example 3.12

The comparator in Figure 3.25 has a worst-case input offset voltage of ±50 mV and a midsupply voltage of 1.5V. Describe a test setup and procedure with which to obtain its input offset voltage.

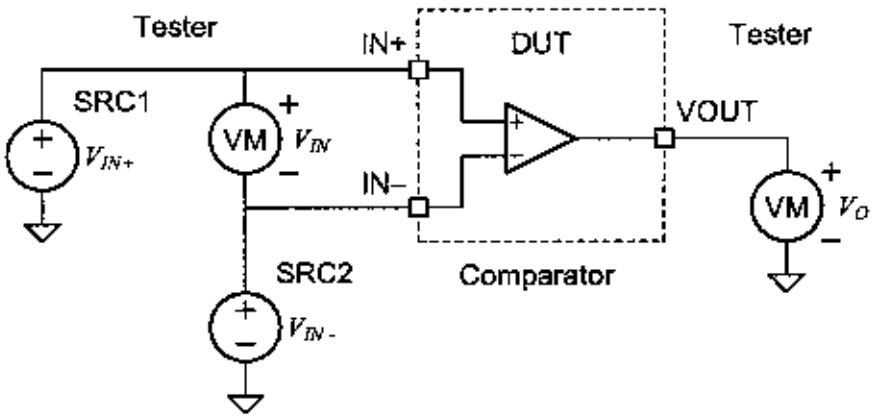

Figure 3.25. Comparator input offset voltage test setup.

Solution:

The comparator in Figure 3.25 is connected to two voltage sources, SRC1 and SRC2. SRC2 is set to 1.5 V and SRC1 is ramped upward from 1.45 to 1.55 V, as the switching point is expected to lie within this range. When the output changes from logic LO to logic HI, the differential input voltage V_{IN} is measured, resulting in an input offset voltage reading of +5 mV. The V_{IN} voltage could be deduced by simply subtracting 1.5 V from the SRC1 voltage, assuming the DC sources force voltages to an accuracy of a few hundred microvolts. This is usually a questionable assumption, though. It is best to measure small voltages using a voltmeter rather than assume the tester's DC sources are set to exact voltages.

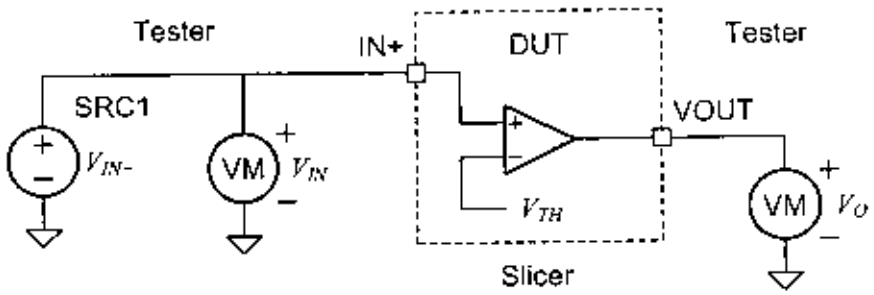

Figure 3.26. Slicer threshold voltage test setup.

3.10.2 Threshold Voltage

Sometimes a fixed reference voltage is supplied to one input of a comparator, forming a circuit known as a *slicer*. The input offset voltage specification is typically replaced by a single-ended specification, called *threshold voltage*.

The slicer in Figure 3.26 is tested in a similar manner as the comparator circuit in the previous example. Assuming the threshold voltage is expected to fall between 1.45 and 1.55 V, the input voltage from SRC1 is ramped upward from 1.45 to 1.55 V. The output switches states when the input is equal to the slicer's threshold voltage.

Notice that threshold voltage will be affected by the accuracy of the on-chip voltage reference, V_{TH}. In theory, the threshold voltage should be equal to the sum of the slicer's reference voltage V_{TH} plus the input offset voltage of the comparator. Threshold voltage error is defined as the difference between the actual and ideal threshold voltages.

3.10.3 Hysteresis

In the comparator input offset voltage example, the output changed when the input voltage reached 5 mV. This occurred on a rising input voltage. On a falling input voltage, the threshold may change to a lower voltage. This characteristic is called *hysteresis*, and it may or may not be an intentional design feature. Hysteresis is defined as the difference in threshold voltage between a rising input test condition and a falling input condition.

Example 3.13

The comparator in Figure 3.25 is connected to two voltage sources, SRC1 and SRC2. SRC2 is set to 1.5 V and SRC1 is ramped upward from 1.45 to 1.55 V in 1-mV steps. When the output changes from logic LO to logic HI, the differential input voltage is measured, resulting in an input offset voltage reading of +5 mV. Then the input is ramped downward from 1.55 to 1.45 V and the output switches when the input voltage reaches ~3 mV. What is the hysteresis of this comparator?

Solution:

The hysteresis is equal to the difference of the two input offset voltages

$$5 \text{ mV} - (-3 \text{ mV}) = 8 \text{ mV}$$

It should be noted that input offset voltage and hysteresis may change with different common-mode input voltages. Worst-case test conditions should be determined during the characterization process.

Exercises

3.17. A comparator has an input offset voltage of 50 mV and its positive terminal is connected to a 1-V level, at what voltage on the negative terminal does the comparator change state?

Ans. 0.950 V.

3.18. A slicer circuit is connected to a 1.65 V reference V_{TH} and has a comparator input offset voltage of 11 mV. At what voltage level will the slicer change state?

Ans. 1.76 V.

3.19. A comparator has a measured hysteresis of 9 mV and switches state on a rising input at 2.100 V. At what voltage does the comparator change to a low state on a falling input?

Ans. 2.091 V.

3.11 Voltage Search Techniques

3.11.1 Binary Searches versus Step Searches

The technique of ramping input voltages until an output condition is met is called a *ramp search*, or *step search*. Step searches are time-consuming and not well suited for production testing. A more efficient binary search technique may be used to reduce test time while maintaining the desired search resolution.

In a binary search, the input is adjusted up or down using a successive approximation algorithm. A binary search can be applied to the comparator input offset voltage test described in the previous section. Instead of ramping the input voltage from 1.45 to 1.55 V, the comparator input is set to 1.5 V and the output is observed. If the output is high, then the input is increased by one quarter of the 100-mV search range (25 mV) to try to make the output go low. If, on the other hand, the output is low, then the input is reduced by 25 mV to try to force the output high. Then the output is observed again. This time, the input is adjusted by one-eighth of the search range (12.5 mV). This process is repeated until the desired input adjustment resolution is reached.

The problem with the binary search technique is that it does not work well in the presence of hysteresis. The binary search algorithm assumes that the input offset voltage is the same whether the input voltage is increased or decreased. If the comparator exhibits hysteresis, then there are two different threshold voltages to be measured. To get around this problem without reverting to the time-consuming ramp search technique, a hybrid approach can be used. A binary search can be used to find the approximate threshold voltage quickly. Then a step search can be used with a much smaller search voltage range.

Another solution to the hysteresis problem is to use a modified binary search algorithm in which the output state of the comparator is returned to a consistent logic state between binary search approximations. The output state is set to a consistent level between approximations by forcing the input either well above or well below the threshold voltage. In this way, steps are always taken in one direction, avoiding hysteresis effects. To measure hysteresis, a binary search is used once with the output state forced high between approximations. Then input offset is measured again with the output state forced low between approximations. The difference in input offset readings is equal to the hysteresis of the comparator.

3.11.2 Linear Searches

Linear circuits can make use of an even faster search technique called a *linear search*. A linear search is similar to the binary search, except that the input approximations are based on a linear interpolation of input-output relationships. For example, if a 0-mV input to a buffer amplifier results in a 10-mV output and a 1-mV input results in a 20-mV output, then a −1-mV input will probably result in a 0-mV output. The linear search algorithm keeps refining its guesses using a simple $V_{OUT} = M \times V_{IN} + B$ algorithm until the desired accuracy is reached. The following example will illustrate the method.

Example 3.14

Using a linear search algorithm find the input offset voltage V_{OS} for a ×10 amplifier.

Solution:

The input to a ×10 amplifier is set to 0 V and the output is measured, yielding a reading of 120 mV. The gain M is known to be approximately 10, since this is supposed to be a ×10 amplifier. The value of offset B can be approximately determined using the $V_{OUT} = M \times V_{IN} + B$ linear equation, that is

$$120 \text{ mV} = M \times 0 \text{ mV} + B = 10 \times 0 \text{ mV} + B$$
$$\Rightarrow B = 120 \text{ mV (first-pass guess)}$$

Since 0 mV is the desired output, the next estimate for V_{OS} can be calculated using the linear equation again

$$0 \text{ mV (desired } V_{OUT}) = M \times V_{IN} + B = 10 \times V_{IN} + 120 \text{ mV}$$

Rewriting this equation to solve for V_{IN}, we get

$$V_{IN} = \frac{(0\text{ mV}-120\text{ mV})}{10} = -12\text{ mV}$$

Applying the best guess of –12 mV to the input, another output measurement is made, resulting in a reading of 8 mV. Now we have two equations in two unknowns

$$120\text{ mV} = M \times 0\text{ mV} + B$$
$$8\text{ mV} = M(-12\text{ mV}) + B$$

from which a more accurate estimate of M and B can be made. Solving for the two unknowns

$$M = \frac{120\text{ mV}-8\text{ mV}}{0\text{ mV}-(-12\text{ mV})} = 9.333\text{ V/V}$$
$$B = 10\text{ mV}-[M(-12\text{ mV})] = 122\text{ mV}$$

The next input approximation should be close enough to the input offset voltage to produce an output of 0 mV, that is

$$V_{OS} = \frac{(0\text{ mV}-B)}{M} = \frac{(0\text{ mV}-122\text{ mV})}{9.333} = -13.1\text{ mV}$$

The input offset voltage of the ×10 amplifier is therefore –13.1 mV, assuming the circuit is linear. In cases where the input-output relationship is not linear, the linear search technique will still work, but will require more iterations of the above process. During each iteration, the linear interpolations are calculated using the most recent two input-output data points until the input converges to the desired measurement resolution.

Exercises

3.20. For an amplifier characterized by $V_{OUT} = 10V_{IN} - V_{IN}^2 + 5$ over a ±5 V output voltage range, determine the input offset voltage using a binary search process. The input offset voltage is known to fall between 464 and 496 mV. How many search iterations are required for a maximum error of 1 mV? List the input values and corresponding outputs.

Ans. A 32-mV search range with 2-mV resolution is required, requiring four binary iterations: (1) –480 mV, –30.4 mV; (2) –472 mV, +57 mV; (3) –476 mV, +13.4 mV; (4) –478 mV, –8.5 mV. The final estimate is thus –477 mV (V_{OS} = +477 mV; true answer is +477.2 mV).

3.21. Repeat Exercise 3.20 using a linear search process starting with two points at V_{IN} = –250 mV and –750 mV. How many iterations are required for < 1 mV error in V_{OS}?

Ans. Two iterations produce estimates of V_{OS} = +471.6 mV and V_{OS} = +477.1 mV.

3.12 DC Tests for Digital Circuits

3.12.1 I_{IH}/I_{IL}

The data sheet for a mixed-signal device usually lists several DC specifications for digital inputs and outputs. Input leakage currents (I_{IH} and I_{IL}) were discussed in Section 3.2.2. Input leakage is also specified for digital output pins that can be set to a high-impedance state.

3.12.2 V_{IH}/V_{IL}

The input high voltage (V_{IH}) and input low voltage (V_{IL}) specify the threshold voltage for digital inputs. It is possible to search for these voltages using a binary search or step search, but it is more common to simply set the tester to force these levels into the device as a go/no-go test. If the device does not have adequate V_{IH} and V_{IL} thresholds, then the test program will fail one of the digital pattern tests that are used to verify the DUT's digital functionality. To allow a distinction between pattern failures caused by V_{IH}/V_{IL} settings and patterns failing for other reasons, the test engineer may add a second identical pattern test that uses more forgiving levels for V_{IH}/V_{IL}. If the digital pattern test fails with the specified V_{IH}/V_{IL} levels and passes with the less demanding settings, then V_{IH}/V_{IL} thresholds are the likely failure mode.

3.12.3 V_{OH}/V_{OL}

V_{OH} and V_{OL} are the output equivalent of V_{IH} and V_{IL}. V_{OH} is the minimum guaranteed voltage for an output when it is in the high state. V_{OL} is the maximum guaranteed voltage when the output is in the low state. These voltages are usually tested in two ways. First, they are measured at DC with the output pin set to static high/low levels. Sometimes a pin cannot be set to a static output level due poor design for test considerations, so only a dynamic test can be performed. Dynamic V_{OH}/V_{OL} testing is performed by setting the tester to expect high voltages above V_{OH} and low voltages below V_{OL}. The tester's digital electronics are able to verify these voltage levels as the outputs toggle during the digital pattern tests. Dynamic V_{OH}/V_{OL} testing is another go/no-go test approach, since the actual V_{OH}/V_{OL} voltages are verified but not measured.

3.12.4 I_{OH}/I_{OL}

V_{OH} and V_{OL} levels are guaranteed while the outputs are loaded with specified load currents, I_{OH} and I_{OL}. The tester must pull current out of the DUT pin when the output is high. This load current is called I_{OH}. Likewise, the tester forces the I_{OL} current into the pin when the pin is low. These currents are intended to force the digital outputs closer to their V_{OH}/V_{OL} specifications, making the V_{OH}/V_{OL} tests more difficult for the DUT to pass. I_{OH} and I_{OL} are forced using a diode bridge circuit in the tester's digital pin card electronics. The diode bridge circuit is discussed in more detail in Chapter 5, "Tester Hardware."

3.12.5 I_{OSH} and I_{OSL} Short Circuit Current

Digital outputs often include a current-limiting feature that protects the output pins from damage during short circuit conditions. If the output pin is shorted directly to ground or to a power supply pin, the protection circuits limit the amount of current flowing into or out of the pin. Short circuit current is measured by setting the output to a low state and forcing a high voltage

(usually V_{DD}) into the pin. The current flowing into the pin (I_{OSL}) is measured with one of the tester's current meters. Then the output is set to a high state and 0 V is forced at the pin. The current flowing out of the pin (I_{OSH}) is again measured with a current meter.

3.13 Summary

This chapter has presented only a few of the many DC tests and techniques the mixed-signal test engineer will encounter. Several chapters or perhaps even a whole book could be devoted to highly accurate DC test techniques. However, this book is intended to address mixed-signal testing. Hopefully, the limited examples given in this chapter will serve as a solid foundation from which the test engineer can build a more diversified DC measurement skill set.

DC measurements are trivial to define and understand, but they can sometimes be excruciatingly difficult to implement. A DC offset of 100 mV is very easy to measure if the required accuracy is ±10 mV. On the other hand if 1-μV accuracy is required, the test engineer may find this to be one of the more daunting test challenges in the entire project. The accuracy and repeatability requirements of seemingly simple tests like DC offset can present a far more challenging test problem than much more complicated AC tests.

Accuracy and repeatability of measurements is the subject of the next chapter. This topic pertains to a wide variety of analog and mixed-signal tests. Much of a test engineer's time is consumed by accuracy and repeatability problems. These problems can be one of the most aggravating aspects of mixed-signal testing. The successful resolution of a perplexing accuracy problem can also be one of the most satisfying parts of the test engineer's day.

Problems

3.1. The output of a 10-V voltage regulator varies from 9.95 V under no-load condition to 9.34 V under a 10-mA maximum rated load current. What is its load regulation?

3.2. The output of a 5-V voltage regulator varies from 4.86 to 4.32 V when the input voltage is changed from 14 to 6 V under a maximum load condition of 10 mA. What is its line regulation?

3.3. A 9-V voltage regulator is rated to have a load regulation of 150 mV for a maximum load current of 15 mA. Assuming a no-load output voltage of 9 V, what is the expected output voltage at the maximum load current?

3.4. A 6-V regulator has an output no-load voltage specification of 5.75 V (MIN) to 6.25 V (MAX), a load regulation specification of 150 mV (MAX) and a dropout voltage specification of 1.5 V (MAX). With a 7.5-V input voltage, what is the lowest output voltage that a passing regulator could produce under maximum loading conditions?

3.5. A voltage of 1.2 V is dropped across an input pin when a 100 μA current is forced into the pin. Subsequently, a 1.254-V level occurs when the current is increased to 200 μA. What is the input impedance?

3.6. The input pin of a device is characterized by the i-v relationship: $i = 0.001\ v \cdot 100$. What is the impedance seen looking into this pin?

3.7. Voltages of 1.2 and 3.3 V appear at the output of an amplfier when currents of −10 and +10 mA, respectively, are forced into its output. What is the output impedance?

3.8. The no-load output voltage of an amplifier is 4 V. When a 600-Ω load is attached to the output, the voltage drops to 3 V. What is the amplifier's output impedance?

3.9. For a ×10 amplifier characterized by $V_{OUT} = 10V_{IN} - V_{IN}^2 + 5$ over a ±15-V range, what are its input and output offset voltages?

3.10. A voltmeter introduces a measurement error of -5% while measuring a 1-V offset from an amplifier. What is the actual reading captured by the voltmeter?

3.11. A voltmeter with an input impedance of 500 kΩ is used to measure the DC output of an amplifier with an output impedance of 500 kΩ. What is the expected relative error made by this measurement?

3.12. A differential amplifier has outputs of 2.4 V (OUTP) and 2.7 V (OUTN) with its input set to a V_{MID} reference level of 2.5 V. What are the single-ended and differential offsets? The common-mode offset? (All offsets are to be measured with respect to V_{MID}.)

3.13. A perfectly linear amplifier has a measured gain of 5.1 V/V and an output offset of −3.2 V. What is the input offset voltage?

3.14. Voltages of 0.8 and 4.1 V appear at the output of a single-ended amplifier when inputs of 1.4 and 1.6 V are applied, respectively. What is the gain of the amplifier in V/V? What is the gain in decibels?

3.15. An amplifier is characterized by $V_{OUT} = 3.5V_{IN} + 1$ over the input voltage range 0 to 5 V. What is the amplifier output for a 2-V input? Similarly for a 3-V input? What is the corresponding gain of this amplifier in V/V over the 1-V swing? What is the gain in decibels?

3.16. An amplifier is characterized by $V_{OUT} = 1.5V_{IN} + 0.35V_{IN}^2 + 1$ over the input voltage range 0 to 5 V. What is the amplifier output for a 1-V input? Similarly for a 3-V input? What is the corresponding gain of this amplifier in V/V over the 1-V swing? What is the gain in decibels?

3.17. For the nulling amplifier setup shown in Figure 3.20 with R_1=100 Ω, R_2=200 kΩ, and R_3=50 kΩ, an SRC1 input swing of 1 V results in a 130-mV swing at the output of the nulling amplifier. What is the open-loop gain of the DUT amplifier in V/V? What is the gain in decibels?

3.18. For the nulling amplifier setup shown in Figure 3.20 with R_1=200 Ω, R_2=100 kΩ, and R_3=100 kΩ, and a V_{MID} of 2.5 V, an offset of 3.175 V (relative to ground) appears at the output of the nulling op amp when the input is set to V_{MID}. What is the input offset of the DUT amplifier?

3.19. For the nulling amplifier setup shown in Figure 3.20 with R_1=100 Ω, R_2=300 kΩ, and R_3=100 kΩ, and the DUT op amp having an open-loop gain of 1000 V/V, what is the output swing of the nulling amplifier when the input swings by 1 V?

3.20. The input of a ×10 amplifier is connected to a voltage source forcing 1.75 V. The power supply is set to 4.9 V and a voltage of 1.700 V is measured at the output of the amplifier. The power supply voltage is then changed to 5.1 V and the output measurement changes to 1.708 V. What is the PSS? What is the PSRR if the measured gain is 9.8 V/V?

3.21. For nulling amplifier CMRR setup shown in Figure 3.23 with R_1=100 Ω, R_2=300 kΩ, and R_3=100 k Ω, SRC1 is set to +3.5 V and a differential voltage of 130 mV is measured between SRC1 and the output of the nulling amplifier. Then SRC1 is set to 1.0 V and the measured voltage changes to –260 mV. What is the CMRR of the op amp in decibels?

3.22. An amplifier has an expected CMRR of -85 dB. For a 1-V change in the input common-mode level, what is the expected change in the input offset voltage of this amplifier?

3.23. A comparator has an input offset voltage of 6 mV and its negative terminal is connected to a 2.5-V level, at what voltage on the positive terminal does the comparator change state?

3.24. A slicer circuit is connected to a 2-V reference and has a threshold voltage error of 20 mV, at what voltage level will the slicer change state?

3.25. If a slicer's 2.5-V reference has an error of +100 mV and the comparator has an input offset of –10 mV, what threshold voltage should we expect?

3.26. A comparator has a measured hysteresis of 10 mV and switches state on a rising input at 2.5 V. At what voltage does the comparator change to a low state on a falling input?

3.27. For an amplifier characterized by $V_{OUT} = 6V_{IN} + 0.5V_{IN}^2 - 2$ over a ±1-V input voltage range, determine the input offset voltage using a linear search process, starting with two points at ±1 V. After how many iterations did the answer change by less than 1 mV? How many iterations would have been required using a binary search from –1 to +1 V?

References

1. Sreejit Chakravarty, Paul J. Thadikaran, *Introduction to IDDQ Testing*, May, 1997, Kluwer Academic Publishers, Boston, MA, ISBN: 0792399455

2. Analog Devices application note*, *How to Test Basic Operational Amplifier Parameters*, Analog Devices, Inc., Norwood, MA, July, 1982

* The nulling amplifier/servo loop methods presented in this chapter were adapted from the referenced application note to allow compatibility with single-supply op amps having a V_{GND} reference voltage. The technique has been presented with permission from Analog Devices, Inc.

CHAPTER 4

Measurement Accuracy

4.1 Terminology

4.1.1 Accuracy and Precision

In conversational English, the terms *accuracy* and *precision* are virtually identical in meaning. Roget's Thesaurus[1] lists these words as synonyms and Webster's Dictionary[2] gives almost identical definitions for them. However, these terms are defined very differently in engineering textbooks[3-5]. Combining the definitions from these and other sources gives us an idea of the accepted technical meaning of the words:

> Accuracy – The difference between the average of measurements and a standard sample for which the "true" value is known. The degree of conformance of a test instrument to absolute standards, usually expressed as a percentage of reading or a percentage of measurement range (full scale).
>
> Precision – The variation of a measurement system obtained by repeating measurements on the same sample back-to-back using the same measurement conditions.

According to these definitions, precision refers only to the repeatability of a series of measurements. It does not refer to consistent errors in the measurements. A series of measurements can be incorrect by 2 V, but as long as they are consistently wrong by the same amount, then the measurements are considered to be precise.

This definition of precision is somewhat counterintuitive to most people, since the words *precision* and *accuracy* are so often used synonymously. Few of us would be impressed by a "precision" voltmeter exhibiting a consistent 2-V error! Fortunately, the word *repeatability* is far more commonly used in the test engineering field than the word *precision*. This textbook will use the term *accuracy* to refer to the overall closeness of an averaged measurement to the true value and *repeatability* to refer to the consistency with which that measurement can be made. The word *precision* will be avoided.

Unfortunately, the definition of accuracy is also somewhat ambiguous. Many sources of error can affect the accuracy of a given measurement. The accuracy of a measurement should probably refer to all possible sources of error. However, the accuracy of an instrument (as distinguished from the accuracy of a measurement) is often specified in the absence of repeatability fluctuations and instrument resolution limitations. Rather than trying to decide which of the various error sources are included in the definition of accuracy, it is probably more useful to discuss some of the common error components that contribute to measurement

inaccuracy. It is incumbent upon the test engineer to make sure all components of error have been accounted for in a given specification of accuracy.

4.1.2 Systematic Errors

Systematic errors are those that show up consistently from measurement to measurement. For example, assume an amplifier's output exhibits an offset of 100 mV from the ideal value of 0 V. Using a digital voltmeter (DVM) we could take multiple readings of the offset over time and record each measurement. A typical measurement series might look like this:

101 mV, 103 mV, 102 mV, 101 mV, 102 mV, 103 mV, 103 mV, 101 mV, 102 mV...

This measurement series shows an average error of about 2 mV from the true value of 100 mV. Errors like this are caused by consistent errors in the measurement instruments. The errors can result from a combination of many things, including DC offsets, gain errors, and nonideal linearity in the DVM's measurement circuits. Systematic errors can often be reduced through a process called *calibration*. Various types of calibration will be discussed in more detail in Section 4.2.

4.1.3 Random Errors

Notice in the preceding example that the measurements are not repeatable. The DVM gives readings from 101 to 103 mV. Such variations do not surprise most engineers because DVMs are relatively inexpensive. On the other hand, when a two million dollar piece of ATE equipment cannot produce the same answer twice in a row, eyebrows may be raised.

Inexperienced test engineers are sometimes surprised to learn that an expensive tester cannot give perfectly repeatable answers. They may be inclined to believe that the tester software is defective when it fails to produce the same result every time the program is executed. However, experienced test engineers recognize that a certain amount of random error is to be expected in analog and mixed-signal measurements.

Random errors are usually caused by thermal noise or other noise sources in either the DUT or the tester hardware. One of the biggest challenges in mixed-signal testing is determining whether the random errors are caused by bad DIB design, by bad DUT design, or by the tester itself. If the source of error is found and cannot be corrected by a design change, then averaging or filtering of measurements may be required. Averaging and filtering are discussed in more detail in Section 4.3.

4.1.4 Resolution (Quantization Error)

In the 100-mV measurement list, notice that the measurements are always rounded off to the nearest millivolt. The measurement may have been rounded off by the person taking the measurements, or perhaps the DVM was only capable of displaying three digits. ATE measurement instruments have similar limitations in measurement resolution. Limited resolution results from the fact that continuous analog signals must first be converted into a digital format before the ATE computer can evaluate the test results. The tester converts analog signals into digital form using analog-to-digital converters (ADCs).

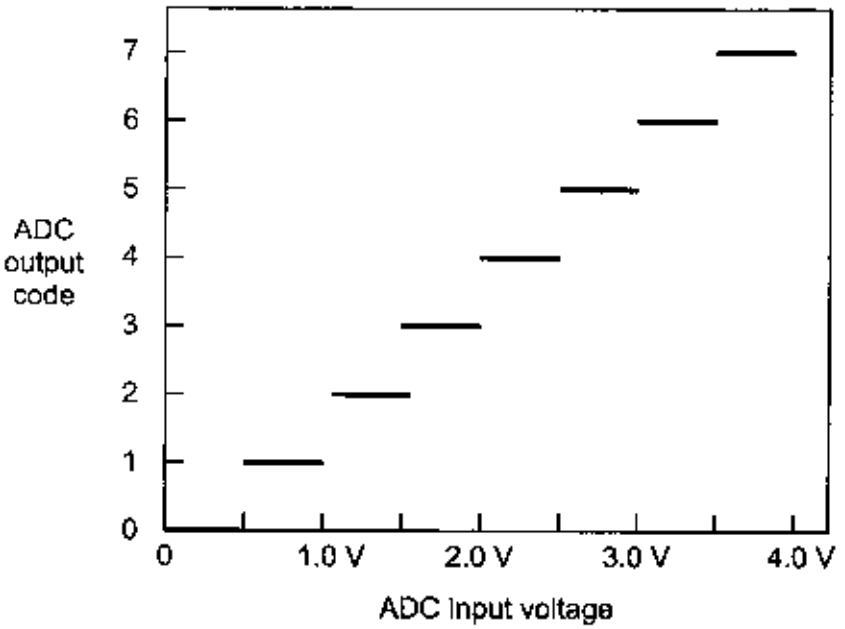

Figure 4.1. Output codes versus input voltages for an ideal 3-bit ADC.

ADCs by nature exhibit a feature called *quantization error*. Quantization error is a result of the conversion from an infinitely variable input voltage (or current) to a finite set of possible digital output results from the ADC. Figure 4.1 shows the relationship between input voltages and output codes for an ideal 3-bit ADC. Notice that an input voltage of 1.2 V results in the same ADC output code as an input voltage of 1.3 V. In fact, any voltage from 1.0 to 1.5 V will produce an output code of 2.

If this ADC were part of a crude DC voltmeter, the meter would produce an output reading of 1.25 V any time the input voltage falls between 1.0 and 1.5 V. This inherent error in ADCs and measurement instruments is caused by quantization error. The resolution of a DC meter is often limited by the quantization error of its ADC circuits.

If a meter has 12 bits of resolution, that means it can resolve a voltage to one part in 2^{12}-1 (one part in 4095). If the meter's full-scale range is set to ±2 V, then a resolution of approximately 1 mV can be achieved (4 V / 4095 levels). This does not automatically mean that the meter is accurate to 1 mV, it simply means the meter cannot resolve variations in input voltage smaller than 1 mV. An instrument's resolution can far exceed its accuracy. For example, a 23-bit voltmeter might be able to produce a measurement with a 1-μV resolution, but it may have a systematic error of 2 mV.

4.1.5 Repeatability

Nonrepeatable answers are a fact of life for mixed-signal test engineers. A large portion of the time required to debug a mixed-signal test program can be spent tracking down the various sources of poor repeatability. Since all electrical circuits generate a certain amount of random noise, measurements such as those in the 100-mV offset example are fairly common. In fact, if a test engineer gets the same answer 10 times in a row, it is time to start looking for a problem. Most likely, the tester instrument's full-scale voltage range has been set too high, resulting in a

measurement resolution problem. For example, if we configured a meter to a range having a 10-mV resolution, then our measurements from the prior example would be very repeatable (100 mV, 100 mV, 100 mV, 100 mV, etc.). A novice test engineer might think this is a terrific result, but the meter is just rounding off the answer to the nearest 10-mV increment due to an input ranging problem. Unfortunately, a voltage of 104 mV would also have resulted in this same series of perfectly repeatable, perfectly incorrect measurement results. Repeatability is desirable, but it does not in itself guarantee accuracy.

Exercises

4.1. A 5-mV signal is measured with a meter ten times resulting in the following sequence of readings: 5 mV, 6 mV, 9 mV, 8 mV, 4 mV, 7 mV, 5 mV, 7 mV, 8 mV, 11 mV. What is the average measured value? What is the systematic error?

Ans. 7 mV, 2 mV.

4.2. A meter is rated at 8-bits and has a full-scale range of ±5 V. What is the measurement uncertainty of this meter, assuming only quantization errors from an ideal meter ADC?

Ans. ± 19.5 mV.

4.3. A signal is to be measured with a maximum uncertainty of ±0.5 μV. How many bits of resolution are required by an ideal meter having a ±1 V full-scale range?

Ans. 21 bits.

4.1.6 Stability

A measurement instrument's performance may drift with time, temperature, and humidity. The degree to which a series of supposedly identical measurements remains constant over time, temperature, humidity, and all other time-varying factors is referred to as *stability*. Stability is an essential requirement for accurate instrumentation.

Shifts in the electrical performance of measurement circuits can lead to errors in the tested results. Most shifts in performance are caused by temperature variations. Testers are usually equipped with temperature sensors that can automatically determine when a temperature shift has occurred. The tester must be recalibrated anytime the ambient temperature has shifted by a few degrees. The calibration process brings the tester instruments back into alignment with known electrical standards so that measurement accuracy can be maintained at all times.

After the tester is powered up, the tester's circuits must be allowed to stabilize to a constant temperature before calibrations can occur. Otherwise, the measurements will drift over time as the tester heats up. When the tester chassis is opened for maintenance or when the test head is opened up or powered down for an extended period, the temperature of the measurement electronics will typically drop. Calibrations then have to be rerun once the tester recovers to a stable temperature.

Shifts in performance can also be caused by aging electrical components. These changes are typically much slower than shifts due to temperature. The same calibration processes used to

account for temperature shifts can easily accommodate shifts of components caused by aging. Shifts caused by humidity are less common, but can also be compensated for by periodic calibrations.

4.1.7 Correlation

Correlation is another activity that consumes a great deal of mixed-signal test program debug time. Correlation is the ability to get the same answer using different pieces of hardware or software. It can be extremely frustrating to try to get the same answer on two different pieces of equipment using two different test programs. It can be even more frustrating when two supposedly identical pieces of test equipment running the same program give two different answers.

Of course correlation is seldom perfect, but how good is good enough? In general, it is a good idea to make sure the correlation errors are less than one-tenth of the full range between the minimum test limit and the maximum test limit. However, this is just a rule of thumb. The exact requirements will differ from one test to the next. Whatever correlation errors exist, they must be considered part of the measurement uncertainty, along with nonrepeatability and systematic errors.

The test engineer must consider several categories of correlation. Test results from a mixed-signal test program cannot be fully trusted until the various types of correlation have been verified. The more common types of correlation include tester-to-bench, tester-to-tester, program-to-program, DIB-to-DIB, and day-to-day correlation.

Tester-to-Bench Correlation

Often, a customer will construct a test fixture using bench instruments to evaluate the quality of the device under test. Bench equipment such as oscilloscopes and spectrum analyzers can help validate the accuracy of the ATE tester's measurements. Bench correlation is a good idea, since ATE testers and test programs often produce incorrect results in the early stages of debug. In addition, IC design engineers often build their own evaluation test setups to allow quick debug of device problems. Each of these test setups must correlate to the answers given by the ATE tester. Often the tester is correct and the bench is not. Other times, test program problems are uncovered when the ATE results do not agree with a bench setup. The test engineer will often need to help debug the bench setup to get to the bottom of correlation errors between the tester and the bench.

Tester-to-Tester Correlation

Sometimes a test program will work on one tester, but not on another presumably identical tester. The differences between testers may be catastrophically different, or they may be very subtle. The test engineer should compare all the test results on one tester to the test results obtained using other testers. Only after all the testers agree on all tests is the test program and test hardware debugged and ready for production.

Similar correlation problems arise when an existing test program is ported from one tester type to another. Often, the testers are neither software compatible nor hardware compatible with one another. In fact, the two testers may not even be manufactured by the same ATE vendor. A myriad of correlation problems can arise because of the vast differences in DIB layout and tester

software between different tester types. To some extent, the architecture of each tester will determine the best test methodology for a particular measurement. A given test may have to be executed in a very different manner on one tester versus another. Any difference in the way a measurement is taken can affect the results. For this reason, correlation between two different test approaches can be very difficult to achieve. Conversion of a test program from one type of tester to another can be one of the most daunting tasks a mixed-signal test engineer faces.

Program-to-Program Correlation

When a test program is streamlined to reduce test time, the faster program must be correlated to the original program to make sure no significant shifts in measurement results have occurred. Often, the test reduction techniques cause measurement errors because of reduced DUT settling time and other timing-related issues. These correlation errors must be resolved before the faster program can be released into production.

DIB-to-DIB Correlation

No two DIBs are identical, and sometimes the differences cause correlation errors. The test engineer should always check to make sure that the answers obtained on multiple DIB boards agree. DIB correlation errors can often be corrected by *focused calibration* software written by the test engineer (this will be discussed further in Section 4.2 and in Chapter 10, "Focused Calibrations").

Day-to-Day Correlation

Correlation of the same DIB and tester over a period of time is also important. If the tester and DIB have been properly calibrated, there should be no drift in the answers from one day to the next. Subtle errors in software and hardware often remain hidden until day-to-day correlation is performed. The usual solution to this type of correlation problem is to improve the focused calibration process.

4.1.8 Reproducibility

The term *reproducibility* is often used interchangeably with *repeatability*, but this is not a correct usage of the term. The difference between reproducibility and repeatability relates to the effects of correlation and stability on a series of supposedly identical measurements. Repeatability is most often used to describe the ability of a single tester and DIB board to get the same answer multiple times as the test program is repetitively executed.

Reproducibility, by contrast, is the ability to achieve the same measurement result on a given DUT using any combination of equipment and personnel at any given time. It is defined as the statistical deviation of a series of supposedly identical measurements taken over a period of time. These measurements are taken using various combinations of test conditions that ideally should not change the measurement result. For example, the choice of equipment operator, tester, DIB board, etc., should not affect any measurement result.

Consider the case in which a measurement is highly repeatable, but not reproducible. In such a case, the test program may consistently pass a particular DUT on a given day, and yet consistently fail the same DUT on another day or on another tester. Clearly, measurements must be both repeatable and reproducible to be production-worthy.

4.2 Calibrations and Checkers

4.2.1 Traceability to Standards

Every tester and bench instrument must ultimately correlate to standards maintained by a central authority, such as the National Institute of Standards and Technology (NIST). In the United States, this government agency is responsible for maintaining the standards for pounds, gallons, inches, and electrical units such as volts, amperes, and ohms. The chain of correlation between the NIST and the tester's measurements involves a series of calibration steps that transfers the "golden" standards of the NIST to the tester's measurement instruments.

Many testers have a centralized standards reference, which is a thermally stabilized instrument in the tester mainframe. The standards reference is periodically replaced by a freshly calibrated reference source. The old one is sent back to a certified calibration laboratory, which recalibrates the reference so that it agrees with NIST standards. Similarly, bench instruments are periodically recalibrated so that they too are traceable to the NIST standards. By periodically refreshing the tester's traceability link to the NIST, all testers and bench instruments can be made to agree with one another.

4.2.2 Hardware Calibration

Hardware calibration is a process of physical "knob tweaking" that brings a piece of measurement instrumentation back into agreement with calibration standards. For instance, oscilloscope probes often include a small screw that can be used to nullify the overshoot in rapidly rising digital edges. This is one common example of hardware calibration.

One major problem with hardware calibration is that it is not a convenient process. It generally requires a manual adjustment of a screw or knob. Robotic screwdrivers might be employed to allow partial automation of the hardware calibration process. However, the use of robotics is an elaborate solution to the calibration problem. Full automation can be achieved using a simpler procedure known as *software calibration*.

4.2.3 Software Calibration

Using software calibration, ATE testers are able to correct hardware errors without adjusting any physical knobs. The basic idea behind software calibration is to separate the instrument's ideal operation from its nonidealities. Then a *model* of the instrument's nonideal operation can be constructed, followed by a *correction* of the nonideal behavior using a mathematical routine written in software. Figure 4.2 illustrates this idea for a voltmeter.

In part (a) a "real" voltmeter is modeled as a cascade of two parts: (1) an ideal voltmeter, and (2) a black box that relates the voltage across its input terminals v_{DUT} to the voltage that is measured by the ideal voltmeter, $v_{measured}$. This relationship can be expressed in more mathematical terms as

$$v_{measured} = f\left(v_{DUT}\right) \tag{4.1}$$

where $f(\cdot)$ indicates the functional relationship between $v_{measured}$ and v_{DUT}.

The true functional behavior $f(\cdot)$ is seldom known; so one assumes a particular behavior or model, such as a first-order model given by

$$v_{measured} = Gv_{DUT} + offset \tag{4.2}$$

where G and *offset* are the gain and offset of the voltmeter, respectively. These values must be determined from measured data. Subsequently, a mathematical procedure is written in software that performs the inverse mathematical operation

$$v_{calibrated} = f^{-1}(v_{measured}) \tag{4.3}$$

where $v_{calibrated}$ replaces v_{DUT} as an estimate of the true voltage that appears across the terminals of the voltmeter as depicted in Figure 4.2(b). If $f(\cdot)$ is known precisely, then $v_{calibrated} = v_{DUT}$.

In order to establish an accurate model of an instrument, precise reference levels are necessary. The number of reference levels required to characterize the model fully will depend on its order, that is, the number of parameters used to describe the model. For the linear or first-order model described, it has two parameters, G and *offset*. Hence, two reference levels will be required.

To avoid conflict with the meter's normal operation, relays are used to switch in these reference levels during the calibration phase. For example, the voltmeter in Figure 4.3 includes a pair of calibration relays, which can connect the input to two separate reference levels, V_{ref1} and V_{ref2}. During a system level calibration, the tester closes one relay and connects the voltmeter to

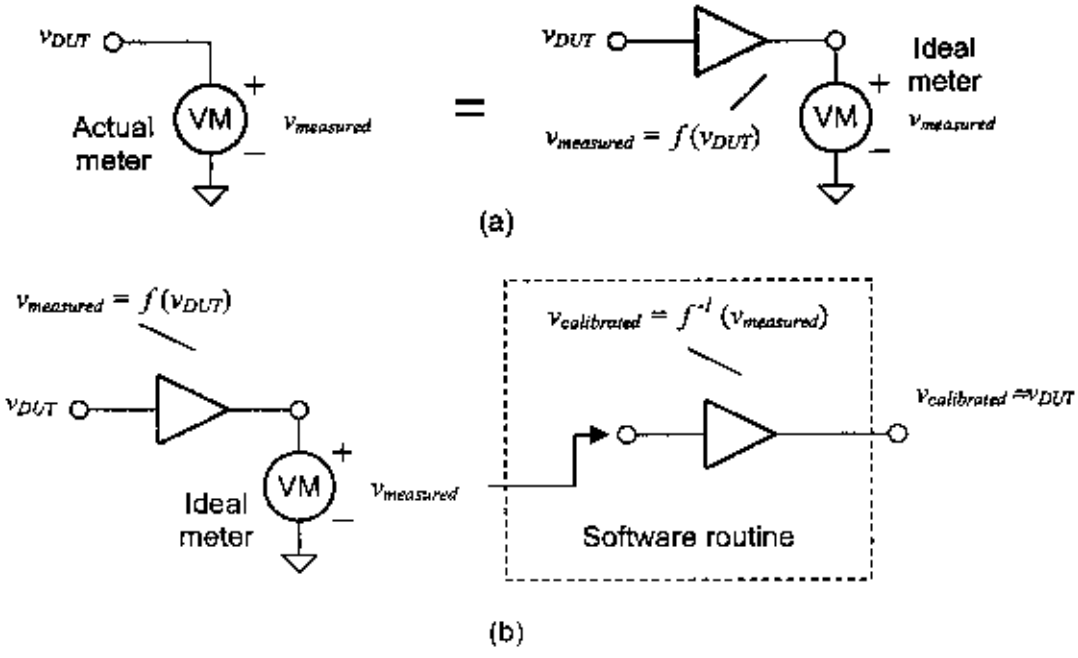

Figure 4.2. (a) Modeling a voltmeter with an ideal voltmeter and a nonideal component in cascade. (b) Calibrating the nonideal effects using a software routine.

V_{ref1} and measures the voltage, which we shall denote as $v_{measured1}$. Subsequently, this process is repeated for the second reference level V_{ref2} and the voltmeter provides a second reading, $v_{measured2}$.

Based on the assumed linear model for the voltmeter, we can write two equations in terms of two unknowns

$$\begin{aligned} v_{measured1} &= GV_{ref1} + offset \\ v_{measured2} &= GV_{ref2} + offset \end{aligned} \tag{4.4}$$

Using linear algebra (Gauss-Jordan elimination method), the two model parameters can then be solved to be

$$G = \frac{v_{measured2} - v_{measured1}}{V_{ref2} - V_{ref1}} \tag{4.5}$$

and

$$offset = \frac{v_{measured1}V_{ref2} - v_{measured2}V_{ref1}}{V_{ref2} - V_{ref1}} \tag{4.6}$$

The parameters of the model, G and *offset*, are also known as *calibration factors*, or cal factors for short.

When subsequent DC measurements are performed, they are corrected using the stored calibration factors according to

$$v_{calibrated} = \frac{v_{measured} - offset}{G} \tag{4.7}$$

This expression is found by isolating v_{DUT} on one side of the expression in Eq. (4.2) and replacing it by $v_{calibrated}$.

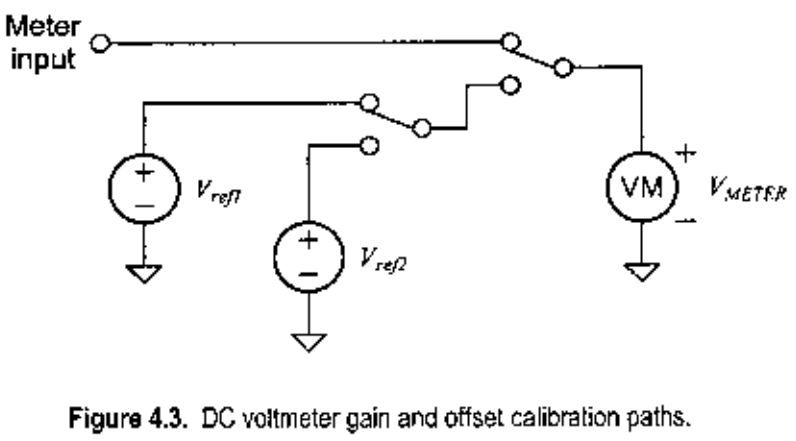

Figure 4.3. DC voltmeter gain and offset calibration paths.

Of course, this example is only for purposes of illustration. Most testers use much more elaborate calibration schemes to account for linearity errors and other nonideal behavior in the meter's ADC and associated circuits.. Also, the meter's input stage can be configured many ways, and each of these possible configurations needs a separate set of calibration factors. For example, if the input stage has ten different input ranges, then each range setting requires a separate set of calibration factors. Fortunately for the test engineer, most instrument calibrations happen behind the scenes. The calibration factors are measured and stored automatically during the tester's periodic system calibration and checker process.

Exercises

4.4. A meter reads 0.5 mV and 1.1 V when connected to two precision reference levels of 0 and 1 V, respectively. What are the offset and gain of this meter? Write the calibration equation for this meter.

Ans. 0.5 mV, 1.0995 V/V, $v_{calibrated} = (v_{measured} - 0.5\text{ mV})/1.0995$.

4.5. A meter is assumed characterized by a second-order equation of the form: $v_{measured} = offset + G_1 v_{calibrated} + G_2 v_{calibrated}^2$. How many precision DC reference levels are required to obtain the parameters of this second-order expression?

Ans. Three.

4.6. A meter is assumed characterized by a second-order equation of the form: $v_{measured} = offset + G_1 v_{calibrated} + G_2 v_{calibrated}^2$. Write the calibration equation for this meter in terms of the unknown calibration factors.

Ans. $v_{calibrated} = \dfrac{-G_1 + \sqrt{G_1^2 + 4G_2 v_{measured}}}{2G_2}$ or $v_{calibrated} = \dfrac{-G_1 - \sqrt{G_1^2 + 4G_2 v_{measured}}}{2G_2}$

depending on the data conditions.

4.2.4 System Calibrations and Checkers

Testers are calibrated on a regular basis to maintain traceability of each instrument to the tester's calibration reference source. In addition to calibrations, software is also executed to verify the functionality of hardware and make sure it is production worthy. This software is called a *checker program*, or *checker* for short. Often calibrations and checkers are executed in the same program. If a checker fails, the repair and maintenance (R&M) staff replaces the failing tester module with a good one. After replacement, the new module must be completely recalibrated.

There are several types of calibrations and checkers. These include calibration reference source replacement, performance verification (PV), periodic system calibrations and checkers, instrument calibrations at load time, and focused calibrations. Calibration reference source replacement and recalibration was discussed in Section 4.2.1. A common replacement cycle time for calibration sources is once every six months.

To verify that the tester is in compliance with all its published specifications, a more extensive process called *performance verification* may be performed. Although full performance verification is typically performed at the tester vendor's production floor, it is seldom performed on the production floor. By contrast, periodic system calibrations and checkers are performed on a regular basis in a production environment. These software calibration and checker programs verify that all the system hardware is production worthy.

Since tester instrumentation may drift slightly between system calibrations, the tester may also perform a series of fine-tuning calibrations each time a new test program is loaded. The extra calibrations can be limited to the subset of instruments used in a particular test program. This helps to minimize program load time. To maintain accuracy throughout the day, these calibrations may be repeated on a periodic basis after the program has been loaded. They may also be executed automatically if the tester temperature drifts by more than a few degrees.

Finally, focused calibrations are often required to achieve maximum accuracy and to compensate for nonidealities of DIB board components such as buffer amplifiers and filters. Unlike the ATE tester's built-in system calibrations, focused calibration and checker software is the responsibility of the test engineer. Focused calibrations fall into two categories: (1) focused instrument calibrations and (2) focused DIB calibrations and checkers.

4.2.5 Focused Instrument Calibrations

Testers typically contain a combination of slow, accurate instruments and fast instruments that may be less accurate. The accuracy of the faster instruments can be improved by periodically referencing them back to the slower more accurate instruments through a process called *focused calibration*. Focused calibration is not always necessary. However, it may be required if the test engineer needs higher accuracy than the instrument is able to provide using the built-in calibrations of the tester's operating system.

A simple example of focused instrument calibration is a DC source calibration. The DC sources in a tester are generally quite accurate, but occasionally they need to be set with minimal DC level error. A calibration routine that determines the error in a DC source's output level can be added to the first run of the test program. A high-accuracy DC voltmeter can be used to measure the actual output of the DC source. If the source is in error by 1 mV, for instance, then the requested voltage is reduced by 1 mV and the output is retested. It may take several iterations to achieve the desired value with an acceptable level of accuracy.

A similar approach can be extended to the generation of a sinusoidal signal requiring an accurate RMS value from an arbitrary waveform generator (AWG). A high-accuracy AC voltmeter is used to measure the RMS value from the AWG. The discrepancy between the measured value and the desired value is then used to adjust the programmed AWG signal level. The AWG output level will thus converge toward the desired RMS level as each iteration is executed.

Example 4.1

A 2.500-V signal is required from a DC source as shown in Figure 4.4. Describe a calibration procedure that can be used to ensure that 2.500 V ± 500 μV does indeed appear at the output of the DC source.

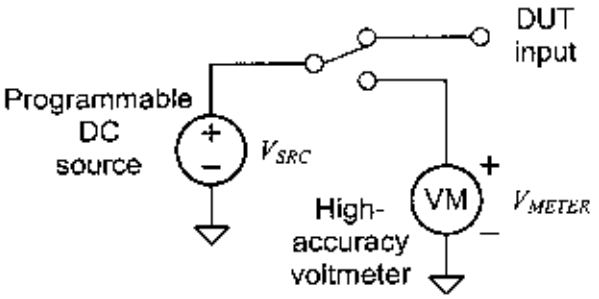

Figure 4.4. DC source focused calibration.

olution:

The source is set to 2.500 V and a high-accuracy voltmeter is connected to the output of the source using a calibration path internal to the tester. Calibration path connections are made through one or more relays such as the ones in Figure 4.3. Assume the high-accuracy voltmeter reads 2.510 V from the source. The source is then reprogrammed to 2.500 V - 10 mV and the output is remeasured. If the second meter reading is 2.499 V, then the source is reprogrammed to 2.500 V - 10 mV + 1 mV and measured again. This process is repeated until the meter reads 2.500 V (plus or minus 500 μV). Once the exact programmed level is established, it is stored as a calibration factor (e.g., calibration factor = 2.500 V - 10 mV + 1 mV = 2.491 V). When the 2.500-V DC level is required during subsequent program executions, the 2.491-V calibration factor is used as the programmed level rather than 2.500 V. Test time is not wasted searching for the ideal level after the first calibration is performed. However, calibration factors may need to be regenerated every few hours to account for slow drifts in the DC source. This recalibration interval is dependent on the type of tester used.

Another application of focused instrument calibration is spectral leveling of the output of an AWG. An important application of AWGs is to provide a composite signal consisting of N sine waves or *tones* all having equal amplitude at various frequencies and arbitrary phase. Such waveforms are in a class of signals commonly referred to as *multitone* signals. Mathematically a multitone signal $y(t)$ can be written as

$$\begin{aligned} y(t) &= A_0 + A_1 \sin(2\pi f_1 t + \phi_1) + \cdots + A_N \sin(2\pi f_N t + \phi_N) \\ &= A_0 + \sum_{k=1}^{N} A_k \sin(2\pi f_k t + \phi_k) \end{aligned} \tag{4.8}$$

where A_k, f_k, and ϕ_k denotes the amplitude, frequency, and phase, respectively, of the kth tone. A multitone signal can be viewed in either the time domain or in the frequency domain. Time-domain views are analogous to oscilloscope traces, while frequency-domain views are analogous to spectrum analyzer plots. The frequency-domain graph of a multitone signal contains a series of vertical lines corresponding to each tone frequency and whose length* represents the root-

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* Spectral density plots are commonly defined in engineering textbooks with the length of the spectral line representing one-half the amplitude of a tone. In most test engineering work, including spectrum analyzer displays, it is more common to find this length defined as an RMS quantity.

mean-square (RMS) amplitude of the corresponding tone. Each line is referred to as a *spectral line*. Figure 4.5 illustrates the time and frequency plots of a composite signal consisting of three tones of frequencies 1, 2.5 and 4.1 kHz, all having an RMS amplitude of 2 V. Of course, the peak amplitude of each sinusoid in the multitone is simply $\sqrt{2}\times 2$ or 2.82 V, so we could just as easily plot these values as peak amplitudes rather than RMS. This book will consistently display frequency-domain plots using RMS amplitudes.

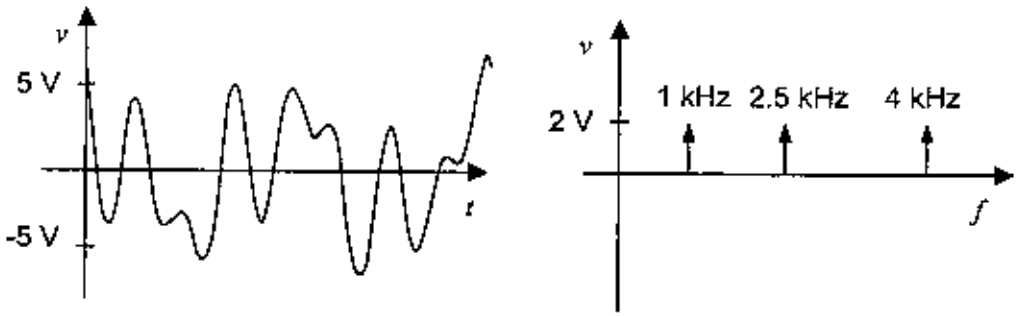

Figure 4.5. Time-domain and frequency-domain views of a three-tone multitone.

The AWG produces its output signal by passing the output of a DAC through a low-pass anti-imaging filter. Due to its frequency behavior, the filter will not have a perfectly flat magnitude response. The DAC may also introduce frequency-dependent errors. Thus the amplitudes of the individual tones may be offset from their desired levels. We can therefore model this AWG multitone situation as illustrated in Figure 4.6. The model consists of an ideal source connected in cascade with a linear block whose gain or magnitude response is described by $G(f)$, where f is the frequency expressed in Hz. To correct for the gain change with frequency, the amplitude of each tone from the AWG is measured individually using a high-accuracy AC voltmeter. The ratio between the actual output and the requested output corresponds to $G(f)$ at that frequency. This gain can then be stored as a calibration factor that can subsequently be retrieved to correct the amplitude error at that frequency. The calibration process is repeated for each tone in the multitone signal. The composite signal can then be generated with corrected amplitudes by dividing the previous requested amplitude at each frequency by the corresponding AWG gain calibration factor. Because the calibration process equalizes the amplitudes of each tone, the process is called *multitone leveling*.

As testers continue to evolve and improve, it may become increasingly unnecessary for the test engineer to perform focused calibrations of the tester instruments. Focused calibrations were once necessary on almost all tests in a test program. Today, they can sometimes be omitted with little degradation in accuracy. Nevertheless, the test engineer must evaluate the need for focused

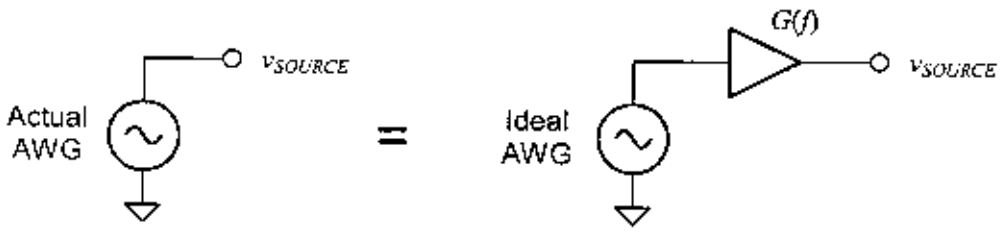

Figure 4.6. Modeling an AWG as a cascaded combination of an ideal source and frequency-dependent gain block.

calibrations on each test. Even if calibrations become unnecessary in the future, the test engineer should still understand the methodology so that test programs on older equipment can be comprehended.

Calibration of circuits on the DIB, on the other hand, will probably always be required. The tester vendor has no way to predict what kind of buffer amplifiers and other circuits will be placed on the DIB board. The tester operating system will never be able to provide automatic calibration of these circuits. The test engineer is fully responsible for understanding the calibration requirements of all DIB circuits.

Example 4.2

A multitone signal consisting of three tones at 1.0, 2.5, and 4.1 kHz is desired from an AWG. Each tone should have exact RMS amplitude of 2.0 V, corresponding to a peak amplitude of $\sqrt{2}\times 2.0$ V. This multitone should have 0 DC offset. Using Eq. (4.8), a three-tone signal is mathematically created with parameters $A_0 = 0$, $A_1 = A_2 = A_3 = \sqrt{2}\times 2$, $f_1 = 1$ kHz, $f_2 = 2.5$ kHz, $f_3 = 4.1$ kHz and is written as

$$y(t) = 2\sqrt{2}\sin(2\pi\times 1\text{ kHz}\times t) + 2\sqrt{2}\sin(2\pi\times 2.5\text{ kHz}\times t) + 2\sqrt{2}\sin(2\pi\times 4.1\text{ kHz}\times t)$$

Sequentially, beginning with the lowest-frequency tone and progressing up in frequency, each tone is loaded into the AWG and the sine wave is passed from the AWG into a high-accuracy AC RMS voltmeter. For each tone, the voltmeter reads: 1.980, 2.023 and 1.950 V. Compute the calibration factors and provide a formula that describes the modified three-tone signal.

Solution:

Three calibration factors are calculated as the ratio of the measured signal to the desired signal

$$cal_1 = G(1\text{ kHz}) = \frac{1.980\text{ V}}{2.0\text{ V}} = 0.99\text{ V/V}$$

$$cal_2 = G(2.5\text{ kHz}) = \frac{2.023\text{ V}}{2.0\text{ V}} = 1.012\text{ V/V}$$

$$cal_3 = G(4.1\text{ kHz}) = \frac{1.950\text{ V}}{2.0\text{ V}} = 0.975\text{ V/V}$$

As long as the AWG is linear, it should be possible to get exactly 2.0 V at each tone by asking for 2.0 V divided by the appropriate calibration factor. The three-tone signal is thus created using the equation

$$y(t) = \frac{2\sqrt{2}}{cal_1}\sin(2\pi\times 1\text{ kHz}\times t) + \frac{2\sqrt{2}}{cal_2}\sin(2\pi\times 2.5\text{ kHz}\times t) + \frac{2\sqrt{2}}{cal_3}\sin(2\pi\times 4.1\text{ kHz}\times t)$$

This waveform is loaded into the AWG and the three-tone signal is produced with equal levels of 2.0 V RMS per tone.

4.2.6 Focused DIB Circuit Calibrations

Often circuits are added to a DIB board to improve the accuracy of a particular test or to buffer the weak output of a device before sending it to the tester electronics. As the signal-conditioning DIB circuitry is added in cascade with the test instrument, a model of the test setup is identical to that given in Figure 4.2(a). The only difference is that functional block $v_{measured} = f(v_{DUT})$ includes both the meter and the DIB's behavior. As a result, the focused instrument calibrations of Section 4.2.3 can be used with no modifications. Conversely, the meter may already have been calibrated so that the functional block $f(\cdot)$ covers the DIB circuitry only. One must keep track of the extent of the calibration to avoid any double counting.

Example 4.3

The op amp in Figure 4.7 has been added to a DIB board to buffer an output of a DUT. The buffer will be used to condition the DC signal from the DUT before sending it to a calibrated DC voltmeter resident in the tester. If the output is not buffered, then we may find that the DUT breaks into oscillations as a result of the stray capacitance arising along the lengthy signal path leading from the DUT to the tester. The buffer prevents these oscillations by substantially reducing stray capacitance at the DUT output. In order to perform an accurate measurement, the behavior of the buffer must be accounted for. Outline the steps to perform a focused DC calibration on the op amp buffer stage.

Solution:

To perform a DC calibration of the output buffer amplifier it is necessary to assume a model for the op amp buffer stage. It is reasonable to assume that the buffer is fairly linear over a wide range of signal levels, so that the following linear model can be used

$$v_{measured} = Gv_{DUT} + offset$$

Subsequently, following the same procedure as outlined in Section 4.2.3, a pair of known voltages are applied to the input of the buffer from source SRC1 via the relay connection and the output of the buffer is measured with a voltmeter. This temporary connection is called a *calibration path*. As an example, let SRC1 force 2 V and assume that an output voltage of 2.023 V is measured using the voltmeter. Next the input is dropped to 1 V, resulting in an output

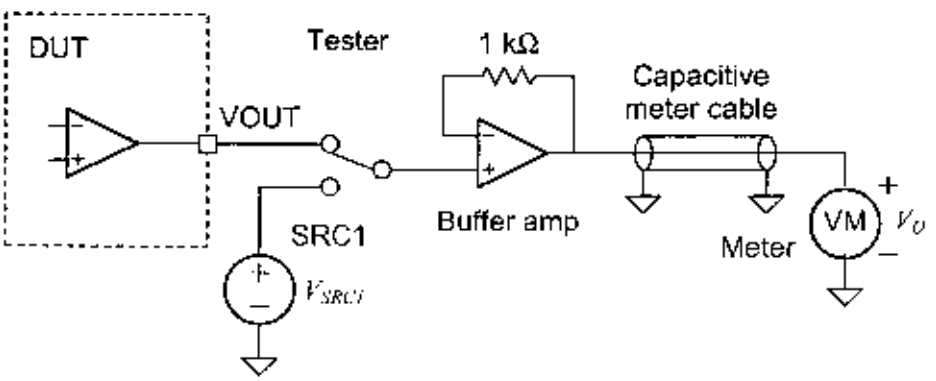

Figure 4.7. DC calibration for op amp buffer circuit.

voltage of 1.012 V. Using Eq. (4.5), we find the buffer has gain given by

$$G = \frac{2.023\ \text{V} - 1.012\ \text{V}}{2\ \text{V} - 1\ \text{V}} = 1.011\ \text{V/V}$$

and the offset is found from Eq. (4.6) to be

$$offset = \frac{1.012\ \text{V} \cdot 2\ \text{V} - 2.023\ \text{V} \times 1\ \text{V}}{2\ \text{V} - 1\ \text{V}} = 1\ \text{mV}$$

Hence, the DUT output v_{DUT} and the voltmeter value $v_{measured}$ are related according to

$$v_{measured} = 1.011\ \text{V/V} \times v_{DUT} + 0.001\ \text{V}$$

The goal of the focused DC calibration procedure is to find an expression that relates the DUT output in terms of the measured value. Hence, by rearranging the expression and replacing $v_{calibrated}$ for v_{DUT}, we obtain

$$v_{calibrated} = \frac{v_{measured} - 0.001\ \text{V}}{1.011\ \text{V/V}}$$

For example, if the voltmeter reads 1.732 V, the actual voltage appearing at its terminals is actually

$$v_{calibrated} = \frac{1.732\ \text{V} - 0.001\ \text{V}}{1.011\ \text{V/V}} = 1.712\ \text{V}$$

If the original uncalibrated answer had been used, there would have been a 20-mV error! This example shows why focused DUT calibrations are so important to accurate measurements.

When buffer amplifiers are used to assist the measurement of AC signals, a similar calibration process must be performed on each frequency that is to be measured. Like the AWG calibration example, the buffer amplifier also has a nonideal frequency response and will affect the reading of the meter. Its gain variation, together with the meter's frequency response, must be measured at each frequency used in the test during a calibration run of the test program. Assuming that the meter has already been calibrated, the frequency response behavior of the DIB circuitry must be correctly accounted for. This is achieved by measuring the gain in the DIB's signal path at each specific test frequency. Once found, it is stored as a calibration factor. If additional circuits such as filters, ADCs, etc., are added on the DIB board and used under multiple configurations, then each unique signal path must be individually calibrated. Chapter 10, "Focused Calibrations," will address these and other issues in greater depth.

4.2.7 DIB Checkers

In addition to focused DIB calibrations, the test program should also include DIB checkers to verify the basic operation of as many DIB circuits and signal paths as possible. DIB failures can be a major source of downtime on a production floor unless thorough checkers are available to quickly diagnose DIB hardware failures. The first run of the test program should not only

calibrate the DIB circuits, but it should also perform a go/no-go test on as many of the DIB board components and signal paths as is possible. It is seldom possible to pass signals through every possible relay and every possible trace on the DIB board. However, every path and every component that can be tested with checker code should be verified.

A good example of a circuit in which a checker is useful is a relay path. While the gain through a relay seldom requires focused calibration, relays can become defective with age. They can also be welded shut by high currents or they can become stuck in the open state. The DIB checker code should verify that each accessible relay can be opened and then closed. The easiest way to do this is to apply a 1 V / -1 V voltage pair at the input to the relay and look for a 2-V swing at its output while the relay is closed. To verify the relay can be opened, the program should look for little or no output swing with the 1 V / -1 V input.

Exercises

4.7. A DC source is assumed characterized by a third-order equation of the form $V_{MEASURED} = 0.005 + V_{PROGRAMMED} - 0.003\, V^3_{PROGRAMMED}$ and is required to generate a DC level of 2.6 V. However, when programmed to produce this level, only 2.552 V is measured. Using iteration, determine a value of the programmed source voltage that will establish a measured voltage of 2.6 V to within a ± 1 mV accuracy.

Ans. 2.651 V.

4.8. An AWG has a gain response described by $\left(\sqrt{1+\left(f/10^3\right)^2}\right)^{-1}$ and is to generate three tones at frequencies of 1, 2, and 3 kHz. What are the calibration factors?

Ans. 0.707, 0.447, and 0.316.

4.2.8 Tester Specifications

The test engineer should exercise diligence when evaluating tester instrument specifications. It can be difficult to determine whether or not a particular tester instrument is capable of making a particular measurement with an acceptable level of accuracy. The tester specifications usually do not include the effects of uncertainty caused by instrument repeatability limitations. All the specification conditions must be examined carefully. Consider the following DC meter example.

A DC meter consisting of an analog-to-digital converter and a programmable gain amplifier (PGA) is shown in Figure 4.8. The programmable gain stage is used to set the range of the meter so that it can measure small signals as well as large ones. Small signals are measured with the highest gain setting of the PGA, while large signals are measured with the lowest gain setting. This ranging process effectively changes the resolution of the ADC so that its quantization error is minimized.

Calibration software in the tester compensates for the different PGA gain settings so that the digital output of the meter's ADC can be converted into an accurate voltage reading. The calibration software also compensates for linearity errors in the ADC and offsets in the PGA and

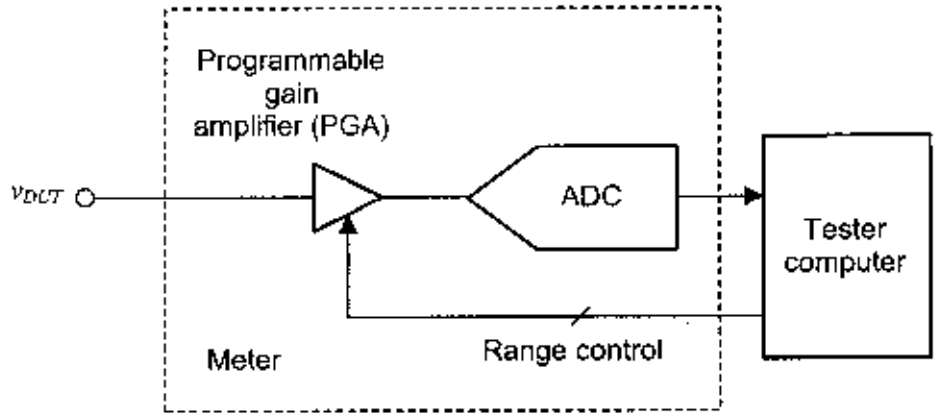

Figure 4.8. Simplified DC voltmeter with input ranging amplifier.

ADC. Fortunately, the test engineer does not have to worry about these calibrations because they happen automatically.

Table 4.1 shows an example of a specification for a fictitious DC meter, the DVM100. This meter has five different input ranges, which can be programmed in software. The different ranges allow small voltages to be measured with greater accuracy than large voltages. The accuracy is specified as a percentage of the measured value, but there is an accuracy limit of 1 mV for the lower ranges and 2.5 mV for the higher ranges.

This accuracy specification probably assumes that the measurement is made 100 or more times and averaged. For a single nonaveraged measurement, there may also be a repeatability error to consider. It is not clear from the table above what assumptions are made about averaging. The test engineer should make sure that all assumptions are understood before relying on the accuracy numbers.

Table 4.1. DVM100 DC Voltmeter Specifications

Range	Resolution	Accuracy (% of Measurement)
±0.5 V	15.25 μV	±0.05 % or 1 mV (whichever is greater)
±1 V	30.5 μV	±0.05 % or 1 mV
±2 V	61.0 μV	±0.05 % or 1 mV
±5 V	152.5 μV	±0.10 % or 2.5 mV
±10 V	305.2 mV	±0.10 % or 2.5 mV

Note: All specs apply with the measurement filter enabled.

Example 4.4

A DUT output is expected to be 100 mV. Our fictitious DC voltmeter, the DVM100, is set to the 0.5 V range to achieve the optimum resolution and accuracy. The reading from the meter (with

the meter's input filter enabled) is 102.3 mV. Calculate the accuracy of this reading (excluding possible repeatability errors). What range of outputs could actually exist at the DUT output with this reading?

ution:

The measurement error would be equal to ±0.05% of 100 mV, or 50 μV, but the specification has a lower limit of 1 mV. The accuracy is therefore ±1 mV. Based on the single reading of 102.3 mV, the actual voltage at the DUT output could be anywhere between 101.3 and 103.3 mV.

Exercises

4.9. A voltmeter is specified to have an accuracy of ±1% of programmed range. If a DC signal is measured on a ±1 V range, what are the minimum and maximum DC levels that might have been present at the meter's input during this measurement?

Ans. 0.5 V ±10 mV (i.e., the input could lie anywhere between 490 and 510 mV).

In addition to the ranging hardware, the meter also has a low-pass filter in series with its input. The filter can be bypassed or enabled, depending on the measurement requirements. Repeatability is enhanced when the low-pass filter is enabled, since the filter reduces electrical noise in the input signal. Without this filter the accuracy would be degraded by nonrepeatability. The filter undoubtedly adds settling time to the measurement, since all low-pass filters require time to stabilize to a final DC value. The test engineer must often choose between slow, repeatable measurements and fast measurements with less repeatability.

It may be possible to empirically determine through experimentation that this DC voltmeter has adequate resolution and accuracy to make a DC offset measurement with less than 100 μV of error. Since this level of accuracy is far better than the instrument's ±1 mV specifications, though, the instrument should probably not be trusted to make such a measurement in production. The accuracy might hold up for 100 days and then drift toward the specification limits of 1 mV on day 101.

Another possible scenario is that multiple testers may be used that do not all have 100-μV performance. Tester companies are often conservative in their published specifications, meaning that the instruments are often better than their specified accuracy limits. This is not a license to use the instruments to more demanding specifications. It is much safer to use the specifications as printed, since the vendor will not take any responsibility for use of instruments beyond their official specifications.

Sometimes the engineer may have to design front-end circuitry such as PGAs and filters onto the DIB board itself. The DIB circuits might be needed if the front-end circuitry of the meter is inadequate for a high-accuracy measurement. Front-end circuits may also be added if the signal from the DUT cannot be delivered cleanly through the signal paths to the tester instruments. Very high-impedance DUT signals might be susceptible to externally coupled noise, for example. Such signals might benefit from local buffering and amplification before passing to

the tester instrument. The test engineer must calibrate any such buffering or filtering circuits using a focused DIB calibration.

4.3 Dealing with Measurement Error

4.3.1 Filtering

Analog filters are often used in tester hardware to remove unwanted signal components before measurement. A DC voltmeter may include a low-pass filter as part of its front end. The purpose of the filter is to remove all but the lowest-frequency components. It acts as a hardware averaging circuit to improve the repeatability of the measurement. More effective filtering is achieved using a filter with a low cutoff frequency, since a lower cutoff frequency excludes more electrical noise. Consequently, a lower frequency cutoff corresponds to better repeatability in the final measurement.

Unfortunately, it takes longer to measure a series of DC voltages with a low-pass filter in the signal path. Since the filter has a settling time that is inversely proportional to the cutoff frequency, though, a lower cutoff frequency adds extra test time while the filter settles to a stable DC level. Thus, there is an inherent tradeoff between repeatability and test time. The following two examples will quantify this tradeoff for a first-order system.

Example 4.5

The simple *RC* low-pass circuit shown in Figure 4.9 is used to filter the output of a DUT containing a noisy DC signal. For a particular measurement, the signal component is assumed to change from 0 to 1 V, instantaneously. How long does it take the filter to settle to within 1% of its final value? By what factor does the settling time increase when the filter's 3-dB bandwidth is decreased by a factor of 10?

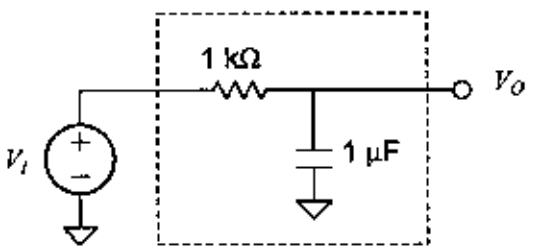

Figure 4.9. *RC* low-pass filter.

Solution:

From the theory of first-order networks, the step response of the circuit starting from rest (i.e., $v_i = 0$) in Figure 4.9 is

$$v_o(t) = S\left(1 - e^{-t/\tau}\right) \tag{4.9}$$

where $S = 1$ V is the magnitude of the step and $\tau = RC = 10^{-3}$ s. Moreover, the 3-dB bandwidth ω_b (expressed in rad/s) of a first-order network is $1/RC$, so we can rewrite the above expression as

$$v_O(t) = S\left(1 - e^{-\omega_b t}\right) \tag{4.10}$$

Clearly, the time $t = t_S$ the output reaches an arbitrary output level of V_O is then

$$t_S = -\frac{\ln\left(\frac{S - V_O}{S}\right)}{\omega_b} \tag{4.11}$$

Further, we recognize that $(S - V_O)/S$ is the settling error ε or the accuracy of the measurement, so we can rewrite Eq. (4.11) as

$$t_S = -\frac{\ln(\varepsilon)}{\omega_b} \tag{4.12}$$

Hence, the time it takes to reach within 1% of 1 V, or 0.99 V, is

$$t_S = -\frac{\ln(0.01)}{1/10^{-3}} = 4.6 \text{ ms}$$

Since settling time and 3-dB bandwidth are inversely related according to Eq. (4.12), a tenfold decrease in bandwidth leads to a tenfold increase in settling time. Specifically, the settling time becomes 46 ms.

Example 4.6

The simple *RC* low-pass circuit shown in Figure 4.9 is used to filter the output of a DUT containing a noisy DC signal. If the noise voltage has a constant spectral density of η V^2/Hz, what is the RMS noise voltage that appears at the output of the filter? If the filter bandwidth decreases by a factor of 10, by what factor does the output noise voltage decrease?

Solution:

To answer this question we must rely on our knowledge of noise and linear system theory. We shall make use of frequency-domain techniques. While periodic signals have power at distinct frequency locations (see, for example, Figure 4.5), noise signals have their power spread out over the entire frequency spectrum. As such, noise signals are characterized by a noise spectral density function, which we shall denote as $S(f)$. It represents the average power over a 1-Hz bandwidth centered at each frequency, f. To simplify our discussion, $S(f)$ will have units of volts-squared/hertz or V^2/Hz. It can also be expressed in terms of amps-squared/hertz or watts/hertz. (Data sheets often specify noise using volts per root-hertz, which is simply the

square root of the noise spectral density as we have defined it here.) The total mean-squared value of the noise is obtained by integrating the spectral density over the entire frequency spectrum. Thus the RMS value of the noise signal can also be obtained in the frequency domain using the following relationship

$$V_{RMS} = \sqrt{\int_0^{\infty} S(f)df} \tag{4.13}$$

Now to get back to the question at hand, the noise that appears at the output of the filter is related to the input noise voltage according to the following

$$S_{n_o}(f) = S_{n_i}(f)\left|G(f)\right|^2 \tag{4.14}$$

where $S_{n_i}(f)$ and $S_{n_o}(f)$ are the input and output noise voltage spectral densities, respectively, and $G(f)$ is the system input-output transfer function. Hence, the RMS value of the output noise voltage V_{n_o} is

$$V_{n_o} = \sqrt{\int_0^{\infty} S_{n_o}(f)df} \tag{4.15}$$

or, once we substitute Eq. (4.14), we obtain

$$V_{n_o} = \sqrt{\int_0^{\infty} S_{n_i}(f)\left|G(f)\right|^2 df} \tag{4.16}$$

Since we are told

$$S_{n_i}(f) = \eta \quad \frac{V^2}{Hz} \tag{4.17}$$

and that we can calculate the system transfer function for the RC low-pass filter to be

$$G(f) \equiv \frac{V_o}{V_i}(f) = \frac{\omega_b}{\omega_b + j2\pi f} = \frac{1}{1 + j\dfrac{2\pi f}{\omega_b}} \tag{4.18}$$

where $\omega_b = 1/RC$. We can then write Eq. (4.16) as

$$V_{n_o} = \sqrt{\eta \int_0^{\infty} \left|\frac{1}{1 + j\dfrac{2\pi f}{\omega_b}}\right|^2 df} \tag{4.19}$$

Integrating and performing the square root, we obtain the RMS output noise voltage to be

$$V_{n_o} = \frac{1}{2}\sqrt{\eta\omega_b} \quad \text{V} \tag{4.20}$$

Here we clearly see that the output noise voltage depends on two factors: the level of the input noise voltage spectral density and the filter's 3-dB bandwidth expressed in rad/s. If the filter's bandwidth is decreased by a factor of 10, then a $\sqrt{10}$ reduction in output noise RMS voltage will occur. We can also conclude that the repeatability will improve.

However, at this time we can not formally quantify the improvement until a mathematical definition for repeatability is given. For now, we will offer without proof that the total variation in measurement values is proportional to the level of noise. Thus, in the example above, we can expect the variability of measurements to improve by a factor of $\sqrt{10}$. We shall offer a formal analysis of the relationship between noise and repeatability in Chapter 15, "Data Analysis."

In the preceding example, the concept of a noise spectral density was introduced and used to characterize the noise at the input of the filter. Subsequently, it was used to determine the RMS level of the noise at the output of the filter. Often the test engineer knows only the RMS noise value from the output of the DUT, rather than the output noise spectral density. Interestingly enough, using Eq. (4.20) we can work backwards and obtain an estimate of the spectral density level η coming from the DUT

$$\eta = 4\frac{(V_{DUT})^2}{\omega_{DUT}} \quad \frac{\text{V}^2}{\text{Hz}} \tag{4.21}$$

where V_{DUT} is the DUT output noise (RMS volts) and ω_{DUT} is the 3-dB bandwidth of the DUT.

Exercises

4.10. What is the 3-dB bandwidth of the *RC* circuit of Figure 4.9, expressed in Hertz, when $R = 1$ kΩ and $C = 2.2$ nF?

Ans. 72.34 kHz.

4.11. How long does it take a first-order *RC* low-pass circuit with $R = 1$ kΩ and $C = 2.2$ nF to settle to 5% of its final value?

Ans.. 6.6 μs.

4.12. A noise signal having a spectral density of 10^{-9} V²/Hz is applied to the *RC* circuit of Figure 4.9 with $R = 1$ kΩ and $C = 2.2$ nF. What is the RMS-level of the noise voltage that appears at the output?

Ans. 10.7 mV RMS.

Provided $\omega_b << \omega_{DUT}$, it is reasonable to assume that the noise has a constant spectral density over the frequencies of interest given by Eq. (4.21). Substituting Eq. (4.21) back into Eq. (4.20), we can write

$$V_{n_O} = V_{DUT}\sqrt{\frac{\omega_b}{\omega_{DUT}}} \quad \text{V} \tag{4.22}$$

This expression clearly illustrates the noise reduction gained by filtering the output. The smaller the ratio ω_b / ω_{DUT}, the greater the noise reduction. Other types of filtering circuits can be placed on the DIB board when needed. For example, a very narrow bandpass filter may be placed on the DIB board to clean up noise components in a sine wave generated by the tester. The filter allows a much more ideal sine wave to the input of the DUT than the tester would otherwise be able to produce.

Exercises

4.13. By what factor should the bandwidth of an *RC* low-pass filter be decreased in order to reduce the variation in a DC measurement from 250 μV-RMS to 100 μV-RMS. By what factor does the settling time increase.

Ans. The bandwidth should be decreased by 6.25 (=2.5^2). Settling time increases by 2.5.

4.14. The variation in the output signal of a DUT is 1 mV RMS. Assume that the DUT's output follows a first-order frequency response and has a 3-dB bandwidth of 100 Hz. Estimate the output noise voltage spectral density.

Ans. 6.37×10^{-9} V^2/Hz.

4.15. The variation in the output RMS signal of a DUT is 1 mV, but it needs to be reduced to a level closer to 500 μV. What filter bandwidth is required to achieve this level of repeatability? Assume that the DUT's output follows a first-order frequency response and has a 3-dB bandwidth of 1000 Hz

Ans.. 250 Hz.

4.16. A DUT output consisting of a noise component having a spectral density of 10^{-6} V^2/Hz is to be measured 100 times and the results averaged. What is RMS value of the noise component in the final result?

Ans. 100 μV RMS.

4.17. The output of a DUT has an uncertainity of 10 mV. How many samples should be combined in order to reduce the uncertainity to 100 μV?

Ans. 10.000.

4.3.2 Averaging

Averaging is a form of discrete-time filtering. Averaging can be used to improve the repeatability of a measurement. For example, we can average the following series of nine voltage measurements

101 mV, 103 mV, 102 mV, 101 mV, 102 mV, 103 mV, 103 mV, 101 mV, 102 mV

and obtain an average of 102 mV. There is a good chance that a second series of nine unique measurements will again result in something close to 102 mV. If the length of the series is increased, the answer will become more repeatable and reliable. But there is a point of diminishing returns. To reduce the effect of noise on the voltage measurement by a factor of two, one has to take four times as many readings and average them. At some point, it becomes prohibitively expensive (i.e., from the point of view of test time) to improve repeatability.

To better understand the above statement, consider representing a sequence of numbers as $x(n)$, where n indicates the order at which the samples appear in the sequence. Further, let $x(n)$ consist of both signal and noise. Now, consider $x(n)$ as input to a discrete-time system whose output is the average value of $x(n)$ and the N-1 previous input samples. Mathematically, we can write the input-output relationship as

$$\begin{aligned} y(n) &= \frac{1}{N}\left[x(n)+x(n-1)+\cdots+x(n-N+1)\right] \\ &= \frac{1}{N}\sum_{k=1}^{N} x(n-k+1) \end{aligned} \tag{4.23}$$

This system is called an *N-point running averager* and it can easily be shown that it has a frequency response* for $-½ \le f \le ½$ given by

$$\begin{aligned} G(f) &= \left(\frac{\sin(2\pi fN/2)}{N\sin(2\pi f/2)}\right)\left[\cos\left(2\pi f(N-1)/2\right)-j\sin\left(2\pi f(N-1)/2\right)\right] \\ &= \left(\frac{\sin(2\pi fN/2)}{N\sin(2\pi f/2)}\right)e^{-j2\pi f(N-1)/2} \end{aligned} \tag{4.24}$$

Technically, we are really only interested in the output after N samples; that is, the output is downsampled or decimated by N

$$y_D(n) = y(nN) \tag{4.25}$$

To introduce its effect on the system's frequency response will only add more complication to an otherwise sophisticated explanation. Nonetheless, regardless of when the output is obtained, one

---

* The frequency response is obtained by first evaluating the z-transform of Eq. (4.23) and then substituting $z = e^{j2\pi f}$.

would not expect the behavior of the noise to be influenced by the observation window. So we shall work with the running average result only as the conclusions are the same.

If the noise component in the input signal has a constant spectral density of η V^2/Hz, the output noise spectral density will then be given by Eq. (4.13). The RMS voltage that appears in the output discrete-time signal is found from an expression very similar to the continuous-time case given in Eq. (4.16). However, in this case the integration is performed from $-½$ to ½ to account for the periodicity of $G(f)$ and because the sampling period is 1

$$V_{n_O} = \sqrt{\int_{-1/2}^{1/2} S_{n_I}(f)\left|G(f)\right|^2 df} \tag{4.26}$$

Substituting the appropriate relationships, we obtain

$$V_{n_O} = \sqrt{\eta \int_{-1/2}^{1/2} \left| \left[\frac{\sin(2\pi fN/2)}{N\sin(2\pi f/2)}\right] e^{-j2\pi f(N-1)/2} \right|^2 df} \tag{4.27}$$

Finally, solving the integration and taking the square root, we obtain

$$V_{n_O} = \sqrt{\frac{\eta}{N}} \quad \text{V} \tag{4.28}$$

If we denote the noise from the DUT before averaging as V_{DUT}, it is easy to show that $V_{n_O} = \sqrt{\eta}$. This can be seen directly from Eq. (4.28) when $N = 1$. However, with no averaging taking place, $V_{n_O} = V_{DUT}$. Hence, we can write the final expression as

$$V_{n_O} = \frac{V_{DUT}}{\sqrt{N}} \quad \text{V} \tag{4.29}$$

Here we see the output noise voltage reduces the input noise before averaging by the factor $\sqrt{N}$. Hence, to reduce the noise RMS voltage by a factor of two requires an increase in the sequence length, N, by a factor of four.

AC measurements can also be averaged to improve repeatability. A series of sine wave signal level measurements can be averaged to achieve better repeatability. However, one should not try to average readings in decibels. If a series of measurements is expressed in decibels, they should first be converted to linear form using the equation $V = 10^{dB/20}$ before applying averaging. Normally, the voltage or gain measurements are available before they are converted to decibels in the first place; so the conversion from dB to linear units or ratios is not necessary. Once the average voltage level is calculated, it can be converted to decibels using the equation $dB = 20\log_{10}(V)$. To understand why we should not perform averaging on decibels, consider the sequence 0, -20, -40 dBV. The average of these values is –20 dBV. However, the actual voltages are 1 V, 100 mV, and 10 mV. Thus the correct average value is (1 V + 0.1 V + 0.01 V) / 3 = 37 mV, or -8.64 dBV.

4.3.3 Guardbanding

Guardbanding is an important technique for dealing with the uncertainty of each measurement. If a particular measurement is known to be accurate and repeatable with a worst-case uncertainty of $\pm\varepsilon$, then the final test limits should be tightened from the data sheet specification limits by ε to make sure no bad devices are shipped to the customer. In other words

$$\begin{aligned}\text{guardbanded upper test limit} &= \text{upper specification limit} - \varepsilon \\ \text{guardbanded lower test limit} &= \text{lower specification limit} + \varepsilon\end{aligned} \tag{4.30}$$

So, for example, if the data sheet limit for the offset on a buffer output is −100 mV minimum, 100 mV maximum, and an uncertainty of ±10 mV exists in the measurement, the test program limits should be set to −90 mV minimum and 90 mV maximum. This way, if the device output is 101 mV and the error in its measurement is −10 mV, the resulting reading of 91 mV will cause a failure as required. Of course, a reading of 91 mV may also represent a device with an 81-mV output and a +10 mV measurement error.

In such cases, guardbanding has the unfortunate effect of disqualifying good devices. Ideally, we would like all guardbands to be set to 0 so that no good devices will be discarded. To minimize the guardbands we must improve the repeatability and accuracy of each test, but this typically requires longer test times. There is a balance to be struck between repeatability and the number of good devices rejected. At some point, the added test time cost of a more repeatable measurement outweighs the cost of discarding a few good devices.

Example 4.7

Table 4.2 lists a set of output values from a DUT together with their measured values. It is assumed that the upper test limit is 100 mV and the measurement uncertainty is ±6 mV. How many good devices are rejected because of the measurement error? How many good devices are rejected if the measurement uncertainty is increased to ±10 mV?

Table 4.2. DUT Output and Measured Values

DUT Output	Measured Value
105 mV	101 mV
101 mV	107 mV
98 mV	102 mV
96 mV	95 mV
86 mV	92 mV
72 mV	78 mV

lution:

From the DUT output column on the left, four devices are below the upper test limit of 100 mV and should be accepted. The other two should be rejected. Now with a measurement uncertainty of ±6 mV, according to Eq. (4.30) the guardbanded upper test limit is 94 mV. With the revised test limit, only two devices are acceptable. The others are all rejected. Hence, two otherwise good devices are disqualified.

If the measurement uncertainty increases to ±10 mV, then the guardbanded upper test limit becomes 90 mV. Five devices are rejected and only one is accepted. Consequently, three otherwise good devices are disqualified.

Exercises

4.18. A device is expected to exhibit a worst-case offset voltage of ±50 mV and is to be measured using a voltmeter having an accuracy of only ±5 mV. Where should the guardbanded test limits be set?

Ans. ±45 mV.

4.19. The guardband of a particular measurement is 10 mV and the test limit is set to ±25 mV. What are the original device specification limits?

Ans. ±35 mV.

4.20. The following lists a set of output voltage values from a group of DUTs together with their measured values: {(2.3, 2.1), (2.1, 1.6), (2.2, 2.1), (1.9, 1.6), (1.8, 1.7), (1.7, 2.1), (1.5, 2.0)}. If the upper test limit is 2.0 V and the measurement uncertainty is ±0.5 V, how many good devices are rejected due to the measurement error?

Ans. Four devices (all good devices are rejected by the 1.5-V guardbanded upper test limit).

4.4 Basic Data Analysis

4.4.1 Datalogs

A datalog is a concise listing of the test results generated by a test program. Datalogs are the primary means by which test engineers evaluate the quality of a device as it is tested. The format of a datalog typically includes a test category, test description, upper and lower test limits, and a measured result. The exact format of datalogs varies from one tester type to another, but they all convey similar information.

A short datalog from a Teradyne A580 tester is listed in Figure 4.10. Each line of the datalog contains a shorthand description of the test. For example, "DAC Gain Error" is the name given to test number 5000. The gain error is part of the S_VDAC_SNR test group and is executed during a test routine called T_VDAC_SNR. The upper and lower limits for the test are also

listed. Using test number 5000 as an example, the lower limit of DAC Gain Error is –1.00 dB, the upper limit is +1.00 dB, and the measured value for this DUT is –0.13 dB.

The datalog lists an easily recognizable fail flag for values that fall outside the specified test limits. Test 7004 shows a test failure in which the measurement reads 1.23 LSBs (least significant bits). The upper limit is 0.9 LSBs, so this test fails. Because the device is not a good one, it is categorized into Bin 10 in this example. Bin 1 usually represents a good device, while other bins usually represent various categories of failure.

Sometimes multiple good bins are defined, allowing devices to be graded into several passing categories. For instance, a microprocessor may fail full speed digital pattern testing at 750 MHz, but may operate perfectly well at 500 MHz. In such a case, the 500-MHz processor might be graded into Bin 2 and sold at a lower price while higher-grade 750-MHz processors are graded into Bin 1 and sold at a premium.

```
Sequencer:  S_continuity
  1000 Neg PPMU Cont       Failing Pins:  0
Sequencer:  S_VDAC_SNR
  5000 DAC Gain Error      T_VDAC_SNR  -1.00  dB <    -0.13  dB      <  1.00  dB
  5001 DAC S/2nd           T_VDAC_SNR   60.0  dB <=   63.4  dB
  5002 DAC S/3rd           T_VDAC_SNR   60.0  dB <=   63.6  dB
  5003 DAC S/THD           T_VDAC_SNR  60.00  dB <=  60.48  dB
  5004 DAC S/N             T_VDAC_SNR   55.0  dB <=   70.8  dB
  5005 DAC S/N+THD         T_VDAC_SNR   55.0  dB <=   60.1  dB
Sequencer:  S_UDAC_SNR
  6000 DAC Gain Error      T_UDAC_SNR  -1.00  dB <    -0.10  dB      <  1.00  dB
  6001 DAC S/2nd           T_UDAC_SNR   60.0  dB <=   86.2  dB
  6002 DAC S/3rd           T_UDAC_SNR   60.0  dB <=   63.5  dB
  6003 DAC S/THD           T_UDAC_SNR  60.00  dB <=  63.43  dB
  6004 DAC S/N             T_UDAC_SNR   55.0  dB <=   61.3  dB
  6005 DAC S/N+THD         T_UDAC_SNR   55.0  dB <=   59.2  dB
Sequencer:  S_UDAC_Linearity
  7000 DAC POS ERR         T_UDAC_Lin  -100.0 mV <      7.2 mV      <  100.0 mV
  7001 DAC NEG ERR         T_UDAC_Lin  -100.0 mV <      3.4 mV      <  100.0 mV
  7002 DAC POS INL         T_UDAC_Lin -0.90  lsb <   0.84  lsb      < 0.90  lsb
  7003 DAC NEG INL         T_UDAC_Lin -0.90  lsb <  -0.84  lsb      < 0.90  lsb
  7004 DAC POS DNL         T_UDAC_Lin -0.90  lsb <   1.23  lsb (F)  < 0.90  lsb
  7005 DAC NEG DNL         T_UDAC_Lin -0.90  lsb <  -0.83  lsb      < 0.90  lsb
  7006 DAC LSB SIZE        T_UDAC_Lin    0.00 mV <     1.95 mV      < 100.00 mV
  7007 DAC Offset V        T_UDAC_Lin  -100.0 mV <      0.0 mV      <  100.0 mV
  7008 Max Code Width      T_UDAC_Lin  0.00  lsb <   1.23  lsb      < 1.50  lsb
  7009 Min Code Width      T_UDAC_Lin  0.00  lsb <   0.17  lsb      < 1.50  lsb
Bin:  10
```

Figure 4.10. Example datalog from a Teradyne A580 tester.

4.4.2 Histograms

When a test program is executed multiple times on a single DUT, it is common to get multiple answers due to imperfect repeatability. If we repeatedly execute the test program corresponding to Figure 4.10 and display only the results from test 5000, the DAC Gain Error test may show slight repeatability errors:

```
  5000 DAC Gain Error      T_VDAC_SNR  -1.000  dB <  -0.127  dB      < 1.000  dB
  5000 DAC Gain Error      T_VDAC_SNR  -1.000  dB <  -0.129  dB      < 1.000  dB
  5000 DAC Gain Error      T_VDAC_SNR  -1.000  dB <  -0.125  dB      < 1.000  dB
  5000 DAC Gain Error      T_VDAC_SNR  -1.000  dB <  -0.131  dB      < 1.000  dB
```

```
5000 DAC Gain Error      T_VDAC_SNR  -1.000  dB <  -0.129  dB     < 1.000  dB
5000 DAC Gain Error      T_VDAC_SNR  -1.000  dB <  -0.129  dB     < 1.000  dB
5000 DAC Gain Error      T_VDAC_SNR   1.000  dB <  -0.132  dB     < 1.000  dB
5000 DAC Gain Error      T_VDAC_SNR  -1.000  dB <  -0.130  dB     < 1.000  dB
5000 DAC Gain Error      T_VDAC_SNR  -1.000  dB <  -0.134  dB     < 1.000  dB
5000 DAC Gain Error      T_VDAC_SNR  -1.000  dB <  -0.131  dB     < 1.000  dB
...
```

Notice that the resolution of the datalog output has been increased to three digits after the decimal point in this second example. The printout resolution is specified in the test program. The extra resolution in this second example allows the variations in the results to be more easily seen. Otherwise, all the results above would have been rounded off to –0.13 dB. It is important to note that there may be a difference between datalog output resolution and the resolution of the value as it is compared against test limits. Testers generally use the full resolution of the measurement when comparing DUT performance against the specification limits. Only the datalog output values are rounded, not the actual measured values.

We can view the repeatability of a group of readings using a tool called a *histogram*. A histogram for the repeatability example above is shown in Figure 4.11. It shows both numerical results and a plot of the distribution of measured values. The distribution plot is a convenient graphical way to understand the repeatability of the measurement. Ideally, the distribution should be closely packed, as the example in Figure 4.11 shows. However, if the measurement repeatability is poor the histogram spreads out into a larger range of values.

This histogram output also displays a number of useful values. The population size is listed next to the heading "Total Results =". It indicates how many times the measurement was repeated on the same device. Histograms are also used to look at distributions of measurements over many DUTs to determine how much variability there is from one device to another. In the case of multiple DUTs, the total results would be the number of DUTs tested.

The larger the population of results, the more trustworthy a histogram becomes. A histogram with less than 50 results is statistically questionable because of the limited sample size. Ideally a histogram should contain results from at least 100 devices (or 100 test executions on a single device in the case of repeatability studies).

Another useful item in the histogram is the population statistics. The mean μ and standard deviation σ are the most important of these. The mean, or average, represents the most probable value of a measured variable. The best approximation will be made when the number of readings N of the same quantity is very large. The mean value is defined as

$$\mu = \frac{1}{N}\sum_{n=1}^{N} x(n) \tag{4.31}$$

For the DAC Gain Error example shown in Figure 4.11, the mean value from 110 measurements is -0.1300 dB. The standard deviation is a measure of the dispersion or uncertainty of the measured quantity about the mean value, μ. If the values tend to be concentrated near the mean, the standard deviation is small, while if the values tend to be distributed far from the mean, the standard deviation is large. Standard deviation is defined as

$$\sigma = \sqrt{\frac{1}{N}\sum_{n=1}^{N}\left[x(n)-\mu\right]^2} \tag{4.32}$$

Test No	Test Function Name	Test Label	Units
5000	T_VDAC_SNR	DAC Gain Error	dB

Lower Test Limit=	-1dB	Upper Test Limit=	1dB

– DISTRIBUTION STATISTICS –

Lower Pop Limit=	-Infinity	Upper Pop Limit=	+Infinity
Total Results=	110	Results Accepted=	110
Underflows=	0	Overflows=	0
Mean=	-0.13003dB	Std Deviation=	0.00292899
Mean - 3 Sigma=	-0.13882dB	Mean + 3 Sigma=	-0.12125dB
Minimum Value=	-0.13594dB	Maximum Value=	-0.12473dB

– PLOT STATISTICS –

Lower Plot Limit=	-0.14dB	Upper Plot Limit=	-0.12dB
Cells=	15	Cell Width=	0.0013333dB
Full Scale Percent=	16.36%	Full Scale Count=	18

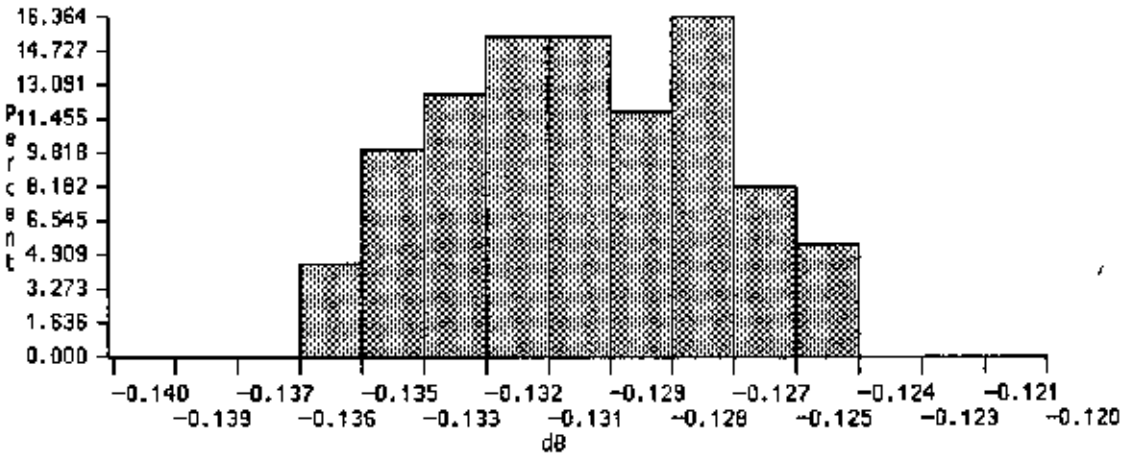

Figure 4.11. Histogram of the DAC gain error test.

Standard deviation and mean are expressed in identical units. In our DAC example, the standard deviation was found to be 0.0029 dB. Notice that we have broken the previously stated rule that we should not calculate averages (and standard deviations for that matter) using logarithmic units such as the decibel. However, we are often able to take this statistical shortcut when all the values are very near one another. The reason for this is that logarithmic curves are approximately linear over a limited span of values. It would not be advisable to take such a shortcut if the range of values covered a 20-dB span. We can still view histograms of logarithmic values to get a general idea of the mean and standard deviation, but we should remember that these values are not entirely accurate. To be perfectly correct we would need to convert the logarithmic values into linear units such as V/V before reading the mean and standard deviation from a histogram.

The histogram in Figure 4.11 exhibits a common feature for analog and mixed-signal measurements. The distribution of values has a shape similar to a bell. The bell curve (also called a *normal distribution* or *Gaussian distribution*) is a common one in the study of statistics. According to the central limit theorem,[6] any summation of a large number ($N > 30$) of statistically independent random variables converges toward a Gaussian distribution. The

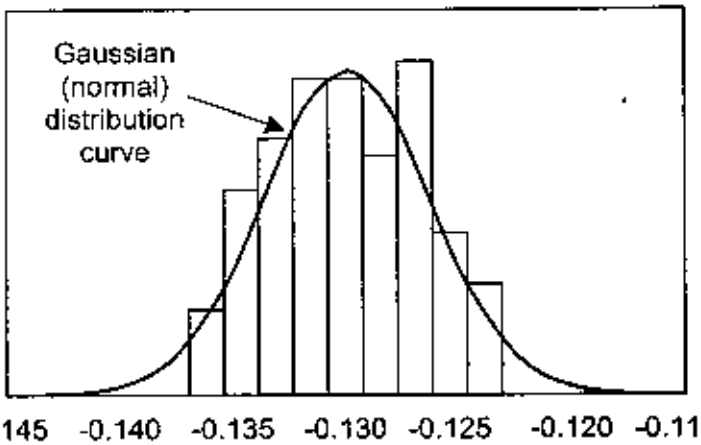

Figure 4.12. Continuous normal (Gaussian) distribution for the DAC gain example.

variations in a typical mixed-signal measurement are caused by a summation of many different sources of noise and crosstalk in both the device and the tester instruments. As a result, many mixed-signal measurements exhibit the familiar Gaussian distribution.

For the DAC Gain Error example, Figure 4.12 illustrates the results using a smooth curve through all the measured points. As is evident, the graph has a bell shape, quite similar to a Gaussian distribution. In theory, a Gaussian distribution extends to infinity. In other words, if you are willing to wait billions of years you should eventually see an answer of +200 dB in the DAC gain example. In reality, measurements are only near-Gaussian. As a result, the answer in the example will probably never stray more than a few tenths of a dB away from –0.13 dB.

Although the real world only approximates the ideal Gaussian distribution, the comparison is close enough to allow some general statements. First, the standard deviation of a Gaussian distribution is roughly equal to one sixth of the total variation from the minimum value to the maximum value. In the distribution of Figure 4.12 the standard deviation is 0.0029 dB; so we would expect to see values ranging from –0.139 to –0.121 dB. These values are displayed in the sample histogram beside the labels "Mean –3 sigma" and "Mean +3 sigma." The actual minimum and maximum values are not as extreme, which indicates that this is not truly a Gaussian distribution.

It is quite common to obtain distributions that are not Gaussian, though the distributions should be more or less bell-shaped. Common deviations from the familiar bell shape are bimodal distributions (Figure 4.13) and outliers (Figure 4.14). When looking for measurement repeatability on a single DUT, these distributions are a warning sign that something is not sufficiently repeatable. When looking for distributions of a parameter across many DUTs, non-Gaussian plots may indicate a poor design or a fabrication process that needs to be fixed. They may also indicate a test program that is yielding incorrect answers.

4.4.3 Noise, Test Time, and Yield

The yield of a given lot of material is defined as the ratio of the total good devices divided by the total devices tested:

$$\text{yield} = \frac{\text{total good devices}}{\text{total devices tested}} \times 100\% \tag{4.33}$$

If 10,000 parts are tested and only 7,000 devices pass all tests, then the yield on that lot of 10,000 devices is 70%. As explained in Section 4.3.3, there are inherent tradeoffs between repeatability, test time, and production yield.

If a device is well designed and a particular measurement is sufficiently repeatable, then there will be few failures on that measurement. But if the distribution of readings on a production lot of devices is skewed so that it is close to one of the test limits, then production yields are likely to fall. In other words, more good devices will fall beyond the guardband region and be disqualified. Obviously, a measurement with poor accuracy or poor repeatability will just exacerbate the problem.

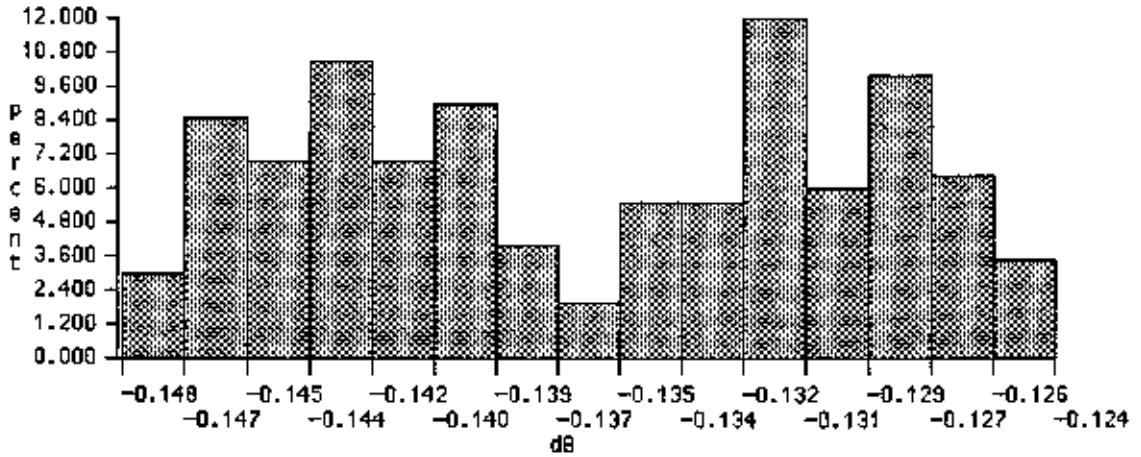

Figure 4.13. Bimodal distribution.

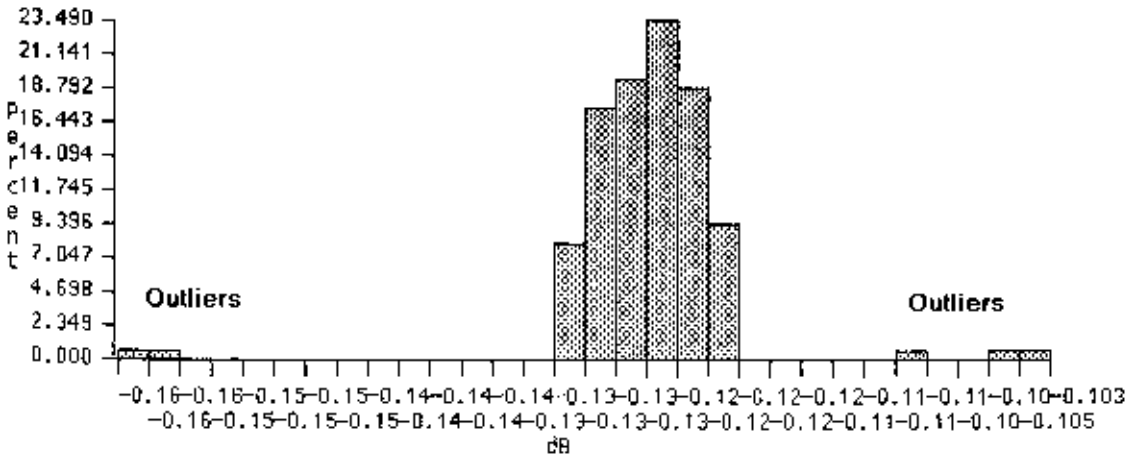

Figure 4.14. Statistical outliers.

In Section 4.3.1 it was shown that averaging or filtering a measurement can make it more repeatable, with the unfortunate consequence of longer test time. On the other hand, centering the design between test limits and making the design insensitive to process variations might make it unnecessary to achieve such accuracy and repeatability. Test costs can be dramatically reduced with well-centered designs with plenty of margin. Unfortunately, well-centered designs with good margin are often power hungry or silicon area intensive. The test engineer and design engineer should work together to achieve an optimum balance between low silicon overhead with minimal power consumption and low test cost with minimum averaging. Only by working as a team can these two engineering disciplines produce a cost-effective product that will succeed in the marketplace.

4.5 Summary

In this chapter we have introduced the concept of accuracy and repeatability and shown how these concepts affect device quality and production test economics. We have examined many contributing factors leading to inaccuracy and nonrepeatability. Using software calibrations, we can eliminate or at least reduce many of the effects leading to measurement inaccuracy. Measurement repeatability can be enhanced through averaging and filtering, at the expense of added test time. The constant balancing act between adequate repeatability and minimum test time represents a large portion of the test engineer's workload. One of fundamental skills that separates good test engineers from average test engineers is the ability to quickly identity and correct problems with measurement accuracy and repeatability. Doing so while maintaining low test times and high yields is the mark of a great test engineer.

In the next chapter, we will take a brief vacation from mathematical equations to examine the measurement instrumentation and other architectural features common to many mixed-signal ATE testers. We will study the various types of instruments such as waveform digitizers, arbitrary waveform generators, digital pattern generators, and other mixed-signal ATE instruments. It might seem that this fundamental topic should have been presented in an earlier chapter. The subject has been delayed until Chapter 5 because many of the architectural features of mixed-signal testers are easier to understand in the context of accuracy, repeatability, and their combined effects on test time and production yield.

Exercises

4.21. A 5-mV signal is measured with a meter ten times, resulting in the following sequence of readings: 7 mV, 6 mV, 9 mV, 8 mV, 4 mV, 7 mV, 5 mV, 7 mV, 8 mV, 11 mV. What is the mean value? What is the standard deviation?

Ans. 7.2 mV, 1.887 mV.

4.22. If 15,000 devices are tested with a yield of 63%, how many devices passed the test?

Ans. 9450 devices.

Problems

4.1. A 55-mV signal is measured with a meter ten times resulting in the following sequence of readings: 57 mV, 60 mV, 49 mV, 58 mV, 54 mV, 57 mV, 55 mV, 57 mV, 48 mV, 61 mV. What is the average measured value? What is the systematic error?

4.2. A DC voltmeter is rated at 14 bits of resolution and has a full-scale input range of ±5 V. Assuming the meter's ADC is ideal, what is the maximum quantization error that we can expect from the meter? What is the error as a percentage of the meter's full-scale range?

4.3. A 100 mV signal is to measured with a worst-case error of ±10 μV. A DC voltmeter is set to a full-scale range of ±1 V. Assuming that quantization error is the only source of inaccuracy in this meter, how many bits of resolution would this meter need to have to make the required measurement? If the meter in our tester only has 14 bits of resolution but has binary-weighted range settings (i.e., ±1 V, ±500 mV, ±250 mV, etc.) how would we make this measurement?

4.4. A voltmeter is specified to have an accuracy error of ±0.1% of full-scale range on a ±1-V scale. If the meter produces a reading of 0.323 V DC, what is the minimum and maximum DC levels that might have been present at the meter's input during this measurement?

4.5. A meter reads −1.039 mV and 1.121 V when connected to two highly accurate reference levels of −1 V and 1 V, respectively. What is the offset and gain of this meter? Write the calibration equation for this meter.

4.6. A DC source is assumed characterized by a third-order equation of the form: $V_{MEASURED} = 0.004 + V_{PROGRAMMED} + 0.001\ V_{PROGRAMMED}^{\ 2} - 0.007\ V_{PROGRAMMED}^{\ 3}$ and is required to generate a DC level of 1.25 V. However, when programmed to produce this level, only 1.242 V is measured. Using iteration, determine a value of the programmed source voltage that will establish a measured voltage of 1.25 V to within a ± 0.5 mV accuracy.

4.7. An AWG has a gain response described by $G(f) = \dfrac{1}{\sqrt{1+\left(\dfrac{f}{4000}\right)^2}}$ and is to generate three tones at frequencies of 1, 2, and 3 kHz. What are the gain calibration factors? What voltage levels would we request if we wanted an output level of 500 mV RMS at each frequency?

4.8. Several DC measurements are made on a signal path that contains a filter and a buffer amplifier. At input levels of 1 and 3 V, the output was found to be 1.02 and 3.33 V, respectively. Assuming linear behavior, what is the gain and offset of this filter-buffer stage?

4.9. Using the setup and results of Problem 4.8, what is the calibrated level when a 2.13 V level is measured at the filter-buffer output? What is the size of the uncalibrated error?

4.10. A simple *RC* low-pass circuit is constructed using a 1-kΩ resistor and a 10-μF capacitor. This *RC* circuit is used to filter the output of a DUT containing a noisy DC signal. If the DUT's noise voltage has a constant spectral density of 100 nV / $\sqrt{\text{Hz}}$, what is the RMS noise voltage that appears at the output of the *RC* filter? If the we decrease the capacitor value to 2.2 μF, what is the RMS noise voltage at the *RC* filter output?

4.11. Assume that we want to allow the *RC* filter in Problem 4.10 to settle to within 0.2% of its final value before making a DC measurement. How much settling time does the first *RC* filter in Problem 4.10 require? Is the settling time of the second *RC* filter greater or less than that of the first filter?

4.12. A DC meter collects a series of repeated offset measurements at the output of a DUT. A first-order low-pass filter such as the one in Problem 4.10 is connected between the DUT output and the meter input. A histogram is produced from the repeated measurements. The histogram shows a Gaussian distribution with a 50-mV difference between the maximum value and minimum value. It can be shown that the standard deviation, σ, of the histogram of a repeated series of identical DC measurements on one DUT is proportional to the RMS noise at the meter's input. Assume the difference between the maximum and minimum measured values is roughly equal to 6σ. How much would we need to reduce the cutoff frequency of the low-pass filter to reduce the nonrepeatability of the measurements from 50 to 10 mV? What would this do to our test time, assuming the test time is dominated by the settling time of the low-pass filter?

4.13. The DUT in Problem 4.12 can be sold for $1.25, assuming it passes all tests. If it does not pass all tests, it cannot be sold at all. Assume that the more repeatable DC offset measurement in Problem 4.12 results in a narrower guardband requirement, causing the production yield to rise from 92% to 98%. Also assume that the cost of testing is known to be 3.5 cents per second and that the more repeatable measurement adds 250 ms to the test time. Does the extra yield obtained with the lower filter cutoff frequency justify the extra cost of testing resulting from the filter's longer settling time?

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CHAPTER 5

Tester Hardware

5.1 Mixed-Signal Tester Overview

5.1.1 General-Purpose Testers versus Focused Bench Equipment

General-purpose mixed-signal testers must be capable of testing a variety of dissimilar devices. On any given day, the same mixed-signal tester may be expected to test video palettes, cellular telephone devices, data transceivers, and general-purpose ADCs and DACs. The test requirements for these various devices are very different from one another. For example, the cellular telephone base-band interface shown in Figure 1.2 may require a phase trajectory error test or an error vector magnitude test. Dedicated bench instruments can be purchased that are specifically designed to measure these application-specific parameters. It would be possible to install one of these stand-alone boxes into the tester and communicate with it through an IEEE-488 GPIB bus. However, if every type of DUT required two or three specialized pieces of bolt-on hardware, the tester would soon resemble Frankenstein's monster and would be prohibitively expensive.

The mixed-signal production tester cannot be focused toward a specific type of device if it is to handle a variety of DUTs. Instead of implementing tests like phase trajectory error and error vector magnitude using a dedicated bench instrument, the tester must emulate this type of equipment using a few general-purpose instruments. The instruments are combined with software routines to simulate the operation of the dedicated bench instruments.

5.1.2 Generic Tester Architecture

Mixed-signal testers come in a variety of "flavors" from a variety of vendors. Unlike the ubiquitous PC, testers are not at all standardized in architecture. Each ATE vendor adds special features that they feel will give them a competitive advantage in the marketplace. Consequently, mixed-signal testers from different vendors do not use a common software platform. Furthermore, a test routine implemented on one type of tester is often difficult to translate to another tester type because of subtle differences in the hardware tradeoffs designed into each tester. Nevertheless, most mixed-signal testers share many common features. In this chapter, we will examine these common features without delving too deeply into specific details for any particular brand of tester.

Figure 5.1 shows a generic mixed-signal tester architecture. It includes system computers, DC sources, DC meters, relay control lines, relay matrix lines, time measurement hardware, arbitrary waveform generators, waveform digitizers, clocking and synchronization sources, and a digital

subsystem for generating and evaluating digital patterns and signals. This chapter will briefly examine the operation of each of these tester subsystems.

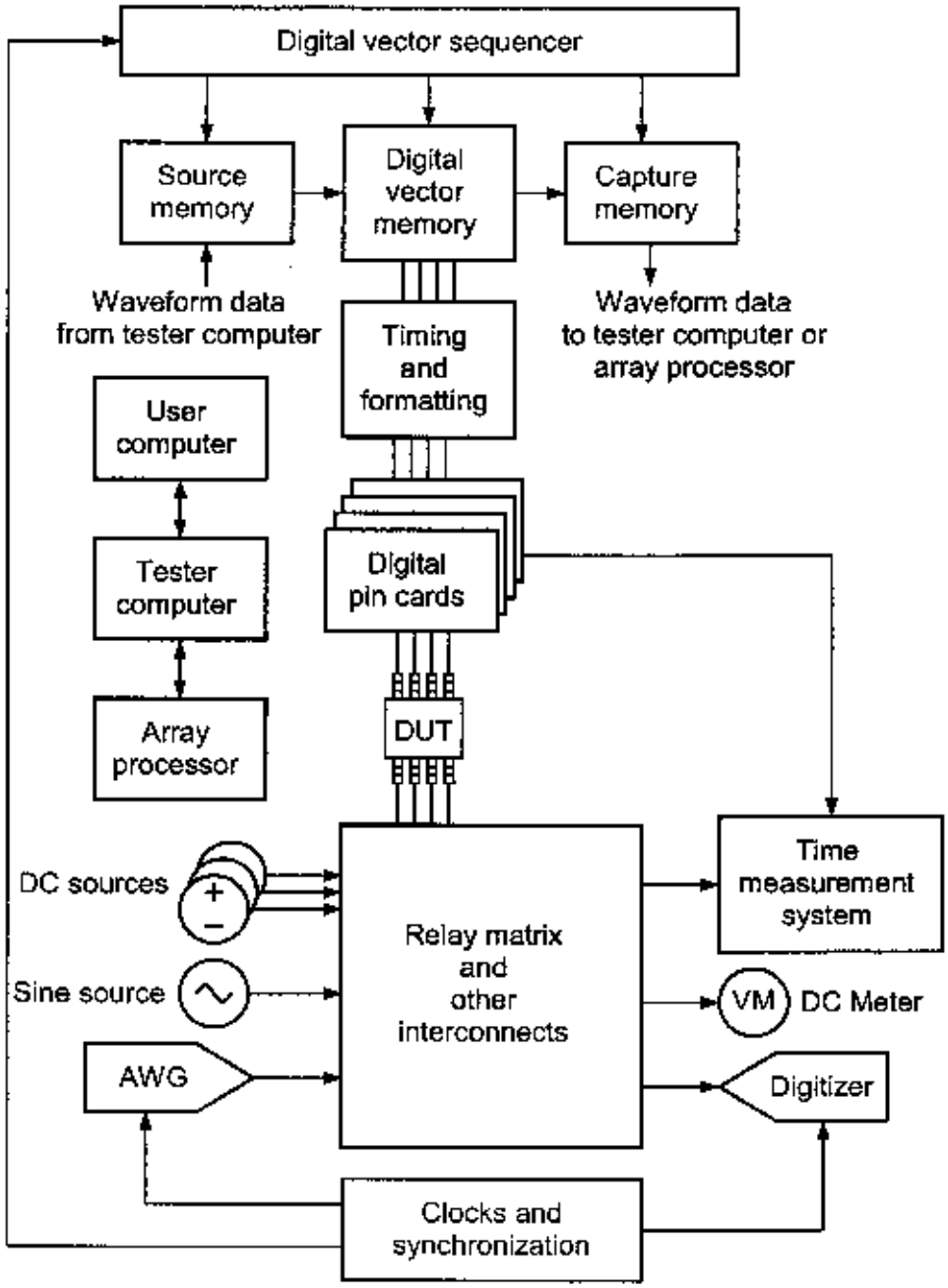

Figure 5.1. Generic mixed-signal tester architecture.

5.2 DC Resources

5.2.1 General-Purpose Multimeters

Most testers incorporate a high-accuracy multimeter that is capable of making fast DC measurements. A tester may also provide a slower, very high-accuracy voltmeter for more demanding measurements such as those needed in focused calibrations. However, this slower instrument may not be usable for production tests because of the longer measurement time. The fast, general-purpose multimeter is used for most of the production tests requiring a nominal level of accuracy.

A very simple DC voltmeter block diagram was presented in Figure 4.8. A more detailed DC multimeter structure is shown in Figure 5.2. This meter can handle either single-ended or differential inputs. Its architecture includes a high-impedance differential to single-ended converter (instrumentation amplifier), a low-pass filter, a programmable gain amplifier (PGA) for input ranging, a high-linearity ADC, integration hardware, and a sample-and-difference stage. It also includes an input multiplexer stage to select one of several input signals for measurement.

The instrumentation amplifier provides a high-impedance differential input. The high impedance avoids potential DC offset errors caused by bias current leaking into the meter. For single-ended measurements, the low end of the meter may be connected to ground through relays in the input selection multiplexer. The multimeter can also be connected to any of the tester's general-purpose DC voltage sources to measure their output voltage. The meter can also measure current flowing from any of the DC sources. This capability is very useful for measuring power supply currents, impedances, leakage currents, and other common DC parametric values. A PGA placed before the meter's ADC allows proper ranging of the instrument to minimize the effects of the ADC's quantization error (see Sections 4.1.4 and 4.2.8).

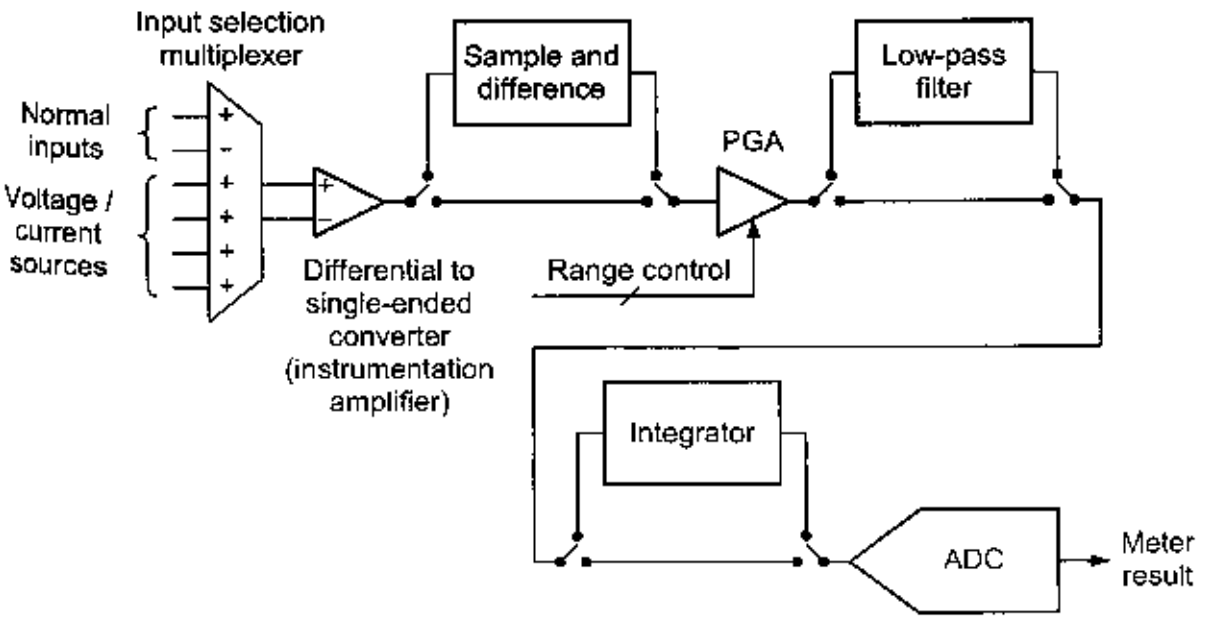

Figure 5.2. General-purpose DC multimeter.

The meter may also include a low-pass filter in its input path. The low-pass filter removes high-frequency noise from the signal under test, improving the repeatability of DC measurements. This filter can be enabled or bypassed using software commands. It may also have a programmable cutoff frequency so that the test engineer can make tradeoffs between measurement repeatability and test time (see Section 4.3.1). In addition, some meters may include an integration stage, which acts as a form of hardware averaging circuit to improve measurement repeatability.

Finally, a sample-and-difference stage is included in the front end of many ATE multimeters. The sample-and-difference stage allows highly accurate measurements of small differences between two large DC voltages. During the first phase of the measurement, a hardware sample-and-hold circuit samples a voltage. This first reference voltage is then subtracted from a second voltage (near the first voltage) using an amplifier-based subtractor. The difference between the two voltages is then amplified and measured by the meter's ADC, resulting in a high-resolution measurement of the difference voltage. This process reduces the quantization error that would otherwise result from a direct measurement of the large voltages using the meter's higher voltage ranges.

---

xample 5.1

A single-ended DC voltmeter has a resolution of 12 bits. It also features a sample-and-difference front-end circuit. We wish to use this meter to measure the differential offset voltage of a DUT's output buffer. Each of the two outputs is specified to be within a range of 1.35 V ± 10 mV, and the differential offset is specified to be ±5 mV. The meter input can be set to any of the following ranges: ±10 V, ±1 V, ±100 mV, ±10 mV, and ±1 mV. Assuming all components in the meter are perfectly linear (with the exception of the meter's quantization error), compare the accuracy achieved using two simple DC measurements with the accuracy achieved using the sample-and-difference circuit.

olution:

The simplest way to measure offset using a single-ended DC voltmeter is to connect the meter to the OUTP output, measure its voltage, connect the meter to the OUTN output, measure its voltage, and subtract the second voltage from the first (see Example 3.4). Using this approach, we have to set the meter's input range to ±10 V to accommodate the 1.35 V DUT output signals. Thus each measurement may have a quantization error of as much as $\pm\frac{1}{2}\left(\frac{20\text{ V}}{2^{12}-1}\right)=\pm 2.44\text{ mV}$.

Therefore, our total error might be as high as ±4.88 mV, assuming the quantization error from the first measurement is positive, while the quantization error from the second measurement is negative. Since we have a specification limit of ±5 mV, this will be an unacceptable test method.

Using the sample-and-difference circuitry, we could range the meter input to the worst-case difference between the two outputs, which is 5 mV, assuming a good device. The lowest meter range that will accommodate a 5-mV signal is ±10 mV. However, we also need to be able to collect readings from bad devices for purposes of characterization. Therefore, we will choose a range of ±100 mV, giving us a compromise between accuracy and characterization flexibility.

During the first phase of the sample-and-difference measurement, the voltage at the OUTN pin is sampled onto a holding capacitor internal to the meter. Then the meter is connected to the OUTP pin and the second phase of the measurement amplifies the difference between the OUTP voltage and the sampled OUTN voltage. Since the meter is set to a range of ±100 mV, a 100-mV difference between OUTP and OUTN will produce a full-scale 10 V input to the meter's ADC. This serves to reduce the effects of the meter's quantization error. The maximum error is given by $\pm\frac{1}{2}\left(\frac{100\text{ mV}}{2^{12}-1}\right)=\pm 12.2\ \mu\text{V}$. Again, our worst-case error is twice this amount, or ±24.4 μV, which is well within the requirements of our measurement.

5.2.2 General-Purpose Voltage/Current Sources

Most testers include general-purpose DC voltage/current sources, commonly referred to as *V/I sources* or *DC sources*. These programmable power supplies are used to provide the DC voltages and currents necessary to power up the DUT and stimulate its DC inputs. Many general-purpose supplies can force either voltage or current, depending on the testing requirements. On most testers, these supplies can be switched to multiple points on the DIB board using the tester's DC matrix (see Section 5.2.5). As mentioned in the previous section, the system's general-purpose meter can be connected to any DC source to measure its output voltage or its output current.

Figure 5.3 shows a conceptual block diagram of a DC source having a differential Kelvin connection. A differential Kelvin connection consists of four lines (high force, low force, high sense, and low sense) for forcing highly accurate DC voltages. The Kelvin connection forms a feedback loop that allows the DC source to force an accurate differential voltage through the resistive wires between the source and DUT. Without the Kelvin connection, the small resistance in the force line interconnections ($R_{TRACE\text{-}H}$ and $R_{TRACE\text{-}L}$) would cause a small *IR* voltage drop. The voltage drop would be proportional to the current through the DUT load (R_{LOAD}). The small

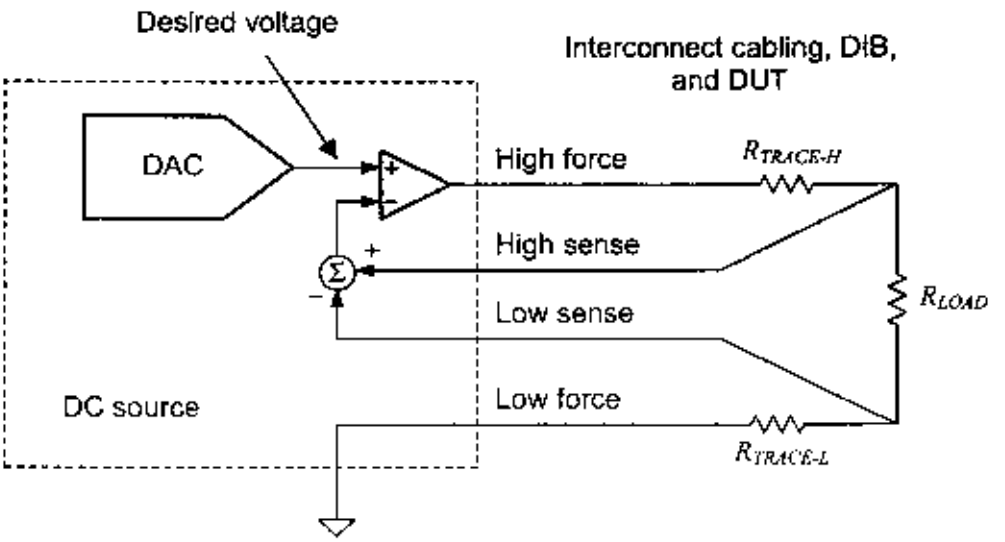

Figure 5.3. General-purpose DC source with Kelvin connections (conceptual diagram).

IR voltage drop would result in errors in the voltage across the DUT load. The sense lines of a Kelvin connection carry no current. Therefore, they are immune to errors caused by *IR* voltage drops.

A sense line is provided on the high side of the DC source and also on the low side of the source. The low-side sense line counteracts the parasitic resistance in the current return path. Since most instruments are referenced to ground, the low sense lines for all the DC instruments in a tester are often lumped into a single ground sense signal called DZ (device zero), DGS (device ground sense), or some other vendor-specific nomenclature. This is one of the most important signals in a mixed-signal tester, since it connects the DUT's ground voltage back to the tester's instruments for use as the entire test system's 0 V "golden zero reference." If any voltage errors are introduced into this ground reference signal relative to the DUT's ground, all the instruments will produce DC voltage offsets.

5.2.3 Precision Voltage References and User Supplies

Mixed-signal testers sometimes include high-accuracy, low-noise voltage references. These voltage sources can be used in place of the general-purpose DC sources when the noise and accuracy characteristics of the standard DC source are inadequate. One common example of a precision voltage reference application is the voltage reference for a high-resolution ADC or DAC. Any noise and DC error on the DC reference of an ADC or DAC translates directly into gain error and increased noise, respectively, in the output of the converter. A precision voltage reference is sometimes used to solve this problem.

Testers may also include nonprogrammable user power supplies with high output current capability. These fixed supplies provide common power supply voltages (±5 V, ±15 V, etc.) for DIB circuits such as op amps and relay coils. This allows DIB circuits to operate from inexpensive fixed power supplies having high current capability instead of tying up the tester's more expensive programmable DC sources.

5.2.4 Calibration Source

The mixed-signal tester's calibration source was discussed in detail in Section 4.2. The purpose of a calibration source is to provide traceability of standards back to a central agency such as the National Institute of Standards and Technology (NIST). The calibration source must be recalibrated on a periodic basis (six months is a common period). Often, the source is removed from the tester and sent to a certified standards lab for recalibration. The old calibration source is replaced by a freshly calibrated one so that the tester can continue to be used in production. On some testers, the high-accuracy multimeter serves as the calibration source. Also, some testers may have multiple instruments that serve as the calibration sources for various parameters such as voltage or frequency. Clearly, this is a highly tester-specific topic. Calibration and standards traceability is discussed in more detail in Chapter 10, "Focused Calibrations."

5.2.5 Relay Matrices

A relay matrix is a bank of electromechanical relays that provides flexible interconnections between many different tester instruments and the DUT. There may be several types of relay matrix in a tester, but they all perform a similar task. At different points in a test program, a particular DUT input may require a DC voltage, an AC waveform, or a connection to a

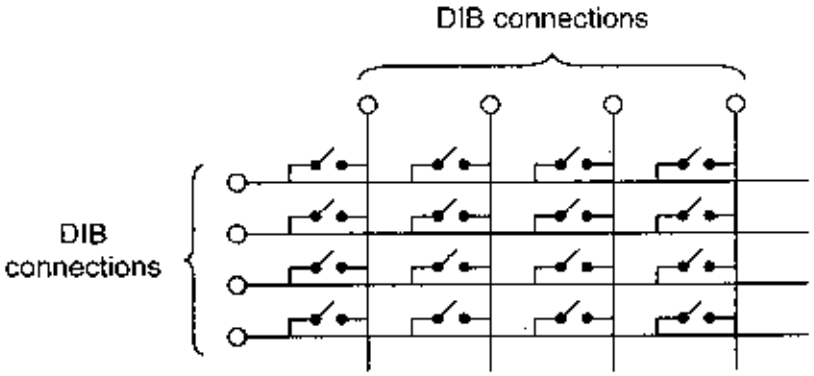

Figure 5.4. Instrument relay matrix.

voltmeter. A relay matrix allows each instrument to be connected to a DUT pin at the appropriate time.

A general-purpose 4 x 4 relay matrix is shown in Figure 5.4. General-purpose relay matrices are used to connect and disconnect various circuit nodes on the DIB board. They have no hardwired connections to tester instruments. Therefore, the purpose and functionality of a general-purpose relay matrix depends on the test engineer's DIB design. A more instrument-specific matrix is shown in Figure 5.5. It allows flexible interconnections between specific tester instruments and pins of the DUT through connections on the DIB board.

In addition to relay matrices, many other relays and signal paths are distributed throughout a mixed-signal tester to allow flexibility in interconnections without adding unnecessary relays to the DIB board. The exact architecture of relays, matrices, and signal paths varies widely from one ATE vendor's tester to the next.

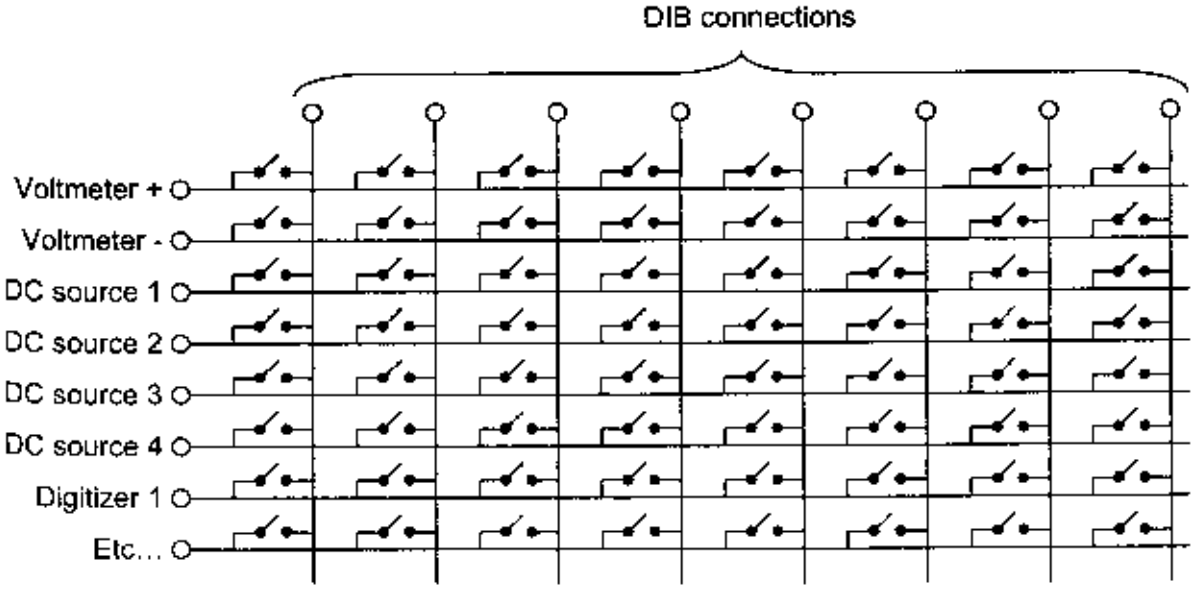

Figure 5.5. General-purpose relay matix.

5.2.6 Relay Control Lines

Despite the high degree of interconnection flexibility provided by the general-purpose relay matrix and other instrument interconnect hardware, there are always cases where a local DIB relay (placed near the DUT) is imperative. Usually the need for a local DIB relay is driven by performance of the DUT. For example, there is no better way to get a low-noise ground signal to the input of a DUT than to provide a local relay placed on the DIB directly between the DUT input and the DUT's local ground plane.

Certainly it is possible to feed the local ground through a DIB trace, through a remote relay matrix, and back through another DIB trace, but this connection scheme invariably leads to poor analog performance. The DIB traces are, after all, radio antennae. Many noise problems can be traced to poor layout of ground connections between the DUT and its ground plane. Local DIB relays minimize the radio antenna effect. Local DIB relays are also used to connect device outputs to various passive loads and other DIB circuits.

The test program controls the local DIB relays, opening and closing them at the appropriate time during each test. The relay coils are driven by the tester's relay control lines. A relay control line driver is shown in Figure 5.6. On some testers, the control line is capable of reading back the state of the voltage on the control line through a readback comparator. The readback comparator allows a low-cost method for determining the state of a digital signal.

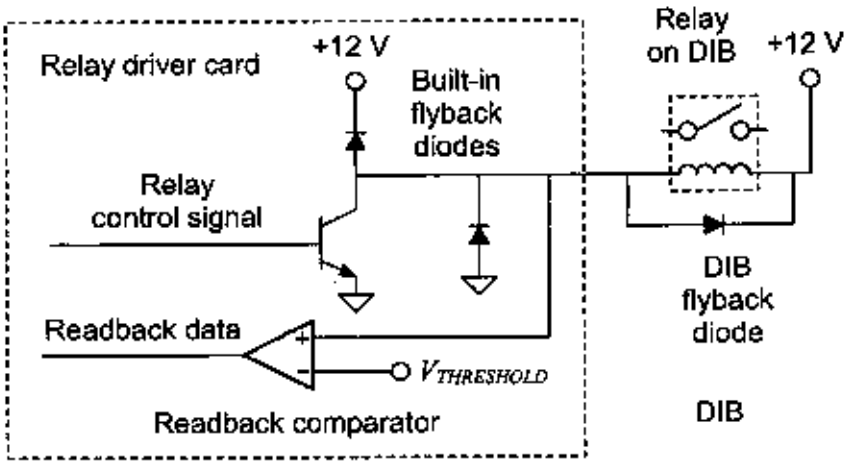

Figure 5.6. Relay coil driver with flyback protection diodes.

Relay coils produce an inductive kickback when the current is suddenly changed between the on and off states. The inductive kickback, or flyback as it is known, is induced according to the inductance formula $v(t) = L\ di/dt$. Since high kickback voltages could potentially damage the output circuits of the relay driver, its output circuits contain flyback protection diodes to shunt the excess voltage to a DC source or to ground. Many test engineers also add flyback diodes across the coils of the relay, as shown in Figure 5.6. The extra diode is probably redundant. However, many engineers consider it good practice to add extra flyback diodes even though they take up quite a bit of DIB board space. To eliminate the board space issue, the test engineer can choose slightly more expensive relays with built-in flyback diodes.

5.3 Digital Subsystem

5.3.1 Digital Vectors

A mixed-signal tester must test digital circuits as well as mixed-signal and analog circuits. The mixed-signal and digital-only sections of the DUT are exercised using the tester's digital subsystem. The digital subsystem can present high, low, and high-impedance (HIZ) logic levels to the DUT. It can also compare the outputs from the DUT against expected responses to determine whether the digital logic of the DUT has been manufactured without defects. The tester applies a sequence of drive data to the device and simultaneously compares outputs against expected results. Each drive/compare cycle is called a *digital vector*. A series of digital vectors is called a *digital pattern*. An example digital pattern for testing a simple 3-bit counter is shown in Figure 5.7. The vectors of a digital pattern are usually sourced at a constant frequency, although some testers allow the period of each vector to be set independently. The ability to change digital timing on a vector-by-vector basis is commonly called *timing on the fly*.

VECTOR	LABEL	COMMAND	TSET	RESET	CLOCK	Q2	Q1	Q0	COMMENT
0000000	TEST_COUNTER:		1	0	0	X	X	X	
0000001			1	0	1	X	X	X	Reset Counter
0000002			1	0	0	L	L	L	Check for all 0's
0000003			1	0	1	L	L	L	
0000004			1	1	0	L	L	L	Release Reset
0000005			1	1	1	L	L	H	Test for 001
0000006			1	1	0	X	X	X	
0000007			1	1	1	L	H	L	Test for 010
0000008			1	1	0	X	X	X	
0000009			1	1	1	L	H	H	Test for 011
0000010			1	1	0	X	X	X	
0000011			1	1	1	H	L	L	Test for 100
0000012			1	1	0	X	X	X	
0000013			1	1	1	H	L	H	Test for 101
0000014			1	1	0	X	X	X	
0000015			1	1	1	H	H	L	Test for 110
0000016			1	1	0	X	X	X	
0000017			1	1	1	H	H	H	Test for 111
0000018			1	1	0	X	X	X	
0000019			1	1	1	L	L	L	Test for wrap
0000020		HALT	1	1	0	X	X	X	

Figure 5.7. Digital pattern for 3-bit binary counter.

5.3.2 Digital Signals

In addition to the simple pass/fail digital pattern tests, the tester must also be capable of sourcing and capturing digital signals. Digital signals are digitized representations of continuous waveforms such as sine waves and multitones. Digital signals are distinct from digital vectors in that they typically carry analog signal information rather than purely digital information. Usually, the samples of a digital signal must be applied to a DUT along with a repetitive digital pattern that keeps the device active and initiates DAC and/or ADC conversions. Each cycle of the repeating digital pattern is called a *frame*.

During a mixed-signal test, the repeating frame vectors must be combined with the nonrepeating digital signal sample information to form a repetitive sampling loop. Combining the digital frame vectors with digital signal data, a long sequence of waveform samples can be sent to or captured from the DUT with a very short digital frame pattern. In effect, the sampling frame results in a type of data compression that minimizes the amount of vector memory needed for the tester's digital subsystem.

Looping frames are commonly used when testing DACs and ADCs. A sequence of samples must be loaded into a DAC to produce a continuous sequence of voltages at the DAC's output. In the case of ADC testing, digital signals must be captured and stored into a bank of memory as the looping frame initiates each ADC conversion.

5.3.3 Source Memory

When testing DACs, the digital signal samples representing the desired DAC analog waveform are typically computed in the tester's main test program code. The digital signal samples are stored into a digital subsystem memory block called *source memory* (or *send memory* in some testers). The digital frame data, on the other hand, are stored in vector memory. To generate a repeating frame with a new sample for each loop, the contents of the vector memory and source memory are spliced together in real time as the digital pattern is executed.

An example digital pattern for a DAC sine wave test is shown in Figure 5.8. This pattern shows a combination of a looping frame of ones and zeros combined with digital signal placeholders (W symbols in this example). Ws are placed wherever analog waveform sample data is to be supplied by source memory. Each W may be either high or low during each loop of the frame, depending on the contents of source memory. The address pointer for source memory is incremented by one sample each time through the frame loop so that a series of different samples can be sent to the DAC.

Because its data are generated algorithmically by the main test program, a digital signal can be modified quickly without changing the frame loop pattern. The ability to quickly modify the digital signal data is especially useful during the DUT debug and characterization phase. For example, a DAC may normally be tested using a 1-kHz sine wave digital signal. During the DAC characterization phase, however, the frequency might be swept from 100 Hz to 10 kHz to look for problem areas in the DAC's design. This would be impossibly cumbersome if the digital pattern had to be generated using an expanded, nonlooping sequence of ones and zeros. In fact, some tester architectures attempt to substitute deep, nonlooping vector memory in place of source memory. This may reduce the cost of tester hardware, but it invariably results in frustrated users. One of the main differences between a mixed-signal tester and a digital tester with bolt-on analog instruments is the presence of source and capture memories in the digital subsystem. Other differences will be pointed out throughout this chapter.

5.3.4 Capture Memory

Devices such as ADCs produce a series of digitized waveform samples that must be captured and stored into a bank of memory called *capture memory* (or *receive memory*). Capture memory serves the opposite function of source memory. Each time the sampling frame is repeated, the digital output from the device is stored into the capture memory. The capture memory address pointer is incremented each time a digital sample is captured. Once a complete set of samples

have been collected, they are transferred to an array processor or to the tester computer for analysis. A simple ADC sine wave test pattern is shown in Figure 5.9.

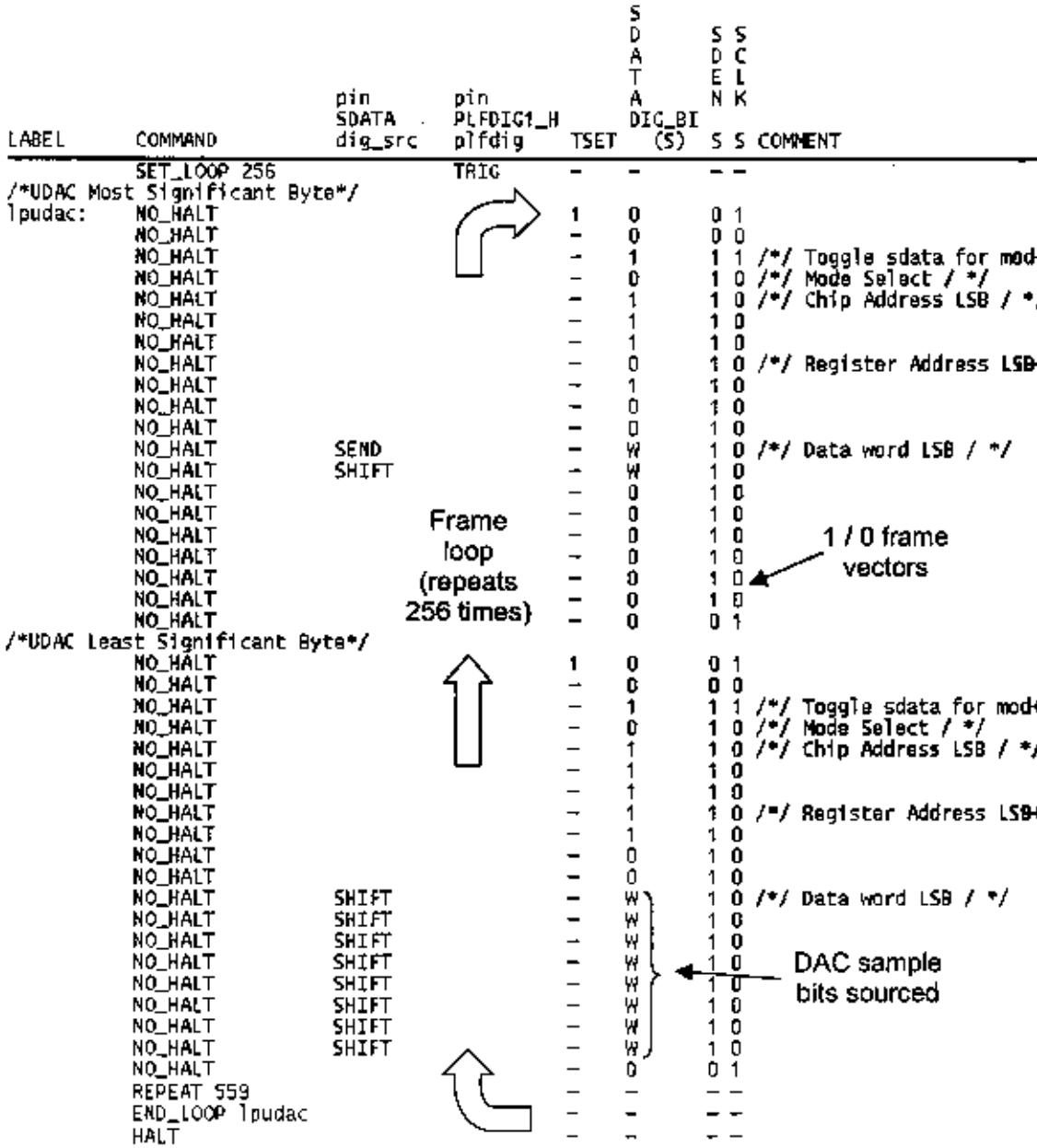

Figure 5.8. DAC data sourcing test pattern.

```
                                                    S
                                                    D      S S
                                                    A      D C
                                                    T      E L
                                pin       pin       A      N K
LABEL       COMMAND             PLFSRC1_H SDATA     DIG_8I
                                plfsrc    dig_cap   TSET   (S)  S S COMMENT
            SET_LOOP 256        START     TRIG      -      -      - -
/*ADC  Most Significant Byte*/
lpadc:      NO_HALT                                 1      0      0 1
            NO_HALT                                 -      0      0 0
            NO_HALT                                 -      1      1 1 /*/ Toggle sdata for mod+
            NO_HALT                                 -      1      1 0 /*/ Mode Select / */
            NO_HALT                                 -      1      1 0 /*/ Chip Address LSB / */
            NO_HALT                                 -      1      1 0
            NO_HALT                                 -      1      1 0
            NO_HALT                                 -      0      1 0 /*/ Register Address LSB+
            NO_HALT                                 -      1      1 0
            NO_HALT                                 -      0      1 0
            NO_HALT                                 -      0      1 0
            NO_HALT             SHIFT               -      X      1 0 /*/ Data word LSB / */
            NO_HALT             SHIFT               -      X      1 0
            NO_HALT                                 -      0      1 0
            NO_HALT                                 -      0      1 0
            NO_HALT                                 -      0      1 0
            NO_HALT                                 -      0      1 0
            NO_HALT                                 -      0      1 0
            NO_HALT                                 -      0      1 0
/*ADC  Least Significant Byte*/
            NO_HALT                                 1      0      0 1
            NO_HALT                                 -      0      0 0
            NO_HALT                                 -      1      1 1 /*/ Toggle sdata for mod+
            NO_HALT                                 -      1      1 0 /*/ Mode Select / */
            NO_HALT                                 -      1      1 0 /*/ Chip Address LSB / */
            NO_HALT                                 -      1      1 0
            NO_HALT                                 -      1      1 0
            NO_HALT                                 -      1      1 0 /*/ Register Address LSB+
            NO_HALT                                 -      1      1 0
            NO_HALT                                 -      0      1 0
            NO_HALT                                 -      0      1 0
            NO_HALT             SHIFT               -      X      1 0 /*/ Data word LSB / */
            NO_HALT             SHIFT               -      X      1 0
            NO_HALT             SHIFT               -      X      1 0
            NO_HALT             SHIFT               -      X      1 0
            NO_HALT             SHIFT               -      X      1 0
            NO_HALT             SHIFT               -      X      1 0
            NO_HALT             SHIFT               -      X      1 0
            NO_HALT             SHIFT               -      X      1 0
            NO_HALT             STORE               -      0      0 1
            REPEAT 559                              -      -      - -
            END_LOOP lpadc                          -      -      - -
            HALT                                    -      -      - -
```

Frame loop (repeats 256 times)

1 / 0 frame vectors

ADC sample bits captured

Figure 5.9. ADC data capture test pattern.

5.3.5 Pin Card Electronics

The pin card electronics for each digital channel are located inside the test head on most mixed-signal testers. A pin card electronics board may actually contain multiple channels of identical circuitry. Each channel's circuits consist of a programmable driver, a programmable

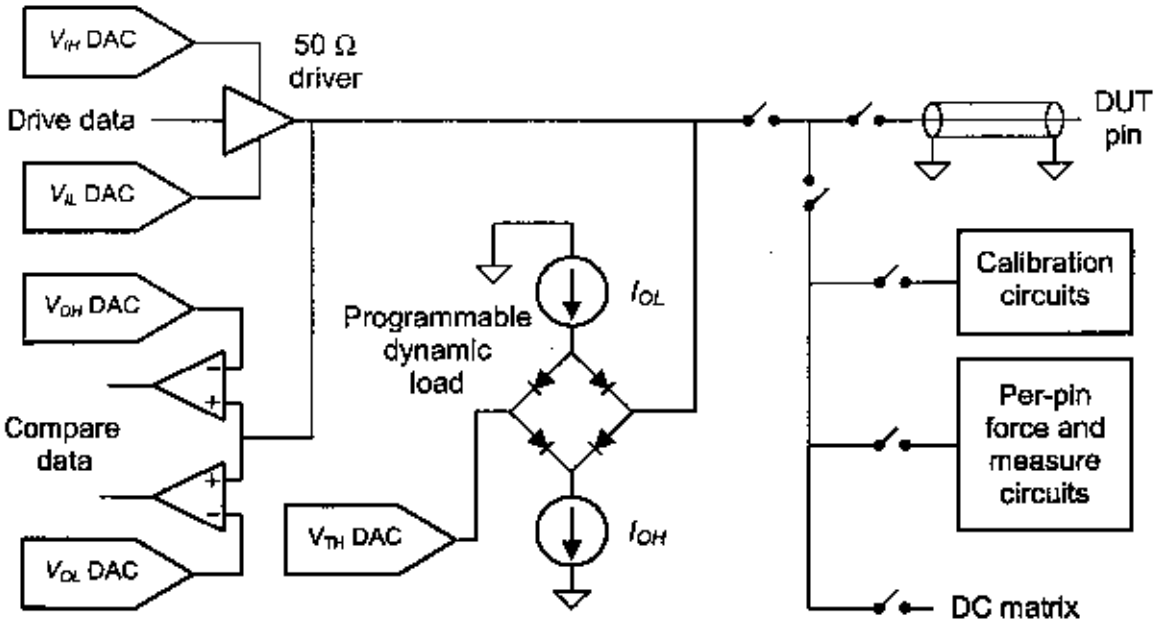

Figure 5.10. Digital pin card circuits.

comparator, various relays, dynamic current load circuits, and other circuits necessary to drive and receive signals to and from the DUT. A generic digital pin card is shown in Figure 5.10.

The driver circuitry consists of a fixed impedance driver (typically 50 Ω) with two programmable logic levels, V_{IH} and V_{IL}. These levels are controlled by a pair of driver level DACs whose voltages are controlled by the test program. The driver can also switch into a high-impedance state (HIZ) at any point in the digital pattern to allow data to come from the DUT into the pin card's comparator. The driver circuits may also include programmable rise and fall times, though fixed rise and fall times are more common. Normally the fixed rise and fall times are designed to be as fast as the ATE vendor can make them. Rise and fall times between 1 and 3 ns are typical in today's testers.

The comparator also has two programmable logic levels, V_{OH} and V_{OL}. These are also controlled by another pair of DACs whose voltages are controlled by the test program. The pin card comparator is actually a pair of comparators, one for the V_{OH} level and one for V_{OL}. If the DUT signal is below V_{OL}, then the signal is considered a logic low. If the DUT is above V_{OH}, then it is considered a logic high. If the DUT output is between these thresholds, then the output state is considered a midpoint voltage. If it is outside these thresholds, then it is considered a valid logic level. Comparator results can also be ignored using a mask. Thus there are typically three drive states (HI, LO, and HIZ) and five compare states (HI, LO, and MID, VALID, and MASK).

The usefulness of the valid comparison is not immediately obvious. If we want to test for valid V_{OH} and V_{OL} voltages from the output of a nondeterministic circuit such as an ADC, we cannot set the tester to expect HI or LO. This is because electrical noise in the ADC and tester will produce somewhat unpredictable results at the ADC output. However, we can set the tester to expect valid logic levels during the appropriate digital vectors without specifying whether the

ADC should produce a HI or a LO. While the pin card tests for valid logic levels, the samples from the ADC are collected into the digital capture memory for later analysis.

In addition to the drive and compare circuits, digital pin cards may also include dynamic load circuits. A dynamic load is a pair of current sources connected to the DUT output with a diode bridge circuit as shown in Figure 5.10. The diode bridge forces a programmable current into the DUT output whenever its voltage is below a programmable threshold voltage, V_{TH}. It forces current out of the DUT output whenever its voltage is above V_{TH}. The sink and source current settings correspond to the DUT's I_{OH} and I_{OL} specifications (see Section 3.12.4).

Another extremely important function that a digital pin card provides is its per-pin measurement capability. The per-pin measurement circuits of a pin card form a low-resolution, low-current DC voltage/current source for each digital pin. The per-pin circuits also include a relatively low-resolution voltage/current meter. The low-resolution and low-current capabilities are usually adequate for performing certain DC tests like continuity and leakage testing. These DC source and measure circuits can also be used for other types of simple DC tasks like input or output impedance testing.

Some testers may also include overshoot suppression circuits that serve to dampen the overshoot and undershoot characteristics in rapidly rising or falling digital signals. The overshoot and undershoot characteristics are the result of a low impedance DUT output driving into the DIB traces and coaxial cables leading to the digital pin card electronics. The ringing is minimized as the signal overshoot is shunted to a DC level through a diode.

Digital pin cards also include relays connected to other tester resources such as calibration standards and system DC meters and sources. These connections can be used for a variety of purposes, including calibration of the pin card electronics during the tester's system calibration process. The exact details of these connections vary widely from one tester type to another.

5.3.6 Timing and Formatting Electronics

When looking at a digital pattern for the first time, it is easy to interpret the ones and zeros very literally, as if they represent all the information needed to create the digital waveforms. However, most ATE testers apply timing and formatting to the ones and zeros to create more complicated digital waveforms while minimizing the number of ones and zeros that must be stored in pattern memory.

Timing and formatting is a type of data compression and decompression. The pattern data are formatted using the ATE tester's formatter hardware, which is typically located inside the tester mainframe or on the pin card electronics in the test head. Figure 5.11 shows how the pattern data are combined with timing and formatting information to create more complex waveforms. Notice that the unformatted data in Figure 5.11 require four times as much 1/0 information and four times the bit cell frequency to achieve the same digital waveform as the formatted data. Another key advantage to formatted waveforms is that the formatting hardware in a high-end mixed-signal tester is capable of placing the rising and falling edges with an accuracy of a few tens of picoseconds. This gives us better control of edge timing than we could expect to achieve using subgigahertz clocked digital logic.

The programmable drive start and stop times illustrated in Figure 5.11 are generated using digital delay circuitry inside the formatter circuits of the tester. Drive and compare timing is

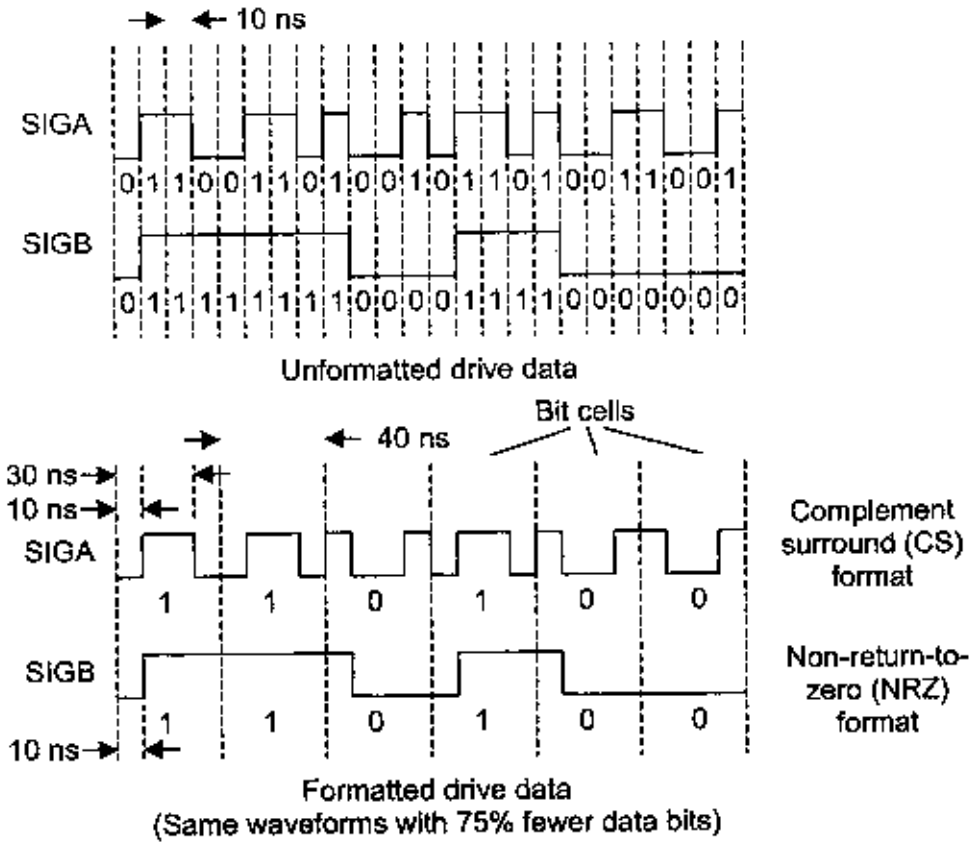

Figure 5.11. Drive data compression using formats and timing.

refined during a calibration process called *deskewing*. This allows subnanosecond accuracy in the placement of driven edges and in the placement of compare times (called *strobes* and *windows*). Strobe comparisons are performed at a particular point in time, while window comparisons are performed throughout a period of time. Window timing is typically used when comparing DUT outputs against expected patterns, while strobe timing is typically used when collecting data into capture memory. Again, this depends on the specific tester.

Figure 5.12 shows examples of several different formatting and timing combinations that create many different waveforms from the same digital data stream. In each case, the drive data sequence is 110X00. The compare data sequence is HHLXLL. Notice that certain formats such as Clock High and Clock Low ignore the pattern data altogether. Since digital pin cards can both drive and expect data, a distinction is made between a driven signal (1 or 0) and an expected signal (H or L). This notation is used for clarity in this book, though it is not universally used in the test industry. In fact, some digital pattern standards define H/L as driven data and 1/0 as expected data.

Example 5.2

Two digital signals, SIGA and SIGB, are generated by an ATE tester's pattern generator. The pattern generator's vector rate (i.e., its bit cell rate) is set to 4 MHz. SIGA is programmed to RO

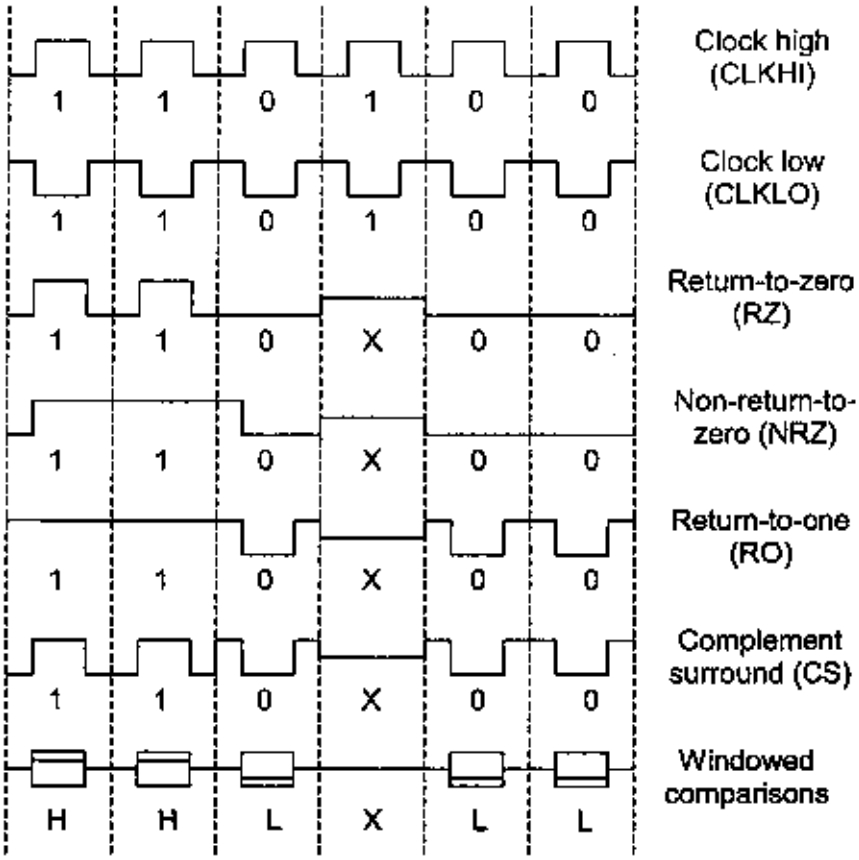

Figure 5.12. Some common digital formats.

format, while SIGB is programmed to NRZ format. The start time for SIGA is programmed to 50 ns and the stop time is programmed to 125 ns. Its initial state is programmed to logic high. The start time for SIGB is programmed to 25 ns and the stop time is programmed to 175 ns. Its initial state is programmed to logic low.

The following digital pattern is executed. Draw a timing diagram for the two signals SIGA and SIGB produced by this pattern. Show the bit cells in the timing diagram and calculate their period. Assume that we want to produce this same pair of signals using a bank of static random access memory (SRAM) whose address is incremented at a fixed rate (i.e., nonformated ones and zeros). What SRAM depth would be required to produce this same pair of signals?

SIGA	SIGB
0	1
0	0
1	1
0	1
1	0
1	1

Solution:

Figure 5.13 shows the digital waveforms resulting from the specified pattern and timing set. The vector rate is specified to be 4 MHz; so the bit cell period is 250 ns. Also notice that NRZ format does not have a stop time; so the 175-ns stop time setting is irrelevant. In this example, all

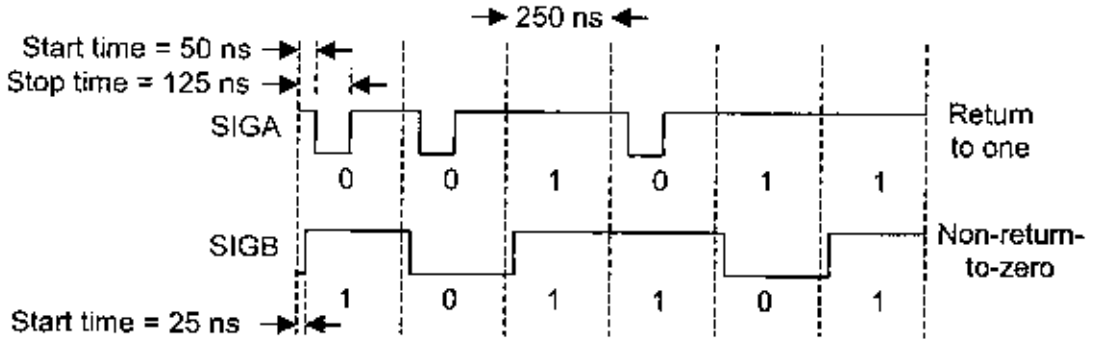

Figure 5.13. Formatted data using return-to-one and non-return-to-zero formats.

timing edges fall on 25-ns boundaries. If we wanted to generate this same pattern using nonformatted data from a bank of SRAM clocked at a fixed frequency, we would have to source a sequence of 6×(250 ns / 25 ns) = 60 bits from SRAM memory at a digital vector rate of 1/(25 ns) = 40 MHz.

5.4 AC Source and Measurement

5.4.1 AC Continuous Wave Source and AC Meter

The simplest way to apply and measure single-tone AC waveforms is to use a continuous wave source (CWS) and an RMS voltmeter. The CWS is simply set to the desired frequency and voltage amplitude to stimulate the DUT. The RMS voltmeter is equally simple to use. It is connected to the DUT output and the RMS output is measured with a single test program command.

But the CWS and RMS voltmeter suffer from a few problems. First, they are only able to measure a single frequency during each measurement. This would be acceptable for bench characterization, but in production testing it would lead to unacceptably long test times. As we will see in Chapters 6 through 9, DSP-based multitone testing is a far more efficient way to test AC performance because multiple frequencies can be tested simultaneously.

Another problem that the RMS voltmeter introduces is that it cannot distinguish the DUT's signal from distortion and noise. Using DSP-based testing, these various signal components can easily be separated from one another. This ability makes DSP-based testing more accurate and reliable than simple RMS-based testing. DSP-based testing is made possible with a more advanced stimulus/measurement pair, the arbitrary waveform generator and the waveform digitizer.

5.4.2 Arbitrary Waveform Generators

An arbitrary waveform generator (AWG) consists of a bank of waveform memory, a DAC that converts the waveform data into stepped analog voltages, and a programmable low-pass filter

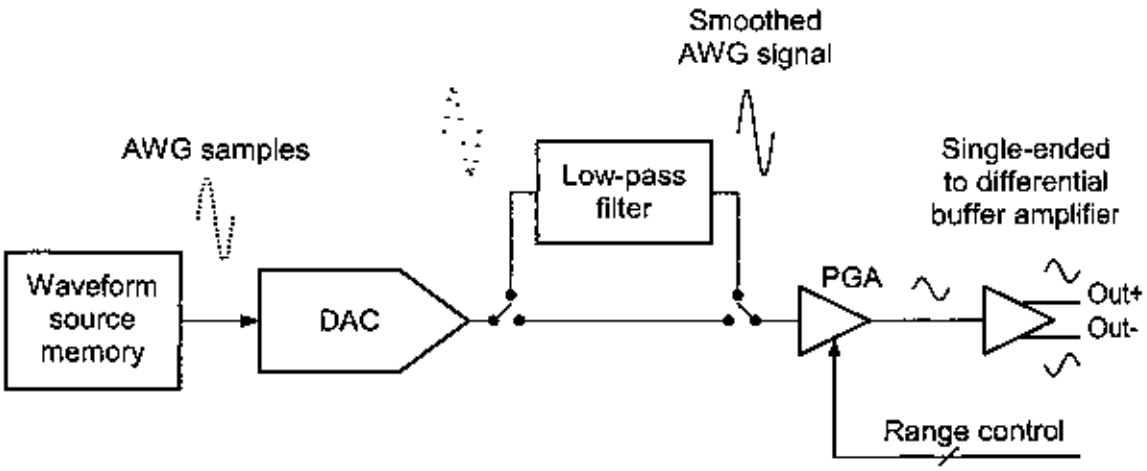

Figure 5.14. Arbitrary waveform generator.

section, which smoothes the stepped signal into a continuous waveform. An AWG usually includes an output scaling circuit (PGA) to adjust the signal level. It may also include differential outputs and DC offset circuits. Figure 5.14 shows a typical AWG and waveforms that might be seen at each stage in its signal path. (Mathematical signal samples are represented as dots to distinguish them from reconstructed voltages.)

An AWG is capable of creating signals with frequency components below the low-pass filter's cutoff frequency. The frequency components must also be less than one-half the AWG's sampling rate. This so-called Nyquist criterion will be explained in the next chapter, "Sampling Theory." An AWG might create the three-tone multitone illustrated in Figure 4.5. It might also be used to source a sine wave for distortion testing or a triangle wave (up ramp / down ramp) for ADC linearity testing (see Chapter 12, "ADC Testing"). Flexibility in signal creation is the main advantage of AWGs compared to simple sine wave or function generators.

5.4.3 Waveform Digitizers

An AWG converts digital samples from a waveform memory into continuous-time waveforms. A digitizer performs the opposite operation, converting continuous-time analog waveforms into digitized representations. The digitized samples of the continuous waveform are collected into a waveform capture memory. The structure of a typical digitizer is shown in Figure 5.15. A digitizer usually includes a programmable low-pass filter to limit the bandwidth of the incoming signal. The purpose of the bandwidth limitation is to reduce noise and prevent signal aliasing, which we will discuss in Chapter 6, "Sampling Theory."

Like the DC meter, the digitizer has a programmable gain stage at its input to adjust the signal level entering the digitizer's ADC stage. This minimizes the noise effects of quantization error from the digitizer's ADC. Waveform digitizers may also include a differential to single-ended conversion stage for measuring differential outputs from the DUT. Digitizers may also include a sample-and-hold circuit at the front end of the ADC to allow undersampled measurements of very high-frequency signals. Undersampling is explained in more detail in Chapter 6, "Sampling Theory."

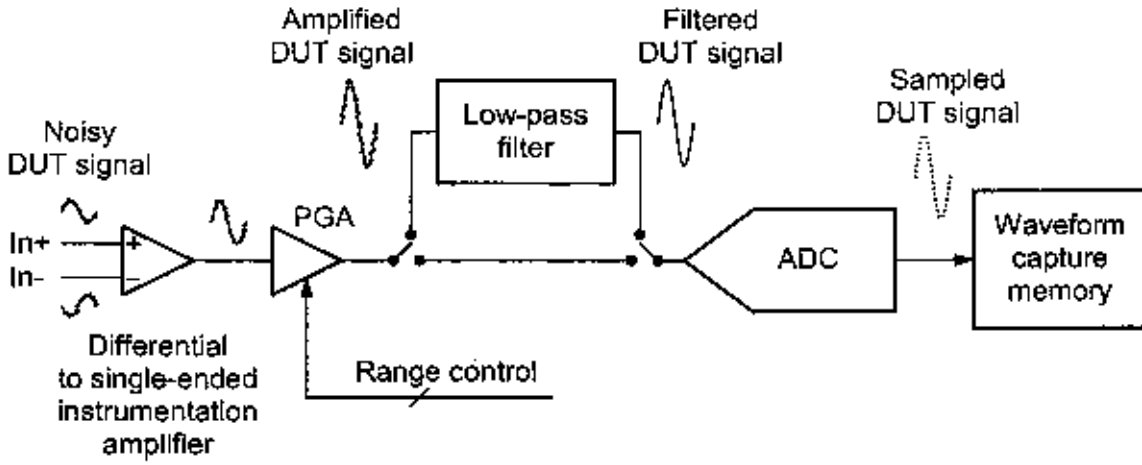

Figure 5.15. Waveform digitizer.

5.4.4 Clocking and Synchronization

Many of the subsections and instruments in a mixed-signal tester derive their timing from a central frequency reference. For example, the digital patterns in the frame loops in Figures 5.8 and 5.9 are generated at a specific frequency. This frequency determines the repetition rate of the sample loop, and therefore sets the frequency of the DAC or ADC sampling rates. The AWG and digitizer also operate from clock sources that must be synchronized to each other and to the digital pattern's frame loop repetition rate.

Figure 5.16 shows a clock distribution scheme that allows synchronized sampling rates between all the DSP-based measurement instruments. Since the clocking frequency for each instrument is derived from a common source, frequency synchronization is possible. Without precise sampling rate synchronization, the accuracy and repeatability of all the DSP-based measurements in a mixed-signal test program would be degraded.

The reason these clocks must all be synchronized will become more apparent in Chapter 6, "Sampling Theory," and Chapter 7, "DSP-Based Testing." Proper synchronization of sample rates between the various AWGs, digitizers, and digital pattern generators is another of the key distinguishing features of a mixed-signal tester. A digital tester with bolt-on analog instruments often lacks a good clocking and synchronization architecture.

5.5 Time Measurement System

5.5.1 Time Measurements

Digital and mixed-signal devices often require a variety of time measurements, such as frequency, period, duty cycle, rise and fall times, jitter, skew, and propagation delay. These parameters can be measured using the ATE tester's time measurement system (TMS).

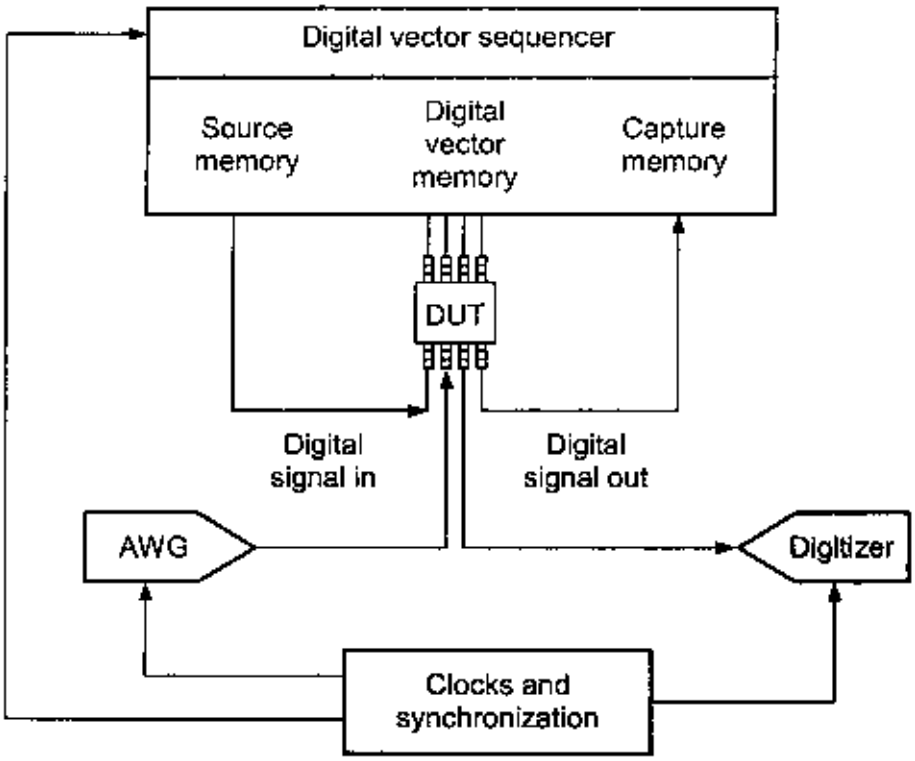

Figure 5.16. Synchronization in a mixed-signal tester.

Figure 5.17 illustrates several of the time measurement capabilities of a typical TMS. Most TMS instruments are capable of measuring these parameters within an accuracy of a few nanoseconds. Some of the more advanced TMS instruments can measure parameters such as jitter to a resolution of less than 1 ps.

Timing parameters that do not change from cycle to cycle (i.e., rise time, fall time, etc.) can sometimes be measured using a very high-bandwidth undersampling waveform digitizer. An undersampling digitizer is similar in nature to the averaging mode of a digitizing oscilloscope. Like digitizing oscilloscopes, undersampling digitizers require a stable, repeating waveform. Thus nonperiodic features such as jitter and random glitches cannot be measured using an undersampling approach. Unfortunately, undersampling digitizers are often considerably slower than dedicated time measurement instruments.

5.5.2 Time Measurement Interconnects

One of the most important questions to consider about a TMS instrument is how its input and interconnection paths affect the shape of the waveform to be measured. It does little good to measure a rise time of 1 ns if the shape of the signal's rising edge has been distorted by a 50-Ω coaxial connection. It is equally futile to try to measure a 100-ps rising edge if the bandwidth of the TMS input is only 300 MHz. Accurate timing measurments require a high-quality signal path between the DUT output and the TMS time measurement circuits.

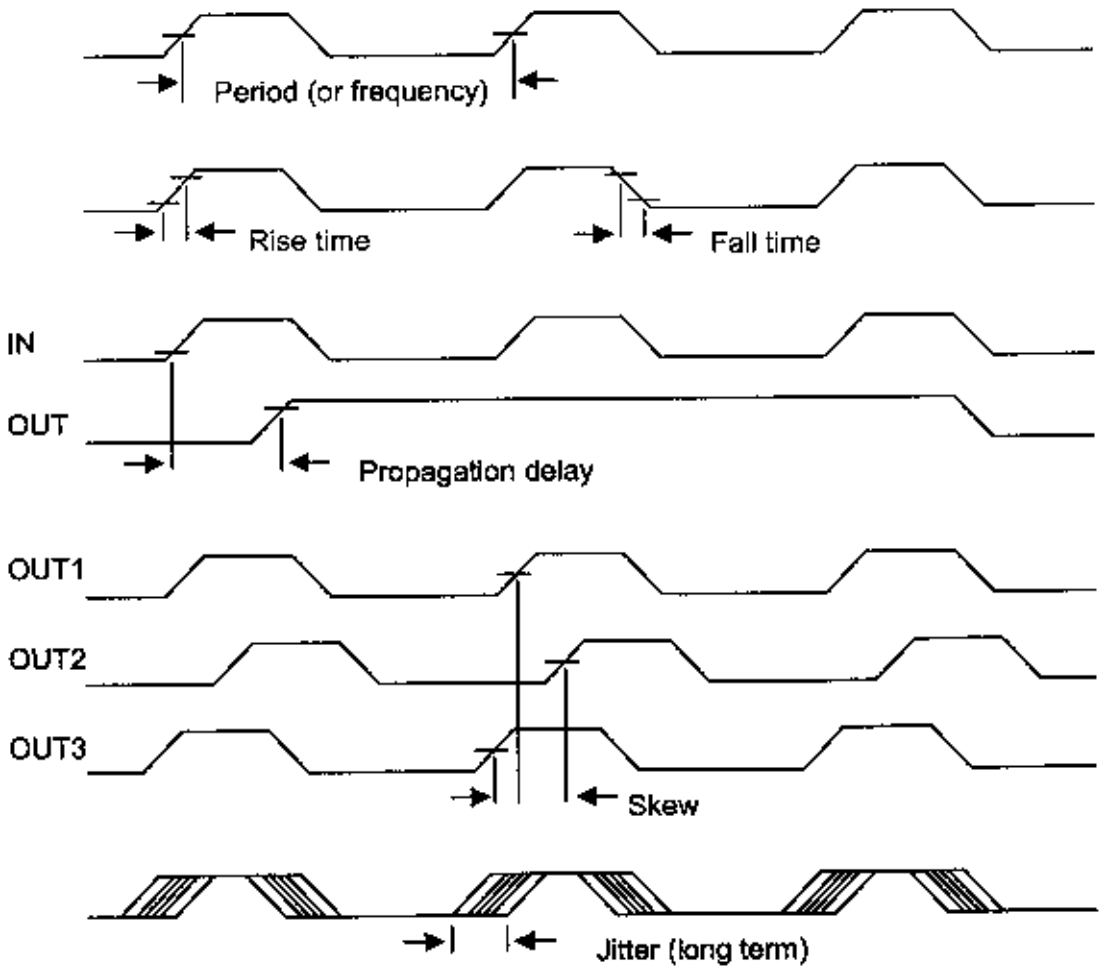

Figure 5.17. Time measurements.

5.6 Computing Hardware

5.6.1 User Computer

Mixed-signal testers typically contain several computers and signal processors. The test engineer is most familiar with the user computer, since this is the one which is attached to the keyboard. The user computer is responsible for all the editing and compiling processes necessary to debug a test program. It is also responsible for keeping track of the datalogs and other data collection information. On low-cost testers, the user computer may also drive the measurement electronics as well. On more advanced mainframe testers, the execution of the test program, including I/O functions to the tester's measurement electronics, may be delegated to one or more tester computers located inside the tester's mainframe.

5.6.2 Tester Computer

The tester computer executes the compiled test program and interfaces to all the tester's instruments through a high-speed data backplane. By concentrating most of its processing power on the test program itself, the tester computer can execute a test program more efficiently than the user computer. The tester computer also performs all the mathematical operations on the data collected during each test. In some cases, the more advanced digital signal processing (DSP) operations may be handled by a dedicated array processor to further reduce test time. However, computer workstations have become fast enough in recent years that the DSP operations are often handled by the tester computer itself rather than a dedicated array processor.

5.6.3 Array Processors and Distributed Digital Signal Processors

Many mixed-signal testers include one or more dedicated array processors for performing DSP operations quickly. This is another difference between a mixed-signal tester and a bolted-together digital/analog tester. Some mixed-signal instruments may even include local DSP processors for computing test results before they are transferred to the tester computer. This type of tester architecture and test methodology is called *distributed processing*. Distributed processing can reduce test time by splitting the DSP computation task among several processors throughout the tester. Test time is further reduced by eliminated much of the raw data transfer that would otherwise occur between digitizer instruments and a centralized tester computer or array processor. Unfortunately, distributed processing may have the disadvantage that the resulting test code may be harder to understand and debug.

5.6.4 Network Connectivity

The user computer and/or tester computer are typically connected into a network using ethernet or similar networking hardware. This allows data and programs to be quickly transferred to the test engineer's desk for offline debugging and data analysis. It also allows for large amounts of production data to be stored and analyzed for characterization purposes.

5.7 Summary

In this chapter we have examined many of the common building blocks of a generic mixed-signal tester. Of course, there are many differences between any two ATE vendors' preferred tester architectures. For example, ATE Vendor A may use a sigma-delta-based digitizer and AWG, while ATE Vendor B may choose to use a more conventional sucessive approximation architecture for its AWG and digitizer. Each architecture has advantages and disadvantages, which the test engineer must deal with. The test engineer's approach to measuring a given parameter will often be driven by the vendor's architectural choices. In the end, though, each tester has to test the same variety of mixed-signal parameters regardless of its architectural peculiarities. A test engineer's job often involves testing parameters the tester was simply not designed to measure. This can be one of the more challenging and interesting parts of a test engineer's task.

In the following chapters we will see how digitizers, AWGs, and digital pattern generators, combined with digital signal processing, can provide greater speed and accuracy than conventional measurement techniques. We will also explain why it is so critical to mixed-signal testing that we achieve precise synchronization of sampling frequencies bewteen all the tester's

instruments. Although the next two chapters represent some of the most difficult material in the book, they also contain some of the most important material. Most mixed-signal testing involves DSP-based measurements of one type or another; so the student will need to devote special attention to these chapters.

Problems

5.1. Name at least six types of subsystems found in a typical mixed-signal tester.

5.2. What is the purpose of the low-pass filter in a DC multimeter's front end?

5.3. What is the purpose of the PGA in a DC multimeter's front end?

5.4. A single-ended DC voltmeter features a sample-and-difference front-end circuit. We wish to use this meter to measure the differential offset voltage of a DUT's output buffer. Each of the two outputs is specified to be within a range of 3.5 V ± 25 mV, and the differential offset is specified in the device data sheet to be ±15 mV. The meter input can be set to any of the following ranges: ±10 V, ±5 V, ±2 V, and ±1 V. The meter has a maximum error of 0.1% of its programmed range. The error includes all sources of inaccuracy (quantization error, linearity error, gain error, etc.). Compare the accuracy achieved using two simple DC measurements with the accuracy achieved using the sample-and-difference circuit. Assume no errors due to nonrepeatability.

5.5. Why are Kelvin connections used to connect high-current DC power supplies to the DUT?

5.6. Name an instance where a local DIB relay might prove to be a better choice for interconnecting signals than a general-purpose relay matrix.

5.7. What is the purpose of the diodes in the output stage of the relay driver in Figure 5.6?

5.8. What is the difference between a digital pattern and a digital signal?

5.9. Why are the number of vectors in the frame loop and the frequency of the digital vectors in a sampling frame important when developing a digital pattern for a mixed-signal test?

5.10. What is the purpose of source memory?

5.11. What is the purpose of capture memory?

5.12. In Figure 5.8, SDATA is a serial input/output (I/O) interface to a DUT containing a 10-bit DAC. The drive data for SDATA consists of a combination of ones, zeros, and Ws. The ones and zeros represent digital logic states that select the DAC for writing. The 10-bit write is broken into two eight-bit write operations. (The first 8-bit write operation contains only the two most significant bits of DAC data.) The Ws represent digital signal data. The digital vectors are supplied at a constant rate of 6 MHz. This pattern supplies 256 samples to the DAC using a total of 600 vectors (40 + 559 + 1) per frame loop. At what rate are the digital signal samples written to the DAC? How long does it take to supply all 256 samples to the DAC?

5.13. In Figure 5.9, the SDATA interface is used to read samples from an ADC located on the DUT from Problem 5.12. The Xs on SDATA represent the time at which the 10 bits of each ADC sample are captured into capture memory. The Xs represent a high-impedance

drive state. Why might Xs be required at this point in the pattern rather than ones and zeros?

5.14. Why is formatting and timing information combined with one/zero information to produce digital waveforms?

5.15. A series of digital bits are driven from a digital pin card at a rate of 1 MHz (1-μs period). The series of bits are 10110X1. The format for this pin is set to return-to-zero (RZ) format. Its initial state is set to logic low. The start time for the drive data is set to 500 ns, and the stop time is set to 900 ns. Draw this waveform using the notation in Figure 5.12. Draw the waveform timing approximately to scale. Next, draw the waveform that would result if we set the format to non-return-to-zero (NRZ). To produce these waveforms using clocked digital logic without timing and formatting circuits, what clock rate would be required? If we wanted to be able to set the start and stop times to 500 and 901 ns, respectively, at what rate would we have to operate the clocked digital logic?

5.16. Name two reasons that AWGs and digitizers are used in mixed signal testing rather than CW sources and RMS voltmeters.

5.17. What is the purpose of the low-pass filter in the AWG illustrated in Figure 5.14?

5.18. Why is a programmable gain amplifier needed in the front end of the waveform digitizer illustrated in Figure 5.15?

5.19. What is the purpose of distributed digital signal processing hardware?

CHAPTER 6

Sampling Theory

6.1 Analog Measurements Using DSP

6.1.1 Traditional versus DSP-Based Testing of AC Parameters

AC measurements such as gain and frequency response can be measured with relatively simple analog instrumentation, as mentioned in Section 5.4.1. To measure gain, an AC continuous sine wave generator can be programmed to source a single tone at a desired voltage level, V_{in}, and at a desired frequency. A true RMS voltmeter can then measure the output response from the DUT, V_{out}. Then gain can be calculated using a simple formula: $gain = V_{out}/V_{in}$.

The pure analog approach to AC testing suffers from a few problems, though. First, it is relatively slow when AC parameters must be tested at multiple frequencies. For example, each frequency in a frequency response test must be measured separately, leading to a lengthy testing process. Second, traditional analog instrumentation is unable to measure distortion in the presence of the fundamental tone. Thus the fundamental tone must be removed with a notch filter, adding to test hardware complexity. Third, analog testing measures RMS noise along with RMS signal, making results unrepeatable unless we apply averaging or band-pass filtering.

In the early 1980s, a new approach to production testing of AC parameters was widely adopted in the ATE industry. The new approach became known as *DSP-based testing*.[1] Digital signal processing (DSP) is a powerful methodology that allows faster, more accurate, more repeatable measurements than traditional AC measurements using an RMS voltmeter. A mixed-signal test engineer will never be fully competent without a strong background in signal processing theory. Unfortunately, a full treatment of sampling theory and DSP is well beyond the scope of this book. Other texts have covered the subject of signal processing in much more detail.[2-4]

The reader is assumed to already have a strong theoretical background in DSP, although this book will undoubtedly fall into the hands of the DSP novice as well. We will review the basics of sampling theory and DSP as they apply to mixed-signal testing, without giving the subject an in-depth treatment. Hopefully, this introductory coverage will both refresh the experienced reader's memory of DSP and allow the novice to understand the fundamentals of DSP-based testing.

Before we can discuss DSP-based testing, we must first understand sampling theory for both analog-to-digital converters and digital-to-analog converters. In this chapter, we will examine the basics of sampling theory before proceeding to a more detailed study of DSP-based testing in Chapter 7.

6.2 Sampling and Reconstruction

6.2.1 Use of Sampling and Reconstruction in Mixed-Signal Testing

Sampling and reconstruction are the processes by which signals are converted from the continuous (i.e., analog) signal domain to the discrete (i.e., digital) signal domain and back again. Both sampling and reconstruction are used extensively in mixed-signal testing. The ATE tester samples and reconstructs signals to stimulate the DUT and measure its response. The DUT may also sample and reconstruct signals as part of its normal operation. Both mathematical and physical sampling and reconstruction occur as the DUT is tested. Figure 6.1 illustrates the various types of sampling and reconstruction that occur when the voice-band interface circuit of Figure 1.2 is tested.

In a purely mathematical world, a continuous waveform can be sampled and then reconstructed without loss of signal quality, as long as a few constraints are met. Unfortunately, a number of imperfections are introduced in the physical world that make the conversion between continuous time and discrete time fall short of the mathematical theory. Many of these imperfections will be discussed in this section.

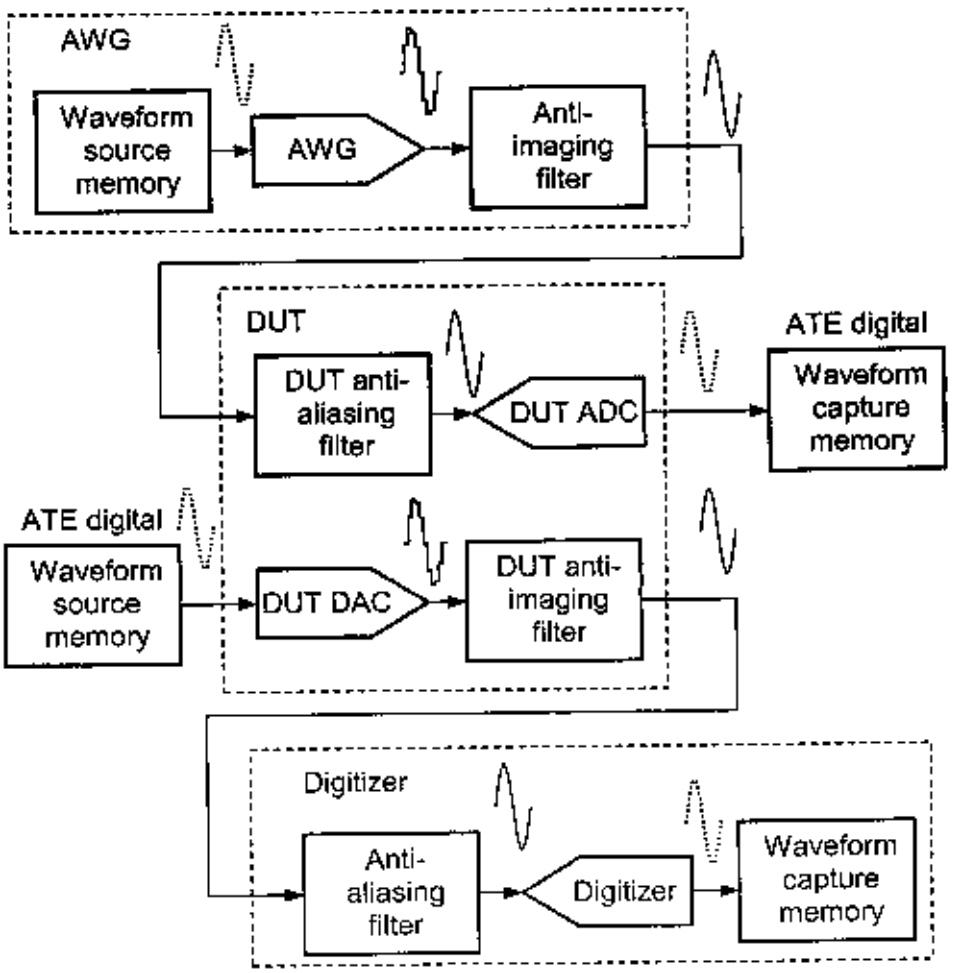

Figure 6.1. Various test signals associated with a voice-band interface circuit.

6.2.2 Sampling: Continuous-Time and Discrete-Time Representation

Many signals in the physical world around us are continuous (i.e., analog) in nature. Familiar examples of real-world analog signals include sound waves, light intensity, temperature, and pressure. Many modern electronic systems, such as the cellular telephone example in Chapter 1, must convert the continuous signals in the physical world into discrete digital representations compatible with digital storage, digital transmission, and mathematical processing. Continuous signals are often described by mathematical equations, such as

$$v(t) = A\ \sin(2\pi f_o t + \phi) \tag{6.1}$$

where $v(t)$ is a continuous function of time t, whose value in this particular case changes in a sinusoidal manner with amplitude A, frequency f_o, and phase shift ϕ.

Sampling is a process in which a continuous-time signal is converted into a sequence of discrete samples uniformly spaced at intervals of T_s seconds, often written as

$$v[n] = v(t)\big|_{t=nT_s} \tag{6.2}$$

where $v[n]$ defines the values of $v(t)$ at the sampling instants defined at $t=nT_s$. Such a process is depicted in Figure 6.2. We refer to T_s as the *sampling period* and its reciprocal $F_s=1/T_s$, as the *sampling frequency* or *sampling rate*, and n as an arbitrary integer. To simplify our notation, it is common practice to drop the T_s term in the argument of Eq. (6.2) as it is assumed to be constant for all time. The continuous waveform $v(t)$ is said to exist in continuous time, while the sampled waveform $v[n]$ is said to exist in discrete time. For example, substituting Eq. (6.1) into (6.2), we can write

$$v[n] = A\ \sin(2\pi f_o n T_s + \phi) = A\ \sin\left(2\pi \frac{f_o}{F_s} n + \phi\right) \tag{6.3}$$

For reasons that will become clear later in this chapter, we often impose the condition that the ratio f_o/F_s be a rational fraction, $f_o/F_s=M/N$, where M and N are integers, allowing one to write

$$v[n] = A\ \sin\left(2\pi \frac{M}{N} n + \phi\right) \tag{6.4}$$

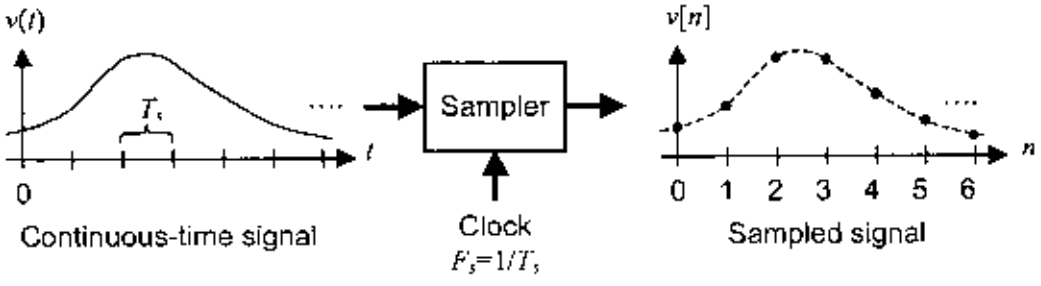

Figure 6.2. Continuous-time signal and its sampled equivalent.

Discrete signals such as this can then be stored in computer arrays and processed using DSP functions.

Up to this point we have defined a sampled waveform in the discrete-time domain as a sequence of numbers defined by $v[n]$. We can also define a sampled waveform as a continuous function of time. The use of this alternative notation is important in the next section where the samples are converted back into the original continuous-time signal. To enable such a description we must make use of the concept of impulse functions. Mathematically, an impulse function, denoted by $\delta(t)$, is defined as having zero amplitude everywhere except at $t=0$, where it is infinitely large in such a way that it contains unit area under its curve, as depicted by the following two rules

$$\delta(t) = 0, \; t \neq 0 \tag{6.5}$$

and

$$\int_{-\infty}^{\infty} \delta(t)\, dt = 1 \tag{6.6}$$

It is important to realize that no function in the ordinary sense can satisfy these two rules. However, we can imagine a sequence of pulselike functions that have progressively taller and thinner peaks, with the area under the curve remaining equal to unity as illustrated in Figure 6.3(a). If we take this argument to the limit, letting the pulse width go to zero while the pulse height goes to infinity, then we have what we refer to as an impulse function. It should be obvious from this description that we are going to encounter some difficulty in graphing the impulse function. Hence, an impulse is graphically represented by an arrow whose height is equal to the area (voltage × time) under the impulse, as shown in Figure 6.3(b).

An important property of impulse functions is the so-called *sifting property*, defined by

$$\int_{-\infty}^{\infty} v(t)\, \delta(t - t_0)\, dt = v(t_0) \tag{6.7}$$

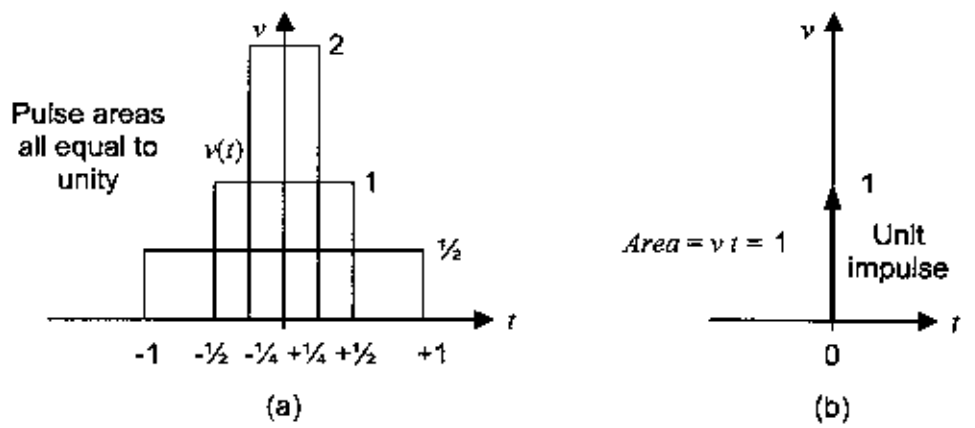

Figure 6.3. Impulse definition.