Wladyslaw Grabinski
Thomas Gneiting
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Power/ HV MOS Devices Compact Modeling

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Preface

The continuous progress in modern power device technology is increasingly supported by power-specific modeling methodologies and dedicated simulation tools. These enable the detailed analysis of operational principles on the the device and on the system level; in particular, they allow the designer to perform trade-off studies by investigating the operation of competing design variants in a very early stage of the development process. Furthermore, using predictive computer simulation makes it possible to analyze the device and system behavior not only under regular operating conditions, but also at the rim of the safe-operating area and beyond of it, where destructive processes occur that limit the lifetime of a power system. Thus, virtual experimentation and virtual test by computer simulations have become an integral part of the design methodology for electronic power devices, modules, and entire components and systems in order to achieve cost-efficient and time-economizing development cycles. This is, in particular, relevant with a view to satisfying all requirements concerning robustness against harsh and exceptional operating conditions ("ruggedness"), long-term reliability, energy efficiency, and cost reduction by increasing integration of multiple functionality in one module.

A successful strategy for "virtual prototyping" of power systems requires modeling methodologies on different levels of abstraction and computational expense. This monography addresses the most important aspects to be focussed on in seven chapters contributed by world-known experts in their field. In the first and fifth chapter state-of-the-art high-voltage device models on the continuous field level and their implementation in numerical simulation are discussed, with emphasis on the consistent treatment of electro-thermally coupled fields and coupled domains. This kind of physically-based modeling is the indispensable prerequisite for predictive "high-fidelity" computer simulations, but computationally very expensive or even prohibitive, so that they cannot be used in a top-down/bottom-up design optimization loop.

It is therefore that over the past decades "order-reduced" compact models have been developed, which are simplified to an extent that the computational cost becomes affordable, but are still phyics-based and, hence, scalable and predictive.

The major part of this book deals with alternative approaches to accurate and efficient high-voltage device compact models as developed during the past years at renowned institutions around the world. While unipolar transport in power

MOSFETs is addressed in Chapters 2–4, distributed macromodels for bipolar transport in IGBTs are presented in Chapter 6.

The book concludes with an example of a modern web-based simulation platform ready for the easy-to-use implementation of the above-discussed compact modeling methodologies.

I feel that this monography may serve as a "catalytic link" between the communities of power device technologists, power electronic engineers, and IC designers in order to produce new synergies in the R&D of power systems, a field with a prosperous future in our high-tech societies.

Technische Universitaet Muenchen Prof. Dr. Gerhard Wachutka

Contents

Introduction

Wladek Grabinski and Thomas Gneiting

Semiconductor power electronics plays a dominant role due its increased efficiency and high reliability in various domains including the medium and high electrical drives, automotive and aircraft applications, electrical power conversion, etc. Our book will cover a very extensive range of topics related to the development and characterization of power/high voltage (HV) semiconductor technologies as well as modeling and simulations of the power/HV devices and smart power integrated circuits (ICs). Emphasis is placed on the practical applications of the advanced semiconductor technologies and the device level compact/SPICE modeling. Our book is intended to provide reference information by selected, leading authorities in their domain of expertise. They are representing both academia and industry. All of them have been chosen because of their intimate knowledge of their subjects as well as their ability to present them in an easily understandable manner.

This book is aimed at power/HVMOS integrated circuit designers, computer-aided design (CAD) engineers, semiconductor physics students as well as wafer fab process engineers working on device, SPICE/compact level. We could summarize the goals of the book as follows:

– Introduce the reader in a consistent manner to the main steps of the compact model developments, including advanced 2/3D process and device TCAD simulations, consistent and accurate MOSFET modeling founded on the physical concepts of the surface potential and charge-based modeling coherent with related electrical devices' characterization.
– To illustrate the impact of the device level modeling on the IC designs using selected examples supported by corresponding TCAD and CAD, SPICE level, simulation solutions.

We have structured this book to address the key aspects of the compact model developments, showing well structured flow of the power/HVMOS models implantation and dissimilation as well as its standardization tasks. Following that organization the book is divided into subsequent chapters:

In the first chapter of this book, Oliver Triebl and Tibor Grasser are introducing the TCAD simulation tools for device modeling and recommending how they can be used for advanced modeling tasks. Selected simulations examples show the

influence of fundamental physical models and demonstrate how TCAD gives the device engineer an insight into the device behavior and analyze that information for further device optimization using the valid drift–diffusion framework. Moreover, advanced transport models such as energy-transport, six moment models, and Monte Carlo simulation which have gained some interest during the last decade are briefly summarized as well.

Bulk CMOS models make up the main stream of the compact models. Next three chapters discuss leading concepts of the physics based models for advanced CMOS technologies.

H.J. Mattausch et al. are discussing modeling concepts of HiSIM_HV, the surface-potential-based HiSIM (Hiroshima-university STARC IGFET Model) model for conventional bulk MOSFETs. The HiSIM_HV modeling concept is valid for modeling both, a laterally-diffused asymmetrical structure, known as LDMOS structure as well as a symmetrical structure with extended drift regions at both source and drain, which are distinguished by referring to it as HVMOS, more generalized modeling case. The HiSIM core model is then extended and enhanced by number of the modular additions to construct the HiSIM-HV model. New extensions are mainly capturing very specific properties of drift regions added to the MOSFET core to obtain the high-voltage capabilities including the self-heating effect essential for modeling of the semiconductor device power dissipation of a high-voltage MOSFET device during its operation. The HiSIM_HV model has been submitted and is evaluated by the Compact Modeling Council (CMC) as a candidate for standardization.

A.C.T. Aarts and A. Tajic are presenting the MOS Model 20 (MM20), which is an advanced public-domain compact LDMOS model used for circuit simulation of high-voltage IC-designs. The MM20 model combines the MOSFET channel region under the thin gate oxide with the drift region of an LDMOS device preserving the effect of the gate extending over the drift region as well as quasi-saturation intrinsic model description. To maintain the model accuracy MM20 has been developed using a surface potential formulations and the internal device potentials are solved numerically inside the model core. This allows the MM20 to serve as the basis building block for all kind of LDMOS devices, for a wide range of supply-voltages. It is important to mention that the MM20 source code as well as the complete documentation including the parameter extraction strategy of the MM20 is available in the public domain.

Y.S. Chauhan et al. are introducing a modeling strategy for HVMOS transistors (HV-EKV) based on the scalable drift resistance and the use of charge based EKV2.6 MOSFET model as the core for the intrinsic MOS channel. The model is stable and robust in the entire bias range useful for circuit design purpose. Used modeling strategy is optimized according to the fast convergence and good accuracy criteria. It should be noted that the general HV-EKV model has scalable physical and electrical parameters allowing correct modeling of quasi-saturation and self-heating effect. The model is validated on the measured characteristics of two widely used industrial high voltage devices' types (LDMOS and VDMOS) and implemented into number of the commercial circuit simulators supporting the Verilog-A standard.

A. Napieralski et al. analyze problems encountered in the compact modeling of the unipolar high power semiconductor devices. After a short introduction to traditional and novel concepts of power device modeling and simulation, the authors discuss a new distributed model of power diode which can be directly integrated into a standard SPICE-based simulation tools. Main analyzed power devices parameters are: voltage blocking capability, or breakdown voltage, current capability and switching performance. Available power MOSFET macromodels and presented approach can facilitate the design process of power electronic circuits by adding distributed models for the IGBT and BJT devices also for the SiC technologies at the later stage of the developments.

P. Austin and J.-L. Sanchez present the physical basis of the new insulated-gate bipolar transistor (IGBT) modeling approach and its implementation. The authors describe the IGBT device and its original modeling method. Presented concept relies on a specific solution to the ambipolar diffusion equation which allows describing the distributed nature of the carrier dynamics occurring in the base region of the IGBT device. These models use physical, geometrical and electrical characteristics derived principally from the methods relying on reverse engineering or electrical measures. To highlight the results, two examples of application are given. The first one deals with the DC/AC voltage inverter while the second addresses the low loss architecture issue.

The final chapter by A. Napieralski et al. introduces the DMCS-SPICE web based tool which gives access to a SPICE-based simulation engine where a new distributed model of the PIN power diode has been implemented. Available model yields both accurate description of power PIN diode and relatively short simulation times, thanks to its distributed nature The DMCS-SPICE is a first step towards a widely accessible simulation environment with high power semiconductor device support, allowing the user to perform reliable simulation of a complete circuit in a reasonable time. That modular web based tool has three features that can make the project successful: it is free, it is widely accessible, and it is based on the well-known SPICE core.

From this summary of the compact modeling book contents, the reader can see that a broad overview of the compact modeling techniques in the power/HVMOS arena is described by selected group of leading authorities in their domain of expertise. It is a unique collection of the contributions regarding the best compact modeling practice which are complemented with equally good work regarding advanced TCAD and CAD simulation techniques as well as electrical characterization of the power/HVMOS semiconductor devices. In addition, a number of selected topics on silicon and alternative semiconductor high voltage possessing as well as introduction of the Verilog-A, hardware behavioral description language, as a compact modeling standardization platform further increases the usefulness of our book.

This book is also an indirect result of ongoing efforts of the MOS-AK Compact Modeling Group which allowed bringing together such a notable group of the authors. The MOS-AK Group is celebration the 20 years of enabling compact modeling R&D exchange in Europe this year. With initiative of one of the book editors, W. Grabinski, the MOS-AK Group and the Global Semiconductor Alliance (GSA) created the alliance as the next step in addressing the complex issues of

the entire compact modeling ecosystem. The MOS-AK/GSA initiative will come to fruition by encouraging interaction and sharing all information related to compact modeling at all levels of the device and circuit characterization, modeling and simulations; conducting regular meetings with industry players and academia to exchange information on the strengths and weaknesses of the industrialization of compact models; and providing comprehensive reports and reference papers as well as further modeling books to accelerate the transfer of advanced compact modeling methodologies and its standardization to the semiconductor industry.

The editors would like to deeply acknowledge all authors for their valuable contributions as well as the publishing team, in particular, Cindy Zitter, Springer SBM NL, for smooth management of our modeling book project.

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Wladek Grabinski
Thomas Gneiting

Chapter 1
Numerical Power/HV Device Modeling

Oliver Triebl and Tibor Grasser

Abstract Modern semiconductor devices have to fulfill many requirements in terms of performance, reliability, and costs. The structures have become very complex and have undergone major optimizations compared to the original proposals half a century ago. This complexity almost always requires Computer Aided Design (CAD) tools for the design of electric and electronic units. Usually different engineering levels have to be considered in the design process. At the circuit level CAD tools like SPICE can be used to adjust and test electronic circuits. Analysis of a device itself can be considered one step down on the engineering hierarchy levels. Dopant and carrier distributions become important and the spatial distribution of quantities has to be considered. Software tools supporting the design of devices at this level are known as Technology Computer Aided Design (TCAD) tools. This chapter will give an introduction in the drift-diffusion method which is probably the most important carrier transport model used in TCAD. Modeling of mobility and of generation and recombination will also be considered. Finally, a discussion on numerical considerations on solving the problems will be given.

Keywords Tcad · Device simulation · High-voltage · Drift-diffusion · Mobility modeling

1 Introduction

Modern semiconductor devices have to fulfill many requirements in terms of performance, reliability, and costs. Structures have become very complex and have undergone major optimizations compared to the semiconductor structures originally proposed half a century ago. This complexity almost always requires Computer

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Aided Design (CAD) tools for the design of electric and electronic units. Different engineering levels are considered in the design process. At the circuit level CAD tools like SPICE can be used to adjust and test electronic circuits. Here, the single devices are commonly simulated using calibrated compact models. Analysis of the device itself can be considered one step down on the engineering hierarchy levels. Dopant and carrier distributions become important and the spatial distribution of quantities has to be considered. Software tools supporting the design of devices at this level are known as Technology Computer Aided Design (TCAD) tools.

This chapter gives an introduction on how TCAD tools for device simulation work and how they can be used. The basic equations needed to perform drift–diffusion simulations are presented together with some mobility and generation/recombination estimations. Sample simulations show the influence of crucial physical models and demonstrate how TCAD gives the device engineer an insight into the device behavior and how that information can be used for further device optimization. Some considerations on solving the equation systems by applying discretization schemes and using iterative solution techniques will be given.

As the focus of this introductive chapter is on the modeling and simulation of high-voltage devices, the validity of drift–diffusion framework will be assumed. These drift–diffusion equations are also the starting point for the derivation of most compact models. More advanced and computationally demanding transport models such as energy-transport, six moment models, and Monte Carlo simulation have gained some interest during the last decade and are briefly summarized.

1.1 TCAD – Technology Computer Aided Design

Tools used to simulate semiconductor manufacturing processes and semiconductor device behavior belong to the group of TCAD tools. These tools aim to reproduce and especially predict the physical mechanisms and to determine the resulting device structure and device behavior. For this, models describing the best physical phenomena are required. Proper models have to be found and have to be included in the simulation tools resulting in differential equation systems. Since the resulting mathematical problem generally cannot be solved explicitly, numerical techniques are applied. Solutions can be found using statistical methods, the Monte Carlo method for example, or iterative techniques. For efficient computation in engineering environments, most often simplified models have to be used.

1.2 Benefits of Numerical Modeling

In numerical device simulation the structure of a device is represented using distributed quantities. With distributed we mean that in the most general case important quantities such as the electrostatic potential ψ and the carrier concentrations n and

p are calculated in the three-dimensional space $r = (x, y, z)$. Since the physical processes in the semiconductor device are modeled as realistically as possible, the device behavior directly results from the simulation. This is fundamentally different compared to compact modeling. There, every type of device requires its own compact model, whereas in device simulation proper modeling of semiconductor physics delivers results for all types of devices. This implies that the geometry and the doping profile of the real device are considered implicitly in the simulation as accurately as required. On the other hand, one has to consider that the use of any of the physically based approaches addressed in this chapter requires a considerable computational effort compared to compact modeling. For an LDMOS structure, for example, it might be required to calculate quantities on 10,000 or even more mesh points. Application of the drift–diffusion model with three unknown quantities for each point results for a two-dimensional problem in an equation system with more than 30,000 unknowns which has to be solved for every step in the iterative solution process.

Nevertheless, numerical device simulation gives the device engineer the possibility to understand and analyze the inner life of the device which is completely hidden in compact modeling. The insight helps to find possible failure mechanisms. Failures in real world devices can be reproduced in the simulation and solutions can be derived and tested. This gives the possibility to reduce the number of test devices that have to be fabricated to a minimum.

TCAD tools also allow to estimate the performance of completely new structures which is especially helpful to predict any parasitic effects in integrated circuits. Possible failures due to parasitic transistors can be discovered by analyzing two or more neighboring devices together in a single simulation. This has also become important for high-voltage and power devices, since integration with other technologies as is used in so called SMART power devices, has become popular and introduces many potential failures. Reliability demands and lifetime predictions are also important for many applications. The analysis of aging and degradation can be supported using numerical modeling approaches.

1.3 Sample Device

For all simulations performed in this chapter the device simulation tool MINIMOS-NT [1] has been used. The sample device used is based on a high-voltage sample device fabricated by austriamicrosystems [2]. It is an n-channel lateral DMOSFET with a gate oxide thickness of 7 nm, fabricated in a 0.35 μm CMOS-based technology. The gate length is 0.5 μm, the width is 40 μm, and the specified application voltage is 50 V. The doping profile and the geometry depicted in Fig. 1.1 were simulated using the Synopsys process simulation tools. The domain used for simulation has a depth of 15 μm, while most figures depict only the upper 3.5 μm of the device.

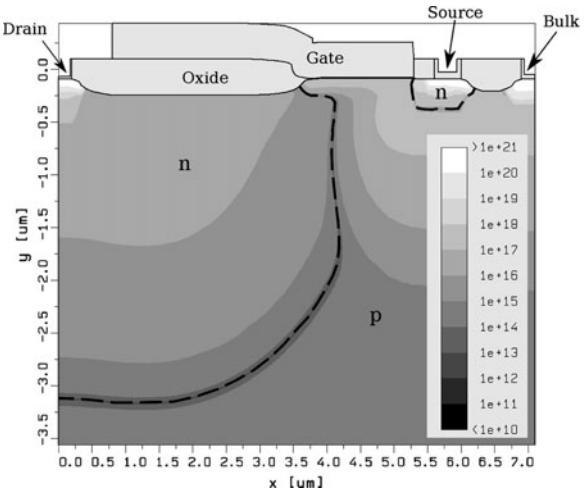

Fig. 1.1 Structure of the sample n-channel LDMOSFET used for simulations in this chapter. The transitions between n- and p-doped regions are marked with dashed lines and the absolute value of the net doping concentration is shown in $1/\mathrm{cm}^3$. The simulated structure of the device continues into a depth of 15 μm, while only the upper part is depicted

2 Device Modeling

TCAD simulations require appropriate physical and mathematical models describing the device behavior in a self consistent way. The fundamental equations needed to model semiconductor device structures are the Poisson equation, the continuity, and transport equations, which in their simplest form have become known as the drift–diffusion model [3]. In the following sections, models for different physical properties relevant to high-voltage devices are presented. The high fields particularly influence the mobility within the device leading to high differences of the mobility in the drift and the channel region. These mobility variations strongly depend on the operating point. The peaks of the electric field require the consideration of impact ionization, whereas Shockley–Read–Hall generation and recombination dominates the currents in space charge regions for lower fields. Due to the thick oxides used in high-voltage devices quantum-mechanical tunneling currents are normally of minor importance. Also, consideration of quantum confinement is usually not required for the relatively thick oxides used in these devices. Thermal modeling definitely plays an important role. Since changes of the device temperature due to power dissipation have a strong impact on nearly all device properties.

2.1 Semiconductor Equations

In macroscopic semiconductor device modeling, Poisson's equation and the continuity equations play a fundamental role. Poisson's equation, one of the basic

equations in electrostatics, is derived from the Maxwell equation $\nabla \cdot \mathbf{D} = \rho$ and the material relation $\mathbf{D} = \hat{\epsilon}\mathbf{E}$. Using the electrostatic potential ψ with $\mathbf{E} = -\nabla\psi$, Poisson's equation reads

$$\nabla \cdot (\hat{\epsilon}\nabla\psi) = -\rho. \tag{1.1}$$

Since even for high frequencies the wavelength is typically much smaller than the device dimension, the quasi stationary approximation used to derive Poisson's equation are justified. In semiconductors the charge density ρ is commonly split into fixed charges which are in particular ionized acceptors N_{A}^{-} and donors N_{D}^{+} and into free charges which are electrons n and holes p. The permittivity tensor $\hat{\epsilon}$ is considered time invariant in the derivation of Poisson's equation. In isotropic materials like silicon the permittivity can be additionally approximated by the scalar value ϵ. Furthermore the permittivity is often considered to be constant within a material segment, therefore Poisson's equation used in device simulation tools looks like

$$\nabla^2\psi = -\frac{\mathrm{q}}{\epsilon}(n - p + N_{\mathrm{A}}^{-} - N_{\mathrm{D}}^{+}). \tag{1.2}$$

The second important equation, the continuity equation, can also be derived from Maxwell's equations and reads

$$\nabla \cdot \mathbf{J} + \frac{\partial\rho}{\partial t} = 0. \tag{1.3}$$

The current density $\mathbf{J}$ is split into $\mathbf{J}_n$ and $\mathbf{J}_p$, for the contributing carrier types n and p, respectively. By introducing the recombination rate R, two separate continuity equations, one for each carrier type, can be written as

$$\nabla \cdot \mathbf{J}_n - \mathrm{q}\frac{\partial n}{\partial t} = +\mathrm{q}R \qquad \text{and} \tag{1.4}$$

$$\nabla \cdot \mathbf{J}_p + \mathrm{q}\frac{\partial p}{\partial t} = -\mathrm{q}R. \tag{1.5}$$

Alternatively, Eqs. 1.4 and 1.5 can be derived from the Boltzmann transport equation using the method of moments [4]. The separation into two equations allows independent transport modeling of the carrier types. Generation and recombination rates of electrons and holes are expressed using physically or empirically based recombination models [3], some of which are described in Section 2.3. The rate R represents the net rate only, which is zero in thermal equilibrium where generation and recombination are balanced.

2.2 Carrier Transport Equations

A semiclassical description of carrier transport is given by Boltzmann's transport equation (BTE) which describes the evolution of the distribution function in the six-

dimensional phase space (x, y, z, p_x, p_y, p_z). Unfortunately, analytical solutions exist only for very simple configurations. One popular approach for solving the BTE is the Monte Carlo method [5] which is highly accurate but also very time consuming.

Simulation on an engineering level requires simpler transport equations which can be solved for complex structures within reasonable time. One method to perform this simplification is to consider only moments of the distribution function [6]. Depending on the number of moments considered for the model, different transport equations can be evaluated. Use of the first two moments results in the drift–diffusion model, a widely applied approach for modeling carrier transport.

2.2.1 The Drift–Diffusion Model

The drift–diffusion current equation can be derived from the BTE using the method of moments [3] or, alternatively, from the basic principles of irreversible thermodynamics [7]. The resulting electron and hole current relations contain at least two components caused by carrier drift and carrier diffusion. Inclusion of the driving force caused by the lattice temperature gradient (∇T_L) [8] leads to

$$\mathbf{J}_n = \mathrm{q} n \mu_n \mathbf{E} + \mathrm{q} D_n \nabla n + \mathrm{q} n D_n^T \nabla T_\mathrm{L} \tag{1.6}$$

$$\mathbf{J}_p = \mathrm{q} p \mu_p \mathbf{E} - \mathrm{q} D_p \nabla p - \mathrm{q} p D_p^T \nabla T_\mathrm{L}. \tag{1.7}$$

μ_ν (ν stands for n and p) represents the carrier mobility, D_ν^T the thermal diffusion coefficients, and D_ν the diffusivity which is often expressed via the mobility invoking the Einstein relation

$$D_\nu = \mu_\nu \frac{\mathrm{k_B} T_\mathrm{L}}{\mathrm{q}}, \tag{1.8}$$

where $\mathrm{k_B}$ is the Boltzmann constant. The Einstein relation is strictly valid only in equilibrium [9].

The Eqs. 1.6 and 1.7 together with (1.4), (1.5), and (1.2) form the drift–diffusion model which was first presented by Van Roosbroeck in [10]. Rigorous derivations from the BTE show that many simplifications are required to obtain the drift–diffusion equations as shown. Simplifications are, for example, the single parabolic band structure or the cold Maxwellian carrier distribution function which assumes the carrier temperature equal to the lattice temperature. Nevertheless, due to its simplicity and excellent numerical properties, the drift–diffusion equations have become the workhorse for most TCAD applications. It also forms the basis for the bulk of compact models.

The following example illustrates that the drift–diffusion model as presented above can be directly applied to semiconductor devices. In this first approach the example LDMOSFET in Fig. 1.1 was simulated, where the recombination rate R was neglected and the mobility assumed to be constant. Note that these are standard

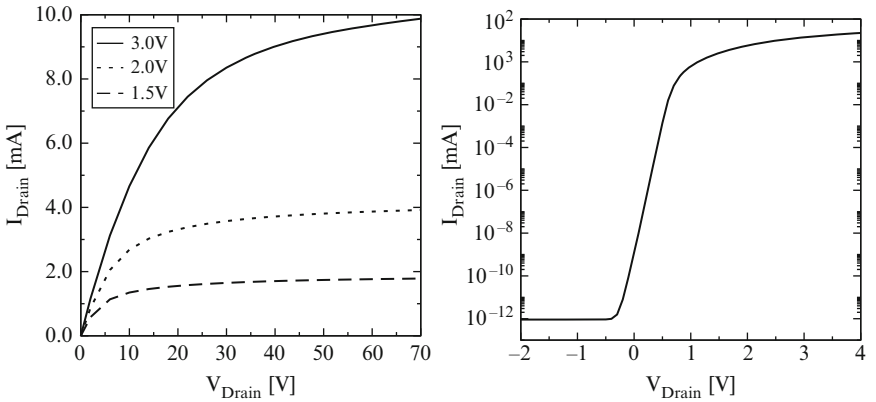

Fig. 1.2 Simulation of output (*left*) and transfer (*right*) characteristic of the sample device using the drift–diffusion model only. Generation and recombination were neglected and the mobility was assumed to be constant

assumptions for the derivation of compact models. This basic simulation gives the output characteristics shown in Fig. 1.2, no other models are required. Despite these simplifications, the basic characteristic of MOSFET devices can already be seen. However, neglecting all generation and recombination effects and assuming a constant mobility is a strong oversimplification resulting in quantitative and qualitative errors. However, the spatial variation of the mobility can be easily included in TCAD simulations since the mobility and other distributed parameters can be evaluated individually for every position within the device. The device geometry and the doping profiles are therefore considered implicitly and directly influence the device behavior.

2.2.2 Higher-Order Transport Models

To obtain a better approximation of the BTE, higher-order transport models can be derived using the method of moments, for example. The most prominent models beside the drift–diffusion model are the energy-transport/hydrodynamic models which use three or four moments. These models are based on the work of Stratton [11] and Bløtekjær [12], a detailed review is given in [4]. In addition to the quantities used in the drift–diffusion model, the energy flux and the carrier temperatures with corresponding equations are introduced, which require additional transport parameters. Modeling of carrier mobility and impact-ionization benefits from more accurate models based on the carrier temperatures rather than the electric field. This advantage is caused by the non-local behavior of the average energy with respect to the electric field and becomes especially relevant for small device structures (Fig. 1.3 left). However, it shows that describing the energy distribution function using only the carrier concentration and the average carrier temperature is still not sufficient for specific problems depending on high energy tails (Fig. 1.3 right). Hot carrier mod-

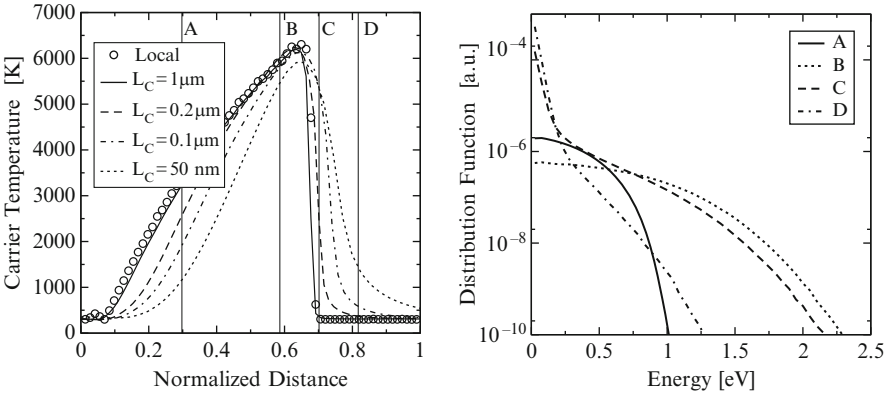

Fig. 1.3 Electron temperature (*left*) and distribution functions (*right*) of comparable $n^+ - n - n^+$ structures with varying channel lengths L_C. The spatial coordinates have been normalized to get an overlapping electric field. It can be seen that the local electric field approach is sufficient for larger structures but gives poor results for small structures. The distribution functions on the right are shown for $L_C = 200\,\text{nm}$ at the positions A to D. Note that the average energies at the points A and C are the same, whereas the distribution function looks completely different. Also note the high-energy tail at point D where the carrier temperature is already close to the lattice temperature with a value of 370 K [13]

eling in small structures, for example, which is based on accurate modeling of the high-energy part of the distribution function would require more complex models. The six moments method [14] is one possibility to improve the approximation of the distribution function.

Due to their better approximation of the BTE, higher-order transport models often give better results than the drift–diffusion model [15]. This effect is especially relevant for small structures where non-local effects gain importance (Fig. 1.3). However, since high-voltage device structures are relatively large, the drift–diffusion model is usually sufficient. The drawbacks of using more complex transport equations are the higher computation time and the increase of numerical instabilities and convergence issues. This issue is even more relevant for a high number of mesh points which are necessary for large devices. If required, different transport equations can be used within one device. This allows to model critical areas using higher-order transport models whereas the drift–diffusion model is used for the rest of the device. Areas of interest might be the channel area of an MOS device or areas having spatially strongly varying electric fields.

2.3 Parameter Modeling

The semiconductor equations discussed in the former section show the basic relations between carrier distribution and the electrostatic potential. Two parameters,

the mobility and the recombination rate were introduced, which require appropriate modeling. The physical phenomena influencing these parameters are manifold and will be discussed in the following.

2.3.1 Mobility

The derivation of the mobility originates from carrier relaxation times. The mobility is influenced by the lattice and its thermal vibrations, impurity atoms, surfaces and interfaces to neighboring materials, the carriers themselves, the energy of the carriers, and other effects like lattice defects. Mobility models are used to make an estimation considering these effects and make simulations in continuous systems possible. Since exact derivations are too complex or just do not exist, empirical approaches are often used. Some of the commonly used approaches will be discussed here.

A common method for modeling the mobility is the hierarchically encapsulation of the physical mechanisms. In this approach, the most fundamental mechanism is considered to be the lattice scattering dependence (μ^{L}) followed by the ionized impurity dependence (μ^{I}). Especially in MOS devices, a surface correction (μ^{S}) is of special importance. These three contributions classify the low-field mobility models. Modeling of high-field effects is introduced with a field dependence model (μ^{F}). These contributions may be combined as it is for example done in the MINIMOS mobility model [16] which looks like

$$\mu^{\mathrm{LISF}} = \mu^{\mathrm{LISF}}\left(\mu^{\mathrm{LIS}}\left(\mu^{\mathrm{LI}}\left(\mu^{\mathrm{L}}\right)\right)\right). \tag{1.9}$$

The individual mechanisms are assumed to be independent of each other. All values resulting from mobility calculations are obviously different for electrons and holes. To demonstrate the impact of lattice, impurity, and surface scattering on the mobility, the electron mobility distribution in the sample device is shown in Fig. 1.4.

In contrast to the encapsulation approach (1.9) for the mobility calculation used in the MINIMOS model, the Lombardi model [17] combines three carrier mobility components using Matthiessen's rule. The components are derived from surface acoustic phonon scattering, from bulk carrier mobility, and from surface-roughness scattering. A similar expression has been used by Agostinelli [18] for holes, additionally accounting for interface charge and screened Coulomb scattering (1.10).

$$\frac{1}{\mu_\nu^{\mathrm{LIS}}} = \frac{1}{\mu_\nu^{\mathrm{ph}}} + \frac{1}{\mu_\nu^{\mathrm{sr}}} + \frac{1}{\mu_\nu^{\mathrm{c}}} \tag{1.10}$$

Here, the phonon scattering component μ_ν^{ph} combines scattering with bulk phonons, surface phonons, and fixed interface charges. μ_ν^{sr} includes the dependence of the surface-roughness scattering on the electric field orthogonal to the interface and μ_ν^{c} models the screened Coulomb scattering. Modeling the influence of interface charges is of special interest in reliability modeling. Effects like negative bias temperature instability [19] or hot carrier degradation [20] generate interface

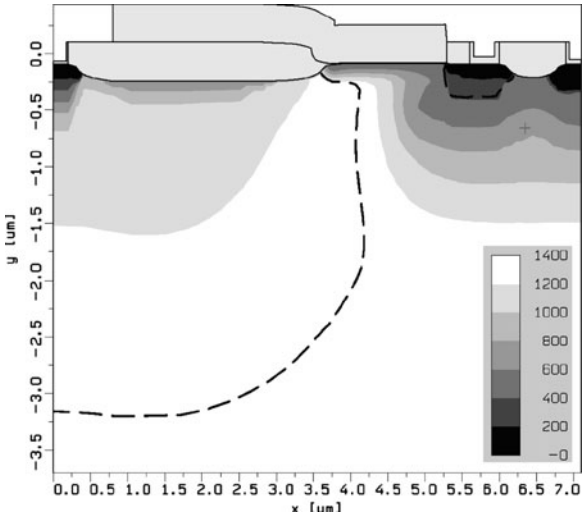

Fig. 1.4 Electron mobility distribution (in $\mathrm{cm}^2/\mathrm{Vs}$) in the sample device taking into account the lattice, impurity, and surface scattering models

traps leading to interface charges. The prediction of this device degradation is of crucial interest for semiconductor manufactures. Other mobility models based on Matthiessen's rule have been developed, for example, by Darwish [21] or Neinhüs [22], the latter additionally includes quantum confinement influences on the mobility.

A universal dependence of the effective minority carrier mobility in inversion channels on the effective vertical field ($E_{\perp,\mathrm{eff}}$) has been shown in [23]. The effective vertical field in the inversion layer is modeled using the bulk (depletion) Q'_{B} and mobile (inversion) Q'_{I} charge layer densities,

$$E_{\perp,\mathrm{eff}} = \frac{1}{\epsilon}\left(Q'_{\mathrm{B}} + \frac{1}{2}Q'_{\mathrm{I}}\right), \tag{1.11}$$

and the effective mobility can be approximated using the empirical fit [24]

$$\mu_{\mathrm{eff}}(E_{\perp,\mathrm{eff}}) = \mu_{\mathrm{max}}\left(\frac{E_{\mathrm{C}}}{E_{\perp,\mathrm{eff}}}\right)^{C_1}. \tag{1.12}$$

In this model, fixed oxide charges and the channel doping are used to model the maximum effective mobility μ_{max} as well as the quantities E_{C} and C_1. This concept has been used among others by Huang [25], to derive a mobility model. Here, the surface-roughness and phonon scattering mobility contributions are modeled using the effective field (1.11). For the calculation of the mobility, the charges Q'_{B} and Q'_{I} have to be extracted. This cannot be included into the TCAD concept straight forwardly, since for the calculation of Q'_{B} and Q'_{I}, integration of the charge along the normal direction to the interface is necessary. The estimated minority carrier

mobility is the same along this cut. Apart from the necessity of an additional preprocessing step to extract the charges, the ability of estimating the mobility for every location independently is lost. This approach also results in numerical difficulties since the integration introduces a lot of dependencies in the equation system, which leads to a poor solver performance. Approaches based on the effective vertical field are therefore used rather for compact modeling than for device simulation.

Up to this point, the discussion on mobility did not consider the electric field in the direction of the current flow and are therefore also called low-field mobility models. However, the carrier mobility strongly depends on the distribution function. Since the distribution function used in the transport models is strongly simplified and the detailed shape is not available, models have to be based on other quantities. In the case of the drift–diffusion model the electric field is commonly used and models are therefore called high-field mobility models. Simulation tools often differ between low- and high-field mobility and let the user select the models independently. Modeling of the high-field mobility dependence is often accomplished using the approach presented by Caughey and Thomas [26]. A slightly different version, suggested by Jaggi [27,28], is used in the MINIMOS model:

$$\mu_\nu^{\mathrm{LISF}} = \frac{2\mu_\mu^{\mathrm{LIS}}}{1+\left(1+\left(\dfrac{2\mu_\mu^{\mathrm{LIS}}|\mathbf{F}_\nu|}{v_\nu^{\mathrm{sat}}}\right)^{\beta_\nu}\right)^{1/\beta_\nu}}. \tag{1.13}$$

$\mathbf{F}_\nu$ describes the driving force, which is the gradient of the quasi-Fermi level, v_ν^{sat} is the saturation velocity, and the coefficient β_ν is 1 for holes and 2 for electrons. The impact of this field dependence can be seen in the mobility distribution of the sample device shown in Fig. 1.5.

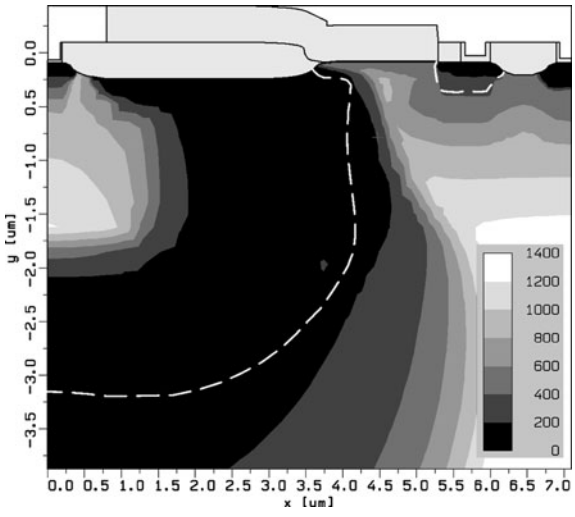

Fig. 1.5 Electron mobility distribution (in $\mathrm{cm}^2/\mathrm{Vs}$) in the sample device considering additionally to the lattice, impurity, and surface scattering models a field dependence model

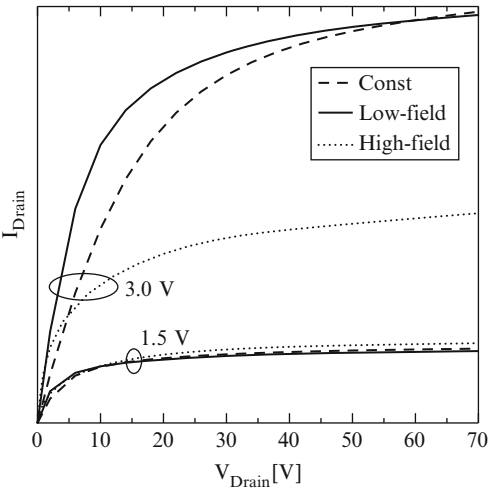

Fig. 1.6 Output characteristic of the sample device for different gate voltages using a constant mobility, a low-field mobility, and a high-field mobility model (1.13). For visualization the curves were scaled along the current axis so that the output for the gate voltage of 1.5 V overlaps

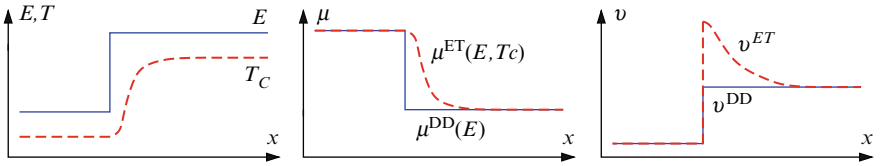

Fig. 1.7 Carriers traversing an abruptly changing electric field do not gain the resulting energy immediately and the carrier temperature therefore increases with a delay (*left*). High-field mobility models for drift–diffusion are based on the electric field and therefore react instantly to changes of the electric field while models based on the carrier temperature capture that delay (*center*). As a consequence the velocity overshoot ($v = \mu E$) cannot be observed in drift–diffusion (*right*)

To illustrate the impact of the high-field mobility a comparison of simulation results with and without active high-field mobility are shown in Fig. 1.6. Qualitative and quantitative differences can be seen. Both the constant mobility and the low-field mobility model only depend on fixed quantities so that the mobility does not change with the operating point which results in a similar transconductance. The fact that the low-field dependent model shown has spacial varying mobility values leads to the change of the shape of the output characteristic compared to the constant mobility model. The high-field mobility model leads to a considerable reduction of the mobility with increasing fields and therefore to a substantial reduction of the output current for increasing gate voltages.

Carrier mobility modeling has been investigated since the beginning of semiconductor engineering and there are still new models published. However, all models in drift–diffusion incorporating the influence of carriers that are not in thermal equilibrium basically rely on the electric field. Changes in the electric field therefore directly change the calculated mobility (see Fig. 1.7), whereas the carrier temperature does not increase immediately. Mobility models in energy-transport which

are based on the carrier temperature capture this effect. As a consequence velocity overshoot can be observed. In larger device structures, such as the high-voltage devices discussed here, this effect is normally unimportant and can be neglected.

2.3.2 Carrier Generation and Recombination

The recombination rate R was formally introduced in the drift–diffusion equations by splitting the continuity equation into two individual equations for electrons and holes. From a physical point of view this term includes the generation and the recombination of electron-hole pairs. In thermal equilibrium carrier generation and recombination are balanced and the carrier concentrations are given by their equilibrium values n_0 and p_0 ($n_0 p_0 = n_i^2$). The net recombination rate therefore vanishes. An excess number of carriers leads to an increased recombination, a low carrier concentration leads to an increased generation. The generation and recombination processes contributing to the total effective net generation rate are based on different physical effects which are modeled independently. Each model is evaluated separately and the total net recombination rate is calculated by adding the individual rates. The resulting rate is used to complete the continuity equations (1.4) and (1.5).

One important generation/recombination process is the well-known Shockley–Read–Hall (SRH) mechanism [29,30] which describes a two-step phonon transition. One trap level which is energetically located within the band-gap is utilized. There are four partial processes considered: the capture and the emission of both, electrons and holes, on the trap level. Balance equations can be formulated for the trap occupancy function. In the stationary case the rates for electrons and holes are equal. The trap occupancy function can be eliminated and the SRH generation rate can be calculated using

$$R^{\mathrm{SRH}} = \frac{np - n_i^2}{\tau_p \left(n + n_1\right) + \tau_p \left(p + p_1\right)}. \tag{1.14}$$

n_1 and p_1 are auxiliary concentrations depending on the energy level of the traps, τ_n and τ_p are carrier lifetimes for electrons and holes.

In MOS devices SRH generation especially influences the bulk current. In an n-channel device, for example, holes generated at the pn-junction are attracted by the low bulk potential which leads to an increased bulk current. This can be easily observed in device simulation since models can be switched on or off allowing to deactivate SRH. Figure 1.8 shows the hole current flow and the SRH generation rate in the sample device and in Fig. 1.9 the current components on the bulk contact are compared with and without SRH enabled.

The SRH model is not restricted to the description of capture and emission of carriers in the bulk, it can also be extended to determine the occupancy of interface traps [31]. Modeling of interface states is especially important for reliability modeling in MOS devices. Simulations of charge pumping measurements [32], for example, which are used to determine interface trap distributions, require appropriate modeling of trapping and de-trapping effects of carriers in interface traps. A simulation replicates the measurement procedure, by performing a transient

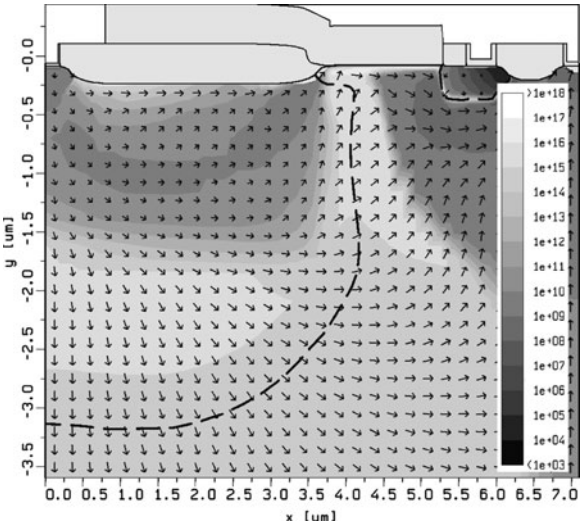

Fig. 1.8 SRH generation rate (in $s^{-1}\,cm^{-3}$) in the sample device with a drain voltage of 50 V and a gate voltage of 2 V. The *arrows* show the hole current flow

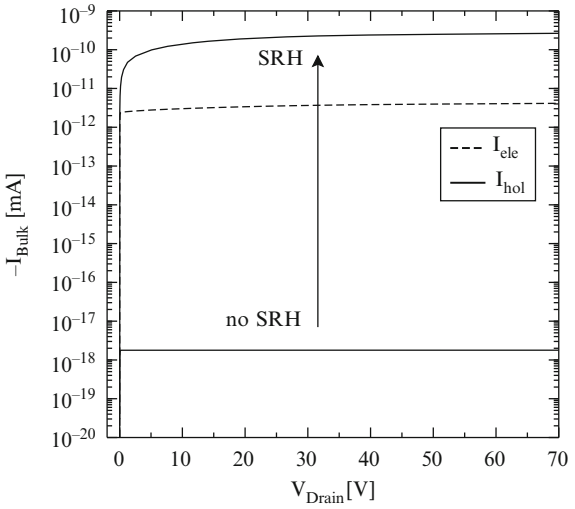

Fig. 1.9 Bulk current for the sample device using a gate voltage of 2 V with and without the SRH model activated. While the electron current stays the same, the hole current increases due to the SRH generated holes in the space charge region

simulation for every gate pulse level (Fig. 1.10). In contrast to the stationary SRH formulation shown in (1.14), time dependent simulations require to capture the transient behavior of the occupancy function [33]. The charge pumping curve can be constructed by extracting the mean current of the simulations for every single gate pulse (Fig. 1.11).

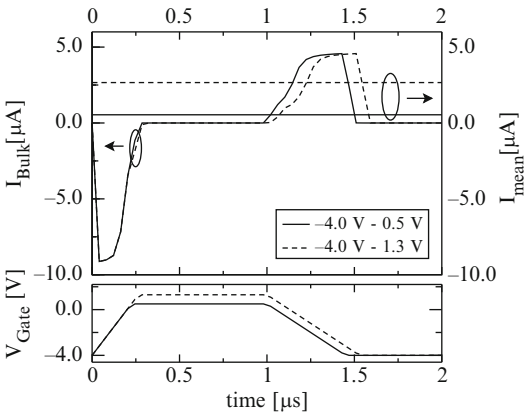

Fig. 1.10 Bulk current during two different gate voltage pulses. The mean currents are the charge pumping currents which are transferred to the charge pumping curve in Fig. 1.11

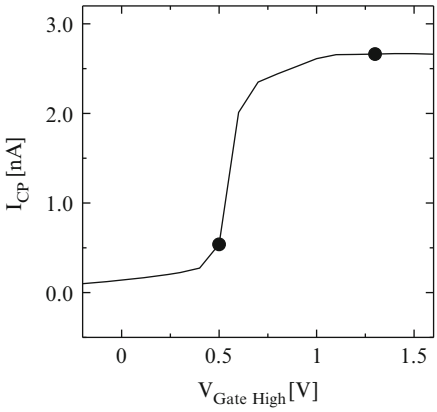

Fig. 1.11 Charge pumping curve of the sample device using gate pulses with constant low level of −4 V and changing high level. Values taken from Fig. 1.10 are highlighted

Beside the two-particle SRH mechanism there are two important three-particle generation/recombination mechanisms to mention: the Auger and the impact-ionization process, whereas the latter is a pure generation process. There, the energy required for generation is delivered by a third high-energetic electron or hole. The excess energy available after a recombination process is transferred to a third electron or hole. Modeling of this process can be achieved by defining rates for each partial process. Assuming a stationary case the rate evaluates to [3]

$$R^{\mathrm{AUG}} = \left(nC_n^{\mathrm{AUG}} + pC_p^{\mathrm{AUG}}\right)\left(np - n_i^2\right). \tag{1.15}$$

The coefficients C_n^{AUG} and C_p^{AUG} have only a weak dependence on the temperature [34] and are therefore often assumed to be constant, however, also temperature dependent models have been suggested [35].

The second three-particle mechanism mentioned, the impact-ionization carrier generation, describes electrons or holes which gain high energy from the electric field when traveling through the semiconductor. A scattering event between such

a high-energetic carrier and an electron or hole in the valence or conduction band, respectively, creates a new electron-hole pair. Impact-ionization is a pure generation process. Since there is no information on the carrier energy in the drift–diffusion model, as a compromise modeling is usually based on the current densities and on ionization coefficients which depend on the electric field. Many different approaches to model the coefficients have been proposed. Most device simulation tools [1, 36] include variations of the proposal of Chynoweth [37]:

$$G^{\mathrm{II}} = -\alpha_n(\mathbf{E})\frac{|\mathbf{J}_n|}{\mathrm{q}} - \alpha_p(\mathbf{E})\frac{|\mathbf{J}_p|}{\mathrm{q}} \tag{1.16}$$

A commonly used formulation applies as parameter the electric field in the direction of the current flow (1.17).

$$\alpha_\nu(\mathbf{E}, \mathbf{J}_\nu) = \alpha_\nu^\infty \exp\left(-\left(\frac{E_\nu^{\mathrm{crit}}\,|\mathbf{J}_\nu|}{\mathbf{E}\cdot\mathbf{J}_\nu}\right)^{\beta_\nu}\right) \tag{1.17}$$

α_ν^∞ is the temperature dependent maximum generation rate for high-fields. TCAD simulations using this model help to locate areas with high generation rates, see Fig. 1.12, and show the impact on the output characteristics Fig. 1.13.

Lower impact ionization rates have been observed for surface near currents [38] and models have been developed describing the transition between surface and bulk impact ionization [39]. However, Monte Carlo simulations have shown that there are no or only minor differences between surface and bulk impact ionization [40].

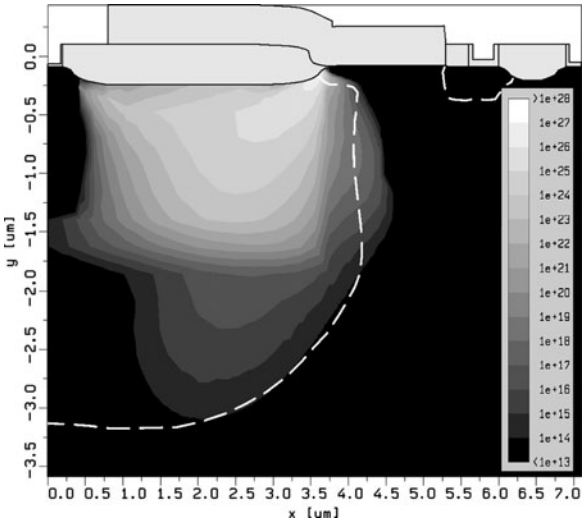

Fig. 1.12 Impact ionization generation rate in the sample device with a drain voltage of 40 V and a gate voltage of 2 V

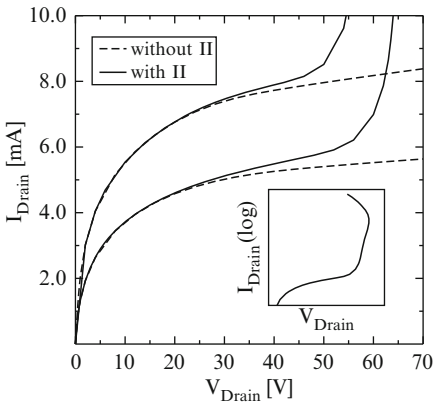

Fig. 1.13 Comparison of the output characteristic with and without impact-ionization. The inset shows a simulated snap-back curve

This means that there is no physical evidence of different rates near the surface and that these models are based on artifacts resulting from the approximate ionization rates based on the electric field.

Concerning the impact-ionization model presented, one has to note that carriers do not gain the energy from the electric field instantly. From a physical point of view the dependence of the impact-ionization rate on the local electric field is therefore not correct and only valid under homogenous conditions. A rigorous modeling should be based on the energy distribution function of the carriers, since only the high energetic carriers are relevant for impact-ionization [41]. Modeling of this high energy tail requires higher order transport models like the six moments model (see Fig. 1.3). Since the average carrier temperature which is available in the hydrodynamic model gives no information on the shape of the high energy tail, models based on this average temperature often overestimate the actual rate (compare Fig. 1.14). However, for larger structures the electric field based approximations give good results and can be used in the drift–diffusion model. As empirical alternatives to models based on the high energy tail, non-local impact-ionization models for the drift–diffusion model have been suggested [42].

Beside the generation and recombination mechanisms discussed here, many additional mechanisms are possible, which are more important for other device types. Some of the typical mechanisms considered in modeling include direct recombination which is important for direct bandgap semiconductors, direct [44] and trap assisted [45] band-to-band tunneling in high field regions, and optical generation [3].

2.4 Thermal Modeling

Physical properties of semiconductor devices strongly depend on the lattice temperature. Due to self-heating effects in the devices and due to changing ambient

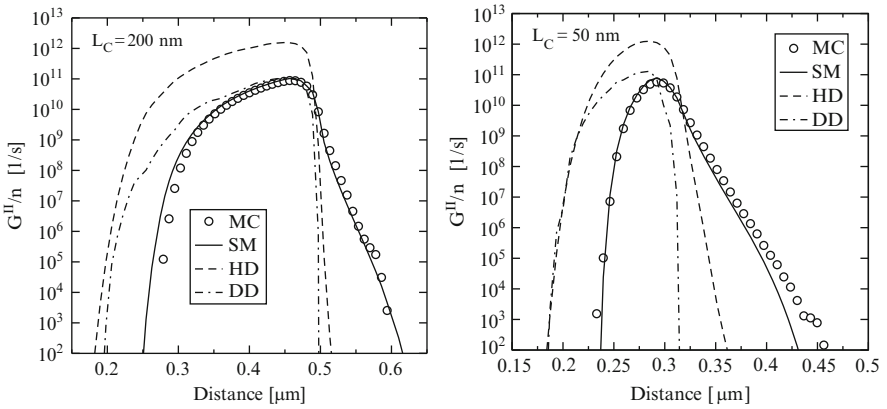

Fig. 1.14 Impact ionization rates in two comparable n^+-n-n^+ structures with a channel length of 200 nm (*left*) and 50 nm (*right*) [43]. The rates are calculated using the drift–diffusion (DD), hydrodynamic (HD), and six moments (SM) models. The Monte Carlo (MC) date serves as reference solution. Above 200 nm channel length the empirical drift–diffusion approximation fits reasonably well, whereas the hydrodynamic solution overestimates the generation rate. Only the six moments model is able to reproduce the impact-ionization rate in short channel devices

temperatures, the temperature distribution within a device is needed to estimate the device behavior at operating conditions. Modeling of the temperature requires some reference temperature, which might be a heat sink or the ambient temperature. The boundary condition for the temperature is commonly modeled with a thermal resistance to this fixed reference temperature. An important issue in thermal simulations is the size of the simulation domain. The heat flow in a semiconductor device extends to areas that are electrically less important and the simulation domain usually has to be extended compared to iso-thermal simulations.

The lattice temperature distribution T_L is modeled using the heat conduction equation [7]

$$c_\mathrm{tot}\frac{\partial T_\mathrm{L}}{\partial t} = \nabla\cdot(\kappa_\mathrm{tot}\nabla T_\mathrm{L}) + H, \tag{1.18}$$

where c_tot is the total heat capacity and κ_tot the total thermal conductivity. Both parameters include contributions from the lattice, the electron, and the hole subsystem. The temperature differences in the lattice lead to an additional driving force on the carriers which has to be considered in the current equations. For a non iso-thermal simulation, the last terms in (1.6) and (1.7) have to be considered in the solution of the drift–diffusion model.

Different approaches of modeling the heat generation rate H have been proposed. The most simple approach considers only the Joule heat $\mathbf{J}\cdot\mathbf{E}$ [46]. A more complex model according to Adler [47] describes the generated heat using

$$H = \mathbf{J}_n\cdot\nabla\frac{E_\mathrm{c}}{\mathrm{q}} + \mathbf{J}_p\cdot\nabla\frac{E_\mathrm{v}}{\mathrm{q}} + R\,(E_\mathrm{c}-E_\mathrm{v})\,. \tag{1.19}$$

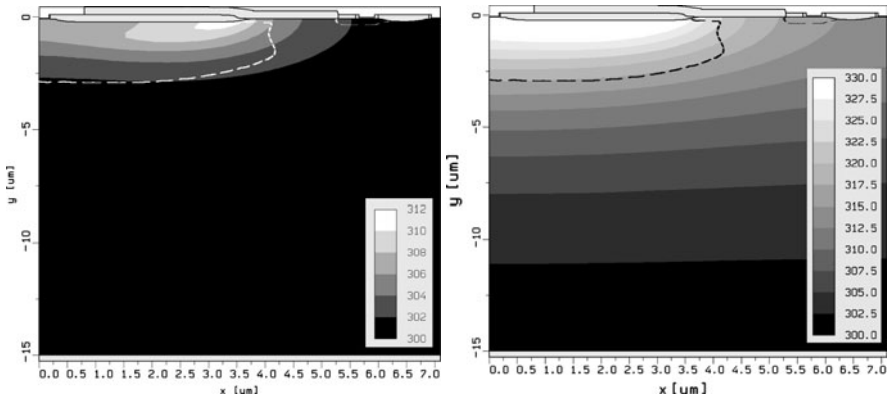

Fig. 1.15 Temperature distribution in Kelvin in the sample device with the gate biased to 2 V at the end of a linearly increase of the drain voltage from 0 to 50 V in 50 ns (*left*) and 500 ns (*right*)

Here, the energy dissipation due to recombination is considered. A more rigorous approach to thermal generation is given by Wachutka [7].

Transient simulations including thermal modeling were performed using the sample device. The lower bulk contact is linked with a thermal resistance to the ambient temperature of 300 K. In this simulation, the drain voltage is raised linearly from 0 to 50 V using two different slopes. The temperature distributions at the end of the two voltage ramps are depicted in Fig. 1.15. At the end of the 50 ns slope a rapid increase of the temperature near the birds beak can be observed.

2.5 Additional Physical Effects

In addition to the physical mechanisms addressed so far, there are obviously many other relevant modeling issues for semiconductor devices. For most of them, well established approaches are available in TCAD device simulation environments. Band-structure physics, for example, requires modeling for the bandgap energy and bandgap narrowing [48]. At low temperatures, incomplete ionization becomes important [49]. Also, semiconductor-metal contacts require appropriate treatment. The most common models for that include the well-known ohmic contact model where charge neutrality and equilibrium are assumed at the electrodes [3] and the Schottky contact models [50].

Especially in highly down-scaled MOS devices, tunneling and quantum effects have to be considered. For direct tunneling, which is most interesting for thin oxides, typically the Tsu–Esaki [51] or the Fowler–Nordheim [52] models are used. Herrmann and Schenk [53] proposed models for trap assisted tunneling, which has also been extended to multi-trap assisted tunneling models [54], especially interesting for highly degraded devices.

The inclusion of quantum confinement effects becomes especially important in SOI or double gate devices [55]. One modeling proposal is the modified local density approach [56] which is used in the model of Hänsch [57]. Here, a local correction of the effective density of states near the gate oxide is used to contribute to the quantum effects. An empirical correction approach has been presented by Van Dort et al. [58] which models the quantum confinement by increasing the band-gap near the interface.

3 Numerical Issues

In TCAD environments, the physical properties of a semiconductor device are described using models based on differential equation systems. Generally, the problems cannot be solved explicitly and numerical solution techniques are required. The system is solved at discrete points in space which are represented in terms of a mesh. The differential equations are then approximated using difference equations which can be solved using iterative solution techniques, typically based on the Newton method. Solving the transport equations together with the equations of the models for the mobility and for generation/recombination in a self-consistent way is a very complex task and requires considerable computational power. Since also the accuracy of the solution has to be considered, a proper trade off between accuracy, solvability, and simulation time has to be found.

3.1 Meshing

The points in space on which solutions for quantities are calculated are represented using a mesh consisting of nodes, edges, and elements. Quantities like the electrostatic potential or the electron and hole carrier concentrations are assigned to nodes. Fluxes like the electron or hole current are modeled along edges between the nodes. The structure of the real device obviously expands in three dimensions. However, to decrease the complexity of the problem, most applications can be reduced to a two-dimensional problem by assuming an infinite homogenous extension in the third dimension, the width of the device. This can be done if the fields and currents along the omitted dimension can be neglected, which is often possible for MOS devices. This simplification does not account for inhomogeneities along the width, effects near corners or changes in the doping profile at the border of the device are neglected. Considering that the width of the example device in this chapter is much larger than the length, most border effects are of minor importance. Further reduction of the problem complexity can be accomplished by utilizing symmetries in the device as much as possible without loosing information.

The simplest meshes used in device simulation are orthogonal grids that consist of mesh lines aligned parallel to the rectangular simulation domain (see Fig. 1.16).

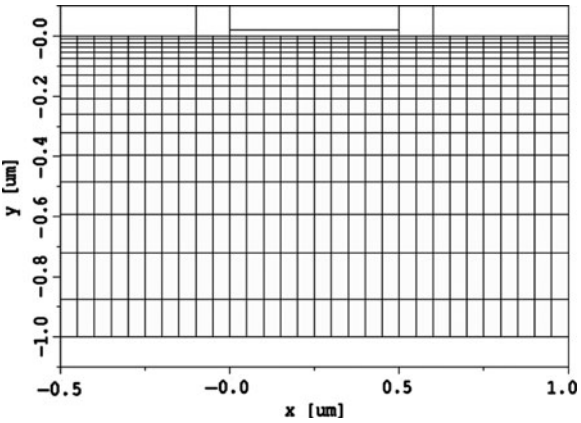

Fig. 1.16 Simple orthogonal grid of a planar MOS field effect transistor using a finer mesh near the channel

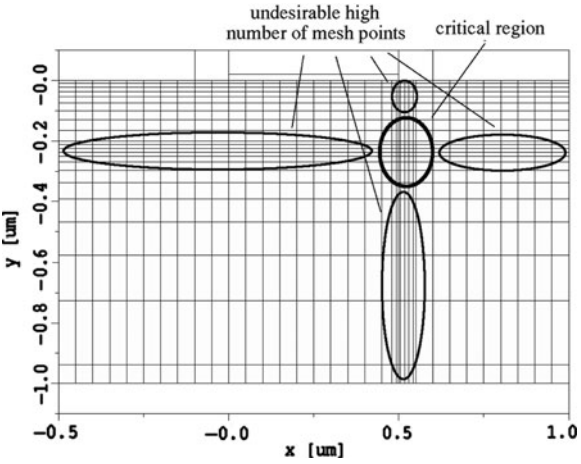

Fig. 1.17 Orthogonal grid with a refinement near the drain side of the channel. The number of grid points rises dramatically

This approach is easy to handle and not much effort is required to generate this type of mesh. In areas which require a higher spatial resolution a higher density of grid lines can be inserted. Adding grid lines is straight-forward but since grid lines are continued throughout the whole device, a high number of unnecessary mesh points in areas of low interest are created (see Fig. 1.17). This leads to long simulation times and poor convergence. Additionally, the rectangularly aligned mesh lines do not permit a smooth representation of non-planar surfaces (see Fig. 1.18), which is another major disadvantages of orthogonal grids.

Application of rectangular triangular elements allows to overcome the disadvantages mentioned above. The mesh used for the simulations on the sample device is shown in Fig. 1.19. It was created on the basis of an orthogonal mesh with refinements in areas of special interest. However, generation of triangular meshes suitable for device simulation is a cumbersome task. The box discretization (see Section 3.2) requires the mesh to fulfill the Delaunay criterion [59]. This criterion

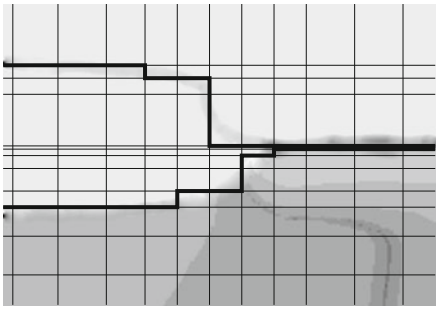

Fig. 1.18 Modeling of non-planar surfaces using orthogonal grids is not satisfying

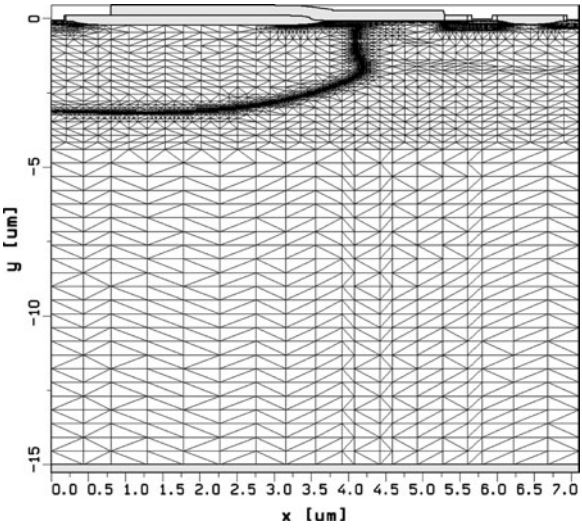

Fig. 1.19 The mesh of the sample device is based on an orthogonal grid which is triangulated and refined. Areas of special interest are the channel and the junction regions which thus require a denser mesh

describes triangular meshes constructed for a set of points such that no point is positioned inside the circumcircle of any triangle (see Fig. 1.20). This is always valid for triangulated rectangular grids but can be difficult to obtain in general. Other obstacles during mesh generation are the proper representation of borders and surfaces and the definition of mesh refinement criteria for areas of special interest. The details of the mesh refinement procedure often have to be specified manually, since mesh generation tools have no a priori information of the device behavior. Also the orientation of the elements to the current direction has to be considered, which is especially relevant in the channel region of MOS devices and additionally depends on the bias condition. Since fully automatic mesh generation would clearly simplify the work-flow, considerable efforts have been put into the development of

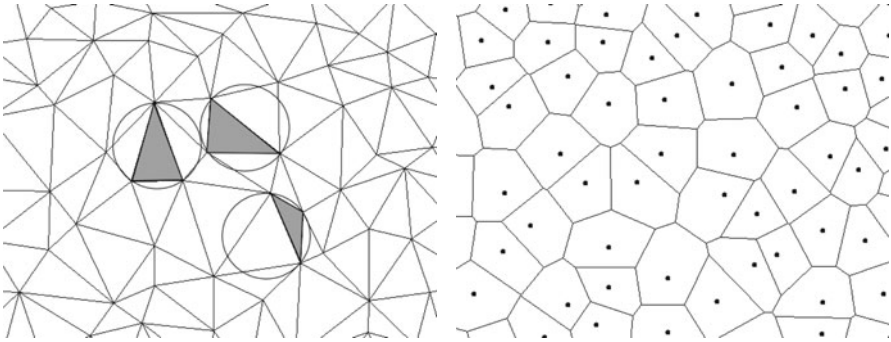

Fig. 1.20 A Delaunay mesh is shown at the left and the Voronoi tessellation of that mesh at the *right* (created using [61]). The circumcircles of three randomly selected triangles are emphasized. Every mesh point has an associated volume – every point in the domain has exactly one associated box volume

methods for automatic mesh generation. One approach applies error estimation algorithms on simulation results [60]. This information is recursively used to optimize the simulation mesh.

3.2 Discretization

The discretization of the partial differential semiconductor equations in space and time is needed to obtain difference equations which can be solved using numerical methods. A common approach for discretization of the differential equations is the box integration method [62, 63], also known as the finite volume method. For this the mesh has to fulfill the Delaunay criterion and can therefore be split into boxes using a Voronoi tessellation [59]. Doing this, every point in the domain is assigned to its closest mesh point and is therefore inside the box volume of that point (see Fig. 1.20). The basic method of the box discretization and how it is applied to the divergence operator is illustrated in the following using Poisson's equation,

$$\nabla \cdot \mathbf{D} = \rho, \tag{1.20}$$

where $\mathbf{D} = -\epsilon \nabla \psi$ and ϵ is considered to be a scalar and homogeneous. The equation can be transformed by integration over a volume V and by applying Gauss' law. With the assumption that ρ is constant inside the volume, one can write

$$\oint_{\partial V} \mathbf{D}\, \mathrm{d}\mathbf{A} = \rho V, \tag{1.21}$$

with $\mathbf{A}$ being the outwardly oriented surface area ∂V. The assumption that ρ is constant is very crude but is often used due to its simplicity [63, 64]. Other approaches

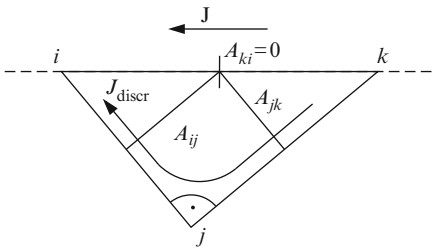

Fig. 1.21 A *triangle* aligned with its hypotenuse along the current direction. Due to the vanishing Voronoi surface A_{kj} there is no contribution along the current by the hypotenuse

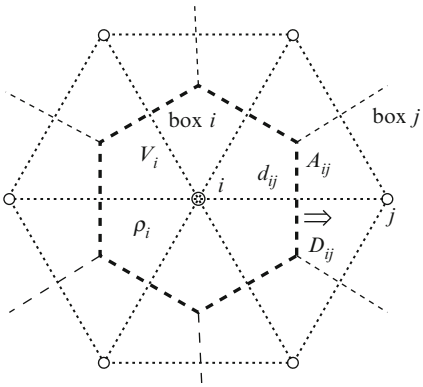

Fig. 1.22 Voronoi box i of mesh point i with connections to its neighboring mesh points. The flux D_{ij} from box i to box j through the area A_{ij} is depicted. ρ is assumed constant over the whole box volume V

estimate ρ element-wise which results in an implicitly increased resolution and a more accurate physical representation [65]. Equation 1.21 can be applied to each Voronoi box in the mesh (see Fig. 1.22). Since the boundary ∂V is a polygon (in 2D) or polyhedron (in 3D) it can be split into planar surface elements normal to the edges leading to the neighboring mesh points. For a mesh point i and its box volume V_i which has N_i neighboring boxes j, Eq. (1.21) can be approximated to

$$\sum_{j \in N_i} D_{ij} A_{ij} = \rho_i V_i . \tag{1.22}$$

D_{ij} is the dielectric flux density from box i to box j along the connecting edge through the common boundary area A_{ij}. The dielectric flux density D_{ij} can be approximated using the directional derivative of the electrostatic potential:

$$D_{ij} = \boldsymbol{\xi}_{ij} \cdot \mathbf{D} = -\epsilon \, \boldsymbol{\xi}_{ij} \cdot \nabla \psi = -\epsilon \frac{\partial \psi}{\partial \boldsymbol{\xi}_{ij}} \approx -\epsilon \frac{\psi_j - \psi_i}{d_{ij}} . \tag{1.23}$$

$\boldsymbol{\xi}_{ij}$ is the unit vector pointing from mesh points i to j and d_{ij} is the distance between the two mesh points. Discretization of the current continuity equations (1.4) and (1.5) is accomplished similarly. In the static case, at the left hand side of the discretized formulation (1.22) J_{ij} is used instead of D_{ij} and at the right hand side the

charge density ρ is replaced by the generation rate R. If the drift term dominates over the diffusion term numerical oscillation can result when a simple finite difference approach like in (1.23) is used [66]. Very fine meshes would be necessary to stabilize the system. However, a stable discretization can be obtained using the Scharfetter–Gummel method [67] instead of finite differences. Here, the drift–diffusion current equations (1.6) and (1.7) are used to solve the one-dimensional carrier concentration along the edge. The boundary conditions of the carrier concentration are given using the known values at the mesh points. The values of $J_{n,ij}$ and $J_{p,ij}$, E_{ij}, and μ_n and μ_p are considered constant along the edge. Solving this one-dimensional differential equation results in

$$J_{n,ij} = \frac{\mathrm{q}\mu_n V_\mathrm{T}}{d_{ij}}\Big(n_j \mathcal{B}(\triangle_{ij}) - n_i \mathcal{B}(-\triangle_{ij})\Big) \tag{1.24}$$

for electrons and

$$J_{p,ij} = -\frac{\mathrm{q}\mu_p V_\mathrm{T}}{d_{ij}}\Big(p_j \mathcal{B}(-\triangle_{ij}) - p_i \mathcal{B}(\triangle_{ij})\Big) \tag{1.25}$$

for holes, where $\triangle_{ij} = \big(\psi_j - \psi_i\big) / V_\mathrm{T}$ and $\mathcal{B}$ is the Bernoulli function.

The box method is used in most device simulation environments as it has proven to deliver good results and is simple to implement. Problems arise when the Delaunay criterion is violated and obtuse elements degenerate the accuracy due to negative flux areas A_{ij} [68, 69]. Also, use of the one-dimensional Scharfetter–Gummel discretization to solve multiple dimensional problems leads to the crosswind diffusion effect resulting in artificial current components normal to the actual current direction [70]. The accuracy of the discretization also degrades if triangles are aligned with the hypotenuse along the current flow. As depicted in Fig. 1.21, a vanishing boundary area A_{ki} leads according to (1.22) to a vanishing contribution of the current along this edge. A zig-zag characteristic of the discretized current is the result. There have been many proposals for more accurate discretizations (e.g. Patil in [68]). Some focus on the extension of the one-dimensional to a two-dimensional Scharfetter–Gummel current discretization [71, 72]. But none of these extensions is as universal to use as the box integration method which is dimension independent and can be used for rectangular and triangular meshes alike.

3.3 Vectors in Discretized Systems

Some physical models such as the impact-ionization rate and the high-field mobility are approximate in the drift–diffusion framework as depending on vector quantities. Impact ionization generation models depend on the electric field projected on the current density vector. Within the box method the discretization of two or three-dimensional vector quantities is based on the one-dimensional discretization along the edges ($J_{ij} = \mathbf{J} \cdot \boldsymbol{\xi}_{ij}$). Since models that are field dependent are especially relevant

for high-voltage operation conditions, break-down and snap-back simulation results are influenced by the selected vector discretization approach.

As previously discussed, the calculation of the charge ρ in the discretized Poisson equation (1.22) can be calculated per box or per element [64]. The same holds for the generation rate in the continuity equation where the right hand side reads $R_i V_i$. The rate calculation for the rate per element approach requires discretized field vectors per element. For a constant electric field in a triangular mesh, this can be accomplished exactly by a linear combination of two of the three one-dimensional edge contributions. However, for non-constant fields or for a non-linear discretization like the Scharfetter–Gummel discretization, each edge combination delivers a different result and approximations have to be made. There are different approaches how to calculate the rates and vectors for each element. One approach is the edge pair method [73], other approaches calculate the rate for every edge in the element individually [74].

For the box based approach which corresponds to the formulation in (1.22), the calculation of rates per box requires vector quantities discretized for every box. The advantage of such an approach is that a single generation rate can be evaluated per box and the continuity equation can be solved directly as shown in (1.22). A scheme to estimate vector quantities per box has been presented in [64]. This scheme has the advantage that the same implementation is suitable for triangular and orthogonal meshes alike and can thus be used for two and three-dimensional problems.

3.4 Numerical Challenges Related to HV Devices

Application of the box discretization method to the drift–diffusion model and utilizing the Scharfetter–Gummel method for the current equations is an established method used in most TCAD simulation environments [1, 36, 65]. Together with the Newton procedure for solving the equation system, a numerically stable simulation environment can be built.

Numerical challenges usually originate from the models used for the mobility and for the generation rates. Especially field dependent models, like the high-field mobility (1.13) or the impact ionization rate (1.17) may lead to convergence difficulties. The dependence on vector quantities, especially the electric field, results in couplings to many neighboring mesh points which generate many dependencies in the Jacobian matrix. The high number of non-zero entries in the system matrix leads to poor performance or failure of iterative linear solvers [75]. Additionally, strong non-linear relations, for example the exponential dependence used to model the impact ionization rate, might lead to poor convergence. Many of the numerically problematic models are important in high-voltage and power devices and therefore have to be considered in the simulation.

An approach to overcome convergence issues is to calculate more intermediate solutions between the initial simulation step (equilibrium) and the desired operating point. This can be achieved by ramping up the contact potentials step by step until

the final value is achieved. Results from former steps can be used as initial guesses for the Newton method in the next step. Decreasing the step size therefore improves the quality of the initial guess for the next step and finally for the desired operating point. Obviously a good balance between step size, robustness, and simulation time has to be found. Other approaches to overcome convergence issues are to tune the Newton procedure, for example, by changing parameters of the damping algorithm [76]. This changes the calculation of the Newton update vectors and is often required to achieve convergence.

Numerical problems are frequently caused by the simulation mesh used. For mesh design a trade-off between accuracy and numerical stability has to be found. High convergence rates can be achieved having a moderate number of well shaped elements [77]. However, smaller elements usually lead to a higher resolution and therefore to a higher accuracy. On the other hand, the limited numerical accuracy in computer systems can result in numerical noise [78] which degrades the condition of the system matrix. For accurate results, a proper alignment of the elements regarding the direction of the current flow (see Fig. 1.21) is also important. Near the channel area this often leads to poorly shaped thin elements having small internal angles. Creating a mesh for the simulation of high-voltage devices that has good numerical properties and delivers accurate results is very challenging.

Applications with special demands on the numerics of TCAD simulation tools are break-down [77], electro-static discharge (ESD) [79], and snap-back simulations. Difficulties arise from the strongly field dependent behavior and the physically unstable operating points. Physical quantities undergo strong variations near break-down and snap-back processes as the device changes its operation state. This also impacts the convergence of the device due to the state transition leading to strong changes in conductivity, current path, and carrier concentration. The different states of the devices before and after snap-back additionally result in multivalued I/V curves. The boundary conditions therefore have to be selected appropriately to avoid unintentional transitions between the branches of the I/V curve. Special curve-tracing algorithms have been suggested to deal with these problems [80, 81].

4 Conclusion

TCAD in general and numerical device simulation software in particular can be used as a very powerful tool for device engineering in academic as well as in industrial environments. The possibility of obtaining an insight into the device behavior results in a better understanding of the physics and enables the device designer to tune the device performance. Consequences of changing the device design can be tested without the time consuming and expensive fabrication of test devices. To increase the performance of special parameters, automatic optimization procedures can be set up. Optimization goals might be the maximum power output, the ratio between the on- and off-resistance, or the ratio between the maximum blocking voltage and the on-resistance.

It is important that the user of TCAD simulation tools has a fundamental knowledge of semiconductor device physics. Many different physical mechanisms have to be considered and for most of them a variety of models exist. Some models are derived to accurately describe special operation conditions, others are for multi purpose usage and cover a broad range of different operation conditions. The models also differ in the complexity leading to different simulation times. It is also important to consider that the impact of the individual physical effects are more or less important for different devices and operation conditions. Together with the understanding of how the simulation environment works, the device engineer can select the proper models and meaningful simulation results can be produced.

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Chapter 2
HiSIM-HV: A Scalable, Surface-Potential-Based Compact Model for High-Voltage MOSFETs

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Abstract The main features of the industry standard compact model HiSIM-HV for high-voltage MOSFETs are described. The basis of HiSIM-HV is a consistent physically correct potential determination in the MOSFET core and the surrounding drift regions, providing the high-voltage capabilities. Consequently, HiSIM-HV can accurately calculate the physical potential distribution in the entire asymmetric LDMOS structure or the symmetric HVMOS structure and determine all electrical and thermal high-voltage MOSFET properties without relying on any form of macro modeling or sub-circuit formulation. Furthermore, HiSIM-HV's consistent potential-based approach enables the reproduction of all structure-dependent scaling properties of high-voltage MOSFET features with a single global parameter set. The full scaling properties of HiSIM-HV with respect to the MOSFET-core geometry parameters of gate length and gate width as well as the drift-region parameters of drift-region length and drift-region doping are unique among the available compact high-voltage MOSFET models. Continuous development of HiSIM-HV is carried out in cooperation with the international semiconductor industry and improved versions of HiSIM-HV are released 2 times per year through the Compact Modeling Council (CMC).

Keywords High-voltage MOSFET · LDMOS · HVMOS · Surface potential · Consistent potential distribution · Drift region · Global parameter set · Scaling properties · Self-heating · Industry standard · Compact Modeling Council

1 Introduction

In recent years the success of cellular wireless networks, consumer appliances like digital televisions or digital cameras, mobile computers as well as automotive elec-

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tronics, has resulted in a significant increase of the practical usage of high-voltage MOSFET devices. Furthermore, advances in one-chip process technologies have allowed the integration of high-voltage devices in substantial numbers to produce complex high-voltage circuits on a single chip. Consequently, to enable a more efficient design of such integrated high-voltage circuits, the requirement for accurate compact modeling of high-voltage MOSFETs is increasing.

There are two major types of high-voltage MOSFET structures commonly used by the semiconductor industry, which have to be covered in the compact modeling. The first type is a laterally-diffused asymmetrical structure called commonly LDMOS structure. The second type is a symmetrical structure with extended drift regions at both source and drain, which we distinguish by referring to it as HVMOS because it represents the more generalized case. HiSIM-HV is valid for modeling both structure types, and has been developed as an extension of the surface-potential-based HiSIM (Hiroshima-university STARC IGFET Model) model for conventional bulk MOSFETs [1, 2].

The described practical needs for accurate compact high-voltage MOSFET modeling have also led to an international industrial effort to standardize a compact high-voltage MOSFET model for high-voltage circuit simulation, which is conducted by the Compact Model Council (CMC) [3] and recently resulted in the selection of HiSIM-HV as the international standard compact model for high-voltage MOSFETs. Several versions of the HiSIM-HV standard have been already released by the CMC and this chapter mainly describes the HiSIM-HV102 standard version. An important reason for the selection of HiSIM-HV as the industry-standard model has been the fact that it is the only existing model, which can accurately reproduce the full spectrum of high-voltage-MOSFET behavior, including the effects due to the scaling of device dimensions, with a single global parameter set and without relying on a macro-model concept by adding sub-circuits.

2 Modeling Concepts of HiSIM-HV

The high-voltage MOSFET model HiSIM-HV, reported and described in this chapter, uses a modular concept for its construction. The properties of the MOSFET core in the high-voltage structure are captured by using the advanced bulk-MOSFET model HiSIM (Hiroshima-university STARC IGFET Model), which is the first complete surface-potential-based MOSFET model for circuit simulation, and which avoids introducing any explicit-equation approximations for solving the implicit surface-potential equation of the drift–diffusion theory. The HiSIM core model is then extended and enhanced by various modular additions to construct the HiSIM-HV model. These additional modules mainly have the purpose to capture the specific properties of drift regions added to the MOSFET core for obtaining the high-voltage capabilities and to include the self-heating effect which becomes indispensable due to the increased power dissipation of a high-voltage MOSFET device during its operation.

2.1 Surface-Potential-Based Bulk-MOSFET Core Model

The HiSIM core model implements the drift–diffusion theory, which was originally developed by Pao and Sah [4], and makes this theory available in the form of a compact model for circuit simulation. The most important advantage of the surface-potential-based modeling is a unified description of the device characteristics for all bias conditions with a single although non-explicit equation. The physical reliability of the drift–diffusion theory has been proved by 2D device simulations with channel lengths down to well below 0.1 μm [5], so that it remains valid for the most advanced technologies. To obtain analytical solutions for describing device performances, the charge sheet approximation for the inversion layer with zero thickness has been introduced (for example [6]). Together with the gradual-channel approximation all device characteristics are then described analytically by the channel-surface potentials at the source side (ϕ_{S0}) and at the drain side (ϕ_{SL}) (see Fig. 2.1).

These surface potentials are functions of applied voltages on the four terminals; the gate voltage V_g, the drain voltage V_d, the bulk voltage V_b and the reference potential at the source V_s. The resistance in the contact region causes potential drops and therefore also affects the surface potential values. Since the surface potentials are implicit functions of the applied voltages, model-internal iteration procedures are introduced, but only for calculating the surface potential ϕ_{S0} at the source end and ϕ_{SL} at the end of the inversion channel. These model internal iterations are executed in addition to the global iteration of the circuit simulator. The potential $\phi_S(\Delta L)$, which appears under the saturation condition at the drain end due to the so-called channel-length modulation effect and which represents the potential drop in the pinch-off region (see Fig. 2.3), is calculated from ϕ_{S0}, ϕ_{SL} and V_{ds} involving also a fitting parameter in the respective equation.

The above described modeling concept constitutes the long-channel basis of the HiSIM model, and extensions of the model approximations are then done to capture the properties of advanced MOSFET technologies. All newly appearing phenomena

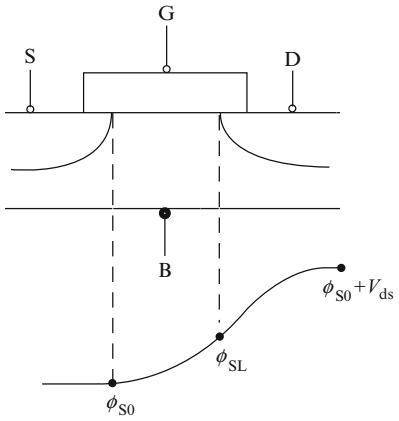

Fig. 2.1 Schematic of the surface potential distribution in the channel

such as short-channel or reverse-short-channel effects are included in the surface potential calculations and cause modifications resulting from the specific features of these advanced technologies [1].

By choosing the iterative solution in the HiSIM core, we preserve the MOSFET physics, which is built into the set of implicit equations resulting from the rigorous application of the drift–diffusion theory. Since an iterative solution is commonly believed to result in an execution-time penalty for the compact model, specific attention is directed towards calculating the surface potentials with enough accuracy under the boundary condition of a small CPU run-time. The number of HiSIM-internal iteration steps could in particular be reduced to an average of two steps in typical circuit-simulation tasks. Furthermore, with advancing scaled-down fabrication technologies, the necessity of including higher-order phenomena like noise effects, non-quasi-static (NQS) effects, or non-homogeneous channel doping into the compact models turned out to be less a burden for HiSIM with its iterative approach than for other non-iterative approaches. Up to now the validity of HiSIM has been tested for channel lengths down to 45 nm with CMOS fabrication technologies using the pocket-implant technology. All theoretical descriptions and equations in the following sections of this chapter are given for the n-channel MOSFET, but they are of course also valid for the p-channel case with the appropriate modifications to account for the exchange of p- and n-doped regions.

2.2 High-Voltage LDMOS Structure

The most important features of LDMOS and HVMOS devices, different from the conventional MOSFET, are originating from the drift region introduced to achieve the sustainability of high voltages. By varying the length and the dopant concentration of this drift region as well as the length of the gate-overlap region, various device types with a variety of operating bias conditions are realized as shown in Fig. 2.2 for the LDMOS structure, which features a drift region only at its drain side. In any of these modified cases, the drift region represent a dynamically varying resistance for the current flow and also induces additional charges, which cause the

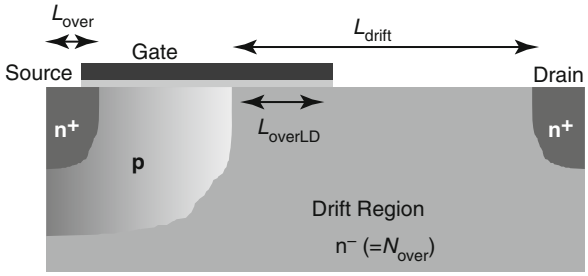

Fig. 2.2 Schematic of the typical LDMOS device structure and the respective structure parameters

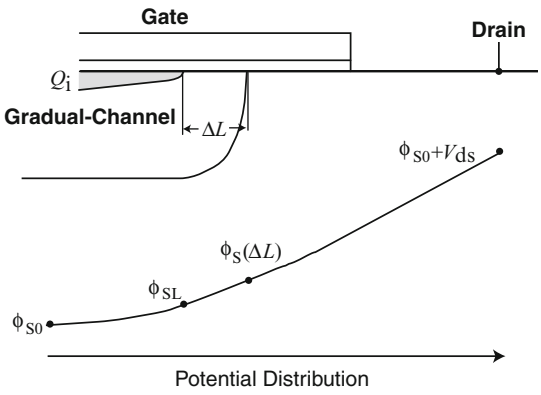

Fig. 2.3 Schematic of the surface potential distribution in the channel at the drain side of the LDMOS device structure

especially unique features of the LDMOS and HVMOS capacitances. Thus accurate modeling of the drift region is the main task for the construction of the HiSIM-HV compact model.

A fortunate feature of the HiSIM compact model, which simplifies the physically consistent capturing of the drift-region properties, is the fact that HiSIM determines the complete potential distribution along the gate from source to drain contact, namely the surface potential at the source side ϕ_{S0}, the surface potential at the pinch-off point ϕ_{SL}, the potential at the channel/drain junction, $\phi_S(\Delta L)$, and the final potential value at the drain contact $\phi_{S0} + V_{ds}$ as shown in simplified from in Fig. 2.3.

For the LDMOS devices it turns out, that the iterative solution for obtaining accurate potentials is the only possible solution to model the specific features of these devices accurately and in a physically consistent way. In particular, if one aims at obtaining a scalable compact high-voltage MOSFET model with respect to gate length, gate width and drift-region length, an iterative solution is unavoidable. The main reason for this comes from the subtle dependence of the potential at the beginning of the drift region, and therefore of the resistance effect in the drift region, on the bias conditions as well as on the detailed geometrical LDMOS structure. The basic modeling method of HiSIM is already suitable for this purpose and can thus be taken over from the HiSIM2 model for advanced MOSFETs [7]. Further equations for capturing the drift-region effects are then included within the framework of HiSIM's modeling method. Since the overlap length is, in comparison to the bulk MOSFET, relatively long for LDMOS devices, accurate surface-potential calculation for this overlap region as a function of applied voltages is also necessary for accurate prediction of the capacitances of the high-voltage LDMOS device.

2.3 General High-Voltage MOSFET Structure

To make the structural definition flexible, the Flag **COSYM** is introduced in HiSIM-HV, as shown in Fig. 2.4. **COSYM** $= 0$ refers to the asymmetrical LDMOS case, where drain-side and source-side parameters are different because the source side

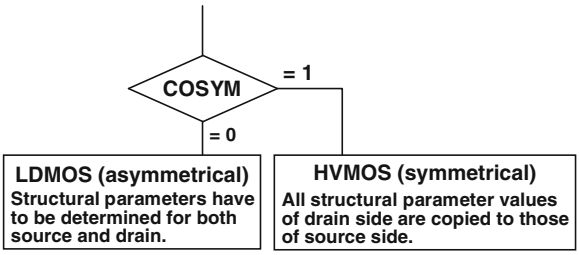

Fig. 2.4 Selection of LDMOS or HVMOS compact-model cases, including respective model parameters, in HiSIM-HV by setting the flag COSYM

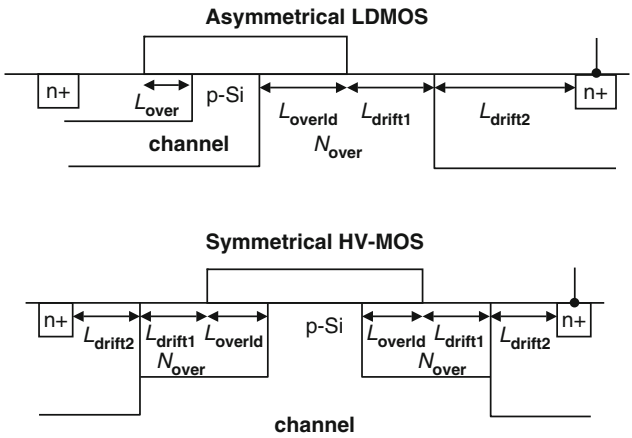

Fig. 2.5 Structure parameters asymmetrical and symmetrical structures selectable in HiSIM-HV

does not include a drift region. **COSYM** = 1 refers to the symmetrical HVMOS case, and all parameter types of the drain side, especially those related to the drift region, have to be determined also for the source side.

HiSIM-HV considers the length of the drift region L_{drift}, the overlap length L_{over}, and the impurity concentration of the drift region N_{over} explicitly. Schematics of the general structures for LDMOS and HVMOS are shown in Fig. 2.5 for the n-channel case. For the LDMOS device, independent structures at the source side and the drain side can be distinguished, due to the fact that the L_{drift} region is not present at the source side. In the HVMOS case, the drift-region-related parameter values for the source side have to be determined, and are copied from the drain-side parameters, automatically. If the drift-region related parameters are not determined, default values are taken.

One most significant feature of the LDMOS/HVMOS devices is that the drain current continues to increase quite steeply even under the saturation condition, which is referred to as the quasi saturation. Other peculiar features are observed in the capacitances, showing strong sharp peaks, which significantly change depending on the structure as well as doping levels. All these phenomena are caused by

Table 2.1 HiSIM-HV model parameters introduced in Section 2 of this chapter

LOVER	Overlap length at source side
LOVERLD	Overlap length at drain, and at source, if **COSYM** = 1
LDRIFT1	Length of lightly doped drift region at drain, and at source, if **COSYM** = 1
LDRIFT2	Length of heavily doped drift region at drain, and at source, if **COSYM** = 1
NOVER	Impurity concentration of **LOVERLD** at drain, and at source, if **COSYM** = 1
VBSMIN	Minimum V_{bs} voltage applied

the highly resistive drift region, enabling the high-voltage application of MOSFETs. The structural parameters of the LDMOS/HVMOS devices are explicitly considered in the resistance modeling, and the resistance effect is considered as a potential drop, which is determined iteratively within HiSIM-HV.

Consequently, the basic modeling concept of LDMOS/HVMOS devices is kept the same as in the HiSIM2 model for the conventional MOSFET. HiSIM-HV also determines the potential distribution between source and drain contacts by solving the Poisson equation iteratively, but includes the resistance effect in the drift region and considers the bias dependence of this resistance.

HiSIM-HV limits the minimum value of the applied bulk voltage V_{bs} to -10.5V. However, this limitation can be changed by adjusting the model parameter **VBSMIN**.

The HiSIM-HV model parameters introduced in Section 2 are summarized in Table 2.1.

3 Implementation of the HiSIM-HV Modeling Concept

As explained in the previous section HiSIM-HV has been developed by building on the bulk-MOSFET model HiSIM2, which is used as the core part. The specific effects of a high-voltage MOSFET, due to the added drift regions for providing the high-voltage blocking and switching capability, are the added in a modular way by either modifying affected modules for certain phenomena already considered in HiSIM2 or by adding new modules.

In this section, the main changes of HiSIM2, which were implemented to develop HiSIM-HV, and which affect the capacitance model, the resistance model, the non-quasi-static (NQS) model, as well as the implementation of the self-heating effect, are described in this section in more detail.

3.1 Capacitances

The capacitance model of HiSIM-HV remains conceptually very similar to that of the bulk-MOSFET model HiSIM2 and mainly covers in addition the increased overlap capacitances including their surface-potential dependence.

3.1.1 Intrinsic Capacitances

The intrinsic capacitances are derivatives of the node charges determined as

$$C_{jk} = \delta \frac{\partial Q_j}{\partial V_k}$$
$$\delta = -1 \quad \text{for} \quad j \neq k$$
$$\delta = 1 \quad \text{for} \quad j = k \tag{2.1}$$

HiSIM-HV uses analytical solutions for all nine independent intrinsic capacitances, derived from the equations for the respective terminal charges [7] as explicit functions of the surface potentials. Therefore, there are no extra model parameters required for the intrinsic capacitances.

The lateral electric field along the channel induces a capacitance C_{Q_y} which significantly affects the gate capacitance in saturation [8]. This induced charge associated with C_{Q_y} is described with the surface potential values as

$$Q_y = \epsilon_{\mathrm{Si}} W_{\mathrm{eff}} \cdot \mathbf{NF} W_{\mathrm{d}} \left(\frac{\phi_{\mathrm{S0}} + V_{\mathrm{ds}} - \phi_{\mathrm{S}}(\Delta L)}{\mathbf{XQY}} \right) + \frac{\mathbf{XQY1}}{L_{\mathrm{gate}}^{\mathbf{XQY2}}} V_{\mathrm{bs}} \tag{2.2}$$

introducing **XQY**, a parameter determining the maximum field at the channel/drain junction independent of L_{gate}. For $\mathbf{XQY} = 0$ the charge Q_{y} is fixed to zero. To compensate the enhanced short-channel effect, determined by the current characteristics, two model parameters **XQY1** and **XQY2** are introduced. Under the saturation condition, C_{Q_y} together with the overlap capacitance dominates the gate-drain capacitance C_{gd}. This effect is more visibly observed as the gate-length reduces. Therefore, in the C_{gd} modeling, C_{Q_y} is added to the conventional components as depicted in Fig. 2.6 and replaces the so-called inner-fringing field effects which are conventionally applied [9]. To activate Q_{y} the model parameter **CLM1** must be smaller than unity.

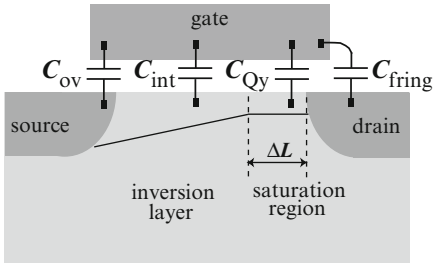

Fig. 2.6 Modeling of the gate-drain capacitance with C_{Q_y} added to the conventional capacitance components

3.1.2 Overlap Capacitances

The overlap charge at the drain side is written as

$$\frac{Q_{\text{god}}}{W_{\text{eff}} \cdot \mathbf{NF} \cdot C_{\text{ox}}} = \int_0^{\mathbf{LOVERLD}} (V_{\text{gs}} - \phi_{\text{S}}) dy \tag{2.3}$$

Thus the surface-potential distribution along the overlap region determines the charge and the capacitance. The potential increase of $\phi_{\text{S}}(y)$ from $\phi_{\text{S}}(\Delta L)$ to $\phi_{\text{S0}} + V_{\text{ds}}$ is modeled by considering the lateral impurity-profile gradient of the drain contact [10]. However, the influence of the gradient is often negligible, and only the surface-potential change as a function of the applied voltage is considered here.

The overlap capacitance includes three model options as summarized in Fig. 2.7. Besides the constant overlap-capacitance option, two bias dependent models are provided: One considers the surface potential change as a function of V_{gs} and the other calculates the overlap capacitance with a simplified V_{gs} dependence.

(i) Surface-Potential-Based Model

The surface-potential-based concept for the overlap capacitance is described here for the drain side. For the source side the same calculation is performed with $V_{\text{ds}} = 0$. The calculation of the surface potential in the drain contact region is done for all possible conditions, from the inversion condition to the accumulation condition. The surface potential ϕ_{S} is calculated in the same manner as in the channel region, and only the polarity is inverted in comparison to the channel. The final overlap charge equation is written with the calculated ϕ_{S}

(a) under the depletion and the accumulation conditions

$$Q_{\text{over}} = W_{\text{eff}} \cdot \mathbf{NF} \cdot \mathbf{LOVERLD} \cdot \left(\sqrt{\frac{2\epsilon_{\text{Si}} q \mathbf{NOVER}}{\beta}} \sqrt{\beta(\phi_{\text{S}} + V_{\text{ds}}) - 1} \right) \tag{2.4}$$

(b) under the inversion condition

$$Q_{\text{over}} = W_{\text{eff}} \cdot \mathbf{NF} \cdot \mathbf{LOVERLD} \cdot C_{\text{ox}} \left[(V_{\text{gs}} - \mathbf{VFBOVER} - \phi_{\text{S}}) \right] \tag{2.5}$$

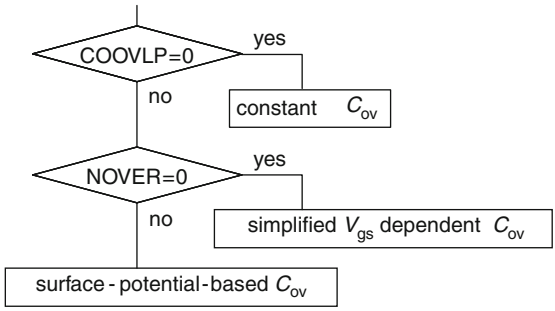

Fig. 2.7 Summary of the HiSIM-HV model options for the overlap capacitance

where **LOVERLD** is the length of the overlap region of the gate over the drain, **NOVER** is the impurity concentration in the drain contact region, and **VFBOVER** is the flat-band voltage in the overlap region. This model is selected, if **NOVER** is not equal to 0.

A smoothing function is introduced with a model parameter **QOVSM** to achieve a smooth transition between the depletion region and the inversion region of the overlap charge.

(ii) Simplified Bias-Dependent Model

If **LOVER** > 0 and the flag **COOVLP** $= 1$, the overlap gate charge at the source side is modeled as

$$\begin{aligned}\frac{Q_{\mathrm{gos}}}{W_{\mathrm{eff}} \cdot \mathbf{NF} \cdot C_{\mathrm{ox}}} &= V_{\mathrm{gs}} \cdot \mathbf{LOVER} \\ &\quad - \mathbf{OVSLP} \cdot (1.2 - (\phi_{\mathrm{S0}} - V_{\mathrm{bs}})) \\ &\quad \cdot (\mathbf{OVMAG} + V_{\mathrm{gs}})\end{aligned} \tag{2.6}$$

If **NOVER** is equal to 0, the overlap charge at the drain is also calculated with the same type of simplified equation as

$$\begin{aligned}\frac{Q_{\mathrm{god}}}{W_{\mathrm{eff}} \cdot \mathbf{NF} \cdot C_{\mathrm{ox}}} &= (V_{\mathrm{gs}} - V_{\mathrm{ds}}) \cdot \mathbf{LOVERLD} \\ &\quad - \mathbf{OVSLP} \cdot (1.2 - (\phi_{\mathrm{SL}} - V_{\mathrm{bs}})) \\ &\quad \times (\mathbf{OVMAG} + V_{\mathrm{gs}})\end{aligned} \tag{2.7}$$

The overlap capacitance at the source side is calculated by differentiating Q_{gos}. Whereas the overlap capacitances at the drain side is calculated by differentiating either Q_{god} or Q_{over} of the overlap charge equations.

In summary these bias-dependent overlap-capacitance models can be selected using the model flag **COOVLP** $= 1$, and require **OVSLP** and **OVMAG** or **NOVER** and **VFBOVER** in addition as model parameters. For further model adjustments **LOVER** (overlap length) is used.

The default overlap capacitance flag (**COOVLP** $=$ 0) calculates bias-independent drain and source overlap capacitances. User-defined values can be specified using the input parameters **CGDO** and **CGSO**. If these values are not specified, the overlap capacitances are calculated using

$$C_{\mathrm{ov}} = -\frac{\epsilon_{\mathrm{ox}}}{\mathbf{TOX}} \mathbf{LOVER} \cdot W_{\mathrm{eff}} \cdot \mathbf{NF} \tag{2.8}$$

The gate-to-bulk overlap capacitance $C_{\mathrm{gbo\_loc}}$ is calculated only with a user-defined value **CGBO** using

$$C_{\mathrm{gbo\_loc}} = -\mathbf{CGBO} \cdot L_{\mathrm{gate}} \tag{2.9}$$

independent of the model flag **COOVLP**.

Table 2.2 HiSIM-HV model parameters introduced in subsection 3.1 of this chapter

XQY	Distance from drain junction to maximum electric field point
***XQY1**	V_{bs} dependence of Q_y
***XQY2**	L_{gate} dependence of Q_y
VFBOVER	Flat-band voltage in overlap region
***QOVSM**	Smoothing Q_{over} at depletion/inversion transition
OVSLP	Coefficient for overlap capacitance
OVMAG	Coefficient for overlap capacitance
CGSO	Gate-to-source overlap capacitance
CGDO	Gate-to-drain overlap capacitance
CGBO	Gate-to-bulk overlap capacitance
TPOLY	Height of the gate poly-Si

3.1.3 Extrinsic Capacitances

The outer fringing capacitance is modeled as [11]

$$C_f = \frac{\epsilon_{ox}}{\pi/2} W_{gate} \cdot \mathbf{NF} \cdot \ln\left(1 + \frac{\mathbf{TPOLY}}{T_{ox}}\right) \tag{2.10}$$

where **TPOLY** is the gate-poly thickness. This outer fringing capacitance is bias independent.

The HiSIM-HV model parameters introduced in Section 3.1 are summarized in Table 2.2.

3.2 Resistances of the High-Voltage MOSFET

This section describes the equations of the resistance model for the LDMOS case. In the symmetrical HVMOS case, the resistance at the source side is modeled with the same equations as for the drain side in the LDMOS case, but without the V_{ds} dependence.

The source and the drain resistances R_s and R_d are considered by voltage drops across each of the resistances as:

$$V_{gs,eff} = V_{gs} - I_{ds} \cdot R_s \tag{2.11}$$

$$V_{ds,eff} = V_{ds} - I_{ds} \cdot (R_s + R_{drift}) \tag{2.12}$$

$$V_{bs,eff} = V_{bs} - I_{ds} \cdot R_s \tag{2.13}$$

where

$$R_s = \frac{\mathbf{RS}}{W_{eff}} + \mathbf{NRS} \cdot \mathbf{RSH} \tag{2.14}$$

$$R_{\mathrm{drift}} = (R_{\mathrm{d}} + V_{\mathrm{ds}} \cdot R_{\mathrm{DVD}}) \left(1 + \mathbf{RDVG11} - \frac{\mathbf{RDVG11}}{\mathbf{RDVG12}} \cdot V_{\mathrm{gs}}\right) \times (1 - V_{\mathrm{bs}} \cdot \mathbf{RDVB}) \tag{2.15}$$

and

$$R_{\mathrm{d}} = \frac{R_{\mathrm{d0}}}{W_{\mathrm{eff}}} \left(1 + \frac{\mathbf{RDS}}{(W_{\mathrm{gate}} \cdot 10^4 \times L_{\mathrm{gate}} \cdot 10^4)^{\mathbf{RDSP}}}\right) + \mathbf{RSH} \cdot \mathbf{NRD} \tag{2.16}$$

$$R_{\mathrm{d0}} = \left(\mathbf{RD} + R_{\mathrm{d0,temp}}\right) f_1 \cdot f_2 \tag{2.17}$$

$$R_{\mathrm{DVD}} = \frac{\mathbf{RDVD} + R_{\mathrm{dvd,temp}}}{W_{\mathrm{eff}}} \cdot \exp\left(-\mathbf{RDVDL} \times (L_{\mathrm{gate}} \cdot 10^4)^{\mathbf{RDVDLP}}\right) \cdot \left(1 + \frac{\mathbf{RDVDS}}{(W_{\mathrm{gate}} \cdot 10^4 \times L_{\mathrm{gate}} \cdot 10^4)^{\mathbf{RDVDSP}}}\right) \cdot f_1 \cdot f_3 \tag{2.18}$$

$$f_1(L_{\mathrm{drift1}}) = \frac{\mathbf{LDRIFT1}}{1\mu\mathrm{m}} \cdot \mathbf{RDSLP1} + \mathbf{RDICT1} \tag{2.19}$$

$$f_2(L_{\mathrm{drift2}}) = \frac{\mathbf{LDRIFT2}}{1\mu\mathrm{m}} \cdot \mathbf{RDSLP2} + \mathbf{RDICT2} \tag{2.20}$$

$$f_3(L_{\mathrm{over}}) = 1 + \mathbf{RDOV11} - \frac{\mathbf{RDOV11}}{\mathbf{RDOV12}} \cdot \frac{\mathbf{LOVERLD}}{1\mu\mathrm{m}} \tag{2.21}$$

NRS and **NRD** are instance parameters describing the number of squares resulting from the geometrical layout of the source and the drain diffusions, while **RSH** is the sheet resistance of one square of diffusion area. In each of the Eqs. 2.14 and 2.16, the first term of the right hand side considers the resistance of the LDD region and the drift region, and the second term takes account of the diffusion region, which is layout dependent. **LDRIFT1** and **LDRIFT2** are model parameters denoting the length of different parts of the drift region (see Fig. 2.5). The source resistance in the LDMOS case, for which the above equations are valid, does not include a drift region and has therefore no drift length parameters.

The voltage drops at the source and the drain resistances are calculated iteratively within HiSIM-HV for given terminal voltages to keep consistency among all device performances. However, R_{s} and R_{drift} can also be treated as extrinsic resistances, and can be included in an equivalent circuit applied externally. Consequently, the parasitic source and drain resistances, R_{s} and R_{drift}, can be taken account of in HiSIM-HV by two optional approaches. The first approach is to include them as external resistances, so that the circuit simulator generates nodes and finds the solution with the source/drain resistances iteratively (Flag: **CORSRD** $= -1$). The

second approach is to include them as internal resistances of HiSIM-HV, so that HiSIM-HV solves iteratively for the now internal nodes (Flag: **CORSRD** $= 1$). The Flag **CORSRD** is provided for the selection of one of the altogether four possible approaches, namely **CORSRD** $= 0, 1, 2, -1$ meaning "no resistance", "internal", "analytical", and "external" source/drain resistances, respectively. The selection procedure of the different options by the Flag **CORSRD** is summarized in the flow-diagram of Fig. 2.8.

A further flag option **CORSRD** $= 2$ was originally introduced to avoid simulation time penalties by providing the possibility of an analytical description of the resistance effect as

$$I_{\mathrm{ds}} = \frac{I_{\mathrm{ds0}}}{1 + I_{\mathrm{ds0}} \frac{R_{\mathrm{d}}}{V_{\mathrm{ds}}}} \tag{2.22}$$

where I_{ds0} is the drain current without the resistance effect and where R'_{d} takes account of the resistance effect in the following simplified form.

$$R_{\mathrm{d}} = \frac{1}{W_{\mathrm{eff}}} \left(R'_{\mathrm{d}} \cdot V_{\mathrm{ds}}^{\mathbf{RD21}} + V_{\mathrm{bs}} \cdot \mathbf{RD22} \right) \tag{2.23}$$

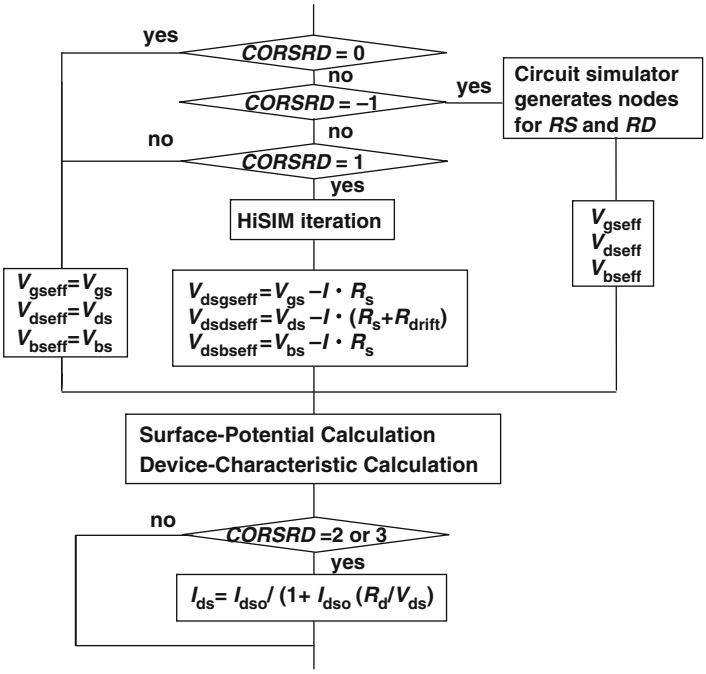

Fig. 2.8 Model options provided in HiSIM-HV for the resistance models at source and drain side, and their selection by the Flag **CORSRD**

The magnitude determination of the resistance R'_{d} includes equations with parameters introduced to consider the resistance reduction due to the current flow in the drift region. Further model parameters have the purpose to include the size dependences of the resistance as

$$R'_{\mathrm{d}} = RD23' \tag{2.24}$$

where

$$RD23' = \mathbf{RD23} \cdot \exp\left(-\mathbf{RD23L} \times (L_{\mathrm{gate}} \cdot 10^4)^{\mathbf{RD23LP}}\right) \cdot \left(1 + \frac{\mathbf{RD23S}}{(W_{\mathrm{gate}} \cdot 10^4 \times L_{\mathrm{gate}} \cdot 10^4)^{\mathbf{RD23SP}}}\right) \tag{2.25}$$

For large V_{gs}, it happens that the resistance effect becomes too strong with the global parameter set fitted to the whole V_{gs} regime. For covering also this effect for large V_{gs} in the global parameter set, the V_{gs} dependence has to be included by the introduction of further model parameters. In HiSIM-HV the equation for R'_{d} is therefore modified to the form

$$R'_{\mathrm{d}} = \mathbf{RD24}\left(V_{\mathrm{gs}} - \mathbf{RD25}\right) \tag{2.26}$$

where the modification of R'_{d} itself is restricted with two boundaries, namely with a lower boundary defined to be $RD23'$ and with an upper boundary given by $RD23'$ multiplied with $(1 + \mathbf{RD20})$ as

$$RD23' \leq R'_{\mathrm{d}} \leq RD23'(1 + \mathbf{RD20}) \tag{2.27}$$

If $\mathbf{RD20} = 0$, R'_{d} reduces to $RD23'$, meaning that the R'_{d} modification is deselected. For the LDMOS case **RD21** (see Eq. 2.23) is normally fixed to be unity. Here it should to be noticed that the described resistance affects only the drain current, and that the LDMOS capacitances are not influenced.

The accurate approach to consider the resistance effect is to treat it with an internal node by selecting ($\mathbf{CORSRD} = 1$). However, in cases where it is necessary, both types of resistance models (internal-node approach and analytical approach) can be applied with $\mathbf{CORSRD} = 3$ simultaneously.

The approach with external source/drain resistances ($\mathbf{CORSRD} = -1$) leads to shorter simulation times for circuits with small to medium transistor numbers, while the approach with internal source/drain resistances leads to shorter simulation times for circuits with very large transistor numbers. The transistor number, for which both approaches result in approximately equal simulation times (the switching point for the choice between the two approximations) is normally between 10,000 and 50,000 transistors.

The gate resistance becomes larger when the gate width increases, and therefore the gate-resistance effect has to be included in the compact model for correctly simulating the circuit properties at sufficiently high operating frequencies, a condition

which applies for the practical operation frequencies of many RF circuits. The approach for the gate-resistance calculation applied in HiSIM-HV is similar to that used in BSIM4 [12] and is described by the equation

$$R_{\mathrm{g}} = \frac{\mathbf{RSHG} \cdot \left(\mathbf{XGW} + \frac{W_{\mathrm{eff}}}{3 \cdot \mathbf{NGCON}}\right)}{\mathbf{NGCON} \cdot (L_{\mathrm{drawn}} - \mathbf{XGL}) \cdot \mathbf{NF}} \tag{2.28}$$

where the parameter **RSHG** is the gate's sheet resistance, while the other parameters are instance parameters dependent on the layout. The flag **CORG** is provided for selecting the inclusion of the gate resistance. The flag settings **CORG** $= 0, 1$ mean "no", "external" gate resistance, respectively.

Model parameters for the same substrate resistance network as applied in BSIM4 (**RBPB**, **RBPD**, **RBPS**, **RBDB**, **RBSB**) are additionally included in the model parameter list, and these parameters are also treated as instance parameters.

The HiSIM-HV model parameters introduced in Section 3.2 are summarized in Table 2.3.

3.3 Non-Quasi-Static (NQS) Model

Carriers in the channel and the drift region take time to build-up as opposed to the quasi-static (QS) approximation. In HiSIM-HV, the carrier formation within the device is modeled by considering the carrier-delay mechanisms as described in the following subsections.

3.3.1 Carrier Formation

To consider the non-quasi-static (NQS) phenomenon of carrier delay in HiSIM-HV, the carrier formation is modeled as [13–15]

$$q(t_{\mathrm{i}}) = \frac{q(t_{\mathrm{i}-1}) + \frac{\Delta t}{\tau} Q(t_{\mathrm{i}})}{1 + \frac{\Delta t}{\tau}} \tag{2.29}$$

where $q(t_{\mathrm{i}})$ and $Q(t_{\mathrm{i}})$ represent the non-quasi-static (NQS) and the quasi-static (QS) carrier density at time t_{i}, respectively, while $\Delta t = t_{\mathrm{i}} - t_{\mathrm{i}-1}$ is the time interval parameter between two sequential time points in the circuit simulation. Equation 2.29 implies that the formation of carriers under the NQS approximation is always delayed in comparison to the QS approximation, and therefore captures the basic physical origin of the NQS effect. The delay in changes of the charge density is determined by the carrier transit delay τ and the time interval Δt used in the circuit simulation.

Table 2.3 HiSIM-HV model parameters introduced in Section 3.2 of this chapter

RS	Source-contact resistance of LDD region
RD	Drain-contact resistance of LDD region
RSH	Source/drain sheet resistance of diffusion region
RSHG	Gate sheet resistance
RBPB	Substrate resistance network
RBPD	Substrate resistance network
RBPS	Substrate resistance network
RBDB	Substrate resistance network
RBSB	Substrate resistance network
#NRS	Number of source squares
#NRD	Number of drain squares
#XGW	Distance from the gate contact to the channel edge
#XGL	Offset of the gate length
#NF	Number of fingers
#NGCON	Number of gate contacts
***RDVG11**	V_{gs} dependence of **RD** for **CORSRD** $= 1, 3$
***RDVG12**	V_{gs} dependence of **RD** for **CORSRD** $= 1, 3$
RDVD	V_{ds} dependence of **RD** for **CORSRD** $= 1, 3$
RDVB	V_{bs} dependence of **RD** for **CORSRD** $= 1, 3$
***RDS**	Small size dependence of **RD** for **CORSRD** $= 1, 3$
***RDSP**	Small size dependence of **RD** for **CORSRD** $= 1, 3$
***RDVDL**	L_{gate} dependence of **RD** for **CORSRD** $= 1, 3$
***RDVDLP**	L_{gate} dependence of **RD** for **CORSRD** $= 1, 3$
***RDVDS**	Small size dependence of **RD** for **CORSRD** $= 1, 3$
***RDVDSP**	Small size dependence of **RD** for **CORSRD** $= 1, 3$
RDOV11	L_{over} dependence of resistance for **CORSRD** $= 1, 3$
RDOV12	L_{over} dependence of resistance for **CORSRD** $= 1, 3$
RDSLP1	L_{drift1} dependence of resistances for **CORSRD** $= 1, 3$
RDICT1	L_{drift1} dependence of resistances for **CORSRD** $= 1, 3$
RDSLP2	L_{drift2} dependence of resistances for **CORSRD** $= 1, 3$
RDICT2	L_{drift2} dependence of resistances for **CORSRD** $= 1, 3$
RD20	**RD23** boundary for **CORSRD** $= 2, 3$
RD21	V_{ds} dependence of **RD** for **CORSRD** $= 2, 3$
RD22	V_{bs} dependence of **RD** for **CORSRD** $= 2, 3$
RD23	Modification of **RD** for **CORSRD** $= 2, 3$
***RD23L**	L_{gate} dependence of **RD21** boundary for **CORSRD** $= 2, 3$
***RD23LP**	L_{gate} dependence of **RD21** boundary for **CORSRD** $= 2, 3$
***RD23S**	Small size dependence of **RD21** for **CORSRD** $= 2, 3$
***RD23SP**	Small size dependence of **RD21** for **CORSRD** $= 2, 3$
***RD24**	V_{gs} dependence of **RD** for **CORSRD** $= 2, 3$
***RD25**	V_{gs} dependence of **RD** for **CORSRD** $= 2, 3$

#indicates instance parameters and * indicates minor parameters

3.3.2 Delay Mechanisms

Up to the weak inversion regime, the carriers diffuse into the channel and the transit delay can be approximated by

$$\tau_{\mathrm{diff}} = \mathbf{DLY1} \tag{2.30}$$

In the strong inversion regime, there is already conduction due to field-driven carriers which dominates the carrier movement. The transit delay due to this flow of conductive carriers is

$$\tau_{\mathrm{cond}} = \mathbf{DLY2} \cdot \frac{Q_{\mathrm{i}}}{I_{\mathrm{ds}}} \tag{2.31}$$

where **DLY2** is a constant coefficient. These two delay mechanisms (diffusion and conduction) are combined in HiSIM-HV by using the Matthiessen rule

$$\frac{1}{\tau} = \frac{1}{\tau_{\mathrm{diff}}} + \frac{1}{\tau_{\mathrm{cond}}} \tag{2.32}$$

Carrier delay mechanisms in a switch-on operation of the MOSFET part with a gate-voltage rise time t_{r} of 20ps are illustrated in Fig. 2.9.

Applying the same approach of a carrier transit delay also for the formation of bulk carriers, leads to the approximation of the bulk carrier delay as an RC delay in the form

$$\tau_{\mathrm{B}} = \mathbf{DLY3} \cdot C_{\mathrm{ox}} \tag{2.33}$$

where **DLY3** is a constant coefficient and C_{ox} is the oxide capacitance of the gate.

3.3.3 Time-Domain Analysis

The total drain/source/bulk terminal currents in the MOSFET part are derived from the superposition of the transport current and the charging current. The transport

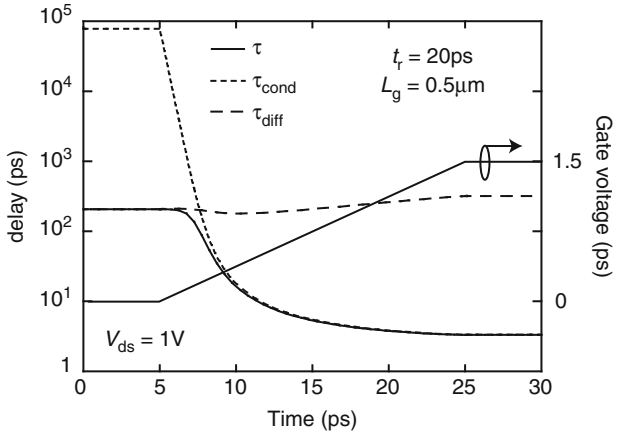

Fig. 2.9 Example of the dynamically calculated transit delay times, as incorporated in the NQS model for the MOSFET part of HiSIM-HV, in a switch-on simulation

current is a function of the instantaneous terminal voltages and is approximated by the steady-state solution. The source/drain/bulk charging currents are the time derivatives of the associated non-quasi-static (NQS) charges, q_S, q_D, and q_B, respectively.

For high-voltage LDMOS/HVMOS devices, the carrier transit delay τ in the drift regions becomes additionally very important, because the considerable length of these drift regions contributes a strong NQS effect during their charging and discharging. The compact modeling of the NQS effect due to the drift region is done in a similar way as for the channel region using the following equation.

$$\tau_{LD} = \frac{(\mathbf{LOVERLD} + \mathbf{LDRIFT1} + \mathbf{LDRIFT2})^2}{\mathbf{DLYDFT} \cdot (V_{ds} - \phi_{SL} + \phi_{S0})} \tag{2.34}$$

The formation delay of the equilibrium charge density for the accumulation condition is also modeled in HiSIM-HV as

$$\tau_{LD} = \mathbf{DLYOV} \cdot C_{ox0} \tag{2.35}$$

The HiSIM-HV model parameters described in Section 3.3 are summarized in Table 2.4.

3.4 Modeling of the Self-Heating Effect

The self-heating effect is modeled in HiSIM-HV according to a conventional approach with the thermal network shown in Fig. 2.10. The self-heating extension is completely integrated in the HiSIM-HV model equations and does therefore not require a subcircuit approach. The flag **COSELFHEAT** must be set equal to 1 and **RTH0** must not be set equal to 0 to activate the self-heating model. The temperature node is automatically generated in the circuit simulator for each device as it is also done with other bias nodes. First, the model core (HiSIM.eval) is called to evaluate device characteristics without heating. Then, the temperature is updated considering the self-heating effect by creating the temperature node. The model core is then

Table 2.4 HiSIM-HV model parameters introduced in Section 3.3 of this chapter

DLY1	Coefficient for delay due to diffusion of carriers
DLY2	Coefficient for delay due to conduction of carriers
DLY3	Coefficient for RC delay of bulk carriers
LOVERLD	Length of the gate-overlap part of the drift region
LDRIFT1	Length of the first lower-doped part of the drift region
LDRIFT2	Length of the second higher-doped part of the drift region
DLYDFT	Coefficient for carrier transit delay
DLYOV	Coefficient for RC delay of carriers for the accumulation condition

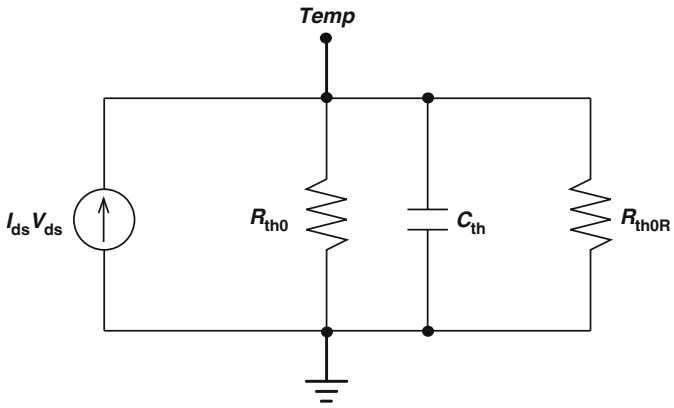

Fig. 2.10 Thermal Network applied for the self-heating effect

called again to update the device characteristics with the calculated temperature T. Under the DC condition the temperature increase is calculated analytically as

$$T = T + R_{\mathrm{TH}} \cdot I_{\mathrm{ds}} \cdot V_{\mathrm{ds}} \tag{2.36}$$

The model parameter **RTH0** is thermal-resistance related and is fitted to measured DC data, while the model parameter **CTH0** is thermal-capacitance related and is introduced for fitting the thermal behavior under AC operation. Furthermore, as the self-heating strongly depends on the width of the LDMOS/HVMOS device and on the number of used fingers **NF** in the layout, these effects have to be included in the compact modeling and result in the formulation of the HiSIM-HV equations for thermal resistance and thermal capacitance as

$$R_{\mathrm{th}} = \frac{\mathbf{RTH0}}{W_{\mathrm{eff}}} \cdot \left(\frac{1}{\mathbf{NF}^{\mathbf{RTH0NF}}} \right) \left(1 + \frac{\mathbf{RTH0W}}{(W_{\mathrm{gate}} \cdot 10^4)^{\mathbf{RTH0WP}}} \right) \tag{2.37}$$

$$C_{\mathrm{th}} = \mathbf{CTH0} \cdot W_{\mathrm{eff}} \tag{2.38}$$

An additional model parameter **RTH0R** is introduced as

$$R_{\mathrm{TH0W}} = \frac{\mathbf{RTH0R}}{\mathbf{TEMP}^3} \tag{2.39}$$

to improve the modeling of the thermal dissipation.

The HiSIM-HV model parameters introduced in Section 3.4 are summarized in Table 2.5.

Table 2.5 HiSIM-HV model parameters introduced in Section 3.4 of this chapter

RTH0	Thermal resistance
CTH0	Thermal capacitance
RTH0W	Width dependence of thermal resistance
RTH0WP	Width dependence of thermal resistance
RTH0NF	Number of finger dependence of thermal resistance
RTH0R	Thermal dissipation

4 Overview of the Parameter-Extraction Procedure

The parameter extraction has to cover the parameters specific for the MOSFET part, which is analogous to the bulk-MOSFET model HiSIM2, and the parameters specific for the high-voltage part of the LDMOS/HVMOS device. Model parameters categorized as group (1), i.e. conventional MOSFET related parameters, are extracted first and parameters characterized as group (2), i.e. LDMOS/HVMOS specific parameters, are extracted afterwards. In this section we discuss the main points of the HiSIM-HV parameter extraction and point out the differences in comparison to the normal MOSFET-parameter extraction.

4.1 Conventional MOSFET Part

In the bulk-MOSFET model HiSIM, device characteristics are strongly dependent on the basic device parameter values, such as the impurity concentration or the oxide thickness. Therefore, the parameter-value extraction has to be repeated with measured characteristics of different devices in a specific sequence until extracted parameter values reproduce all device characteristics consistently and reliably. To achieve reliable extraction results, it is recommended to start with initial parameter values according to the recommendations listed in the Table 2.6. Since some of the model parameters such as T_{ox} are difficult to extract unambiguously with the correct physical values, their determination is recommended directly by dedicated measurements of the MOSFET-device part. Threshold voltage measurements as a function of gate length allow the derivation of a rough extraction for the model parameters referred to as “basic device parameters”. The parameters identified with the symbol “*” in the model-parameter table are initially fixed to zero and only adjusted in the final stage of the extraction, if necessary.

The sequence of the MOSFET-channel-size selection for the parameter-extraction procedure is recommended in four steps:

1. Long-Channel Devices
2. Short-Channel Devices
3. Long-Narrow Devices
4. Short-Narrow Devices

Table 2.6 Recommendation for initial parameter settings at the beginning of the extraction procedure

Determined by dedicated measurements (not changed during extraction procedure)	Default values used (see [7]) initially for parameter groups listed below
TOX	Basic device parameters (not listed on left side)
	Gate leakage
	GIDL
	Source/bulk and drain/bulk diodes
	Noise
	Subthreshold swing
	Non-quasi-static model
	Overlap capacitances

Prior to the detailed extraction, a rough extraction with measured $V_{\text{th}} - L_{\text{gate}}$ characteristics is recommended to get a rough idea about the basic-parameter values. These basic parameters are usually important because they give a strong influence on the accuracy and physical correctness of the total parameter extraction. The parameter extraction procedure of the conventional MOSFET part is summarized in the following Table 2.7.

4.2 LDMOS/HVMOS Specific Part

The LDMOS/HVMOS specific model parameters (group (2) parameters) are extracted, as already mentioned, after the extraction of the intrinsic MOSFET-part parameters (group (1) parameters) of the high-voltage device. According to this recommended extraction procedure, namely to perform first group (1) and then group (2) parameters, the parameter extraction is done in the following sequence:

1. Rough extraction of the MOSFET parameters with measured $V_{\text{th}} - L_{\text{gate}}$
2. Fine extraction with measured subthreshold data for $I_{\text{ds}} - V_{\text{gs}}$
3. Extraction of mobility parameters with $I_{\text{ds}} - V_{\text{gs}}$ and $I_{\text{ds}} - V_{\text{ds}}$
4. Extraction of resistance parameters with $I_{\text{ds}} - V_{\text{gs}}$ and $I_{\text{ds}} - V_{\text{ds}}$
5. Fine extraction of resistance parameters with channel-conductance and transconductance
6. Capacitance extraction

Agreement of the extraction results with measurements after the 3rd step is normally not sufficient, especially in the high V_{gs} region and in the low V_{ds} region. The 4th step for resistance extraction is therefore focused on the measurement regions where the quasi-saturation effect of the LDMOS/HVMOS device becomes obvious. It is recommended to repeat the extraction steps from 3 to 5 because this repetition leads to better fitting results in most practical cases. The initial extraction steps 1 to 3 are basically the same as in the conventional extraction procedure for the bulk MOSFET.

Table 2.7 Summary of the seven steps of the parameter-extraction procedure for the bulk-MOSFET model HiSIM

Step 1: Initial preparation and rough extraction		
1-1.	Initialize all parameters to their default values	
1-2.	Use the measured gate-oxide thickness for TOX	TOX
1-3.	Rough extraction with $V_{\rm th}$-dependence on $L_{\rm gate}$ $[V_{\rm th} - V_{\rm gs}]$	**NSUBC**, **VFB**, **SC1**, **SC2** **SC3**, **NSUBP**, **LP**, **SCP1** **SCP2**, **SCP3** **NPEXT**, **LPEXT**
1-4.	Quantum and poly-depletion effects $[C_{\rm gg} - V_{\rm gs}]$	**QME1**, **QME2**, **QME3** **PGD1**, **PGD2**
Step 2: Extraction with long and wide transistors		
2-1.	Fitting of sub-threshold characteristics $[I_{\rm ds} - V_{\rm gs}]$	**NSUBC**, **VFB**, **MUECB0** **MUECB1**
2-2.	Determination of mobility parameters for low $V_{\rm ds}$ $[I_{\rm ds} - V_{\rm gs}]$	**MUEPH0**, **MUEPH1** **MUESR0**, **MUESR1**
2-3.	Determination of mobility parameters for high $V_{\rm ds}$ $[I_{\rm ds} - V_{\rm gs}]$	**NINVPH**, **NINVSR** **NDEP**
Step 3: Extraction with medium/short length and large width transistors		
3-1.	Pocket-parameter extraction with medium length transistors $[I_{\rm ds} - V_{\rm gs}]$	**NSUBP**, **LP** **SCP1**, **SCP2**, **SCP3** **NPEXT**, **LPEXT**
3-2.	Short-channel-parameter extraction with short-length transistors $[V_{\rm th} - L_{\rm gate}]$	**SC1**, **SC2**, **SC3** **PARL2**, **XLD**
3-3.	Mobility-parameter refinement for low $V_{\rm d}$ $[I_{\rm ds} - V_{\rm gs}]$	**MUEPHL**, **MUEPLP** **MUESRL**, **MUESLP**
3-4.	Velocity parameter extraction for high $V_{\rm d}$ $[I_{\rm ds} - V_{\rm gs}]$	**VMAX**, **VOVER**, **VOVERP**
3-5.	Parameters for channel-length modulation $[I_{\rm ds} - V_{\rm ds}]$	**CLM1**, **CLM2**, **CLM3**
3-6.	Source/drain resistances $[I_{\rm ds} - V_{\rm ds}]$	**RS**, **RD**, **RSH**, **NRS**, **NRD**
Step 4: Extraction of the width dependencies for long transistors		
4-1.	Fitting of sub-threshold width dependencies $[I_{\rm ds} - V_{\rm gs}]$	**NSUBC**, **NSUBCW**, **NSUBCWP** **WFC**, **XWD**, **WVTH0**
4-2.	Fitting of mobility width dependencies $[I_{\rm ds} - V_{\rm gs}]$	**MUEPHW**, **MUEPWP** **MUESRW**, **MUESWP**
Step 5: Extraction of the width dependencies for short transistors		
5-1.	Fitting of sub-threshold dependencies $[I_{\rm ds} - V_{\rm gs}]$	**NSUBP0**, **NSUBWP**
Step 6: Extraction of small-geometry effects		
6-1.	Effective channel-length corrections	**WL2**, **WL2P**
6-2.	Mobility and velocity $[I_{\rm ds} - V_{\rm ds}]$	**MUEPHS**, **MUEPSP** **VOVERS**, **VOVERSP**
Step 7: Extraction of temperature dependence with long-channel transistors		
7-1.	Sub-threshold dependencies $[I_{\rm ds} - V_{\rm gs}]$	**BGTMP1**, **BGTMP2** **EG0**
7-2.	Mobility and maximum carrier-velocity dependencies $[I_{\rm ds} - V_{\rm gs}]$	**MUETMP**, **VTMP**

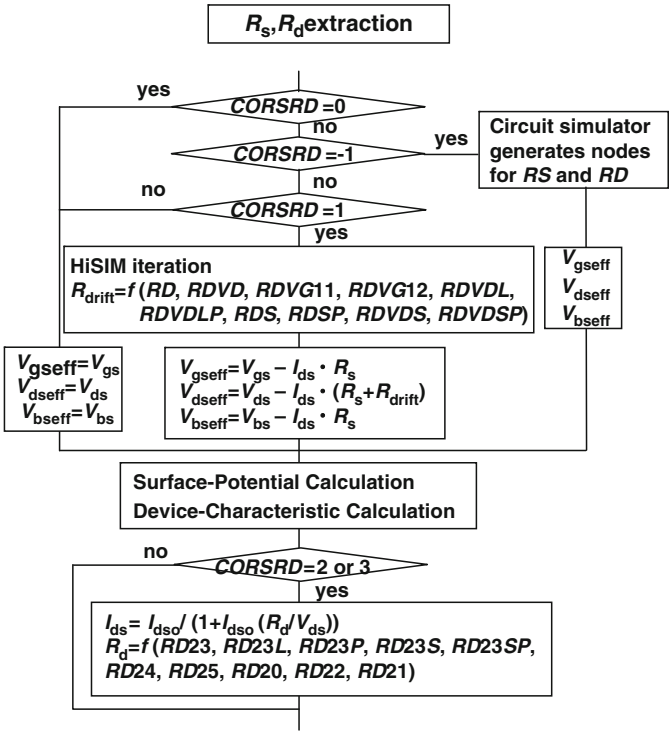

Fig. 2.11 Parameter extraction flow for resistance parameters of HiSIM-HV, which changes according to the resistance-model selection

The extraction of the resistance parameters is done according the selection of the resistance model as summarized in Fig. 2.11.

If the self-heating effect is activated, all device characteristics will normally change drastically. Retuning of model parameters is therefore required. The main affected model parameters, which need this retuning step, are related to the mobility and the resistance models. The temperature-dependent parameters are normally extracted without the self-heating effect from temperature-dependent measurements. It is usually not necessary to modify these initially extracted values of the temperature-dependent parameters after activating the self-heating effect.

5 Reproduction of High-Voltage MOSFET Characteristics

In this section the basic modeling capabilities of HiSIM-HV are demonstrated for the device characteristics, which newly appear in high-voltage MOSFETs and which are known to be difficult to capture by a compact model. Particularly, the anomalies in the capacitances of high-voltage MOSFETs, the quasi-saturation behavior in

the I-V characteristics, the scaling properties with drift-region doping and the scaling properties with drift-region length will be analyzed. Two-dimensional device-simulation results are used to analyze the newly occurring effects and to compare them to the compact-model results, thus verifying the correct modeling of these main high-voltage-MOSFET characteristics with HiSIM-HV.

5.1 Capacitances

The wide range of switching operations from a few volts to several hundred volts is realized in the high-voltage MOSFETs, as mentioned before, with a drift region of low-impurity concentration, which provides the required high-voltage-blocking capability. This has been observed to lead to anomalous characteristics for the capacitances of high-voltage MOSFETs, which become more pronounced with lower impurity concentrations of the drift regions. In particular, capacitance peaks appear in the C_{gg} capacitances as a function of V_{gs}. The effect is demonstrated by the 2-dimensional device simulations of Fig. 2.12 for the LDMOS structure, where the properties of C_{gg} change completely when the drift-region doping is reduced from 10^{17} to 10^{16}cm^{-3}. The experimentally often observed anomalous, V_{gs} -dependent capacitance peaks are seen to appear for the lower impurity concentration.

This anomalous capacitance effect has been modeled in previous approaches either by introducing an internal node at the channel/drift junction [16] or a resistance added as a sub-circuit in a macro model [17]. The former model solves the node potential iteratively until channel current and the current in the drift region at the node becomes equal. However, it is difficult to extract model parameters for both

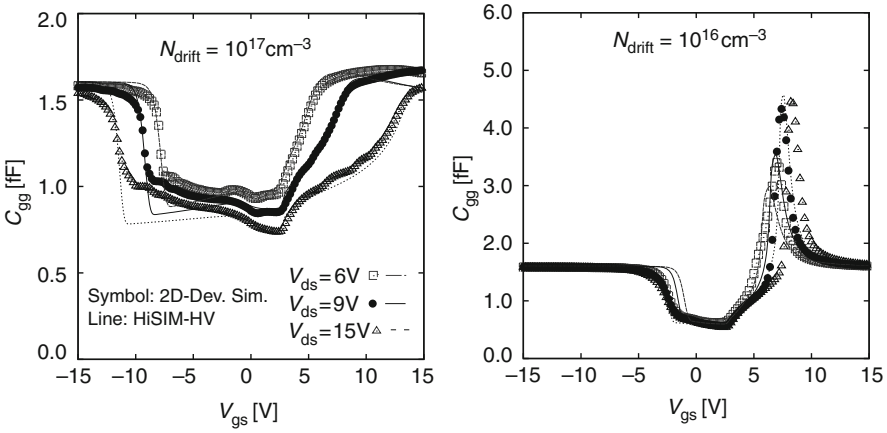

Fig. 2.12 Capacitance comparison between 2D-device simulation (*symbols*) and HiSIM-HV (*lines*) results for the LDMOS structure with different drift-region dopings of 10^{17}cm^{-3} (*left*) and 10^{16}cm^{-3} (*right*)

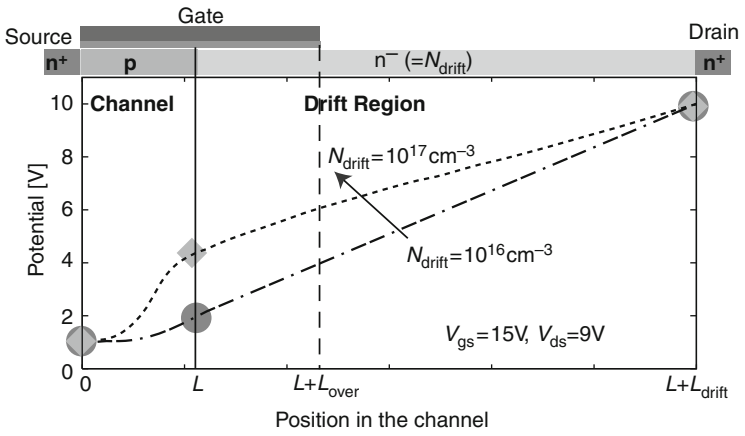

Fig. 2.13 Calculated potential distribution along the channel and the drift region of the LDMOS device with the developed HiSIM-HV model (shown with symbols) for two drift-region concentrations of 10^{17}cm^{-3} and 10^{16}cm^{-3}. Lines are 2-dimensional device simulation results

channel and drift regions with a single set of measured drain currents. The macro model description used in [17], is not valid for a sufficiently accurate modeling in the LDMOS case, because the internal node potential, which is determined by a balance between channel conductivity and the resistivity in the drift region, and which is responsible for all device features, cannot be correctly calculated.

On the other hand, HiSIM-HV consistently calculates the potential distribution along the channel and the drift region from the source to the drain contact. The changes in the potential distribution for different impurity concentrations in the drift region can therefore be accurately calculated, as demonstrated with the LDMOS structure in Fig. 2.13 for the drift-region-doping cases of 10^{17}cm^{-3} and 10^{16}cm^{-3}. Consequently, due to this accurate potential-distribution determination, HiSIM-HV is able to capture the scaling properties of the high-voltage MOSFET capacitances with respect to drift-region doping accurately, as verified by the lines in Fig. 2.12.

5.2 I-V Characteristics and Derivatives

Figure 2.14a,b,c shows a comparisons of $I - V$ and g_m characteristics for the LDMOS device structure and the two impurity concentrations 10^{17}cm^{-3} and 10^{16}cm^{-3} in the drift region, while keeping the length of the drift region and the other device parameters the same. Good agreement between the 2-dimensional device-simulation and HiSIM-HV results is again verified. Furthermore, the quasi-saturation effect can be clearly seen, in particular for the lower doping concentration, and is reproduced quantitatively.

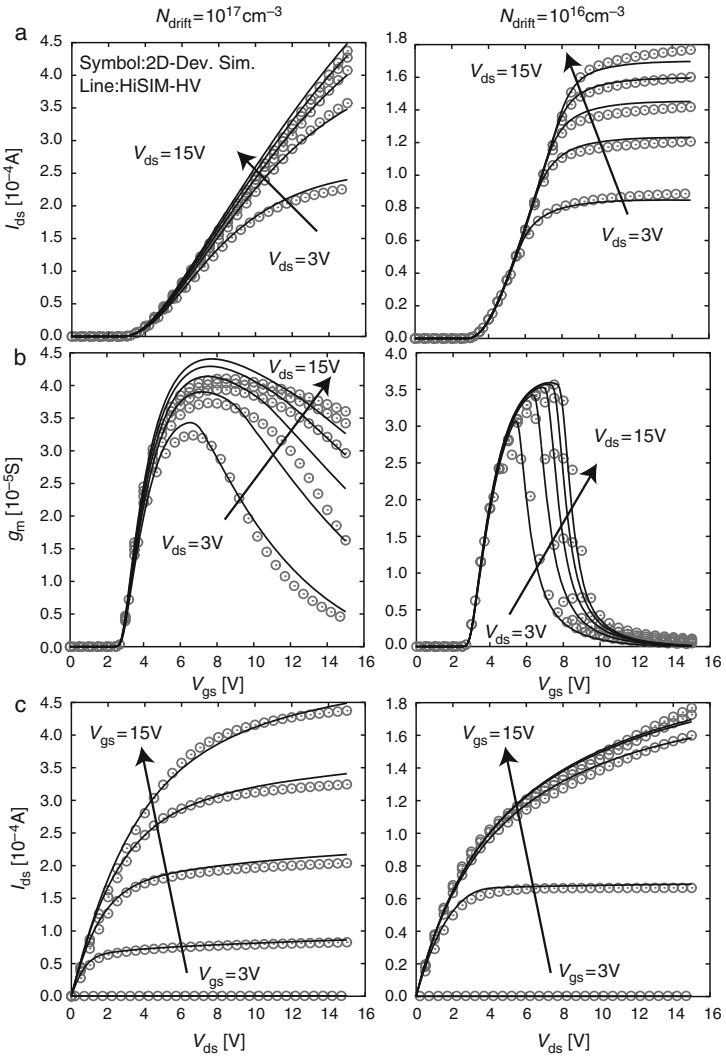

Fig. 2.14 Comparison of $I - V$ and g_m characteristics between 2-dimensional device simulator (*symbols*) and HiSIM-HV (*lines*) results for the LDMOS structure with different drift-region dopings of 10^{17} cm^{-3} (*left*) and 10^{16} cm^{-3} (*right*)

The corresponding C_{gg} characteristics has been compared in Fig. 2.12 of the previous section with for the two different drift-region doping values. As discussed, the anomalies observed as peaks in the V_{gs} dependence of C_{gg} for reduced drift-region doping are caused by the increased resistance effect in the drift region due to this lower impurity concentration. Figure 2.14b verifies that the drastic reduction of g_m as a function of V_{gs} coincides very well with these capacitance peaks.

5.3 Symmetric Versus Asymmetric Characteristics

Accurate surface-potential-dependent modeling of the overlap charge, Q_{over}, between the gate oxide and the drift region is already very important for the asymmetrical LDMOS structure. However, since substantial surface-potential-dependent overlap capacitances are located at source end as well as drain end for the symmetrical HVMOS-device structure, their contribution to the operational characteristics of the symmetrical devices becomes even more important.

For providing sufficient accuracy, the bias dependent surface potentials within the overlap regions consequently have to be considered in describing the formation of the accumulation, the depletion as well as the inversion condition underneath the gate overlap region, which now depend in a complicated way dynamically on the bias conditions.

These modeling tasks for the overlap region are achieved by solving the Poisson equation in the same way as in the channel. The overlap charges are determined in HiSIM-HV from the calculated surface-potential distribution under the simplifying approximation that the potential variation along the overlap region (see Section 3.1) is negligible. The surface-potential values are of course a function of the drift-region doping N_{drift}, which determines also the flat-band voltage within the overlap region. Calculated overlap capacitances with HiSIM-HV are shown in Fig. 2.15 as a function of V_{gs}.

Figure 2.16 compares the calculated capacitances for the asymmetrical LDMOS device and the symmetrical HVMOS device as obtained with HiSIM-HV and a 2-dimensional device simulator. It can be seen that the results agree well for both device structures. The shoulders in the overall capacitances originate from the overlap

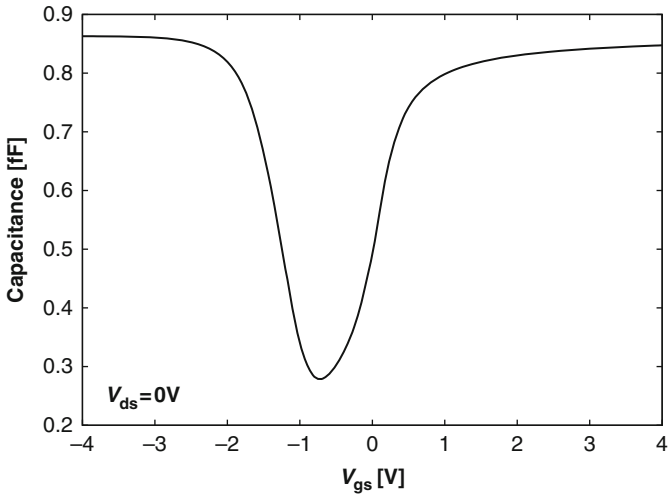

Fig. 2.15 Calculated overlap capacitance at the drain side with HiSIM-HV at $V_{\text{gs}} = 0\text{V}$

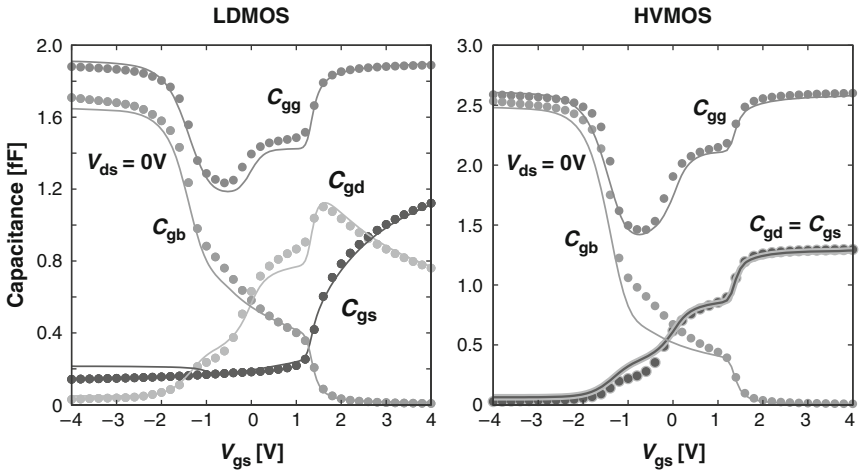

Fig. 2.16 Comparison of capacitances calculated for the asymmetrical LDMOS and symmetrical HVMOS structure with HiSIM-HV (*lines*) and a 2-dimensional device simulator (*symbols*). Again HiSIM-HV is verified to be in good agreement with the device-simulation results

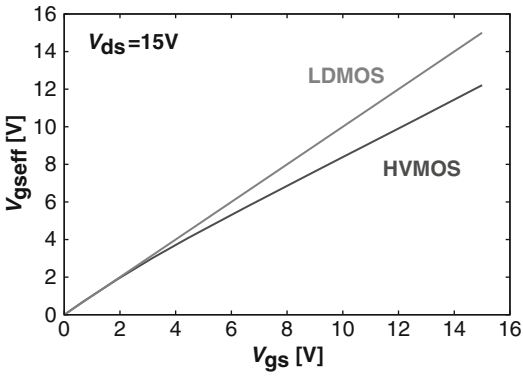

Fig. 2.17 Comparison of the effective gate-source voltage (V_{gseff}) as a function of the applied gate-source voltage (V_{gs}) for the symmetrical HVMOS and the asymmetrical LDMOS device structures

capacitances between the gate and the drift regions, which are non-negligible for high-voltage MOSFETs and have to be modeled under inclusion of their bias dependences.

For modeling of the symmetrical HVMOS device, the resistance model for the drift region, described in Section 3.2, has to be applied to the source side as well. Figure 2.17 shows the calculated potential drop within the drift region at the source end, causing a reduction of the effective gate-source potential of the MOSFET core from V_{gs} to V_{gseff}, which now furthermore depends in a dynamic way on bias conditions. This additional potential drop at the source end results of course also in a bias-dependent reduction of V_{ds} and V_{bs} as well. Therefore, the influence of the source resistance in the symmetric HVMOS device on the device characteristics can be expected to be very drastic.

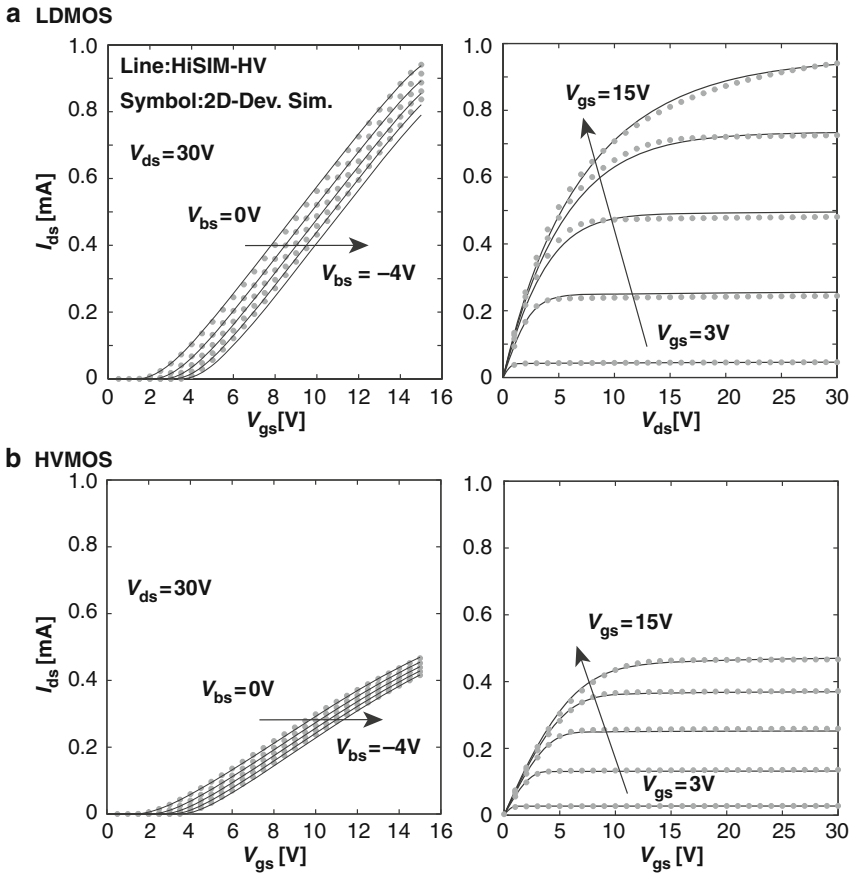

Fig. 2.18 Current comparison, (*left-hand side*) as a function of Vgs and (*right-hand side*) as a function of Vds, between LDMOS and HVMOS structures, respectively. Results from HiSIM-HV (*lines*) and 2-dimensional device simulation (*symbols*) are in very good agreement

Figure 2.18a,b compares the calculated I-V characteristics of HiSIM-HV for the asymmetrical LDMOS and the symmetrical HVMOS with 2-dimensional device-simulation results. The high resistance effect of the drift region causes a reduction of the potential increase in the channel, which also results in a drastic reduction of the drain current. This drain-current reduction is much more enhanced for the symmetrical HVMOS case due to the potential drop in the drift region at the source side. On the other hand the LDMOS device shows a more gradually increasing current due to the dynamic reduction of R_{drift} for an increased carrier concentration in the drift region. Thus, it is verified that all specific features of LDMOS and HVMOS devices can be well reproduced with the single model HiSIM-HV. This is an advantage obtained by the modeling based on the surface potential, which secures the consistency of the overall model description due to the consistent potential determination in the complete high-voltage MOSFET device.

5.4 Scaling Properties

As explained before, HiSIM-HV is constructed as a modular extension of the bulk-MOSFET model HiSIM2, which is fully scalable with respect to gate length L_g and gate width W_g, enabling the provision of a single global parameter set for the complete L_g-W_g space. Due to the modular extension concept, it becomes possible to preserve the L_g- as well as the W_g-scalability in HiSIM-HV and care is taken that this task is achieved. It turns out that the L_g-scalability can be achieved quite easily, without taking special measures in the modeling equations. However, the W_g-scalability is more difficult to achieve because the power dissipation increases drastically with larger W_g, while the thermal resistance and thermal capacitance properties change too. These power-dissipation effects under W_g-scaling are appropriately taken care of in the scaling properties of the self-heating model, so that accurate W_g-scaling of HiSIM-HV model is achieved.

Another desirable scaling property of a high-voltage MOSFET model is the correct scaling with respect to the drift-region parameters, in particular the drift-region doping N_{drift} and the drift-region length L_{drift}. The correct scaling properties of HiSIM-HV with respect to N_{drift} have already been demonstrated in Fig. 2.12 for the capacitances, in Fig. 2.13 for the potential distribution and in Fig. 2.14 for the $I-V$ characteristics.

Figure 2.19 verifies the scalability of HiSIM-HV with the drift-region length L_{drift} for the case of the $I-V$ characteristics as a function of the gate-source voltage V_{gs} with high and also low drain-source voltage V_{ds} biases.

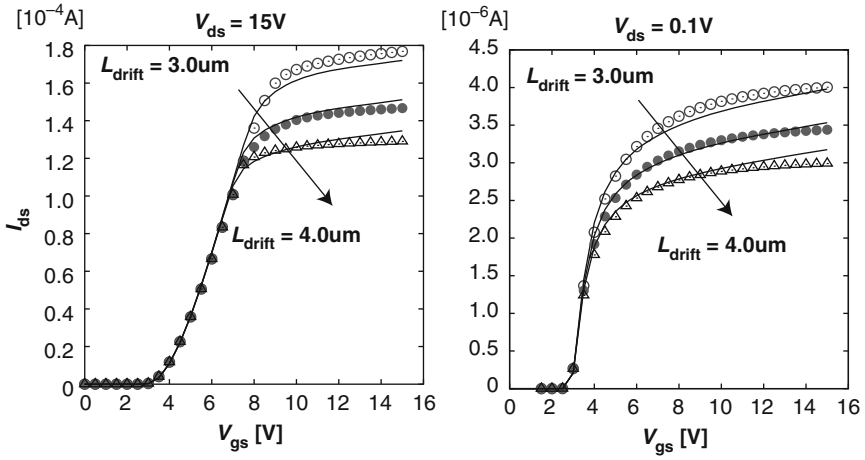

Fig. 2.19 Scalability of HiSIM-HV model with drift-region length L_{drift}. The plots compare the I_{ds}-V_{gs} characteristics at high and low drain bias for 2-dimensional device simulation (*symbols*) and HiSIM-HV (*lines*)

In fact HiSIM-HV is the only available high-voltage MOSFET model, which features the full scalability with MOSFET-core parameters and drift-region parameters, therefore being able to provide single global parameter set for high-voltage MOSFETs fabricated in a given technology.

6 Conclusion

The compact model HiSIM-HV for high-voltage MOSFETs, whose main features are described in this chapter, is based on the determination of the surface-potential distribution in the MOSFET core and the consistent potential extension to the drift region. Consequently, HiSIM-HV can accurately calculate the potential distribution in the entire asymmetric LDMOS structure or the symmetric HVMOS structure and determine all electrical and thermal high-voltage MOSFET properties without relying on any form of macro- or sub-circuit formulation. Furthermore, this consistent potential-based approach enables HiSIM-HV to reproduce all structure-dependent scaling properties of high-voltage MOSFET features with a single global parameter set.

The full scaling properties of HiSIM-HV with respect to the MOSFET-core geometry parameters L_g and W_g as well as the drift-region parameters L_{drift} and N_{drift} is unique among the compact high-voltage MOSFET models available today. As a result, HiSIM-HV has been selected by the Compact Model Council (CMC) [3] as the international compact-model standard for high-voltage-MOSFET devices. Continuously improved versions of the HiSIM-HV standard are released 2 times per year through the CMC.

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Chapter 3
MM20 HVMOS Model: A Surface-Potential-Based LDMOS Model for Circuit Simulation

Annemarie C.T. Aarts and Alireza Tajic

Abstract MOS Model 20 is an advanced public-domain compact LDMOS model, to be used for circuit simulation of high-voltage IC-designs. By combining the description of the MOSFET channel region with that for the drift region of an LDMOS device, MOS Model 20 includes all specific high-voltage aspects into one model. This chapter presents the physical background of the model, the model parameter extraction strategy, and ends with the verification in comparison to dc- and ac-measurements.

Keywords Compact model · LDMOS · Surface potential · High-voltage · IC-design

1 Introduction

For the design of Integrated Circuits (ICs) compact models are essential, since they enable the prediction of the electrical behaviour of the transistors used. In this way, compact models enhance the productivity of ICs, and they reduce the cycle time during the design process. In many IC-designs dedicated high-voltage devices are used, like, for instance, Laterally Double-Diffused MOS (LDMOS) devices. These LDMOS devices are processed in both bulk- and Silicon-on-Insulator (SOI) technology [34]. The major characteristic of an LDMOS device is the existence of a (diffused) MOSFET channel region in combination with a drift region to withstand the high voltages applied; see Figs. 3.1 and 3.2. For optimal high-voltage IC-design compact LDMOS models are thus needed, which describe the electrical behaviour accurately over a wide range of bias conditions.

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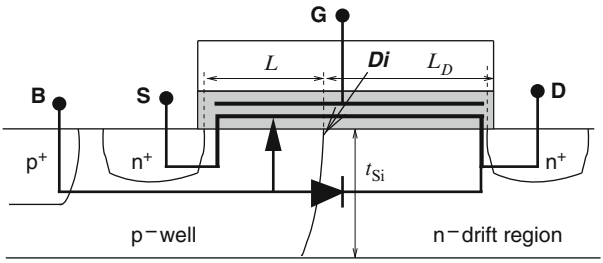

Fig. 3.1 A low-voltage LDMOS device with a MOSFET channel region and a short drift region completely covered by the gate and its thin-gate oxide. The device is described by MOS Model 20 and an additional diode for the pn-junction between drain and bulk terminal

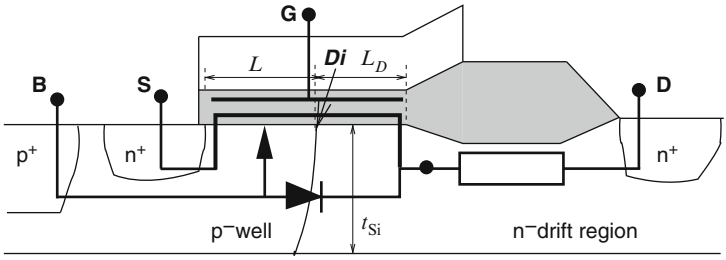

Fig. 3.2 A high-voltage LDMOS device with a MOSFET channel region and a long drift region, covered partly by the gate and its thin-gate oxide, and partly by the thick-field oxide. The device is described by MOS Model 20 in series with an additional resistor and a diode

A frequently followed approach in high-voltage modeling is to describe the LDMOS device by a sub-circuit, in which the channel region is described by a compact MOS model and the drift region by either a resistor or a dedicated drift region model; see [3, 10, 11, 13, 16, 17, 19, 25, 30, 31, 36, 37]. In the sub-circuit approach the circuit simulator thus solves the potential at the internal drain between the channel region and the drift region. The disadvantage of a sub-circuit is that the voltage at the internal drain can not be controlled, so that during circuit simulation the model may have difficulty to converge, or that simulation time increases due to the extra circuit node. The advantage, on the other hand, is the flexibility to cover a broad range of different high-voltage device structures. In the sub-circuit model of [30], however, only a linear resistance is taken for the drift-region model, while in [10,16,17,19,31] an empirical, non-physical relation is taken for the bias-dependent drift-region resistance. In the models of [11, 25] velocity saturation in the drift region (leading to quasi-saturation [14]) is taken into account, but not the effect of accumulation due to the gate extending over the drift region.

Another approach in high-voltage modeling is one model for the channel and drift region together, so that the potential at the internal drain is determined inside the model, either by means of a numerical iteration procedure [12,18,21], or through

an analytical, explicit expression for this potential [15, 24]. In order to be able to determine the potential analytically, in an explicit form, simplifications to the current descriptions are needed. Therefore, a numerical iteration procedure enables the use of extensive and sophisticated current expressions, but care should be taken that the iteration procedure is always converging. What is lacking in the models of [12, 18, 21] is the sub-threshold regime, while in [24] no terminal charge model is present from which the capacitances can be determined. The model of [15] has been found to be limited due to poor convergence during circuit simulation.

To account for the specific high-voltage characteristics inside one compact model, a dedicated LDMOS compact model, called MOS Model 20 (MM20), has been developed. This model combines the MOSFET channel region under the thin gate oxide with the drift region of an LDMOS device. Thus, all main characteristics of an LDMOS device, like the effect of the gate extending over the drift region as well as quasi-saturation, are covered inside the model. For accuracy purposes, MOS Model 20 has been developed in terms of surface potential formulations, and the internal drain potential is solved numerically inside the model.

The use of MOS Model 20 in circuit design is as follows: LDMOS devices with a short drift region, i.e. LDMOS devices for relatively low supply-voltages (in the range of approximately 12–24 V), can be described by MOS Model 20 without any additional drift region model; see Fig. 3.1. For LDMOS devices with an intermediately long drift region, i.e. for medium supply-voltages (in the range of approximately 24–100 V), MOS Model 20 can be used in series with a simple resistor; see Fig. 3.2. In LDMOS devices with a very long drift region, i.e. for extremely high supply-voltages (in the range of approximately 100–1000 V), the influence of the voltage applied at the bulk becomes significant, and MOS Model 20 can be used in series with a dedicated drift region model, like, for instance, MOS Model 31 for junction-isolated devices, or MOS Model 40 for SOI-LDMOS; cf. [3, 4]. Thus, MOS Model 20 serves as the basis building block for all kind of LDMOS devices, for a wide range of supply-voltages. It should be noted that MOS Model 20 can also be used for high-voltage devices that have no diffused doping profile in the channel region.

In this chapter MOS Model 20 is presented, and a comparison to measurements is given for both a low-voltage (14 V) and a high-voltage (60 V) LDMOS device. At present two versions have been released: one with level number 2001, and the latest version with level number 2002. The major difference between the two versions is that in level number 2002 the effect of saturation in the drift region (quasi-saturation) as well as avalanche occurring in the drift region have been added, two phenomena which are lacking in the first version (with level number 2001). Notice that the first version of MOS Model 20 has been presented in [1, 6], whereas in [2] the effect of quasi-saturation on the dc-current has been described. In this book, a complete overview of the latest version of the model is given, including its derivation from the physics, and the comparison to measurements. Finally, we mention that the source code as well as the full documentation including the parameter extraction strategy of MOS Model 20 is available in the public domain [4].

1.1 Model Structure

In MOS Model 20, the currents through the device consist of the dc-current I_{DS} from drain to source, and the charging currents at the drain, gate, source and bulk terminal. Hence, the total current into each terminal is given by

$$I_D = I_{DS} + I_{DB} + \frac{dQ_D}{dt}, \quad I_G = \frac{dQ_G}{dt},$$
$$I_S = -I_{DS} + \frac{dQ_S}{dt}, \quad I_B = -I_{DB} + \frac{dQ_B}{dt}, \tag{3.1}$$

where I_{DS} is the dc-current due to drift and diffusion, I_{DB} is the dc-current due to avalanche, and Q_D, Q_G, Q_S and Q_B are the terminal charges at the terminals. We have neglected gate leakage currents, which, if necessary, could easily be added according to [22]. From the dc-currents the conductances are determined according to

$$g_{DS} = \frac{\partial (I_{DS} + I_{DB})}{\partial V_D}, \quad g_m = \frac{\partial (I_{DS} + I_{DB})}{\partial V_G}, \quad g_{mb} = \frac{\partial (I_{DS} + I_{DB})}{\partial V_B}, \tag{3.2}$$

while from the terminal charges the capacitances are determined according to

$$C_{ij} = (2\delta_{ij} - 1)\frac{\partial Q_i}{\partial V_j}, \quad i, j = D, G, S, B, \tag{3.3}$$

where δ_{ij} is the Kronecker delta, equal to 1 if $i = j$ and equal to 0 if $i \neq j$. Recently, it has been found that for laterally non-uniform devices, like an LDMOS device is, no terminal drain- and source charge exists from which the corresponding drain- and source related capacitances can be determined [5]. Only for the gate- and bulk related capacitances it has been demonstrated that a terminal gate and bulk charge exist from which the corresponding capacitances can be determined. A similar result has been found for a conventional MOSFET in saturation [28], for which in [7] a capacitance model has been derived. For practical reasons, however, MOS Model 20 is equipped with a carefully tuned terminal charge model from which the capacitances are derived according to (3.3). In Section 3 we show that with our approach the measured capacitances can accurately be modeled over a wide range of bias conditions.

Finally, MOS Model 20 is equipped with a noise model. This noise model consists of 1/f noise, thermal noise, and gate induced noise. For an overview of the noise model we refer to [4].

2 The Model

To derive the dc- and charging currents through the LDMOS device, the following model methodology is used in MOS Model 20. First the device is considered in two parts: the channel region and the drift region, with the internal drain Di representing

the point of where the two regions meet, see Figs. 3.1 and 3.2. Next, the current I_{ch} through the channel region is determined, in terms of the external gate, source, and bulk potential V_G, V_S and V_B, and the internal drain potential V_{Di}. For the drift region, the current I_{dr} is determined in terms of the external gate, drain, and bulk potential V_G, V_D and V_B, and the internal drain potential V_{Di}. By equating the channel region current I_{ch} to the drift region current I_{dr}, the internal potential V_{Di} is solved inside the model. The solution of this potential is obtained through a numerical iteration procedure. As the current difference $I_{ch} - I_{dr}$ is a monotonically increasing function of the internal drain potential with exactly one zero, the standard Newton–Raphson scheme can be used combined with a bisection procedure to speed up the iteration process and to ensure that the internal drain potential remains between the source and drain potential. In this way, a robust and fast computation of the internal drain potential is obtained. This internal potential is subsequently used to determine the surface-potentials of the channel region and drift region, to set both the dc-currents I_{DS} and I_{avl} as well as the terminal charges Q_D, Q_G, Q_S, Q_B.

The equations derived in this section are for an n-channel device. Of course, MOS Model 20 also contains a p-channel device option. It should be noticed that MOS Model 20 can also be used if the pn-junction between bulk- and drain terminal is biased in the forward operation (i.e. for negative drain–source voltages in case of an n-channel device).

2.1 Model for DC-Currents

To obtain an accurate description of the dc-currents, a charge-sheet MOS model approach based on surface potentials is taken, for both the channel and drift region. To that end, the surface potential ψ_s in the channel region and the surface potential ψ_s^{dr} in the drift region are determined in terms of the quasi-Fermi potentials, which are known at the terminals of the device.

In the channel region, the surface potential ψ_s with respect to the bulk satisfies the implicit equation obtained from Poisson's equation and Gauss' law, according to (see [22, 26])

$$\begin{aligned}\left(\frac{V_{GB}^{*}-\psi_s}{k}\right)^2 &= \psi_s + \phi_T\left(\exp\left[-\frac{\psi_s}{\phi_T}\right]-1\right)\\ &\quad+\phi_T\exp\left[-\frac{\phi_B+V_{CB}}{\phi_T}\right]\left(\exp\left[\frac{\psi_s}{\phi_T}\right]-\frac{\psi_s}{\phi_T}-1\right),\end{aligned} \tag{3.4}$$

where $V_{GB}^{*} = V_{GB} - V_{FB}$ is the effective gate-bulk bias with V_{FB} the flatband voltage, V_{CB} ($V_S \le V_C \le V_{Di}$) is the quasi-Fermi potential, and $k = \sqrt{2q\epsilon_{Si}N_A}/C_{ox}$ is the body factor, with $C_{ox} = \epsilon_{ox}/t_{ox}$ the gate oxide capacitance per unit area, t_{ox} the oxide thickness, q the electronic charge, ϵ_{Si} the permittivity of silicon, ϵ_{ox} that of oxide, and N_A the p-well doping concentration. The potential $\phi_B = 2\phi_F$ is taken as model parameter, where the Fermi-potential ϕ_F of the channel is given by

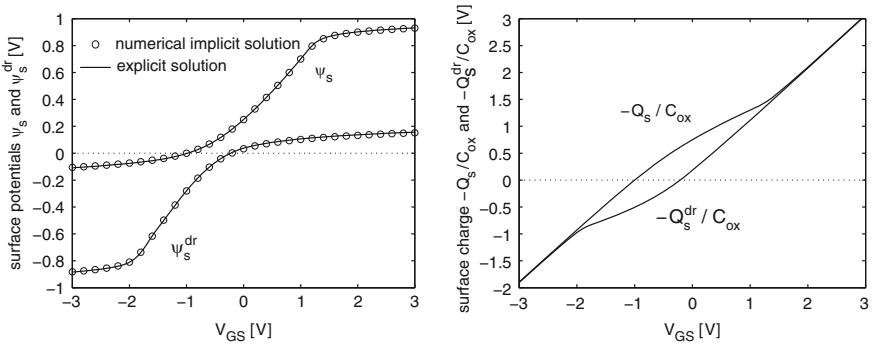

Fig. 3.3 The surface potentials ψ_s and ψ_s^{dr}, and the corresponding surface charge densities Q_s and Q_s^{dr}, for $V_{SB} = V_{CS} = 0V$, for channel region parameters $V_{FB} = -1.0V$, $\phi_B = 0.81V$, $k = 1.58V^{1/2}$, and drift region parameters $V_{FB}^{dr} = -0.21V$, $\phi_B^{dr} = 0.76V$ and $k^{dr} = 1.0V^{1/2}$. Solutions are obtained by a numerical iteration procedure for Eqs. 3.4 and 3.10 (*symbols*), and the approximation (*solid lines*) according to Eq. 3.17 (see [35]) as used in MOS Model 20

$\phi_F = \phi_T \ln(N_A/n_i)$, with n_i the intrinsic carrier concentration of silicon and ϕ_T the thermal voltage. The first term in the right-hand side of (3.4) accounts for depletion (due to the channel region doping N_A), the second term is due to accumulation (holes), while the third term is due to strong inversion (electrons). In Fig. 3.3 the surface potential ψ_s, obtained by solving (3.4) by means of a numerical iteration procedure, is plotted versus the gate voltage.

In the channel region the surface charge Q_s per unit area is given by

$$Q_s = -C_{ox}\left(V_{GB}^* - \psi_s\right), \tag{3.5}$$

which we write as

$$Q_s = Q_{inv} + Q_{dep} + Q_{acc} = -C_{ox}\left(V_{inv} - V_{dep} - V_{acc}\right), \tag{3.6}$$

to distinguish between the occurrence of accumulation, depletion, and (strong) inversion. In case $V_{GB}^* < 0$, accumulation occurs, and the surface charge Q_s is equal to the (positive) accumulation charge $Q_{acc} = C_{ox}V_{acc}$. In case $V_{GB}^* > 0$, depletion and inversion occurs, and the surface charge Q_s is equal to $Q_{dep} + Q_{inv}$, with the (negative) depletion charge Q_{dep} given by

$$Q_{dep} = -C_{ox}V_{dep} = -C_{ox}\,k\,\sqrt{\psi_s}, \tag{3.7}$$

and the (negative) strong inversion charge Q_{inv} given by

$$Q_{inv} = Q_s - Q_{dep} = -C_{ox}V_{inv} = -C_{ox}\left(V_{GB}^* - \psi_s - k\sqrt{\psi_s}\right). \tag{3.8}$$

Notice that in case only depletion occurs (so no strong inversion), the depletion charge, in terms of $V_{\rm dep}$, satisfies

$$V_{\rm dep} = k\left(-\frac{k}{2} + \sqrt{\left(\frac{k}{2}\right)^2 + V_{\rm GB}^*}\right), \tag{3.9}$$

in which the right-hand side of (3.9) is equal to $k\sqrt{-\psi_{\rm s}}$. In strong inversion the surface potential $\psi_{\rm s}$ is approximately equal to $V_{\rm CB} + \phi_{\rm B}$. Hence, strong inversion occurs if approximately $V_{\rm GB} > V_{\rm FB} + \phi_{\rm B} + V_{\rm CB} + k\sqrt{\phi_{\rm B} + V_{\rm CB}}$; cf. Fig. 3.3.

In the drift region, the surface potential $\psi_{\rm s}^{\rm dr}$ with respect to the channel of that drift region satisfies the implicit equation obtained from Poisson's equation and Gauss' law, according to (see [33])

$$\begin{aligned}\left(\frac{V_{\rm GC}^{*\rm dr} - \psi_{\rm s}^{\rm dr}}{k^{\rm dr}}\right)^2 &= -\psi_{\rm s}^{\rm dr} + \phi_{\rm T}\left(\exp\left[\frac{\psi_{\rm s}^{\rm dr}}{\phi_{\rm T}}\right] - 1\right) \\ &\quad + \phi_{\rm T}\exp\left[-\frac{\phi_{\rm B}^{\rm dr} + V_{\rm CB}}{\phi_{\rm T}}\right]\left(\exp\left[-\frac{\psi_{\rm s}^{\rm dr}}{\phi_{\rm T}}\right] - 1\right),\end{aligned} \tag{3.10}$$

where $V_{\rm GC}^{*\rm dr} = V_{\rm GC} - V_{\rm FB}^{\rm dr}$ is the effective gate-channel bias of the drift region, with $V_{\rm FB}^{\rm dr}$ the flatband voltage of the drift region, $V_{\rm CB}$ ($V_{\rm Di} \le V_{\rm C} \le V_{\rm D}$) is the quasi-Fermi potential, and $k^{\rm dr} = \sqrt{2q\epsilon_{\rm Si}N_{\rm D}}/C_{\rm ox}$ is the body factor, with $N_{\rm D}$ the drift region doping concentration. The potential $\phi_{\rm B}^{\rm dr} = -2\phi_{\rm F}^{\rm dr}$ is taken as model parameter, where the Fermi-potential $\phi_{\rm F}^{\rm dr}$ of the drift region is given by $\phi_{\rm F}^{\rm dr} = -\phi_{\rm T}\ln(N_{\rm D}/n_{\rm i})$. The first term in the right-hand side of (3.10) accounts for depletion (due to the drift region doping $N_{\rm D}$), the second term is due to accumulation (electrons), while the third term is due to strong inversion (holes) coming from the p-well of the device. Notice that in case of depletion and strong inversion (i.e. for $V_{\rm GC}^{*\rm dr} < 0$), the surface potential $\psi_{\rm s}^{\rm dr}$ is negative; see Fig. 3.3. In this figure the surface potential $\psi_{\rm s}^{\rm dr}$, obtained by solving (3.10) by means of a numerical iteration procedure, is plotted versus the gate voltage.

In the drift region the surface charge $Q_{\rm s}^{\rm dr}$ per unit area is given by

$$Q_{\rm s}^{\rm dr} = -C_{\rm ox}\left(V_{\rm GC}^{*\rm dr} - \psi_{\rm s}^{\rm dr}\right), \tag{3.11}$$

which we write as

$$Q_{\rm s}^{\rm dr} = Q_{\rm acc} + Q_{\rm dep} + Q_{\rm inv} = -C_{\rm ox}\left(V_{\rm acc} - V_{\rm dep} - V_{\rm inv}\right), \tag{3.12}$$

to distinguish between the occurrence of accumulation, depletion, and (strong) inversion. In case $V_{\rm GC}^{*\rm dr} > 0$, accumulation occurs, and the surface charge $Q_{\rm s}^{\rm dr}$ is equal to the accumulation charge $Q_{\rm acc}^{\rm dr}$. Since in that case the surface potential is small (see Fig. 3.3), the accumulation charge can be approximated by

$$Q_{\rm acc}^{\rm dr} = -C_{\rm ox}V_{\rm acc}^{\rm dr} \approx -C_{\rm ox}V_{\rm GC}^{*\rm dr}. \tag{3.13}$$

In case $V_{GC}^{*dr} < 0$, depletion and strong inversion occur, and the surface charge Q_s^{dr} equals $Q_{dep}^{dr} + Q_{inv}^{dr}$, with the (positive) depletion charge Q_{dep}^{dr} given by

$$Q_{dep}^{dr} = C_{ox} V_{dep}^{dr} = C_{ox}\, k^{dr} \sqrt{-\psi_s^{dr}}, \tag{3.14}$$

and the (positive) inversion charge Q_{inv}^{dr} given by

$$Q_{inv}^{dr} = Q_s^{dr} - Q_{dep}^{dr} = C_{ox} V_{inv}^{dr} = C_{ox} \left(-V_{GC}^{*dr} + \psi_s^{dr} - k^{dr} \sqrt{-\psi_s^{dr}} \right). \tag{3.15}$$

In this case, the surface potential ψ_s^{dr} is negative; see Fig. 3.3. Notice that if only depletion occurs (so no strong inversion), then the depletion charge, in terms of V_{dep}^{dr}, satisfies

$$V_{dep}^{dr} = k^{dr} \left(-\frac{k^{dr}}{2} + \sqrt{\left(\frac{k^{dr}}{2} \right)^2 - V_{GC}^{*dr}} \right), \tag{3.16}$$

in which the right-hand side of (3.16) is equal to $k^{dr}\sqrt{-\psi_s^{dr}}$. In strong inversion the surface potential ψ_s^{dr} is approximately equal to $-(V_{CB} + \phi_B^{dr})$, hence it occurs if approximately $V_{GS} < V_{FB}^{dr} - \phi_B^{dr} - V_{CB} - k^{dr}\sqrt{\phi_B^{dr} + V_{CB}}$; cf. Fig. 3.3. For an LDMOS device, strong inversion in the drift region only occurs in case the device is switched off, for sufficiently low gate voltages. Notice that in case of strong inversion in either the channel region or the drift region the relation $\psi_s = \psi_s^{dr} + V_{CB} + V_{FB}^{dr} - V_{FB}$ holds between the surface potentials; cf. Fig. 3.3. In that case, the surface charge per unit area in the drift region and in the channel region are equal.

In order to reduce computation time for solving Eqs. 3.4 and 3.10, the explicit yet accurate relation between the surface potential and the terminal voltages according to [35] is used. By use of this relation, we write the surface potential ψ_s of the channel region, and ψ_s^{dr} of the drift region as

$$\psi_s = \Psi\left[V_{CB} + \phi_B, V_{GB}^*; k\right], \quad \psi_s^{dr} = -\Psi\left[V_{CB} + \phi_B^{dr}, -V_{GC}^{*dr}; k^{dr}\right], \tag{3.17}$$

where Ψ denotes the relation according to [35]. Notice that this relation is valid in all regimes ranging from accumulation to weak- and strong inversion. In Fig. 3.3 the comparison is shown between the solutions obtained from solving (3.4) and (3.10) by a numerical iteration procedure, as well as the explicit relations (3.17) from [35]. We observe that the explicit relations (3.17) yield a very accurate approximation of the numerical solutions of (3.4) and (3.10).

Due to the p-diffusion from the source side the doping concentration N_A, and thus the body factor k, decreases towards the end of the channel region. Hence, in contrast to a uniform MOS, the surface potential of an LDMOS device depends on the position along the channel, not only via the quasi-Fermi potential but also via the body factor k. With the body factor at the source denoted by k_0, an LDMOS device is thus switched on if the threshold voltage of the channel region at the source side is

reached, i.e. if approximately $V_{GS} > V_{TO} = V_{FB} + \phi_B + k_0\sqrt{\phi_B}$. In MOS Model 20 we take for simplicity an effective body factor k_0 along the whole channel region. Hence, we write the surface potential at the source as $\psi_{s_0} = \Psi\left[V_{SB} + \phi_B, V^*_{GB}; k_0\right]$, and the surface potential at the internal drain as $\psi_{s_L} = \Psi\left[V_{DiB} + \phi_B, V^*_{GB}; k_0\right]$. Notice that the surface potential ψ_{s_L} thus depends on the internal quasi-Fermi potential V_{Di}, which we determine by equating I_{ch} to I_{dr}. Once this internal drain potential is determined, the surface potentials in the drift region are computed according to $\psi^{dr}_{s_{Di}} = -\Psi\left[V_{DiB} + \phi^{dr}_B, -V^{*dr}_{GDi}; k^{dr}\right]$, and $\psi^{dr}_{s_D} = -\Psi\left[V_{DB} + \phi^{dr}_B, -V^{*dr}_{GD}; k^{dr}\right]$.

2.1.1 Channel Current

The channel current is given by

$$I_{ch} = W\mu_{ch}\left((-Q_{inv})\frac{d\psi_s}{dx} + \phi_T\frac{dQ_{inv}}{dx}\right), \tag{3.18}$$

where W is the device width, μ_{ch} the electron mobility, and Q_{inv} is the strong inversion charge per unit area, given by (3.8). Integration of (3.18) from source $x = 0$ to internal drain $x = L$ (cf. Fig. 3.1) yields

$$I_{ch} = \frac{W\mu_{ch}C_{ox}}{L}\left(\int_{\psi_{s_0}}^{\psi_{s_L}} V_{inv}d\psi_s + \phi_T\left(V_{inv_0} - V_{inv_L}\right)\right), \tag{3.19}$$

in which μ_{ch} is assumed to be independent of the channel potential V_C. Here, V_{inv_0} and V_{inv_L} represent the strong inversion charge at the source and internal drain, respectively. We linearize the inversion charge according to

$$V_{inv} = V_{inv_0} - \xi\left(\psi_s - \psi_{s_0}\right), \tag{3.20}$$

in which $\xi = -dV_{inv}/d\psi_s$ is taken as $\xi = 1 + \frac{1}{2}k_0/\sqrt{V_1 + \psi_{s_0}}$ with V_1 set to 1V. Substitution of (3.20) into (3.19) yields

$$I_{ch} = \frac{W\mu_{ch}C_{ox}}{L}\left(V_{inv_0} - \frac{1}{2}\xi\Delta\psi_s + \xi\phi_T\right)\Delta\psi_s, \tag{3.21}$$

where $\Delta\psi_s = \psi_{s_L} - \psi_{s_0}$ is the potential drop across the channel.

Mobility reduction due to the horizontal and vertical electrical fields in the channel are accounted for by taking the mobility μ_{ch} as

$$\mu_{ch} = \frac{\mu_{eff}}{1 + \frac{\mu_{eff}}{Lv_{sat}}\Delta\psi_s}, \tag{3.22}$$

with μ_{eff} representing the effective electron mobility, and v_{sat} the saturated drift velocity of electrons; cf. [32, p. 283]. The effective electron mobility depends on the effective vertical electrical field E_{eff} according to (see [32, p. 185])

$$\mu_{\text{eff}} = \frac{\mu_0}{F_{\text{mob}}}, \qquad F_{\text{mob}} = 1 + a_\theta \, E_{\text{eff}}, \qquad E_{\text{eff}} = -\frac{\eta Q_{\text{inv}} + Q_{\text{dep}}}{\epsilon_{\text{Si}}}, \tag{3.23}$$

where a_θ and η are constants, with η ideally equal to $\frac{1}{2}$ for electrons [29] and $\frac{1}{3}$ for holes [9]. In MOS Model 20, the effective electrical field is taken equal to the one at the source side. For ease of parameter extraction, we next replace the depletion charge Q_{dep_0} at the source by $Q_{\text{dep}_0} - Q_{\text{dep}_0}|_{V_{\text{SB}}=0}$, and obtain

$$F_{\text{mob}} = 1 + \theta_1 V_{\text{inv}_0} + \theta_2 \left(\sqrt{\psi_{\text{s}_0}} - \sqrt{\psi_{\text{s}_0}|_{V_{\text{SB}}=0}} \right), \tag{3.24}$$

where $\theta_1 = \eta a_\theta C_{\text{ox}}/\epsilon_{\text{Si}}$ and $\theta_2 = a_\theta k_0 C_{\text{ox}}/\epsilon_{\text{Si}}$ are model parameters. In this way, we decouple the effect due to a back bias, so that θ_2 can easily be extracted from measurements for $V_{\text{SB}} > 0$. Finally, by replacing $\mu_{\text{eff}}/(L v_{\text{sat}})$ by $\mu_0/(L v_{\text{sat}})$ in the denominator of (3.22), and substituting (3.23) into the result, we obtain for the channel mobility

$$\mu_{\text{ch}} = \frac{\mu_0}{F_{\text{mob}} \, (1 + \theta_3 \ \Delta\psi_{\text{s}})}, \tag{3.25}$$

where $\theta_3 = \mu_0/(L v_{\text{sat}})$ is a model parameter. Substitution of (3.25) into (3.21) yields for the channel region current

$$I_{\text{ch}} = \beta \, \frac{\left(V_{\text{inv}_0} - \frac{1}{2}\xi \Delta\psi_{\text{s}} + \xi \phi_{\text{T}} \right) \Delta\psi_{\text{s}}}{F_{\text{mob}} \, (1 + \theta_3 \ \Delta\psi_{\text{s}})}, \tag{3.26}$$

where $\beta = W\mu_0 C_{\text{ox}}/L$ is taken as model parameter. Thus, the channel region current is expressed in terms of the internal drain potential V_{DiS} through its relation (3.17) with the surface potential ψ_{s_L}. In strong inversion the potential drop $\Delta\psi_{\text{s}}$ approximately equals V_{DiS}.

In case of saturation in the channel region, the potential drop $V_{\text{DiS}} = V_{\text{DiS,sat}}$ is determined from $\partial I_{\text{ch}}/\partial \Delta\psi_{\text{s}}|_{\Delta\psi_{\text{s}}=V_{\text{DiS,sat}}} = 0$. By use of (3.26) we obtain

$$V_{\text{DiS,sat}} = \frac{2\left(V_{\text{inv}_0}/\xi + \phi_T\right)}{1 + \sqrt{1 + 2\theta_3 \left(V_{\text{inv}_0}/\xi + \phi_T\right)}}. \tag{3.27}$$

Hence, in solving the internal potential V_{Di} from $I_{\text{ch}} = I_{\text{dr}}$, we replace in (3.26) the potential drop $\Delta\psi_{\text{s}}$ by an effective potential drop $V_{\text{DiS,eff}}$, which takes the minimum of V_{DiS} and $V_{\text{DiS,sat}}$ in a smooth manner according to [20]

$$V_{\text{DiS,eff}} = \frac{V_{\text{DiS}} V_{\text{DiS,sat}}}{\left(V_{\text{DiS}}^{2m} + V_{\text{DiS,sat}}^{2m} \right)^{1/(2m)}}. \tag{3.28}$$

Here, m is a model parameter, representing the smoothness of the transition from the linear operating regime to saturation. Finally, the surface potential ψ_{s_L} is calculated by using $V_{\mathrm{DiB}} = V_{\mathrm{SB}} + V_{\mathrm{DiS,eff}}$, which determines the drain-to-source current I_{DS} according (3.26).

2.1.2 Drift Region Current

The current I_{dr} through the drift region of width W_{D} is given by

$$I_{\mathrm{dr}} = -W_{\mathrm{D}}\mu_{\mathrm{dr}}\left(Q_{\mathrm{i}} + Q_{\mathrm{acc}}^{\mathrm{dr}} + Q_{\mathrm{dep}}^{\mathrm{dr}}\right)\frac{\mathrm{d}V_{\mathrm{C}}}{\mathrm{d}x}, \tag{3.29}$$

with V_{C} the quasi-Fermi potential in the drift region, μ_{dr} the electron mobility in the drift region, and $Q_{\mathrm{acc}}^{\mathrm{dr}}$ and $Q_{\mathrm{dep}}^{\mathrm{dr}}$ the accumulation- and depletion charge per unit area of the drift region, given by (3.13) and (3.14), respectively. Furthermore, Q_{i} is due to the doping N_{D} of the drift region according to

$$Q_{\mathrm{i}} = -C_{\mathrm{ox}}V_{\mathrm{oxp}} = -qN_{\mathrm{D}}t_{\mathrm{Sieff}}, \tag{3.30}$$

with t_{Sieff} the effective thickness of the drift region. Integration of (3.29) from internal drain $x = L$ to drain $x = L + L_{\mathrm{D}}$ (cf. Fig. 3.1) yields

$$I_{\mathrm{dr}} = \frac{W_{\mathrm{D}}\mu_{\mathrm{dr}}C_{\mathrm{ox}}}{L_{\mathrm{D}}}\int_{V_{\mathrm{Di}}}^{V_{\mathrm{D}}}\left(V_{\mathrm{oxp}} + V_{\mathrm{acc}}^{\mathrm{dr}} - V_{\mathrm{dep}}^{\mathrm{dr}}\right)\mathrm{d}V_{\mathrm{C}}, \tag{3.31}$$

in which we assumed the electron mobility in the drift region independent of the channel potential V_{C}. We linearize the accumulation and depletion charge $V_{\mathrm{q}}^{\mathrm{dr}} = V_{\mathrm{acc}}^{\mathrm{dr}} - V_{\mathrm{dep}}^{\mathrm{dr}}$ as

$$V_{\mathrm{q}}^{\mathrm{dr}} = V_{\mathrm{q_{Di}}}^{\mathrm{dr}} - V_{\mathrm{CDi}}, \qquad 0 \le V_{\mathrm{CDi}} \le V_{\mathrm{DDi}}, \tag{3.32}$$

in which $\zeta = -\mathrm{d}V_{\mathrm{q}}^{\mathrm{dr}}/\mathrm{d}V_{\mathrm{C}}$ is set to 1, and $V_{\mathrm{q_{Di}}}^{\mathrm{dr}} = V_{\mathrm{acc_{Di}}}^{\mathrm{dr}} - V_{\mathrm{dep_{Di}}}^{\mathrm{dr}}$, with $V_{\mathrm{acc_{Di}}}^{\mathrm{dr}}$ the accumulation charge at the internal drain (according to (3.13), in case $V_{\mathrm{GDi}}^{*\mathrm{dr}} > 0$), and $V_{\mathrm{dep_{Di}}}^{\mathrm{dr}}$ the depletion charge at the internal drain (according to (3.16), in case $V_{\mathrm{GDi}}^{*\mathrm{dr}} < 0$). Substitution of (3.32) into (3.31) yields

$$I_{\mathrm{dr}} = \frac{W_{\mathrm{D}}\mu_{\mathrm{dr}}C_{\mathrm{ox}}}{L_{\mathrm{D}}}\left(V_{\mathrm{oxp}} + V_{\mathrm{q_{Di}}}^{\mathrm{dr}} - \frac{1}{2}V_{\mathrm{DDi}}\right)V_{\mathrm{DDi}}, \tag{3.33}$$

in which the effective thickness $t_{\mathrm{Si_{eff}}}$ is taken independent of the channel position. Due to depletion caused by the pn-junction, this effective thickness depends on the potential drop across the depletion layer. However, the extension of the depletion layer into the drift region is a two-dimensional effect. Since incorporation of the two-dimensional depletion effect is too complicated for a compact model, we follow

a pragmatic approach. We write for ease of parameter extraction the effective drift region thickness as

$$t_{\mathrm{Si_{eff}}} = t_{\mathrm{Si}}|_{V_{\mathrm{SB}}=0}\ f_{\mathrm{lin}}, \tag{3.34}$$

where $t_{\mathrm{Si}}|_{V_{\mathrm{SB}}=0}$ is the thickness at $V_{\mathrm{SB}} = 0$. The function f_{lin} accounts for $V_{\mathrm{SB}} > 0$ for the reduction of the drift region thickness due to the extension of the depletion layer into the drift region, according to

$$f_{\mathrm{lin}} = 1 - \lambda \frac{\sqrt{\phi_0 + V_{\mathrm{SB}}} - \sqrt{\phi_0}}{\sqrt{\phi_0}}. \tag{3.35}$$

Here, $\phi_0 = \frac{1}{2}\left(\phi_{\mathrm{B}} + \phi_{\mathrm{B}}^{\mathrm{dr}}\right)$ is the built-in potential of the pn-junction, and λ is a model parameter (usually, in the range of $0.1 - 0.4$).

Mobility reduction due to the horizontal and vertical electrical fields in the drift region is accounted for by taking the mobility μ_{dr}, analogously as that for the channel region, as

$$\mu_{\mathrm{dr}} = \frac{\mu_{\mathrm{eff}}^{\mathrm{dr}}}{1 + \dfrac{\mu_0^{\mathrm{dr}}}{L_{\mathrm{D}} v_{\mathrm{sat}}} V_{\mathrm{DDi}}}, \tag{3.36}$$

with $\mu_{\mathrm{eff}}^{\mathrm{dr}}$ the effective electron mobility and μ_0^{dr} the zero-field electron mobility in the drift region. The electron mobility in the drift region is reduced by the vertical electrical fields, according to

$$\mu_{\mathrm{eff}}^{\mathrm{dr}} = \frac{\mu_0^{\mathrm{dr}}}{F_{\mathrm{mob,acc}}}, \qquad F_{\mathrm{mob,acc}} = 1 + a_{\theta,\mathrm{acc}}\, E_{\mathrm{eff}}^{\mathrm{dr}}, \tag{3.37}$$

where $a_{\theta,\mathrm{acc}}$ is a constant, and $E_{\mathrm{eff}}^{\mathrm{dr}} = -Q_{\mathrm{acc}}^{\mathrm{dr}}/\epsilon_{\mathrm{Si}}$ represents the effective vertical electrical field in the drift region. To arrive at an expression independent of the internal drain potential, the effective vertical electrical field is taken as $E_{\mathrm{eff}}^{\mathrm{dr}} = -\frac{1}{2}\left(Q_{\mathrm{acc}}^{\mathrm{dr}}|_{V_{\mathrm{C}}=V_{\mathrm{S}}} + Q_{\mathrm{acc}}^{\mathrm{dr}}|_{V_{\mathrm{C}}=V_{\mathrm{D}}}\right)/\epsilon_{\mathrm{Si}}$, such that

$$F_{\mathrm{mob,acc}} = 1 + \theta_{1\mathrm{acc}}\left(\frac{1}{2}\left(V_{\mathrm{GS}} + V_{\mathrm{GD}}\right) - V_{\mathrm{FB}}^{\mathrm{dr}}\right), \tag{3.38}$$

for given model parameter $\theta_{1\mathrm{acc}} = a_{\theta,\mathrm{acc}} C_{\mathrm{ox}}/\epsilon_{\mathrm{Si}}$. Substitution of (3.36) and (3.37) into (3.33) yields

$$I_{\mathrm{dr}} = \beta_{\mathrm{acc}} \frac{\left(V_{\mathrm{oxp}} + V_{\mathrm{qDi}}^{\mathrm{dr}} - \dfrac{1}{2} V_{\mathrm{DDi}}\right) V_{\mathrm{DDi}}}{F_{\mathrm{mob,acc}}\left(1 + \theta_3^{\mathrm{dr}} V_{\mathrm{DDi}}\right)}, \tag{3.39}$$

where $\beta_{\mathrm{acc}} = W_{\mathrm{D}} \mu_0^{\mathrm{dr}} C_{\mathrm{ox}}/L_{\mathrm{D}}$ and $\theta_3^{\mathrm{dr}} = \mu_0^{\mathrm{dr}}/(L_{\mathrm{D}} v_{\mathrm{sat}})$ are taken as model parameter, and V_{oxp} is written as

$$V_{\mathrm{oxp}} = \frac{t_{\mathrm{Si_{eff}}}}{C_{\mathrm{ox}}} = \frac{f_{\mathrm{lin}}}{R_{\mathrm{D}} \beta_{\mathrm{acc}}}, \qquad R_{\mathrm{D}} = \frac{L_{\mathrm{D}}}{W_{\mathrm{D}} \mu_0^{\mathrm{dr}}\, q N_{\mathrm{D}}\, t_{\mathrm{Si}}|_{V_{\mathrm{SB}}=0}}. \tag{3.40}$$

Here, R_D represents the on-resistance of the drift region, which is taken as model parameter.

In case of saturation in the drift region (also referred to as quasi-saturation), the potential drop $V_{DDi} = V_{DDi,sat}$ is determined from $\partial I_{dr}/\partial V_{DDi} = 0$. By use of (3.39) we obtain

$$V_{DDi,sat} = \frac{2\left(V_{oxp} + V_{qDi}^{dr}\right)}{1 + \sqrt{1 + 2\theta_3^{dr}\left(V_{oxp} + V_{qDi}^{dr}\right)}}. \tag{3.41}$$

Hence, in solving the internal potential V_{Di} from $I_{ch} = I_{dr}$, we replace in (3.39) the potential drop V_{DDi} by an effective potential drop $V_{DDi,eff}$, which takes the minimum of V_{DDi} and $V_{DDi,sat}$ in a smooth manner according to [20]

$$V_{DDi,eff} = \frac{V_{DDi} V_{DDi,sat}}{\left(V_{DDi}^{2m_{dr}} + V_{DDi,sat}^{2m_{dr}}\right)^{1/(2m_{dr})}}. \tag{3.42}$$

Here, m_{dr} is a model parameter, representing the smoothness of the transition from the linear operating regime to quasi-saturation.

2.2 Additional Effects and Avalanche Currents

In the final drain-to-source current I_{DS} calculation, second-order effects like channel length modulation, drain-induced barrier lowering and static feedback are incorporated. Also the effect of avalanche occurring in both the channel and drift region are included. For an overview of the governing equations for channel length modulation, drain-induced barrier lowering, static feedback and avalanche in channel- and drift region, we refer to [4].

2.3 Terminal Charge Model

To determine the terminal charges Q_i, $i = D, G, S, B$, all different stadia of strong inversion, depletion and accumulation in both the drift region and the channel region have to be taken into account. The gate charge Q_G of the device consists of the gate charge Q_G^{ch} of the channel region and the gate charge Q_G^{dr} of the drift region, according to

$$Q_G = Q_G^{ch} + Q_G^{dr}, \tag{3.43}$$

where

$$Q_G^{ch} = -W \int_0^L Q_s \, dx, \qquad Q_G^{dr} = -W_D \int_L^{L+L_D} Q_s^{dr} \, dx, \tag{3.44}$$

with the surface charges, given by (3.5) and (3.11), corresponding to the contribution due to accumulation, depletion and (strong) inversion; see (3.6) and (3.12).

Recently, it has been found that for laterally non-uniform devices, like an LDMOS, no terminal drain- and source charge exists from which the corresponding drain- and source related capacitances can be determined [5]. For practical reasons, however, MOS Model 20 is equipped with also a drain- and source charge model, carefully chosen to incorporate the effect of the non-uniformity due to the two different regions. The charge at the drain- and source terminal is written as

$$Q_{\mathrm{D}} = Q_{\mathrm{D}}^{\mathrm{ch}} + Q_{\mathrm{D}}^{\mathrm{dr}}, \qquad Q_{\mathrm{S}} = Q_{\mathrm{S}}^{\mathrm{ch}} + Q_{\mathrm{S}}^{\mathrm{dr}}, \tag{3.45}$$

where $Q_{\mathrm{D}}^{\mathrm{ch}}$ and $Q_{\mathrm{S}}^{\mathrm{ch}}$ represent the contribution due to inversion in the channel region, while $Q_{\mathrm{D}}^{\mathrm{dr}}$ and $Q_{\mathrm{S}}^{\mathrm{dr}}$ represent the contribution due to accumulation and depletion in the drift region. To determine how the charge is distributed between the source and drain terminal two limits are identified. The first limit is for well above threshold (i.e. for the gate voltage sufficiently large), and the charge is distributed according to the Ward–Dutton charge partitioning scheme [27] (valid for a uniform MOSFET without velocity saturation; see [28]), so that

$$\begin{aligned} Q_{\mathrm{D}}^{\mathrm{ch}} &= W \int_0^L \frac{x}{L + L_{\mathrm{D}}} Q_{\mathrm{inv}}\, \mathrm{d}x, \\ Q_{\mathrm{S}}^{\mathrm{ch}} &= W \int_0^L \left(1 - \frac{x}{L + L_{\mathrm{D}}}\right) Q_{\mathrm{inv}}\, \mathrm{d}x, \end{aligned} \tag{3.46}$$

and

$$\begin{aligned} Q_{\mathrm{D}}^{\mathrm{dr}} &= W_{\mathrm{D}} \int_L^{L+L_{\mathrm{D}}} \frac{x}{L + L_{\mathrm{D}}} \left(Q_{\mathrm{acc}}^{\mathrm{dr}} + Q_{\mathrm{dep}}^{\mathrm{dr}}\right) \mathrm{d}x, \\ Q_{\mathrm{S}}^{\mathrm{dr}} &= W_{\mathrm{D}} \int_L^{L+L_{\mathrm{D}}} \left(1 - \frac{x}{L + L_{\mathrm{D}}}\right) \left(Q_{\mathrm{acc}}^{\mathrm{dr}} + Q_{\mathrm{dep}}^{\mathrm{dr}}\right) \mathrm{d}x. \end{aligned} \tag{3.47}$$

In [7] the deviation from the Ward–Dutton charge partitioning scheme in case of velocity saturation is shown, which has been found to be relatively small for sufficiently long devices. Hence, in Eqs. 3.46 and 3.47 the charges of the channel and drift region are distributed between the source and drain terminal. The second limit is for below threshold (i.e. for the gate voltage sufficiently small), and the contribution due to the drift region is attributed completely to the drain, i.e.

$$\begin{aligned} Q_{\mathrm{D}}^{\mathrm{dr}} &= W_{\mathrm{D}} \int_L^{L+L_{\mathrm{D}}} \left(Q_{\mathrm{acc}}^{\mathrm{dr}} + Q_{\mathrm{dep}}^{\mathrm{dr}}\right) \mathrm{d}x, \\ Q_{\mathrm{S}}^{\mathrm{dr}} &= 0. \end{aligned} \tag{3.48}$$

The second limit is calculated in case $V_{\mathrm{invL}} = 0$. In the model, the transition from the first limit (3.47) to the second limit (3.48) has been implemented in a smooth and continuous way.

Finally, the bulk charge Q_{B} of the device consists of the sum of the charges at the drain, gate and source terminal, according to

$$Q_{\mathrm{B}} = -\left(Q_{\mathrm{G}} + Q_{\mathrm{D}} + Q_{\mathrm{S}}\right), \tag{3.49}$$

so that charge conservation in the device is satisfied.

For elaboration of the integrals in the channel region, we transform the integration variable x to ψ_{s} by use of (3.18), and to V_{inv} by use of (3.8). Under the assumption that $\xi = -\mathrm{d}V_{\mathrm{inv}}/\mathrm{d}\psi_{\mathrm{s}}$ is independent of the channel position, these integrals can be expressed in terms of the surface potentials ψ_{s_0} and ψ_{s_L}, and inversion charges V_{inv_0} and V_{inv_L}. For the channel region contribution to the gate charge we thus obtain (cf. [22])

$$Q_{\mathrm{G}}^{\mathrm{ch}} = C_{\mathrm{OX}}\left[V_{\mathrm{GB}}^{*} - \frac{1}{2}\left(\psi_{\mathrm{s}_L} + \psi_{\mathrm{s}_0}\right) + \frac{F}{12\,\xi}\Delta V_{\mathrm{GT}}\right], \tag{3.50}$$

where

$$\Delta V_{\mathrm{GT}} = V_{\mathrm{inv}_0} - V_{\mathrm{inv}_L}, \qquad \overline{V}_{\mathrm{GT}} = \frac{V_{\mathrm{inv}_0} + V_{\mathrm{inv}_L}}{2}, \qquad F = \frac{\Delta V_{\mathrm{GT}}}{\overline{V}_{\mathrm{GT}} + \xi\phi_{\mathrm{T}}}. \tag{3.51}$$

For the channel region contribution (3.46) to the drain and source charge we obtain

$$Q_{\mathrm{D}}^{\mathrm{ch}} = F_L\, Q_{\mathrm{D}}^{\mathrm{mos}}, \qquad Q_{\mathrm{S}}^{\mathrm{ch}} = Q_{\mathrm{S}}^{\mathrm{mos}} + (1 - F_L)\, Q_{\mathrm{D}}^{\mathrm{mos}}, \tag{3.52}$$

where $F_L = L/(L + L_{\mathrm{D}})$, and $Q_{\mathrm{D}}^{\mathrm{mos}}$ and $Q_{\mathrm{S}}^{\mathrm{mos}}$ represent the terminal drain- and source charge of a conventional MOS transistor, given by

$$\begin{aligned} Q_{\mathrm{D}}^{\mathrm{mos}} &= -\frac{C_{\mathrm{OX}}}{2}\left[\overline{V}_{\mathrm{GT}} - \frac{\Delta V_{\mathrm{GT}}}{6}\left(1 - \frac{F}{2} - \frac{F^2}{20}\right)\right], \\ Q_{\mathrm{S}}^{\mathrm{mos}} &= -\frac{C_{\mathrm{OX}}}{2}\left[\overline{V}_{\mathrm{GT}} + \frac{\Delta V_{\mathrm{GT}}}{6}\left(1 + \frac{F}{2} - \frac{F^2}{20}\right)\right]. \end{aligned} \tag{3.53}$$

Here, $C_{\mathrm{OX}} = WLC_{\mathrm{ox}}$ is taken as model parameter.

For elaboration of the integrals in the drift region, we transform the integration variable x to V_{C} by use of (3.29), and to $V_{\mathrm{q}}^{\mathrm{dr}} = V_{\mathrm{acc}}^{\mathrm{dr}} - V_{\mathrm{dep}}^{\mathrm{dr}}$ by use of (3.13) and (3.16). Under the assumption that $\zeta = -\mathrm{d}V_{\mathrm{q}}^{\mathrm{dr}}/\mathrm{d}V_{\mathrm{C}}$ is independent of the channel position, these integrals can be expressed in terms of the surface potentials $\psi_{\mathrm{s_{Di}}}^{\mathrm{dr}}$ and $\psi_{\mathrm{s_D}}^{\mathrm{dr}}$, and accumulation- and depletion charges $V_{\mathrm{q_{Di}}}^{\mathrm{dr}}$ and $V_{\mathrm{q_D}}^{\mathrm{dr}}$. For the contribution to the gate charge we thus obtain

$$Q_{\mathrm{G}}^{\mathrm{dr}} = C_{\mathrm{OXD}}\left[\frac{1}{2}\left(V_{\mathrm{GDi}}^{*\mathrm{dr}} + V_{\mathrm{GD}}^{*\mathrm{dr}}\right) - \frac{1}{2}\left(\psi_{\mathrm{s_{Di}}}^{\mathrm{dr}} + \psi_{\mathrm{s_D}}^{\mathrm{dr}}\right) + \frac{F^{\mathrm{dr}}}{12}\Delta V_{\mathrm{q}}^{\mathrm{dr}}\right], \tag{3.54}$$

where

$$\Delta V_{\mathrm{q}}^{\mathrm{dr}} = V_{\mathrm{qDi}}^{\mathrm{dr}} - V_{\mathrm{qD}}^{\mathrm{dr}}, \qquad \overline{V}_{\mathrm{q}}^{\mathrm{dr}} = \frac{V_{\mathrm{qDi}}^{\mathrm{dr}} + V_{\mathrm{qD}}^{\mathrm{dr}}}{2}, \qquad F^{\mathrm{dr}} = \frac{\Delta V_{\mathrm{q}}^{\mathrm{dr}}}{\overline{V}_{\mathrm{q}}^{\mathrm{dr}} + V_{\mathrm{oxp}}}. \tag{3.55}$$

Here, $C_{\mathrm{OX}}^{\mathrm{dr}} = W_{\mathrm{D}} L_{\mathrm{D}} C_{\mathrm{ox}}$ is taken as model parameter. For the drift region contribution (3.47) to the drain and source charge valid for well above threshold, we obtain

$$Q_{\mathrm{D}}^{\mathrm{dr}} = Q_{\mathrm{D}}^{\mathrm{accdep}} + F_L Q_{\mathrm{S}}^{\mathrm{accdep}}, \qquad Q_{\mathrm{S}}^{\mathrm{dr}} = (1 - F_L) Q_{\mathrm{S}}^{\mathrm{accdep}}, \tag{3.56}$$

where, analogously as for the channel region, $Q_{\mathrm{D}}^{\mathrm{accdep}}$ and $Q_{\mathrm{S}}^{\mathrm{accdep}}$ are given according to (3.53) with C_{OX} replaced by $C_{\mathrm{OX}}^{\mathrm{dr}}$, $\overline{V}_{\mathrm{GT}}$ by $\overline{V}_{\mathrm{q}}^{\mathrm{dr}}$, ΔV_{GT} by $\Delta V_{\mathrm{q}}^{\mathrm{dr}}$, and F by F^{dr}. For the drift region contribution (3.47) to the drain and source charge valid for below threshold, we obtain

$$Q_{\mathrm{D}}^{\mathrm{dr}} = Q_{\mathrm{D}}^{\mathrm{accdep}} + Q_{\mathrm{S}}^{\mathrm{accdep}}, \qquad Q_{\mathrm{S}}^{\mathrm{dr}} = 0. \tag{3.57}$$

2.4 Self-Heating

For high-voltage devices the effect of self-heating is significant. The effect is even more significant in case of SOI-technology; see [3, 8] and [23]. To account for the temperature rise due to self-heating MOS Model 20 is equipped with a self-heating model. In this model the dissipation power P_{diss} is determined from the dc-currents according to

$$P_{\mathrm{diss}} = I_{\mathrm{DS}} V_{\mathrm{DS}} + I_{\mathrm{DB}} V_{\mathrm{DB}}. \tag{3.58}$$

Subsequently, the temperature rise ΔT_{th} due to self-heating is determined according to

$$C_{\mathrm{th}} \frac{\mathrm{d}\Delta T_{\mathrm{th}}}{\mathrm{d}t} + \frac{\Delta T_{\mathrm{th}}}{R_{\mathrm{th}}} = P_{\mathrm{diss}}, \tag{3.59}$$

as represented in the equivalent circuit depicted in Fig. 3.4. Here, R_{th} is the thermal resistance of the device, and C_{th} is its thermal capacitance. Notice that the temperature rise due to self-heating affects the dc-currents, so that the dissipation power P_{diss} also depends on the temperature rise ΔT_{th}. The computation of the temperature rise in MOS Model 20 is thus throughout the consistent solution of the thermal circuit depicted in Fig. 3.4.

In Fig. 3.5 the effect of self-heating is demonstrated for a high-voltage (60 V) LDMOS device in SOI-technology. In this figure we observe that for high drain- and gate voltages the slope of the measured I_{DS} versus V_{DS} curve becomes negative, which indicates the effect of self-heating. After all, due to self-heating the temperature inside the device increases, which results in a decrease of, for instance, the electron mobility, and thus the current (cf. Section 2.5). We also observe that if

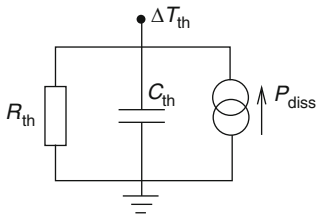

Fig. 3.4 The equivalent circuit used in MOS Model 20 to determine the temperature rise ΔT_{th} due to self-heating

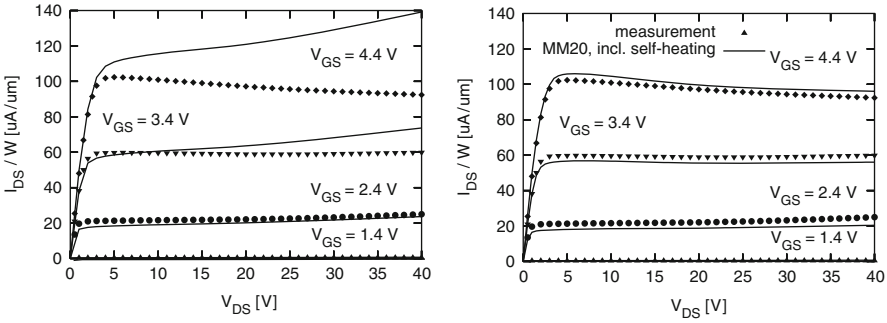

Fig. 3.5 The comparison between measurements (*symbols*) and MOS Model 20 (*solid lines*) with self-heating switched off (*left*) and switched on (*right*), for a 60 V LDMOS device in SOI-technology, for $V_{\text{SB}} = 0$ V

self-heating is switched off in MOS Model 20 (left picture), the model does not fit the measurements. If self-heating is switched on (right picture), however, the model agrees very well with the measurements.

2.5 Scaling

MOS Model 20 is equipped with scaling rules for the model parameters, to be able to predict the device behaviour at various widths, lengths and temperatures. For an overview of the model parameters, we refer to the Appendix.

2.5.1 Temperature Scaling

In MOS Model 20 the reference temperature T_{ref}, given as model parameter in °C, represents the temperature at which the model parameters are extracted. The actual temperature T_{K} of the device (in Kelvin) is determined as

$$T_{\text{K}} = 273.15 + T_{\text{amb}} + \Delta T_{\text{amb}} + \Delta T_{\text{th}}, \tag{3.60}$$

Table 3.1 Overview of the temperature scaling rules of the dc- and terminal charge model parameters

Symbol	Unit	Model parameter	Scaling rule
V_{FB}	V	VFB	$V_{\mathrm{FB}} = \mathrm{VFB} + \mathrm{STVFB}\,\Delta T$
$V_{\mathrm{FB}}^{\mathrm{dr}}$	V	VFBD	$V_{\mathrm{FB}}^{\mathrm{dr}} = \mathrm{VFBD} + \mathrm{STVFBD}\,\Delta T$
ϕ_{B}	V	PHIB	$\phi_{\mathrm{B}} = \mathrm{PHIB} + \mathrm{STPHIB}\,\Delta T$
$\phi_{\mathrm{B}}^{\mathrm{dr}}$	V	PHIBD	$\phi_{\mathrm{B}}^{\mathrm{dr}} = \mathrm{PHIBD} + \mathrm{STPHIBD}\,\Delta T$
β	A/V^2	BET	$\beta = \mathrm{BET}\left(\frac{T_{\mathrm{Kref}}}{T_{\mathrm{K}}}\right)^{\mathrm{ETABET}}$
β_{acc}	A/V^2	BETACC	$\beta_{\mathrm{acc}} = \mathrm{BETACC}\left(\frac{T_{\mathrm{Kref}}}{T_{\mathrm{K}}}\right)^{\mathrm{ETABETACC}}$
R_{D}	V/A	RD	$R_{\mathrm{D}} = \mathrm{RD}\left(\frac{T_{\mathrm{K}}}{T_{\mathrm{Kref}}}\right)^{\mathrm{ETARD}}$
θ_3	1/V	THE3	$\theta_3 = \mathrm{THE3}\left(\frac{T_{\mathrm{Kref}}}{T_{\mathrm{K}}}\right)^{\mathrm{ETATHE3}}$
θ_3^{dr}	1/V	THE3D	$\theta_3^{\mathrm{dr}} = \mathrm{THE3D}\left(\frac{T_{\mathrm{Kref}}}{T_{\mathrm{K}}}\right)^{\mathrm{ETATHE3D}}$

in which T_{amb} is the ambient temperature of the device (given in °C), ΔT_{amb} is an additional temperature difference (given as model parameter), and ΔT_{th} is the temperature rise due to self-heating. The difference between the reference and actual temperature is denoted by $\Delta T = T_{\mathrm{K}} - T_{\mathrm{Kref}}$, with $T_{\mathrm{Kref}} = 273.15 + T_{\mathrm{ref}}$ the reference temperature in Kelvin, and T_{ref} that in °C. The parameters of the dc-model and the terminal charge model of MOS Model 20 are scaled with temperature according to the rules of Table 3.1. For an overview of the temperature scaling rules for all model parameters, we refer to [4].

2.5.2 Width Scaling

In MOS Model 20 the reference width W_{ref} is set to 1μm. The actual width W of the channel region is determined from $W = \mathrm{W} + \Delta W$, in which W and ΔW are model parameters. Similarly, the actual width W_{D} of the drift region is determined from $W_{\mathrm{D}} = \mathrm{WD} + \Delta W_{\mathrm{D}}$, in which WD and ΔW_{D} are model parameters. The parameters of the dc-model and the terminal charge model of MOS Model 20 are scaled with width according to the rules of Table 3.2. For an overview of the width scaling rules for all model parameters, we refer to [4].

2.5.3 Length Scaling

MOS Model 20 is capable of characterizing devices of different lengths. To that end, the model parameters of MOS Model 20 which include the length L of the

Table 3.2 Overview of the width scaling rules of the dc- and terminal charge model parameters

Symbol	Unit	Model parameter	Scaling rule
k_0	$V^{1/2}$	KOR	$k_0 = \text{KOR}\left(1 + \frac{W_{\text{ref}}}{W}\text{SWKO}\right)$
k_{dr}	$V^{1/2}$	KODR	$k_{\text{dr}} = \text{KODR}\left(1 + \frac{W_{\text{ref}}}{W_{\text{D}}}\text{SWKOD}\right)$
β	A/V^2	BETW	$\beta = \text{BETW}\frac{W_{\text{ref}}}{W}$
β_{acc}	A/V^2	BETACCW	$\beta_{\text{acc}} = \text{BETACCW}\frac{W_{\text{ref}}}{W_{\text{D}}}$
R_{D}	V/A	RDW	$R_{\text{D}} = \text{RDW}\frac{W_{\text{D}}}{W_{\text{ref}}}$
θ_1	1/V	THE1R	$\theta_1 = \text{THE1R}\left(1 + \frac{W_{\text{ref}}}{W}\text{SWTHE1}\right)$
θ_2	1/V	THE2R	$\theta_2 = \text{THE2R}\left(1 + \frac{W_{\text{ref}}}{W}\text{SWTHE2}\right)$
θ_3	1/V	THE3R	$\theta_3 = \text{THE3R}\left(1 + \frac{W_{\text{ref}}}{W}\text{SWTHE3}\right)$
θ_3^{dr}	1/V	THE3DR	$\theta_3^{\text{dr}} = \text{THE3DR}\left(1 + \frac{W_{\text{ref}}}{W_{\text{D}}}\text{SWTHE3D}\right)$
C_{OX}	F	COXW	$C_{\text{OX}} = \text{COXW}\frac{W_{\text{D}}}{W_{\text{ref}}}$
$C_{\text{OX}}^{\text{dr}}$	F	COXDW	$C_{\text{OX}}^{\text{dr}} = \text{COXDW}\frac{W}{W_{\text{ref}}}$

channel region and/or the length L_{D} of the drift region need to be adapted accordingly. The major parameters which depend on length are β, β_{acc}, R_{D}, C_{OX}, and $C_{\text{OX}}^{\text{dr}}$. In Section 3 the results are shown for two LDMOS devices of different length.

3 Results and Parameter Extraction Strategy

In this section results are shown for MOS Model 20 in comparison to measurements. The measurements have been performed for a low- and a high-voltage LDMOS device, both in SOI-technology, yielding devices of different length; cf. Figs. 3.1 and 3.2. In this section, also the parameter extraction strategy is briefly discussed, based on the measurements shown in the plots.

3.1 Dc-Currents

In the following the dc-currents are shown for a high-voltage (60V) LDMOS device in SOI technology, as depicted in Fig. 3.2. Here, an additional resistor is used for the extension of the drift region underneath the thick field oxide. To model the

current through the pn-junction in case it is biased in forward operation, a parasitic diode is included for this current; see Fig. 3.2. The length of the region underneath the thin gate oxide is $L_{ch} + L_D = 2.6$ μm, while the extension of the drift region underneath the thick field-oxide is 3.5 μm. The threshold voltage of the device is approximately 1.4 V.

In Fig. 3.6 the sub-threshold current is plotted versus gate voltage, for various drain and bulk voltages. In this regime the current is mainly characterized by the gain factor β, the body factor k_0, the potential ϕ_B at the onset of strong inversion, and the flatband voltage V_{FB} of the channel region. We observe that the model predicts the measured current accurately, for all voltages applied. For high drain voltages static feedback occurs, an effect which is also adequately described by MOS Model 20 (tuned by model parameter σ_{sf}). Notice that the accurate description in the sub-threshold region is thanks to formulation in terms of surface potentials.

In Fig. 3.7 the dc-current and transconductance are plotted in the linear operating regime. Here, also the threshold voltage is determined, from the model parameters

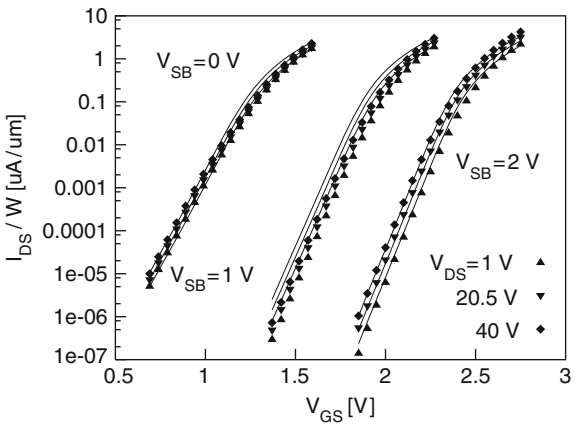

Fig. 3.6 The drain–source current in the sub-threshold regime, simulated by means of MOS Model 20 (*solid lines*) in comparison to measurements (*symbols*), for various drain and bulk voltages V_{DS} and V_{SB}

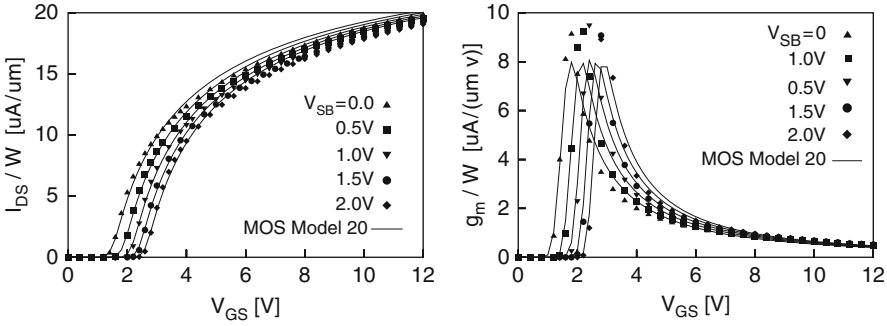

Fig. 3.7 The drain–source current (*left picture*) and transconductance (*right picture*) in the linear operating regime ($V_{DS} = 0.25$ V), simulated by means of MOS Model 20 (*solid lines*) in comparison to measurements (*symbols*), for various bulk voltages V_{SB}

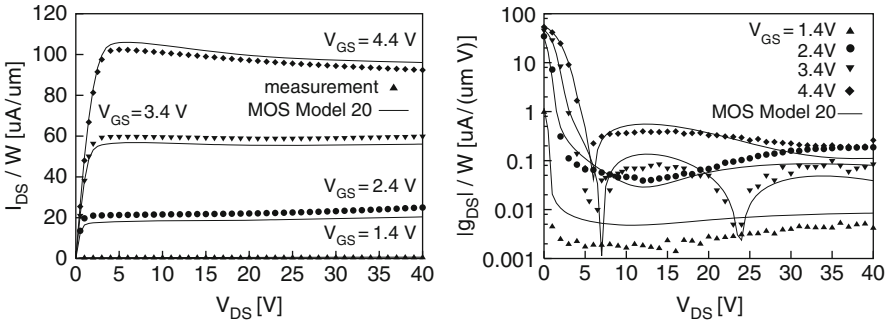

Fig. 3.8 The drain–source current (*left picture*) and output conductance (*right picture*), simulated by means of MOS Model 20 (*solid lines*) in comparison to measurements (*symbols*), for $V_{SB} = 0$V, and various gate voltages V_{GS}

k_0, ϕ_B and V_{FB}. Above threshold, the current is mainly characterized by the channel region gain factor parameter β, and the gain factor β_{acc} and resistance R_D of the drift region. For high gate-voltages the effect of gate extending over the drift region is observed, and electron mobility is reduced due to the high electrical fields, an effect mainly characterized by θ_1 and θ_{1acc}. We observe that the model predicts the measured current accurately, also for the high-gate voltages. We notice that although the effect of the diffused doping profile is not covered in MOS Model 20, the transconductance is quite well described; only around the threshold voltage the model underestimates the transconductance.

In Fig. 3.8 the dc-current and output conductance are plotted, for relatively low gate-voltages. For high drain voltages the current saturates, due to the occurrence of velocity saturation in the channel region. Here, in saturation the current is mainly characterized by the channel region parameters β, θ_1 and θ_3. We observe that for $V_{GS} = 3.4$ and 4.4 V the slope of I_{DS} versus V_{DS} becomes negative, an effect caused by self-heating; cf. Section 2.4. The output conductance is plotted on a logarithmic scale, to indicate the accuracy for low V_{GS}. The output conductance is characterized mainly by the static-feedback and drain-induced-barrier-lowering parameters for the lowest gate voltages (around threshold), by the channel-length-modulation parameters for the intermediate gate-voltage, and by the thermal resistance R_{th} and the avalanche parameters for the channel region for higher gate voltages. We observe that the model predicts the measured current and output conductance accurately, including the effect of self-heating.

In Fig. 3.9 the dc-current and output conductance are plotted for relatively high gate-voltages. For these high gate voltages the current saturates because of velocity saturation in the drift region (quasi-saturation). In the left picture we observe that if quasi-saturation is switched off in MOS Model 20 (i.e. $\theta_3^{dr} = 0$), only the currents at the lower gate voltages are accurately described. If quasi-saturation is switched on in MOS Model 20, on the other hand, we observe in the right picture that also the currents at the high gate voltages are accurately described. The current at high gate

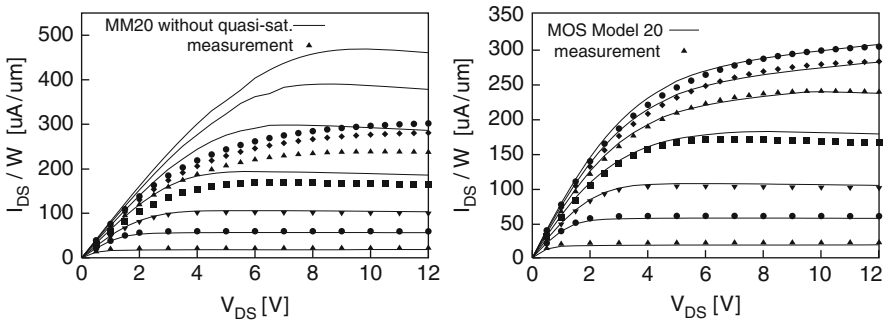

Fig. 3.9 The drain–source current in the quasi-saturation regime, simulated by means of MOS Model 20 (*lines*) without quasi-saturation (*left picture*) and including quasi-saturation (*right picture*), in comparison to measurements (*symbols*), for $V_{SB} = 0$ V, and gate voltages $V_{GS} = 2.4$, 3.4, 4.4, 6, 8, 10, and 12 V

voltages is mainly described by the quasi-saturation parameters θ_3^{dr} and m^{dr}, with the avalanche parameters for the drift region determining the current at the highest drain voltages.

3.2 Capacitances

For verification of the terminal charge model, high-frequency S-parameter measurements have been carried out, from which the Y-parameters have been determined, and subsequently the capacitances C_{ij} are determined according to

$$C_{ij} = \left(2\delta_{ij} - 1\right) \frac{\mathrm{Im}\left[Y_{ij}\right]}{2\pi f}, \tag{3.61}$$

for given frequency f. In MOS Model 20 the capacitances are determined from the terminal charge model according to (3.3). Due to the resistance of the gate terminal, the imaginary parts of the Y-parameters of the device are related to the intrinsic capacitances C_{ij} and transconductance g_{m} of MOS Model 20, according to

$$\begin{aligned}
\mathrm{Im}\left[Y_{\mathrm{GG}}\right] &= 2\pi f\ C_{\mathrm{in}}, \\
\mathrm{Im}\left[Y_{\mathrm{GD}}\right] &= -2\pi f\ \left[C_{\mathrm{GD}} + C_{\mathrm{GDO}}\right], \\
\mathrm{Im}\left[Y_{\mathrm{DG}}\right] &= -2\pi f\ \left[\left(C_{\mathrm{DG}} + C_{\mathrm{GDO}}\right) + g_{\mathrm{m}} R_{\mathrm{G}} C_{\mathrm{in}}\right], \\
\mathrm{Im}\left[Y_{\mathrm{DD}}\right] &= 2\pi f\ \left[C_{\mathrm{DD}} + g_{\mathrm{m}} R_{\mathrm{G}}\left(C_{\mathrm{GD}} + C_{\mathrm{GDO}}\right)\right],
\end{aligned} \tag{3.62}$$

where R_{G} represents the resistance of the gate, $C_{\mathrm{in}} = C_{\mathrm{GG}} + C_{\mathrm{GDO}} + C_{\mathrm{GSO}}$ is the input capacitance, and C_{GDO} and C_{GSO} are the overlap capacitances between gate and drain, and gate and source, respectively.

In this section the Y-parameters are shown for a low-voltage (14 V) LDMOS device in SOI-technology, as depicted in Fig. 3.1. The length of the region underneath the thin gate oxide is $L_{ch} + L_D = 5.0\,\mu m$, and the LDMOS device has a threshold voltage of around 2.8 V. The bulk and source terminal are tied together, so that here $V_{SB} = 0$ V. The Y-parameters have been measured at $f = 0.1$ GHz.

In Fig. 3.10 the imaginary part of Y_{GG} is plotted for various drain- and gate voltages. For V_{GS} strongly negative, accumulation in the channel region and inversion in the drift region occur, so that the intrinsic capacitance C_{GG} equals the total capacitance $C_{OX} + C_{OX}^{dr}$. The model parameters V_{FB}^{dr}, ϕ_B^{dr} and k^{dr} determine the onset of inversion in the drift region. For V_{GS} around 0V, depletion occurs in both the channel and drift region; cf. Fig. 3.3. With the body factor k_0 of the channel region already determined from the dc-currents, here only the body factor k^{dr} of the drift region is set to characterize the total amount of depletion. We observe that the model agrees well with the measurements over the whole bias range.

In Fig. 3.11 the imaginary part of Y_{GD} is plotted for various drain- and gate voltages. For V_{GS} strongly negative, accumulation in the channel region and

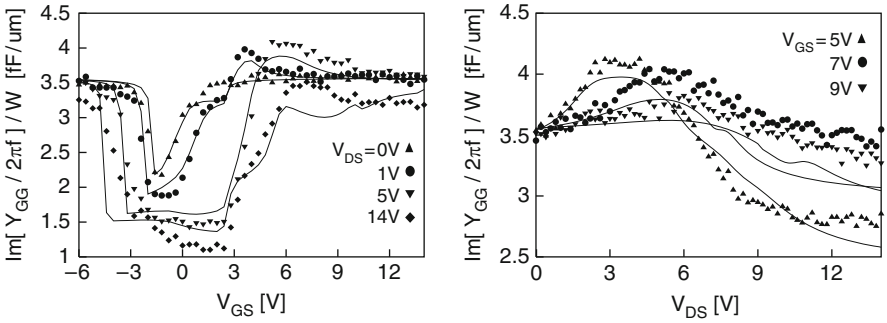

Fig. 3.10 The imaginary part of Y_{GG}, simulated by means of MOS Model 20 (*solid lines*) in comparison to measurements (*symbols*)

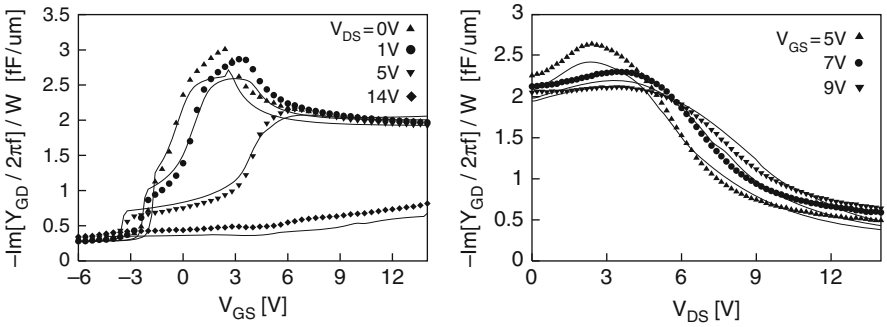

Fig. 3.11 The imaginary part of Y_{GD}, simulated by means of MOS Model 20 (*solid lines*) in comparison to measurements (*symbols*)

inversion in the drift region occur, so that C_{GD} becomes zero, and subsequently $\mathrm{Im}[Y_{GD}]/(2\pi f) = C_{GDO}$. For V_{GS} around 0V, we observe the square-root capacitance behaviour due to depletion in both the channel and drift region. Around the threshold voltage we observe for low drain voltages a peak in $\mathrm{Im}[Y_{GD}]/(2\pi f)$, which is caused by a redistribution of the charge underneath the oxide when the transistor is switched on. This peak is due to the diffused doping profile in the channel region as well as the non-uniformity of the channel region in combination with the drift region in the LDMOS device itself. We note that only the part of the peak due to the diffused doping profile (cf. [5]) is not covered by MOS Model 20, an effect which we observe in Fig. 3.11 to be relatively small. For high gate voltages the intrinsic capacitance C_{GD} tends to the value $\frac{1}{2}[C_{OX}^{dr} + \left(C_{OX}^{dr} + C_{OX}\right)\partial V_{DiS}/\partial V_{DS}]$, for $V_{DS} = 0$V. The solution of the internal drain voltage V_{DiS} in the model thus automatically generates the adequate gate-related capacitances.

In Figs. 3.12 and 3.13 the imaginary parts of Y_{DG} and Y_{DD} are plotted, representing the drain-related intrinsic capacitances C_{DG} and C_{DD}; see (3.62). In these figures we observe that the modeled drain-related capacitances correspond reasonably

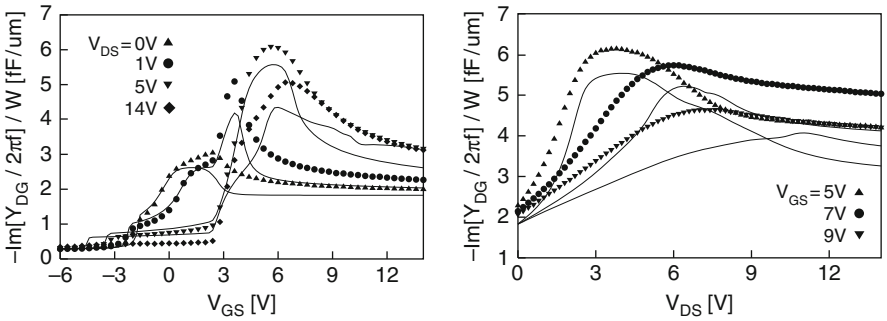

Fig. 3.12 The imaginary part of Y_{DG}, simulated by means of MOS Model 20 (*solid lines*) in comparison to measurements (*symbols*)

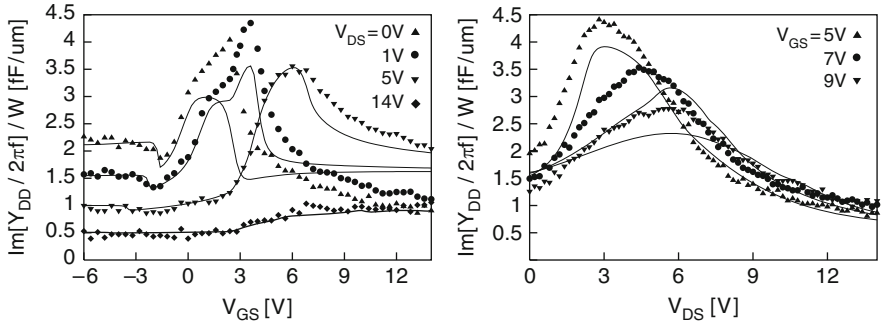

Fig. 3.13 The imaginary part of Y_{DD}, simulated by means of MOS Model 20 (*solid lines*) in comparison to measurements (*symbols*)

well with the measurements. We note that in MOS Model 20 the drain-related capacitances are determined from a modified Ward–Dutton charge partitioning scheme according to (3.46)–(3.48).

4 Discussion and Conclusion

A surface-potential based compact LDMOS model has been presented, which combines the MOSFET channel region with the drift region of an LDMOS device inside one model. The model includes all specific high-voltage aspects, like the effect of the gate extending over the drift region and velocity saturation in the drift region (quasi-saturation). The numerical iteration procedure implemented inside the model provides a robust and efficient way to determine the internal drain potential in all operating regimes. Effects like mobility reduction, velocity saturation, channel-length-modulation, static-feedback, drain-induced-barrier lowering, and avalanche, are included. MOS Model 20 is completed with a self-heating model, a terminal charge model (from which the capacitances are determined), and a noise model with 1/f-, thermal- and gate-induced noise. A comparison to measurements shows an excellent agreement for both the dc-currents and the capacitances, ranging from sub-threshold to strong inversion, in both the linear and saturation operating regime. By the use of MOS Model 20 for different LDMOS devices and at different operating temperatures, we found that the model has good width, length- and temperature scaling rules. Finally, we mention that the model is available in the public domain, and has been successfully used for the design of high-voltages IC's.

Acknowledgments The authors would like to thank D.B.M. Klaassen from NXP-TSMC Research Center for the helpful comments and suggestions.

Appendix: Model Parameters

In this section the model parameters of the electrical model of MOS Model 20, level number 2002, are given. For an overview of the model parameters of the corresponding geometrical model, we refer to [4]

No.	Parameter	Symbol	Units	Meaning
0	LEVEL	level	–	Must be 2002
1	TREF	T_{ref}	°C	Reference temperature
2	VFB	V_{FB}	V	Flatband voltage of the channel region, at reference temperature
3	STVFB	$S_{T;\mathrm{V_{FB}}}$	V/K	Temperature scaling coefficient for V_{FB}

(continued)

(continued)

No.	Parameter	Symbol	Units	Meaning
4	VFBD	$V_{\mathrm{FB}}^{\mathrm{dr}}$	V	Flatband voltage of the drift region, at reference temperature
5	STVFBD	$S_{T;\mathrm{V}_{\mathrm{FB}}^{\mathrm{dr}}}$	V/K	Temperature scaling coefficient for $V_{\mathrm{FB}}^{\mathrm{dr}}$
6	KO	k_0	$\mathrm{V}^{1/2}$	Body factor of the channel region
7	KOD	k_{dr}	$\mathrm{V}^{1/2}$	Body factor of the drift region
8	PHIB	ϕ_{B}	V	Surface potential at the onset of strong inversion in the channel region, at reference temperature
9	STPHIB	$S_{T;\phi_{\mathrm{B}}}$	V/K	Temperature scaling coefficient for ϕ_{B}
10	PHIBD	$\phi_{\mathrm{B}}^{\mathrm{dr}}$	V	Surface potential at the onset of strong inversion in the drift region, at reference temperature
11	STPHIBD	$S_{T;\phi_{\mathrm{B}}^{\mathrm{dr}}}$	V/K	Temperature scaling coefficient for ϕ_{BD}
12	BET	β	$\mathrm{A/V}^2$	Gain factor of the channel region, at reference temperature
13	ETABET	η_β	–	Temperature scaling exponent for β
14	BETACC	β_{acc}	$\mathrm{A/V}^2$	Gain factor for accumulation in the drift region, at reference temperature
15	ETABETACC	$\eta_{\beta_{\mathrm{acc}}}$	–	Temperature scaling exponent for β_{acc}
16	RD	R_{D}	Ω	On-resistance of the drift region, at reference temperature
17	ETARD	$\eta_{R_{\mathrm{D}}}$	–	Temperature scaling exponent for R_{D}
18	LAMD	λ	–	Quotient of the depletion layer thickness of the drift region for $V_{\mathrm{SB}} > 0$, to that for $\mathrm{V}_{\mathrm{SB}} = 0\mathrm{V}$
19	THE1	θ_1	V^{-1}	Mobility reduction coefficient in channel region due to vertical electrical field caused by strong inversion
20	THE1ACC	$\theta_{1\mathrm{acc}}$	V^{-1}	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation
21	THE2	θ_2	$\mathrm{V}^{-1/2}$	Mobility reduction coefficient at $V_{\mathrm{SB}} > 0$ in the channel region due to the vertical electrical field caused by depletion
22	THE3	θ_3	V^{-1}	Mobility reduction coefficient in the channel region due to the horizontal electrical field caused by velocity saturation
23	ETATHE3	η_{θ_3}	–	Temperature scaling exponent for θ_3
24	MEXP	m	–	Smoothing factor for transition from linear to saturation regime
25	THE3D	θ_3^{dr}	V^{-1}	Mobility reduction coefficient in the drift region due to the horizontal electrical field caused by velocity saturation
26	ETATHE3D	$\eta_{\theta_3^{\mathrm{dr}}}$	–	Temperature scaling exponent for θ_3^{dr}
27	MEXPD	m_{dr}	–	Smoothing factor for transition from linear to quasi-saturation regime
28	ALP	α	–	Factor for channel length modulation

(continued)

(continued)

No.	Parameter	Symbol	Units	Meaning
29	VP	V_{P}	V	Characteristic voltage of channel length modulation
30	SDIBL	σ_{dibl}	$\mathrm{V}^{-1/2}$	Factor for drain-induced barrier lowering
31	MSDIBL	$m_{\sigma_{\mathrm{dibl}}}$	–	Exponent for the drain-induced barrier lowering dependence on backgate bias
32	MO	m_0	V	Parameter for the (short-channel) sub-threshold slope
33	SSF	σ_{sf}	$\mathrm{V}^{-1/2}$	Factor for static feedback
34	A1CH	$a_{1\mathrm{ch}}$	–	Factor of weak avalanche current in channel region, at reference temperature
35	STA1CH	$S_{T;a_{1\mathrm{ch}}}$	K^{-1}	Temperature scaling coefficient for $a_{1\mathrm{ch}}$
36	A2CH	$a_{2\mathrm{ch}}$	V	Exponent of weak avalanche current in channel region
37	A3CH	$a_{3\mathrm{ch}}$	–	Factor of internal drain-source voltage above which weak avalanche in channel region occurs
38	A1DR	$a_{1\mathrm{dr}}$	–	Factor of weak avalanche current in drift region, at reference temperature
39	STA1DR	$S_{T;a_{1\mathrm{dr}}}$	K^{-1}	Temperature scaling coefficient for $a_{1\mathrm{dr}}$
40	A2DR	$a_{2\mathrm{dr}}$	V	Exponent of weak avalanche current in drift region
41	A3DR	$a_{3\mathrm{dr}}$	–	Factor of drain–internal drain voltage above which weak avalanche in drift region occurs
42	COX	C_{ox}	F	Oxide capacitance for the intrinsic channel region
43	COXD	$C_{\mathrm{ox}}^{\mathrm{dr}}$	F	Oxide capacitance for the intrinsic drift region
44	CGDO	C_{GDO}	F	Gate to drain overlap capacitance
45	CGSO	C_{GSO}	F	Gate to source overlap capacitance
46	NT	N_T	J	Coefficient of thermal noise, at reference temperature
47	NFA	$N_{f\mathrm{A}}$	$\mathrm{V}^{-1}\mathrm{m}^{-4}$	First coefficient of flicker noise
48	NFB	$N_{f\mathrm{B}}$	$\mathrm{V}^{-1}\mathrm{m}^{-2}$	Second coefficient of flicker noise
49	NFC	$N_{f\mathrm{C}}$	V^{-1}	Third coefficient of flicker noise
50	TOX	t_{ox}	m	Thickness of the oxide above the channel region used in the noise model
51	DTA	ΔT_{a}	K	Temperature offset to the ambient temperature
52	RTH	R_{th}	K/W	Thermal resistance
53	CTH	C_{th}	J/K	Thermal capacitance
54	ATH	a_{th}	–	Thermal coefficient of the thermal resistance
55	MULT	M	–	Number of devices in parallel

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Chapter 4
Modeling of High Voltage MOSFETs Based on EKV (HV-EKV)

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Abstract The accurate compact modeling of High Voltage (HV) MOS transistors has always been a great challenge in the device modeling community. This is due to the fact that the charges and field associated with the drift region and intrinsic MOS have very complex dependence on the external terminal biases owing to the asymmetric device architecture. In this chapter, A modeling strategy for HVMOS transistors (HV-EKV) based on the scalable drift resistance [1, 2] and the use of charge based EKV2.6 MOSFET model [3] as a core for the intrinsic MOS channel is presented [4, 5]. The strategy is optimized according to the fast convergence and good accuracy criteria. The model is stable and robust in the entire bias range useful for circuit design purpose. An important aspect of this *general* model is the scalability of the model with physical and electrical parameters along with the correct modeling of quasi-saturation and self-heating effect. The model is validated on the measured characteristics of two widely used high voltage devices in the industry i.e. LDMOS [6] and VDMOS [7] devices, and tested on commercial circuit simulators like SABER (Synopsys), ELDO (Mentor Graphics), HSpice (Synopsys), Spectre (Cadence) and UltraSim (Cadence). The model shows good behavior for all capacitances which are unique for these devices showing peaks and shift of peaks with bias variation. Also the model exhibits excellent scalability with transistor width, drift length, number of fingers and temperature.

The last part of this chapter will explain the importance of modeling of lateral non-uniform doping in the intrinsic channel [8–11]. It is shown that C_{GD} & C_{DG} capacitances are strong function of lateral doping [11, 12].

Keywords HV-EKV · LDMOS · VDMOS · Model · Lateral non-uniform doping · Self heating

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1 Behavior of Surface Potential in the Drift Region

The LDMOS device architecture under study is shown in Fig. 4.2a. The channel of the LDMOS transistor is obtained by a double diffusion process and not by photolithographic process. Consequently, this transistor has gradual doping profile in the channel decreasing from source to the intrinsic drain (V_K) of the device. The second part of the device, i.e. the drift zone, sustains the high voltage applied on the drain terminal of the device. The device presents a gate overlap over both the channel and the drift region, involving the possibility to obtain operation regions where the intrinsic channel is inverted and accumulation/depletion may exist in the drift region under gate.

Figure 4.1 shows the modeling strategy used in this chapter. The HVMOS is divided into low voltage MOS channel and a drift region. The major issue in HVMOS modeling that makes standard low-voltage MOSFET models un-applicable is the bias dependence of the drift resistance (R_{Drift}) with both gate and drain voltages. Consequently, the efforts in this chapter will be concentrated on different solutions to analytically describe the main dependencies of R_{Drift}, in all operation regimes using simple analytical expressions. The modeling of the intrinsic MOS channel is carried out using EKV model [3]. To understand the behavior of drift region, 2-D numerical device simulation is performed using ISE-DESSIS. The idea is to separate the device into physically significant regions and then to inspect and model them independently. The separation boundary between the intrinsic MOS transistor and the drift region is the metallurgical junction of the PIN diode (see V_K point in Fig. 4.2b). Figure 4.3 shows the plot of V_K for different gate and drain voltages. Figure 4.3a, b shows the V_K vs. V_{GS} and V_{DS} respectively [13]. The unique behavior of V_K can be explained by considering the variation of the channel and drift resistance with bias. Initially as V_{GS} increases, most of the drain voltage drop occurs across intrinsic MOS channel as channel resistance is very high compared to drift resistance. With increasing V_{GS}, channel resistance drops sharply compared with drift resistance and at some bias condition, channel resistance becomes equal to drift resistance. This is the point, where, the peak in V_K occurs on $V_K - V_{GS}$ characteristics (see Fig. 4.3a). V_{GS} keeps on increasing after this point, V_K keeps on decreasing as drift resistance now dominates compared to channel resistance. This same explanation can be easily associated with $V_K - V_{DS}$ characteristics also (Fig. 4.3b). Please note that the effect of drift resistance is observed in the linear region only (see Fig. 4.3b). There are two interesting points to note here. First, the major V_{DS} drop occurs across the drift region in strong inversion,

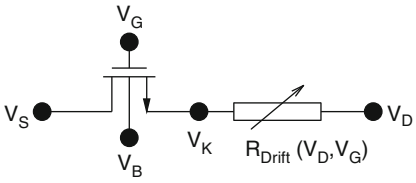

Fig. 4.1 High voltage MOSFET modeling strategy

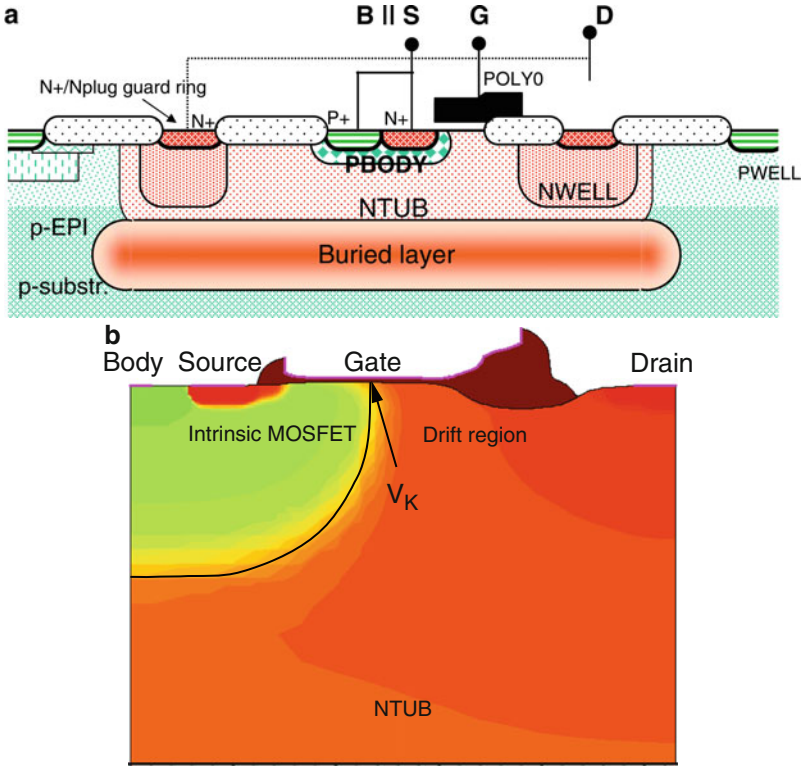

Fig. 4.2 (**a**) Schematic representation and (**b**) device architecture of 40 V SOI-LDMOS transistor from I2T100 AMIS technology. The separation boundary between the intrinsic MOSFET and the drift region is the metallurgical junction of the PIN diode

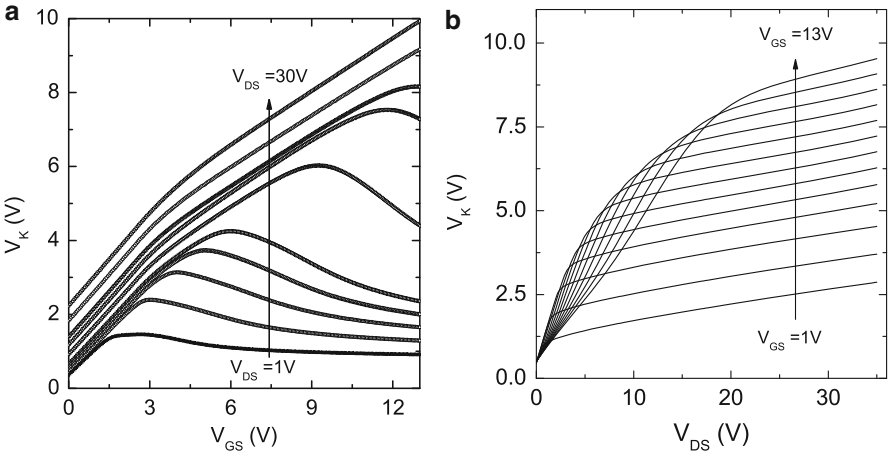

Fig. 4.3 Behavior of intrinsic drain potential (V_K) from numerical device simulation: (**a**) Plot of V_K vs. V_{GS}. (**b**) Plot of V_K vs. V_{DS}

which is also the desired feature. Second, the V_K behavior is quite different in the linear region while it saturates or varies slowly at higher drain voltages. This analysis also points out the importance of the modeling of the drift region in the linear region.

2 General Drift Resistance Model

Figure 4.4a, b shows the schematics of high voltage VDMOS and LDMOS devices, respectively. Even though, simple device architectures are shown here, the model can be used, as described earlier, for any HV device which uses extended drift region to handle the high voltage applied at the drain terminal e.g. LDMOS with thin or thick oxide (shown in Fig. 4.2a) etc.

As discussed in the previous chapter, the intrinsic drain voltage (V_K) always remains at low values for entire bias domain [13]. Based on this understanding, we consider our device divided into an intrinsic MOSFET region and a drift region, where the intrinsic transistor part is modeled by using low voltage EKV model [3] described in the next section while modeling of drift region is carried out by using bias dependent resistance explained below. The motivation to use a resistance to model the drift region is to get the fast convergence along with excellent accuracy. The simplest resistance expression could be a constant resistance. Figure 4.5 shows the transfer characteristics ($I_{DS} - V_{GS}$) using constant resistance (dash lines) as drift resistance. It can be seen that the constant resistance accurately models the low drain and low to medium gate bias behavior, as at low drain bias, the intrinsic transistor drives the current while the drift region behaves like a constant resistor. Another interesting remark is that the fixed resistance cannot model the behavior of the device at low V_{DS}, when high gate voltage is applied. The explanation for this deviation comes from the accumulation charge sheet, which extends into the drift region with the increase of the gate voltage and lowers the resistance of the drift part. In order

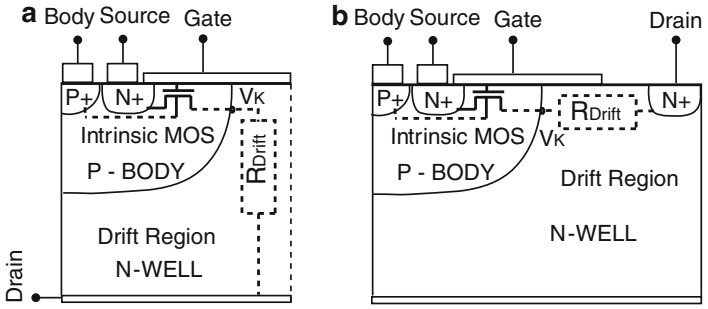

Fig. 4.4 Schematic representation of high voltage (**a**) Vertical DMOS (VDMOS) and (**b**) Lateral DMOS (LDMOS) device Architecture

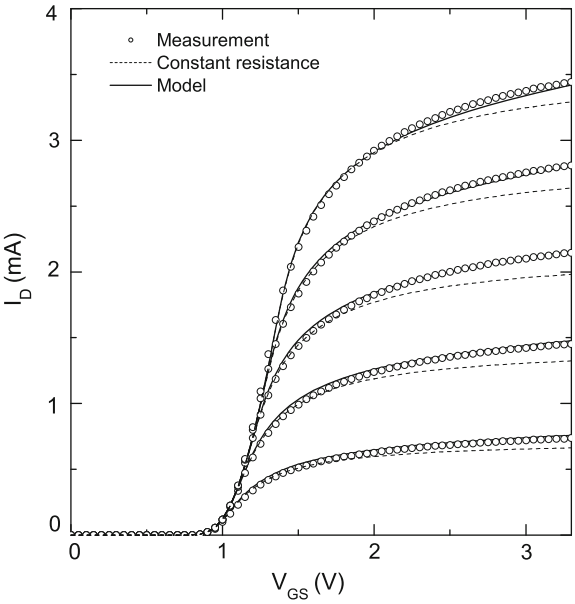

Fig. 4.5 I_{DS} vs. V_{GS} for $V_{DS} = 0.1$ to 0.5 V for 50 V VDMOS transistor. The constant resistance along with the accumulation charge sheet effect provides excellent accuracy at low drain bias

to simulate the above described effect, a slight reduction of the drift resistance with the gate voltage is introduced in the model:

$$R_{Drift} = \frac{R}{1 + \theta_{Acc} \cdot |V_{GS}|} \tag{4.1}$$

where R is the constant resistance, θ_{Acc} is the gate bias modulation parameter (effect of accumulation charge sheet on R_{Drift}) and V_{GS} is the applied gate voltage. The value of R can be obtained by extracting the silicon resistivity and then calculating the global resistance function of the geometrical dimensions, if the doping concentration of the drift zone is known. The model behavior using (4.1) is shown in Fig. 4.5 by solid lines. It can be observed that the matching between the simulation and measured data is excellent. Thus, it can be concluded that (4.1) correctly reproduces the physics inside the device. Moreover, this expression proves to be highly efficient in terms of implementation as it uses the simplest representation and the minimum number of parameters for the description of the physical phenomenon at low gate and drain bias. Figure 4.6 shows the $I_{DS} - V_{DS}$ characteristics using drift resistance derived above by dash lines. It is easily observable that even though above derived expression showed excellent characteristics at low V_{DS}, it is not working well at higher V_{DS}. It is also important to mention that once the current saturates in the intrinsic MOS transistor, the drift part has no influence on the current. Consequently, the drift part only affects the linear regime of the output characteristics. Although, this influence seems to be limited, the transition from

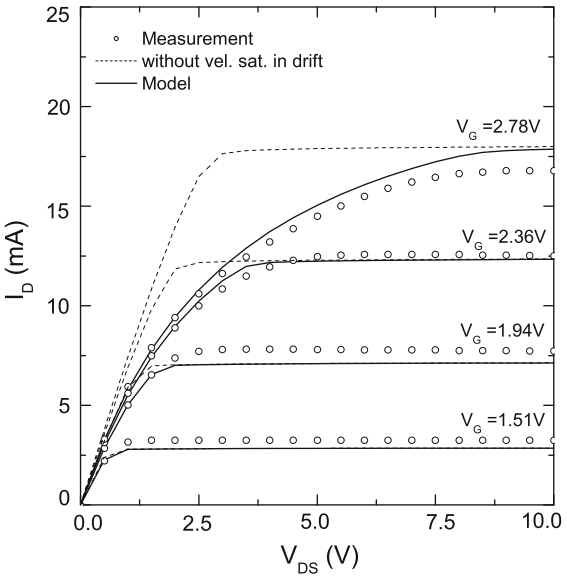

Fig. 4.6 I_{DS} vs. V_{DS} for 50 V VDMOS transistor. The modeling of velocity saturation effect on drift resistance provides good behavior in the linear region

linear to saturation is very sensitive to the drift resistance variation. The delayed transition between linear and saturation regime at high gate voltages occurs due to the carrier velocity saturation in the drift and is equivalent to an increase in the resistance of the drift region. In literature, the carrier velocity saturation effect on the current is modeled using hyperbolic dependence of the electric field across the region. It means that this dependence would be linear for the resistance. Thus, in order to simulate the carrier velocity saturation dependence using the drift resistance expression, a direct dependence on the field applied in the drift region is introduced as

$$R_{Drift} = R \cdot \left[\frac{1 + \left(\frac{V_{DS} - V_K}{VSAT * L_{DR}} \right)^{\alpha_{vsat}}}{1 + \theta_{Acc} \cdot |V_{GS}|} \right] \tag{4.2}$$

where $VSAT$ and α_{vsat} are the velocity saturation parameters. L_{DR} is the length of the drift region. The mobility is considered constant all over the current path and the electric field uniformly distributed along the length of the drift region. Solid lines in Fig. 4.6 show the drain current using (4.2), which proves that this expression takes into account major physical phenomena in the drift region.

The final expression for the drift resistance including geometry and temperature effects can be written as [1, 2]:

$$R_{Drift} = R_{Drift0} \cdot \left[\frac{1 + \left(\frac{V_{DS} - V_K}{VSAT * L_{DR}} \right)^{\alpha_{vsat}}}{1 + \theta_{Acc} \cdot |V_{GS}|} \right] \cdot (1 + \alpha_{vsb} \cdot V_{SB}) \cdot (1 + \alpha_T \cdot \Delta T) \tag{4.3}$$

where R_{Drift0} is the value of the drift resistance at low bias voltage defined as

$$R_{Drift0} = \rho_{Drift} \cdot \left[\frac{L_{DR}}{(W + \Delta W) \cdot N_F}\right] \cdot \left[1 \pm (k_{rd} - 1) \cdot \left(\frac{N_F - 1}{N_F + N_{CRIT}}\right)\right] \quad (4.4)$$

Where ρ_{Drift} is the resistivity per unit length at room temperature ($T = 300$K). W, ΔW and N_F represent the width, width offset and number of fingers respectively. N_{CRIT} and k_{rd} are the parameters for drift scaling with number of fingers. The α_{vsb} is a parameter used for modeling of drift resistance with body bias. The "+" sign is used for drain-on-side devices while "−" sign is used for drain-all-around devices. α_T is the temperature coefficient of the drift region and ΔT is the difference in ambient temperature with normal room temperature ($T = 300$K).

3 Charge Evaluation Based on EKV Model

The main reason behind using EKV MOSFET model [3] for intrinsic channel is that EKV model has physical expressions for current and charges, which are continuous from weak to moderate to strong inversion. Another important characteristic of the EKV model is that compared with other existing MOS models (e.g. BSIM), it uses less number of parameters, most of which are all physical. The intrinsic drain-to-source current (V_K to V_S in our model) in EKV model is given as

$$I_{KS} = I_S(i_f - i_r) \quad (4.5)$$

where I_S is the specific current [3] defined as

$$I_S = 2 \cdot n \cdot \beta \cdot U_T^2 \quad (4.6)$$

$$n = \frac{1}{1 - \frac{\gamma}{2 \cdot \sqrt{V_{GS} - V_T + (\frac{\gamma}{2} + \sqrt{\psi_0})^2}}} \quad (4.7)$$

$$\psi_0 = 2\phi_F + several\ U_T \quad (4.8)$$

$$\beta = \mu \cdot C_{ox} \cdot \frac{W}{L} \quad (4.9)$$

where $U_T = \frac{kT}{q}$ is the thermal voltage, n is the slope factor, V_T is the threshold voltage, γ is the body effect parameter and, C_{ox} is the oxide capacitance per unit area. The normalized forward current i_f and normalized reverse current i_r are defined as

$$i_f = \left[ln\left(1 + e^{\frac{v_p - v_S}{2}}\right)\right]^2, \quad (4.10)$$

and

$$i_r = \left[ln\left(1 + e^{\frac{v_p - v_K}{2}}\right)\right]^2, \quad (4.11)$$

where $v_p = \frac{V_P}{U_T}, v_s = \frac{V_S}{U_T}, v_k = \frac{V_K}{U_T}$ are the normalized pinch-off $\left(V_P = \frac{V_{GS}-V_T}{n}\right)$, source and intrinsic drain voltage, respectively [3].

The total gate charge is the sum of the charges related to intrinsic-drain (V_K), source, body and drift. The charges associated with the intrinsic MOS are directly obtained from EKV model [3].

The R_{Drift} expression (4.3) used above for current modeling does not provide the correct behavior for intrinsic drain voltage (V_K) at low-gate/high-drain biases, as this resistance in actual case should rise to Giga-ohm at low-gate/high-drain biases. The preceding statement is verified by the fact that at low gate bias, the drift region is in depletion and most of the voltage drop applied on drain terminal occurs in this region and the current is very small. But this resistance provides accurate current prediction because at low-gate/high-drain bias (intrinsic MOS in saturation), the current is well modeled by the intrinsic MOS part. The impact of the intrinsic drain potential (V_K) on AC characteristics was shown by Hefyene et al. [14, 15]. The correct V_K behavior is not only important for the peaks of capacitances which are very specific to high voltage devices, it is also extremely important for the position of the peaks with gate and drain bias. Thus it is extremely important to first obtain the correct V_K behavior with gate and drain bias. In literature, this is obtained using interpolation between V_K in the linear region and V_{Ksat} in the saturation region to limit the value of V_K to V_{Ksat} [16]. In this work, the accurate V_K value, which is used in the calculation of accumulation charge, can be obtained by backtracking of K-node charge as given below. The motivation for this strategy is to get the impact of current saturation on charge and then on V_K.

The V_K behavior which has great impact on capacitance of high voltage devices [14,15], is obtained by backtracking of K-node charge or current backtracking [4, 17]. The normalized potential v_k is expressed as a function of v_p and q_k (normalized inversion charge density at V_K) as [17]

$$v_k = v_p - (2 \cdot q_k + \ln q_k) \tag{4.12}$$

where q_k is expressed as [17]

$$q_k = \sqrt{i_r + 0.25} - 0.5. \tag{4.13}$$

Thus V_K can be easily expressed as

$$V_K = U_T \cdot \left[v_p - \left\{2 \cdot \left(\sqrt{i_r + 0.25} - 0.5\right) + \ln\left(\sqrt{i_r + 0.25} - 0.5\right)\right\}\right] \tag{4.14}$$

The intrinsic drain potential (V_K) behavior obtained by this method shows excellent agreement with literature [18] (see Figs. 4.7 and 4.8).

The normalized drift accumulation charge density can be written as

$$q_{drift} = v_g - v_{fb\_drift} - \psi_{s\_drift}. \tag{4.15}$$

where v_{fb_drift} is the normalized flat-band voltage of drift region and ψ_{s_drift} is the normalized surface potential in the drift region. The total drift accumulation charge

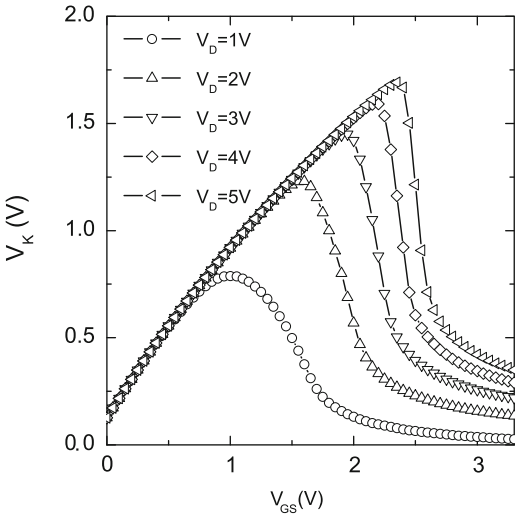

Fig. 4.7 Intrinsic-drain potential V_K vs. V_{GS} for $V_{DS} = 1$ to 5 V in steps of 1 V for VDMOS transistor. The decrease in V_K is caused by drift region

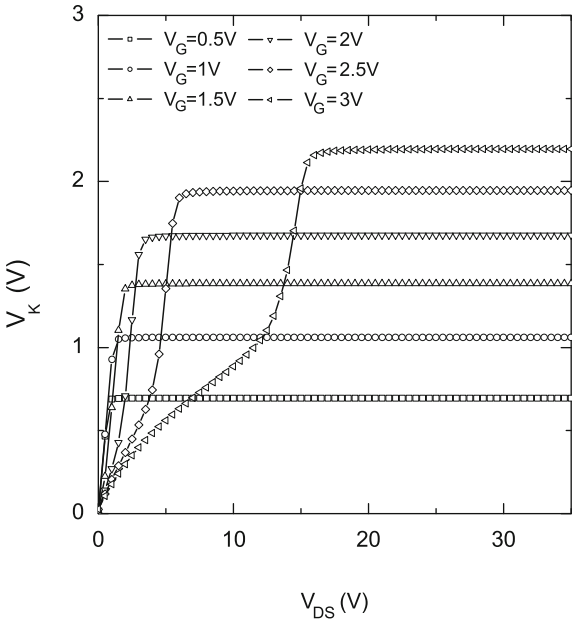

Fig. 4.8 Intrinsic-drain potential V_K vs. V_{DS} for $V_{GS} = 0.5$ to 3 V in steps of 0.5 V for VDMOS transistor

is obtained by integrating the drift charge density over the gate overlap length, assuming ψ_{s_drift} varies linearly in the drift region also validated from numerical device simulation.

Thus total gate charge can be written as,

$$Q_G = Q_S + Q_K + Q_B + Q_{Drift}, \tag{4.16}$$

where Q_S, Q_K and Q_B are the charges related to source, intrinsic drain and body node respectively, obtained from EKV MOS model [3].

The capacitances are defined using standard method as

$$C_{ij} = \begin{cases} -\dfrac{\delta Q_i}{\delta V_j} & i \neq j \\ +\dfrac{\delta Q_i}{\delta V_j} & i = j \end{cases}$$

4 Modeling of Quasi-Saturation and Self-Heating Effects

As discussed in the previous chapter, the high voltage devices show some special effects due to high electric field inside the device e.g. self-heating, quasi-saturation and impact ionization effects. In fact some of these effects (self-heating and impact ionization) are also visible in low voltage MOSFETs as electric field in these devices also becomes quite high as channel length is decreased. Here we will discuss the modeling of these effects.

4.1 Quasi-Saturation Effect

The quasi-saturation effect is one of the unique effects observed in HV devices. This effect originates due to velocity saturation in the drift region when intrinsic MOS is still not saturated. If drift is velocity saturated and intrinsic MOS is in linear region, the increase in V_{GS} does not increase current levels significantly and gate bias has little effect. As our drift resistance already includes the velocity saturation in the drift, the quasi-saturation effect is easily modeled by this model.

4.2 Self-Heating Effect

The self-heating effect (SHE) represents the heating of the device due to its internal power dissipation. This effect appears when high levels of power are attained in the device. The dissipated heat leads to an increase in the internal temperature of the device. The internal temperature increase influences the device characteristics mainly by affecting the mobility, threshold voltage and velocity saturation. In the literature, this effect was mainly studied on the SOI devices and the proposed models for SHE are distributed or non-distributed models. As expected, better accuracy was obtained from distributed models, which offer a larger flexibility for the current simulation. Still, the clear advantage of the non-distributed models over the distributed ones is the parameter extraction procedure, as non-distributed approach offers a simple and

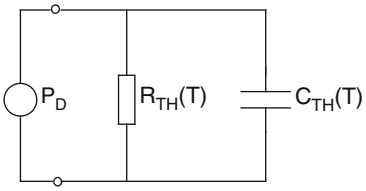

Fig. 4.9 Representation of the electro-thermal circuit for self-heating effect simulation (Power dissipation $P_D = I_{DS}V_{DS}$, thermal resistance $R_{TH}(\mathrm{T}) = R_{THNOM}(1 + \alpha\Delta T)$ and thermal capacitance $C_{TH} = f(R_{TH}, \tau_w)$) [19,20]

efficient representation of the problem. Figure 4.9 shows the equivalent sub-circuit used for the self-heating representation. This classical representation can be used for the DC, AC or transient simulation of the device in some critical regimes (other than analog operation).

In our model, the SHE is modeled using standard circuit shown in Fig. 4.9, where the thermal resistance (R_{TH}) and thermal capacitance (C_{TH}) varies dynamically with the device temperature [19,20]. The extraction procedure for R_{TH} and C_{TH} has been discussed in [19, 20]. The expressions for thermal resistance and capacitance from [19,20] are re-written here to complete this discussion.

The thermal resistance is expressed as [19,20]

$$R_{TH} = R_{THNOM}(T_e) \cdot [1 + \alpha \cdot (T_i - T_e)] \tag{4.17}$$

where T_e, T_i are the ambient and internal device temperatures, respectively and R_{THNOM} is also considered a linear function of the ambient temperature as follows:

$$R_{THNOM}(T_e) = R_{THNOM}(300K) \cdot [1 + \alpha \cdot (T_e - 300K)] \tag{4.18}$$

One should note that in (4.17), the temperature increase, $\Delta T = T_i - T_e$, at known ambient temperature is essentially given by SHE (related to the injected electrical power P_D), and consequently, R_{THNOM} could be considered as the nominal thermal resistance at zero injected power (at given ambient temperature T_e). The thermal capacitance $C_{TH} = f(R_{TH}, \tau_w)$ and temperature coefficient of thermal resistance α are extracted from $I_{DS} - V_{DS}$ characteristics for different pulse widths τ_w [19,20].

4.3 Impact Ionization Effect

When the drain bias across the device increases, the electric field in the drift region also increases as a function drain bias. In this high field zone, the longitudinal electric field varies linearly and reaches its peak value at the drain junction. The impact ionization current (or avalanche current) can be expressed as

$$I_{avl} = (M - 1) \cdot I_D \tag{4.19}$$

Where M is called as Multiplication factor. Rossel et al. [21] developed the following approximate expression for M from impact ionization integral assuming low multiplication level.

$$M - 1 \simeq 1 - \frac{1}{M} = (2.8 \cdot 10^{-73}) \cdot N_{eff}^3 \cdot V_{DS}^4 \tag{4.20}$$

In the model implementation, we combined the constant $(2.8 \cdot 10^{-73})$ with N_{eff} and used a single parameter N_{EFF}. Thus multiplication factor M can be written as:

$$M - 1 = N_{EFF}^3 \cdot V_{DS}^4 \tag{4.21}$$

5 Model Validation and Results

This model is calibrated on the measured characteristics of a 50 V VDMOS and 40 V LDMOS devices provided by AMIS and BOSCH [6, 7]. The source and body are tied to avoid parasitic bipolar transistor for all measurements.

5.1 Case Study 1: VDMOS Transistor

The schematic representation of the VDMOS device (half of the device is shown as it is symmetrical along the vertical axis) under study is shown in Fig. 4.4a. Figure 4.10a shows the transfer characteristics for low drain bias, which demonstrates that the model provides accurate simulation of current and subthreshold slope. From Fig. 4.10b, it can be observed that the model not only gives accurate values of peak in transconductance and its slope in the subthreshold regime but also predicts the correct behavior after the peak, which is very important in circuit design. Figure 4.11 shows the transfer characteristics for medium drain bias ($V_{DS} = 1 - 5$ V in steps of 1 V). The drain current at higher gate voltages is heavily affected by the drift region. Figure 4.12a, b shows the output characteristics and output-conductance, respectively, for different gate bias which show that not only the transition from linear to saturation regime in I_{DS} is well simulated by the model, validating correct drift model, it also correctly simulates the self-heating effect in the output characteristics. The dips in output-conductance are also well predicted by the model. The first dip in $|g_{ds}|$ originates from self-heating effect, while second dip is caused by impact ionization effect. Capacitances C_{GD} and $C_{GS} + C_{GB}$ obtained using this model, are shown in Fig. 4.13a, b, respectively. The special behavior of the high voltage capacitances, i.e. the peaks [15, 24] in C_{GD} and C_{GS} are well modeled. It can be seen that all the capacitances show good trend for the entire gate and drain bias range. It should be noted that in literature very few models have been successful in modeling the correct behavior of capacitances of HVMOS

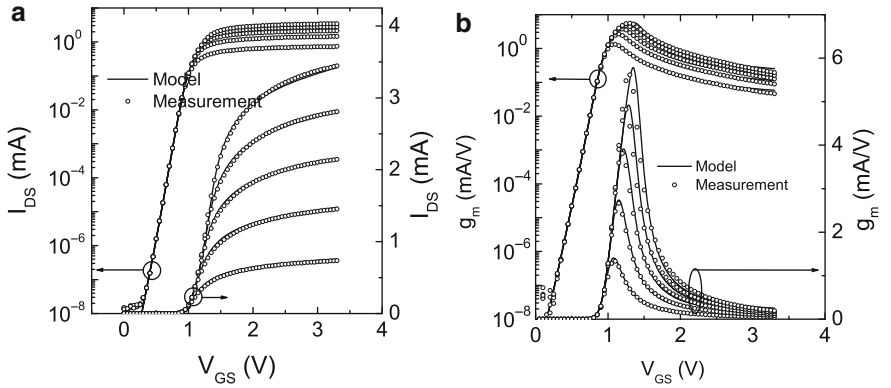

Fig. 4.10 Transfer characteristics of VDMOS transistor at low drain bias for $W = 40\,\mu\text{m}$, $L = 0.6\mu\text{m}$ and $N_F = 2$ at $T = 30°\text{C}$: (**a**) $I_{DS} - V_{GS}$ for $\text{V}_{DS} = 0.1 - 0.5\,\text{V}$ in steps of 0.1 V. The current at higher V_{GS} is heavily affected by drift region. (**b**) $g_m - V_{GS}$ for $\text{V}_{DS} = 0.1 - 0.5\,\text{V}$ in steps of 0.1 V. The sharp decrease in transconductance at higher gate bias can be explained by the dominance of drift resistance over channel resistance

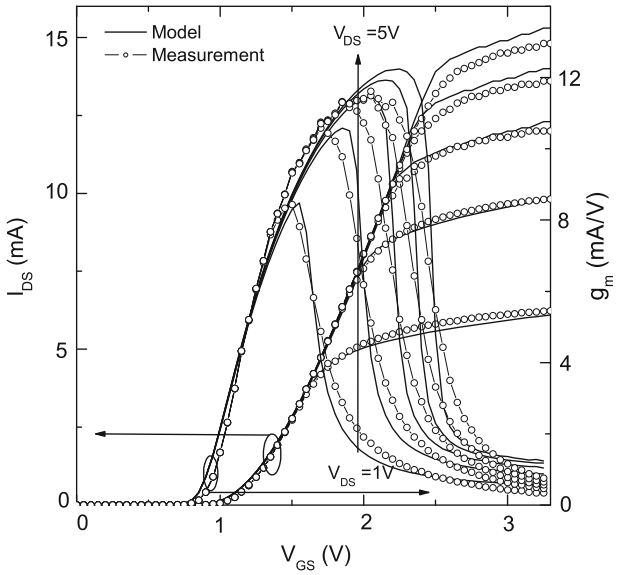

Fig. 4.11 Transfer characteristics at medium drain bias for $W = 40\,\mu\text{m}$, $L = 0.6\,\mu\text{m}$ and $N_F = 2$ at $T = 30°\text{C}$: I_{DS} and $g_m - V_{GS}$ for $\text{V}_{DS} = 1 - 5\,\text{V}$ in steps of 1 V for VDMOS transistor

devices [1, 2, 8, 24, 25]. Furthermore the accuracy on capacitances can be improved by modeling the lateral non-uniform doping in the intrinsic MOS channel of high voltage devices [12, 22, 23]. The modeling of lateral non-uniform doping will be discussed in the next chapter.

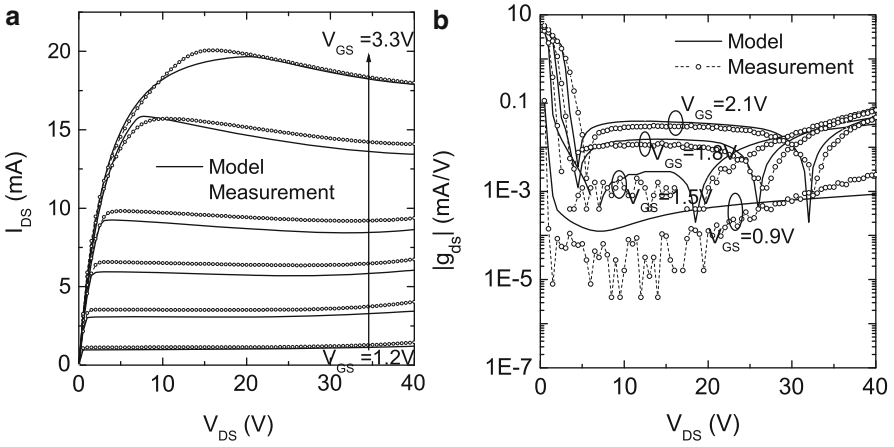

Fig. 4.12 Output characteristics of VDMOS transistor for $W = 40\,\mu\text{m}$, $L = 0.6\,\mu\text{m}$ and $N_F = 2$ at $T = 30°\text{C}$ (**a**) I_{DS} vs. V_{DS} for $V_{GS} = 1.2$, 1.5, 1.8, 2.1, 2.7 and 3.3 V. Note self-heating effect (decrease in I_{DS} with increase in V_{DS}) is correctly simulated. The discrepancy in the curves can be explained by the simultaneous optimization of drift resistance, self-heating effect, impact ionization effect and velocity saturation in MOSFET at high V_{DS}. (**b**) $|g_{ds}|$ vs. V_{DS}. Note peaks in output-conductances are correctly matched. The first dip in $|g_{ds}|$ originates from self-heating effect, while second dip is caused by impact ionization effect

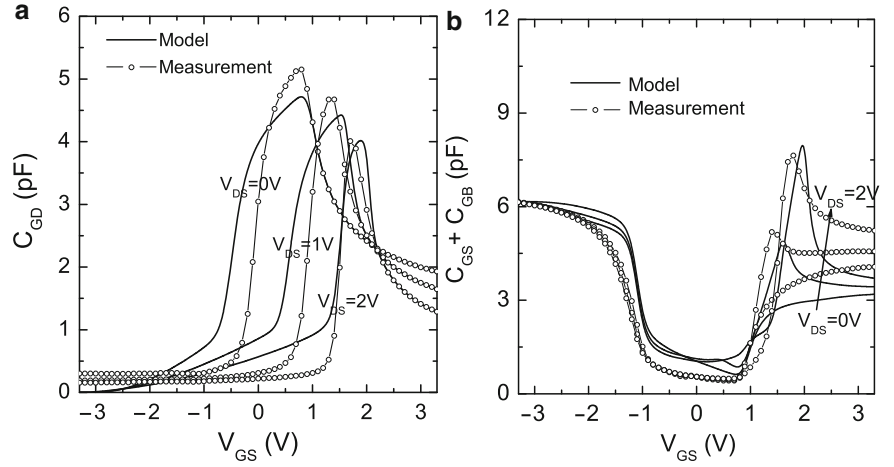

Fig. 4.13 (**a**) C_{GD} vs. V_{GS} and (**b**) $C_{GS} + C_{GB}$ vs. V_{GS} of VDMOS transistor for $V_{DS} = 0$, 1, and 2 V. The sharp decrease in C_{GD} at higher V_{GS} is heavily affected by drift region. The discrepancy in the curves is due to assumption of constant doping in the channel and simplified drift charge evaluation. The accuracy on capacitances can be improved by modeling the lateral non-uniform doping present in the intrinsic MOS channel [12, 15, 22, 23]

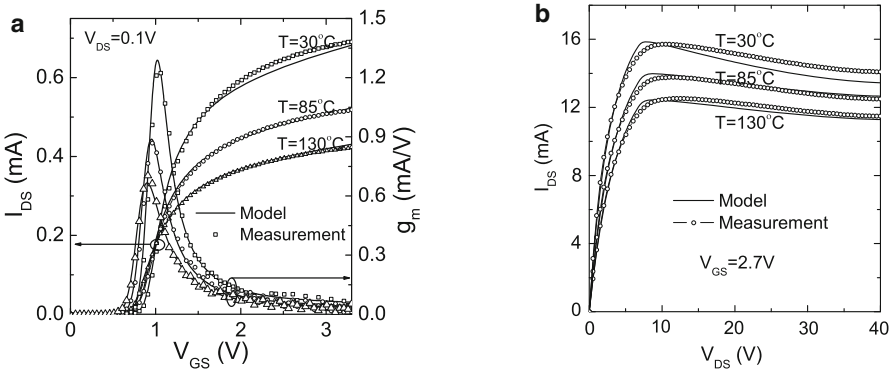

Fig. 4.14 Demonstration of temperature scaling of VDMOS transistor for $W = 40\,\mu$m, $L = 0.6\,\mu$m and $N_F = 2$: (**a**) $I_{DS} - V_{GS}$ and $g_m - V_{GS}$ at $T = 30°$C, 85°C and 130°C. Note, the change in threshold voltage with temperature and peak in transconductance are correctly modeled. The ZTC-point [26, 27] is also well simulated. (**b**) $I_{DS} - V_{DS}$ at $T = 30°$C, 85°C and 130°C. Note self-heating effect is very well modeled at different temperatures. The decrease in slope in the linear region is caused by the increase in drift resistance with temperature

Model Scalability: An important characteristic of any model is the scalability with physical and electrical parameters. Figure 4.14a shows the I_{DS} and $g_m - V_{GS}$ characteristics for different temperatures. It can be seen that the model correctly simulates the variation of drain current, transconductance and most importantly the threshold voltage shift with temperature. An important observation is that ZTC (Zero-Temperature-Coefficient) point [26–30] is also well modeled in Fig. 4.14a. Figure 4.14b shows the $I_{DS} - V_{DS}$ curves for different temperatures, which demonstrates that the SHE is correctly modeled for entire temperature range. The scaling of the model is also tested for different device geometries. The transfer and output characteristics shown in Fig. 4.15a, b, respectively, demonstrate that the model scales well with different transistor widths. Note that the self-heating effect is more prominent for higher widths due to increased power dissipation. The variation of ON resistance (R_{ON}) with number of fingers (N_F) is modeled using k_{rd} and N_{CRIT} parameters in (4.3). Figure 4.16a shows that the R_{ON} scaling with N_F is well modeled for different widths for *drain-all-around* device. The decrease of R_{ON} with number of fingers for *drain-all-around* device is caused by current spreading at the finger edges. Figure 4.16b shows the R_{ON} scaling with N_F for *drain-on-side* device. The increase in R_{ON} with number of fingers for *drain-on-side* device is caused by the interaction of depletion regions of the neighborhood fingers. The R_{ON} scalability with temperature is shown in Fig. 4.17 for different transistor widths. It can be seen that the increase in R_{ON} with temperature is excellently modeled for different transistor widths.

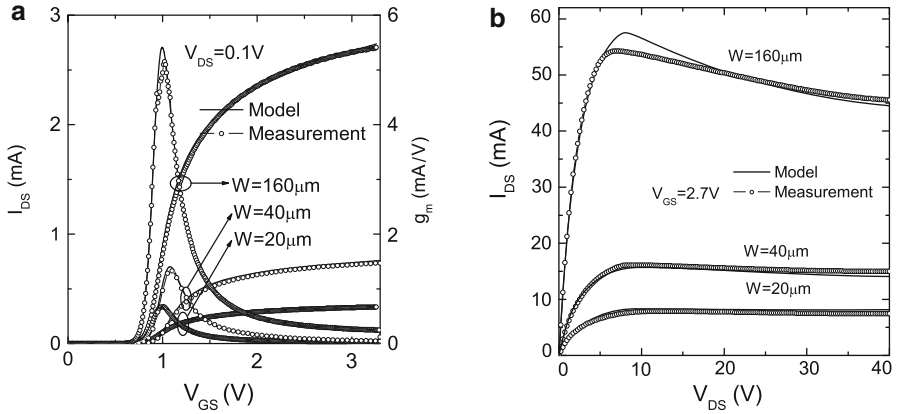

Fig. 4.15 Demonstration of width scaling of VDMOS transistor for $W = 20\,\mu\text{m}, 40\,\mu\text{m}, 160\,\mu\text{m}$, $L = 0.6\,\mu\text{m}$ and $N_F = 2$ at $T = 30°\text{C}$: (**a**) $I_{DS}-V_{GS}$ and g_m-V_{GS} for $\text{V}_{DS} = 0.1\,\text{V}$. (**b**) $I_{DS}-V_{DS}$ for $V_{GS} = 2.7\,\text{V}$. The self-heating effect is more prominent for higher widths due to increased power dissipation

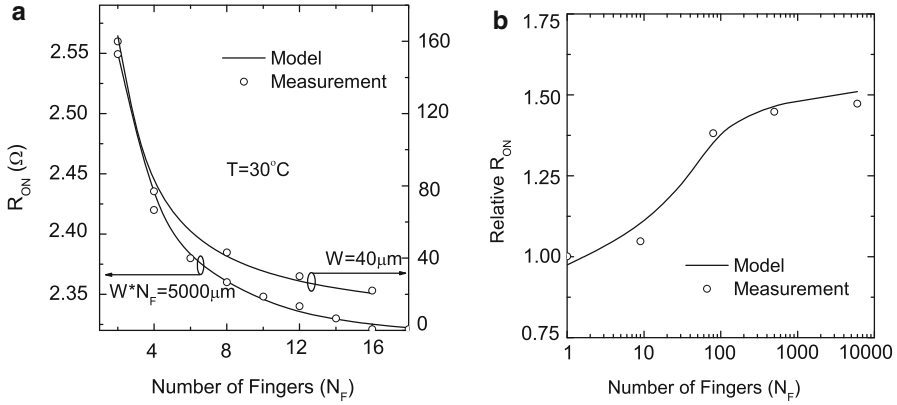

Fig. 4.16 (**a**) R_{ON} with Number of fingers (N_F) for $W = 40\,\mu\text{m}$ and $W \cdot N_F = 5000\,\mu\text{m}$ at $\text{V}_{GS} = 3.3\,\text{V}$ and $\text{V}_{DS} = 0.5\,\text{V}$ for *drain-all-around* VDMOS transistor at $T = 30°\text{C}$. The decrease of R_{ON} with number of fingers for *drain-all-around* device is caused by current spreading at the finger edges. (**b**) Relative On-resistance $\frac{R_{ON}}{R_{ON}|_{N_F=1}}$ with Number of fingers (N_F) for *drain-on-side* VDMOS transistor. The increase in R_{ON} with number of fingers for *drain-on-side* device is caused by the interaction of depletion regions of the neighborhood fingers

5.2 Case Study 2: LDMOS Transistor

The LDMOS devices (FND40 and FND100) used for the validation of the model are obtained from I2T100 AMIS Technology. The schematic representation of the LDMOS device under study is shown in Fig. 4.4b while device architecture of FND40

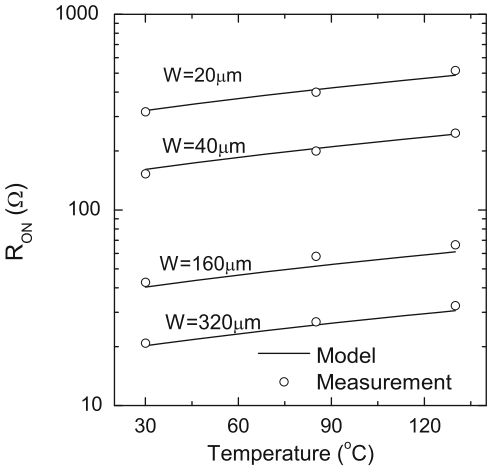

Fig. 4.17 R_{ON} variation with temperature for $N_F = 2$ and $W = 20\,\mu$m, $40\,\mu$m, $160\,\mu$m, $320\,\mu$m for VDMOS transistor

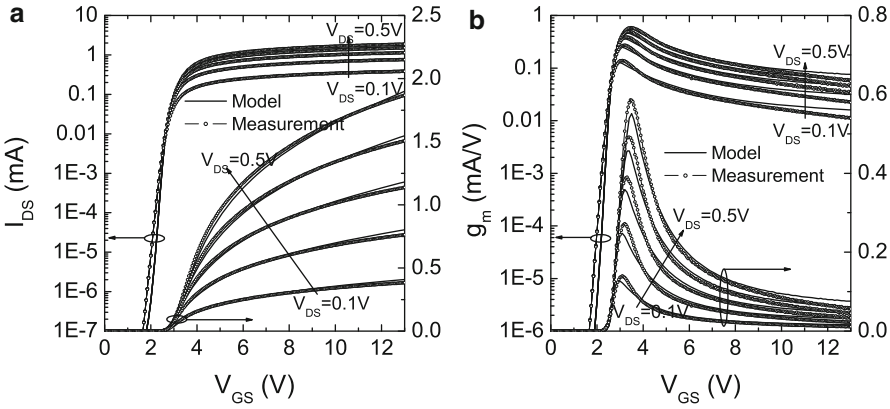

Fig. 4.18 Transfer characteristics of 40 V LDMOS device ($W = 40\,\mu$m, $L = 1.2\,\mu$m and $N_F = 1$ at $T = 30°$C): (**a**) $I_{DS} - V_{GS}$ and (**b**) $g_m - V_{GS}$ for $V_{DS} = 0.1 - 0.5$ V in steps of 0.1 V

device is shown in Fig. 4.2. Figure 4.18a, b shows the $I_{DS} - V_{GS}$ and $g_m - V_{GS}$ for $V_{DS} = 0.1{-}0.5$ V, respectively. Figures 4.19 and 4.20 show the I_{DS} and $g_m - V_{GS}$ for $V_{DS} = 1 - 5$ V, and $I_{DS} - V_{DS}$ characteristics respectively for 40 V LDMOS, which demonstrate that the model provides correct simulation of current and transconductance for different bias conditions. The gate-to-drain and gate-to-gate capacitance curves shown in Fig. 4.21a, b, respectively demonstrate that the model predicts correct trend for capacitances. Furthermore the accuracy on capacitances can be improved by modeling the lateral non-uniform doping in the intrinsic MOS channel of high voltage devices [12, 22, 23]. The modeling of lateral non-uniform doping will be discussed in the next chapter.

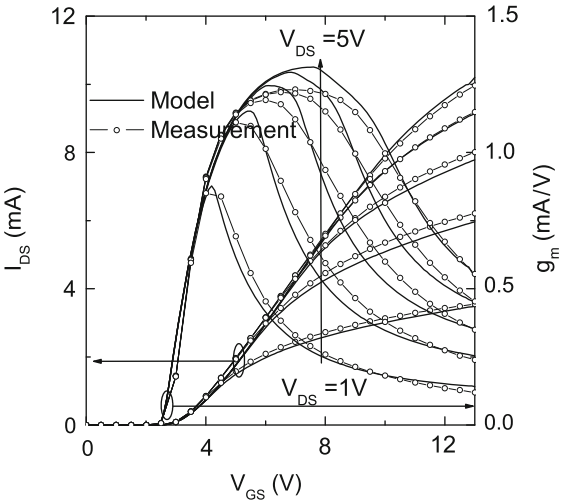

Fig. 4.19 Transfer characteristics of 40 V LDMOS device ($W = 40\,\mu$m, $L = 1.2\,\mu$m and $N_F = 1$): $I_{DS} - V_{GS}$ for $V_{DS} = 1 - 5$ V in steps of 1 V at $T = 30°$C

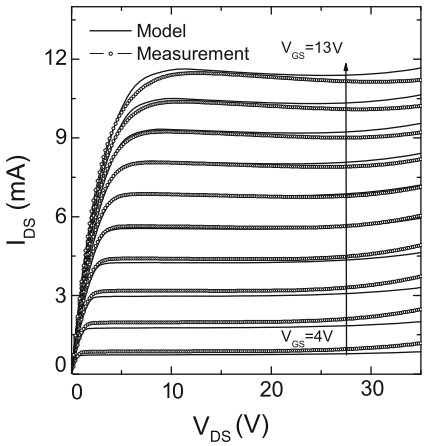

Fig. 4.20 Output characteristics: $I_{DS} - V_{DS}$ of 40 V LDMOS device ($W = 40\,\mu$m, $L = 1.2\,\mu$m and $N_F = 1$) at $T = 30°$C. Note, the self-heating and impact ionization effects are correctly simulated

Model Scalability: An important issue in any LDMOS model is the scalability with drift length for different voltage handling capability. Figure 4.22a, b show the transfer and output characteristics, respectively, of a 100 V LDMOS transistor (FND100 device) on the same technology (as of FND40), which demonstrates that the model scales well with drift length. It should be noted that not only the self-heating effect [20] is well modeled in Fig. 4.22b but also the quasi-saturation effect observed at higher gate biases. The 100 V LDMOS transistor (FND100) has longer drift length, in comparison to 40 V LDMOS transistor (FND40), to handle the higher drain voltages at drain terminal. The scalability of the model is also tested for R_{ON} for different widths of LDMOS device. Figure 4.23 shows the R_{ON} versus V_{GS} for three different widths of 40 V LDMOS device.

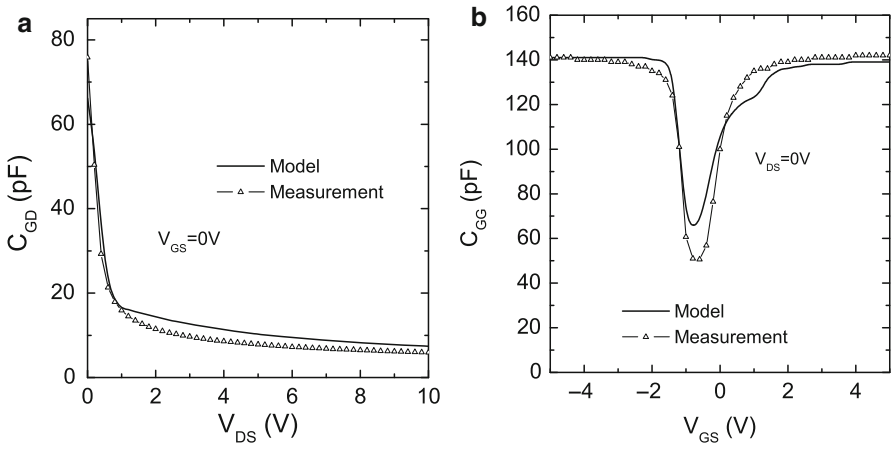

Fig. 4.21 (**a**) Plot of C_{GD} versus V_{DS} at $V_{GS} = 0$ V for 40 V Bosch LDMOS device. (**b**) Plot of C_{GG} versus V_{GS} at $V_{DS} = 0$ V for 40 V Bosch LDMOS device

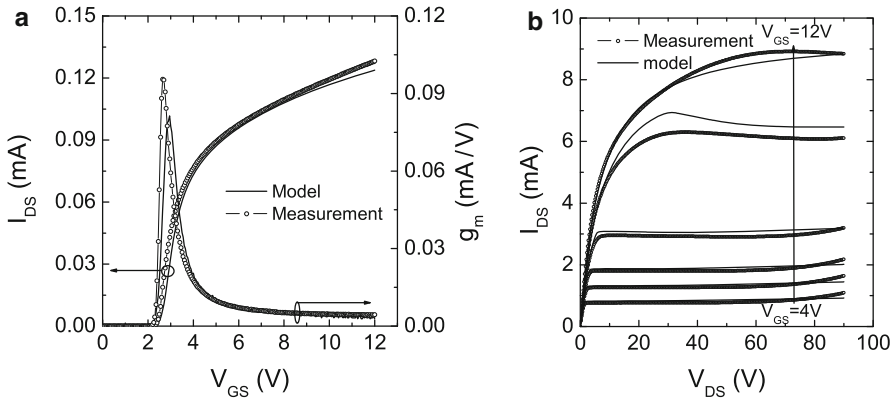

Fig. 4.22 Drift scaling ($W = 40\,\mu$m, $L = 1.2\,\mu$m and $N_F = 1$ at $T = 30°$C): (**a**) $I_{DS} - V_{GS}$ and $g_m - V_{GS}$ at $V_{DS} = 0.1$ V, (**b**) $I_{DS} - V_{DS}$ for $V_{GS} = 4, 4.5, 5, 6, 9$ and 12 V for 100 V LDMOS device

5.3 Case Study 3: SOI – LDMOS Device

Figure 4.24 shows the device architectures of SOI-LDMOS transistor [31] on AMIS technology.

The proposed model is also validated on the measured characteristics of SOI-LDMOS transistor from I2T100 AMIS technology. It should be noted that the model is same for all devices, thus showing the versatility of the model and hence called *general model*. Figure 4.25 shows the $I_{DS} - V_{GS}$ and $g_m - V_{GS}$ characteristics for $V_{DS} = 0.1 - 0.5$ V in steps of 0.1 V. Figure 4.26a, b shows the output characteristics

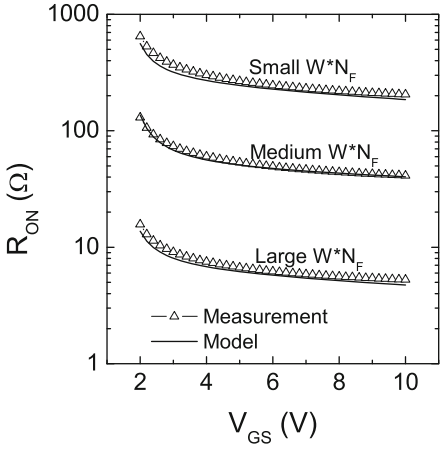

Fig. 4.23 Width scaling: R_{ON} versus V_{GS} for three different $W * N_F$ for 40 V LDMOS device at $T = 30°C$

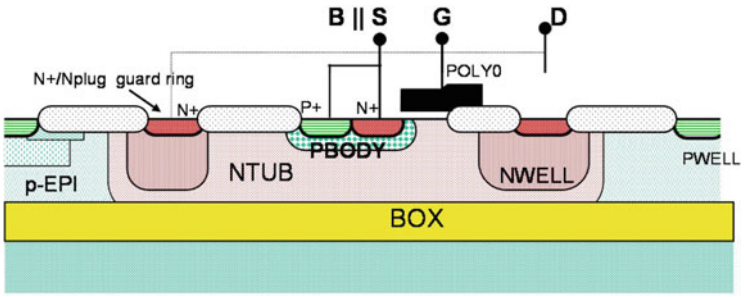

Fig. 4.24 Schematic representation of 40 V SOI-LDMOS transistor from I2T100 AMIS technology

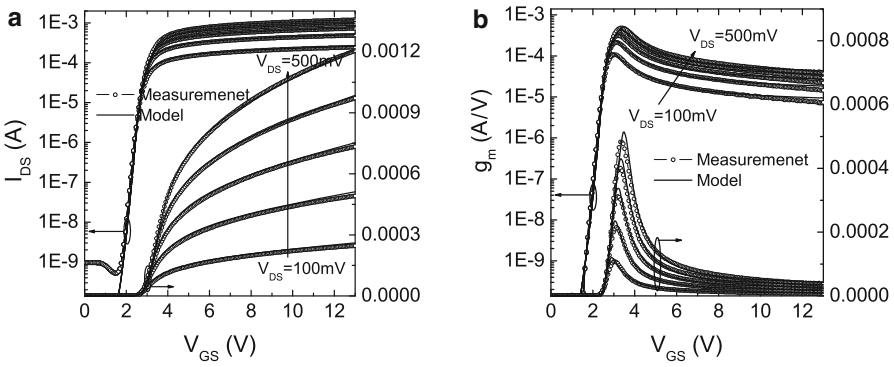

Fig. 4.25 Transfer characteristics of 40 V SOI-LDMOS transistor from I2T100 AMIS technology ($W = 40\,\mu m$, $L = 1.2\,\mu m$): (**a**) $I_{DS} - V_{GS}$ and (**b**) $g_m - V_{GS}$ for $V_{DS} = 0.1 - 0.5$ V in steps of 0.1 V. Note that, the value and position of the peaks on g_m has been modeled very well

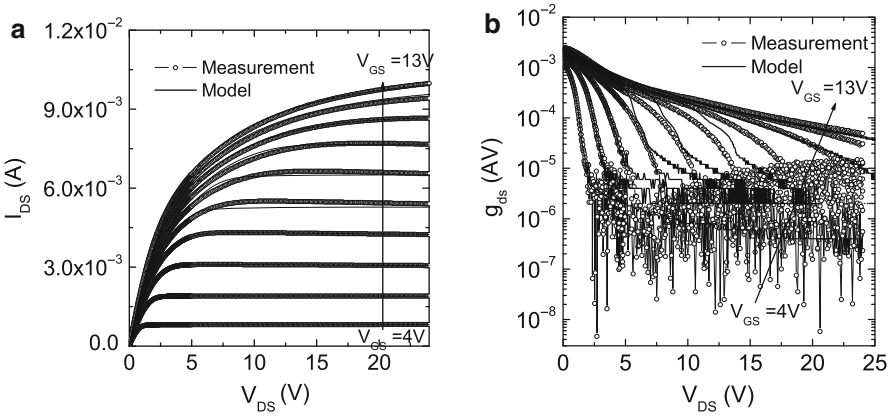

Fig. 4.26 Output characteristics of 40 V SOI-LDMOS transistor on I2T100 AMIS technology ($W = 40\,\mu$m, $L = 1.2\,\mu$m): (**a**)$I_{DS} - V_{DS}$ and, (**b**) $g_{ds} - V_{DS}$ for $V_{GS} = 4 - 13$ V in steps of 1 V

Table 4.1 Main EKV Parameters

Name	Description	Units
TYPE	P-type/N-type	–
W	Channel Width	m
L	Channel Length	m
N_F	Number of fingers	–
COX	Oxide Capacitance	F/m^2
VT0	Long-channel Threshold Voltage	V
U0	Low Field mobility	cm^2/Vs
GAMMA	Body Effect Parameter	$\sqrt{V}$
PHI	Bulk Fermi Potential	V
E0	Mobility Reduction Coefficient	V/m
UCRIT	Longitudinal Critical Field	V/m
LAMBDA	Channel Length Modulation	–

($I_{DS} - V_{DS}$ and $g_{ds} - V_{DS}$) for $V_{GS} = 4 - 13$ V. Note, significant quasi-saturation effect can be seen on the output characteristics at higher gate voltages. It can be seen that model shows good behavior across different gate and drain bias region.

6 Parameter Extraction and Model Calibration

Tables 4.1, 4.2 and 4.3 show the list of main parameters used in the model. These basic parameters are used for modeling of any high voltage device at room temperature. The calibration procedure is described below and also shown in the flowchart (see Fig. 4.27). First threshold voltage and mobility is extracted using any standard extraction method [32–36]. Other standard EKV parameters [37] are extracted using

Table 4.2 Drift parameters

Name	Description	Units
L_{DR}	Drift length	m
L_{OV}	Gate overlap in the drift region	m
ρ_{Drift}	Drift resistivity	V-m/A
VSAT	Velocity saturation parameter	V/m
α_{vsat}	”	–
θ_{Acc}	Accumulation charge effect	1/V
k_{rd}	Effect of number of fingers	–
N_{CRIT}	”	–
α_T	Thermal coefficient of drift resistance	$1/K$

Table 4.3 Self-heating and impact ionization parameters

Name	Description	Units
R_{THNOM}	Thermal resistance	Ks/J
α	Temperature coefficient of R_{THNOM}	1/K
C_{TH}	Thermal capacitance	J/K
NEFF	Effective doping in the drift	$V^{-\frac{4}{3}}$

methodology proposed in [38]. Once we have all of these parameters, *GAMMA* and *PHI* are tuned for subthreshold slope on $I_{DS} - V_{GS}$ characteristics. $E0$ is tuned on $I_{DS} - V_{GS}$ characteristics in strong inversion for mobility degradation due to vertical field. *UCRIT* and *LAMBDA* are tuned on $I_{DS} - V_{DS}$ characteristics for velocity saturation and channel length modulation, respectively. Drift parameters *VSAT* and α_{vsat} are fitted in the linear region of $I_{DS} - V_{DS}$ characteristics while θ_{Acc} is used to lower the drift resistance on $I_{DS} - V_{GS}$ characteristics at high V_{GS} as described earlier. k_{rd} and N_{CRIT} parameters are fitted to model the effect of number of fingers on drift resistance.

The extraction of self-heating parameters requires dedicated measurement setup. The extraction of thermal resistance and capacitance has been discussed in detail in [9, 19, 20, 39]. The impact ionization parameter N_{EFF} is used as a fitting parameter to model the impact ionization in the drift region.

7 Effect of Lateral Non-uniform Doping

Here we will explain, how lateral non-uniform doping affects the small signal capacitance behavior of high-voltage MOSFETs [23, 40]. Figure 4.28a shows the device architecture under study. To see the impact of lateral non-uniform doping on capacitances, let's start with C_{GD} capacitance. Figure 4.29 shows the C_{GD} vs. V_{GS} using device simulation for different drain voltages. As expected, the C_{GD} at $V_{DS} = 0$ for conventional MOS stays low values for $V_{GS} < V_T$ (threshold voltage). As V_{GS} starts to increase beyond V_T, the C_{GD} increases sharply and saturates to $\frac{1}{2}WLC_{OX}$. The situation is completely different for LAMOS. Due to lateral non-uniform doping, the C_{GD} starts increasing as soon as V_{GS} is more than the surface inversion potential

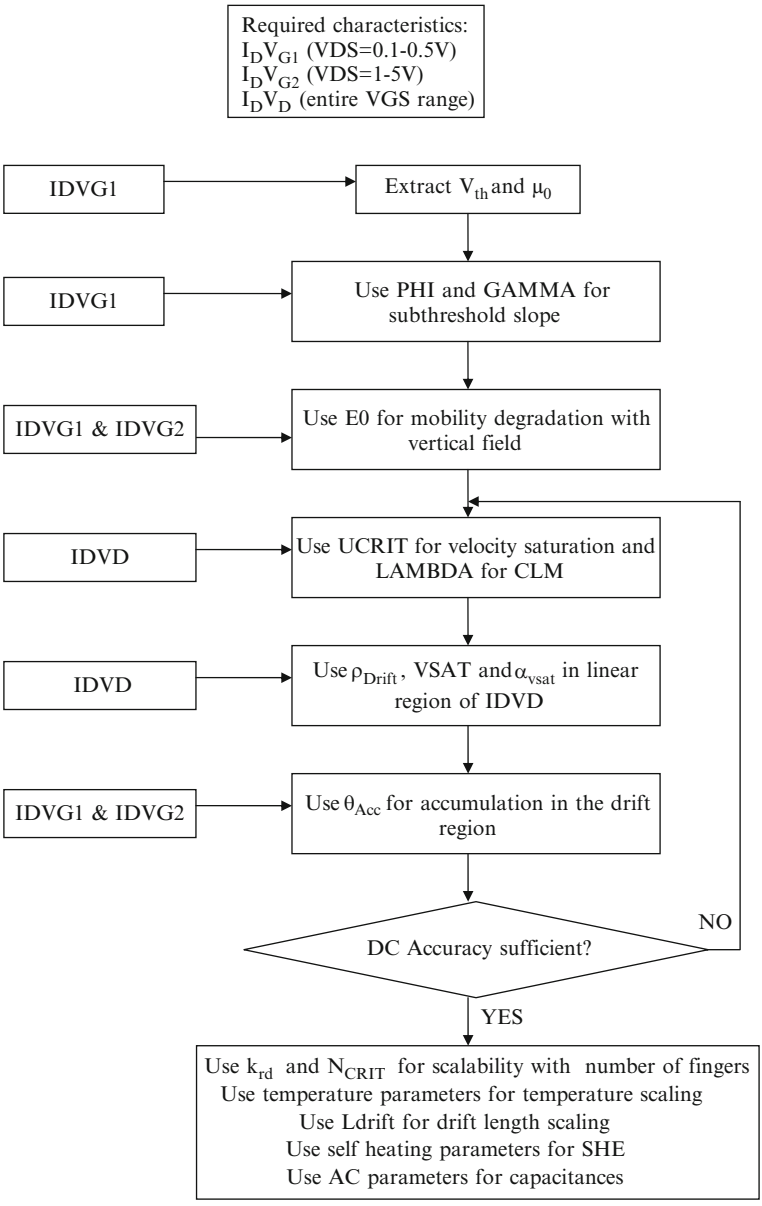

Fig. 4.27 Flowchart of parameter extraction procedure

at drain side. It means that the inversion at the drain side starts at lower values of V_{GS} than source side because of the lower doping at the drain end compared to source end. As V_{GS} keeps on increasing, the inversion in the channel propagates from drain towards source and C_{GD} keeps on rising. Once V_{GS} is greater than the

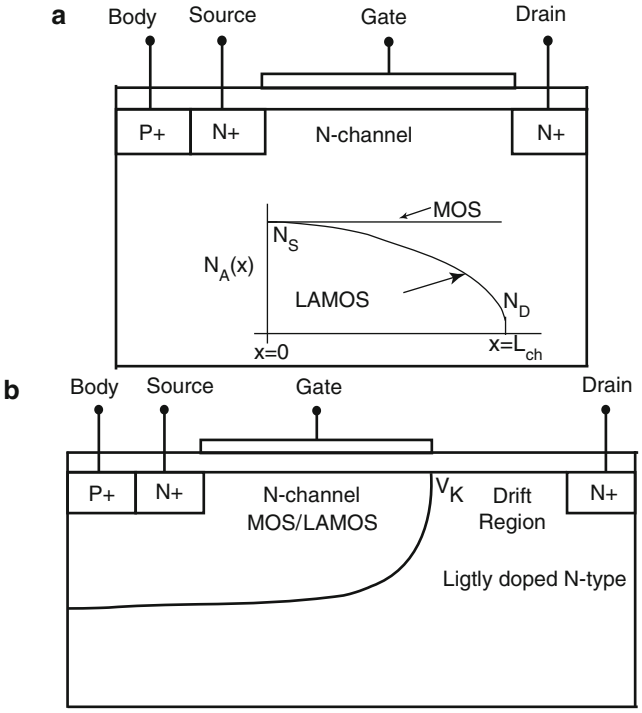

Fig. 4.28 Device architectures of ($L_{ch} = 2\,\mu$m): (**a**) Conventional MOSFET with uniform doping and LAMOS with lateral doping gradient in the channel. The lateral doping gradient is approximated by the complementary error function $N_A(x) = N_S.erfc\,[k_n(\xi)]$ [12,22,23], where $\xi = \frac{x}{L_{ch}}$ is the normalized position along the channel, k_n is a parameter representing the doping gradient. The doping level at the source side of the channel (N_S) is highest and decreases towards the drain in the channel region. Higher k_n means sharp decrease in the doping level from source to drain and vice-versa. (**b**) Conventional MOSFET with uniform doping and LAMOS with lateral doping gradient in the channel and a drift region to sustain high voltage

surface inversion potential at source side (or V_T of LAMOS), the C_{GD} starts to fall [32]. This can be explained by the fact that the rise in inversion charge is exponential for $V_{GS} < V_T$ and after that rise gets slower, ultimately becoming linear function of V_{GS}. In strong inversion ($V_{GS} \gg V_T$), the C_{GD} saturates to some value equal to or higher than $\frac{1}{2}WLC_{OX}$ depending on the doping gradient in the channel [12,23]. The impact of different doping gradients on capacitances will be explained later in this section. Increasing drain voltage reduces the peak due to depletion at drain side. For sufficiently high values of drain voltages, there may not exist any peak in C_{GD} (e.g. $V_{DS} \geq 2$ V in Fig. 4.29).

Another interesting property of LAMOS capacitances is seen on C_{GS} and C_{GG} behavior as shown in Figs. 4.30 and 4.31. The C_{GS} at $V_{DS} = 0$ is similar to MOSFET (except lower values due to low doping in the drain side), where the increase in C_{GS} occurs when channel gets inverted ($V_{GS} \geq V_T$). The situation is quite different for $V_{DS} > 0$. For $V_{DS} < V_{GS} - V_{TD}$ (threshold voltage corresponding to the doping at

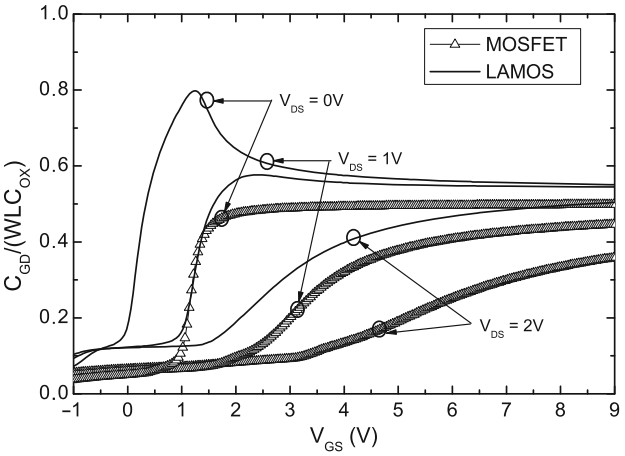

Fig. 4.29 The gate-to-drain capacitance C_{GD} versus V_{GS} for $V_{DS} = 0$, 1 and 2 V. The lateral non-uniform doping in LAMOS produces peaks in C_{GD} capacitances at low drain bias

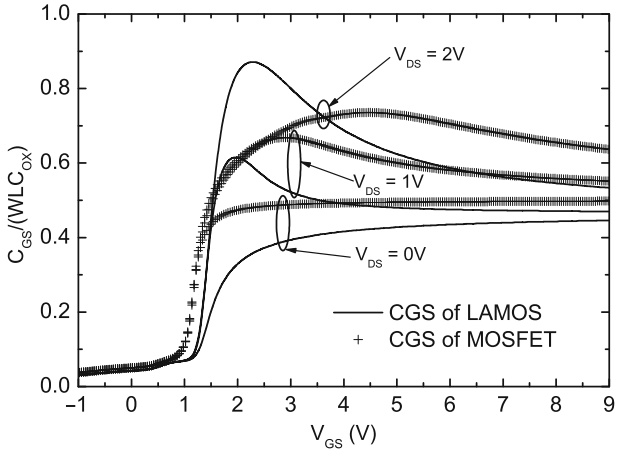

Fig. 4.30 The gate-to-source capacitance C_{GS} versus V_{GS} for $V_{DS} = 0$, 1 and 2 V. The lateral non-uniform doping in LAMOS produces peaks in C_{GS} capacitances around $V_{GS} = V_T$

drain), the C_{GS} is slightly higher than its value at $V_{DS} = 0$ and behaves similar to the MOS capacitance. But if $V_{DS} > V_{GS} - V_{TD}$, the drain end is depleted. For these drain voltages, as V_{GS} increases, there will be small increase in the channel charge from drain side until $V_{GS} < V_T$. At $V_{GS} = V_T$, there is sudden flow of large amounts of charges from source end (the small signal resistance seen from any point in the channel towards the drain will be higher than towards the source and charges choose the least resistive path, which is source side in this case) and whole of the channel gets filled up by these charges. This sudden rise in the charge from source side gives rise to increased peaks in C_{GS} for higher drain voltages as shown in Fig. 4.30.

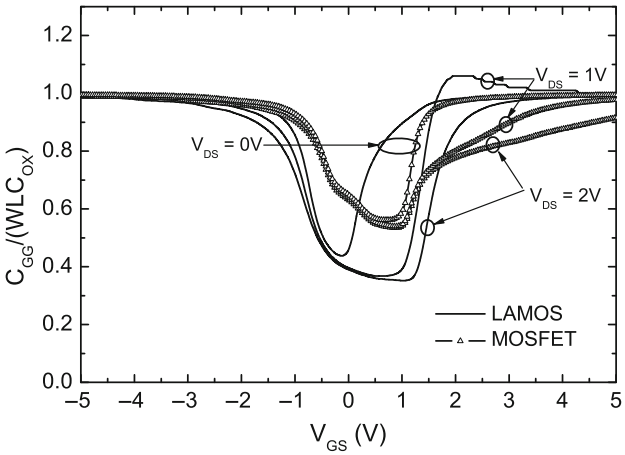

Fig. 4.31 The gate-to-gate capacitance C_{GG} versus V_{GS} for $V_{DS} = 0$, 1 and 2 V. The lateral non-uniform doping in LAMOS produces peaks in C_{GG} capacitances, when V_{GS} is around threshold voltage for small nonzero V_{DS}

It is interesting to note that C_{GG} also has small peaks for $V_{DS} = 1$ V as shown in Fig. 4.31, which was also shown in [41] for nonzero small V_{DS}. These peaks in C_{GG} can be explained by the fact that for $V_{GS} \leq V_T$, the source end of the channel is still in weak inversion while drain end is in depletion. Once V_{GS} reaches close the V_T, there will be sudden flow of charge from source side giving sharp increase in C_{GG}. This is not the case with the C_{GG} of conventional MOS, where continuous supply of charge is maintained from source side due to uniform doping. Also note that for low drain voltages, there will be large supply in the charge from drain end also once it comes out of depletion which again helps in increasing the total channel charge. Note that the peak vanishes as V_{GS} increases significantly above threshold voltage as now inversion charge is being supplied from both source and drain, and now gate charge is a linear function of gate voltage. For high values of drain voltages, no peak is observed, as charges entering from source end also contributes to removing the depletion at the drain side. Hence, the peak in C_{GG} occurs for small nonzero values of V_{DS}, when V_{GS} is around threshold voltage (source end entering into strong inversion from weak/moderate inversion). Another note on the C_{GG} of LAMOS is that the dip (lowest value) is lower compared to C_{GG} of MOS. This is due to the lower doping in the drain side which produces sharper and lower dip on C_{GG}. This can also be analyzed using segmentation approach, where LAMOS channel can be divided in several smaller channel length MOS with uniform doping in each channel but varying across different MOS giving equivalent non-uniform doping also called graded channel approach [41, 42].

The behavior of C_{DG} capacitances is also quite different for LAMOS [41, 43–45] as shown in Fig. 4.32. Similar to other capacitances of LAMOS, peaks are also observed on C_{DG}. The peak in C_{DG} at $V_{DS} = 0$ can be explained similar to the peak in C_{GD} at $V_{DS} = 0$. As gate voltage increases, the drain end of the channel gets inverted

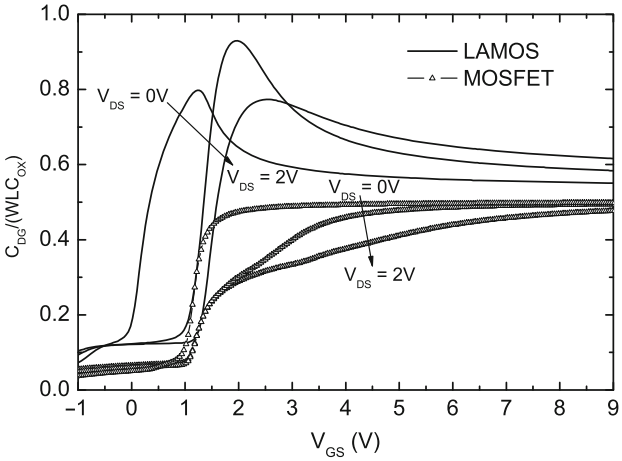

Fig. 4.32 The drain-to-gate capacitance C_{DG} versus V_{GS} for $V_{DS} = 0{,}1$ and 2 V. The lateral non-uniform doping in LAMOS produces peaks in C_{DG} capacitances. The peaks in the C_{DG} can be higher than WLC_{OX} depending on the doping profile and drain voltage [12]. The bias dependent partitioning scheme [43, 44] also explain these peaks

and C_{DG} starts increasing till source end get inverted and after that it decreases and saturates. In fact C_{GD} and C_{DG} are the exactly the same for $V_{DS} = 0$. But for nonzero drain voltages, C_{DG} has totally different behavior than C_{GD}. At $V_{DS} = 1$ V, note that the peak increases because a change in gate voltage induces a change in the channel potential (the perturbed channel potential becomes negative), which in turn causes a change in charge distribution and the combined effect increases the peak [43, 44]. To understand why perturbed channel potential can become negative to increase the small signal charge, consider the situation when the source end is weakly inverted and drain end is strongly inverted. In this case the transistor can be thought of as a series combination of two transistors with different threshold voltages, where the one near the source is weakly inverted and near the drain end is strongly inverted. Now let Q_S and Q_D be the charge at the source and drain end of the strongly inverted transistor. The current flowing through the transistor is proportional to $Q_S^2 - Q_D^2$ [3, 43, 44, 46]. The weakly inverted transistor in series forces current to be very small, therefore $Q_S^2 \approx Q_D^2$. Now as gate voltage increases both Q_S and QD will change and we have $\delta Q_S \cdot Q_S \approx \delta Q_D \cdot Q_D$. As drain end is kept at a fixed channel potential and is in strong inversion $\delta Q_D \approx C_{OX}\delta V_{GS}$. So we have $\delta Q_S/\delta V_{GS} = (Q_D/Q_S)C_{OX}$. As $Q_D > Q_S$ in this situation (because the drain end has lower doping), we have $\delta Q_S/\delta V_{GS} > C_{OX}$, which is only possible if the channel potential goes negative and aids the gate voltage. Depending on the doping profile in the channel and drain voltage, the peak in C_{DG} may even increase above WLC_{OX} in presence of a gate voltage [12, 43].

The above analysis was made using single value of doping gradient (k_n) in the channel of LAMOS. If the value of doping gradient (k_n) is increased giving sharper doping profile in the channel, the peaks on C_{GD} increases and value of C_{GS} decreases

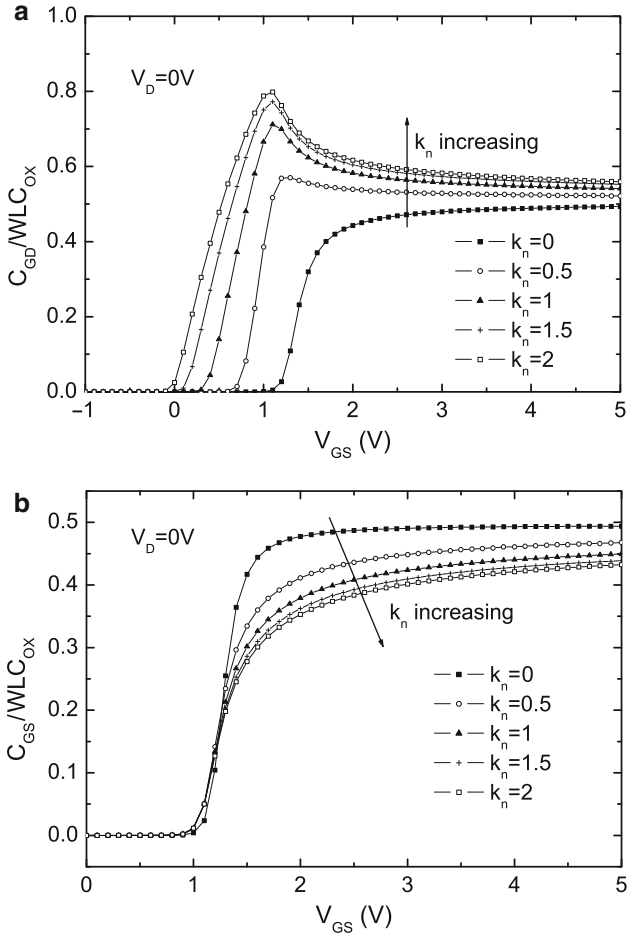

Fig. 4.33 Effect of different doping gradients (k_n) on LAMOS: (**a**) Normalized C_{GD} and (**b**) normalized C_{GS} at $V_{DS} = 0$. Note that the peak in C_{GD} increases, while C_{GS} in strong inversion decreases with increase in doping gradient. The $k_n = 0$ corresponds to uniformly doped MOSFET

in strong inversion, while the rising slope on both capacitances decreases [12] as shown in Fig. 4.33a, b. The lateral doping gradient in the channel also affects DC characteristics of LAMOS. Higher doping gradient increases the saturation voltage and saturation current on the output characteristics as shown in Fig. 4.34. The prolonged linear region in the output characteristics and peaks/slopes on capacitances can be explained by the fact that doping gradient changes the surface potential required for the inversion across the channel decreasing from source to drain.

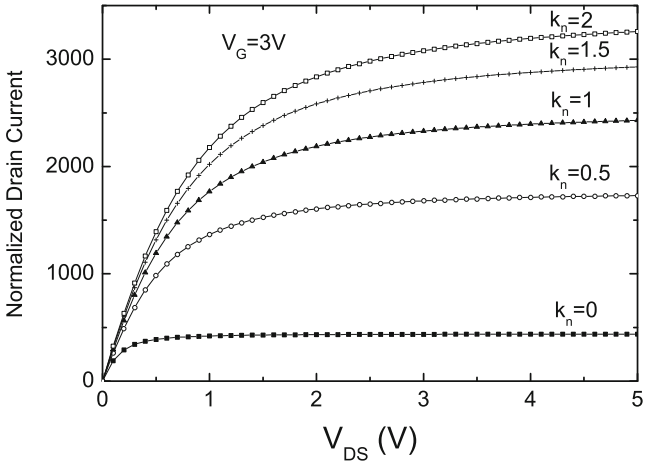

Fig. 4.34 Effect of different doping gradients (k_n) on LAMOS: normalized drain current $\frac{I_D}{2n_q\mu_0\frac{W}{L}C_{OX}U_T^2}$ at $V_{GS} = 3V$ (strong inversion). Note that the linear region extends, current as well as saturation voltage increases and R_{ON} decreases with increase in doping gradient. The $k_n = 0$ corresponds to uniformly doped MOSFET

8 Conclusion

A general High Voltage MOSFET model based on the EKV model as a core (called HV-EKV) and a bias-dependent drift resistance were presented. The main model parameters are physical and can be experimentally extracted from standard I–V plots. The drift resistance includes all major physical effects originating from the drift region of high-voltage devices such as quasi-saturation and accumulation in the gate overlapped drift region. The impact ionization effect was modeled for both intrinsic MOSFET and the drift regions; from our analysis it appears that impact ionization in the intrinsic MOSFET dominates at low to medium gate voltages while at higher gate voltages (and high drain voltages) impact ionization in the drift region is dominant. The self-heating effect was incorporated using a sub-circuit approach. The thermal resistance and capacitance used in the sub-circuit are dynamically varying with the temperature inside the device. The accuracy of the model is better with a temperature-dependent thermal resistance compared to a constant thermal resistance.

The HV-EKV model performance was demonstrated against experimental data for three industrial devices: (i) VDMOS, (ii) bulk-LDMOS and (iii) SOI-LDMOS. The model was able to reproduce the special effects of these high voltage devices like the quasi-saturation and self-heating effect, and is scalable with all physical and electrical parameters such as transistor width, drift length, number of fingers and temperature. In addition to other works in HV device modeling, the model scalability with the drift length in LDMOS transistor is clearly demonstrated in HV-EKV model. The model shows very good accuracy for the entire DC bias range and good

behavior for capacitances, especially the peaks and shift of these peaks with bias. The model provides excellent trade-off between speed, convergence and accuracy, being suitable for circuit simulation in any operation regime of HV MOSFETs. The model has been implemented in Verilog-A and tested on SABER (Synopsys), ELDO (Mentor Graphics), HSpice (Synopsys) and Cadence's Virtuoso Spectre circuit simulator and Virtuoso UltraSim fast-Spice simulator for industrial use.

It is worth noting that the reported model was evaluated according to the Compact Modeling Council (CMC) benchmarking procedure. Below we present a short discussion of model's main features according to such industrial compact model standards.

1. Capable for analog and RF IC simulations, which requires:
   (a) Accurate modeling of DC/AC behavior as well as the derivatives of terminal currents and node charges with respect to node voltages for all working modes (off, linear, saturation regions and reverse modes). Charge model has to be charge conservative, and intrinsic charge model has to take into account the effects of voltage drop across the source and drain resistances.
   (b) Accurate modeling of drain extension (drift region) region resistance including velocity saturation.
   (c) Accurate modeling of gate/drain overlap region bias dependent capacitance and resistance.
   (d) Accurate modeling of parasitic effects (gate, source and drain, and substrate resistances, and source/drain-body junction diodes).
2. Capable of modeling accurately with power supplies up to 200 V and temperature ranges from −50°C to 200°C.
3. Capable of modeling self-heating effects accurately and efficiently, which requires scalable temperature-dependence modeling.
4. Capable of modeling accurately quasi-saturation effects and gm fall-off in the saturation region, namely, the channel current compressions at higher Vgs when Vds is greater than Vdsat.
5. Capable of modeling accurately Cgd drop at higher external Vgs biases.
6. Capable of accurate modeling of the true asymmetry of the source and drain resistances and the source and drain junctions in IV and CV.
7. Capable of modeling substrate current behavior correctly including the impact ionization taking place in the drain drift extension regions.
8. Capable of handling scalability over a wide range of geometries, biases, and temperatures with one set of global model parameter set to cover the entire device matrix provided for model extraction. Provides drain drift region length as an instance parameter.
9. Capable of handling of p-type devices as well as n-type devices.
10. Good convergence in reasonable scale circuit simulation.
11. Capable of modeling accurately a wide array of HV-MOSFET process technologies and device structures, which would include LDMOS and EDMOS

(Extended Drain), both symmetrical and asymmetrical, and other drain drift extension structures including, but not limited to, those of various RESURF flavors.
12. Capable of modeling accurately the long-channel DIBL and Rout degradation for drain extended devices.
13. Capable of modeling layout dependent characteristics including multifinger device structures that have separate, merged, and shared source and drain connections, and point and wide source/drain contacts.
14. Capable of modeling body bias dependency of DC and AC characteristics, as well as Vds-dependence of the body bias effects.
15. Capable of providing optional temperature node for thermal electrical coupling simulation.
16. Capable of modeling parasitic BJT effects.

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Chapter 5
Power Devices

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Abstract Main problems encountered in modelling of high power semiconductor devices are discussed in this paper. Unipolar and bipolar device properties are compared and the problems introduced by high time constant values related to carrier diffusion phenomena in the large base are explained. Traditional and novel concepts of power device modelling and simulation are presented.

A new distributed model of power diode that can be integrated into a SPICE-based circuit simulator is described. Together with the existing power MOSFET macromodel, the presented approach can facilitate the design process of power electronic circuits. In the future, distributed models for IGBT and BJT will be added.

Keywords Power semiconductor devices · Modelling · MOSFET · PIN diode · IGBT · Silicon carbide

1 Introduction

Traditional models of semiconductor devices implemented in widely spread circuit simulators such as SPICE are very often insufficient for professional design of power electronic circuits. This is due to the fact that they are based on built-in quasi-static lumped models which were developed for low power devices. While justified for low power, the quasi-static and lumped simplifications are not acceptable in the case of high power electronic devices.

Power semiconductor devices must contain a long lightly doped layer that can exceed 100 μm and enables them to support high voltages [1, 2]. The negative consequence, however, is that introduction of excess carriers into this region in the on-state may be necessary in order to maintain low voltage drop and thus reduce power loss. In conjunction with the large layer dimension this implies storage of an

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important amount of charge whose behaviour is determined by physical phenomena of distributed nature. This has a great impact on device dynamics.

The importance of accurate simulation of transitory states is high and still increasing because power semiconductor devices are normally used as switches and their working frequency is constantly raised. Therefore, semiconductor switch dynamics is visibly influencing the overall performance of power electronic systems [3, 4].

2 Power Device Modelling

The main parameters of power semiconductor devices are:

- Voltage blocking capability, or breakdown voltage
- Current capability, or maximum rated current, which is a function of on-state voltage drop and maximum power dissipation
- Switching performance, or maximum switching frequency, which results from switching times

The extreme values for basic parameters of modern power devices are presented in Table 5.1, where V_D is the maximum rated off-state voltage, V_{on} is the on-state voltage, I_T is the maximum rated on-state current, t_{on} and t_{off} are the minimum turn-on and turn-off times, and f_s is the maximum switching frequency (dynamic power loss not being taken into account). As can be seen, the unipolar VDMOS (Vertical Double-Diffused MOSFET) has very good switching performance but its current capability and maximum blocking voltage are much smaller than those of bipolar devices (GTO [5, 6] and GCT thyristors). The IGBT (Insulated Gate Bipolar Transistor) combines the best properties of unipolar and bipolar devices. Its voltage and current ratings are much better than those of VDMOS and switching properties are much better than those of GTO and GCT.

Figure 5.1 presents the product of rated voltage and current for different power semiconductor devices. The solid lines represent the present state and the dashed lines show future trends in power semiconductor device development.

For all types of power devices the blocking capability is a function of the large base width and its doping concentration. Equation 5.1 gives the value of

Table 5.1 Performance limits of the most commonly applied modern power devices (commercially available)

		VDMOS	IGBT	GTO	GCT
V_D (V)	Max	1,200	6,500	6,500	6,500
I_T (A)	Max	350	3,500	3,000	3,000
V_{on} (V)	Type	Very high	Low	Very low	Low
t_{on}(μs)	Min	0.005	0.02	3	5
t_{off}(μs)	Min	0.008	0.1	12	3
f_s (kHz)	Max	10,000	400	5	10

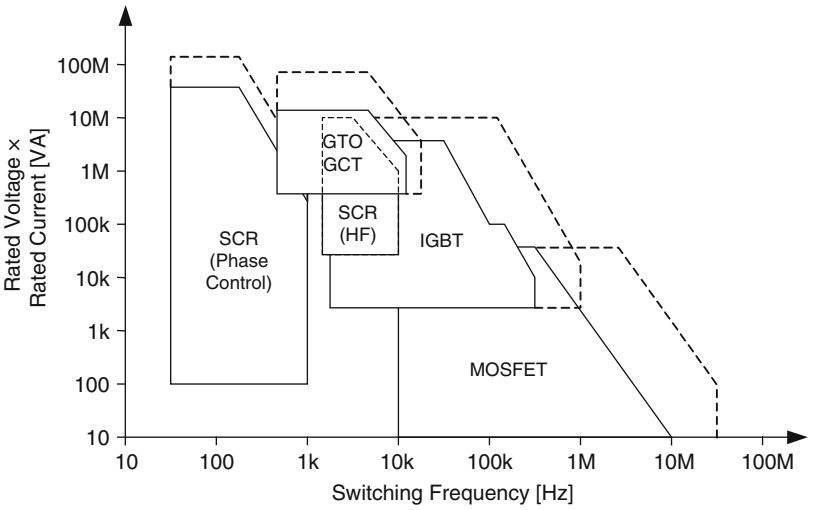


Fig. 5.1 Product of rated voltage and current as function of maximum switching frequency

maximum blocking voltage V_B (breakdown voltage) as a function of base doping concentration:

$$V_B = 60 \times \left(\frac{10^{16}}{N_D}\right)^{3/4} \tag{5.1}$$

with N_D in cm^{-3} and V_B in volts.

Equation 5.2 gives the minimum necessary value of large base width W as a function of maximum blocking voltage and doping concentration without taking into account the punch-through effect. It is equal to the space charge region thickness when maximum blocking voltage is applied:

$$W = \sqrt{\frac{2\varepsilon\,(\Phi + V_B)}{qN_D}} \cong \sqrt{\frac{2\varepsilon V_B}{qN_D}} \tag{5.2}$$

where Φ is the diffusion potential, much smaller than the breakdown voltage, ε is the silicon permittivity, and q is the elementary charge.

The conclusion from these two expressions is that in order to obtain a high value of maximum blocking voltage, semiconductor devices must have a low doping level and a large width of the base.

The minimum necessary base width values have been calculated from expressions 5.1 and 5.2 for three different values of large base doping concentration and have been presented in Table 5.2 together with corresponding maximum blocking voltage values.

The most important observation that can be made is that for the high power semiconductor devices voltage must be supported in a large base. Therefore the charge

Table 5.2 Maximum blocking voltage and minimum necessary base width for three different values of large base doping concentration

Device no.	N_D (cm^{-3})	V_B (V)	W (μm)
1	1.25×10^{14}	1,600	125
2	1.0×10^{14}	1,895	157
3	1.0×10^{13}	10,700	1,175

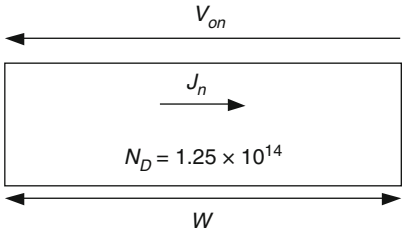


Fig. 5.2 Illustration of the on-state resistance calculation in the case of an n-type unipolar device

transport through the base cannot be treated as instantaneous and the voltage drop across cannot be neglected.

Let's now consider two power devices of different types: a unipolar and a bipolar one.

In the case of the unipolar device the current capability or, in other terms, the on-state resistance R_{on} can be found from a very simple consideration depicted in Fig. 5.2.

According to Table 5.2, for a given value of the large base doping concentration, the corresponding maximum blocking voltage V_B and the necessary base width can be determined. In the case presented in Fig. 5.2, the value of N_D is 1.25×10^{14} cm^{-3}, which corresponds to a maximum blocking voltage of 1,600 V and a minimum base width of 125 μm. Current density in the case of an n-type unipolar device is equal to the electron drift current density:

$$J = J_n = q\mu_n nE = q\mu_n N_D \frac{V_{on}}{W} \tag{5.3}$$

where E is the electric field, n is the carrier concentration (equal to N_D), and μ_n is the electron mobility.

Taking into account Fig. 5.2, the on-state resistance for a unipolar device with a cross-section area of 1 cm^2 can be found as:

$$R_{on,\mathrm{cm}2} = \frac{V_{on}}{J \times 1\mathrm{cm}^2} = \frac{W}{q\mu_n N_D \times 1\mathrm{cm}^2} \tag{5.4}$$

In the considered case, this will be equal to 0.46 Ω. Even for a relatively low current of 10 A, the voltage drop will be as high as 4.6 V and for higher currents it would become unacceptable. We can conclude that unipolar devices cannot be applied in the

very high voltage and very high current range. This conclusion stays in accordance with the real maximum device ratings presented in Table 5.1 and Fig. 5.1.

In the case of the bipolar device the situation is completely different. Two mechanisms, drift and diffusion, are responsible for the current density. Using one-dimension approximation and taking the displacement current into account they can be described with the following set of equations:

$$J_n = q\mu_n nE + qD_n \frac{\partial n}{\partial x} \tag{5.5a}$$

$$J_p = q\mu_p pE - qD_p \frac{\partial p}{\partial x} \tag{5.5b}$$

$$J = J_n + J_p + \varepsilon \frac{\partial E}{\partial t} \tag{5.5c}$$

where p and μ_p are the hole concentration and mobility, respectively, D_n and D_p are the electron and hole diffusion constants, respectively, t is time and x is the position along current path.

As can be seen from Eq. 5, the current capability in the case of bipolar devices is higher than in the previous case. Thanks to diffusion the maximum current density is much higher and consequently the corresponding voltage drop is much lower than in the case of unipolar devices. Additionally, in bipolar structures some effects resulting from effective base doping changes can appear, e.g. the base widening effect, and the thyristor effect, rendering in an additional current capability.

We will now analyze how the mechanism of charge transport through the large base influences the switching performance of the device.

According to Fig. 5.2 the charge transit time through the large base for the unipolar device can be expressed as:

$$t_t = \frac{W}{v_{nsat}} \tag{5.6}$$

where v_{nsat} is the saturation velocity of the electrons in a given temperature T:

$$v_{nsat} = 10^7 \frac{\text{cm}}{\text{s}} \times \left(\frac{T}{300\,\text{K}} \right)^{-0.87} \tag{5.7}$$

In the case of power devices one can assume that the electric field is strong enough for all the charge carriers to attain their maximum speed. For the temperature of 300 K, the transit time through the large base can be easily calculated. In Table 5.3 transit times for three values of large base width are presented. As can be seen, in the case of unipolar devices even for a very large base the transit time remains very

Table 5.3 Electron transit time through the large base for a unipolar device for three different values of large base width

Device no.	W(μm)	t_t(ns)
1	125	1.25
2	157	1.57
3	1,175	11.75

Table 5.4 Electron transit time through the large base for a bipolar device for three different values of large base width

Device no.	$W(\mu m)$	$T_D(\mu s)$
1	125	1.12
2	157	1.76
3	1,175	98.62

short and, in the majority of cases, the internal time constant of the device can be neglected as compared to the time constant of the external circuit.

Again the situation is different in the case of the bipolar device. As a first order simplification, we can assume that the transit time of minority carriers through the large base can be expressed with [1]

$$\tau_D = \frac{W^2}{2D} \cong \frac{W^2}{4D_n} \tag{5.8}$$

where D is the diffusion constant equal $2D_n$ under high carrier injection condition.

In Table 5.4 transit times for three values of large base width are presented. In this case the transit time through the base is very long and the internal time constant of a bipolar device can be much larger than time constants of the external circuit. In such a case, a simple lumped model cannot be used any longer. For bipolar devices it is necessary to take carrier diffusion inside the structure into account and a distributed model should be applied. Until now such a model has not been built in the standard circuit simulators.

3 The Contemporary Methods of Power Device Simulation

Because of the problems mentioned above, correct power device simulation is not possible yet in standard simulation programs. The first question is, why specific power device models are necessary? Their main areas of application are as follows:

- Power integration–simulation of power functionality in integrated circuits [7]
- Correct prediction of power dissipation inside power semiconductor devices (with special emphasis on power loss during device turn-on and turn-off)
- Computation of temperature distribution inside the semiconductor structure
- Correct cooling environment design
- Thermal breakdown prediction

In the case of unipolar devices such as the VDMOS power MOSFET (see Fig. 5.3) in the normal mode of operation majority carriers are responsible for current conduction. Therefore, it is possible to build a relatively simple macromodel taking into account all the elements of the structure.

Such a macromodel developed for SPICE-like simulators is presented in Fig. 5.4 [8–15]. In the case when the body diode D_{body} is not conducting (VDMOS is not reverse biased), this model is sufficiently accurate and can be applied for simulation

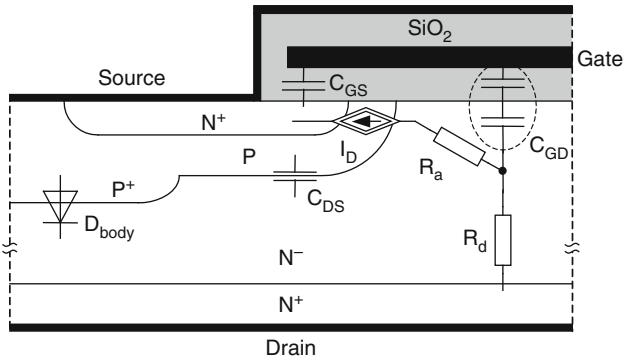
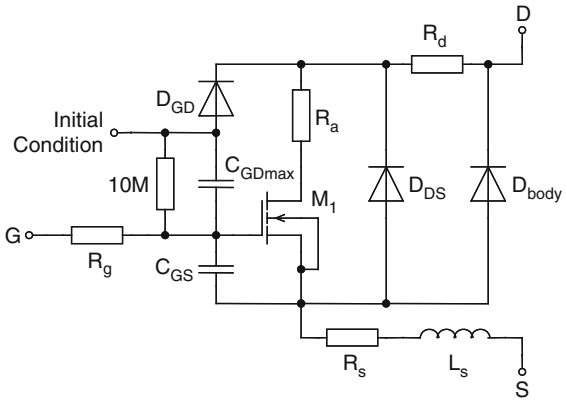


Fig. 5.3 Cross-section of an elementary cell of the VDMOS power transistor with the main structure elements

Fig. 5.4 VDMOS SPICE-like macromodel [14]



of all types of circuits. The situation is different when the body diode D_{body} starts to conduct current and consideration of diffusion phenomena becomes necessary.

In Fig. 5.5 a half-bridge circuit and in Fig. 5.6 simulation and measurement results obtained for this circuit are presented. The voltage and current waveforms are in good agreement with the experiment, and even power dissipation inside the structure can be correctly predicted.

As a conclusion from the above considerations, we state that in the case of unipolar devices:

- There is no problem with diffusion phenomena (majority carriers only)
- Very good accuracy and fast simulation are both achieved with lumped models
- Model parameters have a clear geometrical or physical interpretation
- Distributed models are necessary only for modelling of the body diode

Such a simple approach cannot be applied to a bipolar structure such as PIN diode, thyristor or IGBT. In Fig. 5.7, the cross-section of an elementary IGBT cell is presented. All the important phenomena occur in the large base (in this case in the N^-

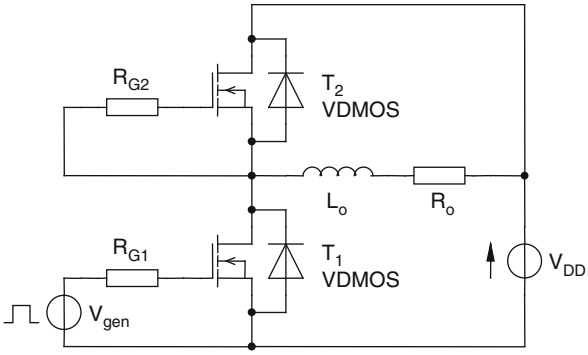


Fig. 5.5 VDMOS in a half-bridge configuration [14]

layer). In this punch-through IGBT transistor, the large base is relatively short, but even in this case, one can not neglect the minority carrier transport phenomena.

In order to take into account the distributed nature of these phenomena, the charge carrier transport (current continuity and drift-diffusion) and electric field (Poisson's) equations must be solved for every point inside the structure [16–20] The most commonly adopted approach is to apply the finite element, the finite difference or the finite box method.

In Fig. 5.8 the discretisation mesh of one IGBT cell for two-dimension simulation is presented. The application of such models enables not only correct current and voltage response simulation but also evaluation of current density and voltage potential inside the structure as well as calculation of dissipated power density and overall dissipated power and energy.

As a simulation example, collector–emitter voltage and collector current as well as dissipated power and energy during IGBT switching are presented in Figs. 5.9 and 5.10.

Application of an additional thermal model [21–26] enables computation of temperature rise inside the semiconductor structure. This additional thermal model has to be a three-dimension one. In Fig. 5.11, time waveforms of total dissipated power and maximum temperature rise inside the studied IGBT structure are presented.

The main drawback of such an approach is a very long simulation time and difficulty in simulating more than one or two power devices in the same circuit. The power circuit designers need relatively simple models which can be applied in standard SPICE-like circuit simulation programs combining very short simulation time and possibility of realistic high power circuit analysis. In the next section a new approach to this problem will be presented.

4 Developing the New Type of Bipolar Power Device Model

In all SPICE-like simulators lumped semiconductor device models are applied. As explained in Section 2, such models can be used in the case of low power devices,

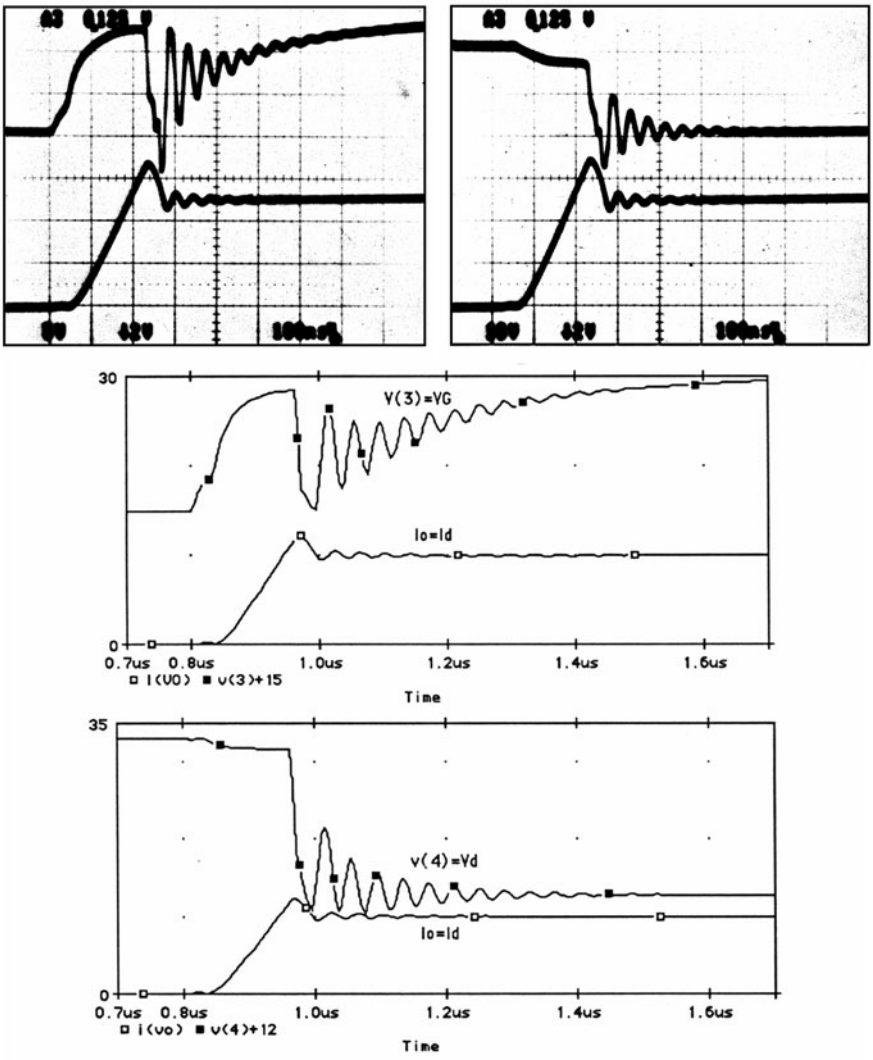


Fig. 5.6 Measurement and simulation results for the half-bridge with VDMOS transistors [14]

where the base is relatively short and any device internal time constants are much lower than time constants of the external circuit.

In order to enable simulation of circuits containing bipolar power semiconductor devices, we will try to develop separate device models taking into account the distributed nature of phenomena that occur in these devices and determine their dynamic response. In this section, a model of PIN diode will be presented [27, 28]. Its development is the key point for future design of such models for BJT, IGBT or thyristors as they all rely on carrier diffusion in a large lightly doped base.

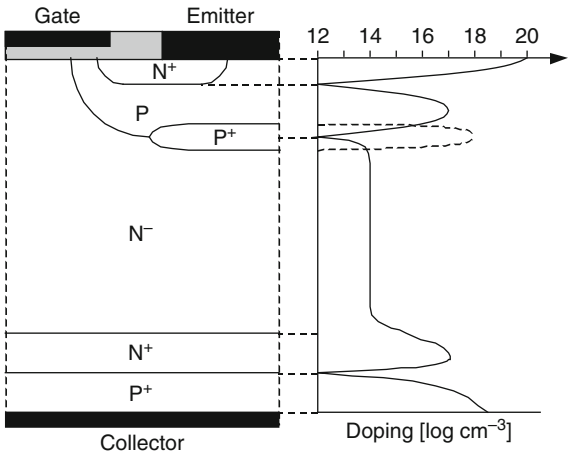


Fig. 5.7 Cross-section of an elementary cell of the PT-IGBT power transistor [17]

In order to simplify the modelling procedure and the model itself, the so-called modular approach [29–31] has been applied. In the considered semiconductor structure several regions of different physical and/or electrical nature have been distinguished. Then a simplified sub-model has been assigned to each of them. This approach allows a considerable decrease in simulation time without any important loss of accuracy provided that the important phenomena are identified and described properly.

It has been shown in Section 2 that in the case of power semiconductor devices the most important is the large base region which assures high voltage blocking capability in the off-state and where excess carriers are stored in the on-state. The simplest device in which one can consider all the important physical phenomena is the PIN diode shown in Fig. 5.12. The one-dimension Benda-Spenke model [33] has been adopted for this purpose. The behaviour of stored charge carriers is there described by means of the ambipolar diffusion equation:

$$\frac{\partial^2 p(x,t)}{\partial x^2} - \frac{1}{D_a}\left(\frac{p(x,t)}{\tau_{hi}} + \frac{\partial p(x,t)}{\partial t}\right) = 0 \tag{5.9}$$

where p is the hole concentration (equal to the electron concentration n under high injection condition), D_a is the ambipolar diffusion constant and τ_{hi} is the common electron and hole lifetime under high injection.

The partial differential equation (5.9) cannot be solved analytically, therefore many different approaches based on numerical methods have been presented in the literature. The proposed model is based on the algorithmic approach, i.e. the solution is obtained with a numerical algorithm. Discretisation of Eq. 5.9 leads to [28, 29]

$$p(x_i, t_j) = C_1\left[p(x_{i-1}, t_{j-1}) + p(x_{i+1}, t_{j-1})\right] - C_2 p(x_i, t_{j-1}) \tag{5.10}$$

where x_i and t_j are discrete position and time, respectively, and C_1 and C_2 are constants dependent primarily on the large base properties. Equation 5.10 is used to obtain a new carrier concentration distribution in the storage region as well as

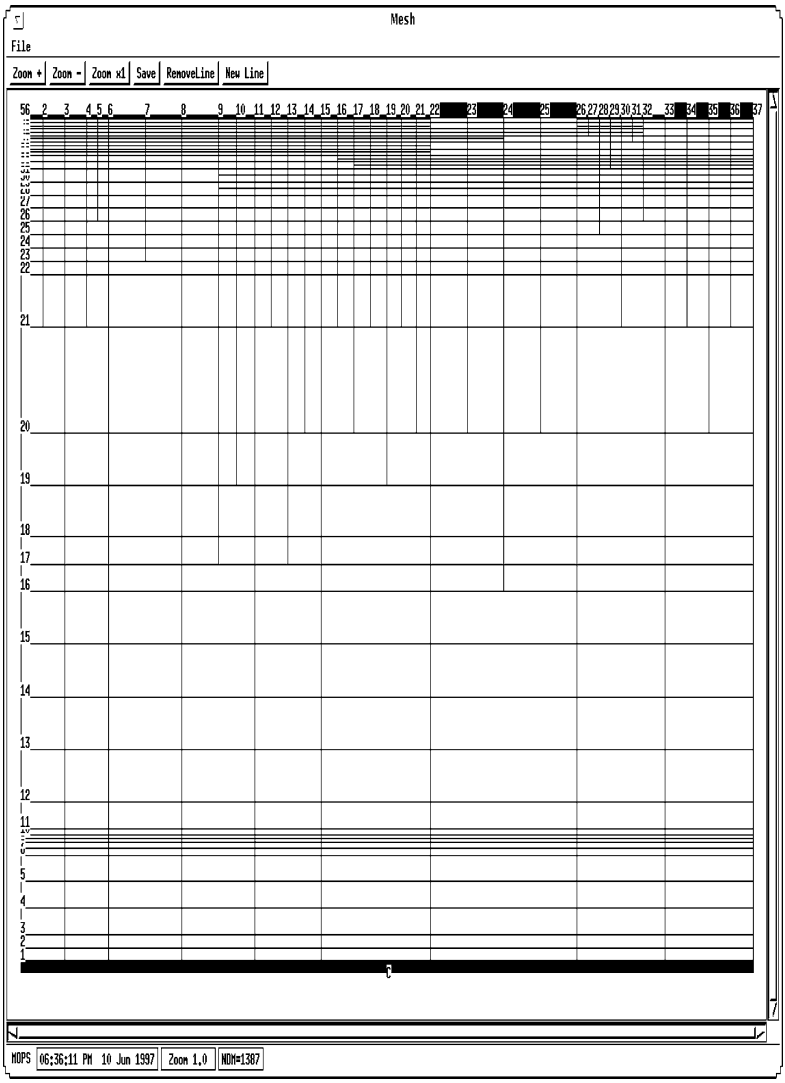


Fig. 5.8 Discretisation mesh used during 2D analysis of an IGBT structure [20]

new storage region boundaries. Figure 5.13 shows an exemplary result of carrier concentration evolution/during diode turn-off.

After a solution of Eq. 5.9 is obtained for a given time point t_j, the negative voltage drop in the space charge region can be calculated from the Poisson's equation:

$$\frac{\partial E(x)}{\partial x} = -\frac{\rho(x)}{\varepsilon} \tag{5.11}$$

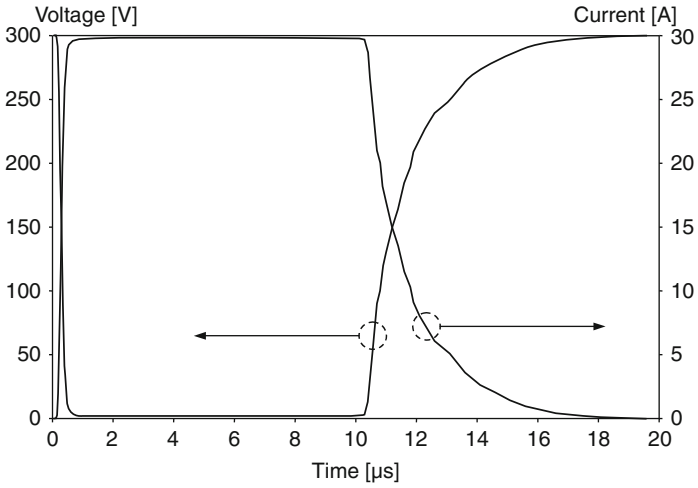


Fig. 5.9 IGBT collector-emitter voltage and collector current waveforms during switching [20]

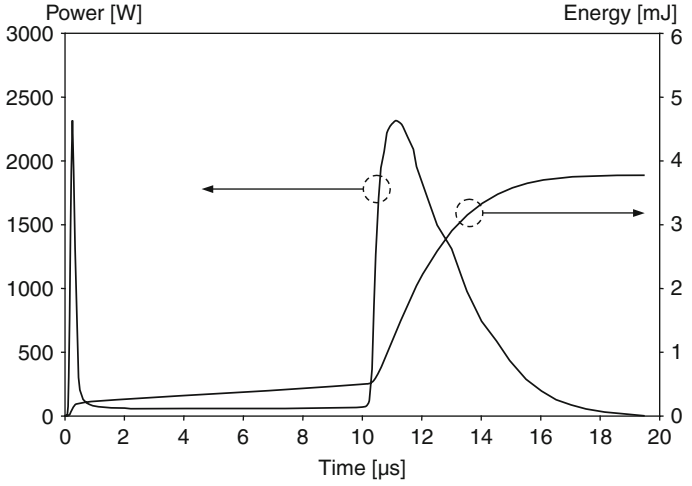


Fig. 5.10 Instantaneous dissipated power and dissipated energy during IGBT switching [20]

where ρ is the local charge density.

In order to solve this non-linear equation, the Newton–Raphson method has been applied [27]. The total voltage drop across the device is the sum of voltage drops across the charge storage region, the space charge region, the ohmic drift region and the two junctions. The expressions for the latter three voltage drops are straightforward [29].

Implementation of the model into a SPICE-based circuit simulator [32] will be described in a more detailed way in Chapter 8.

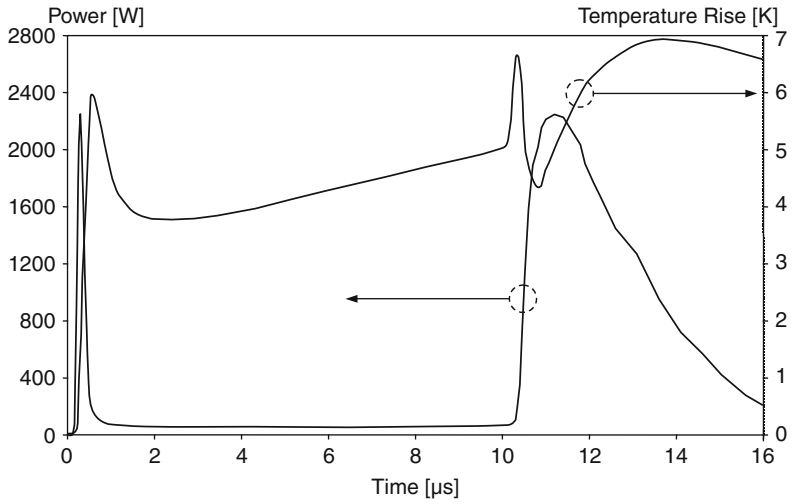


Fig. 5.11 Instantaneous dissipated power and maximum temperature rise inside the IGBT structure during switching [20]

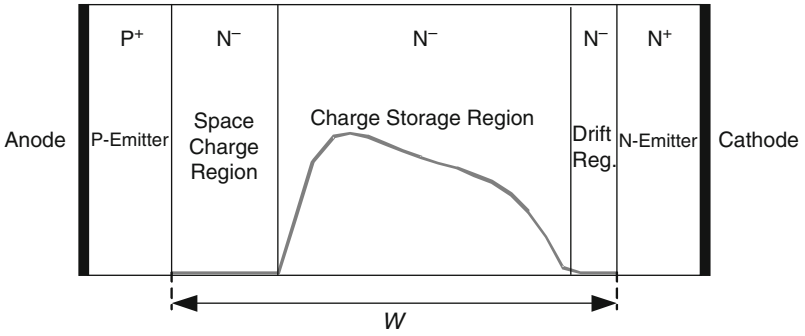


Fig. 5.12 The modular modelling concept and its application to the PIN diode (an exemplary charge carrier concentration distribution inside the large base is shown) [32]

Results of PIN diode simulation using the above-described model are presented in Fig. 5.14 and compared with an accurate 2D model and the lumped built-in SPICE diode model. It becomes clear that the built-in model developed for a low power device is unable to describe the real behaviour of a power diode during transitory state because the charge model in the form of a capacitor is no longer valid.

Moreover, Fig. 5.15 shows that the lumped model cannot be used to estimate, even roughly, the power dissipation in the device (0.05 mJ total turn-off energy loss vs 1.91 mJ obtained with the accurate 2D model) whereas the distributed model provides a very good estimation as compared to 2D simulations (1.82 mJ total turn-off energy loss), however, in a considerably shorter time.

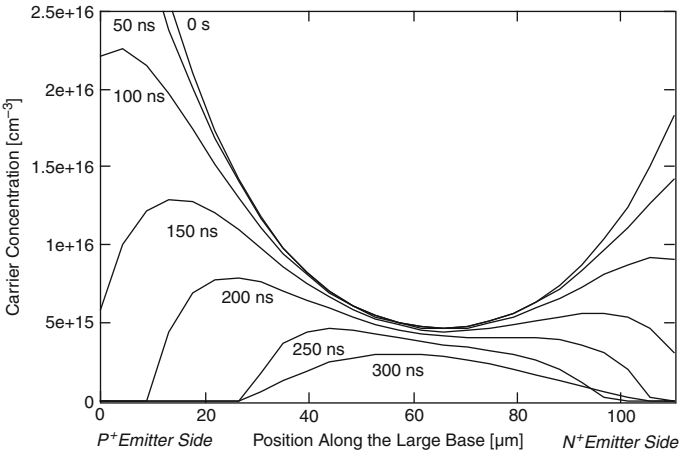


Fig. 5.13 Evolution of carrier concentration distribution in the large base of a PIN diode during turn-off—simulation results obtained with the described model [32]

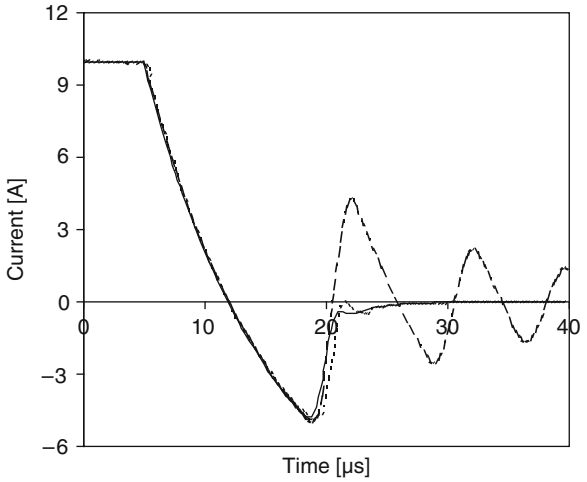


Fig. 5.14 Simulation of PIN diode turn-off with inductive load (solid – distributed model, dotted – 2D model, dashed – built-in model)

5 Recent Power Devices

Recent advances in power semiconductor devices may be grouped into two categories:

- Improvement of existing silicon structures
- Introduction of new materials and structures

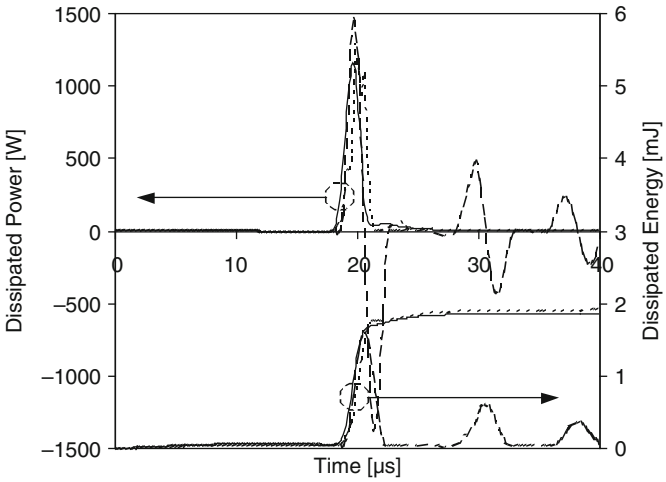


Fig. 5.15 Instantaneous dissipated power and dissipated energy during PIN diode turn-off (solid – distributed model, dotted – 2D model, dashed – built-in model)

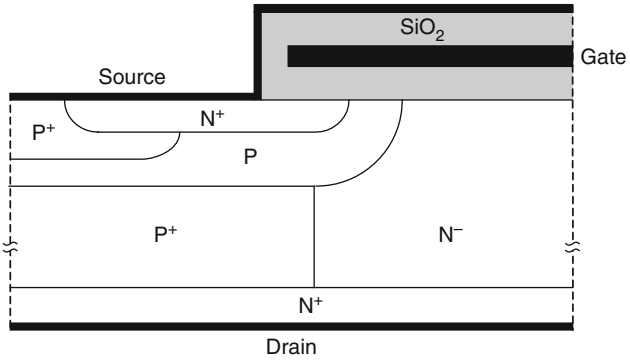


Fig. 5.16 Cross-section of one cell of the CoolMOS power transistor

After VDMOS, many new power MOSFET structures have been proposed [34] such as RESURF, CoolMOS, AccuFET and FLIMOS. As unipolar device switching performance is already outstanding, the basic aim of research work is to lower the ratio of on-state resistance to breakdown voltage.

Some of the above structures have been successfully introduced into commercial device manufacturing, with CoolMOS [35] (vertical superjunction MOSFET, see Fig. 5.16) in first place. This resulted in a need for proper simulation models. These new structures basically may be considered as LDMOS (Lateral DMOS) or VDMOS modifications. Therefore, current conduction is unipolar and there is no need for modelling concepts other than presented in Section 3 for the VDMOS structure. Even if important modifications to model topology and parameters must have been made, it has been proved that lumped models are sufficient to obtain good simulation accuracy [36] still with the exception of the integral diode [37].

Also, temperature dependence of new unipolar device characteristics may be described with lumped electrical models accurately enough to support the circuit design engineer [38]. Still 3-D models are necessary when optimising structures and investigating failure mechanisms.

In the field of bipolar power devices the greatest advances have been made in IGBT and GTO technology. However, charge carrier behaviour still remains the main problem for modelling of these devices and the same modelling approaches continue to be applied [39, 40].

The second group of recent power devices emerged thanks to introduction of new semiconductor materials. Modern applications such as automotive, aviation, mining, space exploration etc. make it necessary for electronic circuits to work in temperatures exceeding 200°C or – the opposite – in cryogenic temperatures. At the same time, thermal issues are known to be an important cause of electronic equipment failures and a major factor limiting the safe operation area of semiconductor devices [1]. Cooling systems are costly and increase overall system size and weight.

Analysis of silicon semiconductor devices has led to the conclusion that further improvements in their thermal characteristics are greatly limited by physical properties of silicon. Therefore, efforts are made in order to introduce semi-conducting materials with better thermal properties, including GaAs, InP, GaN, SiC, diamond, or to make use of SOI technology [41]. In the last years silicon carbide technology has been improved to the extent enabling commercial device manufacturing.

Silicon carbide power diodes are now well established on the market so field engineers must be provided with simulation models. Thanks to the higher maximal electrical field, silicon carbide devices need shorter base to withstand a high voltage as compared to silicon ones. This means that unipolar devices may be used even for high blocking voltages, as voltage drop across a short base is still acceptable.

This explains why Schottky Barrier Diodes (SBD, see Fig. 5.17) are the only SiC power devices commercially available now, reaching as high ratings as 1,200 V and 20 A. This also makes device modelling easier because dynamic behaviour of SiC SBD may be modelled using lumped models. It is common to represent the SBD turn-off charge by means of a lumped voltage-dependent capacitance [42, 43] However, some authors suggest that 1D distributed models should be used [44] similar to the those used for silicon PIN diodes.

It is estimated that first SiC power transistors will be released to the market in 2010 [45]. Most probably they will be MOSFETs or JFETs which are already manufactured in laboratories. Again the unipolar device type and the short base make it possible to avoid modelling problems typical for silicon PIN diode, BJT, IGBT, and GTO, and to use lumped device models [46].

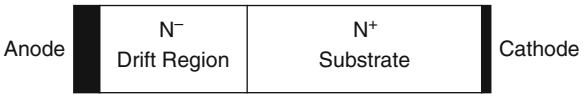


Fig. 5.17 SiC Schottky Barrier Diode (SBD) structure

In conclusion, as opposed to silicon power semiconductor devices, silicon carbide ones are easier to model as far as charge transport in transitory states is considered. On the other hand, another problem arises. It is assumed that the maximum operating temperature for SiC approaches 600°C. Modelling of material properties in such a wide temperature range is a complex issue that falls beyond the scope of this chapter. Several works have been published concerning physical phenomena identification and mathematical description [47, 48] as well as device model development and parameter extraction [49, 50].

Apart from temperature, another silicon carbide-specific phenomena must also be considered and modelled. This concerns e.g. the high carrier mobility anisotropy [51].

6 Conclusion

In this paper the most important phenomena in power semiconductor devices have been discussed. Unipolar devices such as power MOSFET are much more complex than their low power counterparts which makes it necessary to develop separate models. The good news, however, is that for unipolar devices this can be done by means of equivalent circuits which may be large but are composed of low power device models.

On the other hand, for bipolar power devices we found that:

- There is a problem with excess carrier diffusion modelling
- The accuracy of lumped models is very poor and insufficient in this case
- Therefore, for correct simulation distributed models are necessary
- New compact models [52] are very welcome as they combine proper carrier dynamics modelling, good accuracy and relatively short simulation times

In order to make it possible to easily simulate electronic circuits containing power semiconductor devices, a new type of the PIN diode model has been proposed. The results obtained seem to be very promising as far as accuracy and simulation time are concerned.

Recent power devices, both commercially available as the SiC SBD and expected in the nearest future, have introduced modelling problems of different nature. They are no longer connected with charge storage but rather with the wide operating temperature range and specific properties not encountered in silicon.

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Chapter 6
Distributed Modeling Approach Applied to the IGBT

Patrick Austin and Jean-Louis Sanchez

Abstract The carrier diffusion equation which retains the distributed nature of charge dynamics in power bipolar devices can be solved by means of an electrical analogy. This chapter presents the physical basis of the new modelling approach thus allowed, and its implementation in the case of IGBTs.

Keywords Power bipolar device modelling · IGBT

1 Introduction

At present, the demand for power electronics keeps rising as low power applications expand. This trend is certainly to be envisaged within the framework of a "sustainable development" approach. It calls for a better management of the energy source and for a permanent availability of systems. Thus, in the field of power electronics, design is based on such notions as yield and reliability. As a result, performance, reliability and integration requirements become increasingly important and correspond to the ongoing concerns of the research community. Power semiconductor devices must therefore remain efficient not only during normal operating conditions but also under extreme conditions. These are unusual operating conditions like transient overload, short circuit regime, electromagnetic field (EMF), system malfunctioning, high dI/dt and dV/dt. In these types of operation, devices are forced to operate to the limit leading to failures that may in turn bring about the destruction of the device or even, in the most serious cases, complete system breakdown.

To meet these constraints in the best possible way, the use of power systems computer-aided (CAD) design tools is essential. In this context, simulation is needed

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during the various phases of design of a new product. Virtual prototyping is now utilised to save time and costs. Models addressing all the events governing the operation of the different elements that make up the system, are needed.

Thus, the design and optimization of integrated power systems require the most realistic knowledge and modeling of semiconductor devices and of the different interactions occurring between the elements that compose the electric circuit performing the desired function. Taking into account the physical phenomena and nonlinearities involved in the power monolithic structures turns out to be essential.

The approach used to model the active devices (or structures) of power electronics is, therefore, crucial since it will condition the performance of design tools. Only a physical approach can enable us to reach an "ambitious" goal in terms of waveform prediction irrespective of the operating conditions and of the material environment at hand. This is our assigned objective with respect to the modeling of bipolar type power electronic devices and structures.

Power devices may be considered as an assembly of several physical or electrical regions. Thus, there are emitters, depleted zones, accumulation regions, etc.

For power devices, the voltage ranges involved require a vertical layout and low doping of the N^- type drift region. Generally, this region is referred to as base region. In terms of physical modeling, the main difficulty lies in taking into account the phenomena caused by carriers stored in this region which is naturally subject to high injection. This stored charge dynamics is inter alia the cause of the current delay relative to voltage during firing. The stored carrier dynamics in this region is described by the ambipolar diffusion equation. To solve this equation, two approaches giving rise to two types of models can be contemplated. The first type is referred to as the localised constant model while the other one is distributed. Distributed modeling leads to highly realistic results for voltage and current waveforms, irrespective of the applications envisaged and of the conditions of use.

The power bipolar device model described in this chapter, relies on a specific solution to the ambipolar diffusion equation allowing us to describe the distributed nature of the carrier dynamics occurring in the base region. The principle used is based on the fact that the solution $p(x, t)$ to the ambipolar diffusion equation can be regarded as a cosine decomposition of the Fourier series. This approach, which is similar to an analog method, can easily be embedded into all pieces of software dealing with circuit type simulation.

This chapter first describes an original method as well as the modeling of the different regions likely to be involved in a power structure. Then, IGBT-type device models are presented. At the end of this section, two straightforward examples of circuit are given to show the possibilities offered by this modeling. Bibliographic references are also given to enable the most interested readers to get further insights into this topic.

2 General Principles

2.1 Bipolar Device Problematic

To illustrate the issue raised by bipolar power devices, we rely on the insulated Gate Bipolar Transistor IGBT whose operating principle will be qualitatively detailed. At present, several IGBT technologies are commercially available. Here, "Non Punch-Through" (NPT) and "Punch-Through" (PT) structures that are the most commonly found and that support an academic presentation of the modeling principle for bipolar-type distributed devices will be reviewed. For information's sake, Field Stop IGBT (FS IGBT) [1], Stop Punch-Through IGBT (SPT IGBT) [2], High Conductivity IGBT (HiGT) [3] and the Trench IGBT [4] are also mentioned. For the latter technology, a distributed model has been developed [5] as well as PIN diode models [6].

IGBT is a triode type structure with two power electrodes (anode and cathode) and a control electrode (the gate). Therefore, it is a transistor whose switching is driven by the voltage applied to the gate. The design involves multiple cells and is similar to that of a power VDMOS. The only major difference between the two structures lies in the P^+ type emitting region on the anode contact. Figure 6.1 shows a basic NPT-type IGBT assembly with the corresponding electrical equivalent circuit. Section 5.1 details the differing behaviours of the two structures NPT and PT. There are five different semiconductor regions: P^+ and N^+ emitters, N^- type region, the P type well and the MOS section. Note that the N^- region is usually referred to as 'base'. It corresponds to the PIN diode intrinsic region, to the base of the thyristors and to the bipolar transistor collector region. In the case of the PT IGBT, there exists an N^+ layer sandwiched between the P^+ anode and the N^- base.

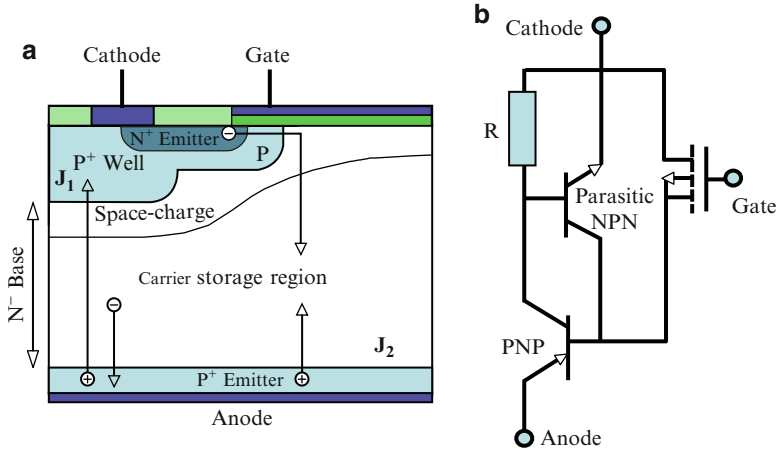

Fig. 6.1 (**a**) IGBT cell structure with carrier flowpath indicated and mains electrical regions. (**b**) Equivalent circuit of the IGBT

These semi-conducting regions highlight NPN and PNP bipolar transistors, an R_P resistance and an N channel MOSFET structure. The metallic short between the N^+ emitter and the P well allows the emitter/base junction of the NPN bipolar transistor to be 'desensitized'.

Under blocking conditions, it is the forward face junction (J_2 junction in Fig. 6.1) which is reverse-biased ($V_{AK} < 0$). The space charge zone stretches towards the N^- base region. Thus, the deeper and more less lowly-doped this region, the higher the holding voltage becomes. At on-state ($V_{AK} > 0$), minority carriers (holes) are mainly injected by the P^+ anode emitter and the electrons (majority carriers) by the MOS channel. This mechanism provides electronic neutrality in the centre N^- base region. As a result, a storage zone appears in the N^- region. This stored charge allows the on-state resistance to be decreased thereby decreasing as well the voltage drop (V_{on}). Given the low doping level of the N^- region, it undergoes high injection: the (p) hole concentration is equal to the (n) electron concentration, and crossover can only take place through a complete removal of carriers in the base region. Modeling this dynamic behaviour is key as it accounts for the switching losses.

Thus, in bipolar type devices, the N^- region plays a key role with respect to the blocking voltage capability, on-state waste voltage and dynamic performances. In other words, this region may be regarded as the 'core' of electrical mechanisms for static and dynamic modes. Other regions surrounding the base are destined to extract or inject from it the holes and electrons needed for conduction purposes. Usually, these different regions are much thinner (and more highly doped than the base region. For these two reasons, excess carriers could be disregarded relative to those in the base. The latter with a width W can then be divided into different electrical zones. One mainly gets the storage zone for excess carriers and the more or less depleted space charge zones. According to the type of base and the bias direction, it may be either a 'depleted' space charge zone or a drift zone in which carriers move mainly through conduction. The storage zone may thoroughly invade the base region as in the saturation mode. During switching modes, it decreases to the point of completely disappearing.

Figure 6.2 shows the carrier distribution in the base region of an NPT-IGBT at different times of a turn-off blocking switching transient. It highlights the (Q_S) carrier storage phenomenon and equally underlines two major behavioural aspects of the storage zone during switching. The first aspect is the distributed nature of electric phenomena and the second, the floating nature of the boundaries in the storage zone. Indeed, under saturation conditions, the boundaries coincide with the metallurgical junctions. However, during the desaturation phase, the space charge zone supporting the voltage drop extends towards the base. The boundaries of the storage zone of the excess carriers move from the metallurgical junctions towards positions (x_g) and (x_d) which maintain the holding voltage drop. The current I_{AK} crosses the structure and reaches zero when the charge (Q_S) has been fully deleted through recombinations.

The distributed nature of carriers $p(x)$ and the floating character of the borders in the storage zone are the main problems posed by bipolar device modeling. If

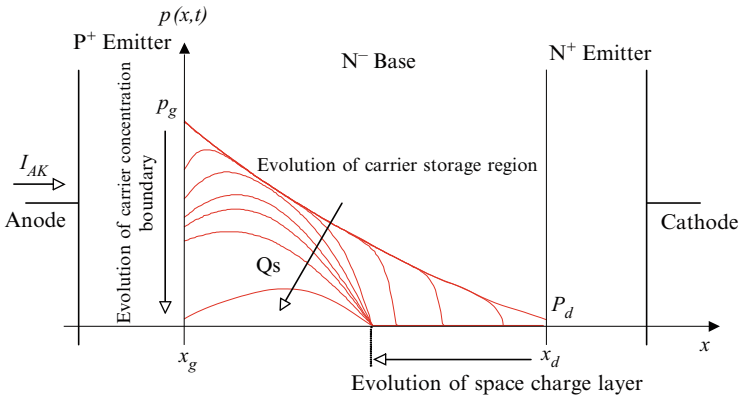

Fig. 6.2 Evolution of the carrier concentration distribution at turn-off in the N^- base's IGBT

modeling turns out to fairly easy to carry out for emitters, as well as the MOS section, the P well and the space charge zone through use of a conventional procedure, the task is not so easy when it comes to the storage zone which requires much more careful consideration.

2.2 What Modeling Approach Should Be Retained?

Within the framework of the development of simulation tools, three modeling approaches may be considered. The first one, referred to as *behavioural modeling* is particularly well-suited to a system perspective aiming to design quickly the electrical template of a function. *Physical models* allow for a particularly accurate description of the internal operation and are used to assess the impact of physical and geometrical parameters on the static and dynamic behaviour of the device. The last modeling approach corresponds to the so-called *finite elements method*. Although more cumbersome in terms of implementation, it enables us to validate ideas about structures and to determine new electrical interactions between different semiconductor regions of the device that might be taken advantage of in the crystal. Only the first two approaches can be used in circuit-type simulators.

At present, more than 150 models have been devised for the main power devices. The interested reader will find comparative studies of the main models in the literature [7–9].

Given the problematics of bipolar structures, only those models based on the internal physics of semiconductors can be considered. The first assumption deals with the (1D) nature of the carrier transport between terminal contacts. Following fundamental work by Shockley, Ebers, Mol and Spenke, etc., physical modeling of semiconducting structures has been organized around a local approach. This is the second assumption. Devices can be considered as different regions with steep

borders from which a number of approximations about fundamental charge transport equations can be made. The different regions can be physical (highly-doped emitters, MOS gates, buffer layers, etc.,) or electrical (space charge region, storage region, accumulation region, ...). These two modeling assumptions are retained within the framework of power bipolar devices.

Carrier distribution in the storage region is governed by the ambipolar diffusion equation (Eq. 6.1). This equation is quite conventional and can easily be derived from the expressions of current densities regarding holes and electrons.

$$\frac{\partial p(x,t)}{\partial t} + \frac{p(x,t)}{\tau} = D\frac{\partial^2 p(x,t)}{\partial x^2} \tag{6.1}$$

where $D = \frac{2D_n D_p}{D_n + D_p}$ is the ambipolar diffusion constant, and τ the carrier lifetime in the base region.

Boundary conditions that apply to the ambipolar diffusion equation change according to the structures studied and the operating conditions. Usually, they address carrier densities at the boundary or most often the concentration carrier gradient (see Fig. 6.3). The latter case will be used in this chapter. Concentration gradients are directly linked to the current densities at the boundary of the storage zone as shown in the equations given in Eq. 6.2 where D_n and D_p are the hole and electron diffusion constants in the N^- region and the active section S. $(J_{nd},\ J_{pd})$ and $(J_{ng},\ J_{pg})$ are the electron and hole current density couples flowing in and out of the base region (see Fig. 6.3). The latter are derived from the physical phenomena of the region adjacent to the storage region.

$$\begin{cases} f_g(t) = \left.\dfrac{\partial p(x,t)}{\partial x}\right|_{x_g} = \dfrac{1}{2qS}\left(\dfrac{I_{ng}}{D_n} - \dfrac{I_{pg}}{Dp}\right) \\ f_d(t) = \left.\dfrac{\partial p(x,t)}{\partial x}\right|_{x_d} = \dfrac{1}{2qS}\left(\dfrac{I_{nd}}{D_n} - \dfrac{I_{pd}}{Dp}\right) \end{cases} \tag{6.2}$$

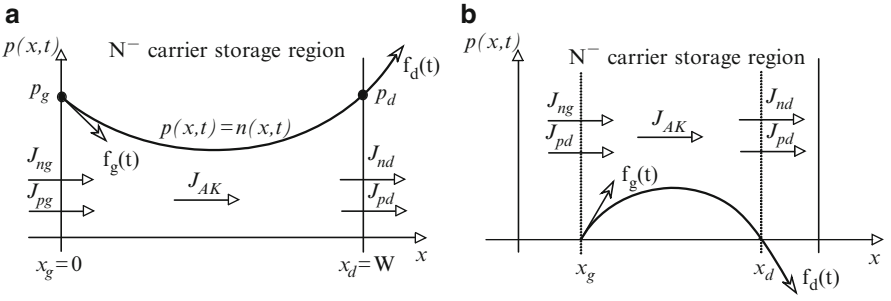

Fig. 6.3 Schematic view of stored carriers distributed in the base layer for a static condition (**a**) and during turn-off transient (**b**)

The solution to Eq. 6.1 is well-known for the static regime and allows us to get the analytical expressions of densities of electrons $J_n(x)$ and holes $J_p(x)$ moving in the base region as a function of the total current J_{AK} (with $J_{AK} = J_n(x) + J_p(x)$). For example, for the holes one gets:

$$J_p(x) \approx \frac{D_p J_{AK}}{D_n + D_p} + q\sqrt{\frac{D}{\tau}} \frac{p_g ch\left[\frac{W-x}{\sqrt{D\tau}}\right] - p_d ch\left[\frac{x}{\sqrt{D\tau}}\right]}{sh\left[\frac{W}{\sqrt{D\tau}}\right]} \tag{6.3}$$

Unfortunately, there is no analytical solution allowing us to give the function $p(x,t)$ for the dynamic regime. The main difficulty in the physical modeling of power bipolar structures is, therefore, due to carrier dynamics in the storage zone.

The first approach used to overcome this difficulty corresponds to what had been historically utilised within the framework of the modeling of macroelectronic devices dedicated to signal and information processing. This approach consists of integrating Eq. 6.1 over the base region. Thus, given the high injection regime, the integral leads to the differential, linear and first-order expression referred to as "charge control equation" (Eq. 6.4).

$$J_{nd} - J_{ng} = J_{pg} - J_{pd} = \frac{Q_s}{\tau} + \frac{\partial Q_s}{\partial t} \tag{6.4}$$

where $Q_s = q \int_{x_g}^{x} pdx$ stands for the stored charge in the base region.

This approach allows charge transport partial derivative equations to be reduced to regular differential equations, by deleting the state variable of position (x) through the variable Q_s. This approach holds as long as the variation of the charge stored according to time occurs quickly relative to the carrier lifetime (τ). This is the case of signal processing devices since bases are generally extremely narrow. In the models based on this approach, the evolution of the stored charge Q_s is taken into account as a whole without considering the real distribution of carriers $p(x)$ in the base. The current in the base region is then considered simply as proportional to the stored charge. In these conditions, the impact of the stored charge zone extension, and therefore, of voltage cannot be taken into account realistically. It is worth noting that the models developed according to this principle are called "quasi-static approximations" using, therefore, localised constants. However, unlike conventional microelectronic devices, and given the fact that transit times of power structures are of the order of magnitudes of the excitation periods (switching times), it follows that all the intricacies of interactions between the power device and the circuit cannot be reproduced by this type of model.

To try to improve the realism of quasi-static approximation models for bipolar structures, various solutions have been proposed. They are mainly based on breaking down the storage region into 'n' zones in which the aspect of the carrier distribution is considered as known and assimilated to affine straight lines or exponentials. Most frequently, the number of zones "n" seldom exceeds three for convergence reasons.

Nonetheless, the limitations of these enhanced quasi-static models are those inherent in the charge control models. However, power structures have been devised and are still in use today. The most famous example is the IGBT model developed by Hefner [10] which is currently held as the reference by the scientific community.

As a result, physical modeling must be supplemented by models taking into account more realistically the distributed aspects of the physical phenomena in this storage region. Therefore, an original method accounting for the distributed nature of carriers in the storage region has been developed. It relies principally on finding an analog solution to the ambipolar diffusion equation based on a Fourier's series decomposition of the carriers in the base [11]. Section 3 deals with the description of this original approach.

3 Principle Used for Solving the Ambipolar Diffusion Equation in the Base Region

In this section, we describe the method used to transform the ambipolar diffusion equation into a first-order, finite differential equation system. The latter can be considered as an equivalent electrical circuit of the RC type with time-varying parameters. The distributed effects of the stored charge can then be taken into account since this is equivalent to an analog method. This method which is easy to implement in a circuit type simulator, could be used to simulate specific power electronic circuits.

3.1 Discreet Transform of the Diffusion Equation

The approach assumes that the solution to the ambipolar diffusion equation (Eq. 6.1) can be written in the form of a cosine Fourier's series:

$$p(x,t) = V_0(t) + \sum_{k=1}^{\infty} V_k(t) \cos\left(\frac{k\pi(x - x_g)}{x_d - x_g}\right) \tag{6.5}$$

where:

- $V_0(t) = \frac{1}{x_d - x_g} \int_{x_g}^{x_d} p(x,t)dx$ mean value of $p(x,t)$ at time t
- $V_k(t) = \frac{2}{x_d - x_g} \int_{x_g}^{x_d} p(x,t) \cos\left(\frac{k\pi(x-x_g)}{x_d - x_g}\right) dx$ harmonic of rank k
- x_d and x_g the floating borders of the storage zone

Introducing Eq. 6.5 as solution $p(x,t)$ in the ambipolar diffusion equation (Eq. 6.1) and integrating onto the storage region between the floating borders x_g and x_d, one gets the equality given by Eq. 6.6.

$$\underbrace{D\int_{x_g}^{x}\left[\frac{\partial^2 p(x,t)}{\partial x^2}\cos\left[\frac{n\pi(x-x_g)}{x_d-x_g}\right)\right]dx}_{A} = \underbrace{\int_{x_g}^{x}\left[\cos\left(\frac{n\pi(x-x_g)}{x_d-x_g}\right)\frac{\partial p(x,t)}{\partial t}\right]dx}_{B} + \underbrace{\frac{1}{\tau}\int_{x_g}^{x}\left[\cos\left(\frac{n\pi(x-x_g)}{x_d-x_g}\right)p(x,t)\right]dx}_{c} \quad (6.6)$$

Following computations of A, B and C, the ambipolar diffusion equation reduces to an infinite system of first-order equations given by the equation system 6.7. The solution to this system leads to determining the amplitudes $V_n(t)$ of the Fourier's series decomposition yielding the carrier distribution $p(x,t)$.

$$\begin{cases} (x_d - x_g)\left(\frac{dV_0(t)}{dt} + \frac{V_0(t)}{\tau}\right) = D\left[f_d(t) - f_g(t)\right] \\ \qquad\qquad - \sum_{k=1}^{\infty} V_k(t)\left[\frac{dx_g}{dt} - (-1)^k \frac{dx_d}{dt}\right] \qquad \text{for } n = 0 \\ \frac{x_d - x_g}{2}\left\{\frac{dV_n(t)}{dt} + V_n(t)\left[\frac{1}{\tau} + \frac{Dn^2\pi^2}{(x_d-x_g)^2} + \frac{1}{4}\left(\frac{dx_d}{dt} - \frac{dx_g}{dt}\right)\right]\right\} \\ \qquad = D\left[(-1)^n f_d(t) - f_g(t)\right] \\ \qquad + \sum_{\substack{k=1 \\ k\neq n}}^{\infty} \frac{k^2}{k^2-n^2} V_k(t)\left[\frac{dx_g}{dt} - (-1)^{k+n}\frac{dx_d}{dt}\right] \quad \text{for } n \neq 0 \\ \text{Equation system} \end{cases} \quad (6.7)$$

3.2 Analogy with RC Lines

Looking at how the equation system 6.7 is expressed, it appears that it can be represented as a line of RC cells. Indeed, for a given rank n, the expressions are of the same form as that of Eq. 6.8 whose equivalent representation in terms of electric circuit is given by Fig. 6.4. Equation 6.8 describes the behaviour of a cell R_kC_k bridged by an inverse current I_k and supplied by an excitation current I_e.

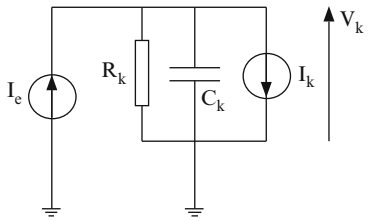

Fig. 6.4 Electrical diagram of an elementary cell of rank n and corresponding equation

Table 6.1 Expressions of coefficients R_n, C_n, $I_n(t)$ and $I_{ex.n}(t)$ for rank n

For rank n = 0	For ranks n
$\begin{cases} \mathrm{I}_{ex.0}(t) = D[f_d(t) - f_g(t)] \\ \mathrm{I}_0(t) = \sum_{k=1}^{\infty} V_k(t) \left[\frac{dx_g}{dt} - (-1)^k \frac{dx_d}{dt} \right] \\ \mathrm{C}_0 = x_d - x_g \\ \mathrm{R}_0 = \frac{\tau}{x_d - x_g} \end{cases}$	$\begin{cases} \mathrm{I}_{ex.n}(t) = D\left[(-1)^n f_d(t) - f_g(t)\right] \\ \mathrm{I}_n(t) = \sum_{\substack{k=1 \\ k \neq n}}^{\infty} \frac{k^2}{k^2 - n^2} V_k(t) \left[\frac{dx_g}{dt} - (-1)^{k+n} \frac{dx_d}{dt} \right] \\ \mathrm{C}_n = \frac{x_d - x_g}{2} \\ \mathrm{R}_n = \frac{2}{x_d - x_g} \frac{1}{\frac{1}{\tau} + \frac{n^2 \pi^2 D}{(x_d - x_g)^2} + \frac{1}{4}\left(\frac{dx_d}{dt} - \frac{dx_g}{dt}\right)} \end{cases}$

Thus the complete identification of the equation system 6.7, for all ranks n, leads to the determination of the expressions of terms $\mathrm{R_n}$, $\mathrm{C_n}$, $\mathrm{I_n}$ and $\mathrm{I_{ex.n}}$. Expressions are listed in Table 6.1 where $f_g(t)$ and $f_d(t)$ are given by Eq. 6.2.

$$C_k \frac{dV_k(t)}{dt} + \frac{\mathrm{I}}{\mathrm{R}_k} V_k(t) = \mathrm{I}_e(t) - \mathrm{I}_n(t) \tag{6.8}$$

$\mathrm{I_e}$ = excitation current
$\mathrm{I_k}$ = line inverse current

It is found that the excitation current $I_{ex.n}$ reverses as a function of the parity of rank n. To be able to maintain a representation per line RC in a circuit type simulator, one has to make a distinction in an RC line between odd and even rank cells. Excitation current are then given by the following analytical relations:

$$\text{pour } n \neq 0 : \begin{cases} \mathrm{I}_{n\ \mathrm{p}}(t) = D[f_d(t) - f_g(t)] & \text{for odd } n \\ \mathrm{I}_{n\ \mathrm{i}}(t) = -D[f_d(t) - f_g(t)] & \text{for even } n \end{cases}$$

Under saturated conditions, borders x_g and x_d are fixed. This is expressed mathematically by the following equation:

$$\frac{dx_g}{dt} = \frac{dx_d}{dt} = 0$$

The current generators $In(t)$ of rank "n" cells are then equal to zero. In this case, there exists an independence of cells relative to each other. For floating borders (desaturation regime), cells are interdependent.

The simulation of odd and even rank RC lines permits to determine the amplitudes $V_n(t)$ of harmonics in the Fourier's series decomposition of $p(x,t)$. For the desaturation regime, concentrations p_g and p_d at the borders x_g and x_d are close to the intrinsic concentration n_i. A control system will be implemented to maintain them at this level and enable the space charge zones to spread freely. This control system is detailed in the next paragraph.

Of course, one cannot consider an infinite number of cells. As a result, we must truncate the lines starting from a given rank N considered adequate for the accuracy

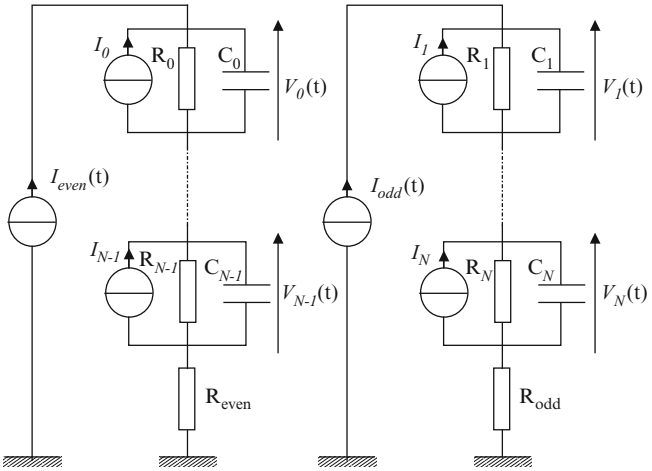

Fig. 6.5 Representation in the form of RC lines

desired (number of harmonics retained in the representation of $p(x,t)$). On each line a truncature resistance is added. These resistances given by Eqs. 6.9 and 6.10, are determined in order to find the exact analytical solution to $p(x)$ for the static regime since it exists. Finally, RC lines which are included in the circuit-type simulator are given in Fig. 6.5.

$$\mathrm{R}_{even} = \frac{1}{2}\sqrt{\frac{\tau}{D}}\frac{1+\cosh\left(\frac{x_g - x_d}{\sqrt{D\tau}}\right)}{\sinh\left(\frac{x_d - x_g}{\sqrt{D\tau}}\right)} - \sum_{\substack{k=0 \\ k\ \text{even}}}^{\mathrm{N}} \mathrm{R}_k \tag{6.9}$$

$$\mathrm{R}_{\mathrm{odd}} = \frac{1}{2}\sqrt{\frac{\tau}{D}}\frac{\cosh\left(\frac{x_g - x_d}{\sqrt{D\tau}}\right)-1}{\sinh\left(\frac{x_d - x_g}{\sqrt{D\tau}}\right)} - \sum_{\substack{k=1 \\ k\ \text{odd}}}^{\mathrm{N}} \mathrm{R}_k \tag{6.10}$$

It is then possible to retrieve the carrier concentrations (p_g and p_d) at the boundaries of the storage zone, the stored charge $Q_s(t)$ and the mean concentration of p_{base} carriers present in the storage zone. These magnitudes are given by the following analytical relationships:

$$p_d = p(x_d,t) = V_0(t) + \sum_{\substack{k=2 \\ k\ \text{even}}}^{N} V_k(t) - \sum_{\substack{k=1 \\ \text{odd}}}^{N} V_k(t) \tag{6.11}$$

$$p_g = p(x_g,t) = V_0(t) + \sum_{k=1}^{N} V_k(t) \tag{6.12}$$

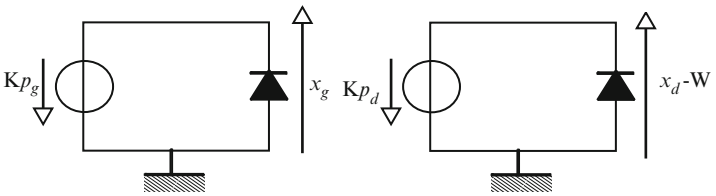

Fig. 6.6 Implementation of the control mechanism for carriers p_g and p_d

$$Q_s(t) = q \int_{x_g}^{x_d} p(x,t)dx = q(x_d - x_g)V_0(t) \tag{6.13}$$

$$p_{base} = \frac{Q_s}{p_d(t) - p_g(t)} \tag{6.14}$$

3.3 Evolution of the Boundaries Position with the Aid of a Control Mechanism on the Carrier Concentration

The borders of the storage zone are fixed if the base is fully immersed into the carriers (saturation regime). They become mobile when the base operates under desaturation conditions. The control system shown in Fig. 6.6 is a good illustration of this.

In the case of the saturation regime, carrier concentrations $p_g(x_g = 0)$ and $p_d(x_d = \mathrm{W})$ are positive and largely in excess of the intrinsic concentration $\mathrm{n_i}$ (see Fig. 6.3a). The x-axes of the border positions coincide with the metallurgical junctions defining the storage zone. The D diodes are then operating under on-state conditions and the voltages across their terminals, which reflect the orders of magnitude $x_g(t)$ and $(\mathrm{W} - x_d(t))$, are considered as zero.

The desaturation regime occurs precisely when a carrier depleted zone is formed on either side of the storage zone (see Fig. 6.3b). The moving position x-axes x_g and x_d of the borders allow the p_g and p_d carrier concentrations to be kept close to zero. Diodes D are blocked and voltages across the terminals reflect the evolution of the depleted zones whilst maintaining the border concentrations close to zero. The diode parameters are selected to be as ideal as possible.

4 Modeling the Other Electrical Regions

Using the charge dynamics in the base region derived from the behaviour of the RC lines, power device modelling can be achieved through the assembly of the physical and electrical regions involved in the operation of the structure. For the IGBT, in addition to the carrier storage region, one gets:

– The depleted space charge zone
– P^+ and N^+ emitters
– The MOS section
– The P^+ well

This paragraph deals with the modeling of these four regions. One part also will be devoted to the way in which the thermosensitive parameters are taken into account. Finally, the different electric potential drops across the terminals will be considered in Section 4.6.

4.1 Modeling the Space Charge Zones

Two types of space charge zones must be considered: the so-called "drift" zones and the depleted regions. In the space charge zones, carriers move mainly through conduction. The depleted area corresponds to a conventional reverse-biased junction transition zone (see Fig. 6.7a) whereas the drift zone corresponds to an electronic conduction whose behaviour is quasi-ohmic (see Fig. 6.7b).

The variation of the electrical field E causes a variation of the storage zone width. This is due to the extraction of holes or electrons from the storage zone. This triggers a displacement current J_{dep} which overlays the already existing currents. The displacement current expressions are obtained by integrating the Poisson's equation over the space charge regions considered. Thus, Eqs. 6.15 and 6.16 show the integration boundaries of the displacement current in a depleted region and in a drift region, respectively. It is worth pointing out that in the case of a reverse-biased IGBT, there exists a depleted zone on the P^+ anode side in lieu of the drift zone.

$$I_{dep} = \varepsilon_{si} S \frac{\partial E_{\max}}{\partial t} = -S \frac{d}{dt} \int_0^{x_g} \rho(x) dx \tag{6.15}$$

$$I_{dep} = \varepsilon_{si} S \frac{\partial E_{\max}}{\partial t} = -S \frac{d}{dt} \int_{x_d}^{W} \rho(x) dx \tag{6.16}$$

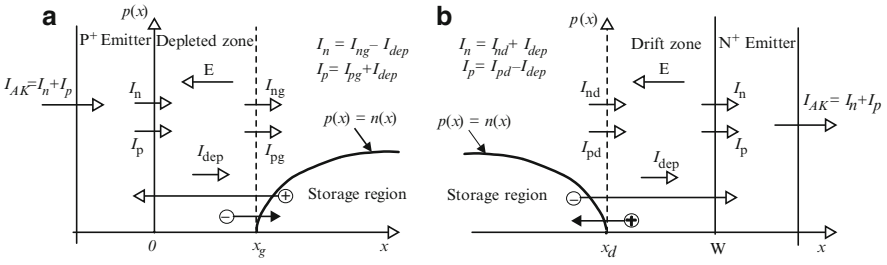

Fig. 6.7 Transport mechanisms in a depleted region (**a**) and in a drift region (**b**)

If one considers that the carriers move at their limit velocity (v_{plim} for holes and v_{nlim} for electrons), then the total charge density is given by:

$$\rho = q \cdot \left(N_D^+ - \frac{|J_n|}{q \cdot v_{n\,\mathrm{lim}}} + \frac{|J_p|}{q \cdot v_{p\,\mathrm{lim}}} \right) \tag{6.17}$$

where J_n and J_p are the electron and hole currents flowing in the space charge zone and $N_D{}^+$ the positive ion concentration of the base region.

To compute the displacement currents, one only needs to consider the additional carriers linked to the variation of the field E in the transient phases. Thus, for the depleted space charge zone, the charge density to be considered is given by Eq. 6.18.

$$\rho = q \cdot \left(N_D^+ + \frac{|J_p|}{q \cdot v_{p\,\mathrm{lim}}} \right) \tag{6.18}$$

For the drift zones, the influence of carriers in transit can be taken into account if the density of current flowing through the zone is in excess of a certain critical value $|J_{critique}| = q.N_d.v_{n\,\mathrm{lim}}$. The density of the charges in this zone can then be given by the following formula:

$$\rho = q \cdot \left(N_D^+ - \frac{|J_n|}{q \cdot v_{n\,\mathrm{lim}}} \right) \tag{6.19}$$

4.2 Modeling Emitters

Usually, the role of an emitter is to act either as an ON-state junction for majority carriers and blocking junction for minority carriers. The parameter accounting for this particular situation is referred to as emitter surface recombination parameter. Denoted h, it is used to compute the minority current (I_{min}) that flows into the junction between two semi-conducting regions. In this case, the emitter is regarded as a recombinant surface. The diagram below depicts the charge transport mechanisms at the junction between the emitting P^+ region and an N^- region (storage region) as shown in Fig. 6.8a. Figure 6.8b shows the particular case of an emitter with a buffer layer in a PT-IGBT.

The use of this formalism h enables us to account for the behaviour of emitters through Eq. 6.20 which yields the minority current I_{min}:

$$I_{\mathrm{min}} = q \cdot h \cdot S \cdot \left[(p \cdot n) - {n_i}^2 \right] \tag{6.20}$$

As reported in [12, 13] parameter h acts as a typical constant depending on the physical parameters of the two juxtaposed regions. An expression of this parameter h is given below in the case of a P^+ type emitter:

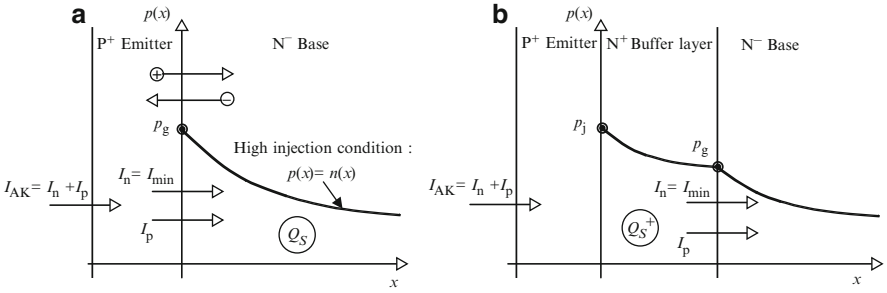

Fig. 6.8 Charge transport mechanisms at the simple emitting junction (**a**) and at the emitting junction with a buffer layer (**b**)

$$h = \frac{D_n}{N_A} \cdot \frac{{n_i}^2|_P}{{n_i}^2|_N} \cdot \left[\frac{1}{\sqrt{D_n \cdot \tau_n}} \cdot \coth\left(\frac{W_P}{\sqrt{D_n \cdot \tau_n}} \right) \right] \tag{6.21}$$

where W_P, N_A, D_n and τ_n stand for depth, concentration, diffusion constant and lifetime of electrons in the P^+ emitter.

According to the technology used, three categories of emitters can be found:

- Conventional, highly-doped emitters. These structures are not much affected by temperature and exhibit doping concentrations in excess of $10^{18}\,\mathrm{cm}^{-3}$. Thus, recombination coefficient may vary from 10^{-14} to $3.10^{-14}\,\mathrm{cm}^4/\mathrm{s}$.
- Thin, highly-doped emitters are known as semi-transparent. They feature concentrations between 10^{16} and $10^{18}\,\mathrm{cm}^{-3}$. Their depth is less than $2\,\mu\mathrm{m}$. They allow for the injection to be limited in the base of IGBTs or fast diodes. The value of h is much more elevated than in conventional emitters and may vary from 10^{-11} to $10^{-13}\,\mathrm{cm}^4/\mathrm{s}$.
- Emitters associated with a buffer layer as in the case of PT-IGBTs. The inclusion of this additional, moderately-doped N^+ layer is used to reduce the thickness of the wide lowly-doped base while maintaining a high avalanche breakdown voltage. Thus, injection and, therefore, the computation of the electron current are carried out at the interface between the N^+ buffer layer and the N^- base. This minority current defines the boundary conditions for the storage zone. This minority current is the sum of the conventional emitter recombination current and the buffer layer recombination current (Eq. 6.22). In the following expressions, parameters with superscript (+) are specific to the buffer layer.

$$I_n = q \cdot h \cdot S \cdot N_D^+ \cdot p_j + \frac{Q_s^+}{\tau_p^+} + \frac{\mathrm{dQ}_s^+}{dt} \tag{6.22}$$

The charge stored in the buffer layer, ${Q^+}_s$, and hole concentration p_j at the buffer layer boundary on the P^+ emitter are given for Eqs. 6.23 and 6.24, respectively. ${L^+}_p$ is the hole diffusion length, ${D^+}_p$ the diffusion constant, W^+ the buffer layer width and ${\tau^+}_p$ the hole lifetime.

$$Q_s^+ = q \cdot S \cdot L_p^+ \cdot \frac{p_j + p_g}{sh\left(\frac{W^+}{L_p^+}\right)} \left[ch\left(\frac{W^+}{L_p^+}\right) - 1 \right] \tag{6.23}$$

and

$$p_j = \frac{I_{AK}/S + q \cdot \sqrt{\frac{D_p^+}{\tau_p^+}} \cdot \frac{p_g}{sh\left(\frac{W^+}{L_p^+}\right)}}{q \cdot \sqrt{\frac{D_p^+}{\tau_p^+}} \cdot \coth\left(\frac{W^+}{L_p^+}\right) + q \cdot h \cdot N_d^+} \tag{6.24}$$

The assumption used to establish these equations is based on the space charge transport equations under a static behaviour. For a dynamic state, they can nevertheless be utilised when the charge $Q^+{}_s$ stored by the minority carriers in the N^+ emitter is negligible relative to the stored charge Q_s in the storage zone. This is definitely the case for power structures.

4.3 Modeling the MOS Section

The model used for the MOS section is directly linked to the theory of VDMOS transistors [14, 15]. The VDMOS model can be adapted by linking the Drain part to the carrier storage region.

Like any MOS type structures, a distinction must be made between three types of operating modes under static conditions. First, the ohmic type is triggered when the gate voltage exceeds the threshold voltage V_{th} and for a drain voltage less than the Punch-Through voltage V_P. The second type, the saturated state, corresponds to a situation where the gate voltage exceeds the threshold voltage V_{th} while the drain voltage exceeds the Punch-Through voltage V_P. The third case is that of a gate voltage less than the threshold voltage. These regimes are expressed as follows:

$$I_{mos} = K_P \cdot \left[(V_{GS} - V_{th})\, V_{DS} - \frac{V_{DS}^2}{2} \right] \quad \text{if } V_{GS} > V_{th} \text{ and } V_{DS} < V_P \tag{6.25}$$

$$I_{mos} = K_P \cdot \left[(V_{GS} - V_{th})\, V_P - \frac{V_P^2}{2} \right] \quad \text{if } V_{GS} > V_{th} \text{ and } V_{DS} > V_P \tag{6.26}$$

$$I_{mos} = I_{sn0} \cdot \left[\exp\left(\frac{-|V_{DS}|}{U_t}\right) - 1 \right] \quad \text{if } V_{GS} < V_{th} \tag{6.27}$$

where K_p stands for the form factor given by:

$$K_p = \mu_N \cdot C_{ox} \cdot \frac{Z}{L} \tag{6.28}$$

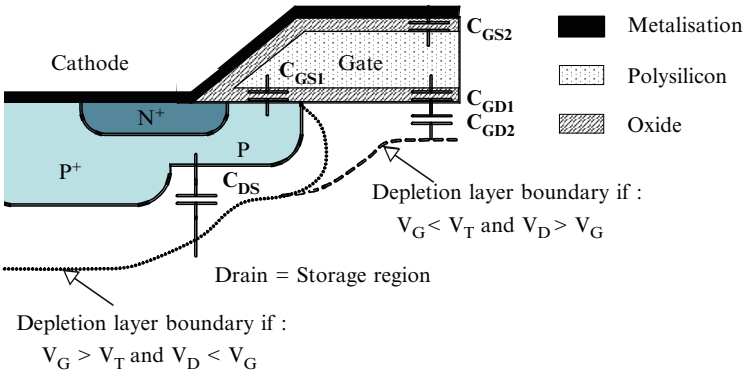

Fig. 6.9 Locations of the different MOS capacitances as a function of the gate and drain voltages

V_p is the Punch Through voltage given by:

$$V_p = \psi_{Xref} \cdot \left[\sqrt{1 + 2 \cdot (V_G - V_T)/\psi_{X\,ref}} - 1 \right] \tag{6.29}$$

where μ_N is the electron mobility in the channel, C_{ox} the gate oxide capacitance, Z the channel width developed and L the channel length. Reference voltages ψ_{Xref} and ψ_{Yref} are used to assess the effects of reduced carrier mobility in the channel due to the longitudinal and transverse electric fields, respectively. The current I_{sn0} is set to 1.10^{-12} A.

Dynamic behaviour is governed by the capacitances' storage and depletion mechanisms as shown in Fig. 6.9. The gate source capacitance (C_{GS}) can be separated into two capacitances (C_{GS1}) and (C_{GS2}). The first one, corresponding to the overflow capacitance of the gate zone on the source diffusion, and the second, to the capacitance defined by the thick oxide between the source metallization and the gate electrode. These capacitances are classically computed by using the geometric size of the oxide and are unrelated to the voltage across the terminals of the MOS section.

The dynamic gate/drain capacitance (C_{GD}) corresponds to the series connection of an oxide capacitance (C_{GD0}) and a space charge capacitance (C_{GD1}) that develops with the voltage increase. It accounts in particular for Miller's effect and offers a constant value (C_{GD0}) as long as the drain voltage remains less than the voltage applied to the gate. Then, it develops in accordance with a law directly derived from that which gives the transition capacitance of a diode operating under reverse conditions:

$$C_{GD} = \frac{C_{GD0}}{\sqrt{1 + (V_D - V_G)/\Phi_{GD}}} \tag{6.30}$$

with

$$\phi_{GD} = \frac{S_I{}^2}{C_{GD0}{}^2} \cdot \frac{q \cdot N_D \cdot \varepsilon_{SI}}{2} \tag{6.31}$$

where S_I stands for the total intercell surface of the device, ε_{si} is the permittivity of silicon, V_D and V_G the potentials applied to the drain and gate.

As long as $V_D < V_G$, the capacitance (C_{GD}) reduces almost to the intercell oxide capacitance (C_{GD0}). When $V_D > V_G$, the then-depleted space charge exhibits a thickness which increases significantly as the square root of voltage. For high voltages V_D, the gate/drain capacitance (C_{GD}) is one with the space charge capacitance.

The source/drain capacitance (C_{DS}) corresponds to the transition capacitance of the drain junction. The latter is nonlinear and depends on the drain voltage V_{DS} and on capacitance (C_{DS1}). Its differential value (C_{DS}) is, as a first analysis, given by the following formula:

$$C_{DS} = \frac{C_{DS0}}{\sqrt{1 + V_{DS}/\phi_{DS}}} \tag{6.32}$$

where ϕ_{DS} is the diffusion voltage of the box/base region junction.

4.4 Modeling the P/P^+ Well [16]

The P well of IGBTs undergoes a number of phenomena that greatly affect electrical behaviour. Indeed, it is within this well that the hole current I_{lat} flows laterally. This causes thyristor parasitic triggering of the IGBT (latch-up phenomenon).

Figure 6.10 shows the topology of a basic cell's P well. Electrically, it can be assimilated to a transverse resistance known as gate/cathode resistance R_{GKcell}. The cathode and P well are connected directly through a surface short. At a certain current level I_{lat}, the voltage across the terminals of this resistance exceeds the threshold voltage of the junction (J_3) and the latter operates in a direct bias mode. The NPN transistor becomes active and supplies the basic current to the PNP transistor which in turn supplies the base of the PNP transistor. The parasitic thyristor becomes effective and the IGBT can no longer be controlled. Equation 6.33 yields the expression of resistance R_{GKcell}

$$R_{GKcell} = \frac{1}{q \cdot \mu_P \cdot N_a} \cdot \frac{L_P}{P_P \cdot W_{cell}} \tag{6.33}$$

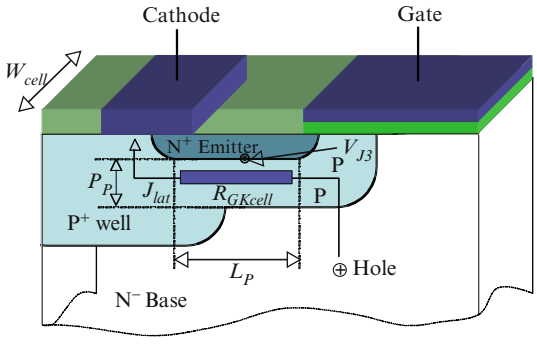

Fig. 6.10 Lateral current flow in the P^+ well inducing "latch-up"

where L_P, P_P and W_{cell} are respectively, the length, depth and width of the P well of a basic cell. μ_P stands for the mobility of holes in the P well and N_A is the mean well concentration.

4.5 Temperature Dependence of the Parameters

The operation of power structures systematically gives rise to a temperature variation in the system. This directly impacts thermosensitive parameters like intrinsic concentration, carrier lifetime and mobility. Therefore, to model the dynamic and static behaviours as accurately as possible, one must take into account the variation of thermosensitive parameters [17, 18]. By way of example, a number of these parameters used in the models are presented below.

4.5.1 Intrinsic Concentration n_i

The empiric formulation has been retained for intrinsic concentration:

$$n_i(T) = 3,1.10^{16} \cdot T^{3/2} \exp\left(\frac{-0,603}{kT}\right) \tag{6.34}$$

with k, Boltzmann's constant ($1.380,662 \times 10^{-23}\,\mathrm{J \cdot K^{-1}}$).

4.5.2 Carrier Lifetime τ

Without going into all the intricacies of recombination mechanisms, it is commonly admitted that the lifetime variation is fairly sensitive to the temperature effects. This variation can be assessed with the following equation:

$$\tau = \tau_0 \cdot \left(\frac{T}{300}\right)^{\alpha_\tau} \tag{6.35}$$

where τ_0 is the carrier lifetime at 300 K. Coefficient α_τ depends mainly on the nature of the recombinant centres used to control lifetime. Gold or platinum doping and irradiation by electrons or protons are the two techniques used to control lifetime. In the first case, a typical value of α_τ is 2 to 2.5 whereas in the second α_τ will be equal to 1.5 on the whole.

4.5.3 Carrier Mobility μ

Carrier mobility results from the interactions between carriers themselves and with the lattice network and doping impurities. Each interaction is governed by a

temperature-dependent law. With respect to lowly-doped semiconductors, carrier mobility is mainly limited by their interactions with the network. However, for more important dopings, interactions due to ionized impurities present in the network are taken into account. With respect to carrier interactions (*carrier–carrier scattering*), the concentrations of the modeled regions are not sufficiently high to take them into account. The following relationship is used to model the hole and electron mobility variation of these two types of interactions.

$$\mu_{A,D} = \mu_{1_{A,D}} \cdot \left(\frac{T}{300}\right)^{\alpha_{A,D}} + \frac{\mu_{2_{A,D}} \cdot \left(\frac{T}{300}\right)^{\beta_{A,D}}}{1 + \frac{N_{A,D}}{N_{c_{A,D}} \cdot \left(\frac{T}{300}\right)^{\gamma_{A,D}}}} \tag{6.36}$$

with $N_{A,D}$ being the concentration of the region considered.

4.5.4 Carrier Limit Velocity

When an electric field is created in a semiconductive region, carriers accelerate. Their velocity is a function of the electric field value and differs between electrons and holes. For field values in excess of 10^5 V/cm, this velocity is saturated by the interactions between carriers and with the lattice network. The saturation rate corresponds to 1.7×10^7 cm/s for electrons ($V_{nsat\ 0}$) and 0.834×10^7 cm/s for holes ($V_{psat\ 0}$). The velocity variation is a function of temperature for electrons and holes and given by Eqs. 6.37 and 6.38 respectively.

$$V_{n\ sat} = V_{n\ sat0} \cdot \left(\frac{T}{300}\right)^{-0,87} \tag{6.37}$$

$$V_{p\ sat} = V_{p\ sat0} \cdot \left(\frac{T}{300}\right)^{-0,52} \tag{6.38}$$

4.6 Total Voltage Drop Across the Terminals of an Assembly

Total voltage drop across the terminals of an assembly is the summation of different voltage drops across the terminals of the various regions. The total current I_{AK} flowing through the structure is computed so that the voltage drop V_{AK} across the terminals of the device complies with its internal equations and the operating conditions imposed by the surrounding environment. This method is said to be implicit and only a circuit-type simulator can implement it.

Four types of voltage drops can be found in a structure according to the nature of the region considered:

– Voltage V_j of a direct-bias P/N junction
– Voltage drop V_{base} across the terminals of the storage zone

– Voltage V_{ZCE} supported by the space charge zone
– Voltage V_{drift} supported by a drift region

4.6.1 Voltage V_J

The voltage drop of a direct bias P/N junction is classically computed using the regular "*Boltzmann*" equation:

$$V_J \approx U_T \cdot \ln\left(\frac{(pn)_J}{{n_i}^2}\right) \tag{6.39}$$

where $(pn)_J$ is the product of concentrations at the metallurgical junction and U_t the thermodynamic voltage. It is worth pointing out that under reverse bias conditions, voltage drop across the terminals of the junction corresponds to that obtained across the terminals of a space charge structure.

4.6.2 Voltage V_{base}

The storage region can be assimilated to a conductivity modulated resistance. The voltage drop V_{base} can be expressed as a function of the carrier densities $n(x)$, $p(x)$ and hole and electron current components $J_n(x)$, $J_p(x)$. Classically, this voltage drop can be formulated as follows:

$$V_{base} \approx \int_{x_g}^{x_d} \frac{J_n}{q \cdot \mu_n \cdot n} dx = \int_{x_g}^{x_d} \frac{J_p}{q \cdot \mu_p \cdot p} dx \tag{6.40}$$

By disregarding the electric field in the regular expressions yielding current densities on electrons (J_n) and holes (J_p), one gets the conventional equation (Eq. 6.41). Starting from this equation and considering, on the one hand, the high injection base region and, on the other, that $J_{AK} = J_n + J_p$, Eq. 6.40 can be written in the form given by Eq. 6.42.

$$p\frac{J_n}{D_n} - n\frac{J_p}{D_p} = q\frac{\partial(pn)}{\partial x} \tag{6.41}$$

$$V_{base}\frac{J_{AK}}{q} \cdot \int_{x_g}^{x_d} \frac{dx}{\mu_n \cdot N_D + (\mu_p + \mu_n)\cdot} + U_T \cdot \int_{x_g}^{x_d} \frac{\frac{\partial(pn)}{\partial x}}{n \cdot \left(p + n \cdot \frac{D_n}{D_p}\right)} dx \tag{6.42}$$

It appears that V_{base} is the sum of a purely ohmic voltage V_Ω and a so-called "Dember" voltage V_{dember}. These voltages are given by Eqs. 6.43 and 6.44, all computations being made.

$$V_{\Omega} = \frac{J_{AK}}{q} \cdot \frac{x_D - x_G}{\mu_n \cdot N_D + (\mu_n + \mu_p) \cdot p_{base}} \tag{6.43}$$

and

$$V_{dember} = 2 \cdot U_T \cdot \frac{D_p}{D_n + D_p} \cdot \ln\left[\frac{p_d}{p_g}\right] \tag{6.44}$$

where p_{base} stands for the mean value of excess carriers in the storage zone given by Eq. 6.14.

4.6.3 Voltages V_{ZCE}

The voltage supported by the depleted space charge zone can be regularly computed by integrating Poisson's equation. This integral is solved by considering, on the one hand, the approximation of steep boundaries and, on the other, that carriers transit at their maximum velocity V_{nsat} and V_{psat}. In addition, as the doping levels of junctions are highly dissymmetric, all the space charge supported develops in the N^- base region. Equation 6.45 stands for the voltage supported by a space charge zone which develops on the left of the storage zone. Equation 6.45 corresponds to a possible space charge on the left of the storage zone and Eq. 6.46 on the right. The charge density is given by Eq. 6.17.

$$V_{ZCEg} = \int_0^{x_g} \int_x^{x_g} \frac{\rho(u)}{\varepsilon_{si}} du \tag{6.45}$$

and

$$V_{ZCEd} = \int_{x_d}^{W} \int_x^{W} \frac{\rho(u)}{\varepsilon_{si}} du \tag{6.46}$$

Similarly, since the drift zones correspond to purely resistive regions, the voltage drops in these zones can be computed directly using Eqs. 6.47 and 6.48.

$$V_{driftg} = J_n \cdot \int_0^{x_g} \frac{dx}{q\mu_n N_D} \tag{6.47}$$

and

$$V_{driftd} = J_n \cdot \int_{x_d}^{W} \frac{dx}{q\mu_n N_D} \tag{6.48}$$

5 Modeling PT-IGBT

5.1 Construction of IGBT Model

Figure 6.11 is a cross-sectional view of a half IGBT-NPT on which the convention used for the currents of the various regions is added. The complete IGBT model is therefore established from the assembly of the regions that make it up. This assembly is achieved by taking into account the continuity between adjacent regions. These continuities relate to:

– The carrier concentration product (pn) at the boundaries
– Current densities taking into account the displacement current item associated with space charge variations

For the NPT-IGBT, P^+ and N^+ type emitters supply the current pairs (I_{nEP}, I_{pEP}) and (I_{nEN}, I_{pEN}), the left and right space charge zones, particularly for displacement currents I_{depg} and I_{depd}, the MOS section whose channel current is denoted I_{mos} and the P/P^+ well involving the lateral current I_{lat} and currents I_{pc} and I_{nc} provided by the P_{well}/N^- base junction. By way of example, Table 6.2 lists the equations derived from the assembly rules for the NPT-IGBT.

The PT-IGBT, allow us to obtain lower on-state voltage drops than for NPT-IGBT while preserving identical break-down voltage. Indeed, the addition of a buffer layer reduces the thickness of the base region leading as well to a reduction of the apparent resistance during the conduction phase. In this type of device, the electrical field

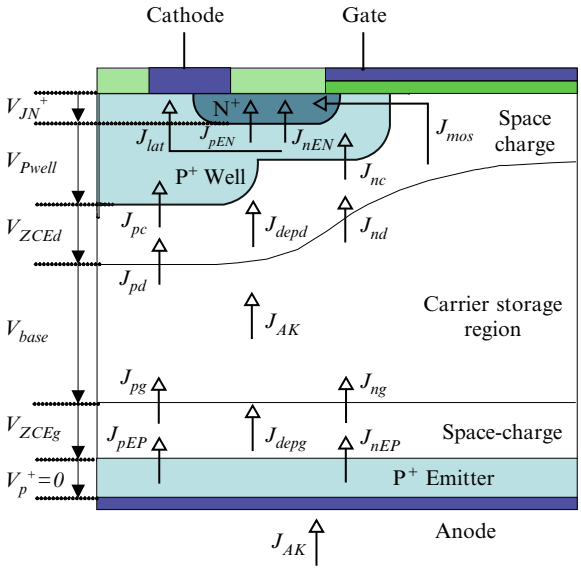

Fig. 6.11 NPT-IGBT half-cell with current convention and voltage drop

Table 6.2 Current continuity equations and voltage summation for a NPT-IGBT model

Current continuity	Voltage summation
$J_{ng} = J_{nEP} + J_{depg}$	$V_{AK} = V_{zceg} + V_{zced} + V_{base} + V_{Pwell} + V_{JN+}$
$J_{pg} = J_{AK} - J_{ng}$	$V_{zceg} = V_{Jg} - \left(q \cdot N_D \cdot + \frac{\lvert J_{pg}\rvert}{v_{p\,\lim}}\right) \cdot \frac{{x_g}^2}{2\varepsilon_{si}}$
$with\ \ J_{depg} = -q \cdot N_D \cdot \frac{dx_g}{dt} - \frac{1}{v_{p\,\lim}} \cdot \frac{d}{dt}\left(x_g \cdot \lvert J_{pg}\rvert\right)$	
$J_{nd} = J_{nc} + J_{mos} + J_{depd}$	$V_{zced} = -V_{Jd} + \left(q \cdot N_D \cdot + \frac{\lvert J_{pd}\rvert}{v_{p\,\lim}} - \frac{\lvert (J_{nc}+J_{mos})\rvert}{v_{p\,\lim}}\right) \cdot \frac{{x_d}^2}{2\varepsilon_{si}}$
$J_{pd} = J_{AK} - J_{nd}$	
$with\ \ I_{depd} = q \cdot N_D \cdot \frac{dx_d}{dt} + \frac{1}{v_{p\,\lim}} \cdot \frac{d}{dt}\left(x_d \cdot \lvert J_{pd}\rvert\right) - \frac{1}{v_{n\,\lim}} \cdot \frac{d}{dt}\left(x_d \cdot \lvert (J_{nc} + J_{mos})\rvert\right)$	$V_{Jg} = 2 \cdot U_T \cdot \ln\left(\frac{p_g}{n_i}\right)$
$J_{pc} = J_{AK} + J_{pEN}$	$V_{Jd} = 2 \cdot U_T \cdot \ln\left(\frac{p_d}{n_i}\right)$
$J_{nc} = J_{nEN}$	$V_{Pwell} = R_{verticalwell} \cdot \left(I_{nEN} + I_{pEN}\right)$
$J_{AK} = J_{pd} + J_{depd} - J_{pEN}$	$V_{J3} = R_{lateralwell} \cdot I_{lat}$

distribution is no longer triangular as in the case of the NPT-IGBT, but assumes a trapeze shape. In these conditions, the base depth can be one-half ratio while maintaining a breakdown voltage of the same order of magnitude. The second benefit of the buffer layer is the lower efficiency of the P^+ anode injection. With these two effects, i.e., reduced thickness of the base region and injection efficiency, the charge stored is diminished, thereby leading to a gain in terms of firing time relative to NPT-IGBT. Nevertheless, for very high breakdown voltage, the latter technology is preferred. The PT-IGBT model is identical to that of the NPT-IGBT except for the modifications of injected currents in the anode side base. These modifications are carried out by adding the (N^+) buffer layer through the buffer emitter which delivers the current I_n given by the Eq. 6.22.

5.2 Simulation Results

Simulation results have been obtained by using commercially available IGBT structures. The values of model parameters can be found on datasheets provided by manufacturers and by means of inverse engineering processes. Two types of simulation are carried out, one dealing with the static state, the other with the dynamic state.

5.2.1 Static Regime

Figure 6.12a and b show the output characteristic networks $I_{AK} = f(V_{AK})$ for temperatures of 300 and 400 K, respectively. Figure 6.13a shows the breakdown voltage, corresponding to the avalanche breakdown modeled by the Miller's empirical Eq. 6.49.

$$BV = 2,93.10^{12} \cdot N_D^{-2/3} \tag{6.49}$$

where N_D is the doping value of the base region.

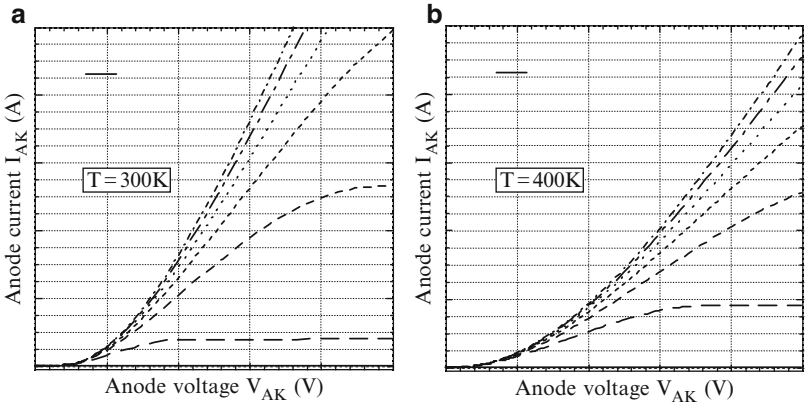

Fig. 6.12 Simulated static characteristics for: (**a**) T = 300 K, and (**b**) T = 400 K

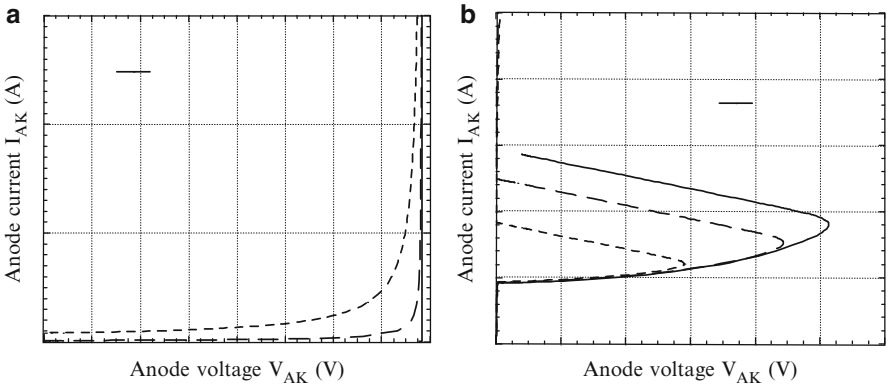

Fig. 6.13 (**a**) Simulated IGBT avalanche characteristic and (**b**) simulated IGBT Latch up characteristic

The latch-up phenomenon corresponds to the firing of the parasitic thyristor. This one is very much dependent on the mean P/P^+ well concentration which sets the value of the resistance R_{GKcell} given by Eq. 6.33. Figure 6.13b shows temperature-dependent firing for a given P-well doping.

5.2.2 Dynamic Regime

The circuit used for the dynamic regime is given in Fig. 6.14. This type of circuit is highly popular among manufacturers to evaluate the various dynamic performances. The free wheel diode utilised for simulation purposes is ideal (zero recovery time, under direct and reverse conditions). Inductance L_f is high and behaves as an ideal

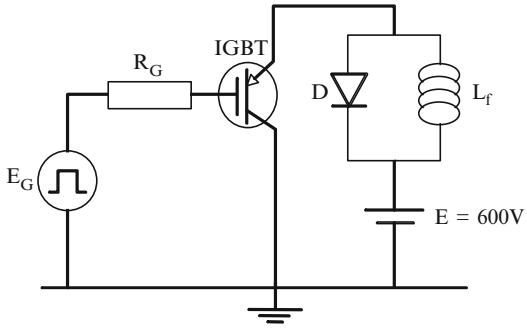

Fig. 6.14 Circuit used for simulated the dynamic regime

current source. The control circuit and the charge feature no parasitic elements. Switched current is 50 A and maximum voltage 600 V. The gate control source delivers trapeze-shaped waves of ± 15 V with rise and fall fronts of 10 ns. The gate resistance is 22Ω and simulations are performed at 300 K.

5.2.3 Simulation of the Turn-On Dynamic

The diagrams shown in Fig. 6.15 give the simulation results obtained during the turn-on phase. Figure 6.15a shows the evolution of the gate voltage, Fig. 6.15b the evolution of V_{AK} voltage and I_{AK} current and Fig. 6.15c gives the dynamic of carriers in the base region.

The turn-on period can be broken down into three phases. The first one is initiated when the gate voltage reaches the threshold voltage ($V_T = 5$ V). The free wheel diode D imposes the whole electromotive force supplied by the circuit to the device. The drain/source voltage (V_{DS}) applied to the MOS is therefore much higher than the punch-through voltage (V_P) (see Eq. 6.29). The channel current I_{mos} then corresponds to its saturation value (see Eq. 6.26). The increased I_{AK} current is only linked to this current. The bipolar component of the current lags slightly due to the charge time constant of the gate circuit.

The second phase is started when the current reaches the value imposed by the charge inductance L_f. The free-wheeling diode D gets blocked and the voltage across the terminals starts to decrease. This results in the creation of displacement currents. The latter's effect is designed to compensate for MOS through the bipolar component. The gate voltage gets stabilized (see Fig. 6.15b) on the Miller plateau. This is due to the gate current drift in the capacitance C_{GD}.

The last phase is initiated when the drain voltage V_{DS} of the MOS structure becomes less than the channel Punch Through voltage (V_P). The channel then undergoes desaturation and the current I_{mos} is once again determined by voltages V_{DS} and V_{GS}. The quickly-decreasing phase of the anode voltage is then ended. The carrier distribution (Fig. 6.15c) shows that the base is not fully invaded by carriers. As a result the modulation of the base region resistance (R_{base}) has not yet reached the value corresponding to the conduction regime of the IGBT. After a short while of

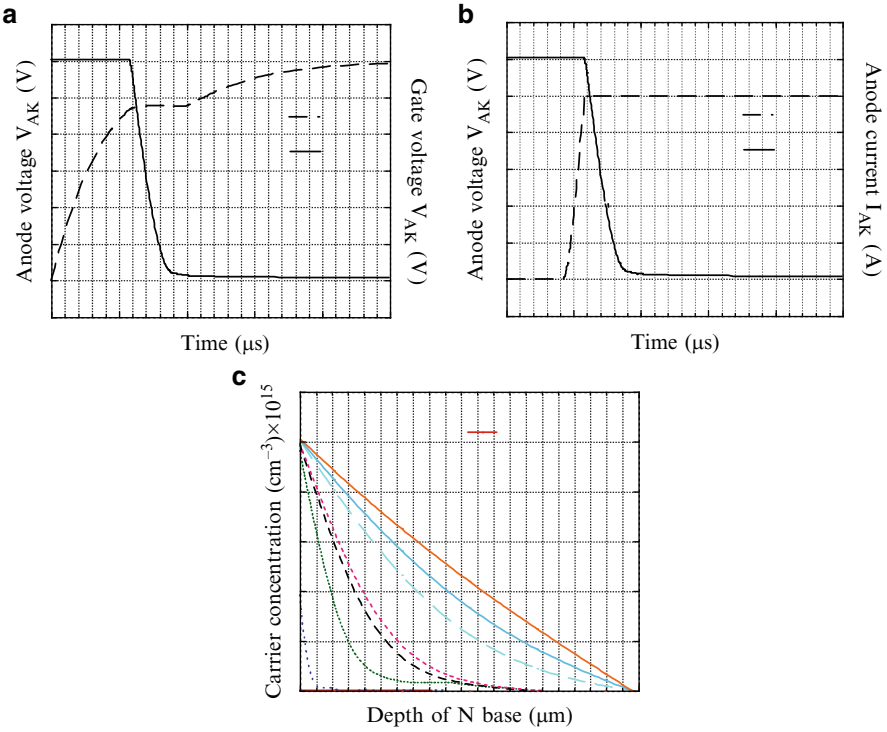

Fig. 6.15 (**a**) Evolution of the gate voltage at turn-on, (**b**) I_{AK} current and V_{AK} voltage evolutions at turn-on, and (**c**) carrier concentration evolution in the base region of a NPT-IGBT

the order of 10 µs, a permanent regime is reached allowing for carriers to be present in the base. Then the voltage reaches its lowest level, corresponding to the on-state voltage drop (V_{on}).

5.2.4 Simulation of the Turn-Off Dynamic

The diagrams of Fig. 6.16 give the simulation results during the turn-off phase. The latter can be broken down into three subphases.

The first one is initiated when the decreasing gate voltage fails to impact the channel current I_{MOS}. On the other hand, it causes an increase in internal drain voltage up to the Punch Through voltage (V_P). At that moment, the channel current is determined by the instantaneous gate voltage only. As in the case of turn-on, the Miller effect occurs. Now, the current resulting from the gate/drain capacitance charge substitutes for the gate/source capacitance discharge. This provides continuity of the current spent by the gate control circuit.

With the onset of the depleted space charge, the second subphase is initiated. It occurs along with the increase in the absolute value of the concentration gradient at

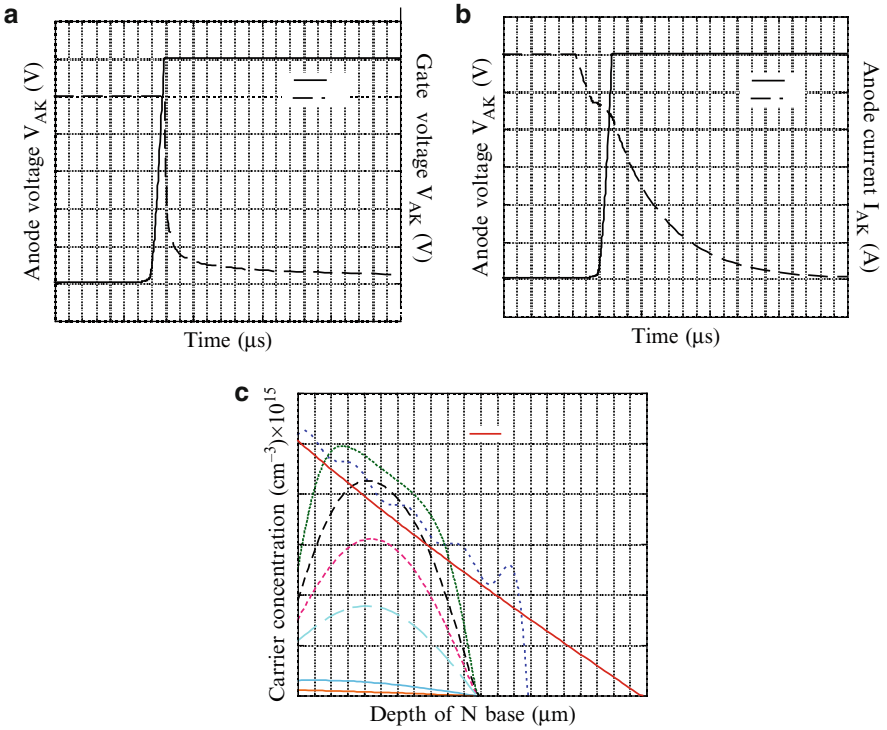

Fig. 6.16 (**a**) Evolution of the gate voltage at turn-off, (**b**) I_{AK} current and V_{AK} voltage evolutions at turn-off, and (**c**) carrier concentration evolution in the base region of a NPT-IGBT

the very right end of the storage zone (Eq. 6.2). Then, an increase in the number of collected hole current takes place. The anode current remains constant. When the gate voltage becomes less than the threshold voltage (V_T), the channel current I_{mos} diminishes and cancels. At that particular moment, only the bipolar current remains.

The conduction of the free wheel diode D occurs while the anode voltage gets fully re-established and marks the beginning of the third subphase. The opening transient is then identical to that of a zero base current bipolar transistor. The initially sharp current decrease is due to the carrier recombination. The final current decrease asymptotically tends towards a value equal to the carrier lifetime. This concludes the IGBT turn-off operation.

6 Examples of Power Electronics Simulation Circuits

The use of physical models for the study of device/circuit interactions is essential in power electronics. This section is designed to show that physical models can be used for the design and analysis of power electronics circuits. Two examples of

study of circuits are presented. The first simulated circuit is regular since it consists of a bridge AC–DC supplied by a resistive inductance. The second circuit deals with the connection in parallel of IGBT's to obtain a low loss macro-device. In this case, the study shall tackle the evolution of energy losses as a function of frequency, the cycle ratio and the surface recombination of the P^+ anode.

6.1 Voltage DC/AC Voltage Inverter [19]

Voltage AC–DC converters are known as "direct current voltage" devices supplied with a direct voltage source. Usually, they are current-reversible. In turn, they can be used to supply under alternating voltage, charges with a current source behaviour. They consist of two switching cells. Figure 6.17 shows the DC/AC converter circuit where the four switches must operate jointly to avoid a short-circuit of the current source and to allow firing of the current source. The current source I is a sine waveform and each switch corresponds to the association of an IGBT with antiparallel free-wheel diode. Voltage source E is direct and exhibits a value of 300 V. Gate resistance values are equal to 20 Ω. The charge used is a variable value inductance and a resistance whose value is set to 2 Ω. The signal across the charge terminals is a function of electric values assigned to it and of the control signals from the different switches. Two values are successively attributed to the charge inductance: 10 mH and 1 μH. Figure 6.18 shows the current flowing in the inductance for these two values. For the former value, the output signal obtained is a square signal. The latter value involves a slower energy storage dynamics leading to a triangular signal.

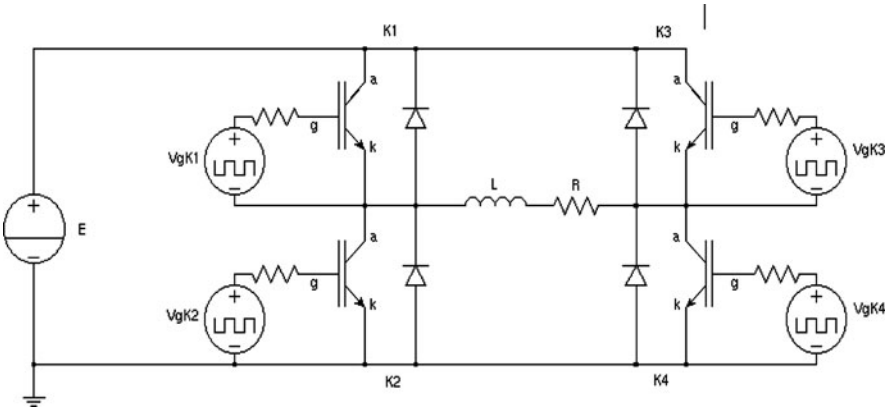

Fig. 6.17 Circuit used for the DC/AC voltage inverter simulations

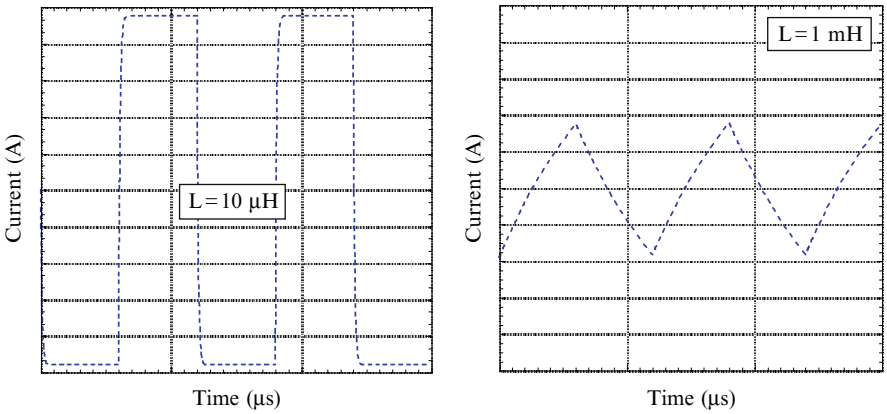

Fig. 6.18 Waveform of the current flowing in the charge for L = 10 mH and L = 1 mH

6.2 Low Losses Structure

IGBT type devices act as a switch in the power electronic circuits. They must exhibit a low voltage drop during on-state (V_{ON}) and low losses during switching phases. This is achieved by modulating the wide base, lowly-doped region conductivity though a bipolar injection. This modulation increases the charges in this region thereby diminishing the on-state resistance. However, this method implemented to decrease V_{ON} causes the onset of a tail current during turn-on which may last for a while according to the quantity of charge to be evacuated. Therefore, it is essential to control the level of charge stored to arrive at a trade-off between on-state voltage drop and current tail duration (causing switching losses).

Given the state of the art (monolithic or hybrid integration), *systems* approaches may be contemplated to improve the trade-off between on-state voltage and switching losses beyond what is currently available. One possible approach lies in associating in parallel a fast IGBT and a slow IGBT (as depicted in Fig. 6.19) [20]. The fast device is intended for switching (short lifetime or low injection of the anode in the base region) and the slow one for the conduction phase (high lifetime or high injection in the base region).

In this configuration, both IGBTs are simultaneously controlled upon turn-on since switching times are almost identical. During this conduction phase, the current is distributed according to the apparent resistivity of each IGBT. On the other hand, during the turn-on phase, the slow IGBT is first controlled. After a certain time corresponding to the current tail duration of the slow structure (about 80 µs in our example), the fast IGBT is controlled during firing. The main benefit of this control cycle is that the IGBT in charge of conduction will switch to the off-state under a low voltage corresponding to the on-state voltage drop of the fast IGBT. Switching losses upon firing are thus minimized.

To highlight the advantages of this association, three series of simulation are carried out. The first uses two slow IGBTs, the second two fast IGBTs and the third

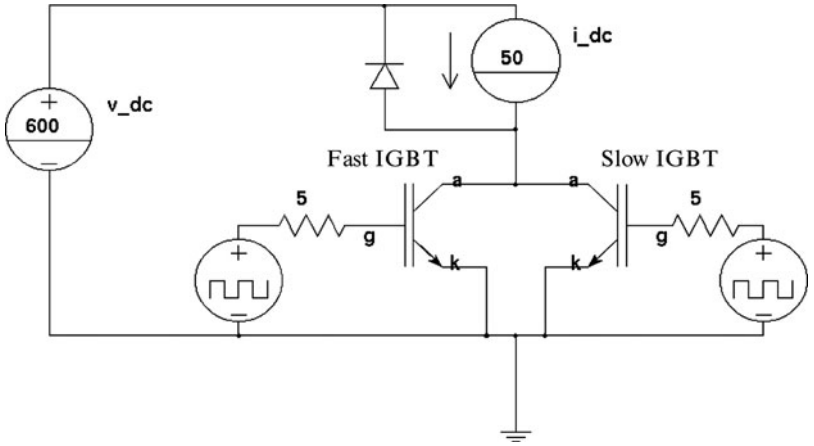

Fig. 6.19 Simulation circuit for the low loss association

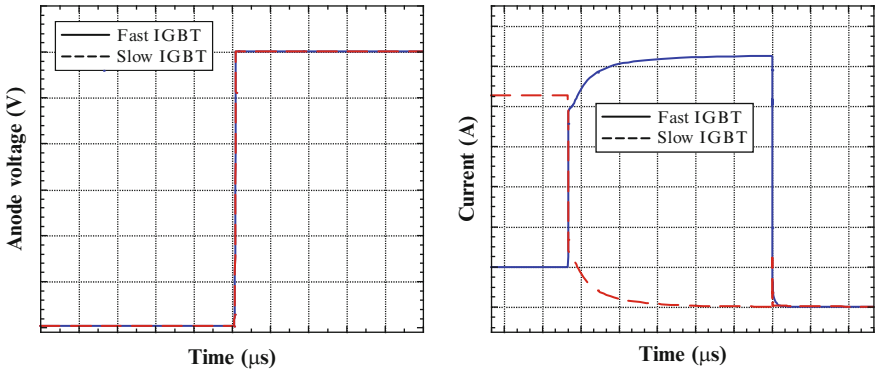

Fig. 6.20 Voltage waveforms and current distribution during the turn-on phase

a slow IGBT (assigned to conduction) associated with a fast device (assigned to switching). Individual losses incurred by these two IGBTs (fast and slow) were previously simulated as a function of the frequency and of the cyclic control ratio. The values obtained are used a posteriori to justify the benefit of the parallel connection. The silicon surface occupied by each IGBT is the same, that is, the parallel association will occupy a space twice the size used by a single IGBT. This is the only constraint imposed by this method.

Figure 6.20 shows an example of current distribution across the terminals of two IGBTs during a turn-on phase. The slow IGBT current transfer toward the fast IGBT is well depicted in this figure. All simulation results are given in Fig. 6.21a–c. The energy loss is computed over a complete switching cycle. Simulations are conducted for three values of the cyclic ratio 1/4, 1/2 and 3/4 and for four different frequency values 2 kHz, 1 kHz, 500 kHz and 100 Hz. The gate control cycle *Vg* is frequency-dependent and the rise-fall times have been set to 20 ns.

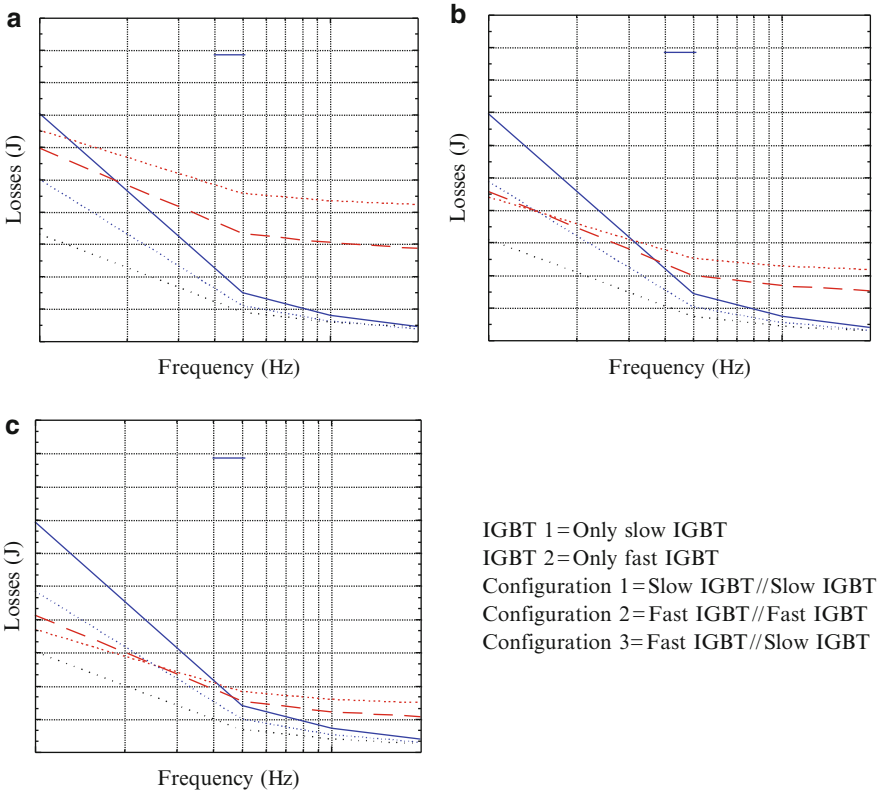

Fig. 6.21 Losses on a switching cycle as a function of f and for different cyclic ratios (**a**) 1/4 (**b**) = 1/2 (**c**) = 3/4

The analysis of the simulation results clearly show that the connection in parallel of two IGBTs (configuration 3) leads to less energy losses over a switching cycle relative to the use of a single IGBT or two identical IGBTs connected in parallel. For given IGBTs, the impact of the working frequency and the cyclic ratio are essentials in respect of the pertinence of such an association.

The maximum working frequency can be determined first by the duration of the slow IGBT current tail duration and by using the cyclic ratio which the application contemplates. Therefore, the gain brought about by the association during the conduction phase must be greater than the losses generated by the switching phase. The duration of the conduction period must be sufficiently long (by including the slow IGBT current tail duration) for the association (slow IGBT-fast IGBT) to be viable.

For this type of setup, one has to consider the conduction duration and not only the working frequency. The optimal conduction duration, associated with the desired cyclic ratio shall determine the maximum frequency. Simulation results show that the maximum working frequency of configuration 3 is set to 2 kHz (slow IGBT tail current duration equal to 60 μs) for a cyclic ratio of 1/2. With respect to lower frequencies, the study shows that the association brings about a gain in terms of energy of about 5–32% for cyclic ratios between 1/4 and 3/4.

7 Conclusion

The development of energy control and conversion systems in power electronics becomes increasingly important in a world where energy resources become a major concern. Thus, to be able to design new, efficient switching functions and to optimize the power systems so as to decrease losses, the use of simulation tools becomes particularly important. Analytical models which account for precise physical phenomena within the highly complex power electronics circuits are part and parcel of this approach.

Modeling bipolar type power devices requires taking into account the distributed nature of the charges present in the wide, lowly-doped base region. The so-called *analog* solution to the ambipolar diffusion equation based on simple RC lines along with controlled sources are the foundations for the modeling presented in this chapter. The other electrical or physical regions rely on much more conventional approaches. Thus, we have described all the simplifications that have been introduced, along with the principle of the method for solving the ambipolar diffusion equation and the modeling of the other regions.

Also the construction of the model in accordance with the NPT type IGBT method has been presented along with the static and dynamic behaviour simulations. To highlight all the benefits that may be derived from this method for power electronic circuits, two examples of application have been given. The first one deals with the DC/AC voltage inverter while the second addresses the low loss architecture issue. The objective of the last example was to associate in parallel the IGBTs whose intrinsic characteristics are used to lower the global losses on a switching cycle.

These models use physical, geometrical and electrical characteristics derived principally from the methods relying on reverse engineering or electrical measures. As in any modeling, the main difficulty is to grasp sufficiently clearly all the parameters that the models need. Therefore, the characterization rules for such devices as well as a parameter extraction methodology will be essential steps in the future.

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Chapter 7
Web-Based Modelling Tools

Andrzej Napieralski, Łukasz Starzak, Bartłomiej Świercz, and Mariusz Zubert

Abstract High prices and hardware requirements considerably limit the access to modern CAD tools and device models while free versions usually have too serious limitations. In order to overcome this problem and to make accurate and modern semiconductor device models widely accessible, a web-based circuit simulation environment has been developed and made available to Internet users. The DMCS-SPICE web site gives access to a SPICE-based simulation engine where a new distributed model of the PIN power diode has been implemented. It is a first step towards a widely accessible simulation environment with high power semiconductor device support, providing the user with reliable simulation results for a complete circuit in a reasonable time. Additional features make the environment well suited for electronics education. Two approaches to web applications are presented and discussed. It is argued that the rich client technology, on which Genersi – the new version of DMCS-SPICE – is based, is much more advantageous. It enables development of generic simulation environments providing portability, support for multiple simulation engines, and a user-friendly advanced graphical user interface.

Keywords Genersi · DMCS-SPICE · SPICE · CAD · WEB-Simulator · PIN diode

1 Introduction to Web-Based Simulation Tools

The dynamic development of microelectronics and power electronics results in more complex semiconductor device structures and makes it necessary to use modern simulation software for circuit design. However, high prices and hardware requirements limit the access to professional CAD tools by some educational institutions, students, or small enterprises. Free versions of commercial software are unable to solve this problem because of their limited functionality and lack of well implemented numerical algorithms and device models. This issue will be addressed in Section 3.

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This is especially true when power electronics is concerned because – as has been shown in Chapter 5 – it requires advanced device models to obtain reliable simulation results. Such models are not available with free simulation environments.

The increasing popularity of the Internet can help to solve this problem. Wilamowski, Malinowski, and Regnier [1] were probably the first to see the possibility of performing circuit simulations over the Internet by means of dedicated web applications. Simulation software may run on remote servers and results may be sent to the user in the form of numeric data or graphics. With the constant increase of network bandwidths, time needed to receive data becomes less important.

However, Wilamowski [2] has put special emphasis on pay-per-use access to simulation software and platform-independent user interface provided by a web page. In this paper it is proposed to take advantage of free simulation software to develop a free simulation environment with new numerical algorithms implemented and modern device models included.

There are two main approaches to development of web-based distributed applications. The thin client technology is the most common. In this case all the operations performed on data are realised on the server side and the client is only responsible for providing a user interface. The thin client approach has been used in a first version of the DMCS-SPICE portal that will be described in Section 2.

The other approach is called the rich client technology. The main feature of rich client applications is the ability to process data stored on the server. This technology has been used to develop Genersi – the new version of DMCS-SPICE portal, which will be described in Section 4.

2 Thin-Client DMCS-SPICE Portal

The DMCS-SPICE portal [3, 4] has been developed to give Internet users access to modern electronic device models and circuit simulation tools. According to the chosen thin client approach, the simulation software runs on a network server and the user interface is ensured by means of a web page providing data entry point and result presentation.

It should be thoroughly considered what operations to perform on the client side and on the server side [1]. Current server performances and network bandwidths enable to perform all operations on the server side. The user receives simulation results in the form he requests and all he needs to use the developed simulation environment is a web browser. This makes the proposed solution maximally portable and platform-independent, which can ease the cooperation between different users. However, in some situations it may be more suitable to do some data processing on the client side. This issue will be addressed in more detail in Section 4.

The developed simulation environment comprises four main modules as illustrated in Fig. 7.1. Computational resources are provided through the Apache server running under Linux operating system. Nevertheless, the code is portable to Windows and Unix operating systems. Circuit analysis is performed with a

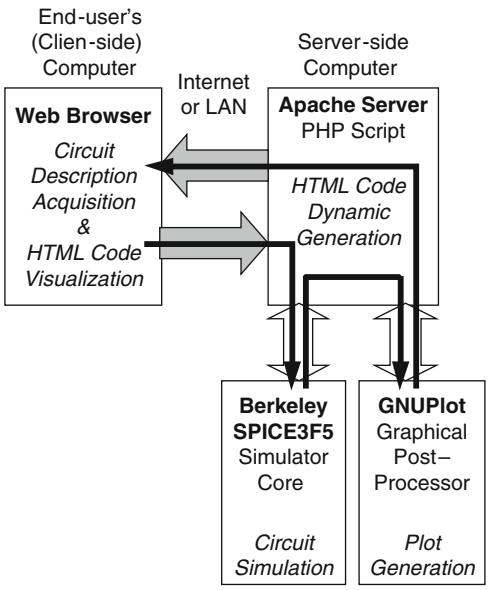

Fig. 7.1 Structure of the developed simulation environment and data flow [3]

batch-executed simulator (SPICE3F5). Simulation results are processed with GNUPlot [5], providing graphical data representation. Finally, graphical user interface functions (circuit description and simulation parameters entry point as well as results visualization) have been implemented in PHP code that dynamically generates HTML pages rendered by the user's web browser (see Figs. 7.2 and 7.3).

Thanks to the proposed solution, simulation and data processing can be performed on dedicated servers, thus not engaging the end-users' computers. Another advantage is that no additional software has to be installed on the end-user side. In order to ensure free access to the environment, it has been based on open source and GNU-licensed software.

It was decided that the circuit simulation core should be based on SPICE because of high popularity and strong position of SPICE-like simulators. This choice ensures wide accessibility and easy usage of the environment, as an average electronic engineer or student has at least basic knowledge of SPICE circuit description format.

When it comes to the selection of a specific simulator, Berkeley SPICE3F5 [6] has been chosen for two reasons:

- Open licensing, which enabled the developed environment to be publicly and freely accessible
- Open sourcing, which gave the possibility of customizing the core to meet the project demands

An important idea behind the portal was to make modern power device models available. This also includes model testing and parameter adjustment to fit characteristics

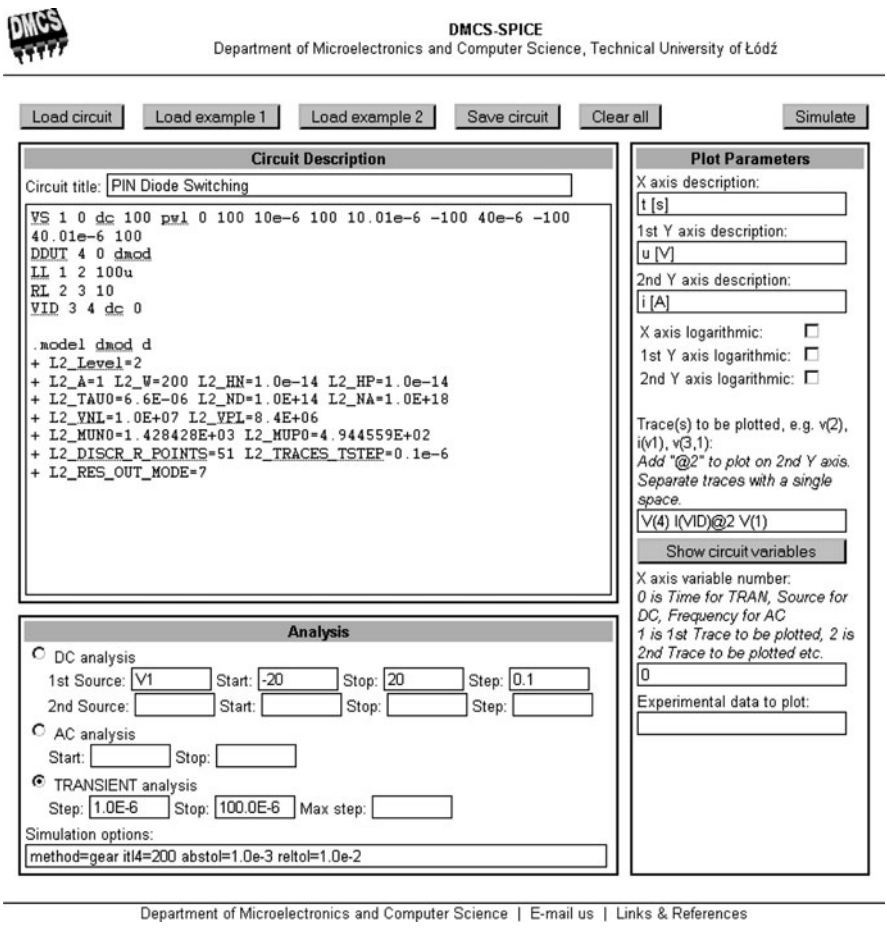

Fig. 7.2 Entry point page for circuit description and simulation options

and waveforms of a specific device. For this purpose, it is possible to upload measurement data in a text file and plot them together with simulation results as shown in Fig. 7.4.

3 Integration of Novel Power Device Models with SPICE3 Engine

CAD programs developed for microelectronics, such as many SPICE-based simulators, have been successfully applied to circuit analysis. However, for power electronic engineers they have some significant drawbacks.

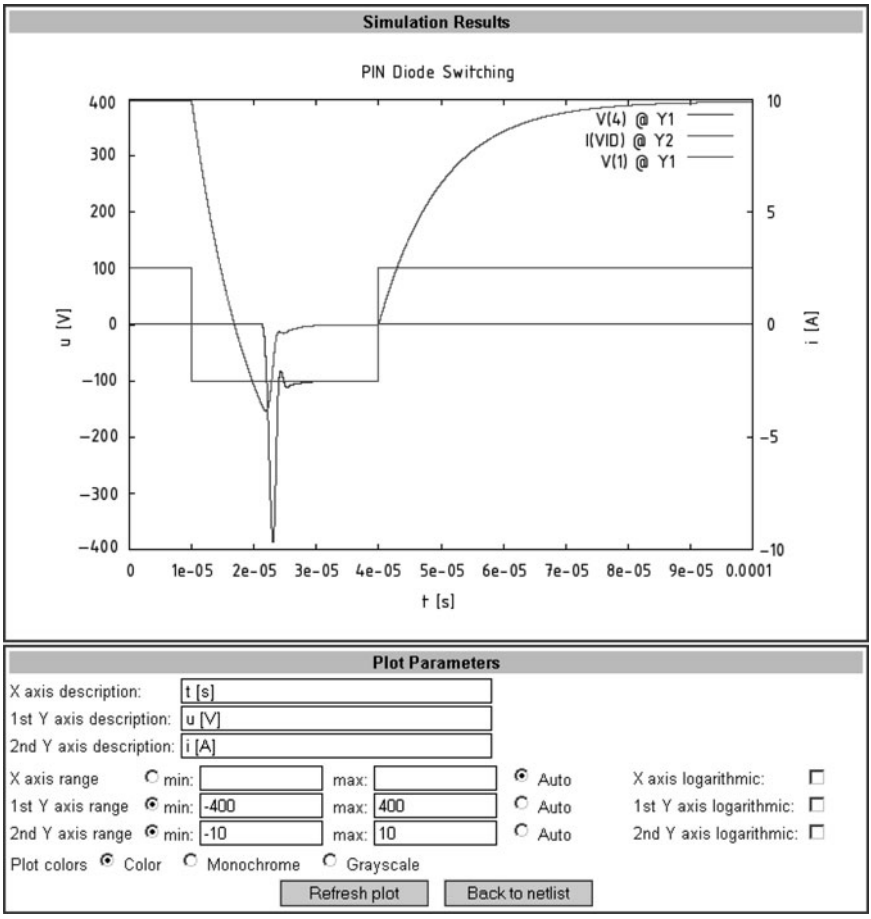

Fig. 7.3 Simulation results graphical presentation page

For instance, simulation of systems with multiple stages, feedback loops, several levels of complexity involving different time constants etc. is very troublesome. This has partially led to opting for other simulation environments such as The MathWorks' Matlab/Simulink or Mentor's SystemVision for system-level simulation.

On the other hand, device-level simulation capability of standard CAD software is also insufficient because of the lack of reliable power semiconductor device and passive element models.

It has been shown in Chapter 5 that distributed models of power semiconductor devices should be used if realistic simulation results are needed. Such models, however, were until now available only in specialized simulators [7] most of all multidimensional ones, that were hard to use for an average engineer and needed large computational resources. Moreover, 3-D or 2-D simulations take an important amount of time and it is difficult to analyze devices together with their external circuits.

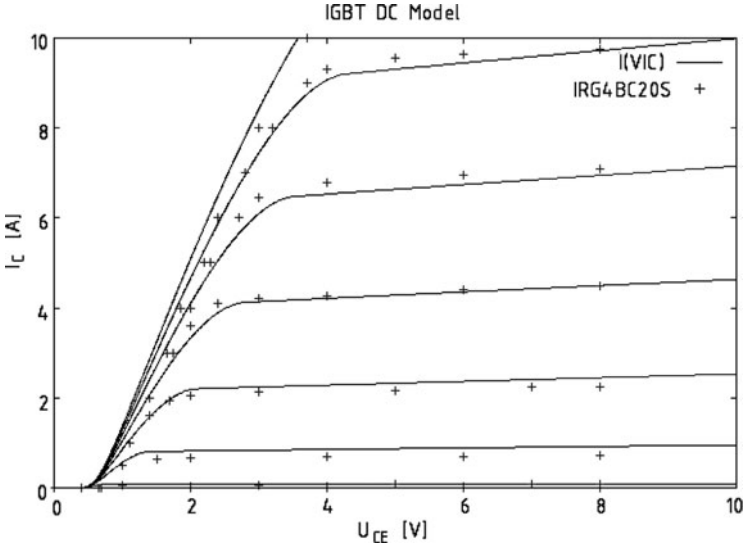

Fig. 7.4 Device modelling with DMCS-SPICE – simulated IGBT characteristics (*lines*) together with measurement data (*crosses*)

In order to solve these problems, it has been proposed to integrate power device models of a new type with a standard circuit simulator. As already demonstrated in Chapter 5, such models combine good accuracy and short simulation times. Together with the usage simplicity of standard CAD software, this can yield new possibilities of power electronic circuit simulation.

In order to prove this feasible, a new model of the PIN power diode [8] described in Chapter 5 has been implemented in the DMCS-SPICE portal presented in Section 2 [9]. Thanks to SPICE3F5 being an open source simulator, it has been possible to insert the new model into the simulation core. An additional code has been added to the one describing the standard diode in SPICE. A new model parameter – called LEVEL by analogy to MOSFET models – enables the choice between the standard lumped model (LEVEL = 1) and the new PIN diode distributed model (LEVEL = 2).

As described in Chapter 5, in the developed model, the voltage across the diode v is calculated as a sum of voltage drops in the particular diode regions:

$$v = v_{jp} + v_{sc} + v_s + v_d + v_{jn} \tag{7.1}$$

where (see Fig. 5.12) v_{jp} corresponds to the P^+N^- junction, v_{sc} corresponds to the space charge region, v_s corresponds to the charge storage region, v_d corresponds to the drift region, and v_{jn} corresponds to the N^-N^+ junction.

Each of the above voltage drops depends on the diode current i. This especially concerns the voltage drop across the charge storage region where the charge

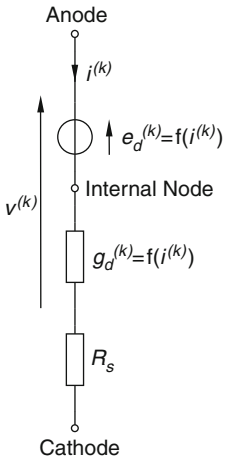

Fig. 7.5 Distributed model of the PIN diode implemented in the developed simulator

carrier concentration is strongly dependent on the current. The current dependence is included in boundary conditions (concentration gradients at both ends of the storage region) that complement Eq. 5.10.

Therefore, the model has been implemented in the form of a voltage source e_d with a series non-linear conductance g_d as shown in Fig. 7.5. It is also possible to specify a constant series resistance R_s as an additional model parameter.

The value of g_d results from numerical linearisation of the model. The original linearisation algorithms implemented in SPICE3F5 are unable to assure numerical convergence during simulation of circuits containing such highly nonlinear elements as the developed diode model. Thus, a better-suited algorithm has been proposed and included in the developed software.

In the new linearisation algorithm g_d in each k-th iteration is calculated based on two points from the closest neighborhood of the present operating point, as demonstrated in Fig. 7.6:

$$g_d^{(k)} = \frac{2\delta i}{v^{(k)}(i^{(k)} + \delta i) - v^{(k)}(i^{(k)} - \delta i)} \tag{7.2}$$

where $v^{(k)}(i)$ is the voltage calculated in the k-th iteration for a given current value i according to Eq. 7.1 and δi is given by

$$\delta i = \min\left(\frac{\left|i^{(k)} - i^{(k-1)}\right|}{4}, \frac{\left|i^{(k)}\right|}{10}\right) \tag{7.3}$$

The voltage source voltage is then calculated according to

$$e_d^{(k)} = v^{(k)}(i^{(k)}) - \frac{i^{(k)}}{g_d^{(k)}} \tag{7.4}$$

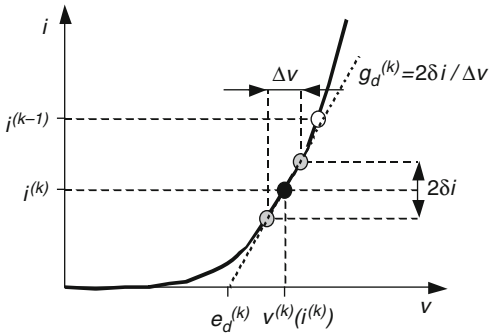

Fig. 7.6 New linearisation algorithm for the distributed PIN diode model (the quasi-static characteristic is shown for easier understanding)

The new algorithm has permitted to decrease the number of v calculations per time point, especially in transitory states. If numerical problems occur or g_d is too close to zero, the simulator tries to find a solution with a simplified algorithm where:

$$g_d^{(k)} = \frac{i^{(k)} - i^{(k-1)}}{v^{(k)}(i^{(k)}) - v^{(k)}(i^{(k-1)})} \tag{7.5}$$

$$e_d^{(k)} = v^{(k-1)}(i^{(k-1)}) - \frac{i^{(k-1)}}{g_d^{(k)}} \tag{7.6}$$

The DMCS-SPICE portal with an accurate, distributed power diode model implemented constitutes an important step towards a simulation environment providing reliable results for power semiconductor devices. Additionally, thanks to simulation times being much shorter than in the case of multidimensional simulation software, it enables realistic simulation of power electronic systems at least at stage or circuit level. As stated earlier, this could not be achieved (with both reasonable speed and accuracy) with multidimensional simulators because of the high computational complexity, nor with standard circuit and system simulators because of the lack of appropriate device models.

Based on the distributed PIN diode model it may be demonstrated that the presented approach to circuit simulator development has its advantages for education, too.

Operation of power semiconductor devices is hard to understand for many students because of many complex physical phenomena occurring simultaneously. A ‘static’ lecture is often insufficient to develop a profound understanding of these issues.

In order to help in solving this problem, the above described model has been enhanced by adding the possibility of creating extra output data comprising charge carrier concentration and voltage potential distributions. Then a module has been added to the DMCS-SPICE portal enabling graphical presentation of these data for a chosen time point [9].

Through tracking the evolution of both distributions jointly with waveforms of external electrical quantities (current, voltage, and dissipated power) students get an

insight into device operation and develop understanding of relationships that connect microscale and macroscale phenomena.

In Fig. 7.7 exemplary results of PIN diode switching simulation are shown for four consecutive instants at different stages of the switching process. Students start with the low voltage drop at full conduction (a), negative voltage is appearing together with the space charge after charge carriers are swept off from this region during diode turn-off (b), peak negative voltage drop and space charge extension are attained (c), and during turn-on, a high positive voltage drop is observed due to the still low excess carrier concentration (d).

In the Power Semiconductor Devices laboratory at the Technical University of Lodz, the DMCS-SPICE portal has been used for several years now [10, 11]. It proved useful both for introducing students to bipolar power semiconductor device issues and for investigating their operation in a more detailed way.

4 New DMCS-SPICE Portal Based on JAVA Web Start Technology

A rich client (also known as fat client) runs as a standalone application. As for Java Enterprise Edition [12] (J2EE) solutions, rich clients are normally written in Java but it is not an absolute requirement. A rich client application [13] provides user with two key benefits: high speed (responsiveness) and standard application look-and-feel. Such an application is fast because it keeps all the presentational code on the client side and only connects to the server to request data.

The two main drawbacks of rich clients are: the problem with centralised configuration and keeping all clients up-to-date, and the requirement of Java Virtual Machine (JVM) being installed on all the client machines (for Java-based rich clients but other frameworks also require their own interpreters or libraries). Especially the second disadvantage makes Java rich clients unpopular because most of standard machines do not have Java installed by default or the installed version is incompatible with the application's requirements. The second issue can be solved using Java Network Launching Protocol [14] (JNLP) that is able to upgrade JVM automatically to the required version.

On the contrary, thin clients run completely in a web browser. They use a mixture of HTML code and JavaScript for simple client-side processing. All the real processing is done on the server side, and it is on the server side that all the contents of the application view are generated. Web browsers are ubiquitous what makes thin client a 'zero configuration solution' as far as the client side is concerned. Because all the client code is generated on the fly on the server side, thin client applications are simple to configure and update in one, central place. Those two features paved the way to success for thin clients in enterprise applications.

Thin clients are not free of problems, though. The first one is responsiveness and speed. A thin client application downloads both data and presentational code from the server at each request and repaints the whole page. Usually the presentational

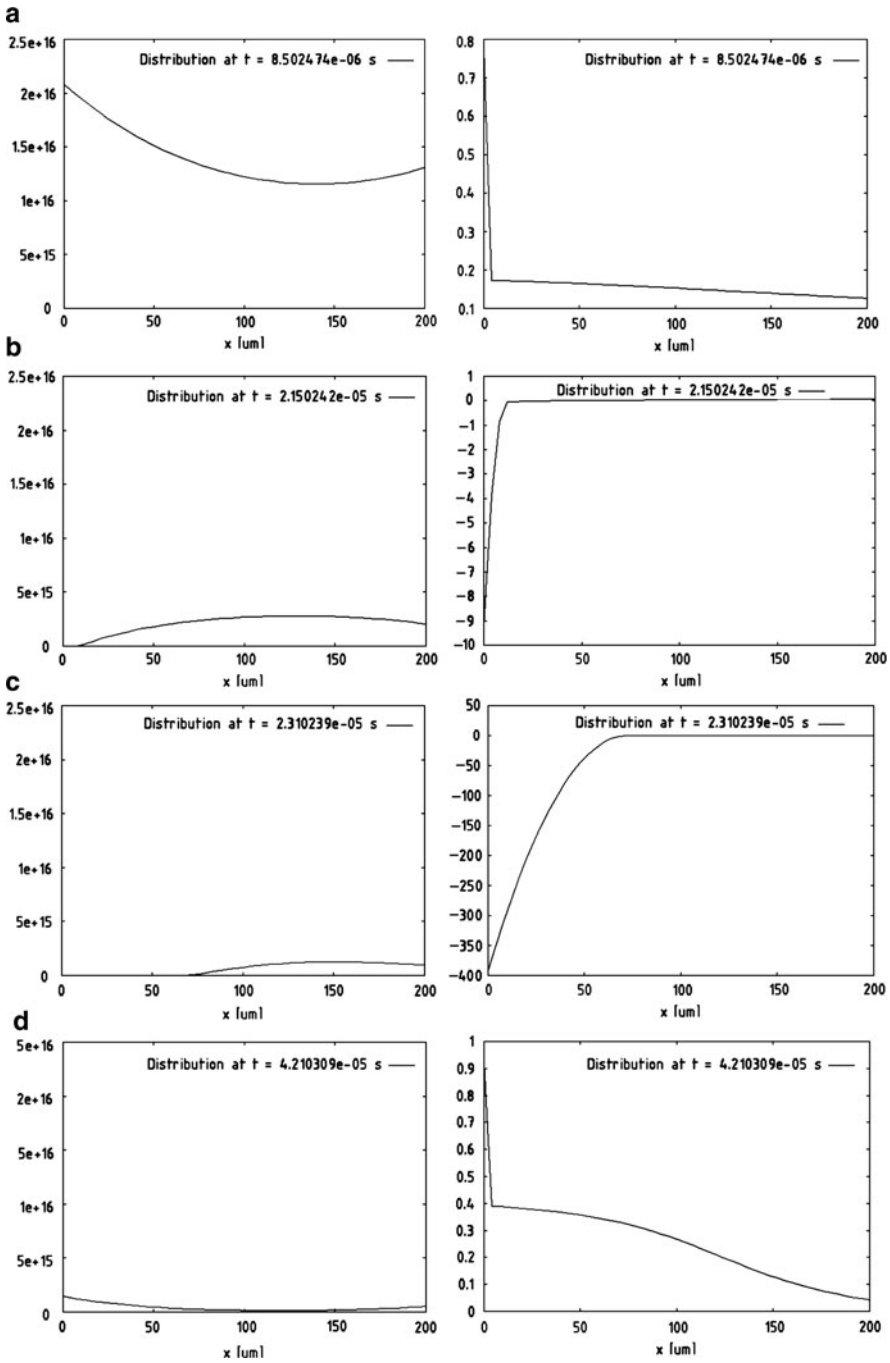

Fig. 7.7 Education support with DMCS-SPICE – investigating PIN power diode operation in transitory states: carrier concentration distribution (*left*) and voltage potential distribution (*right*) along the large base (detailed description provided in the text)

code uses more than half of the bandwidth and it is repeated in all the consecutive requests. This makes thin clients slow and often gives the impression of the application freezing. HTML pages are also very limited in presentation of forms, validating input data, and user interaction (lack of context menus or drag-and-drop). What is worse, the implementation of HTML standards differs between browsers, and is especially poor in the case of the most popular browser, Internet Explorer 6. As a result, designing a really cross-platform thin client GUI requires much more time and knowledge than it should in theory.

Unfortunately, there is no ideal solution for the client application platform. What we would need is a common, widespread platform, preinstalled on all, or most of, machines, with automatic update and configuration features, and capable of displaying the GUI with all the user-interaction features characteristic for desktop applications. But there is no such a platform. There are, however, some solutions going in this direction.

The most popular and well known one is Ajax (Asynchronous JavaScript and XML) [15] Ajax, in principle, resembles rich clients in the way it handles server data retrieval. Ajax applications can reduce the amount of downloaded presentational code to the minimum by requesting pure data contents from the server. They do not use page refreshing, instead they replace only part of the GUI with new data, much as rich clients do. Ajax applications also often use advanced HTML/JavaScript libraries for rendering dynamic and interactive components, imitating such features as drag-and-drop and context menus thus further improving user perception. Successful Ajax examples, like Google Maps of GMail, show that Ajax is an approach that is always worth considering. The price to pay is often high complexity of the application source code.

Another solution is Flash/Flex [16]. Flash was designed from beginning as presentational layer for dynamic, application-like content. Flex is a way to develop Flash applications by programming. It includes a declarative XML language called MXML for laying out user interfaces and a programming language called ActionScript. Flex applications compile directly into Flash binaries (SWFs).

Java-based rich application clients are not very popular but they are still used and their market share can even grow thanks to improvements in user interface rendering in newer JVM. Java-based rich clients can use JNLP implementations like Java Web Start for solving the problem of centralised updates and configuration. This is the way in which NetBeans platform [12] clients can be used. Still, the main restriction for Java rich clients is the lack of JVM on most machines. However, due to the recent open-sourcing of Java, the number of machines with preinstalled JVM should grow in the nearest future.

Based on the above considerations and after determining the drawbacks of the thin-client DMCS-SPICE portal, a generic simulation tool project called Genersi (GENERic SImulator) has been started [17].

The Genersi project is aimed at creating a common, modular framework for deploying simulation engines and developing their clients. Engines and client plug-ins should be deployed and managed (and possibly distributed) centrally and the control over access to restricted resources (plug-in administration, scripts database) is also

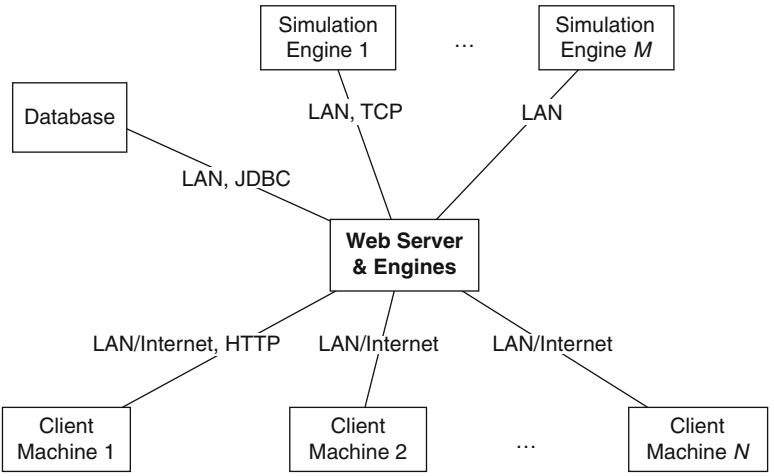

Fig. 7.8 Block scheme of Genersi

required. At the same time, some of the requirements for client functionality (such as displaying interactive graphs) suggested using the client-server architecture with rich clients as an application front-end.

Java EE 5 has been chosen as the answer to those needs, and the NetBeans platform as the base for the client application. The simplified block diagram of Genersi is shown in Fig. 7.8.

Simulation engines are accessible via central Java EE server that maintains the registry of all installed engines together with all information necessary to use them or uninstall them. Clients can use any of the available engines for simulation.

Clients communicate with the server through the simulation web service. This allows using the client even behind a firewall. The server also exposes a second service for storing user simulation scripts and data in the central database. The client application is based on the NetBeans platform framework, which makes it inherently modular. A dedicated server-side, web-based application is also provided for plug-ins management such as listing, installing and uninstalling. The designed solution contains the Genersi framework implementation and one simulation engine (SPICE3F5) with its client application plug-in for performing circuit simulations.

Genersi has been derived from the thin-client DMCS-SPICE portal. The main idea behind Genersi was to eliminate the disadvantages of the thin-client solution:

- Limited functionality (only SPICE3F5 engine allowed)
- Only a simple plot image as presentation of simulation results
- Tight coupling – difficult to change or extend
- Lack of session support and no user data persistence (users cannot store scripts or results on the server for future usage)

The goal of the project has therefore been to create a universal, extendable tool for performing engineering simulations using the client-server architecture, having the following features:

- Support for many simulation engines
- Script files edition and management
- Ability to create, modify and delete script files in different formats
- Remote simulation as in the thin-client DMCS-SPICE portal
- Simulation result presentation using an interactive chart (ability to zoom in/out selected sections of the graph, change the graph options, and export it to a file etc.)
- Database for storage of scripts, simulation results and user information
- Automated check for new versions, download and installation of updates
- Portability of the client application between different platforms and operating systems

In the simplest case Genersi is installed only on one server machine, containing the application server (project home page, access to client applications, plug-in manager, web services), simulation engines, and the database. Separate machines for the engines and the database are optional. They are not used in SPICE engine default implementation but may be used for other engines and configurations.

On the server side Genersi uses Sun Java System Application Server Platform Edition 9 (GlassFish V1) but it is not tightly coupled to this particular implementation. It may use any application server that supports Servlet 2.5, JAX-WS 2.0 and JPA 1.0 APIs, and that handles JNLP files properly (sets the proper MIME header). The servlet container is the only public access point that must be visible for all the clients so it should listen on a commonly accessible port such as the default port 80 for WWW. The other two services, i.e. the database and the simulation one, are exposed as web services.

SPICE engine client plug-in (see Fig. 7.9) is a NetBeans platform module that assures support for SPICE script files recognition and edition, circuit simulation and presentation of simulation results. It is installed by default but it is an optional module and can be uninstalled using the Plug-in Administrator tool. It also requires that the SPICE engine library be installed on the server.

The SPICE editor is registered as the default editor for SPICE scripts. The editor allows parsing scripts and dividing them into four parts: circuit description, traces to be plotted, plot (axis) description, and simulation type and parameters. The editor is capable of parsing the circuit description on-the-fly and automatically finding the set of traces that can be plotted; the user can simply select them from a list (see Figs. 7.9 and 7.10). The user can also manually create own traces (e.g. a difference or a sum of basic traces).

The client application with the appropriate plug-in enable running the simulation by means of a script that is generated based on data inputed by the user into the editor. The client connects to the SPICE engine service, passes the data received in response and converts them to PlotML format understood by the Client Base module that is responsible for plotting the results.

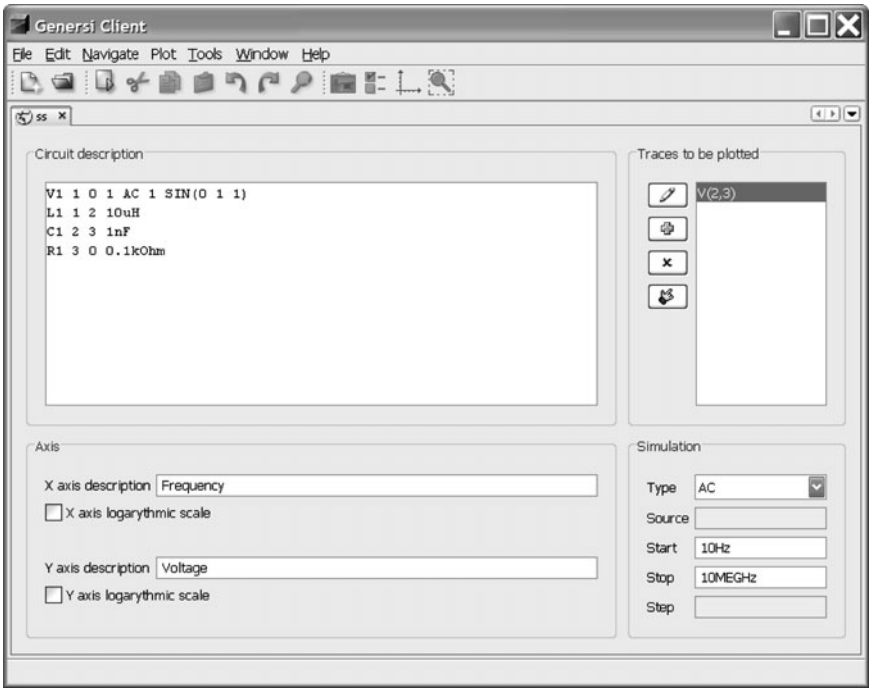

Fig. 7.9 SPICE script editor in the Genersi client application

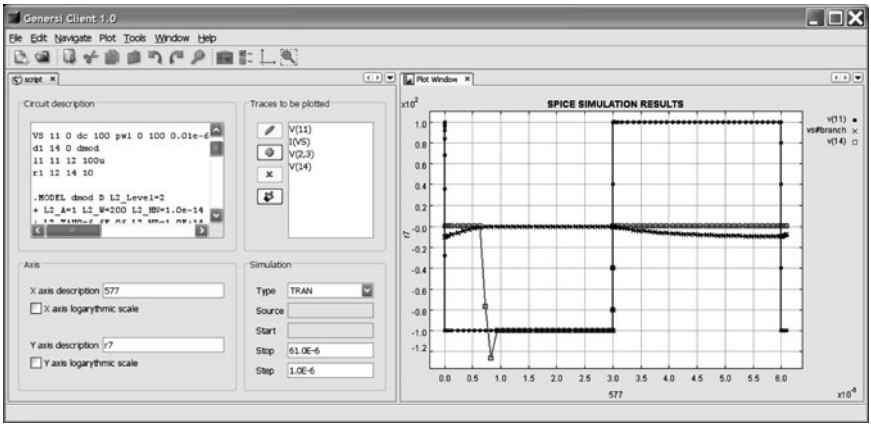

Fig. 7.10 Genersi client's graphical user interface split between the SPICE editor and the plot window

User interface comparison shows that the JNLP version based on the NetBeans platform looks in a more natural way (a standard menu, toolbars) than the HTML (thin-client) version. It also provides much more functionality. For instance, the

user can split the main window between several internal windows to see the editor and the plot concurrently, as shown in Fig. 7.10. Windows can also be moved and minimized separately. In the thin-client portal, the plot was simply an image so no user interaction was possible. In the Genersi rich client, the user can zoom in and zoom out the graphic, change the plot settings (e.g. assign different symbols to different traces, which is very useful for printing plots on a monochrome printer), and export the plot to a file.

5 Conclusion

The DMCS-SPICE simulation environment presented in this paper gives the access to semiconductor device and electronic circuit simulation software by means of the Internet or Local Area Network. The package has three features that can make the project successful: it is free, it is widely accessible, and it is based on the well-known SPICE core. It is worth noting that the Internet is not only a data transmission medium but also an environment for sharing, spreading, and improving modern device models and simulation tools thanks to international cooperation of users.

Thanks to its being based on free code and the client-server architecture, the presented framework is well suited for education including distance learning.

A modern PIN power diode model has been implemented in the simulation core of DMCS-SPICE. It is visible to the user as another level of the built-in diode model. Thus, its usage is straightforward to an average engineer familiar with any SPICE-based popular simulator, which is the opposite of other distributed – and usually multidimensional – models.

The implemented model yields both accurate description of power PIN diode and relatively short simulation times, thanks to its distributed nature on the one hand and the modular approach with one-dimension approximation on the other. This enables reliable simulation of power electronic circuits at a higher level than that of a single device in a reasonable time. Additionally, the Internet is an excellent medium to promote and test this new modelling approach.

The PIN diode example shows that the adopted approach has additional advantages for education. By means of supplementary model features and web portal modules, power electronics can be taught in a more illustrative and thus efficient way.

The recent version of DMCS-SPICE portal, Genersi, is a next step towards a flexible simulation environment. While retaining the portability of the previous thin-client approach, it yields the possibility of using different simulation engines, user and session management, centralised configuration and updates. Moreover, the rich client technology together with the NetBeans platform enabled the client application to be much more user-friendly. The modular client structure makes it possible to develop specific user interfaces for different simulator engines and facilitates future enhancements of the GUI.

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