Pulsewidth Modulated DC-to-DC Power Conversion

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Pulsewidth Modulated DC-to-DC Power Conversion

Circuits, Dynamics, and Control Designs

Byungcho Choi

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To my family –
Meeleeyah, Jieyeon, Ann,
Yeonsoo, and Sunghyuk

PREFACE

The area of power electronics encompasses all engineering and scientific fields that deal with the conversion of electrical power. Each of these power electronics fields has its own theoretical frameworks, underlying principles, analytical methodologies, and engineering disciplines. Accordingly, each power electronics field requires specific knowledge, skill, and expertise dedicated to that field, as well as a solid background in electrical engineering in general. It is the purpose of this book to provide such requirements for students, researchers, and engineers working on one specific field of power electronics — the pulsewidth modulated (PWM) dc-to-dc power conversion.

This book is primarily intended to be a textbook for undergraduate students who are beginning to study power electronics focusing on the PWM dc-to-dc power conversion. This book supplements existing textbooks with more dedicated treatments on the PWM dc-to-dc power conversion. This book is also written as a reference book for postgraduate students and engineers working in the area of modeling, analysis, and control of PWM dc-to-dc converters.

This book is divided into three parts based on technical contents and targeted readers. The first four chapters cover the static characteristics of PWM dc-to-dc converters, concentrating on the steady-state time-domain operation. This part is mainly for undergraduate students exposed to power electronics for the first time. Experienced engineers or postgraduate students may quickly review or skip some sections in this part.

The next five chapters constitute the second part of this book. This part treats the dynamic characteristics of PWM dc-to-dc converters. The second part covers the modeling, dynamic analysis, and control design of PWM dc-to-dc converters. While most of the materials are adequate for junior or senior students with a reasonable academic background, some advanced topics can be omitted for inexperienced undergraduate students. This part can be a reference for engineers working on the modeling and control of PWM dc-to-dc converters.

The last two chapters are devoted to one very important topic of PWM dc-to-dc converters — current mode control. This part presents the functional basics, dynamic modeling and analysis, compensation design, and applications of current mode control. One chapter fully investigates the sampling effects of current mode control. This last part of the book is aimed towards experienced engineers and postgraduate students. Engineers may acquire in-depth knowledge about current mode control. For postgraduate students, this part could serve as a foundation to start out their research on relevant topics.

This book is suited for a textbook for one-semester power electronics classes for undergraduate or postgraduate students. A typical syllabus for an undergraduate class and postgraduate class will consist of as the following.

Undergraduate Class

Chapter 1: PWM Dc-to-Dc Power Conversion
Chapter 2: Power Stage Components
Chapter 3: Buck Converter
Chapter 4: Dc-to-Dc Power Converter Circuits
Chapter 5: Modeling PWM Dc-to-Dc Converters
Chapter 6: Power Stage Transfer Functions
Chapter 8: Closed-Loop Performance and Feedback Compensation

Postgraduate Class

Chapter 3: Buck Converter
Chapter 5: Modeling PWM Dc-to-Dc Converters
Chapter 7: Dynamic Performance of PWM Dc-to-Dc Converters
Chapter 8: Closed-Loop Performance and Feedback Compensation
Chapter 9: Practical Considerations in Modeling, Analysis, and Design of PWM Converters
Chapter 10: Current Mode Control – Functional Basics and Classical Analysis
Chapter 11: Current Mode Control – Sampling Effects and New Control Design Procedures

In writing this book, special efforts have been made in the following two aspects.

1) Computer simulations are used as much as possible, as an instrumental tool to demonstrate the validity of the theoretical developments and accuracy of analytical predictions.

2) Technical contents are presented in a format directly adaptable to practical applications. Converter design examples are given with all engineering details so that each design can immediately be transformed into working hardware.

The following materials are prepared to assist students and lecturers who will study and teach the PWM dc-to-dc power conversion using this book.

End-of-Chapter Problems: Each chapter contains a number of problems to reinforce the technical contents of the text. The problems are rated differently based on the their importance and significance, not necessarily on the degree of difficulty. The problems with one asterisk '*' are important problems, while the problems with two asterisks '**' are more important and essential problems. Solutions to the End-of-Chapter Problems are available from the publisher.

On-Line Teaching and Learning Aids: Power Point® files for lecture slides are available at **http://booksupport.wiley.com.** PSpice® codes used for illustrative simulations are also accessible at the same site.

The author is deeply indebted to many individuals who helped to improve the technical contents of this book. In particular, the chapters on current mode control are strongly influenced from the author's learning and research experiences at Virginia Polytechnic Institute and State University, Blacksburg, VA. The author expresses special gratitude to the persons associated with the preceding works that were used as valuable references in writing this book. A list of those references is shown at the end of each chapter.

The author's warmest appreciation goes to Jieyeon, the author's eldest daughter, for being successfully enticed to become a competent power electronics engineer, as well as providing numerous technical and editorial help in finalizing this book.

This book evolved from the class materials taught by the author over the last 10 years at the Kyungpook National University (KNU) in Daegu, Korea. The author expresses affection and thanks to the former and current students at KNU who inspired the author to undertake the task of writing this book. Some materials in this book were presented by the author in short courses at several power electronics industries. The author is also grateful for the engineers who participated in the short courses and provided valuable feedback.

BYUNGCHO CHOI

Daegu, Korea
April 2013

CONTENTS IN BRIEF

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PART I

CIRCUITS FOR DC-TO-DC POWER CONVERSION

Pulsewidth Modulated Dc-to-Dc Power Conversion. By Byungcho Choi

CHAPTER 1

PWM DC-TO-DC POWER CONVERSION

The dc-to-dc power conversion is broadly referred to as the process of generating a desired dc voltage using a dc source whose voltage level is different from the desired value: namely, changing the voltage level of a dc source into another value. The dc-to-dc conversion is performed in many different ways, each with a distinctive circuit technique. The most popular scheme among them is the dc-to-dc conversion circuit employing the pulsewidth modulation (PWM) technique. The dc-to-dc power conversion based on the PWM technique is called the PWM dc-to-dc power conversion.

This book deals with broad aspects of the PWM dc-to-dc power conversion, covering both academic and engineering perspectives. This introductory chapter presents an overview of the PWM dc-to-dc power conversion. The current chapter discusses basic principles and unique natures of dc-to-dc power conversion circuits, along with the concept of the PWM technique. This chapter also presents the features and issues of PWM dc-to-dc power conversion systems employed to modern electronic equipment and systems. Finally, this chapter outlines the contents of the forthcoming chapters.

Pulsewidth Modulated Dc-to-Dc Power Conversion. By Byungcho Choi

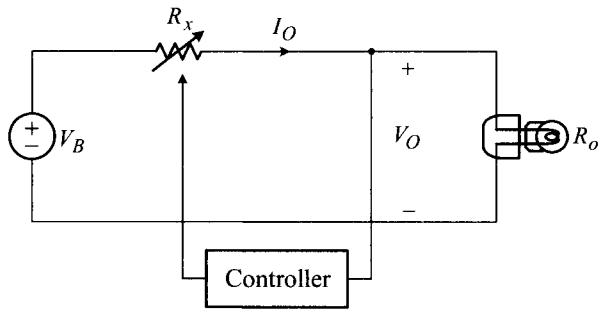

Figure 1.1 Conventional approach to lighting electric bulb.

1.1 PWM DC-TO-DC POWER CONVERSION

The PWM dc-to-dc power conversion is described as the process of changing the voltage level of a dc source using the PWM technique. However, a more definitive and precise description is necessary to comprehend the natures and features of the PWM dc-to-dc power conversion circuit.

1.1.1 Dc-to-Dc Power Conversion

To formulate an accurate description of the dc-to-dc power conversion, this section discusses two different approaches to operating an electric bulb using a dc voltage sourced from a battery. It is presumed that the electric bulb requires a strict 12 V for operation, while the battery voltage is varied between 18 V and 30 V depending on its charging status. Figure 1.1 shows the first approach where a variable resistor and controller are employed between the battery and electric bulb. The controller is assumed to only draw a negligible current.

In Fig. 1.1, the controller adjusts the resistance of the variable resistor R_x to meet the following relationship

$$V_O = \frac{R_o}{R_x + R_o} V_B = 12 \text{ V} \tag{1.1}$$

where V_O is the voltage across the electric bulb, R_o denotes the resistance of the bulb, and V_B is the battery voltage that varies between $18 \text{ V} < V_B < 30 \text{ V}$. Figure 1.1 certainly fulfills the goal of providing a fixed dc voltage from a variable voltage source, however, it has one critical problem that makes this approach impractical.

The variable resistor is accompanied by an ohmic power loss

$$P_{loss} = P_{in} - P_{out} = I_O V_B - I_O V_O = I_O(V_B - V_O) \tag{1.2}$$

where P_{in} is the input power drawn from the battery, P_{out} is the output power delivered to the electric bulb, and I_O is the current flowing from the battery to the electric bulb. The power loss is given by the product of the load current and the difference

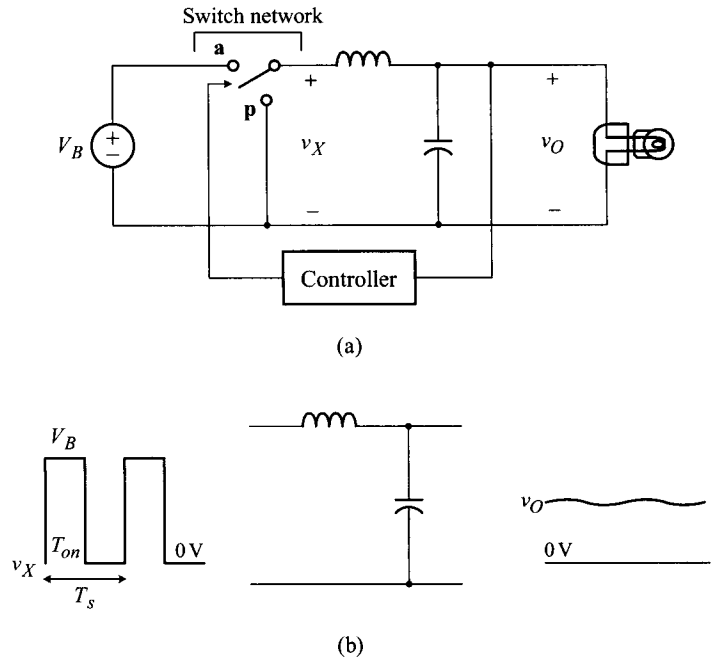

Figure 1.2 Dc-to-dc power conversion applied to power electric bulb. (a) Circuit diagram. (b) Input and output waveforms of LC filter.

between the battery voltage and bulb voltage. This power loss easily becomes significant. For example, when an electric bulb that consumes a 60 W power at 12 V voltage level is connected to a 30 V battery, the power loss is as large as $P_{loss} = (60/12)(30 - 12) = 90$ W. This loss is even larger than the power consumed in the bulb, $P_{out} = 60$ W.

The power loss is always transformed into heat and the resulting heat must be removed using an appropriate cooling system. The cooling system usually employs bulky heat sinks and noisy fans, consequently increasing the size and weight of the entire system. Accordingly, Fig. 1.1 cannot be used for applications where the dimension and weight should be limited, which is usually the case for most modern electronic equipment and systems.

Figure 1.2 shows an alternative approach where a *switch network* and LC filter are inserted between the battery and electric bulb. The switch network periodically changes its connection. Within each switching period T_s, the switch network maintains position **a** for T_{on} and position **p** for the remaining part of the switching period, $T_s - T_{on}$. This switch network is called the *single-pole double-throw (SPDT) switch* because it contains one pole which is always connected to one of the two contacts, the throw **a** and the throw **p**. With the switching action of the SPDT switch, the battery voltage is transformed into a rectangular waveform at the output of the SPDT

switch, v_X in Fig. 1.2. The rectangular waveform is then applied to the LC filter. The LC filter alters the rectangular waveform into a smoothly-filtered continuous voltage waveform, v_O in Fig. 1.2.

If the LC filter provides sufficient filtering, the output voltage nearly becomes a dc waveform corresponding to the average value of v_X

$$v_O(t) \approx V_O = \bar{v}_X(t) = \frac{T_{on}}{T_s} V_B \tag{1.3}$$

To maintain $V_O = 12$ V at the presence of the battery voltage variation, the controller adjusts the ratio T_{on} to T_s. With a fixed T_s, the controller changes T_{on} to meet the condition

$$\frac{T_{on}}{T_s} V_B = 12 \text{ V} \tag{1.4}$$

For example, with a battery voltage $V_B = 24$ V and switching period $T_s = 10\,\mu$s, the controller generates $T_{on} = 5\,\mu$s to produce $V_O = (5 \times 10^{-6}/10 \times 10^{-6})\,24 = 12$ V. If the battery voltage is increased to $V_B = 30$ V, the controller reduces T_{on} to $4\,\mu$s to regulate V_O at 12 V: $V_O = (4 \times 10^{-6}/10 \times 10^{-6})\,30 = 12$ V.

Although Figs. 1.1 and 1.2 both achieve the same goal, a crucial difference exists between them. Figure 1.2 presumes a lossless operation because the SPDT switch and reactive components in the LC filter do not consume any power. The lossless operation eliminates all the problems associated with the power loss. Because no heat management is required, the circuit can be packaged with a smaller size and lighter weight, thereby making it fully compatible with modern electronic systems.

A more definitive description of the dc-to-dc power conversion is now established as the process of changing the voltage level of a dc source, while eliminating or minimizing power loss. In this perspective, Fig. 1.2 is a typical example of the dc-to-dc power conversion circuit, while the conventional circuit illustrated in Fig. 1.1 is not classified so.

1.1.2 PWM Technique

The concept of PWM technique can be envisaged from the operation of Fig. 1.2, where the ratio T_{on} to T_s of the SPDT switch is adjusted to keep the output voltage constant. By changing the T_{on}/T_s ratio, the pulsewidth of the rectangular voltage waveform, which passes through the LC filter to yield its average value as the output voltage, is adaptively modulated so that the output voltage remains constant despite the input voltage variation. This control scheme is called the *pulsewidth modulation (PWM) technique* and the dc-to-dc conversion circuit based on the PWM scheme is known as the *PWM dc-to-dc converter*. The PWM dc-to-dc converter is widely adapted to modern industrial and consumer electronics, thereby becoming the most prevailing dc-to-dc power conversion circuit.

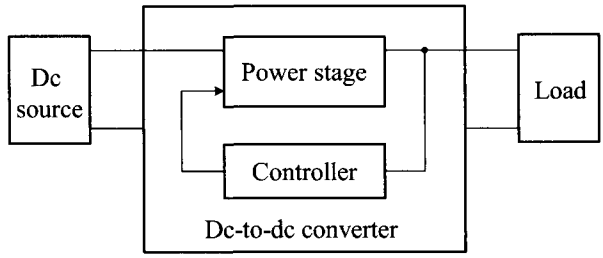

Figure 1.3 Dc-to-dc power conversion system.

1.2 DC-TO-DC POWER CONVERSION SYSTEM

The basic concept illustrated in Fig. 1.2 is generalized into dc-to-dc power conversion systems whose block diagram representation is shown in Fig. 1.3. The system consists of the dc source, dc-to-dc converter, and load. The dc source provides an arbitrary dc voltage to the dc-to-dc converter. The dc-to-dc converter then converts the given dc voltage to the value required by the load and delivers it to the load. The load is an application system that operates with a fixed voltage and eventually consumes electrical power. This section presents the characteristic features of the dc source, dc-to-dc converter, and load.

Dc Source with Non-Ideal Characteristics

The practical dc source falls short of the characteristics of an ideal voltage source in many aspects. First, the voltage level of the dc source could vary with time, as is the case with batteries, fuel cells, and other standalone dc sources. The change in the voltage could occur either gradually or abruptly, depending on the characteristics and condition of the dc source.

Second, a rectified ac source is often used as a substitute for the dc source. For this case, the rectified ac source could contain a considerable amount of ac components, known as *ac ripple*. In addition, the output of the rectified ac source could be corrupted with various noises. Accordingly, the dc source represents any non-ideal source whose voltage can be varied, polluted with ac ripple and noises, and switched from one value to another.

Dc-to-Dc Converter as Voltage Source

The dc-to-dc converter receives an arbitrary voltage from the non-ideal source and is required to provide a fixed dc voltage for the load. Thus, in addition to altering the voltage level, the dc-to-dc converter should have the capacity of maintaining its output constant at the presence of the variation, ac ripple component, and abrupt change in the input voltage. Ideally, the dc-to-dc converter should function as an *ideal*

voltage source, powered by a non-ideal voltage source and programmed to produce the required dc voltage for the load, regardless of the condition of the voltage source.

Although practical dc-to-dc converters are more complicated in their structures and operations than those of Fig. 1.2, they still can be divided into two functional blocks: the power stage and controller. The power stage alters the level of the input voltage into a desired value using various circuit components, while the controller provides the necessary signals for the power stage to execute its function.

Dc-to-dc converters come with numerous variations in their power stage configurations and each dc-to-dc converter is named differently after its power stage structure. In spite of the wide diversity in structure, all the power stages employ the common electronic components to perform the dc-to-dc power conversion. The power stage utilizes semiconductor devices to implement the function of the SPDT switch, energy storage components to perform filtering, and transformers to change the voltage and current levels of circuit variables while transferring electrical energy.

The controller also varies widely in its structure and functionality. Nonetheless, all the controllers perform the same role of providing the control signals that are required for the power stage to generate a fixed output voltage, regardless of variations in the input voltage and other operating conditions. In PWM dc-to-dc converters, this important function is executed in a closed-loop fashion using the PWM technique. The closed-loop PWM controller uses various analog and digital ICs, as well as discrete circuit components, to generate the required control signals.

Load as Dynamic Current Sink

The load of a dc-to-dc converter can be any electronic equipment or system operating with a fixed dc voltage. The load draws the current from the dc-to-dc converter to meet its power requirement. Thus, the load current could fluctuate depending on operational conditions of the load system. In particular, when high-frequency digital systems are connected to a dc-to-dc converter, the current change could occur frequently and rapidly, including step changes between two different values. Accordingly, the load system presents a dynamic current sink to the dc-to-dc converter, whose current level could change widely and abruptly.

1.3 FEATURES AND ISSUES OF PWM DC-TO-DC CONVERTER

The PWM dc-to-dc converter is a dc-to-dc converter that operates based on the principle of PWM. The PWM dc-to-dc converter is intended to function as an efficient and reliable voltage source, interfacing with the non-ideal dc source and dynamic load system. Accordingly, there are specific features demanded for the dc-to-dc converter and issues involved with implementing such features in a PWM dc-to-dc converter.

Power Stage Components

A dc-to-dc converter employs semiconductor devices, reactive components such as inductors and capacitors, and transformers in the power stage; in contrast, the power stage never contains any resistive component in order to avoid power loss. The semiconductor devices are employed as the switches that losslessly alternate on-state and off-state at very high frequency, up to several MHz range in some applications. Due to this switching action, all the power stage components are subjected to periodic voltage and current excitations. The switching action and periodic operation are the characteristic features of the power stage components employed in dc-to-dc converters. Circuit analysis skills beyond the standard linear circuit theory are required for understanding the operations of the power stage components under periodic switching operations.

Power Stage Configuration

A dc-to-dc converter is required to accept an arbitrary voltage as the input and to generate a predetermined output voltage. The ratio between the input voltage and output voltage could be either very large or considerably small. Also, a dc-to-dc converter should provide an arbitrary load current, as required by the load. Accordingly, there are demanding requirements for the converter power stage in voltage and current ratings, input-to-output voltage ratio, and power handling capacity. In addition, dc-to-dc converters are frequently needed to provide galvanic isolation between the source and load. To meet these demands, numerous power stage configurations have been developed, each with a different complexity and functionality. The power stage configuration occupies a large and important portion of the dc-to-dc power conversion technology.

Dynamic Modeling and Analysis

A dc-to-dc converter should function as a voltage source which holds its output voltage constant at the desired value, irrespective of any possible changes in the input voltage, load current, and other operational conditions. This vital function is achieved by the closed-loop feedback controller operating under the principle of PWM.

It is well known that a closed-loop controlled system becomes unstable if the system is not properly designed. Stability can be assessed by investigating the dynamic characteristics of the closed-loop controlled system. There are many analytical methods to determine whether a closed-loop controlled system is stable or not. However, these methods are mainly intended for linear time-invariant systems. As will be discussed in Chapter 5, the PWM dc-to-dc converter falls into the category of the nonlinear time-variant system to which the aforementioned stability analysis methods cannot be directly applied.

The dynamic modeling refers to the analytical process of describing the dynamic characteristics of the nonlinear PWM dc-to-dc converter in a special format to which all the classical analysis methods, originally aimed to linear systems, can be applied.

Accordingly, the dynamic modeling allows us to investigate the stability and performance of the nonlinear PWM dc-to-dc converter using the familiar classical control theory. The dynamic modeling and ensuing analysis using the resultant model are collectively referred to as the *dynamic modeling and analysis*. The dynamic modeling and analysis plays an important role in the PWM power conversion technology and deserves rigorous treatment.

Dynamic Performance and Control Design

The performance of a dc-to-dc converter will be divided into two categories in this book: the static performance and dynamic performance. The *static performance* characterizes the dc-to-dc converter as a static voltage source. The static performance includes the input-to-output voltage conversion ratio and power handling capacity. The static performance is solely determined by the power stage and is irrelevant to the feedback controller.

The second category is the *dynamic performance* which depicts the dc-to-dc converter as a closed-loop controlled dynamic system. The most important dynamic performance is *stability*. The dc-to-dc converter should establish a periodic steady-state operation to produce the desired output voltage. When a certain disturbance is introduced, the converter could temporarily deviate from its steady-state operation. However, the converter should always return to the original operating point as the disturbance disappears. This essential feature is possible only when the converter meets the stability criterion.

Another important dynamic performance is the step load response. A stable dc-to-dc converter provides a fixed steady-state output voltage, regardless of any changes in the load current. When a step change occurs in the load current, the output voltage of the converter would show a transitional excursion before it returns to its steady-state value. The transitional output voltage response is called the *step load response* in this book. The step load response is of particular concern when digital logic circuits are employed as the load. Modern logic circuits operate with a very tightly-regulated low voltage, for example 2.1 ± 0.02 V, and draw a large pulsating current. These logic circuits naturally and frequently incur substantial step changes in the load current. For this case, the output voltage excursion should be minimized, in order to avoid the potential failure of digital logic circuits due to an excessive transitional overshoot or undershoot in the supply voltage.

The dynamic performance is solely determined by the design of the feedback controller. For a given power stage configuration, the controller should be designed for stability and good dynamic performance. While the controller design is primarily based on the dynamic modeling and analysis, it also requires extensive knowledge about the control theory, linear system theory, and feedback compensation design.

1.4 CHAPTER HIGHLIGHTS

This book is aimed to cover the PWM dc-to-dc power conversion, while focusing on the features and issues addressed in the previous section. Chapter 2 deals with the power stage components. This chapter presents the circuit behavior of semiconductor switches, inductors, capacitors, and transformers, all operating under periodic excitations. First, Chapter 2 describes the operation of MOSFETs as an active switch, diodes as a passive switch, and MOSFET-diode pairs as a single-pole double-throw (SPDT) switch. Then, this chapter discusses the basic circuit equations of inductors and capacitors. Chapter 2 also presents important circuit theorems pertinent to inductors and capacitors under periodic excitations. Lastly, this chapter describes the operation of transformers and introduces a circuit model for practical transformers.

Chapter 3 presents the simplest dc-to-dc power conversion circuit, known as the buck converter. Theoretical basics and operational details of the buck converter are both presented. This chapter also illustrates circuit analysis techniques that are commonly applicable to all other forthcoming PWM dc-to-dc converters. In addition, Chapter 3 discusses the underlying basics of the PWM technique and closed-loop control of dc-to-dc converters. Chapter 4 deals with the topology and operation of an important class of PWM dc-to-dc converters. For each converter, the origin of the circuit topology is first illustrated and the steady-state operation is then investigated, using the analysis techniques established in Chapter 3.

Dc-to-dc converters employ semiconductor switches in their power stage to achieve efficient power conversion. Depending on the status of switches, the structure of converters' power stage changes over time, thus becoming nonlinear time-variant systems. Conventional linear analysis techniques cannot be directly applied to nonlinear time-variant dc-to-dc converters. To circumvent this obstacle, the dynamic modeling has been developed for PWM dc-to-dc converters.

Chapter 5 covers the dynamic modeling of PWM dc-to-dc converters. This chapter illustrates the procedures of describing the dynamic characteristics of nonlinear time-variant dc-to-dc converters, using the terms and formats that have been used for linear time-invariant systems. As the ultimate outcome of the dynamic modeling, this chapter provides a linear circuit model for PWM dc-to-dc converters, which allows us to investigate the nonlinear converter dynamics using conventional linear analysis techniques. Chapter 6 presents the dynamic analysis of PWM dc-to-dc converters using the linear circuit model developed in Chapter 5. This chapter describes the dynamic characteristics of an important class of PWM dc-to-dc converters, thus providing theoretical foundations for the control design and closed-loop analysis.

In Chapter 7, the dynamic performance of the closed-loop controlled dc-to-dc converter is discussed. The implication and significance of the performance criteria are demonstrated with practical examples. Chapter 8 is devoted to the closed-loop performance analysis and feedback controller design. This chapter first introduces a graphical analysis method which greatly facilitates the dynamic analysis and control design. Using this method, this chapter presents detailed controller design procedures. Impacts of the control design on the dynamic performance are discussed. Chapter 9 addresses the practical considerations in modeling, analysis, and design of

PWM converters. This chapter illustrates how the outcomes of the earlier chapters, developed for the PWM converters under *ideal* operational conditions, can be adapted to all practical dc-to-dc converters with *non-ideal* operational conditions.

The last two chapters of this book address theoretical and technical details of one very important topic of PWM dc-to-dc converters — *current mode control.* Current mode control, which distinguishes itself from the conventional control scheme covered in Chapter 8 by employing an additional current feedback, is the most prevailing control scheme for modern PWM dc-to-dc converters. Chapter 10 presents functional basics and dynamic analysis of current mode control. The motivation and benefits of current mode control are described. The converter dynamics under current mode control are investigated, leading to general procedures for the closed-loop analysis.

Chapter 11 deals with the *sampling effects* of current mode control. The origin and consequence of the sampling effects are discussed. This chapter extensively analyzes the sampling effects with focuses on the converter dynamics and performance. Based on the analysis results, systematic design procedures for current mode control are established. This chapter also presents applications of current mode control to practical PWM dc-to-dc converters. Several design examples are given to substantiate theoretical discussions.

REFERENCES

1. R. W. Erickson and D. M. Maksimović, *Fundamentals of Power Electronics*, 2nd Ed., Kluwer Academic Publishers, 2001.
2. R. D. Middlebrook and S. Ćuk, *Advances in Switch-Mode Power Conversion*, TESLAco, Pasadena, CA, 1983.

CHAPTER 2

POWER STAGE COMPONENTS

Power stages of PWM dc-to-dc converters contain semiconductor switches, inductors, capacitors, and transformers. This chapter describes the operations of these power stage components under periodic excitations. The current chapter also presents several important circuit theorems that will be used in later chapters for the analysis of dc-to-dc power conversion circuits. Finally, this chapter analyzes two practical switching circuits, the solenoid drive circuit and capacitor charging circuit, in order to demonstrate the functions of power stage components in real applications.

2.1 SEMICONDUCTOR SWITCHES

Dc-to-dc power conversion circuits extensively use active and passive semiconductor switches. The active switch usually refers to the three-terminal semiconductor device whose *on/off* status is actively controlled by exciting one of the device terminals. On the other hand, the passive switch is the two-terminal device whose on/off status is passively determined by the conditions of the application circuit. The switching action of active and passive semiconductor switches allows the voltage and current waveforms of the application circuit to be altered, as required to perform the desired dc-to-dc power conversion.

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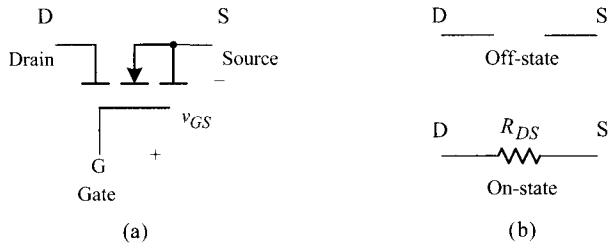

Figure 2.1 MOSFET. (a) Circuit symbol. (b) Circuit representations.

As illustrated in Fig. 1.2 in Section 1.1.1, the dc-to-dc power conversion is performed by converting the dc voltage into a rectangular waveform and filtering the resulting rectangular voltage into another dc voltage. The conversion from the dc input to the intermediate rectangular waveform is performed using the single-pole double-throw (SPDT) switch. It will be shown that the SPDT switch is implemented with a pair of active and passive semiconductor switches.

There are numerous semiconductor switches available for dc-to-dc conversion circuits. The selection of switching devices depends on both how well the existing devices perform and what the application circuits require. In many dc-to-dc conversion circuits, MOSFETs are commonly used for active switches because of their fast switching characteristics compared with other alternatives. For passive switches, fast recovery diodes or Schottky diodes are used due to their excellent switching characteristics. This section describes the function of MOSFETs as an active switch, diodes as a passive switch, and MOSFET-diode pairs as an SPDT switch. Emphases are placed on the functional behavior of these devices in dc-to-dc power conversion circuits, rather than on their physical or operational principles.

2.1.1 MOSFETs

When employed as an active switch, MOSFETs can only have either an off-state or on-state. Figure 2.1 shows the symbol of an n-channel MOSFET and its circuit representations for the off-state and on-state. When the gate drive signal, denoted by v_{GS} in Fig. 2.1(a), is below the threshold voltage, the MOSFET is turned-off. At the off-state, the drain-source terminal simply behaves open-circuited because the conduction channel is not created. When the gate drive signal is larger than the threshold voltage, the conduction channel is formed and the MOSFET is turned-on. Once turned-on, the drain and source terminals are connected through the resistance of the conduction channel, denoted by R_{DS} in Fig. 2.1(b). While the resistance R_{DS} varies with the voltage and current ratings of MOSFETs, it is usually so small that a turned-on MOSFET can be viewed as a short circuit.

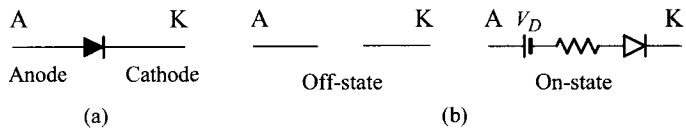

Figure 2.2 Diode. (a) Circuit symbol. (b) Circuit representations.

2.1.2 Diodes

Diodes always presume one of two possible states, the off-state or on-state. Figure 2.2 depicts the symbol of a diode and its circuit representations for off-state and on-state. At an off-state, the diode becomes open-circuited. At an on-state, a practical diode can be viewed as a series connection of a voltage source V_D, resistor, and *ideal* diode. The voltage source and resistor are necessary to approximate the nonlinear $v - i$ characteristics of the diode to a piecewise linear function. The ideal diode ensures the *unidirectional* current flow from the anode terminal to cathode terminal. While the values of the voltage source and resistor vary with types of diodes, they are usually negligibly small. Accordingly, the on-state circuit representation is approximated to a short circuit for practical circuit analyses.

The state of a diode is determined by the condition of the application circuit. When the application circuit forces a positive voltage from the anode to cathode terminal, the diode establishes the on-state. Conversely, when the application circuit imposes a negative voltage, the diode is turned-off. As an illustration, Fig. 2.3(a) shows a

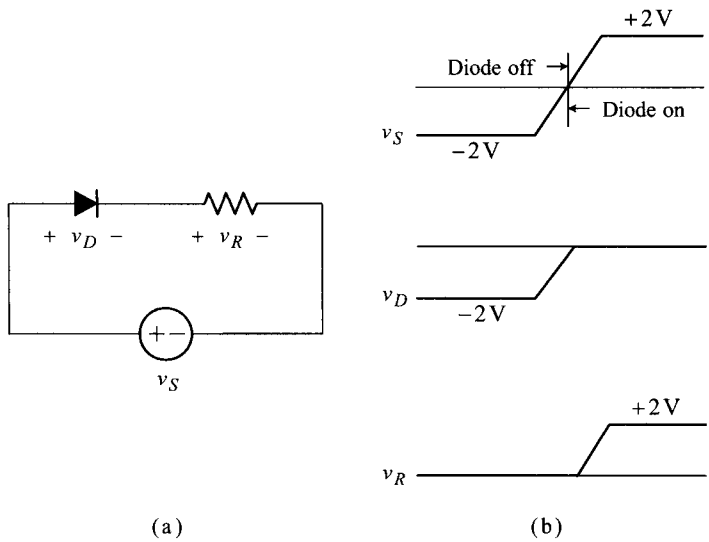

Figure 2.3 Diode switching with voltage source. (a) Circuit diagram. (b) Voltage waveforms.

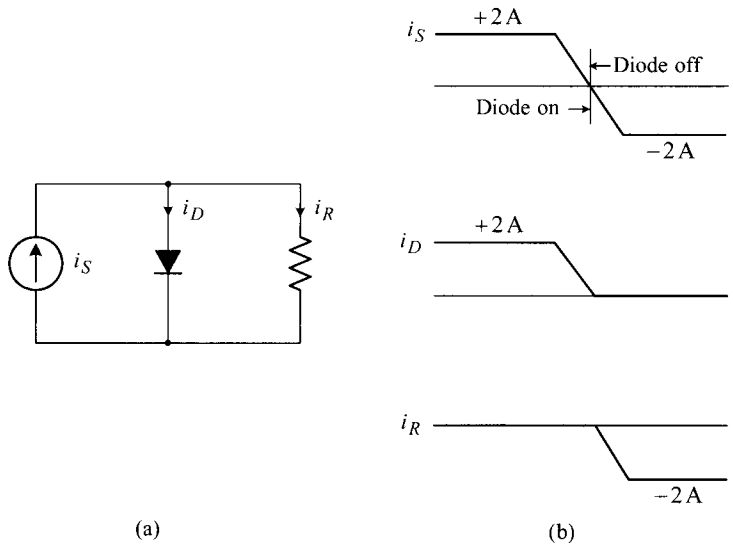

Figure 2.4 Diode switching with current source. (a) Circuit diagram. (b) Current waveforms.

simple circuit consisting of a diode, resistor, and time-varying voltage source, v_S. The diode is turned-off when v_S is negative and turned-on when v_S is positive. The transition from the off-state to on-state occurs at the moment the negative voltage v_S increases to hit the *zero* voltage. The voltage waveforms across the diode and resistor are determined as shown in Fig. 2.3(b), based on the circuit behavior of the diode at the on-state and off-state.

The state of a diode can also be judged based on the direction of the current flow. When the application circuit forces a *positive* current flow from the anode to cathode terminal, the diode is turned-on and retains the on-state as long as the current remains positive. On the other hand, when the application circuit forces a *negative* current flow from the cathode to anode terminal, the diode becomes open-circuited. Figure 2.4 is a simple circuit which illustrates the diode switching using a time-varying current source, i_S. When i_S is positive, the diode is turned-on and carries the entire current. Conversely, when i_S becomes negative, the diode is turned-off and the current diverts to the resistor. The transition from the on-state to off-state happens at the instant the positive current i_S reduces to the *zero* current.

2.1.3 MOSFET-Diode Pair as SPDT Switch

Figure 2.5(a) shows a simple switching circuit where a voltage source is connected to a current source via an SPDT switch. The SPDT switch toggles its position periodically as illustrated in Fig. 2.5(a). Figure 2.5(b) shows representations of the switching circuit with two different switch positions: one is at the **a** position and the

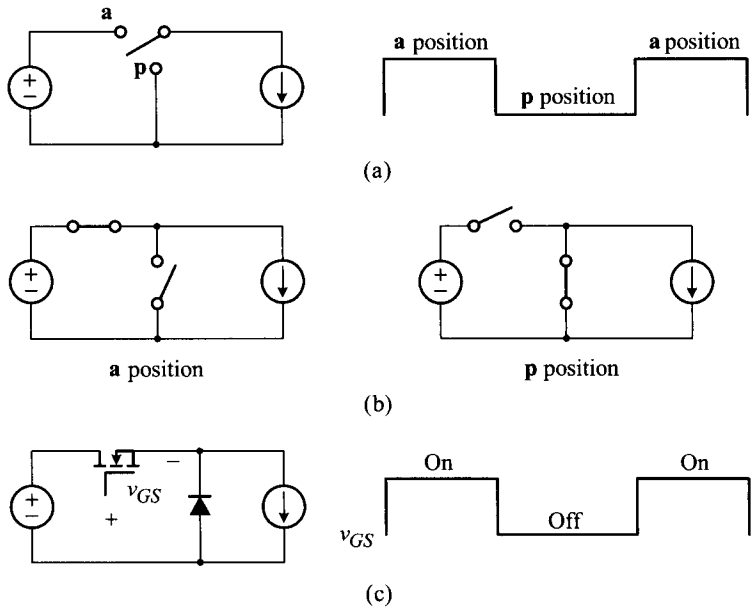

Figure 2.5 Simple switching circuit. (a) Original circuit with SPDT switch. (b) Equivalent circuits. (c) Implementation of SPDT switch using semiconductor switches.

other is at the **p** position. Finally, Fig. 2.5(c) depicts an implementation of the SPDT switch using MOSFET and diode.

The MOSFET is turned-on/off by the gate drive signal v_{GS}. When the MOSFET is turned-on by the *on* signal, the diode is turned-off because the voltage source forces a negative voltage across the diode. Conversely, when the MOSFET is turned-off by the *off* signal, the current source forces the diode to turn on. The equivalence between Fig. 2.5(a) and Fig. 2.5(c) now becomes apparent. As shown in this example, the SPDT switch can readily be implemented using the MOSFET-diode pair.

2.2 ENERGY STORAGE AND TRANSFER DEVICES

Dc-to-dc power conversion circuits utilize energy storage devices to perform filtering and energy transfer devices to transfer electrical energy while altering the magnitude of voltage and current waveforms. Energy storage and transfer devices include inductors, capacitors, and transformers. This section analyzes the circuit behavior of such devices under periodic excitations.

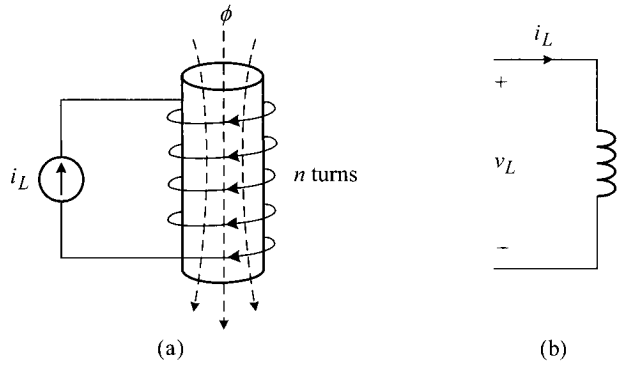

Figure 2.6 Inductor and terminal properties. (a) Electro-magnetic process within inductor. (b) Polarity/direction of inductor voltage/current waveform.

2.2.1 Inductors

This section deals with circuit properties of inductors. In addition to basic circuit equations, the current section discusses the operations of inductors under periodic excitations. This section also presents important circuit theorems for inductors.

Circuit Equations

An inductor is typically constructed by winding a copper wire on a magnetic core. When the inductor is excited by a current source i_L as shown in Fig. 2.6(a), a series of electro-magnetic phenomena occur inside the magnetic core. First, the current passing through the copper winding creates magnetic field intensity H. The magnetic field intensity in turn produces magnetic flux density: $B = \mu H$ with μ representing the permeability of the core. The total magnetic flux inside the core is then calculated as $\phi = BS$ where S is the cross-sectional area of the core. Finally, the magnetic flux linkage is given by $\lambda = n\phi$ where n is the number of the copper winding turns. The cause-and-effect of the aforementioned process is summarized as $i_L(t) \Rightarrow H(t) \Rightarrow B(t) \Rightarrow \phi(t) \Rightarrow \lambda(t)$. When the current i_L is considered as the input of the electro-magnetic process, the magnetic flux linkage λ becomes the output of the process. The ratio of the output variable, λ , to the input variable of the process, i_L, is defined as the inductance of the inductor

$$L \equiv \frac{\lambda(t)}{i_L(t)} \tag{2.1}$$

According to Faraday's law, the time-varying magnetic flux linkage induces a voltage across the inductor terminals

$$v_L(t) = \frac{\mathrm{d}\lambda(t)}{\mathrm{d}(t)} \tag{2.2}$$

Using the definition of the inductance, Faraday's law is rewritten as

$$v_L(t) = L\frac{di_L(t)}{dt} \tag{2.3}$$

thus establishing the $v-i$ relationship of the inductor. The polarity of the induced voltage is defined as shown in Fig. 2.6(b).

Equation (2.3) is integrated to yield an alternative circuit equation for the inductor

$$i_L(t) = \frac{1}{L}\int v_L(t)\,dt \tag{2.4}$$

When a dc voltage V_S is applied across the inductor, the inductor current is given by

$$i_L(t) = \frac{V_S}{L}t \tag{2.5}$$

Expression (2.5) indicates that the inductor current continues to increase linearly without bounds, as long as the dc voltage is present. In practice, however, a real inductor cannot sustain an excessively large current and eventually becomes saturated. The saturation of an inductor will be discussed later in this section.

■ EXAMPLE 2.1 Inductance of Toroidal Inductor

This example illustrates the inductance of an inductor fabricated using a toroidal core, as depicted in Fig. 2.7. Referring to Fig. 2.7(a), the magnetic flux linkage of the inductor is given by

$$\lambda(t) = n\phi(t) = nSB(t) = nS\mu H(t) = \mu_r\mu_o nSH(t) \tag{2.6}$$

where μ_r is the relative permeability of the core material, μ_o is the permeability of free space, n denotes the turns of the inductor winding, and S is the cross-sectional area of the core. On the other hand, Ampere's law leads to the relationship

$$H(t)\,l_m = n\,i_L(t) \quad \Rightarrow \quad H(t) = \frac{n\,i_L(t)}{l_m} \tag{2.7}$$

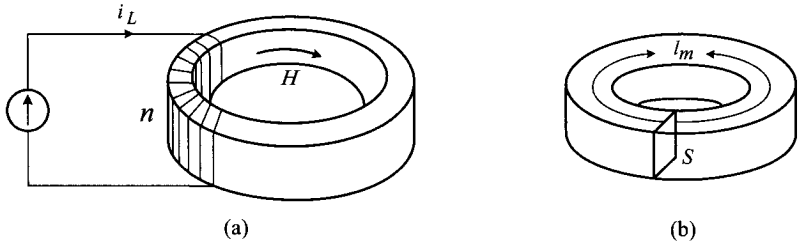

Figure 2.7 Toroidal inductor. (a) Inductor structure. (b) Geometry of toroidal core.

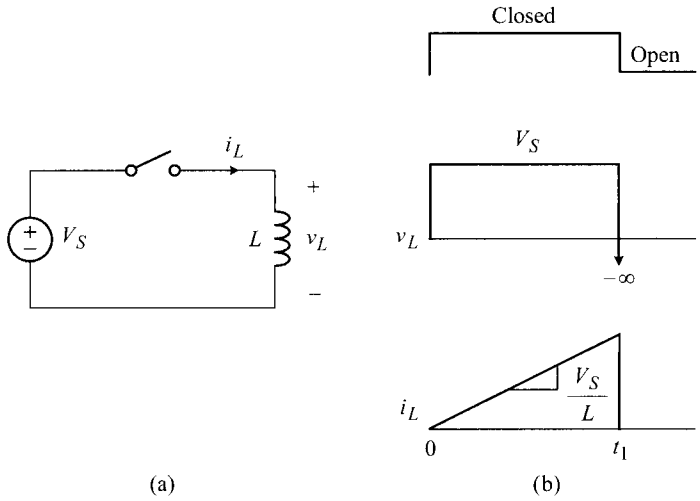

Figure 2.8 Inductive switching circuit. (a) Circuit diagram. (b) Circuit waveforms.

where l_m is the length of the magnetic path along the toroidal core. From (2.6) and (2.7), it follows that

$$\lambda(t) = \mu_r \mu_o \frac{S}{l_m} n^2 i_L(t) \tag{2.8}$$

Finally, the inductance of the toroidal inductor is given by

$$L = \frac{\lambda(t)}{i_L(t)} = \mu_r \mu_o \frac{S}{l_m} n^2 \tag{2.9}$$

■ EXAMPLE 2.2 Inductive Switching Circuit

This example illustrates the circuit behavior of the inductor excited by a pulse voltage waveform. Figure 2.8 shows a simple switching circuit along with its circuit waveforms. Assume that the inductor is initially unenergized and the switch is opened. When the switch is closed at $t = 0$, a dc voltage V_S is applied across the inductor and i_L starts to increase linearly with a slope V_S/L. The switch is then opened at $t = t_1$, thereby forcing the inductor current to collapse. The change in the inductor current in turn induces a voltage across the inductor. Equation (2.3) indicates that a negative voltage, whose magnitude is proportional to the decaying slope of the inductor current, will be induced across the inductor.

When the switch is assumed to open instantaneously, the magnitude of the induced voltage is infinite. In practice, however, the magnitude of the negative

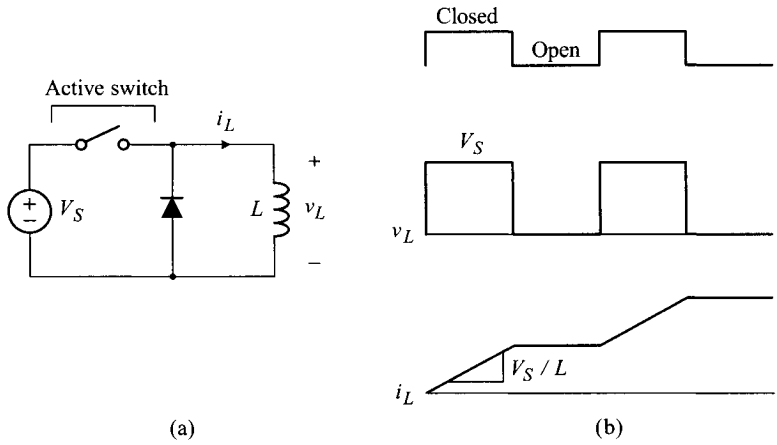

Figure 2.9 Inductive switching circuit. (a) Circuit diagram. (b) Circuit waveforms.

voltage is finite because a real switch can only react with finite response time. Even so, the magnitude is still large enough to destroy any practical semiconductor switch.

The behavior of the inductor in this example can also be explained using the energy conservation principle. As the inductor current ramps up, the magnetic energy stored inside the inductor continues to increase. When the inductor current is collapsed at $t = t_1$, the total energy $E_m = 0.5L\big(i_L(t_1)\big)^2$ is instantaneously released in the shape of a voltage spike. As illustrated in this example, a sudden interruption of the inductor current incurs a *destructive* voltage spike and therefore should be avoided, unless the circuit is intentionally designed to operate so.

■ EXAMPLE 2.3 Inductive Switching Circuit

This example shows the operation of another inductive switching circuit. In the circuit depicted in Fig. 2.9(a), a dc voltage source is connected to an inductor through an active-passive switch pair. In Fig. 2.9, the on/off status of the active switch is controlled by the switch drive signal shown in Fig. 2.9(b). As explained earlier, the active-passive switch pair functions as an SPDT switch. When the active switch turns on, the passive switch is turned-off; conversely, when the active switch turns off, the passive switch is turned-on. With the active switch turned-on, the dc voltage V_S is applied across the inductor L and the inductor current thus ramps up with a slope V_S/L.

When the active switch turns off, the diode is turned-on because the current-carrying inductor behaves as a current source. Once the diode is turned-on, the voltage across the inductor becomes zero. According to (2.3), the inductor

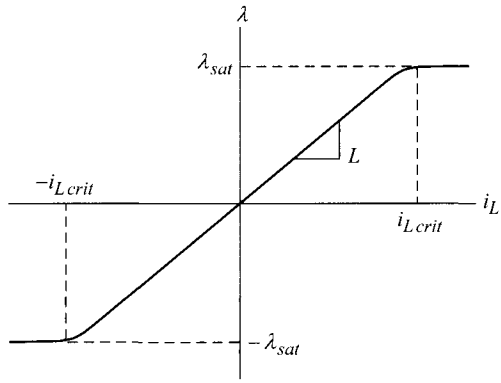

Figure 2.10 i_L–λ characteristics of inductor.

current remains constant when its voltage is zero; the inductor current thus maintains the value that appeared before the switch is turned-off. When the switch is turned-on in the next operational cycle, the inductor current again starts to increase. By repeating this process, the inductor current proceeds as depicted in Fig. 2.9(b).

Saturation of Inductor

Figure 2.10 illustrates the relationship between the inductor current i_L and magnetic flux linkage λ. As i_L is increased from zero, so is λ. However, the linear relationship between i_L and λ is valid only within a limited range. When the inductor current exceeds the critical values, $\pm i_{Lcrit}$ in Fig. 2.10, the magnetic flux linkage remains the same at $\pm \lambda_{sat}$, regardless of the magnitude of the inductor current; this phenomenon is referred to as magnetic saturation. Because the slope of the i_L–λ curve represents the inductance as shown in (2.1), the saturation implies a *zero* inductance for the inductor. Thus, the saturation causes a profound impact on the circuit operation. For example, when a dc voltage V_S is applied to an inductance L, the current increases towards i_{Lcrit} by the equation $i_L(t) = (V_S/L)t$. When the inductor current reaches i_{Lcrit}, magnetic saturation occurs. Upon magnetic saturation, the inductor current shoots up boundlessly because the inductance becomes *null* at the instant of saturation. Because a real circuit cannot support such an excessive inductor current, magnetic saturation should be avoided to prevent a catastrophic failure of the circuit.

Magnetic saturation is attributed to the properties of the core material of the inductor. Numerous magnetic dipoles exist inside the core material. When no external current is present, the magnetic dipoles are randomly oriented. For this case, the core material does not exhibit any magnetic properties because the effects of individual magnetic dipoles are canceled by each other.

When the inductor current begins to flow, the magnetic field is developed inside the core and some magnetic dipoles start to align in parallel with the magnetic field,

thereby generating additional magnetic flux; this effect is known as the magnetic induction. As the current continues to grow, more magnetic dipoles align with the magnetic field, thereby increasing the magnetic flux. When the inductor current reaches the critical value i_{Lcrit}, all the magnetic dipoles line up in parallel with the magnetic field and the magnetic flux attains its maximum value, λ_{sat}. The core now becomes saturated and the magnetic flux remains at λ_{sat} even if the inductor current is further increased.

Flux Balance Condition or Volt-Sec Balance Condition

In most switching circuits, inductors are operated in such a way that the magnetic flux is increased during one part of a switching period and then decreased during the other part of the same switching period. The *flux balance condition* asserts that the flux increase in one switching period should be equal to the flux decrease in that switching period, or equivalently the net change in the magnetic flux over one switching period must be zero.

The justification for the flux balance condition is self-explanatory. If the net flux change within each switching period is not balanced at zero, the flux will continue to grow towards the positive direction or negative direction, eventually encountering the magnetic saturation. Therefore, all the inductors in a properly-designed inductive switching circuit should satisfy the flux balance condition.

The flux balance condition can also be paraphrased into an alternative form, which is more convenient for circuit analysis purposes. Faraday's law states that

$$v_L(t) = n\frac{\mathrm{d}\phi(t)}{\mathrm{d}t} \tag{2.10}$$

where v_L is the instantaneous voltage across the inductor, n is the number of turns of the inductor winding, and ϕ denotes the magnetic flux inside the inductor. Equation (2.10) is rearranged as

$$\mathrm{d}\phi(t) = \frac{v_L(t)}{n}\mathrm{d}t \tag{2.11}$$

to express the flux change as a function of the inductor voltage. Now assume that the inductor is excited by a rectangular voltage waveform in Fig. 2.11. The positive voltage V_1 increases the magnetic flux, whereas the negative voltage $-V_2$ decreases the flux. The flux increase during T_1 is given by

$$\Delta\phi_{inc} = \frac{V_1}{n}T_1 \tag{2.12}$$

and the flux decrease during T_2 becomes

$$\Delta\phi_{dec} = \frac{V_2}{n}T_2 \tag{2.13}$$

By equating (2.12) and (2.13) based on the flux balance condition, it follows that

$$\Delta\phi_{inc} = \Delta\phi_{dec} \quad \Rightarrow \quad V_1T_1 = V_2T_2 \tag{2.14}$$

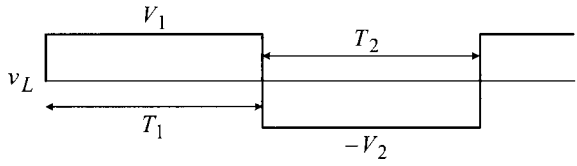

Figure 2.11 Volt-sec balance condition: $V_1T_1 = V_2T_2$.

which states that the product of the voltage and time interval during which the inductor voltage is positive should be equal to that calculated when the inductor voltage is negative, or equivalently *the average value of the inductor voltage over one switching period must be zero.* This principle is referred to as the *volt-sec balance condition.* The volt-sec balance condition is generalized as follows. The average value of the inductor voltage calculated over integer multiples of the switching period is zero. Furthermore, the average value of the inductor voltage in general can be considered to be zero, assuming that the averaging is performed over a sufficiently longer period than the switching period.

An inductive switching circuit will establish the steady-state equilibrium where all the circuit variables are settled down into the values that satisfy the volt-sec balance condition on inductors. Thus, the volt-sec balance condition can be used as a circuit theorem in evaluating steady-state values of circuit waveforms.

Freewheeling Path and Freewheeling Diode

The inductor current should not be discontinued abruptly because a sudden interruption of the inductor current generates a destructive high voltage spike. Therefore, the circuit path, which is connected to an inductor and will be open-circuited during the circuit operation, should always be accompanied by an alternative circuit path, which becomes operative only when the original inductor current path is broken. This alternative path for the inductor current is called the *freewheeling path.* The freewheeling path is usually constructed with a diode which is normally turned-off and only becomes turned-on when the original inductor current path is disrupted. The diode employed to provide a freewheeling path is called a *freewheeling diode.*

■ EXAMPLE 2.4 Inductive Switching Circuit with Freewheeling Path

This example illustrates the operation of an inductive switching circuit with a freewheeling path. Figure 2.12 shows the circuit diagram and waveforms of an inductive switching circuit. If the freewheeling diode located in the middle of Fig. 2.12(a) is not present, a high voltage spike will be generated when the switch is opened. The freewheeling diode prevents the occurrence of such a voltage spike. When the switch turns off, the freewheeling diode is now turned-on, thereby creating a freewheeling path for the inductor current.

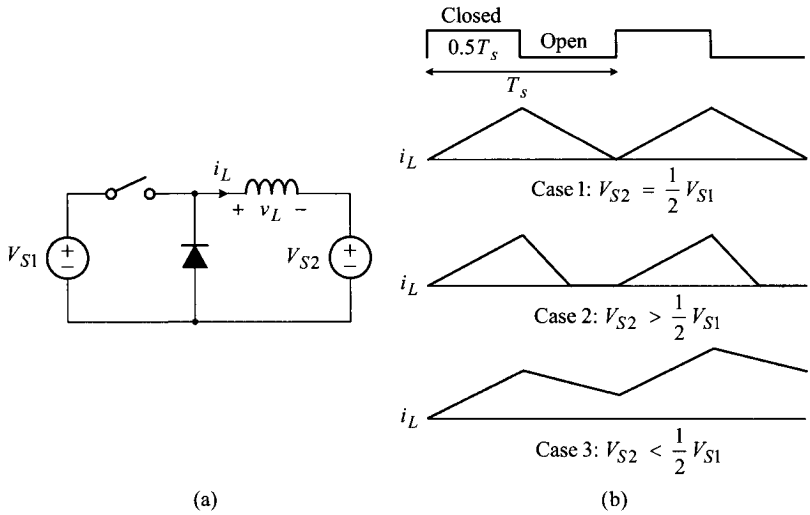

Figure 2.12 Inductive switching circuit with freewheeling path. (a) Circuit diagram. (b) Inductor current waveforms.

When the switch is turned-on, the inductor current increases according to the equation

$$i_L(t) = \frac{v_L}{L}t = \frac{V_{S1} - V_{S2}}{L}t \tag{2.15}$$

On the other hand, when the switch is turned-off and the freewheeling diode conducts, the inductor current decreases as

$$i_L(t) = -\frac{V_{S2}}{L}t \tag{2.16}$$

Now, it is assumed that the active switch is turned-on for half the switching period and turned-off for the remaining switching period, as shown in Fig. 2.12(b). With this assumption, the following three different cases are considered:

- Case 1: $V_{S2} = \frac{1}{2}V_{S1}$
- Case 2: $V_{S2} > \frac{1}{2}V_{S1}$
- Case 3: $V_{S2} < \frac{1}{2}V_{S1}$

The inductor current waveforms, i_L, for these three cases are shown in Fig. 2.12(b). For Case 1, the increasing slope of the inductor current is identical to the decreasing slope, resulting in a periodic triangular waveform. For Case

2, the falling rate is faster than the rising rate, as such, the inductor current i_L is reduced to zero before the onset of the next operational period. When i_L is reduced to zero, the diode turns off and remains off for the remaining switching period because the diode cannot carry the current in the reverse direction.

Finally, for Case 3, the rate of the inductor current falling is slower than the rate of the inductor current rising. At each switching period, the final value of the inductor current will be larger than the initial value. Accordingly, the inductor current will respond as shown in Fig. 2.12(b). Case 3 violates the flux balance condition and the circuit never reaches steady state. This circuit will eventually encounter inductor saturation and ensuing catastrophic failure. Readers are urged to sketch the inductor voltage waveforms for the three cases, in order to confirm the compliance with or violation of the volt-sec balance condition on the inductor, particularly to understand how Case 2 meets the volt-sec balance condition.

2.2.2 Capacitors

Along with inductors, capacitors are widely used in dc-to-dc power conversion circuits as an energy storage component. This section discusses the circuit properties of capacitors and investigates their operation under periodic excitations. The current section also presents important circuit theorems for capacitors.

Circuit Equations

Capacitors are typically fabricated by placing a pair of conductor plates in parallel and filling the gap with a dielectric material. When a voltage source is applied across the parallel plates, the capacitor accumulates electric charge inside the dielectric material, as shown in Fig. 2.13. The capacitance C of a capacitor is defined as the ratio of the accumulated electric charge q to the applied voltage v_C

$$C \equiv \frac{q(t)}{v_C(t)} \tag{2.17}$$

On the other hand, the current through the capacitor is defined as

$$i_C(t) \equiv \frac{\mathrm{d}q(t)}{\mathrm{d}t} \tag{2.18}$$

Using the definition of the capacitance in (2.17), (2.18) is rearranged as

$$i_C(t) = C\frac{\mathrm{d}v_C(t)}{\mathrm{d}t} \tag{2.19}$$

leading to the $v-i$ relationship for capacitors. Equation (2.19) is integrated to yield an alternative circuit equation for capacitors

$$v_C(t) = \frac{1}{C}\int i_C(t)\,\mathrm{d}t \tag{2.20}$$

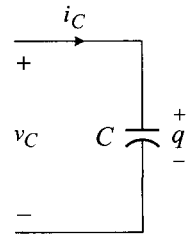

Figure 2.13 Capacitor and polarity/direction of terminal voltage/current waveforms.

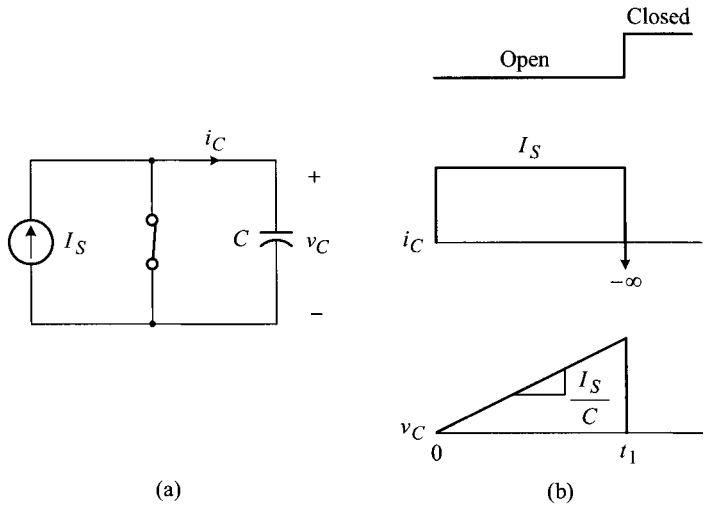

Figure 2.14 Capacitive switching circuit. (a) Circuit diagram. (b) Circuit waveforms.

The polarity/direction of the voltage/current waveform associated with a capacitor is defined as shown in Fig. 2.13.

When a capacitor is connected to a dc current I_S, the voltage across the capacitor rises linearly

$$v_C(t) = \frac{I_S}{C}t \tag{2.21}$$

Equation (2.21) indicates that the capacitor voltage continues to increase boundlessly at the presence of the dc current. However, a practical capacitor will be damaged or destroyed when the capacitor voltage is increased excessively.

■ EXAMPLE 2.5 Capacitive Switching Circuit

This example illustrates the operation of a simple capacitive switching circuit. Figure 2.14(a) shows a capacitive switching circuit where an ideal current

source is connected to an uncharged capacitor. The switch in the middle of the circuit is initially closed. When the switch is opened at $t = 0$, the dc current I_S flows into the capacitance C, thereby raising the capacitor voltage as $v_C(t) = (I_S/C)t$. When the switch is closed at $t = t_1$, the capacitor voltage is forced to collapse. A sudden collapse of the capacitor voltage in turn induces an infinitely large current according to (2.19).

Certainly, a real semiconductor switch cannot carry such a large current and will be permanently damaged. In terms of the energy conservation principle, the energy accumulated in the capacitor at $t = t_1$, $E_e = 0.5C(v_C(t_1))^2$, is instantaneously released when the switch is closed. This instantaneous energy discharge will destroy the semiconductor switch.

■ EXAMPLE 2.6 Capacitive Switching Circuit

This example shows the operation of another capacitive switching circuit. Figure 2.15(a) shows a capacitive switching circuit in which the current source is connected to a capacitor through a diode. The switch in the middle of the circuit is initially closed. When the switch is opened, the current source turns on the diode and charges the capacitor, thereby raising the capacitor voltage by the equation $v_C(t) = (I_S/C)t$. When the switch is closed, the diode is reverse-biased by the elevated capacitor voltage. The capacitor voltage remains constant because the capacitor is isolated from the current source by the turned-off diode. The diode, which isolates the charged capacitor from the current source, is called an *isolation diode.* When the switch is opened in the next switching period, the capacitor voltage starts to rise again. By repeating this process, the circuit produces the waveforms shown in Fig. 2.15(b).

Insulation Breakdown

As the capacitor voltage continues to rise, it eventually reaches the critical value that breaks the insulation of the dielectric material inside the capacitor. This insulation breakdown causes permanent damage to the capacitor and application circuit. Accordingly, all capacitors are specified with the highest voltage they can sustain. The circuit shown in Fig. 2.15 is not practical because the capacitor voltage will eventually rise to the critical value that triggers the insulation to break down.

Charge Balance Condition or Amp-Sec Balance Condition

The *charge balance condition* states that the net change in the charge accumulation in a capacitor should be balanced at zero for each switching period. As with the case of the flux balance condition, the charge balance condition is a prerequisite to assume steady-state operation for a capacitive switching circuit. Because the incremental charge in a capacitor, Δq, is given by the product of the capacitance C

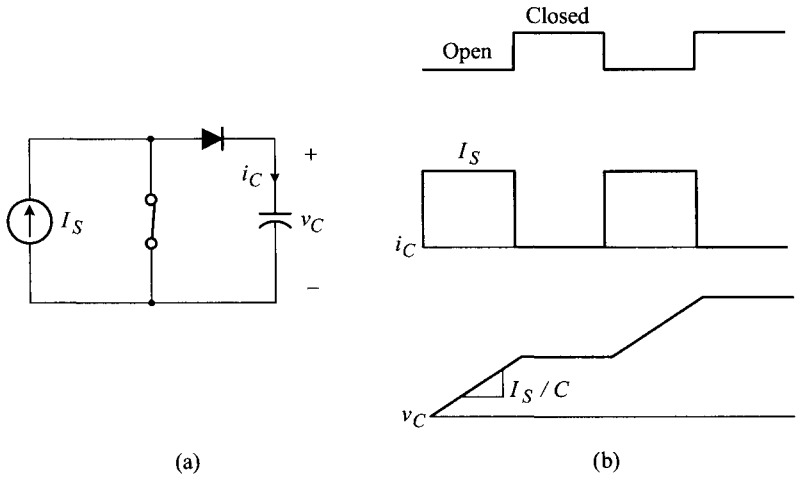

Figure 2.15 Capacitive switching circuit. (a) Circuit diagram. (b) Circuit waveforms.

and incremental capacitor voltage, Δv_C

$$\Delta q = C\Delta v_C \tag{2.22}$$

the violation of the charge balance condition implies that the capacitor voltage will continue to rise in the positive or negative polarity until the capacitor encounters insulation breakdown. Because this is unacceptable to any application circuits, all capacitors should meet the charge balance condition.

The incremental charge over one switching period T_s is given by

$$\Delta q_{T_s} = \bar{i}_C(t)_{T_s} T_s \tag{2.23}$$

where $\bar{i}_C(t)_{T_s}$ represents the averaged capacitor current over one switching period T_s. The charge balance condition asserts that Δq_{T_s} in (2.23) should be zero, thereby indicating that $\bar{i}_C(t)_{T_s}$ is zero as well. Accordingly, the charge balance condition is rephrased as *the average capacitor current should be zero for each switching period.* When a capacitor is excited by a periodic rectangular current shown in Fig. 2.16, the

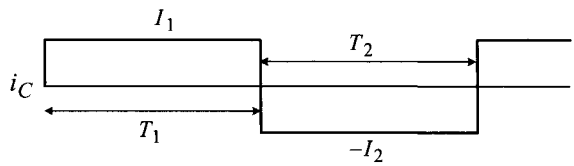

Figure 2.16 Amp-sec balance condition: $I_1T_1 = I_2T_2$.

charge balance condition implies

$$I_1 T_1 = I_2 T_2 \tag{2.24}$$

because the positive current I_1 accumulates the electric charge, whereas the negative current $-I_2$ depletes the electric charge. Equation (2.24) is referred to as the *amp-sec balance condition* as it places a constraint on the product of the magnitude and the period of the capacitor current.

As a generalization of the charge balance condition, the average value of the capacitor current in general can be considered zero. This generalized charge balance condition could simplify the analysis of capacitive switching circuits.

■ EXAMPLE 2.7 Capacitive Switching Circuit

The operation of another capacitive switch circuit is illustrated in this example. Figure 2.17(a) shows a capacitive switching circuit, consisting of two current sources, active switch, diode, and capacitor. As initial conditions, the capacitor is uncharged and the active switch is closed. Under this situation, I_{S1} flows through the active switch while I_{S2} circulates via the diode. For this case, the capacitor current i_C is zero, as shown in Fig. 2.17(a). Now, the circuit begins its operation by opening the active switch.

When the active switch is opened, I_{S1} flows into the capacitor while I_{S2} still runs through the diode, as shown in Fig. 2.17(b). Accordingly, the capacitor voltage increases linearly. When the active switch is closed, the diode is reverse-biased by the elevated capacitor voltage and I_{S2} now flows into the capacitor, *in the opposite direction to* I_{S1}, as shown in Fig. 2.17(c). Now it is assumed that the switch is periodically opened and closed, with an equal time length for the open and closed periods. The following three cases are considered:

- Case 1: $I_{S1} = I_{S2}$
- Case 2: $I_{S1} < I_{S2}$
- Case 3: $I_{S1} > I_{S2}$

The capacitor voltage waveforms, v_C, for these three cases are shown in Fig. 2.17(d). For Case 1, the capacitor voltage v_C becomes a symmetric triangular waveform with the identical rising and falling slopes. For Case 2, the falling slope is steeper than the rising slope. Thus, v_C reduces to zero before the onset of the next operational period. When v_C becomes zero, the diode is turned-on. Under this condition, I_{S2} diverts from the capacitor to the diode and v_C is thus held zero for the remaining operational period.

For Case 3, the rate of the capacitor voltage decreasing is slower than the rate of the capacitor voltage increasing. Accordingly, the capacitor voltage v_C will increase cycle-by-cycle, as illustrated in Fig. 2.17(d). In fact, Case 3 breaks the charge balance condition and the circuit never reaches steady state. It would be informative to sketch the capacitor current waveform i_C, in order

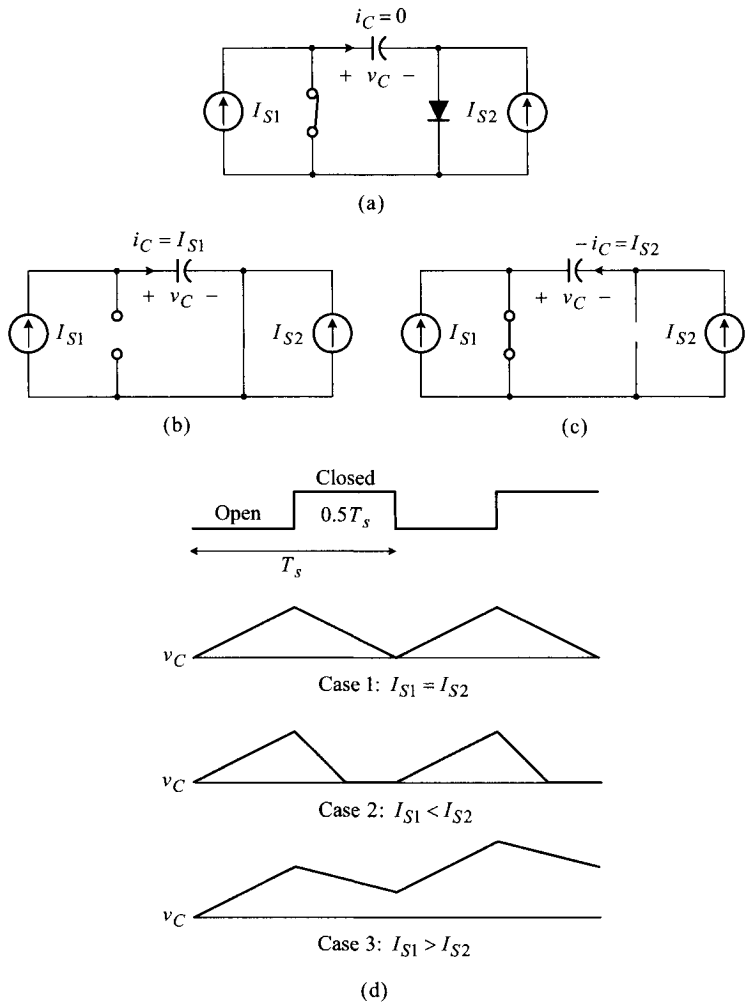

Figure 2.17 Capacitive switching circuit. (a) Circuit diagram. (b) Current flow with switch open. (c) Current flow with switch closed. (d) Capacitor voltage waveforms.

to comprehend how each of the three cases does or does not meet the amp-sec balance condition.

2.2.3 Transformers

Transformers are widely used in dc-to-dc power conversion circuits to change the levels of voltage and current waveforms while transferring electrical energy. Although the electro-magnetic process inside the transformer is rather complicated, the

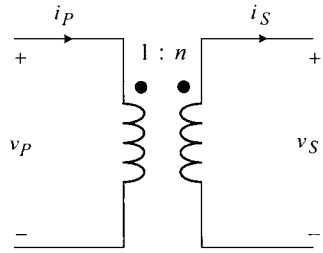

Figure 2.18 Symbol and polarity/direction of voltage/current waveforms of ideal transformer.

external circuit properties can readily be described by a simple circuit model. This section discusses the circuit model for practical transformers and illustrates its use.

First, the concept of the *ideal* transformer is discussed. Then, the electro-magnetic process of practical transformers is described using the equations of the ideal transformer and inductor, leading to the circuit model of practical transformers.

Ideal Transformer

The ideal transformer is a conceptual device that satisfies predefined relationships among its circuit variables. Figure 2.18 shows the symbol and polarity/direction of terminal voltage/current waveforms of an ideal transformer. The following terms are defined for the circuit variables and parameter associated with the ideal transformer:

- $v_P(t)$: primary voltage
- $v_S(t)$: secondary voltage
- n: turns ratio
- $i_P(t)$: primary current
- $i_S(t)$: secondary current

The symbol dot '•' in Fig. 2.18 is involved with the definitions for the polarity/direction of the primary and secondary voltage/current waveforms. In other words, the polarity and direction of the circuit variables are determined in reference to the position of •. Descriptions about • will be given in the next section which deals with non-ideal practical transformers. The turns ratio n is the key parameter that establishes the relationships between the terminal voltage and current waveforms of the ideal transformer

$$v_S(t) = n\, v_P(t) \tag{2.25}$$

$$i_P(t) = n\, i_S(t) \tag{2.26}$$

The ideal transformer is an imaginary device whose terminal circuit variables are always governed by (2.25) and (2.26). For example, if a dc value $v_P = V_1$ is applied as the primary voltage, the secondary voltage is also a dc, given by $v_S = nV_1$. It can be inferred from (2.25) and (2.26) that, when one port of an ideal transformer is short-circuited or open-circuited, the other port becomes the same. Although defined as a conceptual device, the ideal transformer plays a critical role in characterizing the

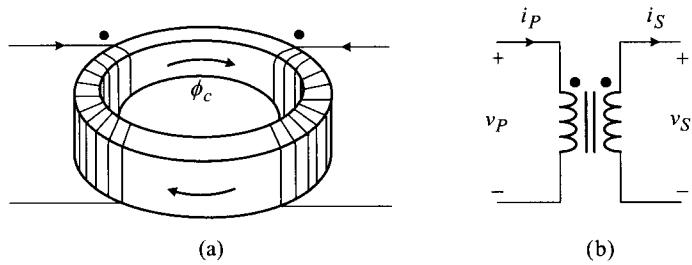

Figure 2.19 Structure, symbol, and polarity of practical transformer. (a) Structure and dot convention. (b) Symbol and polarity of practical transformer.

circuit properties of practical transformers. In fact, the ideal transformer is conceived as a means of describing the circuit properties of non-ideal practical transformers. Now, we start the discussions about practical transformers.

Practical Transformers

Practical transformers are fabricated by wrapping two or more copper windings around a magnetic core. Figure 2.19(a) shows a simplified structure of a two-winding transformer built on a toroidal magnetic core. If one winding is referred to as the primary winding, the other winding becomes the secondary winding. To determine the terminal circuit characteristics of the practical transformer, it is necessary to know *how the primary and secondary windings are wound.* In other words, the polarity/direction of the terminal circuit waveforms depends on the internal pattern of the transformer windings. The following *dot convention* has been used to specify the winding pattern of transformers.

Dot Convention: For both primary and secondary windings, one end of the winding is marked with a *dot* • as a means of indicating the *polarity* of the transformer. The location of • is determined as follows. When the primary current flows into the *dotted* end of the winding and the secondary current also enters the dotted end of the winding, two magnetic fluxes, generated by the two currents running into the respective windings, are directed to be additive, as illustrated in Fig. 2.19(a). Namely, the primary and secondary currents flowing into the winding terminals marked • produce mutually additive magnetic flux. Readers are urged to refer to Fig. 2.19(a) to confirm the dot convention, pattern of the transformer windings, and direction of the magnetic flux, as all illustrated in Fig. 2.19(a).

The operation of the transformer is based on the coupling between the primary winding and the secondary winding via the electro-magnetic induction. According to Lenz's law, the electro-magnetic induction always occurs in such a way that the magnetic flux, produced as the outcome of the induction, opposes the magnetic flux that initiated the induction process. In conjunction with the dot convention,

Lenz's law is reiterated as follows. *When the initiating current enters the dotted end of the primary winding, the induced current should leave from the dotted end of the secondary winding.* The two magnetic fluxes then oppose each other, thereby complying with Lenz's law.

Figure 2.19(b) shows the symbol of a practical transformer together with the polarity/direction of its terminal voltage/current waveforms. The directions of the terminal currents are defined by Lenz's law and dot convention. The polarities of the winding voltages accord with the directions of the winding currents. The polarity/direction of the terminal circuit variables, along with the location of • in Fig. 2.19(b), is consistent with that of the ideal transformer in Fig. 2.18. The vertical bars between the primary and secondary windings signify the presence of a magnetic core in the practical transformer. The vertical bars also symbolically differentiate the practical transformer from the ideal transformer.

The polarity of the transformer can be defined in other way around. In other words, the position of • on each winding can be swapped, along with the reversal of the polarity/direction of voltage/current waveforms associated with each winding. This, of course, does not alter the circuit properties of the transformer.

Circuit Model for Practical Transformers

A circuit model for practical transformers can be created based on Faraday's law, Ampere's law, and properties of the magnetic core. Figure 2.20 shows the circuit configuration that is used in developing a circuit model for the practical transformer. To simplify the model derivation, perfect magnetic coupling is presumed for the practical transformer. In other words, the common magnetic flux, ϕ_c in Fig. 2.20(a), entirely passes through both the primary and secondary windings without any leakage component. According to Faraday's law, the terminal voltage of each winding is given by

$$v_P(t) = \frac{\mathrm{d}\lambda_P(t)}{\mathrm{d}t} = N_P \frac{\mathrm{d}\phi_c(t)}{\mathrm{d}t} \tag{2.27}$$

$$v_S(t) = \frac{\mathrm{d}\lambda_S(t)}{\mathrm{d}t} = N_S \frac{\mathrm{d}\phi_c(t)}{\mathrm{d}t} \tag{2.28}$$

where λ_P and λ_S represent the magnetic flux linkages across the primary and secondary windings due to the common magnetic flux ϕ_c, while N_P and N_S denote the number of the primary and secondary winding turns. From (2.27) and (2.28), the relationship between the terminal voltages is given as

$$v_S(t) = \frac{N_S}{N_P} v_P(t) \tag{2.29}$$

The connection between the terminal currents is formulated by applying Ampere's law along the magnetic path of the transformer

$$N_P i_P(t) - N_S i_S(t) = H_c l_m \tag{2.30}$$

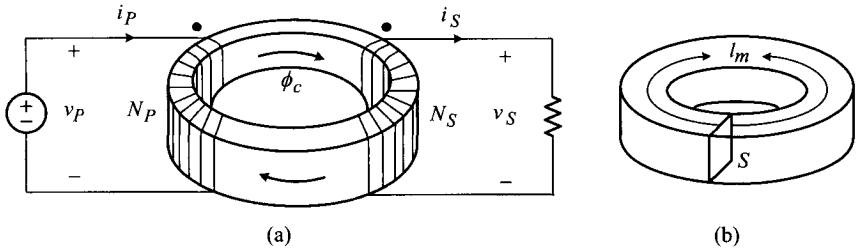

Figure 2.20 Simple circuit using practical transformer. (a) Circuit configuration. (b) Geometry of toroidal core.

where H_c is the magnetic field intensity associated with ϕ_c, and l_m is the length of the magnetic path. Equation (2.30) is rearranged as

$$i_P(t) = \frac{N_S}{N_P} i_S(t) + \frac{H_c l_m}{N_P} \tag{2.31}$$

The last term in (2.31) is referred to as the magnetizing current

$$i_m(t) \equiv \frac{H_c l_m}{N_P} \tag{2.32}$$

The magnetic flux linkage at the primary winding is given by

$$\lambda_P(t) = N_P \phi_c(t) = N_P \mu_r \mu_o H_c S \tag{2.33}$$

with μ_r the relative permeability of the core material, μ_o the permeability of free space, and S the cross-sectional area of the core. The inductance, associated with the magnetizing current of (2.32) and flux linkage of (2.33), is now defined as

$$L_m = \frac{\lambda_P(t)}{i_m(t)} = \frac{N_P \mu_r \mu_o H_c S}{\frac{H_c l_m}{N_P}} = \mu_r \mu_o \frac{S}{l_m} N_P^2 \tag{2.34}$$

This inductance is termed as the magnetizing inductance because it is associated with the magnetizing current. Equation (2.34) indicates that the magnetizing inductance corresponds to the inductance that is evaluated at the primary side of the transformer with the secondary winding removed or unaccounted for, as confirmed by referring to Example 2.1.

The circuit behavior of Fig. 2.20, given by (2.29) and (2.31), can be represented by the circuit model in which the practical transformer is replaced with an ideal transformer plus magnetizing inductance. Figure 2.21 shows such a circuit model, where the turns ratio of the ideal transformer is determined as

$$n = \frac{N_S}{N_P} \tag{2.35}$$

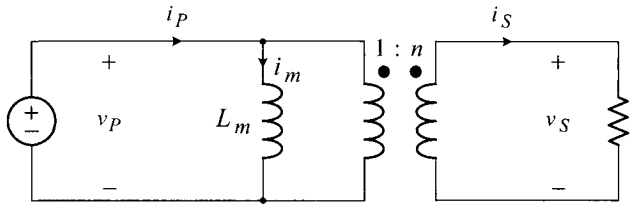

Figure 2.21 Equivalent circuit representation of Fig 2.20.

and the magnetizing inductance L_m is given by (2.34). The validity of Fig. 2.21 is confirmed by showing that the circuit model reproduces the original equations of (2.29) and (2.31). Referring to Fig. 2.21 and the circuit equation of the 1 : n ideal transformer, the relationship between the terminal voltages is given as

$$v_S(t) = nv_P(t) \tag{2.36}$$

and the terminal currents are related as

$$i_P(t) = ni_S(t) + i_m(t) \tag{2.37}$$

The magnetizing current i_m is evaluated as

$$i_m(t) = \frac{\lambda_P(t)}{L_m} = \frac{N_P \mu_r \mu_o H_c S}{\mu_r \mu_o \dfrac{S}{l_m} N_P^2} = \frac{H_c l_m}{N_P} \tag{2.38}$$

Now, the current equation (2.37) becomes

$$i_P(t) = \frac{N_S}{N_P} i_S(t) + \frac{H_c\, l_m}{N_P} \tag{2.39}$$

which is the original current equation of (2.31).

To summarize the model derivation, Fig. 2.22 shows the symbol and circuit model of the practical transformer. The turns ratio of the ideal transformer is given by

$$n = \frac{N_S}{N_P} \tag{2.40}$$

and the magnetizing inductance is determined as

$$L_m = \mu_r \mu_o \frac{S}{l_m} N_P^2 \tag{2.41}$$

The magnetizing inductance represents the *non-ideality* of practical transformers. Thus, it is good engineering practice to maximize the magnetizing inductance while complying with other design constraints. The larger the magnetizing inductance, the closer the practical transformer is to the ideal transformer. The magnetizing

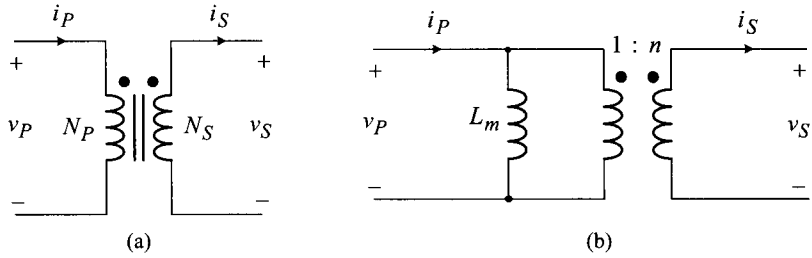

Figure 2.22 Symbol and circuit model for practical transformer. (a) Symbol. (b) Circuit model.

inductance becomes infinitely large when the permeability of the core material is assumed to be infinite. For such a case, the magnetizing inductance disappears and the circuit model reduces to the ideal transformer.

Figure 2.22(b) is the simplest circuit model for practical transformers. The model becomes more complex when the imperfect magnetic coupling, parasitic circuit components, and detailed core properties are incorporated. However, the operations of most dc-to-dc power conversion circuits can duly be described using the transformer model shown in Fig. 2.22(b).

■ EXAMPLE 2.8 Simple Circuit with Practical Transformer

This example illustrates the use of the previous circuit model for practical transformers. Figure 2.23(a) shows a simple circuit in which a practical transformer is connected to a voltage source v_P and current source i_S. The waveforms for the voltage source v_P and current source i_S are shown in Fig. 2.23(a). The transformer is built using a toroidal core with $\mu_r = 5000$, $S = 1$ cm^2, and $l_m = 4\pi\times10^{-1}$ cm. The turns of the primary winding are $N_P = 10$ and that of the secondary winding are $N_S = 20$. Figure 2.23(b) shows the circuit model of Fig. 2.23(a). The magnetizing inductance is evaluated as

$$L_m = \mu_r \mu_o \frac{S}{l_m} N_P^2$$

$$= 5\times10^3\, 4\pi\times10^{-7}\, \frac{10^{-4}}{4\pi\times10^{-3}}\, 10^2 = 5 \text{ mH}$$

and the turns ratio is

$$n = \frac{N_S}{N_P} = \frac{20}{10} = 2$$

The circuit variables are evaluated as

$$v_S(t) = nv_P(t) = 2\, v_P(t) \tag{2.42}$$

and

$$i_P(t) = ni_S(t) + i_m(t) = 2\, i_S(t) + i_m(t) \tag{2.43}$$

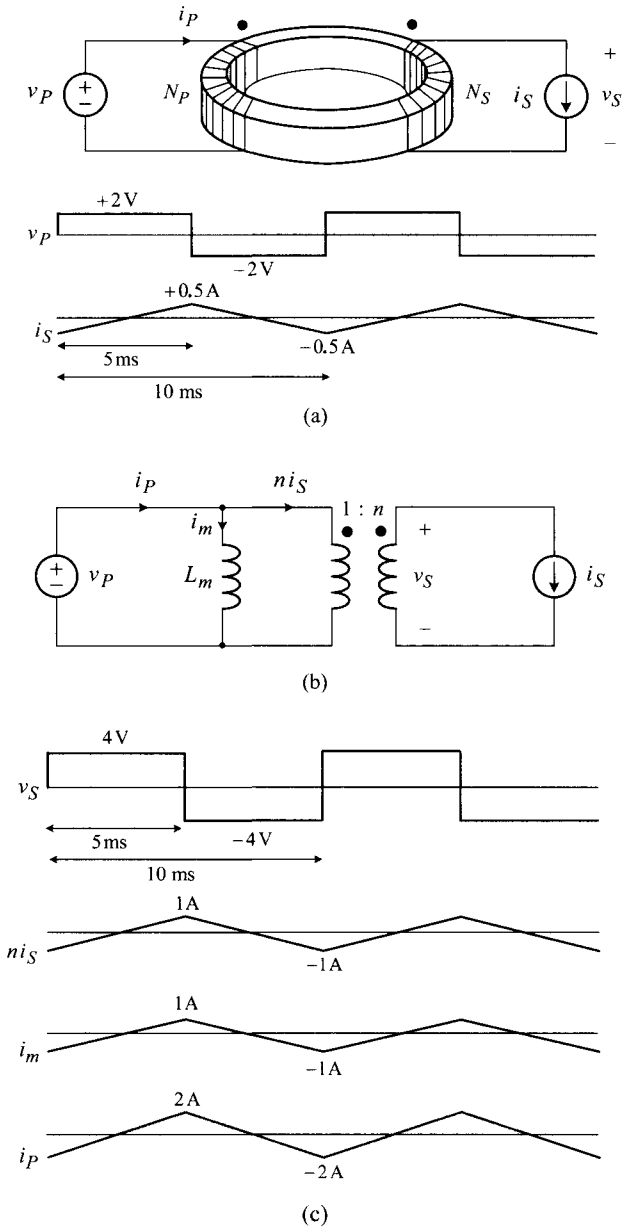

Figure 2.23 Simple transformer circuit. (a) Circuit configuration. (b) Circuit model. (c) Circuit waveforms.

with

$$i_m(t) = \frac{1}{L_m} \int v_P(t)\, dt \tag{2.44}$$

Figure 2.23(c) shows the steps of constructing v_S and i_P, based on the expressions (2.42) through (2.44) along with v_P and i_S waveforms given in Fig. 2.23(a). The average value of i_m is assumed zero in this example.

2.3 SWITCHING CIRCUITS IN PRACTICE

Switching circuits, constructed with the power stage components discussed in this chapter, have been used in many industrial and consumer electronics. In these applications, semiconductor switches and energy storage/transfer elements are appropriately combined to operate as a functional switching circuit. This section presents a couple of such examples.

2.3.1 Solenoid Drive Circuits

An inductor fabricated by winding a copper coil around an iron rod is called a solenoid. The solenoid is often used as an actuator in industrial applications. When a solenoid is connected to a voltage source by turning on a semiconductor switch, a linearly-increasing current is established in the solenoid inductance and energy is thus accumulated inside the solenoid. Although some energy is dissipated during the operation as an actuator, most of the accumulated energy will still remain in the solenoid after operation. The solenoid drive circuit must be designed so that the remnant energy is safely removed from the solenoid inductance without damaging the semiconductor switch. In this section, different solenoid drive circuits are analyzed focusing on their efficiencies. To simplify ensuing discussions, the energy consumed during the actuator operation is assumed negligible and the solenoid is thus represented by a pure inductor.

First, a conceptual solenoid drive circuit is shown in Fig. 2.24. It becomes immediately apparent that this drive circuit is not workable due to the lack of the freewheeling path. When the switch is closed, the inductor current increases linearly, thereby storing energy in the solenoid. When the switch is opened, the inductor current suddenly loses its path and the stored energy is instantaneously released in an uncontrolled manner. This abrupt energy discharge, occurring in the form of a high voltage spike, would destroy the semiconductor switch. This section discusses two different solenoid drive circuits that operate without damaging the semiconductor switch.

Dissipative Solenoid Drive Circuit

Figure 2.25(a) shows the first solenoid drive circuit where a freewheeling path, consisting of a diode and resistor, is employed in parallel with the solenoid. When the switch is opened, the diode conducts to create a freewheeling path for the inductor

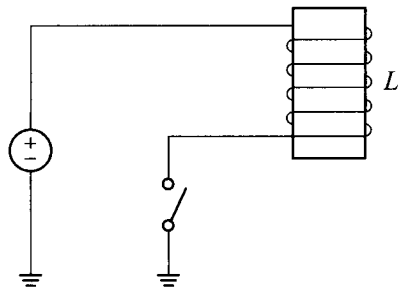

Figure 2.24 Conceptual solenoid drive scheme.

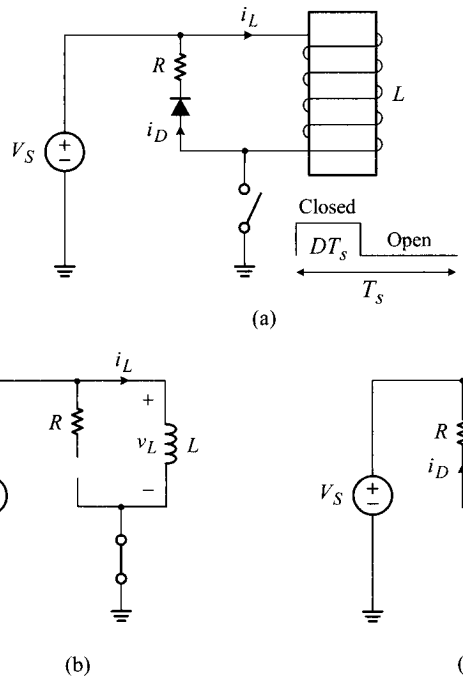

Figure 2.25 Dissipative solenoid drive circuit. (a) Circuit diagram. (b) Energy build-up period. (c) Energy removal period.

current. This prevents the instantaneous energy discharge and protects the switch. Detailed circuit operations are explained below.

Energy Build-up Period: When the switch is closed, the freewheeling diode is turned-off and the circuit is represented by Fig. 2.25(b). The inductor current

increases linearly

$$i_L(t) = \frac{V_S}{L}t \tag{2.45}$$

thereby piling up energy in the solenoid inductance.

Energy Removal Period: When the switch is opened at $t = DT_s$, the diode is turned-on and the freewheeling path is closed. The equivalent circuit in this period is shown in Fig. 2.25(c). The freewheeling current is given by

$$i_D(t) = i_L(t) = i_L(DT_s)\, e^{-t/\tau} \tag{2.46}$$

with $\tau = L/R$. As the freewheeling current circulates through the resistor, the energy stored in the solenoid inductance is gradually dissipated at the resistor. As the freewheeling current reduces to a negligible value, the stored energy is practically all removed by dissipation. Although the solenoid drive circuit functions properly without damaging the switch, efficiency of the drive circuit will be low because the stored energy is dissipated in the resistor. Figure 2.25(a) is referred to as the dissipative solenoid drive circuit.

■ EXAMPLE 2.9 Dissipative Solenoid Drive Circuit

In this example, the operation of the dissipative solenoid drive circuit is illustrated using PSpice® simulations. Figure 2.26(a) is the circuit diagram of a dissipative solenoid drive circuit. Figure 2.26(b) illustrates the major circuit waveforms with $V_S = 90$ V, $L = 180$ mH, $R = 20\,\Omega$, $T_s = 50$ ms, and $D = 0.2$. When the switch is closed, the inductor current grows linearly and reaches the peak value at $t = DT_s = 0.2 \cdot 50 \times 10^{-3}$ s

$$i_{L\,peak} = \frac{V_S}{L}DT_s = \frac{90}{180\times10^{-3}}\,0.2 \cdot 50\times10^{-3} = 5\text{ A}$$

The total energy

$$E_m = \frac{1}{2}L(i_{L\,peak})^2 = \frac{1}{2}180\times10^{-3}\,5^2 = 2.25\text{ J}$$

is stored in the inductor. When the switch is opened, the energy removal period starts and the inductor current i_L freewheels through the loop created by the diode, resistor, and solenoid inductor. The diode current i_D decays exponentially while dissipating the energy at the resistor. When the stored energy is all dissipated in the resistor, i_D converges to zero. The waveforms of the source current i_S and inductor voltage v_L show the operational details of the circuit.

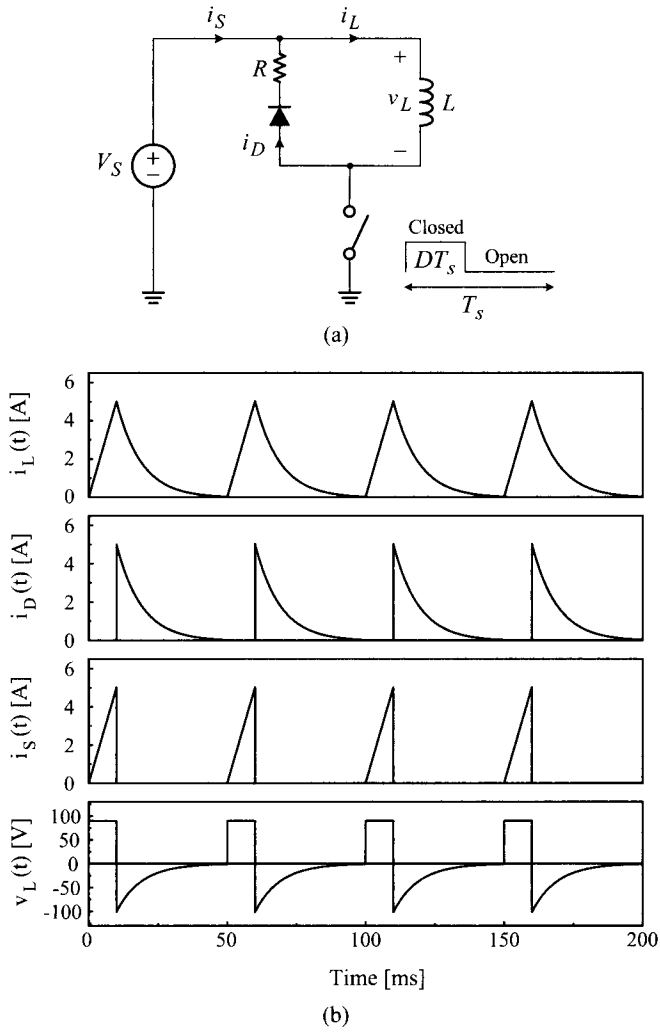

Figure 2.26 Dissipative solenoid drive circuit. (a) Circuit diagram. (b) Circuit waveforms.

Non-Dissipative Solenoid Drive Circuit

Efficiency of the solenoid drive circuit will be improved if the stored energy is recovered by the drive circuit, rather than wasted in the resistor. Figure 2.27(a) shows a non-dissipative solenoid drive circuit. The circuit employs a pair of synchronized switches and two diodes. The synchronized switches are turned-on and off simultaneously, while the two diodes are used to create a freewheeling path for the inductor current. When the synchronized switches are turned-off, the inductor current flows

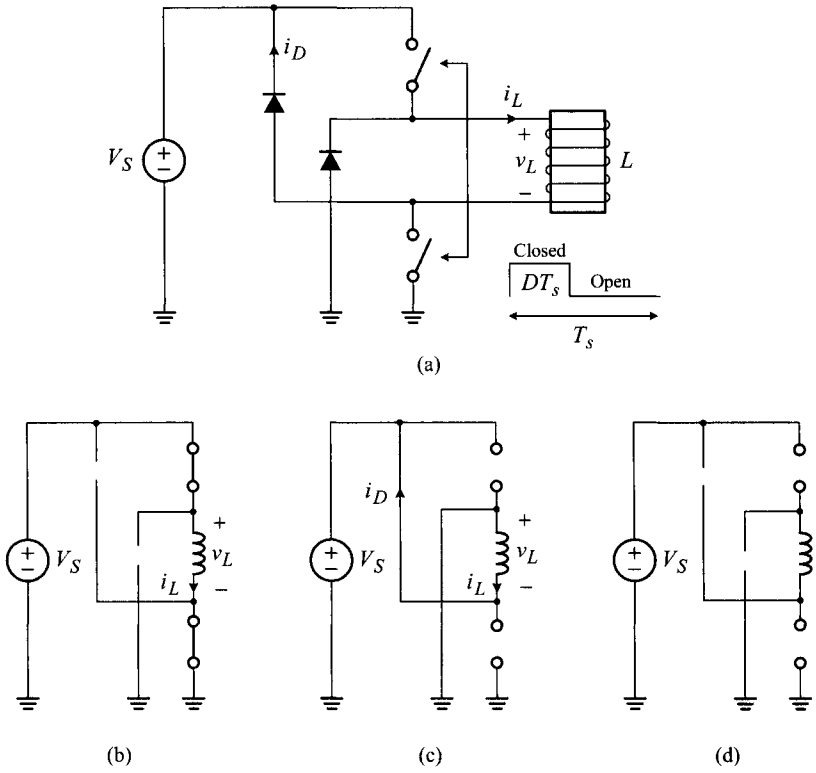

Figure 2.27 Non-dissipative solenoid drive circuit. (a) Circuit diagram. (b) Energy build-up period. (c) Energy recovery period. (d) Recess period.

through the two diodes and the stored energy is transferred back to the voltage source. Operational details of the drive circuit are described below.

Energy Build-up Period: When the synchronized switches are closed, the two diodes are individually reverse-biased by V_S. The equivalent circuit in this period is shown in Fig. 2.27(b). During this period, the solenoid inductor current increases linearly

$$i_L(t) = \frac{V_S}{L}t \tag{2.47}$$

and energy is delivered from the source to solenoid.

Energy Recovery Period: When the switches are opened at $t = DT_s$, the two diodes conduct simultaneously and a freewheeling path is created as shown in Fig. 2.27(c). The solenoid voltage now becomes $-V_S$ and the freewheeling current ramps down from the peak with a slope $-V_S/L$

$$i_D(t) = i_L(t) = i_L(DT_s) - \frac{V_S}{L}t \tag{2.48}$$

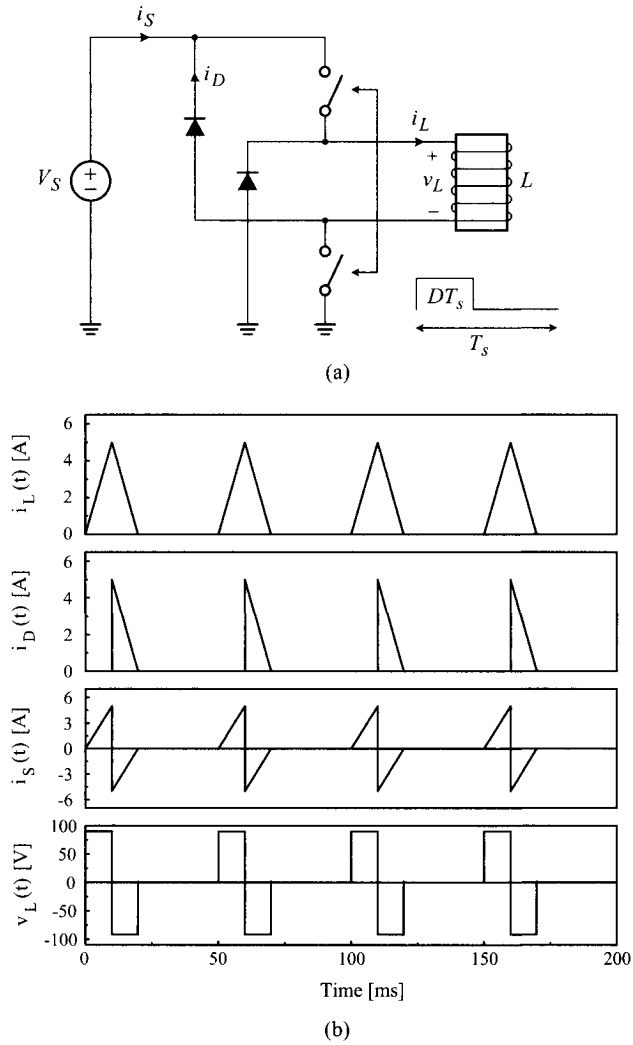

Figure 2.28 Non-dissipative solenoid drive circuit. (a) Circuit diagram. (b) Circuit waveforms.

During this period, the freewheeling current runs into the voltage source and the energy stored in the solenoid is transferred back to the voltage source. The stored energy is thus recovered by the drive circuit, rather than dissipated in the circuit.

Recess Period: When the freewheeling current is reduced to zero, the two diodes are turned-off and remain off thereafter. Because the solenoid is isolated from the source, all the circuit variables are zero, as shown in Fig. 2.27(d).

■ EXAMPLE 2.10 Non-Dissipative Solenoid Drive Circuit

This example illustrates the operation of the non-dissipative solenoid drive circuit. Figure 2.28 shows the circuit diagram and simulated waveforms of a non-dissipative solenoid drive circuit. The operational conditions and circuit parameters are $V_S = 90$ V, $L = 180$ mH, $T_s = 50$ ms, and $D = 0.2$.

Referring to Fig. 2.28(b), the circuit operation is explained as follows. During the energy build-up period, the circuit waveforms are the same as the previous dissipative case. However, during the energy recovery period, the inductor current i_L flows back to the source through the freewheeling diodes, thereby returning the accumulated energy to the source. The source current i_S becomes negative in this period: $i_S = -i_D = -i_L$. The negative current signifies the retrieval of the energy transferred to the solenoid drive circuit during the energy build-up period.

2.3.2 Capacitor Charging Circuit

As the second example of industrial applications, Fig. 2.29(a) shows a switching circuit consisting of a practical transformer, active switch, diode, and capacitor. This circuit is capable of charging the capacitor to a desired voltage level. A simple application will be a high voltage generator which is used in flash lamp driving

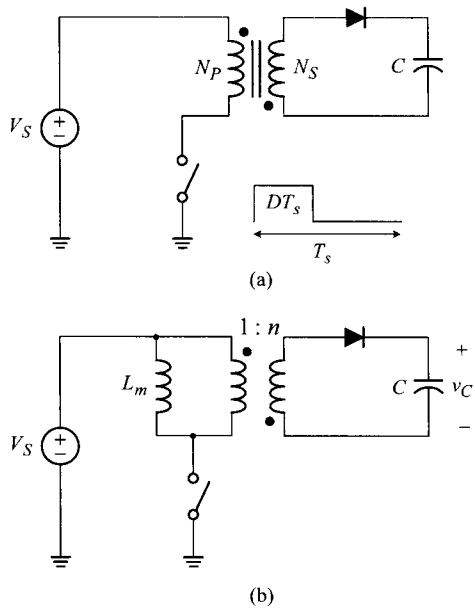

Figure 2.29 Capacitor charging circuit and its circuit model. (a) Capacitor charging circuit. (b) Circuit model: L_m is magnetizing inductance and $n = N_S/N_P$ is turns ratio of transformer.

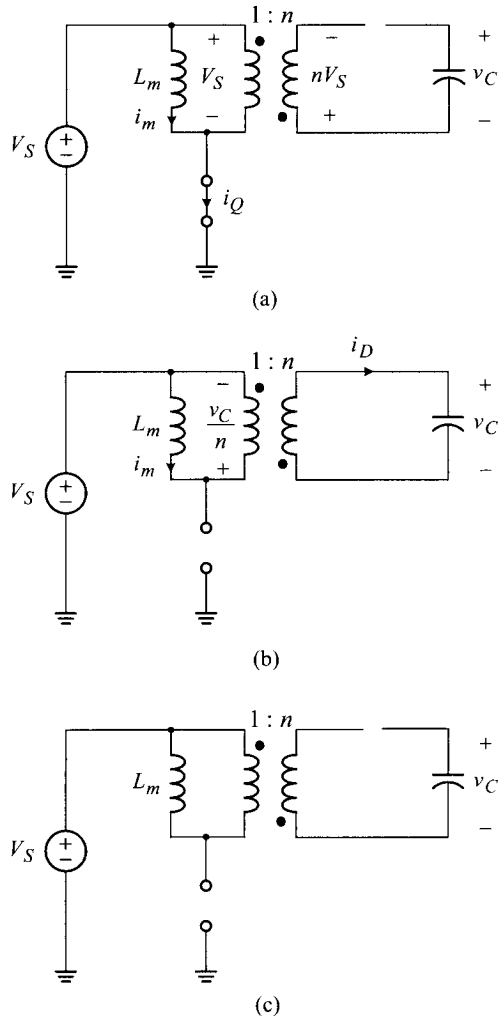

Figure 2.30 Operation of capacitor charging circuit. (a) Energy build-up period. (b) Energy transfer period. (c) Recess period.

circuits for cameras. Figure 2.29(b) shows the circuit model of Fig. 2.29(a), where the practical transformer is replaced with a $1 : n$ ideal transformer and magnetizing inductance L_m. The operation of the capacitor charging circuit is explained using the circuit model in Fig. 2.29(b).

Energy Build-up Period: When the switch is closed, the energy build-up period starts. The circuit model for this period is shown in Fig. 2.30(a). The source voltage V_S is applied across the magnetizing inductance and primary winding

of the ideal transformer. Due to the polarity of the transformer windings, the diode is turned-off by the reverse voltage of $nV_S + v_C$ where v_C is the voltage across the capacitor. A linearly-increasing current flows through the magnetizing inductance and active switch

$$i_m(t) = i_Q(t) = \frac{V_S}{L_m} t \tag{2.49}$$

In this period, the primary winding does not carry any current because the secondary winding is open-circuited. The primary and secondary winding currents are both zero to meet the current equation of the $1 : n$ ideal transformer. With the increasing magnetizing current, energy is piled up in the magnetizing inductance of the transformer.

Energy Transfer Period: When the switch is opened at $t = DT_s$, the energy transfer period begins. As shown in Fig. 2.30(b), the magnetizing current now diverts from the active switch to the primary winding of the ideal transformer, and circulates through the loop formed by the magnetizing inductance and the primary winding. This current in turn forces the diode to conduct, thereby complying with the current equation of the $1 : n$ ideal transformer. Under this situation, the capacitor voltage is reflected to the primary winding and applied across the magnetizing inductance in the negative polarity. The magnetizing current now declines as

$$i_m(t) = -\frac{1}{L_m} \int \frac{1}{n} v_C(t)\, dt \tag{2.50}$$

As the magnetizing current i_m continues to decrease, the accumulated energy is transferred to the capacitor, thereby increasing the capacitor voltage. The diode current is determined by the circuit equation of the $1 : n$ ideal transformer

$$i_D(t) = \frac{1}{n} i_m(t) \tag{2.51}$$

Recess Period: When i_m is reduced to zero, so is the diode current and the accumulated energy is completely transferred to the capacitor. Now, the diode is turned-off and the capacitor voltage is held constant. The circuit model in this recess period is shown in Fig. 2.30(c).

By repeating the above operational cycle, the charge storage in the capacitor will be gradually increased, along with the elevation in the capacitor voltage.

■ EXAMPLE 2.11 Capacitor Charging Circuit

Operational details of the capacitor charging circuit are illustrated in this example. Figure 2.31 shows the circuit diagram and simulated waveforms of a capacitor charging circuit with $V_S = 24$ V, $L_m = 120\,\mu$H, $C = 5\,\mu$F, $n = 1$, $T_s = 100\,\mu$s, and $D = 0.4$.

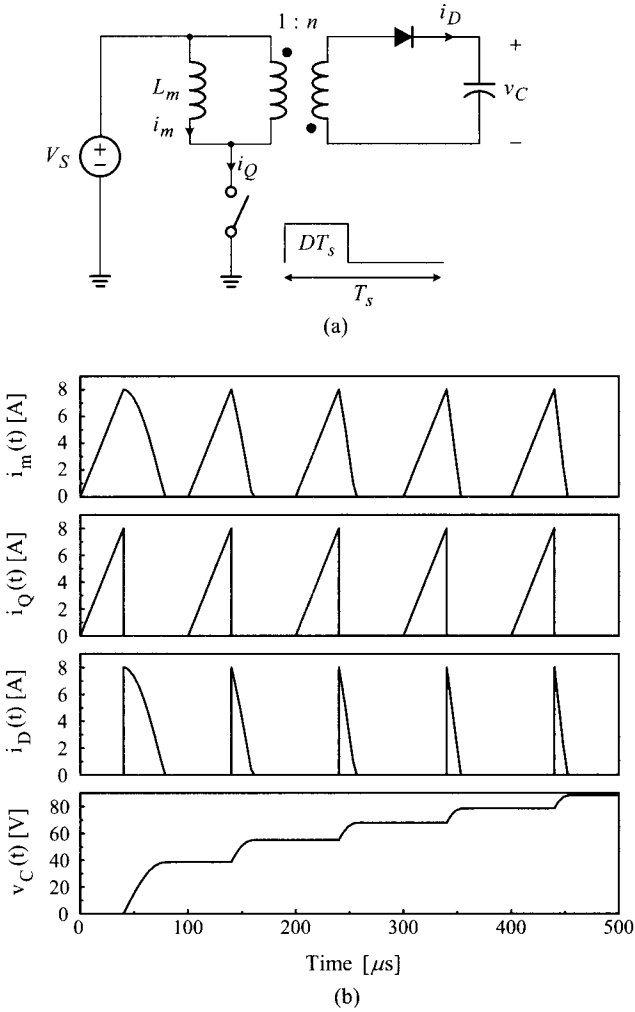

Figure 2.31 Capacitor charging circuit. (a) Circuit diagram. (b) Circuit waveforms.

Referring to Fig. 2.31(b), the circuit operation is explained as follows. The magnetizing current i_m, which is identical to the switch current i_Q during the energy build-up period, increases up to the peak value

$$i_{m\,peak} = \frac{V_S}{L_m} DT_s = \frac{24}{120\times10^{-6}} 0.4 \cdot 100\times10^{-6} = 8 \text{ A}$$

thereby accumulating the total energy

$$E_m = \frac{1}{2} L_m (i_{m\,peak})^2 = \frac{1}{2} 120 \times 10^{-6}\, 8^2 = 3.84 \text{ mJ} \tag{2.52}$$

in the transformer. This energy is delivered to the capacitor by the diode current during the energy transfer period. Thus, E_m represents the amount of the energy transfer from the voltage source to capacitor during one operational period. The capacitor voltage v_C continues to increase in the period when the diode current i_D exists. When i_D reduces to zero, the recess period starts and v_C is held constant until the next energy transfer period.

Figure 2.31(b) reveals important details of the circuit operation. First, although the magnetizing current i_m increases linearly during the energy build-up period, it decays in a nonlinear fashion in the energy transfer period. The voltage across the magnetizing inductance is a constant V_S during the energy build-up period. However, in the energy transfer period, the time-varying capacitor voltage is reflected by the ideal transformer and applied to the magnetizing inductor in the negative polarity. Accordingly, the magnetizing current declines in a nonlinear manner.

Second, the duration of the energy transfer period successively diminishes as the operational cycle proceeds. The decaying slope of the magnetizing current is proportional to the magnitude of the capacitor voltage, which increases cycle-by-cycle. Consequently, the rate of the energy transfer becomes progressively faster, resulting in a continuous reduction in the energy transfer period.

Finally, the incremental growth in the capacitor voltage becomes smaller as the operational cycle proceeds. For each operational period, a fixed amount of energy is transferred to the capacitor, resulting in the cycle-by-cycle growth in the capacitor voltage. Since the energy stored in the capacitor is a quadratic function of the capacitor voltage, the increase in the capacitor voltage becomes smaller in proportion to the initial voltage at each operational cycle.

The capacitor voltage at the end of the kth operational period, $v_C(kT_s)$, is found from the energy balance relationship

$$k\,E_m = \frac{1}{2}C\left(v_C(kT_s)\right)^2 \Rightarrow v_C(kT_s) = \sqrt{\frac{2E_m}{C}k} \tag{2.53}$$

For example, the capacitor voltage at the end of the 5th operational period is given by

$$v_C(5\,T_s) = v_C(500\,\mu s) = \sqrt{\frac{2\cdot 3.84\times 10^{-3}}{5\times 10^{-6}}5} = 87.6\ \text{V}$$

Figure 2.32 shows the capacitor voltage v_C for a longer time period. The time interval required to charge the capacitor at a fixed V_C is determined as follows. First, the required number of the charing operation, k, is found from

$$\frac{1}{2}CV_C^2 = kE_m \quad \Rightarrow \quad k = \frac{1}{2}CV_C^2\frac{1}{E_m} \tag{2.54}$$

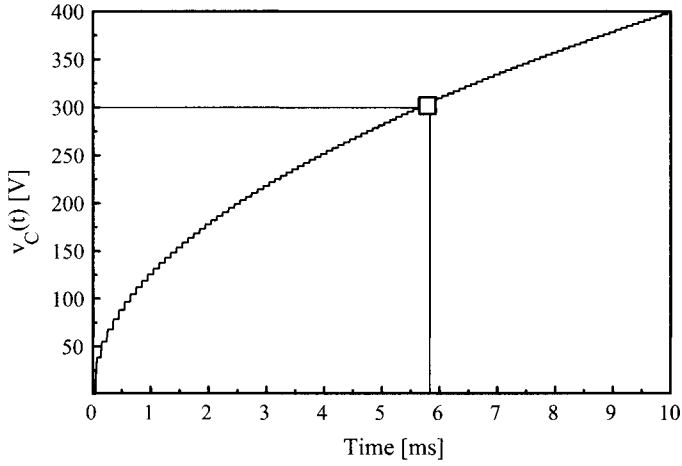

Figure 2.32 Capacitor voltage waveform.

where E_m given by (2.52). Now the total time required for charging V_C is given by

$$T_{charge} = kT_s = \underbrace{\frac{1}{2}CV_C^2\frac{1}{E_m}}_{k} T_s \tag{2.55}$$

where T_s is the switching period. As an example, the time needed to charge $V_C = 300$ V is given by

$$\begin{aligned} T_{charge} &= \frac{1}{2}CV_C^2\frac{1}{E_m}T_s \\ &= \frac{1}{2}5\times10^{-6}\,300^2\frac{1}{3.84\times10^{-3}}100\times10^{-6} \\ &= 5.86 \text{ ms} \end{aligned}$$

Figure 2.32 shows close agreement with the analytical prediction.

2.4 SUMMARY

This chapter investigated the circuit behavior of power stage circuit components. Operations of semiconductor switches, inductors, capacitors, and transformers were presented using several examples. One critical functional component in dc-to-dc power conversion circuits is the single-pole double-throw (SPDT) switch. In all the switching circuits covered in this chapter and other dc-to-dc conversion circuits to be studied in later chapters, the SPDT switch is implemented using the MOSFET-diode

pair. In particular, in the capacitor charging circuit in Section 2.3.2, the MOSFET and diode collectively function as an SPDT switch even though they are physically separated by the transformer.

The energy storage and transfer devices include inductors, capacitors, and transformers. The freewheeling path and flux balance condition are critical to understanding operations of inductive switching circuits. For capacitive switching circuits, the charge balance condition can be used to analyze the circuit waveforms. The practical transformer is modeled as a combination of the ideal transformer and magnetizing inductance. The operation of the practical transformer is then analyzed using the circuit equations of the ideal transformer and inductor.

This chapter analyzed two practical switching circuits — the solenoid drive circuit and capacitor charging circuit. Computer simulations are given to illustrate the operations of the switching circuits. PSpice® codes for these simulations are available at http://booksupport.wiley.com, along with those of other forthcoming simulation examples.

REFERENCES

1. R. D. Middlebrook and S. Ćuk, *Advances in Switch-Mode Power Conversion*, TESLAco, Pasadena, CA, 1983.
2. R. S. Ramshaw, *Power Electronics Semiconductor Switches*, Chapman & Hall, London, 1993.
3. J. K. Watson, *Application of Magnetism*, Gainsville, FL, 1995.
4. D. W. Hart, *Power Electronics*, McGraw-Hill, New York, NY, 2011.

PROBLEMS

2.1* Assume that the inductor and capacitor in Fig. P2.1 are initially unenergized.

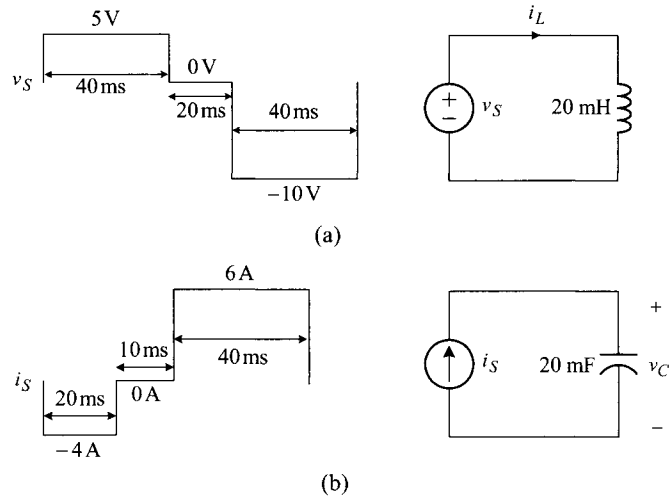

Fig. P2.1

a) For Circuit (a), sketch the inductor current i_L for $0 < t < 100$ ms.

b) For Circuit (b), sketch the capacitor voltage v_C for $0 < t < 70$ ms.

2.2* Figure P2.2 shows four different switching circuits along with their respective inductor voltage or capacitor current waveform.

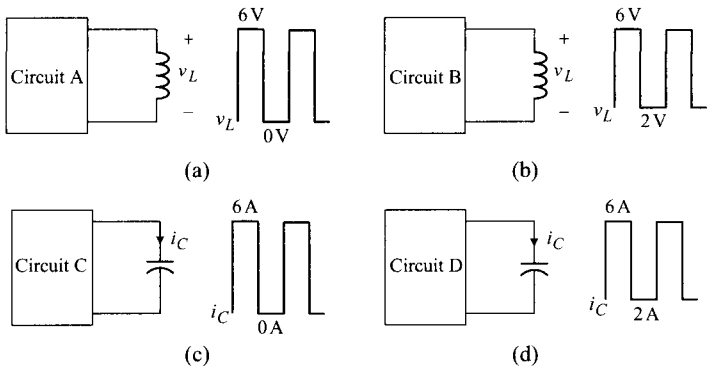

Fig. P2.2

a) Construct Circuit (a) using a 4 V voltage source, 2 V voltage source, MOSFET switch, and diode so that the circuit generates the given inductor voltage waveform v_L.

b) Build Circuit (b) using the same circuit components as those of **a)** so that the circuit produces the given inductor voltage waveform v_L.

c) Construct Circuit (c) using a 4 A current source, 2 A current source, MOSFET switch, and diode so that the circuit generates the given capacitor current waveform i_C.

d) Build Circuit (d) using the same circuit components as those of **c)** so that the circuit produces the given capacitor current waveform i_C.

2.3 Consider the circuit in Fig. P2.3(a) and answer the questions.

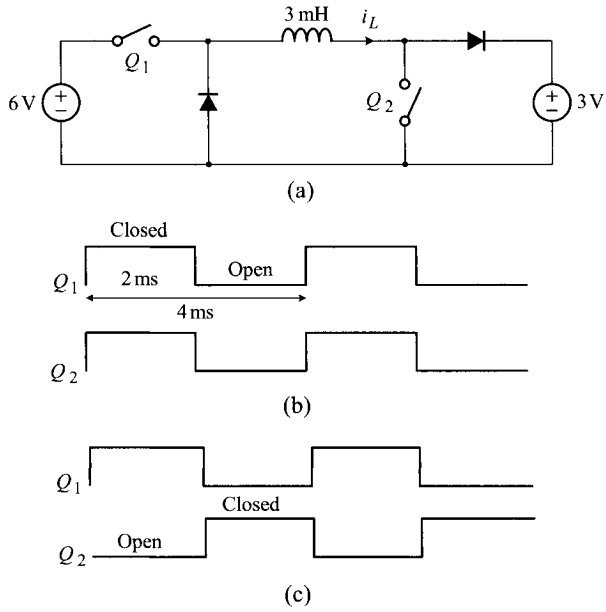

Fig. P2.3

a) Referring to the switch drive signals shown in Fig. P2.3(b), sketch i_L for the first two operational periods. Assume $i_L(0) = 0$.

b) Repeat **a)** for the switch drive signals in Fig. P2.3(c).

2.4* Figure P2.4 shows a switching circuit, along with the switch drive signal and i_L–λ curve of the inductor L.

a) Find the inductance of L.

b) Assume $V_X = 16$ V and sketch i_L for the first three operational periods. Show the peak value of i_L.

c) Find the time instant at which the inductor would saturate.

d) Find the minimum value for the V_X that avoids the inductor saturation.

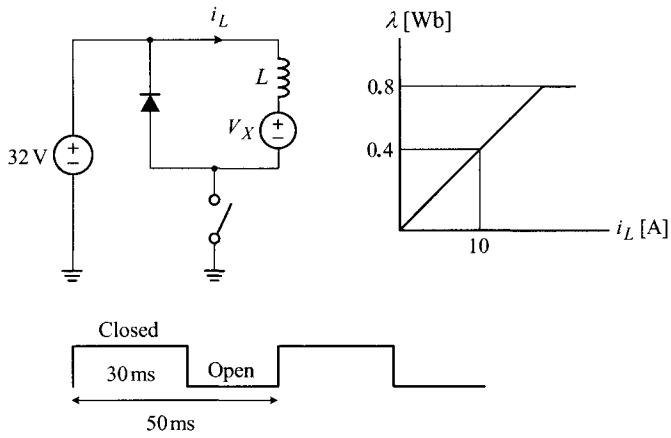

Fig. P2.4

2.5 In the circuits shown in Fig. P2.5, the SPDT switch holds position **x** for DT_s and position **y** for $(1 - D)T_s$.

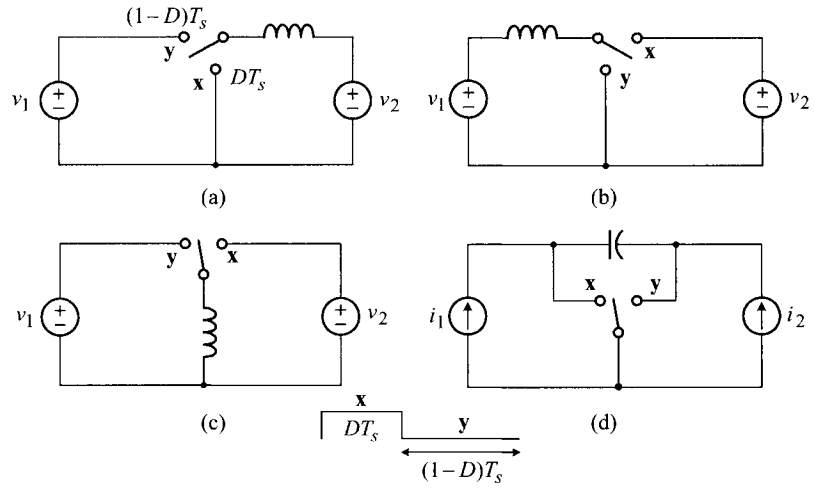

Fig. P2.5

a) For Circuits (a), (b), and (c), find the expression of v_2/v_1.

b) For Circuit (d), find the relationship of i_2/i_1.

2.6* Consider the circuits shown in Fig. P2.6 and answer the questions.

a) For Circuit (a), assume that the inductor is initially unenergized. Sketch the i_L waveform for the first two operational periods for the following two cases. Show the maximum and minimum values of i_L.

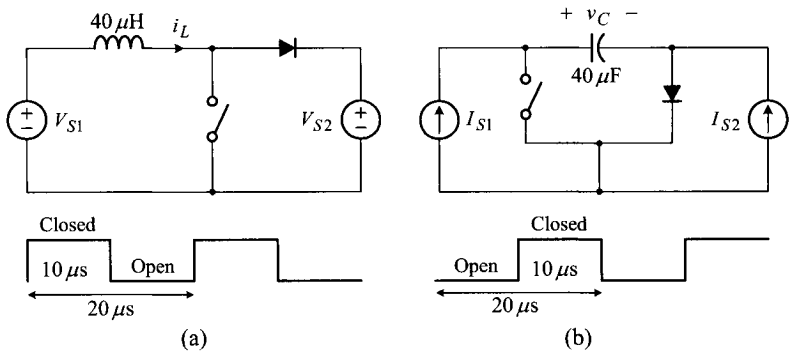

Fig. P2.6

i) $V_{S1} = 4$ V and $V_{S2} = 6$ V
ii) $V_{S1} = 2$ V and $V_{S2} = 6$ V

b) Assume that the capacitor is initially uncharged in Circuit (b). Draw the v_C waveform for the first two operational periods for the following two cases. Show the maximum and minimum values of v_C.
i) $I_{S1} = 4$ A and $I_{S2} = 2$ A
ii) $I_{S1} = 2$ A and $I_{S2} = 4$ A

2.7 Assume that all components are ideal in the circuits shown in Fig. P2.7.

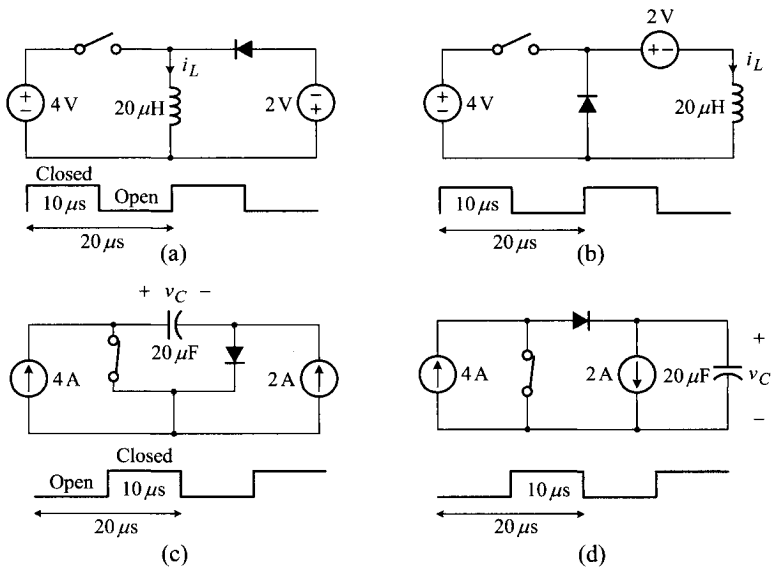

Fig. P2.7

a) For Circuits (a) and (b), sketch the i_L waveform for the first two switching periods. Assume that the inductor is initially unenergized. Show the maximum and minimum values of i_L.

b) For Circuits (c) and (d), draw the v_C waveform for the first two switching periods. Assume the capacitor is initially uncharged. Show the maximum and minimum values of v_C.

2.8* In the four switching circuits shown in Fig. P2.8, the SPDT switch holds position **a** for DT_s and position **p** for $(1-D)T_s$. Answer the following questions.

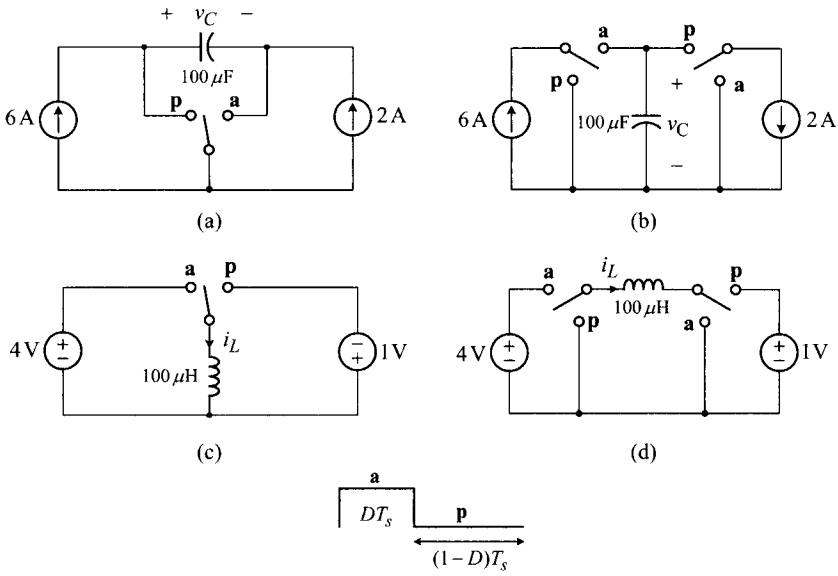

Fig. P2.8

a) For Circuits (a) and (b), determine the values for D and T_s so that each circuit settles in a steady-state operation with a 1.8 V peak value of the capacitor voltage, $v_{C\,peak} = 1.8$ V. Assume the capacitor is initially uncharged.

b) For Circuits (c) and (d), determine the values for D and T_s so that each circuit establishes a steady-state operation with $i_{L\,peak} = 1.2$ A. The inductor is initially unenergized.

2.9** A switching circuit shown in Fig. P2.9 is configured using an SPDT switch and other circuit components. The SPDT switch periodically changes its position, as illustrated in Fig. P2.9. Assume the average value of i_{L2} is 2 A and answer the questions.

a) Use the flux balance condition on L_1 to evaluate the average value of v_C.

b) Apply the flux balance condition to L_2 to find the value for V_2.

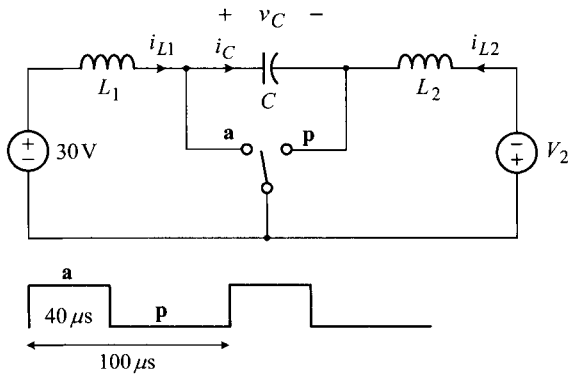

Fig. P2.9

c) Use the charge balance condition on C to evaluate the average value of i_{L1}. The average value of i_{L2} is 2 A.

d) Assume $L_1 = 4.8$ mH, $L_2 = 1.2$ mH, and $C = 120\ \mu$F. Sketch i_{L1}, i_{L2}, i_C, and v_C for the two operational periods. Show the maximum and minimum values of each waveform.

2.10* The switching circuit shown in Fig. P2.10 is fabricated using an SPDT switch and other circuit components. The SPDT switch periodically changes its structure as illustrated in Fig. P2.10.

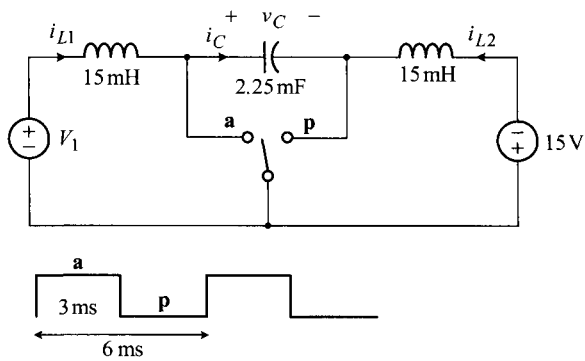

Fig. P2.10

a) Evaluate the average value of v_C and find the value of the dc source V_1.

b) Assume that the average value of i_{L1} is zero. Evaluate the average value of i_{L2}.

c) Using the results of **a)-b)**, sketch i_{L1}, i_{L2}, i_C, and v_C for the two operational periods. Show the maximum and minimum values of each waveform.

2.11** The common switch drive signal is applied to four switching circuits shown in Fig. P2.11. For each circuit, sketch i_S, v_T, and i_{D2} for the two operational periods.

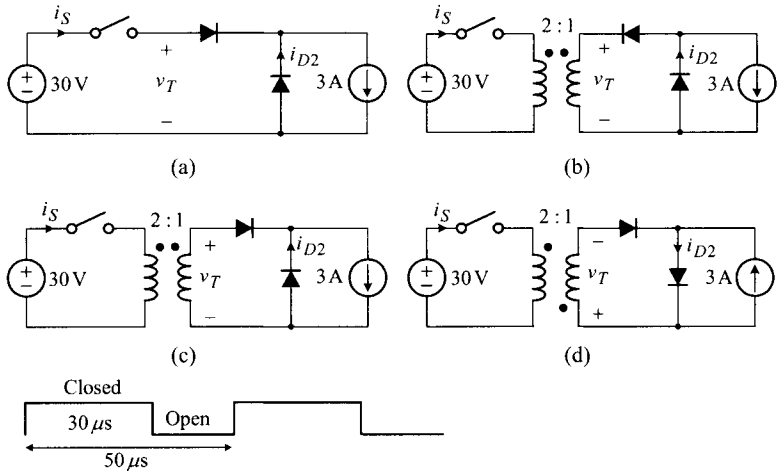

Fig. P2.11

2.12 Find the expressions for the current and voltage waveforms labeled in the two circuits shown in Fig. P2.12.

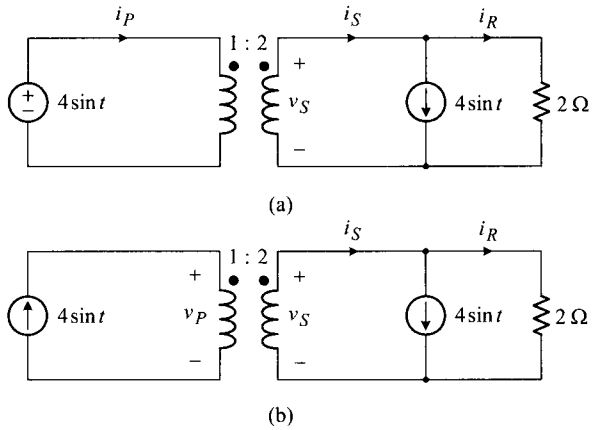

Fig. P2.12

2.13* A transformer is built using a toroidal core with $\mu_r = 5000$, $S = 2\ \text{cm}^2$, and $l_m = 4\pi \times 10^{-1}$ cm. The turns of the primary winding are 200 and the turns of the secondary winding are 400.

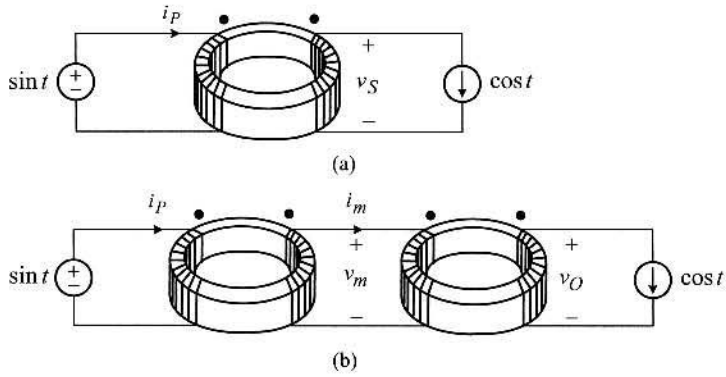

Fig. P2.13

a) A simple circuit shown in Fig. P2.13(a) is constructed using the transformer discussed above. Find the expressions for i_P and v_S.

b) Now assume that the circuit is modified as shown in Fig. P2.13(b) in which the two identical transformers, each constructed as described above, are used. Find the expressions for i_P, i_m, v_m, and v_O.

2.14* An inductor is built using a toroidal core with $\mu_r = 5000$, $S = 2$ cm^2, and $l_m = 4\pi \times 10^{-1}$ cm.

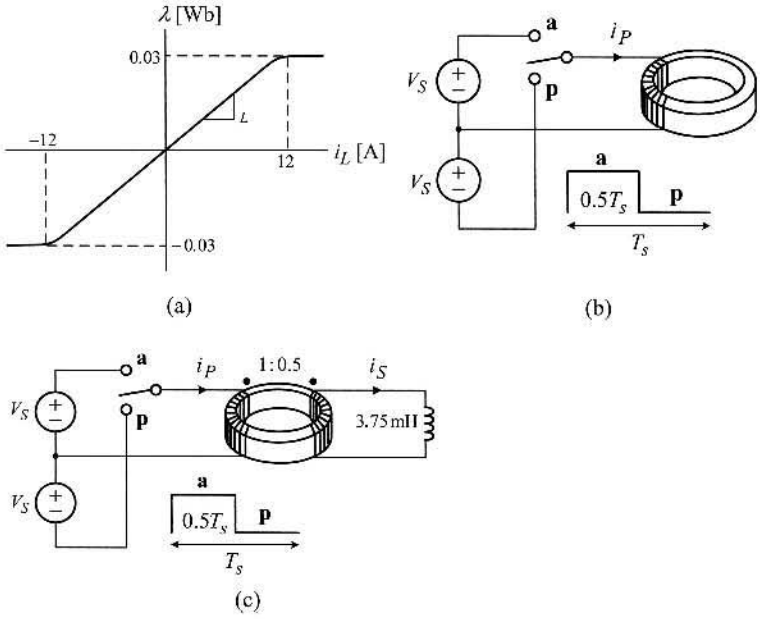

Fig. P2.14

a) Figure P2.14(a) shows the i_L–λ curve of the inductor.
i) Evaluate the inductance of the inductor.
ii) Find the number of the turns of the inductor winding.

b) A switching circuit shown in Fig. P2.14(b) is constructed using the inductor discussed above. In the following problems, the average value of i_P is zero: $\bar{i}_P(t) = 0$.
i) Assume T_s = 1 ms and find the maximum value of V_S for proper operation of the circuit.
ii) Now assume V_S = 30 V and find the maximum value for T_s.
iii) For the case with T_s = 1 ms and V_S = 30 V, sketch i_P for the two operational periods. Show the maximum and minimum values of the waveform.

c) A secondary winding is added to the inductor discussed above, thereby yielding a two-winding transformer with the turns ratio of 1 : 0.5. As shown in Fig. P2.14(c), a 3.75 mH inductor is terminated across the secondary winding of the transformer. For the case with T_s = 1 ms, V_S = 30 V, and $\bar{i}_P(t) = 0$, sketch i_S and i_P for the two operational periods. Show the maximum and minimum values of the waveforms.

2.15 A transformer is fabricated using a toroidal core with $\mu_r = 5000$, $S = 2\ \text{cm}^2$, and $l_m = 4\pi \times 10^{-1}$ cm. The turns of the primary winding are 10 and the turns of the secondary winding are 30.

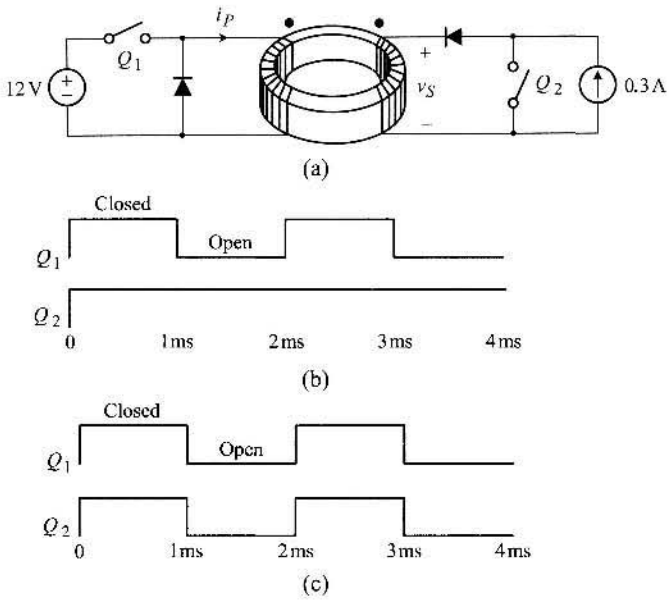

Fig. P2.15

a) Evaluate the magnetizing inductance of the transformer.

b) Draw a circuit model of the transformer.

c) A simple circuit shown in Fig. P2.15(a) is constructed using the transformer discussed above.

i) For the switch drive signals shown in Fig. 2.15(b), sketch i_P and v_S for $0 < t < 4$ ms. Assume the transformer does not saturate for this operation. Show the maximum and minimum values of the waveforms.

ii) Repeat **i)** for the switch drive signals shown in Fig. P2.15(c).

2.16 Consider the switching circuit shown in Fig. P2.16. Referring to the switch drive signals, answer the questions.

a) Assume $D = 0.5$ for the switch drive signal and find the average values of v_C and i_L.

b) Repeat **a)** for $D = 0.25$.

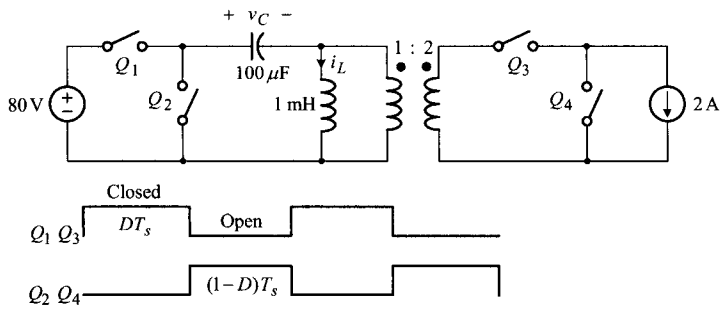

Fig. P2.16

2.17* Figure P2.17 shows a conceptual circuit configured with two inductors and one ideal transformer. The following experiments are performed to determine the values of the inductances and the turns ratio of the ideal transformer.

- A 2 mH inductance is measured at the terminal x–x′ with the terminal y–y′ short-circuited.
- A 7 mH inductance is measured at the terminal x–x′ with the terminal y–y′ open-circuited.
- When a voltage source $v_S(t) = \sin t$ is applied across the terminal x–x′, the same voltage $v_O(t) = \sin t$ is measured across the terminal y–y′.

a) Find the values for the inductances, L_1 and L_2, and the turns ratio n of the ideal transformer.

b) Find the expression for i'_p when a voltage source $v_S(t) = \sin t$ is connected across the x–x′ terminal and the y–y′ terminal is shorted.

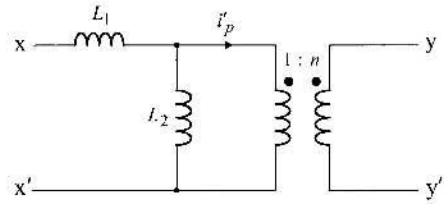

Fig. P2.17

2.18** A couple of experiments are performed to extract the circuit parameters of a practical transformer.

- A 0.5 H inductance is measured at the primary winding with the secondary winding open-circuited.
- When $v_S(t) = 20 \sin t$ is connected to the primary winding, $v_O(t) = 5 \sin t$ is measured at the open-circuited secondary winding.

a) Draw the circuit model for the transformer. Show all the circuit parameters in your model.

b) Five different circuits in Fig. P2.18 are configured using the transformer discussed above. For each circuit, find an expression for the primary winding current, i_P.

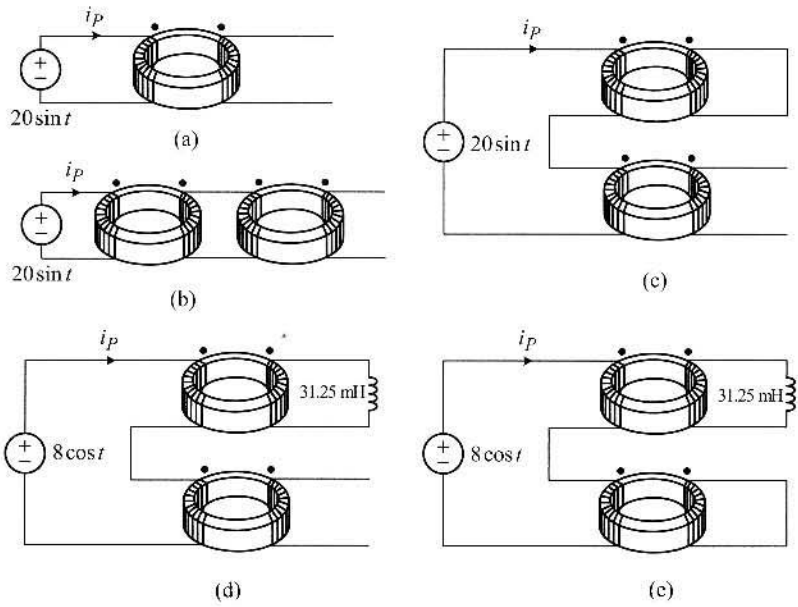

Fig. P2.18

2.19* Referring to the two circuits shown in Fig. P2.19, answer the following questions. The transformer is built using a toroidal core with $\mu_r = 5000$, $S = 2\,\text{cm}^2$, and $l_m = 4\pi \times 10^{-1}$ cm. The turns of the primary winding are 10 and the turns of the secondary winding are 20.

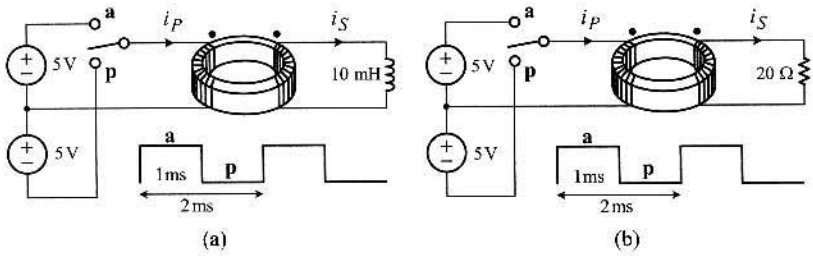

Fig. P2.19

a) For Circuit (a), sketch the steady-state waveforms of i_P and i_S for the two switching periods. Show the maximum and minimum values of each waveform. Assume that the average values of i_P and i_S are zero.

b) Repeat **a)** for Circuit (b).

2.20* Consider a solenoid drive circuit shown in Fig. P2.20 and answer the questions.

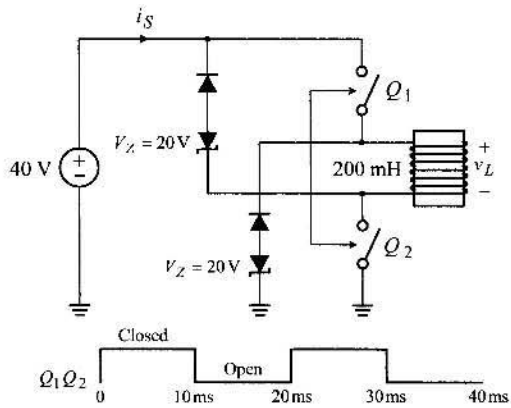

Fig. P2.20

a) Sketch the waveforms of i_S and v_L for $0 < t < 40$ ms. Show the maximum and minimum values on your sketch.

b) Calculate the following items evaluated during $0 < t < 20$ ms:
i) the energy transferred from the source to the solenoid drive circuit,
ii) the energy returned from the solenoid drive circuit to the source, and
iii) the energy dissipated in the solenoid drive circuit.

2.21** Figure P2.21 shows two solenoid drive circuits, along with their switch drive signal and inductor current waveform.

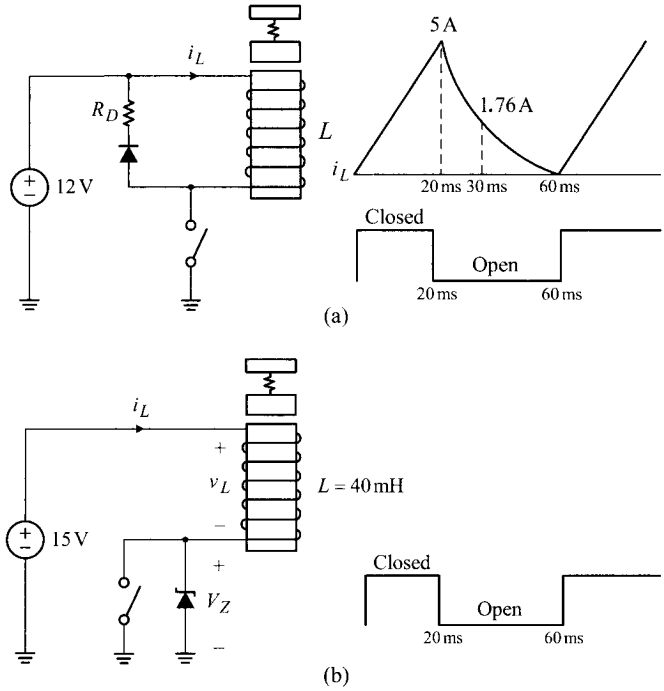

Fig. P2.21

a) Referring to Fig. P2.21(a), find the inductance L of the solenoid and the resistance of R_D.

b) Use the results of **a)** to calculate
i) the peak energy stored in the solenoid,
ii) the energy consumed at the resistor in each switching period, and
iii) the average power supplied by the source.

c) An alternative solenoid drive circuit is configured as shown in Fig. P2.21(b). Referring to the solenoid drive circuit in Fig. P2.21(b), answer the questions.
i) Assuming $V_Z = 25$ V for the Zener diode, sketch i_L and v_L for the two operational periods. Label for the maximum and minimum values of each waveform.
ii) Assuming $V_Z = 20$ V for the Zener diode, sketch i_L for the two operational periods. Show the maximum value and the final value of i_L. Do you think this circuit is workable? Justify your answer.

2.22 Shown in Fig. P2.22 is a solenoid drive circuit along with its switch drive signal. Assume that the inductor is initially unenergized.

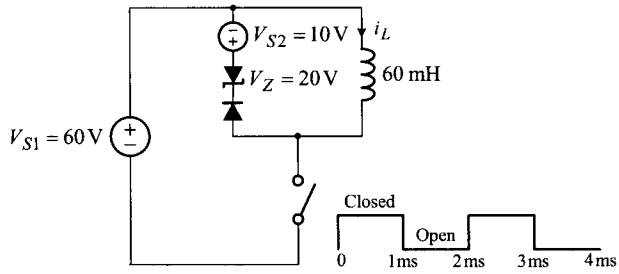

Fig. P2.22

a) Sketch i_L for $0 < t < 4$ ms. Show the maximum value on your sketch.
b) Calculate the energy extracted from the voltage source V_{S1} during $0 < t <$ 1 ms.
c) Calculate the energy stored in the inductor at $t = 2$ ms.
d) Calculate the energy consumed at the Zener diode during $1 < t < 2$ ms.
e) Calculate the energy transferred to V_{S2} during $1 < t < 2$ ms.

2.23 The non-dissipative solenoid drive circuit discussed in Section 2.3.1 is modified as shown in Fig. P2.23. Referring to the switch drive signal, sketch i_L, i_{D1}, i_{D2}, i_{Q1}, and v_X for $0 < t < 6$ ms. Label the maximum and minimum values of each waveform.

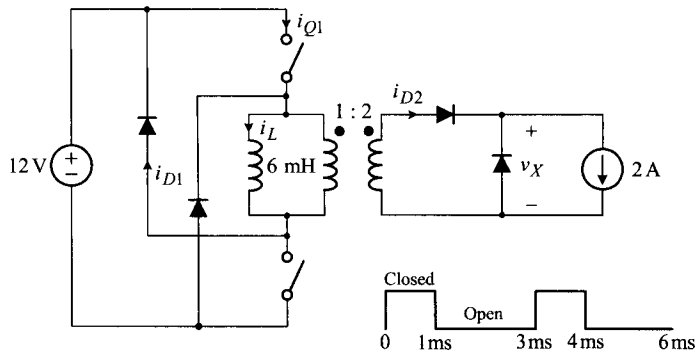

Fig. P2.23

2.24* Consider the capacitor charging circuit and its major circuit waveforms shown in Fig. P2.24(a).

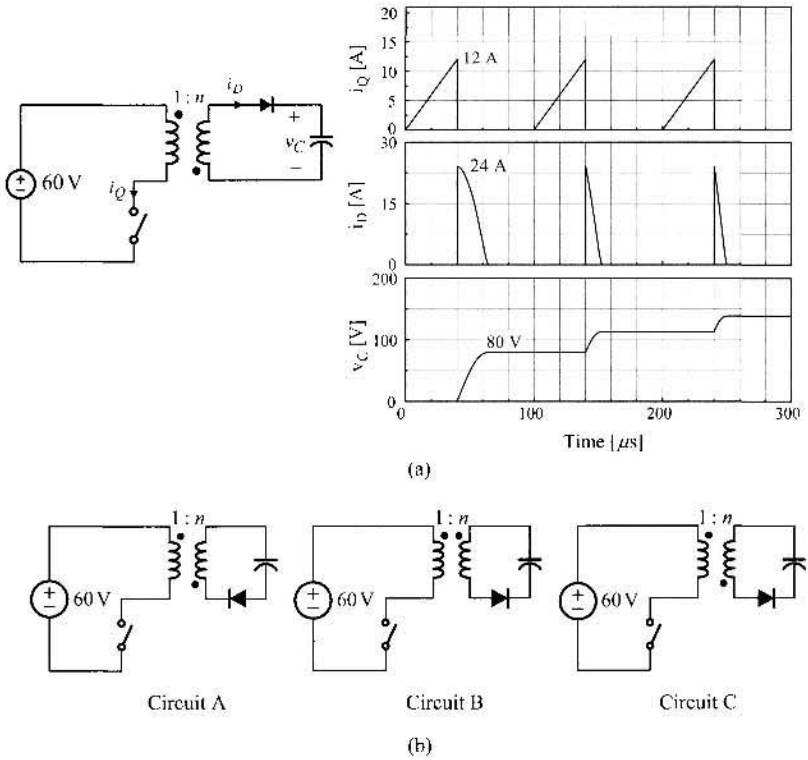

Fig. P2.24

a) Referring to the circuit waveforms, calculate the following circuit parameters and operational conditions of the solenoid driving circuit:
i) L_m: magnetizing inductance of the transformer,
ii) n: turns ratio of the transformer,
iii) D: duty ratio of the switch, and
iv) C: capacitance of the output capacitor.

b) Evaluate the following items based on the circuit waveforms:
i) the energy transferred from the voltage source to the capacitor during the first 10 switching periods,
ii) the capacitor voltage at the end of the 10^{th} switching period, and
iii) the time instant when the capacitor voltage elevates approximately to 300 V.

c) Suggest a new switch drive scheme that would minimize the total time required to charge the capacitor to a desired voltage.

d) Now assume that the capacitor charging circuit is modified into three different circuits, as shown in Fig. P2.24(b). For each circuit, explain its operation or describe the expected response of the circuit.

2.25** Three different solenoid drive circuits are shown in Fig. P2.25. Referring to the common switch drive signal, answer the questions.

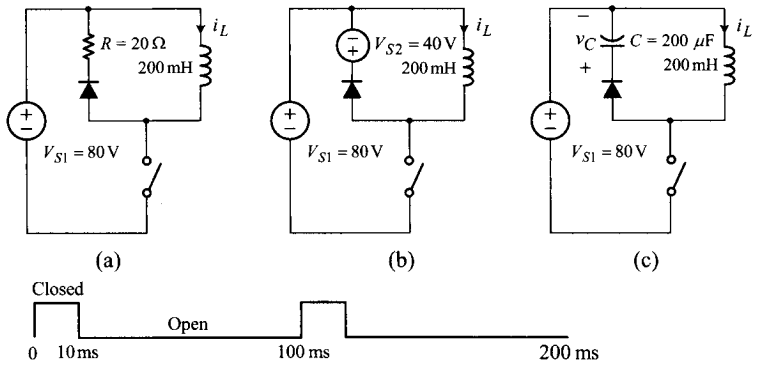

Fig. P2.25

a) Circuit (a) uses a diode-resistor branch as a freewheeling path.
i) Find the expression for i_L for 10 ms < t < 100 ms.
ii) Find the power consumed at the resistor R = 20 Ω.

b) Circuit (b) employs two independent voltages sources: V_{S1} = 80 V and V_{S2} = 40 V.
i) Sketch i_L for 0 < t < 100 ms. Label the value of i_L at t = 20 ms on your sketch.
ii) When the switch is turned-off, what would happen to the energy stored in the inductor?

c) Circuit (c) uses a practical capacitor C = 200 μF in place of V_{S2}.
i) Find the value of v_C at t = 99 ms. Assume the capacitor is initially uncharged and i_L = 0 at t = 99 ms.
ii) Under the same assumptions used in **i)**, sketch the general shapes of i_L and v_C for 0 < t < 200 ms.
iii) What would eventually happen to the circuit as time elapses?

2.26* A transformer is built using a toroidal core with μ_r = 5000, S = 2 cm^2, and $l_m = 4\pi \times 10^{-1}$ cm. The turns of the primary winding are 10 and the turns of the secondary winding are 20. Two different switching circuits shown in Fig. P2.26 are built using the transformer. Referring to the common switch drive signal, sketch i_S and i_T of each circuit for the first two operational periods. Show the maximum and minimum values on your sketch.

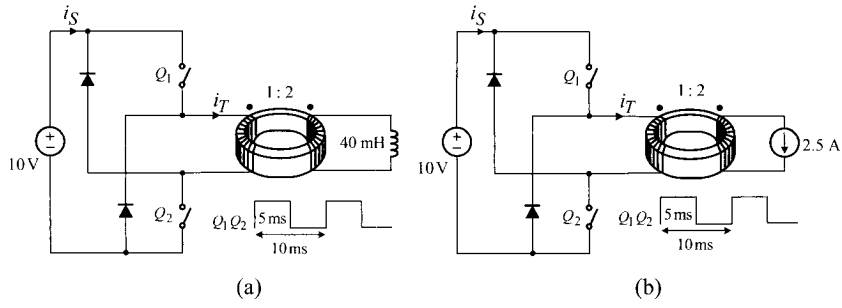

Fig. P2.26

2.27* Consider the circuit shown in Fig. P2.27 along with its switch drive signal. Assume that the inductor and capacitor are initially unenergized.

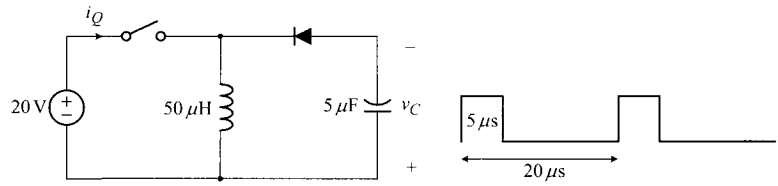

Fig. P2.27

a) Sketch i_Q and v_C for the first two operational periods. Show all the characteristic features of the waveforms including their maximum and minimum values.

b) Evaluate v_C at t = 2.0 ms.

2.28** Figure P2.28 shows the two switching circuits along with their switch drive signals.

a) For Circuit (a), evaluate the following items based on the circuit operation:
i) the energy transferred from the 24 V voltage source to the application circuit during one operational period,
ii) the energy delivered to the capacitor during one operational period,
iii) the energy dissipated in the application circuit during one operational period, and
iv) the capacitor voltage v_C at the end of the first five operational periods.

b) For Circuit (b), evaluate the following items:
i) the energy transferred from the 24 V voltage source to the application circuit during one operational period,
ii) the energy delivered to the capacitor during one operational period,
iii) the energy returned from the application circuit to the 24 V voltage source during one operational period, and

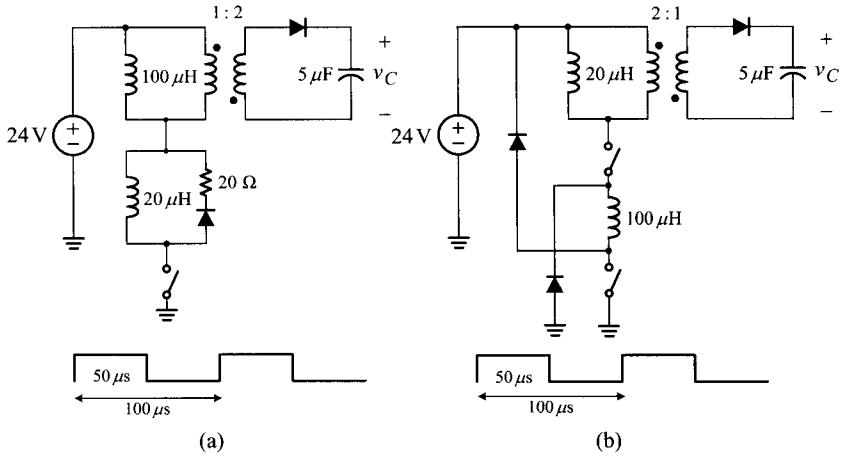

Fig. P2.28

iv) the capacitor voltage v_C at the end of the first five operational periods.

2.29** A transformer is built using a toroidal core with $\mu_r = 5000$, $S = 2$ cm^2, and $l_m = 4\pi \times 10^{-1}$ cm. The turns of the primary winding are 5 and that of the secondary winding are 10. The switching circuit shown in Fig. P2.29 is fabricated using the transformer described above.

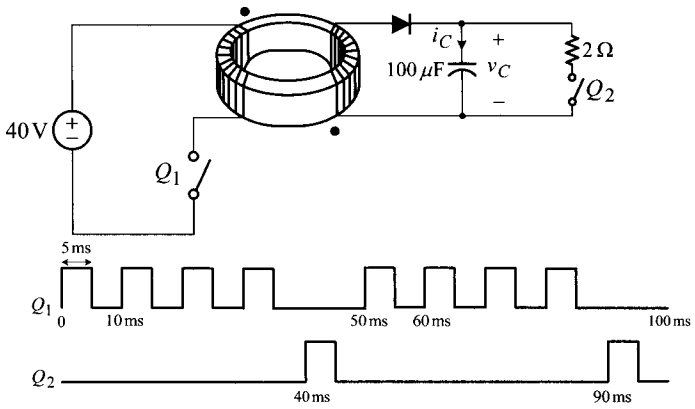

Fig. P2.29

a) Referring to the switch drive signals, sketch the waveforms v_C and i_C for $0 < t < 100$ ms. Show all the important information on your sketch so that your knowledge about the circuit operation is fully exposed.

b) Calculate the average power consumed in the circuit.

CHAPTER 3

BUCK CONVERTER

There are numerous PWM dc-to-dc converters with different power processing functions and respective application areas. Among these, the buck converter has a very simple structure and is straightforward in operation, while also possessing all the essential features commonly found in other PWM dc-to-dc converters. The output voltage of the buck converter is always lower than the input voltage. For this reason, the buck converter is also called the step-down converter.

There is another type of dc-to-dc converter that invariably provides a higher output voltage than the input voltage, called the boost converter or step-up converter. Furthermore, a dc-to-dc converter that either steps down or steps up the input voltage can be synthesized by combining the step-down converter and step-up converter. The resulting converter is called the buck/boost converter or up-down converter.

This chapter deals with the buck converter, while the succeeding chapter covers the boost and buck/boost converters, as well as other PWM dc-to-dc converters. Although focused on the buck converter, theoretical basis and analysis techniques presented in this chapter can readily be extended to other PWM dc-to-dc converters including the boost and buck/boost converters.

As discussed in Chapter 1, the source of a PWM dc-to-dc converter can be any practical standalone dc source or non-ideal dc source obtained by rectifying an ac

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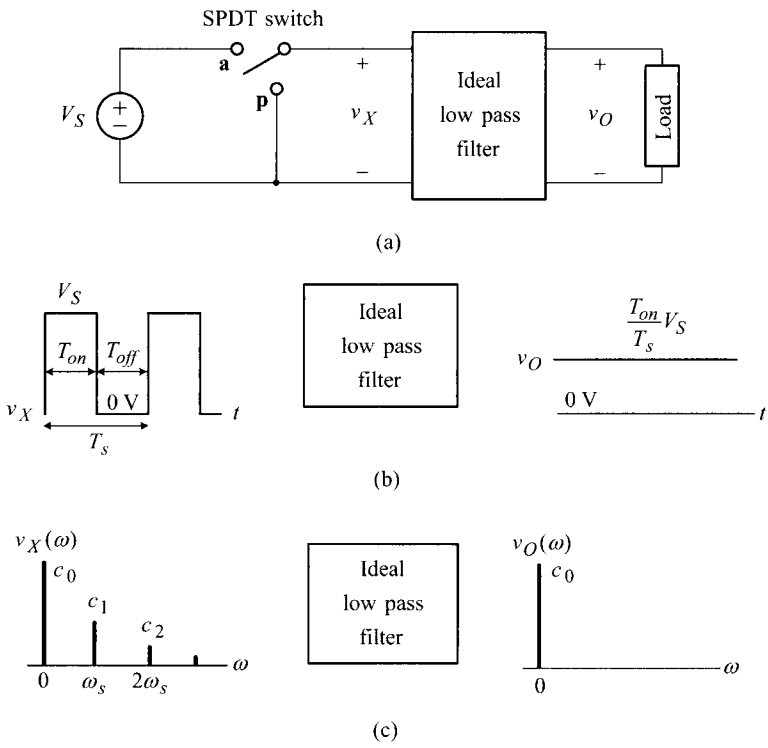


Figure 3.1 Ideal step-down dc-to-dc power conversion. (a) Block diagram representation. (b) Time-domain description. (c) Frequency-domain interpretation.

source. In addition, the load can be any electrical device, equipment, or system operating with a constant voltage. In this book, however, an ideal dc source and resistive load will be initially assumed to concentrate on the study of the dc-to-dc power conversion itself. The issues involved with the non-ideal characteristics of the source and load systems will be addressed in Chapter 9.

This chapter discusses the functional basics and operational details of the buck converter. Several important analysis techniques are introduced and used to reveal the operation and properties of the buck converter. This chapter also illustrates the closed-loop control of the buck converter using the PWM scheme.

3.1 IDEAL STEP-DOWN DC-TO-DC POWER CONVERSION

The buck converter is the simplest circuit configuration that can perform the step-down dc-to-dc power conversion. The concept of the step-down dc-to-dc conversion was introduced in Section 1.1.1 in conjunction with the electric bulb driving circuit

in Fig. 1.2. The current section now presents the theoretical aspects of the step-down power conversion.

The step-down dc-to-dc power conversion can be explained using a conceptual diagram, as shown in Fig. 3.1(a), consisting of two functional blocks: a single-pole double-throw (SPDT) switch and ideal low pass filter. Within one switching period T_s, the SPDT switch holds position **a** for T_{on} and position **p** for $T_{off} = T_s - T_{on}$. The time period T_{on} is defined as the *on-time period*, while T_{off} is denoted as the *off-time period*. The ratio T_{on} to T_s is defined as the *duty ratio* or *duty cycle* D of the SPDT switch

$$D \equiv \frac{T_{on}}{T_s} \tag{3.1}$$

Similarly, the ratio T_{off} to T_s is defined as

$$D' \equiv \frac{T_{off}}{T_s} = \frac{T_s - T_{on}}{T_s} = 1 - D \tag{3.2}$$

The SPDT switch transforms the input voltage V_S into a rectangular waveform v_X, as shown in Fig. 3.1. The rectangular waveform v_X is then applied to the input of the ideal low pass filter.

Using Fourier series expansion, v_X is expressed as the sum of dc component and harmonic sinusoids

$$v_X(t) = c_0 + \sum_{n=1}^{\infty} c_n \sin(n\omega_s t + \theta_n) \tag{3.3}$$

where c_0 represents the dc component and $\omega_s = 2\pi/T_s$ is the fundamental frequency of v_X. The dc component c_0 is simply the average value of v_X

$$c_0 = \bar{v}_X(t) = \frac{T_{on}}{T_s} V_S = DV_S \tag{3.4}$$

If the cut-off frequency of the ideal low pass filter, ω_c, is lower than the fundamental frequency of v_X, $\omega_c < \omega_s$, all the harmonic components will be completely blocked and only the dc component will appear as the output of the low pass filter

$$v_O(t) = c_0 = DV_S \tag{3.5}$$

Figure 3.1(b) shows the time-domain input-to-output description of the ideal low pass filter, while Fig. 3.1(c) depicts the frequency-domain interpretation.

The dc-to-dc power conversion illustrated in Fig. 3.1 has the following properties.

1) The circuit provides a pure dc voltage for the load, due to the ideal characteristics of the low pass filter.

2) The voltage gain of the circuit, the ratio v_O to V_S, is simply the duty ratio of the SPDT switch. Thus, the output voltage can be adjusted by controlling the duty ratio of the SPDT switch.

3) Because $0 < D < 1$, the output voltage is always lower than the input voltage.

For these reasons, the power conversion illustrated in Fig. 3.1 is called the ideal step-down dc-to-dc power conversion.

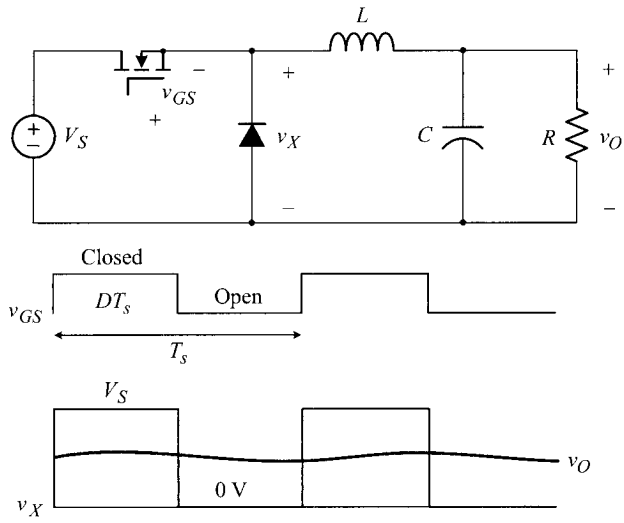


Figure 3.2 Buck converter and major waveforms.

3.2 BUCK CONVERTER: STEP-DOWN DC-TO-DC CONVERTER

Although the block diagram in Fig. 3.1 is a conceptual illustration of the ideal step-down dc-to-dc power conversion, there exists a practical converter that is very similar to Fig. 3.1 in structure and operation. This converter is called the buck converter and is one of most widely-used dc-to-dc converters. This section explains the circuit configuration and theoretical basics of the buck converter, while succeeding sections describe operational details.

3.2.1 Evolution to Buck Converter

The functional diagram in Fig. 3.1 is transformed into the buck converter by implementing the SPDT switch with semiconductor switches and replacing the ideal low pass filter with an LC filter. Figure 3.2 shows the circuit diagram of the buck converter along with its major waveforms. The SPDT switch is implemented with the MOSFET-diode pair. The MOSFET switch is turned-on/off by the gate drive signal v_{GS}, meanwhile the status of the diode is determined by the condition of the MOSFET switch. When the MOSFET switch is turned-on by v_{GS}, the diode is turned-off because the input voltage V_S reverse-biases the pn junction. Conversely, when the MOSFET switch is turned-off, the inductor current forces the diode to conduct, thereby creating a freewheeling path.

A second-order LC filter is used as a functional substitute for the ideal low pass filter. The LC filter, despite its far from ideal characteristics, provides more than adequate filtering for most applications. It will be shown later that the consequences

of the non-ideal filtering property of the LC filter are indeed negligible. A pure resistor is assumed for the load to simplify ensuing discussions.

3.2.2 Frequency-Domain Analysis

The LC filter shown in Fig. 3.2 is unable to completely remove the high-frequency harmonics from v_X and the output voltage v_O invariably contains an ac component, as illustrated in Fig. 3.2. The ac component contained in the output voltage is referred to as the *output (voltage) ripple* or *switching ripple*.

A simple frequency-domain analysis is performed to determine the output ripple due to the non-ideal characteristics of the LC filter. The input-to-output transfer function of the LC filter with a load resistor R is given by

$$F_f(s) = \frac{v_o(s)}{v_x(s)} = \frac{\frac{1}{sC} \parallel R}{sL + \frac{1}{sC} \parallel R} = \frac{1}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \tag{3.6}$$

where ω_o is the pole frequency

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{3.7}$$

and Q is the damping ratio of the filter circuit

$$Q = R\sqrt{\frac{C}{L}} \tag{3.8}$$

Figure 3.3 shows the asymptotic plot of $|F_f|$, drawn with the assumptions that the LC filter has a complex pole pair, $Q > 0.5$, and the switching frequency is higher than the pole frequency of the filter: $\omega_s > \omega_o$. The LC filter passes the dc component unchanged, yet attenuates the harmonic components of v_X. The input of the LC filter is represented by Fourier series

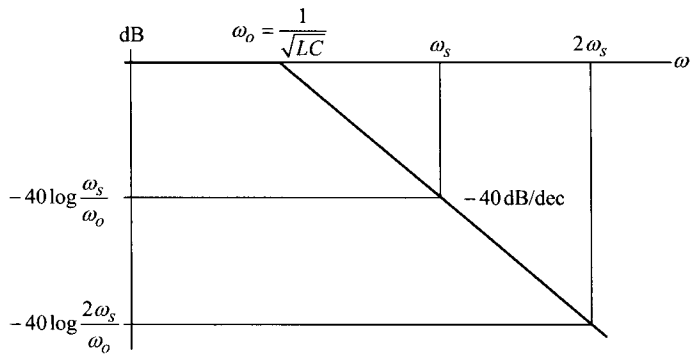


Figure 3.3 Asymptotic plot for transfer function of second-order LC filter.

$$v_X(t) = c_0 + \sum_{n=1}^{\infty} c_n \sin(n\omega_s t + \theta_n) \tag{3.9}$$

The coefficients for the harmonic sinusoids are determined as

$$c_n = \frac{\sqrt{2}V_S}{n\pi}\sqrt{1 - \cos(n2\pi D)} \tag{3.10}$$

from the Fourier series expansion. Referring to Fig. 3.3, the n^{th} order harmonic is attenuated by $-40\log(n\omega_s/\omega_o)$ with the low pass filter, while the dc component remains unaltered. Accordingly, the output of the LC filter is expressed as

$$v_O(t) = c_0 + \sum_{n=1}^{\infty} c'_n \sin(n\omega_s t + \theta'_n) \tag{3.11}$$

where

$$\begin{aligned} c'_n &= c_n 10^{\frac{-40\log\left(\frac{n\omega_s}{\omega_o}\right)}{20}} \\ &= \underbrace{\frac{\sqrt{2}V_S}{n\pi}\sqrt{1 - \cos(n2\pi D)}}_{c_n} 10^{\frac{-40\log\left(\frac{n\omega_s}{\omega_o}\right)}{20}} \end{aligned} \tag{3.12}$$

The second term on the right-hand side of (3.11), representing the total sum of the harmonic sinusoids, collectively constitutes the output ripple. Equation (3.12) shows that the output ripple is reduced to a negligible level if the condition $\omega_s \gg \omega_o$ is met. This can be achieved by either lowering the pole frequency with larger filter components or increasing the switching frequency.

■ EXAMPLE 3.1 Estimation of Output Ripple

This example demonstrates the accuracy of the previous frequency-domain ripple analysis. A buck converter operating with $V_S = 16$ V, $L = 40$ μH, $C = 470$ μF, $R = 1$ Ω, $T_s = 20$ μs, and $D = 0.25$ is considered. The pole frequency of the filter is given by

$$\omega_o = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{40 \times 10^{-6}\, 470 \times 10^{-6}}} = 7.293 \times 10^3 \text{ rad/s}$$

and the switching frequency of the converter is

$$\omega_s = \frac{2\pi}{T_s} = \frac{2\pi}{20 \times 10^{-6}} = 3.142 \times 10^5 \text{ rad/s}$$

The dc component of the output is determined as

$$c_0 = DV_S = 0.25 \cdot 16 = 4 \text{ V}$$

and the magnitude of the fundamental sinusoid is calculated as

$$c_1' = \underbrace{\frac{\sqrt{2}\,V_S}{1\cdot\pi}\sqrt{1-\cos(1\cdot 2\pi D)}}_{c_1} 10^{\frac{-40\log\left(\frac{1\,\omega_s}{\omega_o}\right)}{20}}$$

$$= \frac{\sqrt{2}\;16}{1\cdot\pi}\sqrt{1-\cos(1\cdot 2\pi\, 0.25)}\;10^{\frac{-40\log\left(\frac{1\cdot 3.142\times 10^5}{7.293\times 10^3}\right)}{20}}$$

$$= 3.880\times 10^{-3}$$

Similarly, the magnitudes of the higher-order harmonics are determined as $c_2' = 6.860\times 10^{-4}$, $c_3' = 1.439\times 10^{-4}$, $c_4' = 0$, and $c_5' = 3.104\times 10^{-5}\cdots$.

Two important observations on the output voltage waveform of the buck converter are made from the previous analysis.

1) The coefficients of the harmonic components of the output voltage are negligibly small compared to the dc component. This indicates that the LC filter provides sufficient filtering and the output of the converter is practically $c_0 = 4$ V.

2) Because the coefficient of the fundamental harmonic sinusoid, c_1', is much larger than the coefficients of the higher-order harmonics, the amplitude of the output ripple is estimated as $\Delta v_O(t) \approx 2\,c_1' = 2\cdot 3.880\times 10^{-3} = 7.76$ mV.

Figure 3.4 shows the output voltage of the buck converter obtained from PSpice® simulation. The magnitude of the output ripple is very close to the analytical prediction of 7.76 mV.

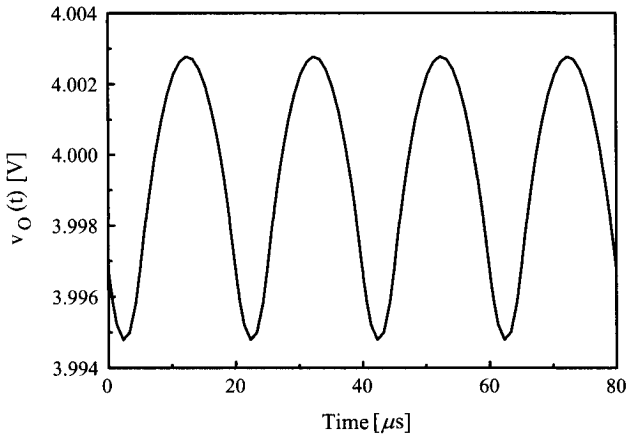


Figure 3.4 Output voltage waveform of buck converter.

As demonstrated in Example 3.1, a simple second-order LC filter readily attenuates the output ripple to a negligible level. The second-order LC filter is just one specific example among many possible filter configurations. If a larger output ripple is allowed, the capacitor can be removed from the second-order filter, resulting in a first-order LR filter. Conversely, if further ripple attenuation is required, a higher-order filter or multi-stage filter can be employed.

3.3 BUCK CONVERTER IN START-UP TRANSIENT

This section explains the operation of the buck converter during the start-up process. The concept of piecewise linear analysis is first introduced and the start-up response is then explained using the piecewise linear analysis method.

3.3.1 Piecewise Linear Analysis

The time-domain analysis of a dc-to-dc converter is not straightforward mainly because the switching action of the semiconductor devices forces the converter to periodically change its topological structure. One standard approach to analyzing the time-domain behavior of dc-to-dc converters is the piecewise linear analysis, where a dc-to-dc converter is considered as a combination of several linear circuits, each of which is valid for a specific time interval within one switching period.

The circuit that is effective when its switch drive signal is *on* (thus, the active switch is turned-on and the diode is turned-off) is defined as the *on-time subcircuit*. Likewise, the effective circuit when the switch drive signal is *off* (thus, with the active switch off and diode on) is denoted as the *off-time subcircuit*. The operation of a dc-to-dc converter is analyzed by first examining each subcircuit individually and later taking into account of the circuit behavior of the two subcircuits collectively. Figure 3.5 shows a buck converter and its on-time and off-time subcircuits. The piecewise linear analysis using these subcircuits simplifies the analysis process and, more importantly, provides significant insights on the converter operation.

3.3.2 Start-up Response

The time-domain response of dc-to-dc converters can be analyzed by solving the circuit equations for the on-time and off-time subcircuits successively. For example, the response of the inductor current during the start-up process can be calculated as outlined below. First, the circuit equations for the on-time subcircuit are solved for $0 < t < DT_s$ with zero initial conditions. The expression for the inductor current is found from the resulting solutions. Second, the circuit equations for the off-time subcircuit are solved for $DT_s < t < T_s$ considering the circuit variables evaluated at $t = DT_s$ as the new initial conditions. By repeating this process, the transient response of the inductor current for the entire start-up period is obtained.

As an alternative to the previous iterative analysis, a qualitative method can be used to predict the behavior of the inductor current. For the time period $0 < t < DT_s$

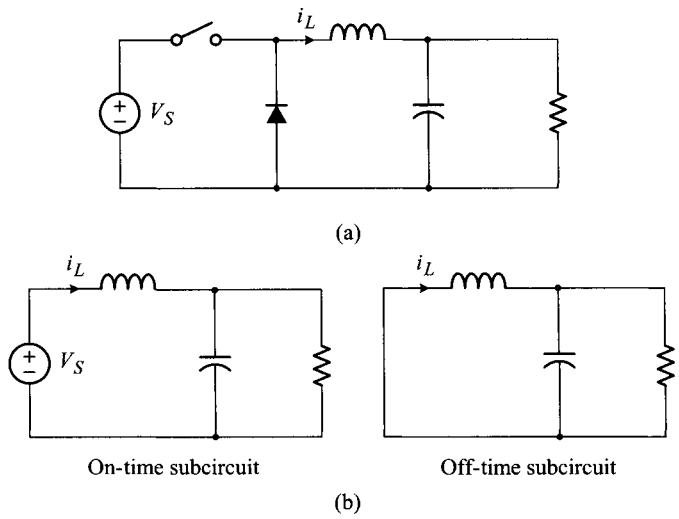


Figure 3.5 Buck converter and on-time and off-time subcircuits. (a) Buck converter. (b) On-time and off-time subcircuits.

during which the converter retains the on-time subcircuit, the voltage source transfers energy to the inductor. As a result, the inductor current is increased as illustrated in Fig. 3.6. For the time interval $DT_s < t < T_s$ in which the converter holds the off-time subcircuit, the energy stored in the inductor is released to the load, and consequently the inductor current is decreased.

During the early stage of the start-up process, the energy transferred from the source is larger than the energy released to the load. Accordingly, the net change in the energy storage in the inductor at each switching period is positive. This implies that the inductor current progresses as illustrated in Fig. 3.6. As time passes, the difference between the amounts of the transferred energy and the released energy

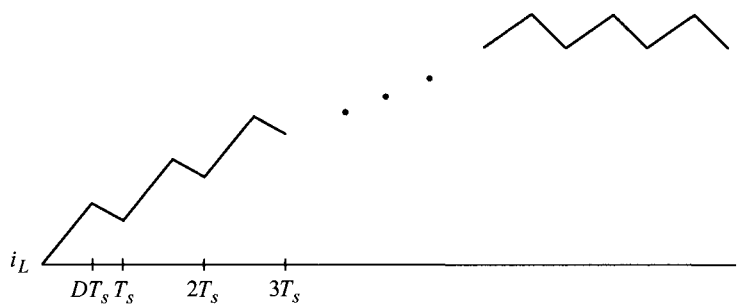


Figure 3.6 Qualitative behavior of inductor current.

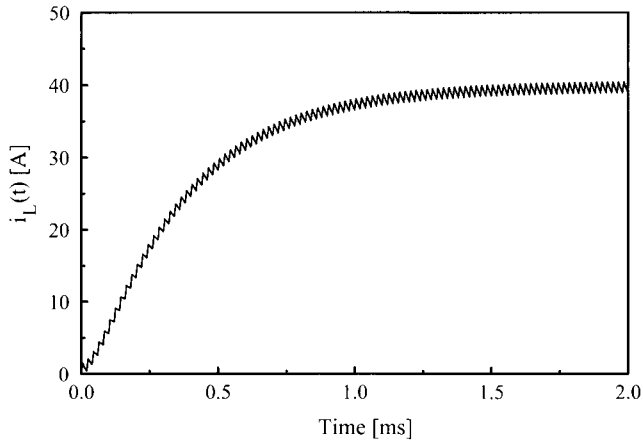


Figure 3.7 Start-up response of inductor current.

becomes smaller. When the on-time energy transfer becomes the same as the off-time energy release, the converter establishes steady state and the inductor current settles into a periodic triangular waveform.

■ EXAMPLE 3.2 Start-up Response of Inductor Current

This example illustrates the start-up response of the buck converter. Figure 3.7 shows the inductor current during the start-up process of the buck converter introduced in Example 3.1. A load resistance $R = 0.1\ \Omega$ is used in this simulation, while other parameters are the same as those of Example 3.1.

3.4 BUCK CONVERTER IN STEADY STATE

A properly designed dc-to-dc converter should eventually reach steady state. When a dc-to-dc converter is in a steady state, the inductor current settles into a periodic triangular waveform and the output voltage becomes nearly constant with a small ripple component. This section first introduces several circuit analysis techniques and later analyzes the circuit waveforms of the buck converter in steady state.

3.4.1 Circuit Analysis Techniques

In addition to standard circuit equations, several specific analysis techniques are used for dc-to-dc power conversion circuits. These include the piecewise linear analysis, small-ripple approximation, flux balance condition on inductors, and charge balance condition on capacitors.

Piecewise Linear Analysis

The piecewise linear analysis technique is a very efficient method to analyze time-variant dc-to-dc power conversion circuits. When coupled with the forthcoming small-ripple approximation, the piecewise linear analysis allows us to study dc-to-dc converters only using very simple circuit equations. In most cases, the circuit waveforms are accurately predicted by quick graphical constructions based on fundamental circuit equations.

Small-Ripple Approximation

Another useful technique for the steady-state analysis of dc-to-dc converters is the *small-ripple approximation.* This analysis postulates that *the ripple component contained in the output of a converter is so small that the output voltage can be considered a pure dc.* This assumption greatly simplifies the circuit analysis without compromising accuracy.

In practice, the ripple component in the output voltage is actually very small compared to the dc component, and its effects on the converter operation are negligible. Consequently, an exact circuit analysis including the ripple component is usually unnecessary and the simplified analysis assuming a constant output is fully adequate for most cases. The streamlined analysis based on the small-ripple approximation quickly yields simple circuit equations, and the resulting solutions retain sufficient accuracy for all engineering purposes.

The small-ripple approximation can be justified from at least two different perspectives. First, because the circuit components of a dc-to-dc converter are selected to minimize the output voltage ripple, the errors caused by the small-ripple approximation are indeed negligible. Second, the output voltage ripple can always be accurately estimated from the results of the simplified analysis based on the small-ripple approximation. Consequently, the small-ripple approximation does not bring in any real loss in the analysis accuracy. Discussions about the output ripple estimation are given in Section 3.4.3.

Flux Balance Condition and Charge Balance Condition

Inductors used in dc-to-dc conversion circuits should satisfy the flux balance condition; the flux increase during an on-time period should be the same as the flux decrease during an off-time period. As demonstrated in Section 2.2.1, the flux balance condition can be transformed into the volt-sec balance condition. The volt-sec balance condition states that *the product of the voltage level and time interval, evaluated over the period when the inductor voltage is positive, should be the same as the voltage-time product calculated when the inductor voltage is negative.* Furthermore, as the generation of the volt-sec balance condition, the average value of the inductor voltage is considered to be zero.

Capacitors are subjected to the charge balance condition; the net change in the charge storage in a capacitor should be balanced at zero for each switching period.

The charge balance condition can be converted into the amp-sec balance condition. The amp-sec balance condition indicates that *the product of the positive current value (coming into the capacitor) and the current-flowing period should be the same as the product of the negative current value (leaving from the capacitor) and the corresponding current-flowing time.* More generally, the average value of the capacitor current is considered to be zero, as is the case for the inductor voltage.

The volt-sec balance condition and amp-sec balance condition place constraints on the circuit variables of inductors and capacitors in dc-to-dc power conversion circuits. When dc-to-dc converters reach steady state, the circuit variables settle down to the values that satisfy the volt-sec and amp-sec balance conditions. Thus, these conditions can be considered as the circuit theorems that facilitate the steady-state analysis of dc-to-dc converters.

3.4.2 Steady-State Analysis

The steady-state analysis of the buck converter is now performed based on the piecewise linear analysis, along with the small-ripple approximation, volt-sec balance condition, amp-sec balance condition, and other standard circuit analysis techniques. Figure 3.8 shows a buck converter, on-time and off-time subcircuits, and major circuit waveforms. Based on the small-ripple approximation, the output of the converter is considered as a constant V_O for both on-time and off-time subcircuits. From Fig. 3.8(b), the voltage across the inductor is determined as

$$v_L(t) = \begin{cases} V_S - V_O & \text{for on-time subcircuit} \\ -V_O & \text{for off-time subcircuit} \end{cases} \tag{3.13}$$

By applying the volt-sec balance condition to the inductor, it follows that

$$(V_S - V_O)DT_s = V_O(1 - D)T_s \tag{3.14}$$

which is simplified to

$$V_O = DV_S \tag{3.15}$$

yielding the voltage gain expression. This voltage gain is identical, as it should be, to the result of the previous frequency-domain analysis.

The circuit equation for the inductor current is given by

$$i_L(t) = \frac{v_L(t)}{L}t = \frac{V_S - V_O}{L}t \tag{3.16}$$

for on-time period DT_s and

$$i_L(t) = -\frac{V_O}{L}t \tag{3.17}$$

for off-time period $(1 - D)T_s$. It is evident from (3.16) and (3.17) that the inductor current ramps up during on-time period and ramps down during off-time period, resulting in a periodic triangular waveform shown in Fig. 3.8(c).

The average value of the inductor current can be determined as follows. The charge balance condition assures that the average value of the current flow through

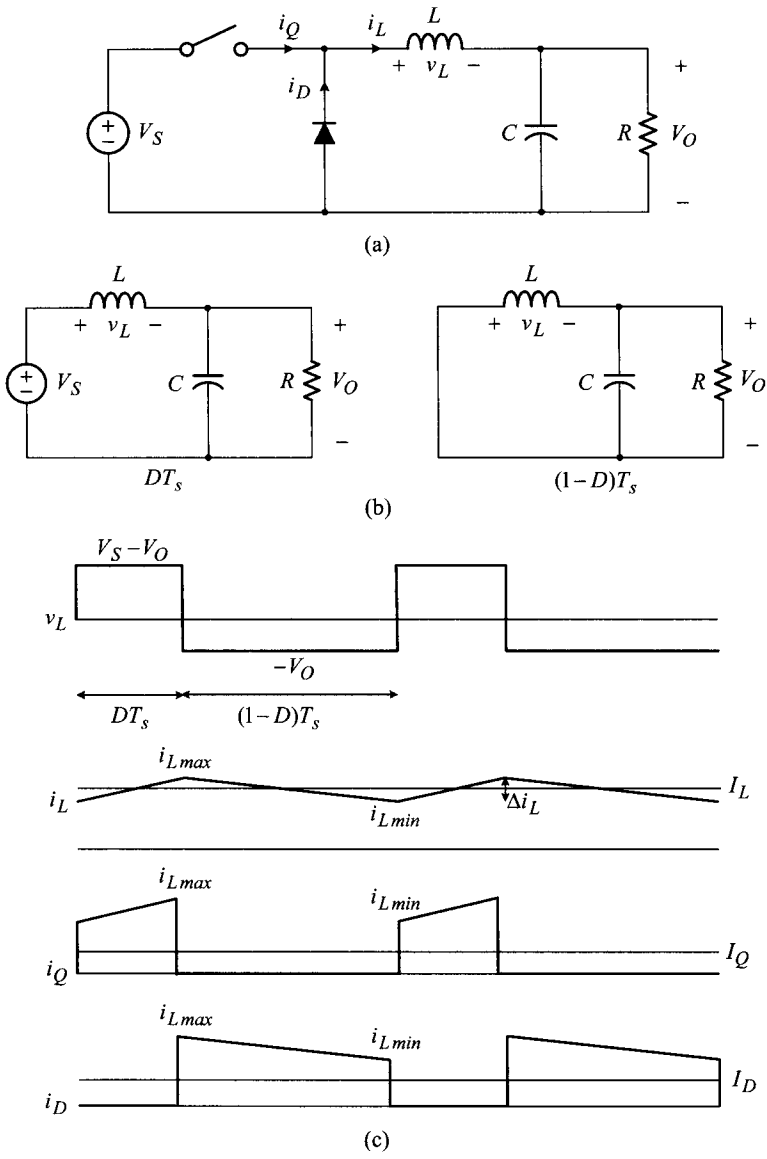


Figure 3.8 Steady-state analysis of buck converter. (a) Buck converter. (b) On-time and off-time subcircuits. (c) Major waveforms.

the capacitor is zero. This implies that the average value of the inductor current should be identical to the dc current passing through the load resistor

$$\bar{i}_L(t) = I_L = \frac{V_O}{R} \tag{3.18}$$

It can also be inferred from (3.16) and (3.17) that the difference between the maximum and minimum values of the inductor current is given by

$$\Delta i_L = \frac{v_L}{L}\Delta t = \frac{V_S - V_O}{L} DT_s = \frac{V_O}{L}(1 - D)T_s \tag{3.19}$$

The maximum and minimum values of the inductor current then become

$$i_{L\,max} = I_L + \frac{1}{2}\Delta i_L \tag{3.20}$$

and

$$i_{L\,min} = I_L - \frac{1}{2}\Delta i_L \tag{3.21}$$

The inductor current flows through the active switch during on-time period, and then freewheels through the diode during off-time period. Figure 3.8(c) also shows the switch current i_Q and diode current i_D, whose average values are given by

$$\bar{i}_Q(t) = I_Q = DI_L \tag{3.22}$$

and

$$\bar{i}_D(t) = I_D = (1 - D)I_L \tag{3.23}$$

■ **EXAMPLE 3.3 Steady-State Analysis of Buck Converter**

This example illustrates the accuracy of the steady-state analysis based on the small-ripple approximation. The important values for the voltage and current waveforms of the buck converter in Example 3.1 are evaluated in Table 3.1. The parameters of the buck converter are $V_S = 16$ V, $L = 40\ \mu$H, $C = 470\ \mu$F, $R = 1\ \Omega$, $T_s = 20\ \mu$s, and $D = 0.25$. Figure 3.9 shows the simulated converter waveforms.

3.4.3 Estimation of Output Voltage Ripple

The output of the buck converter contains a ripple component due to the non-ideal filtering characteristics of an LC filter. An exhaustive analysis can be performed to yield an accurate expression for the output voltage including the ripple component. In practice, however, a quick estimation of the magnitude of the output ripple is more functional and useful than the exact analysis. This section presents a simple output ripple analysis.

Table 3.1 Steady-State Analysis of Buck Converter

Circuit variable	Expression
V_O	$V_S D = 16 \cdot 0.25 = 4$ V
$v_{L\,max}$	$V_S - V_O = 16 - 4 = 12$ V
$v_{L\,min}$	$-V_O = -4$ V
I_L	$\frac{V_O}{R} = \frac{4}{1} = 4$ A
Δi_L	$\frac{V_S - V_O}{L} DT_s = \frac{16-4}{40 \times 10^{-6}} 0.25 \cdot 20 \times 10^{-6} = 1.5$ A
$i_{L\,max}$	$I_L + \frac{1}{2}\Delta i_L = 4 + \frac{1.5}{2} = 4.75$ A
$i_{L\,min}$	$I_L - \frac{1}{2}\Delta i_L = 4 - \frac{1.5}{2} = 3.25$ A

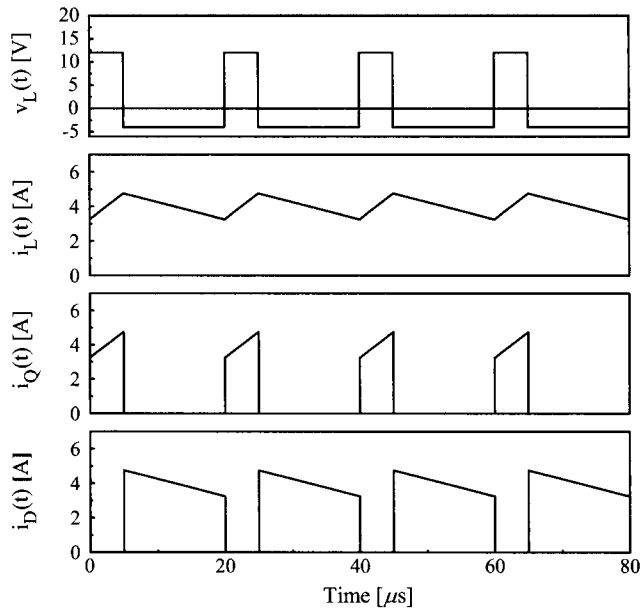


Figure 3.9 Buck converter circuit waveforms.

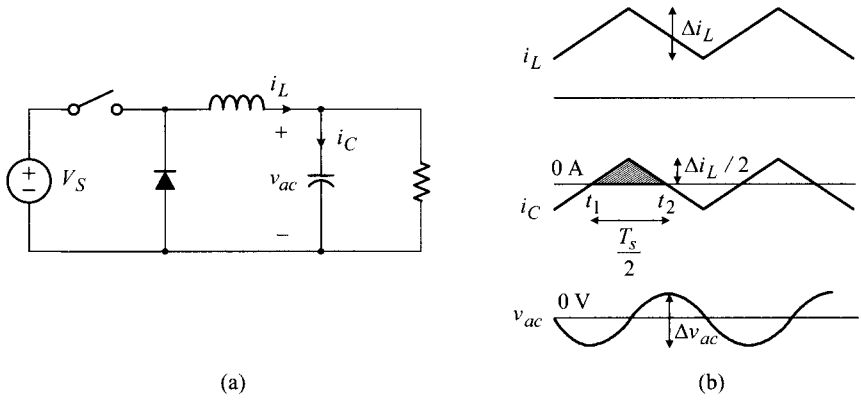


Figure 3.10 Estimation of output ripple. (a) Circuit diagram. (b) Current waveforms and output ripple.

Estimation with Ideal Capacitor

Figure 3.10 shows the circuit diagram and waveforms, associated with the ripple analysis. As shown in the earlier analysis, the inductor current is a triangular waveform consisting of dc and ac components. The dc component passes entirely through the load resistor because the capacitor presents an infinitely large impedance to the dc current.

On the other hand, the ac component, the triangular portion of the inductor current, would flow through both the capacitor and the load resistor. However, a practical converter usually employs a large capacitor to provide sufficient filtering. As a result, the reactance of the capacitor evaluated at the switching frequency is much smaller than the load resistance, and therefore it is highly realistic to assume that the triangular portion of the inductor current fully flows through the capacitor. This situation is illustrated in Fig. 3.10(b).

The triangular current passing through the capacitor develops an ac voltage, thereby creating a ripple component on top of the dc output voltage. The ac voltage across the capacitor is given by

$$v_{ac}(t) = \frac{1}{C}\int i_C(t)\,dt \tag{3.24}$$

where i_C represents the capacitor current. It can be deduced from (3.24) that v_{ac} grows during the period the capacitor current i_C is positive and then decays when i_C is negative, as illustrated in Fig. 3.10(b). The peak-to-peak value of v_{ac} is then found by integrating i_C over the time period during which i_C remains positive

$$\Delta v_{ac} = \frac{1}{C}\int_{t_1}^{t_2} i_C(\tau)\,d\tau \tag{3.25}$$

The integration on the right-hand side of (3.25) in effect corresponds to the area of the triangle enclosed by the positive inductor current and time axis, as highlighted in Fig. 3.10(b). By evaluating the area of the shaded triangle with the incorporation of the fact $|t_2 - t_1| = T_s/2$, the expression (3.25) becomes

$$\Delta v_{ac} = \frac{1}{C}\left(\frac{1}{2}\right)\left(\frac{1}{2}\Delta i_L\right)\left(\frac{1}{2}T_s\right) \tag{3.26}$$

Combining (3.19) into (3.26) leads to the expression for the peak-to-peak variation of v_{ac}

$$\Delta v_{ac} = \frac{1}{8}\frac{V_O}{LC}(1 - D)T_s^2 \tag{3.27}$$

The voltage swing Δv_{ac}, given by (3.27), corresponds to the magnitude of the ripple component, Δv_O, superimposed on the dc value of the output voltage, V_O.

■ EXAMPLE 3.4 Current Waveforms and Output Ripple

This example illustrates the accuracy of the preceding output ripple analysis. Figure 3.11 shows the simulated waveforms for the inductor current i_L, capacitor current i_C, and output voltage v_O of the buck converter used in the previous

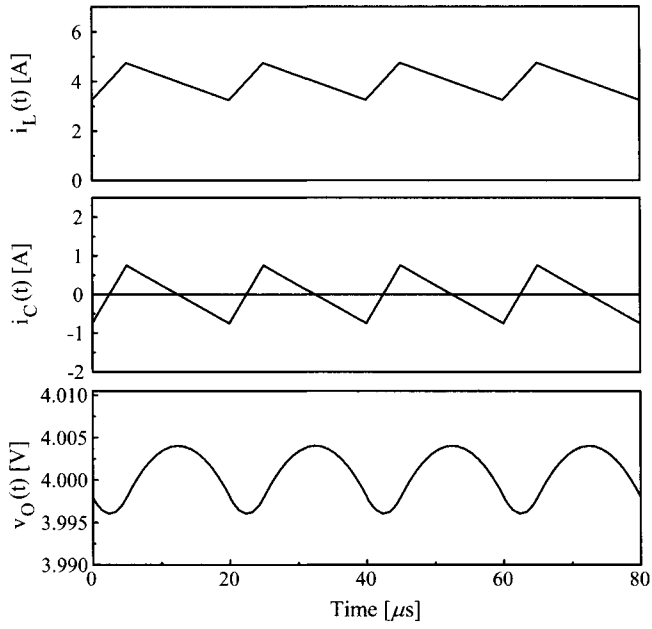


Figure 3.11 Current waveforms and output ripple of buck converter.

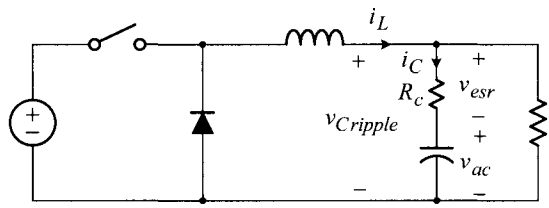


Figure 3.12 Buck converter with practical capacitor.

examples. Based on (3.27), the amplitude of the output ripple is estimated as

$$\begin{aligned}\Delta v_O = \Delta v_{ac} &= \frac{1}{8}\frac{V_O}{LC}(1-D)T_s^2 \\ &= \frac{1}{8}\frac{4}{40\times 10^{-6}\,470\times 10^{-6}}(1-0.25)\left(20\times 10^{-6}\right)^2 \\ &= 7.98\text{ mV}\end{aligned}$$

It is informative to note that the result of this time-domain analysis is very close to the outcome of the previous frequency-domain analysis in Example 3.1. The current analysis shows $\Delta v_O = 7.98$ mV, whereas the previous frequency-domain analysis predicted $\Delta v_O = 7.76$ mV.

Effects of Parasitic Resistance of Capacitor

Earlier discussions on the steady-state operation of the buck converter are based on the assumption that all the circuit components are ideal. In practice, however, the performance of the converter is influenced by non-ideal characteristics of real circuit components. The most noticeable among these is the impact of the parasitic resistance of a real capacitor.

Real capacitors contain an internal parasitic resistance, referred to as the *equivalent series resistance (esr)*, due to the non-ideal characteristics of the dielectric material. Consequently, the circuit model of a real capacitor should include the esr, labeled as R_c in Fig. 3.12. With the presence of the esr, the voltage ripple within a practical capacitor, $v_{Cripple}$, is divided into two components – the ripple voltage produced by the current-carrying capacitance, v_{ac}, and the ripple voltage due to the voltage drop at the esr, v_{esr}, as shown in Fig. 3.12

$$v_{Cripple}(t) = v_{ac}(t) + v_{esr}(t) = \frac{1}{C}\int i_C(t)\,dt + i_C(t)R_c \tag{3.28}$$

where i_C denotes the capacitor current, which corresponds to the triangular portion of the inductor current. From (3.28), the magnitude of the output voltage ripple can be expressed as

$$\Delta v_O = \Delta v_{Cripple} \approx \frac{1}{C}\int_{t_1}^{t_2} i_C(\tau)\,d\tau + \Delta i_C R_c \tag{3.29}$$

Now, using the fact $\Delta i_C = \Delta i_L$, the magnitude of the output ripple is given by

$$\Delta v_O \approx \frac{1}{C}\int_{t_1}^{t_2} i_C(\tau)\,d\tau + \Delta i_L R_c \tag{3.30}$$

The effect of the esr on the output voltage ripple is rather substantial. The magnitude of the ripple component at the esr is usually much larger than the ripple component produced by the capacitance itself. Accordingly, the magnitude of the output voltage ripple can be approximated as

$$\Delta v_O \approx \frac{1}{C}\int_{t_1}^{t_2} i_C(\tau)\,d\tau + \Delta i_L R_c \approx \Delta i_L R_c \tag{3.31}$$

because

$$\frac{1}{C}\int_{t_1}^{t_2} i_C(\tau)\,d\tau \ll \Delta i_L R_c \tag{3.32}$$

■ EXAMPLE 3.5 Output Ripple with Capacitor Esr

This example illustrates the effects of the capacitor esr on the output voltage ripple. The esr of the 470 μF output capacitor used in the buck converter examples is assumed as $R_c = 0.05\ \Omega$. Figure 3.13 shows the simulated waveforms of the voltage across the esr, v_{esr}, and the output voltage, v_O, of the buck converter. As predicted, the output ripple is very similar to the triangular-shaped voltage drop at the capacitor esr. The amplitude of the output ripple is also very close to the analytical prediction of (3.31): $\Delta v_O \approx \Delta i_L R_c = 1.5 \cdot 0.05 = 0.075$ V.

As illustrated above, the ripple component due to the current-carrying capacitance is nearly undetectable and the output voltage ripple is practically determined by the esr of the output capacitor. However, this does not imply that the previous ripple analysis with an ideal capacitor is pointless. The method of ripple calculation in (3.26) is still useful in the sense that the method itself can be applied to many other cases of dc-to-dc converter analyses.

3.5 BUCK CONVERTER IN DISCONTINUOUS CONDUCTION MODE

The operation of the buck converter is relatively simple and easy to understand. The piecewise linear analysis, based on the small-ripple approximation and flux/charge balance conditions, yields an accurate solution for the steady-state operation. However, there are also cases where the buck converter does not follow the aforementioned operational principles and exhibits complicated circuit behavior. This section deals with a new operational mode, known as the discontinuous conduction mode operation.

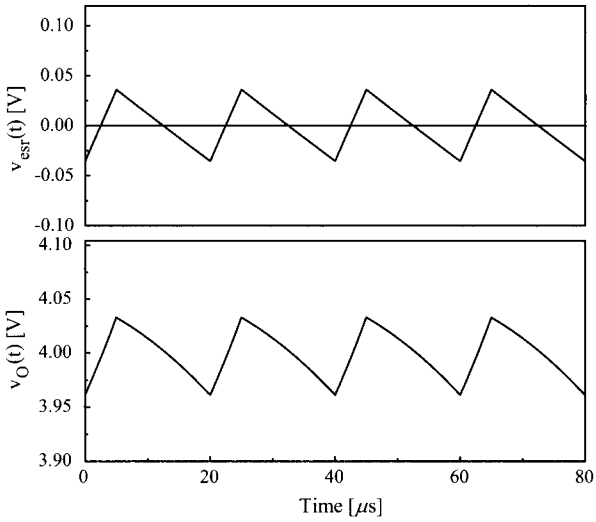


Figure 3.13 Capacitor esr voltage v_{esr} and output voltage v_O.

3.5.1 Origin of Discontinuous Conduction Mode Operation

The existence of the new operational mode can be explained using Fig. 3.14 which shows a series of inductor currents for a buck converter, each with a different value for the load resistance but with the same duty ratio. As the load resistance becomes larger, the inductor current shifts downwards while retaining the same shape. This is because the average value of the inductor current is inversely proportional to the load resistance

$$I_L = \frac{V_O}{R} \tag{3.33}$$

yet the slope of the inductor current remains the same regardless of the change in the load resistance – the inductor voltage that determines the slope of the inductor current will not change as long as the duty ratio remains unaltered. As the load resistance continues to increase, an instant emerges where the minimum value of the inductor current becomes zero. This situation occurs when

$$I_L = \frac{V_O}{R} = \frac{1}{2}\Delta i_L \tag{3.34}$$

If the load resistance is further increased beyond the value that satisfies (3.34), while the converter obeys the same operational principles, the inductor current will shift further down, thereby becoming negative for a certain interval in the switching period. This situation implies that the inductor current should change its direction. However, the current reversal is impossible because the inductor current flows through the diode which is unable to deliver current in the opposite direction.

In reality, when the load resistance becomes large enough to push the average inductor current below the critical value, $I_L = \Delta i_L/2$, the converter no longer follows

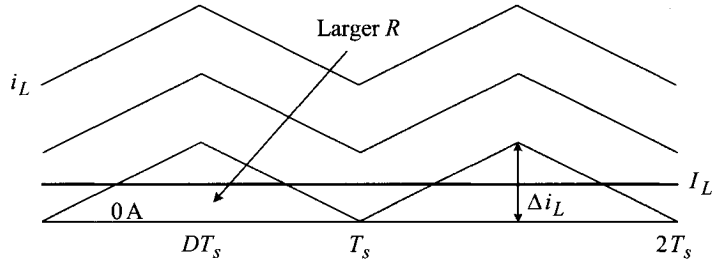


Figure 3.14 Inductor current of buck converter as load resistance increases.

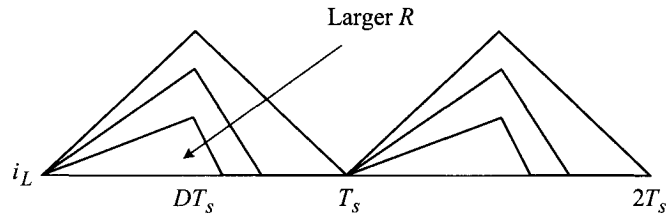


Figure 3.15 Inductor current in DCM operation.

the operational principles discussed earlier and enters a new operational mode. This new operational mode is called the *discontinuous conduction mode* (DCM) where the inductor current vanishes for a certain time interval within each switching period, thereby becoming discontinuous.

The inductor current in DCM operation is illustrated in Fig. 3.15. The qualitative behavior of the inductor current is explained below.

1) During an on-time period, the inductor voltage, $v_L = V_S - V_O$, is always positive and this forces the inductor current to grow linearly. However, as illustrated in Fig. 3.15, the slope of the on-time inductor current varies when the load resistance is changed – the larger the load resistance, the more gradual the slope. The reason for this behavior is that *the voltage gain in DCM operation depends on not only the duty ratio but also the load resistance.* As will be demonstrated in Section 3.5.3, the DCM voltage gain is proportional to the load resistance; namely, as the load resistance becomes larger, so does the voltage gain. Accordingly, a greater load resistance produces a larger output voltage, thereby lowering the ascending slope of the inductor current, $(V_S - V_O)/L$.

2) During an off-time period, the negative inductor voltage, $v_L = -V_O$, forces the inductor current to decay linearly. The condition for DCM is $I_L < \Delta i_L/2$, and this condition implies that the inductor current reduces to zero before the next switching period begins. When the inductor current becomes zero, the diode is turned-off and remains off for the remaining part of the switching period.

As mentioned above, the output voltage in DCM increases in proportion to the load resistance. Accordingly, as the load resistance grows larger, the decaying slope becomes steeper. As the decaying slope becomes steeper, the period during which the inductor current is absent grows wider, as illustrated in Fig. 3.15.

In contrast to the DCM operation, the case where the inductor current is present all the time is called *continuous conduction mode* (CCM) operation. We implicitly assumed CCM operations in the converter analyses of the previous sections. It is important to realize that the DCM operation is as equally important and practical as the CCM operation, because all the dc-to-dc converters, even intended for CCM operation at normal conditions, will encounter DCM operation when the load current becomes smaller than the critical value: $I_L = \Delta i_L/2$.

3.5.2 Conditions for DCM Operation

It is evident from the previous analysis that the operational mode of the converter is determined as

$$\begin{aligned} I_L &> \frac{1}{2}\Delta i_L: \quad \text{CCM} \\ I_L &= \frac{1}{2}\Delta i_L: \quad \text{borderline between CCM and DCM} \\ I_L &< \frac{1}{2}\Delta i_L: \quad \text{DCM} \end{aligned} \tag{3.35}$$

Referring to (3.18) and (3.19), the condition for the borderline between CCM and DCM operations is expressed as

$$I_L = \frac{1}{2}\Delta i_L \quad \Rightarrow \quad \frac{V_O}{R} = \frac{1}{2}\frac{V_O}{L}(1-D)T_s \tag{3.36}$$

Equation (3.36) is used to find the critical value for the load resistance or filter inductance that places the converter at the CCM/DCM borderline

$$R_{crit} = \frac{2L}{(1-D)T_s} \tag{3.37}$$

$$L_{crit} = \frac{(1-D)R\,T_s}{2} \tag{3.38}$$

Equations (3.37) and (3.38) enable us to determine the operational mode based on the value of the specific circuit component. When the load resistance is larger than R_{crit}, the converter establishes DCM operation. Likewise, when the inductance is reduced to a value smaller than L_{crit}, the converter enters DCM operation.

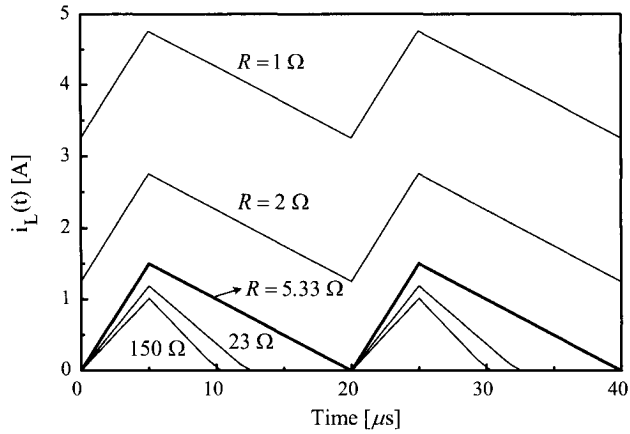


Figure 3.16 Inductor current waveforms with different load resistances.

■ EXAMPLE 3.6 Operational Mode Change with Resistance Variation

This example illustrates the change in the operational mode as the load resistance is varied. The critical resistance R_{crit} of the buck converter in the preceding examples is evaluated as

$$R_{crit} = \frac{2L}{(1-D)T_s} = \frac{2 \cdot 40 \times 10^{-6}}{(1-0.25)\,20 \times 10^{-6}} = 5.33\ \Omega$$

The inductor current waveforms of the buck converter, whose load resistance is varied between $0.2R_{crit} < R < 28R_{crit}$, are shown in Fig. 3.16. The converter is on the boundary of CCM and DCM operations when $R = 5.33\ \Omega = R_{crit}$ and enters DCM when the load resistance is further increased.

■ EXAMPLE 3.7 Operational Mode Change with Inductance Variation

This example shows the operational mode change when the inductance is altered. The critical inductance L_{crit} of the previous buck converter with a load resistance $R = 1\ \Omega$ is given by

$$L_{crit} = \frac{(1-D)RT_s}{2} = \frac{(1-0.25)1 \cdot 20 \times 10^{-6}}{2} = 7.5\ \mu\text{H}$$

Figure 3.17 shows the inductor current waveforms of the converter where the inductance is varied between $0.53L_{crit} < L < 5.3L_{crit}$. As the inductance becomes smaller, the current swing Δi_L increases, thereby causing the converter to operate on the borderline when $L = 7.5\ \mu\text{H} = L_{crit}$, and in DCM when $L < L_{crit}$.

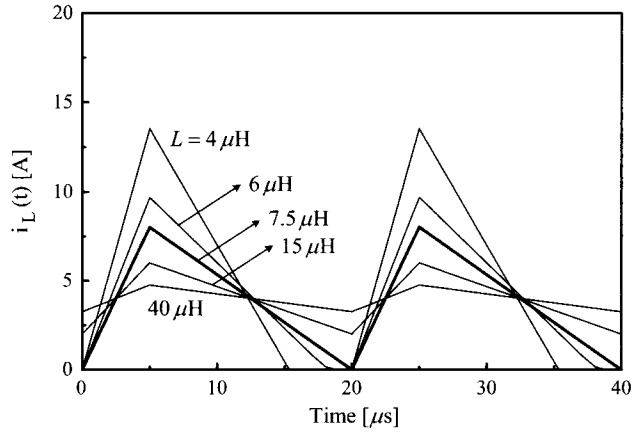


Figure 3.17 Inductor current waveforms with different filter inductances.

3.5.3 Steady-State Operation in DCM

In DCM operation, three topological modes exist within one switching period, as illustrated in Fig. 3.18. In addition to the on-time and off-time subcircuits found in CCM operation, a new subcircuit appears as the inductor current disappears during an off-time period. This third subcircuit is referred to as the DCM subcircuit in Fig. 3.18(a).

Figure 3.18(b) depicts typical DCM waveforms for the inductor current and inductor voltage. The notation D_1 used in Fig. 3.18(b) is defined as

$$D_1 \equiv \frac{\text{a part of off-time period in which inductor current exists}}{\text{switching period}}$$

When the converter is reduced to the DCM subcircuit, the inductor voltage and inductor current both become zero, as shown in Fig. 3.18(b): $i_L = 0 \Rightarrow \Delta i_L = 0 \Rightarrow v_L = L(\Delta i_L/\Delta t) = 0$. By applying the volt-sec balance condition to the inductor, it follows that

$$(V_S - V_O)DT_s = V_O D_1 T_s \tag{3.39}$$

which is simplified to

$$\frac{V_O}{V_S} = \frac{D}{D + D_1} \tag{3.40}$$

The unknown variable D_1 should be eliminated from (3.40) to result in the complete DCM voltage gain. The additional equation, needed for the elimination of D_1, can be formulated as follows. The average value of the inductor current should be the same as the load current, because the average capacitor current is zero due to the charge balance condition. From the geometry of the inductor current, the average

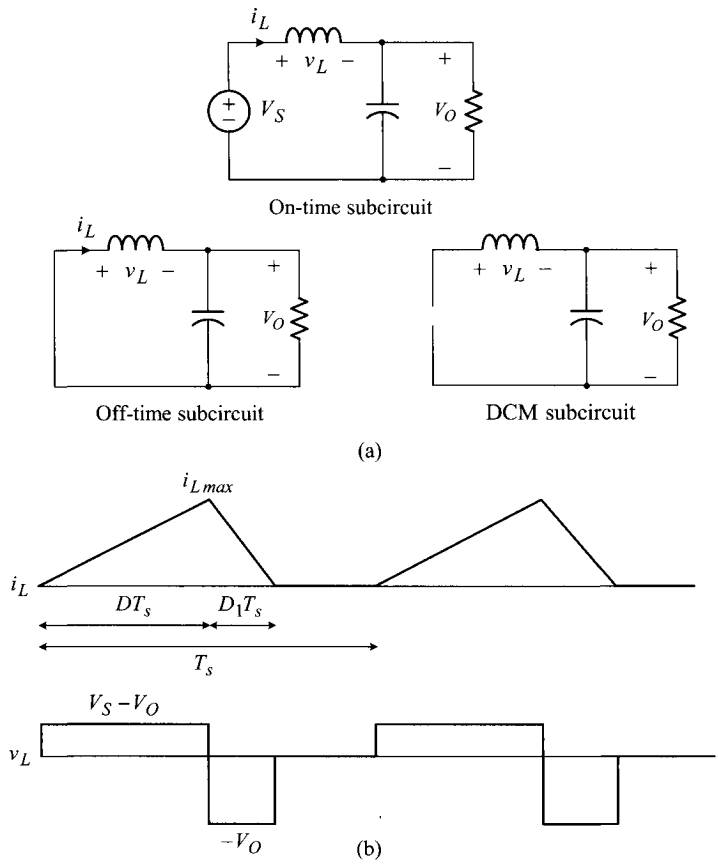


Figure 3.18 Operation of buck converter in DCM. (a) Three subcircuits. (b) Inductor current i_L and inductor voltage v_L.

inductor current is given by

$$I_L = \frac{\frac{1}{2} i_{Lmax}(D + D_1)T_s}{T_s} \tag{3.41}$$

Based on the facts that

$$I_L = I_O = \frac{V_O}{R} \tag{3.42}$$

and

$$i_{Lmax} = \frac{V_O}{L} D_1 T_s \tag{3.43}$$

the expression (3.41) is rewritten as

$$\frac{V_O}{R} = \frac{1}{2}\underbrace{\frac{V_O}{L}D_1 T_s}_{i_{L,max}}(D + D_1) \tag{3.44}$$

which is simplified to

$$D_1^2 + DD_1 - \frac{2L}{RT_s} = 0 \tag{3.45}$$

By solving (3.45) for D_1

$$D_1 = \frac{1}{2}\left(-D + \sqrt{D^2 + \frac{8L}{RT_s}}\right) \tag{3.46}$$

and finally incorporating (3.46) into (3.40), the DCM voltage gain is determined as

$$\frac{V_O}{V_S} = \frac{2D}{D + \sqrt{D^2 + \frac{8L}{RT_s}}} \tag{3.47}$$

The voltage gain is a nonlinear function of the circuit parameters and operational conditions.

Three informative observations can be made from the previous analysis. First, it is evident from (3.47) that the voltage gain increases as the load resistance grows larger, as addressed earlier in conjunction with the behavior of the inductor current in DCM. Second, when the borderline condition given by (3.36) is incorporated into (3.46), it follows that $D_1 = 1 - D$, indicating that the converter is indeed on the boundary between CCM and DCM. Finally, for most converter parameters, the following relationship holds

$$\frac{2D}{D + \sqrt{D^2 + \frac{8L}{RT_s}}} > D \tag{3.48}$$

which indicates that the DCM voltage gain is larger than the CCM counterpart when the same duty ratio is assumed.

■ EXAMPLE 3.8 Steady-State Analysis in DCM

This example illustrates the circuit waveforms of a buck converter in DCM. The load resistance of the buck converter used in the previous examples is reduced to $R = 12\ \Omega$, while the other parameters retain the original values: $V_S = 16$ V, $L = 40\ \mu$H, $C = 470\ \mu$F, $T_s = 20\ \mu$s, and $D = 0.25$. Because $R = 12\ \Omega > R_{crit} = 5.33\ \Omega$, the converter is in DCM region. Theoretical predictions for the steady-state response of the converter are listed in Table 3.2. The accuracy of the theoretical predictions is confirmed with the simulated waveforms in Fig. 3.19.

Table 3.2 Steady-State Analysis in DCM

Circuit variable	Expression
D_1	$\frac{1}{2}\left(-D+\sqrt{D^2+\frac{8L}{RT_s}}\right)$
	$=\frac{1}{2}\left(-0.25+\sqrt{0.25^2+\frac{8\cdot 40\times 10^{-6}}{12\cdot 20\times 10^{-6}}}\right)=0.47$
V_O	$\frac{2D}{D+\sqrt{D^2+\frac{8L}{RT_s}}}V_S$
	$=\frac{2\cdot 0.25}{0.25+\sqrt{0.25^2+\frac{8\cdot 40\times 10^{-6}}{12\cdot 20\times 10^{-6}}}}16=5.59\ \text{V}$
i_{Lmax}	$\frac{V_O}{L}D_1T_s=\frac{5.59}{40\times 10^{-6}}0.47\cdot 20\times 10^{-6}=1.31\ \text{A}$

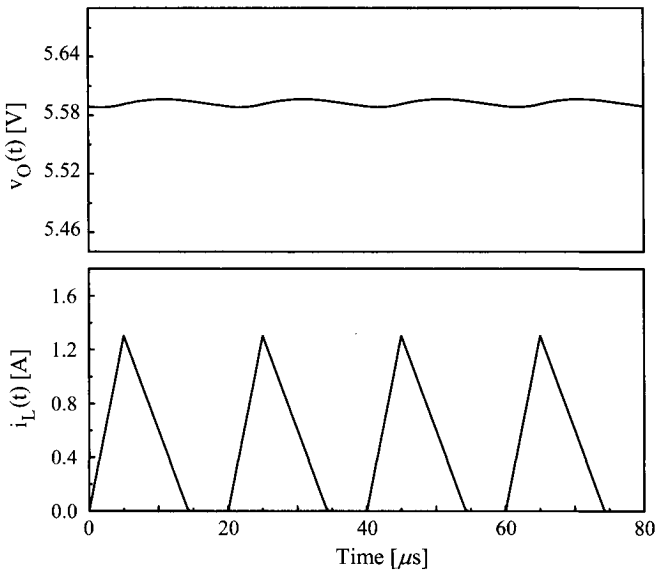


Figure 3.19 Output voltage v_O and inductor current i_L of buck converter in DCM.

The operational mode of a dc-to-dc converter can also go through the CCM/DCM transition when its duty ratio is varied. The condition for the DCM operation

$$\frac{V_O}{R}<\frac{1}{2}\frac{V_O}{L}(1-D)T_s \tag{3.49}$$

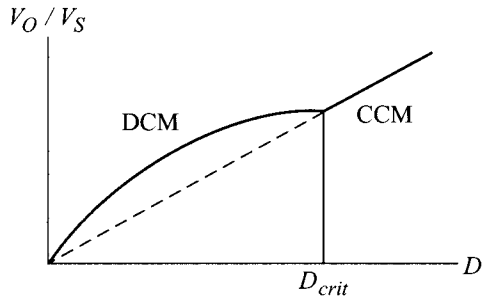


Figure 3.20 Voltage gain of buck converter as function of duty ratio.

is rearranged as

$$D < \left(1 - \frac{2L}{RT_s}\right) \tag{3.50}$$

By defining the right-hand side of (3.50) as

$$1 - \frac{2L}{RT_s} = D_{crit} \tag{3.51}$$

it can be concluded that the converter operates in DCM when $0 < D < D_{crit}$ and in CCM with $D_{crit} < D < 1$. Figure 3.20 depicts the voltage gain of a buck converter. The gain curve follows the DCM gain formula given by (3.47) until the duty ratio increases to D_{crit}, and tracks the CCM formula, $V_O/V_S = D$, thereafter.

It is worthwhile to note that the converter remains in CCM operation for all $0 < D < 1$, if the condition

$$\frac{2L}{RT_s} > 1 \tag{3.52}$$

is satisfied. This condition is derived from

$$D_{crit} = 1 - \frac{2L}{RT_s} < 0 \tag{3.53}$$

which negates the existence of $D_{crit} > 0$.

■ EXAMPLE 3.9 Buck Converter Example

This example shows the case where the converter retains the CCM operation for $0 < D < 1$. For the buck converter used in the previous examples with the circuit parameters of $L = 40\ \mu$H, $R = 1\ \Omega$, and $T_s = 20\ \mu$s, it follows that

$$\frac{2L}{RT_s} = \frac{2 \cdot 40 \times 10^{-6}}{1 \cdot 20 \times 10^{-6}} = 4 > 1$$

indicating that the converter will remain in CCM for all $0 < D < 1$.

As demonstrated in this section, the DCM operation causes significant changes in the operational principles and steady-state characteristics of the buck converter. Furthermore, the DCM operation also alters the dynamic characteristics of the converter. While a detailed analysis of DCM dynamics will be covered later in Chapter 9, it should be reminded that dc-to-dc converters frequently cross the CCM/DCM boundary and therefore should be designed with both CCM and DCM operations in consideration.

3.6 CLOSED-LOOP CONTROL OF BUCK CONVERTER

In real applications, dc-to-dc converters are powered by a non-ideal voltage source rather than a constant dc source. In addition, converters are loaded with general electrical applications, not a resistor. Accordingly, dc-to-dc converters experience certain variations in the input voltage and load current.

As addressed in Chapter 1, a dc-to-dc converter is intended to be a voltage source and, as such, the converter should maintain its output voltage at the desired value, regardless of any changes in the input voltage or load current. This feature is referred to as the output voltage regulation or simply *dc regulation. The term dc regulation implies regulating the output voltage of a converter at a fixed dc value in steady state.*

To implement the dc regulation, a functional connection must be created between the output voltage and duty ratio of the converter. More specifically, a closed-loop feedback control should be employed around the dc-to-dc converter, which adaptively changes the duty ratio of the active switch at the presence of the input voltage and load current variations. This section deals with the dc regulation of a closed-loop controlled buck converter.

Closing a feedback loop is not an easy task and thus requires comprehensive knowledge about modeling, analysis, and control design of dynamic systems. Yet, because the interest of the current section is limited to issues related to the dc regulation, the dynamic modeling, analysis, and control design of dc-to-dc converters are postponed to later chapters.

3.6.1 Closed-Loop Feedback Controller

Figure 3.21 shows a simplified diagram of the buck converter equipped with a closed-loop feedback controller. The feedback controller consists of two functional blocks: the pulsewidth modulation (PWM) block and voltage feedback circuit. The PWM block controls the duty ratio of the active switch using the output of the voltage feedback circuit, labeled as the control voltage v_{con} in Fig. 3.21, and the ramp signal V_{ramp} generated inside the feedback controller. The output of the PWM block is denoted as v_q in Fig. 3.21.

The voltage feedback circuit utilizes the output voltage v_O and reference voltage, denoted as V_{ref} in Fig. 3.21, to generate the control voltage v_{con}. The voltage feedback circuit and PWM block collectively enforce the output of the converter to track the reference voltage in steady state, thereby achieving dc regulation.

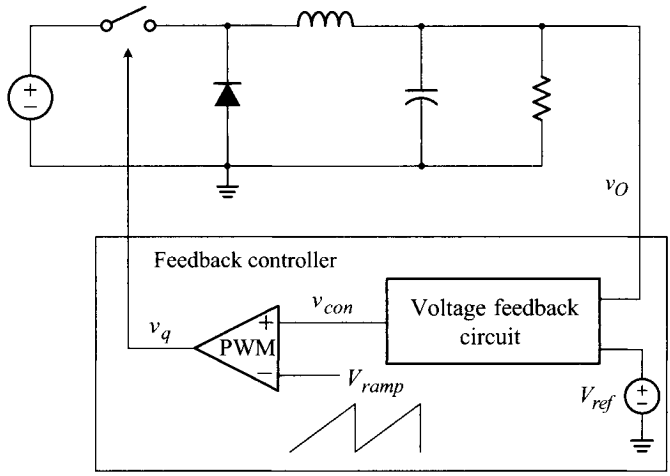


Figure 3.21 Closed-loop controlled buck converter.

Pulsewidth Modulation

The output of the PWM block is the switch drive signal, v_q, whose pulsewidth is modulated to yield the desired duty ratio for the active switch. As shown in Fig. 3.22(a), the PWM block utilizes the control voltage v_{con} and ramp signal V_{ramp}, in order to issue the switch drive signal v_q.

Figure 3.22(b) shows a timing diagram for the PWM waveforms, where the control voltage is assumed to remain constant at $v_{con} = V_{con}$. First, a periodic ramp signal V_{ramp} is generated inside the feedback controller. The period of the ramp signal is in fact the switching period of the converter. The switch drive signal becomes *on* at the instant the ramp signal starts ramping up and resets *off* when the ramp signal intersects with the control voltage. By repeating this process, the PWM block

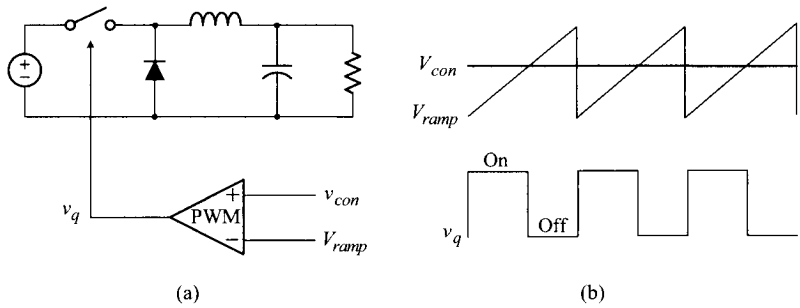


Figure 3.22 PWM block. (a) Block diagram. (b) Timing diagram.

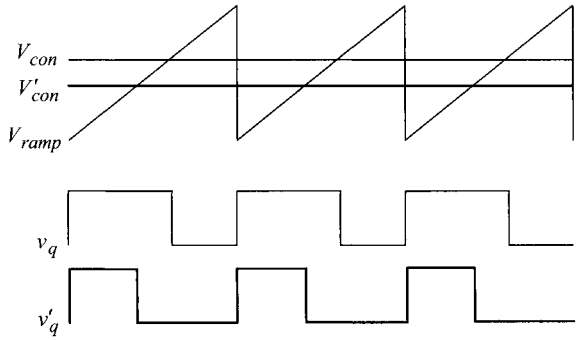


Figure 3.23 Constant-frequency trailing edge modulation.

generates a periodic switch drive signal whose pulsewidth is modulated in proportion to the magnitude of the control voltage, V_{con}.

Figure 3.23 shows the outputs of the PWM block for two different control voltage values, V_{con} and V'_{con}. The modulation scheme generates a switch drive signal whose trailing edge is modulated to change the duty ratio within a fixed switching period. As such, the modulation scheme is called a constant-frequency trailing edge modulation. While many alternative modulation schemes are also available for PWM dc-to-dc converters, this scheme is most widely used and thus adopted as the standard PWM in this book.

Voltage Feedback Circuit

Figure 3.24 shows a simplified diagram of a closed-loop controlled buck converter. The output voltage V_O is fed to a voltage feedback circuit, consisting of an op amp, reference voltage V_{ref}, and two impedance blocks, $Z_1(s)$ and $Z_2(s)$. The output of the voltage feedback circuit is the control voltage, v_{con}, which is used as the input signal for the PWM block.

The voltage feedback circuit operates based on the principle of the negative feedback. When the output voltage V_O grows larger than the nominal value, the output of the op amp, v_{con}, becomes lower than the previous value. With a lowered v_{con}, the PWM block produces the switch drive signal v_q whose duty ratio is reduced. The reduced duty ratio in turn brings down the output voltage to the nominal value.

The mechanism of the dc regulation is explained using the node equation formulated at the inverting terminal of the op amp. Using the *virtual short* between the two input terminals of the op amp, the node equation is written as

$$\frac{V_O - V_{ref}}{Z_1(s)} = \frac{V_{ref} - v_{con}}{Z_2(s)} \tag{3.54}$$

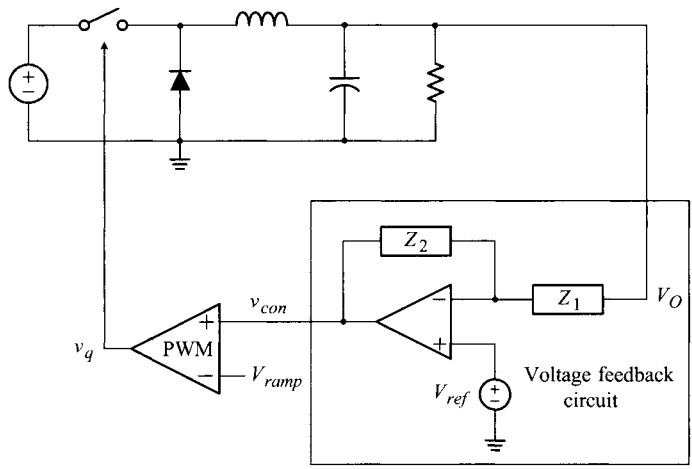


Figure 3.24 Voltage feedback circuit and closed-loop control.

which can be rearranged as

$$\frac{Z_2(s)}{Z_1(s)}\left(V_O - V_{ref}\right) = V_{ref} - v_{con} \tag{3.55}$$

The nature of the dc regulation is deduced from (3.55) as follows.

1) For a proper operation of the converter, the output of the feedback circuit, v_{con}, should have a finite value within the lower and upper bounds of the op amp output voltage.

2) Because both the two variables in the right-hand side of (3.55), V_{ref} and v_{con}, are finite in their magnitude, the term $|Z_2|/|Z_1|(V_O - V_{ref})$ in the left-hand side of the equation should be also finite. Otherwise, the expression (3.55) becomes inconsistent.

3) The steady state is an equilibrium where all the time-varying components of circuit variables settle down to zero and the circuit responds only to dc components. As such, the impedance evaluated at dc, $Z(j0)$, is the factor that determines the steady-state operation of the voltage feedback circuit.

4) If the impedance ratio $|Z_2(j0)|/|Z_1(j0)|$ is selected to be infinite, the variable $(V_{ref} - V_O)$ should converge to zero in order to make their product finite

$$\frac{|Z_2(j0)|}{|Z_1(j0)|}(V_O - V_{ref}) = \infty \cdot 0 \;\Rightarrow\; \text{a finite constant}$$

This condition implies $V_O = V_{ref}$ in steady state, thereby achieving the dc regulation.

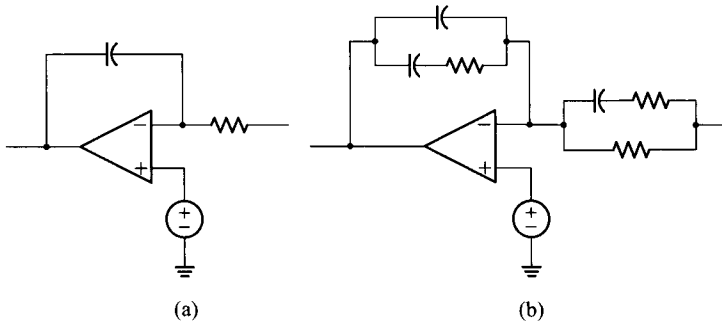


Figure 3.25 Voltage feedback circuits. (a) Miller integrator. (b) Three-pole two-zero circuit.

In conclusion, a voltage feedback circuit that satisfies the following condition

$$\frac{|Z_2(j0)|}{|Z_1(j0)|} = \infty \tag{3.56}$$

forces the output voltage to track the reference voltage in steady state. Accordingly, any circuit that meets the condition (3.56) provides dc regulation, thus eligible for a voltage feedback circuit. The simplest among these is Miller integrator shown in Fig. 3.25(a). However, a voltage feedback circuit employing Miller integrator in its original form does not provide good dynamic performance for reasons that will be discussed in Chapter 8. Consequently, a simple Miller integrator is rarely used for high performance designs.

As will be demonstrated in Chapter 8, it has been established from the past researches that a three-pole two-zero circuit shown in Fig. 3.25(b) is the optimal feedback circuit for the buck converter. The three-pole two-zero circuit, named so after its transfer function, provides excellent dynamic performance as well as tight dc regulation. It is easy to confirm that the three-pole two-zero circuit meets the requirement of (3.56). Because the design of voltage feedback circuit requires comprehensive knowledge about dynamic modeling and frequency-domain analysis, this topic will be treated separately in Chapter 8.

3.6.2 Responses of Closed-Loop Controlled Buck Converter

This section presents the time-domain response of a closed-loop controlled buck converter obtained from PSpice®simulations. Figure 3.26 shows the schematic diagram of a closed-loop controlled buck converter. The power stage parameters are identical to those of the buck converter used in the previous examples, however, the input voltage V_S and load resistance R are allowed to change during the converter operation, in order to investigate transient responses.

The output of the converter is regulated at $V_O = V_{ref} = 4$ V, and the switching frequency is $f_s = 1/20 \times 10^{-6} = 50$ kHz. The ramp signal varies from 0 to 3.8 V. A three-pole two-zero circuit is employed as the voltage feedback circuit. The

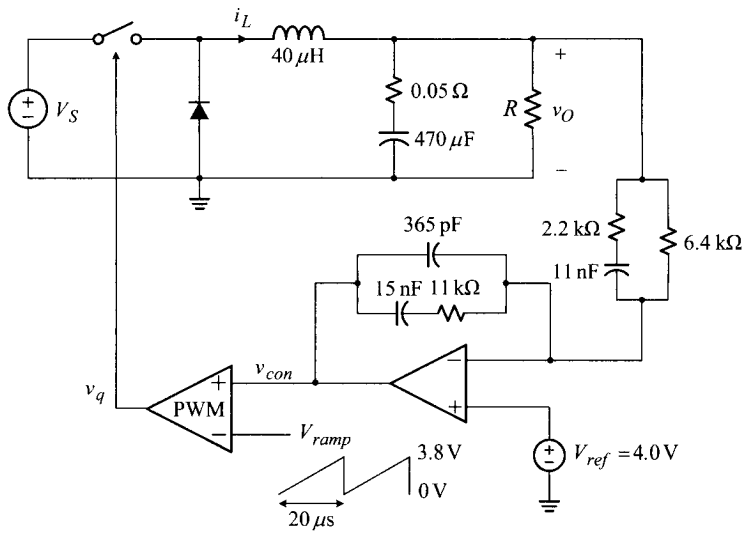


Figure 3.26 Closed-loop controlled buck converter.

circuit parameters for the voltage feedback circuit are optimally selected for good closed-loop performance, as will be demonstrated in Chapter 8.

Step Input Response

The buck converter undergoes a series of step changes in its input voltage, whereas the load resistance is fixed at $R = 1\ \Omega$. As shown in Fig. 3.27, the input voltage is changed as $V_S = 16\ \text{V} \Rightarrow 8\ \text{V} \Rightarrow 16\ \text{V}$ during the converter operation. First, the steady-state waveforms of the converter with $V_S = 16$ V are analyzed. The output voltage v_O is regulated at 4 V with a small ripple component. The inductor current i_L is a triangular waveform. The average value of the inductor current equals to the load current

$$I_L = \frac{V_O}{R} = \frac{4}{1} = 4\ \text{A}$$

The ripple component of the inductor current is given by

$$\Delta i_L = \frac{V_S - V_O}{L} DT_s = \frac{16-4}{40 \times 10^{-6}} \frac{4}{16} 20 \times 10^{-6} = 1.5\ \text{A}$$

The control voltage v_{con} and ramp signal V_{ramp} are simultaneously shown in the third plot in Fig. 3.27, while the switch drive signal v_q is displayed in the bottom plot.

The average value for the control voltage can be evaluated from the PWM waveforms shown in Fig. 3.28. From the PWM waveforms, it can be seen that

$$T_s : DT_s = V_m : V_{con} \tag{3.57}$$

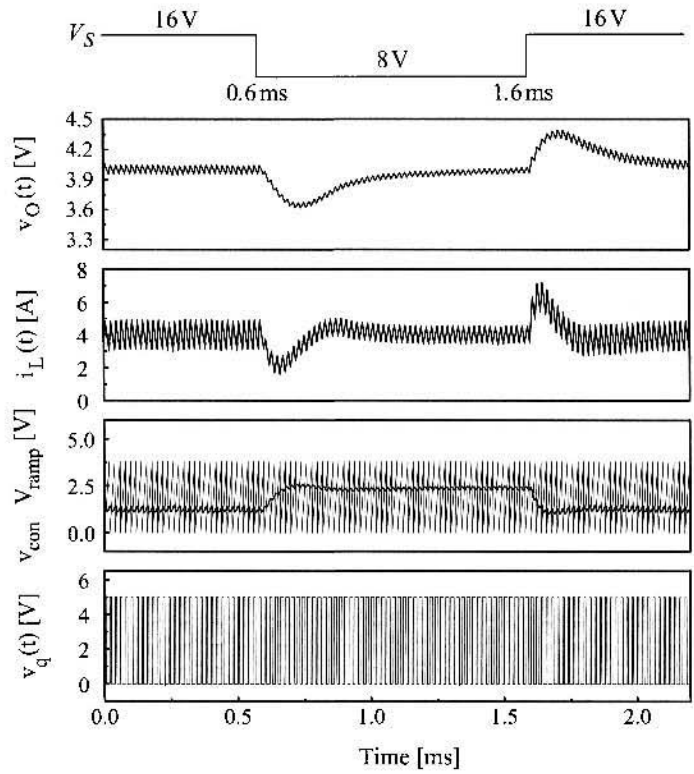


Figure 3.27 Step input response of buck converter: output voltage v_O, inductor current i_L, control voltage v_{con} and ramp signal V_{ramp}, and switch drive signal v_q.

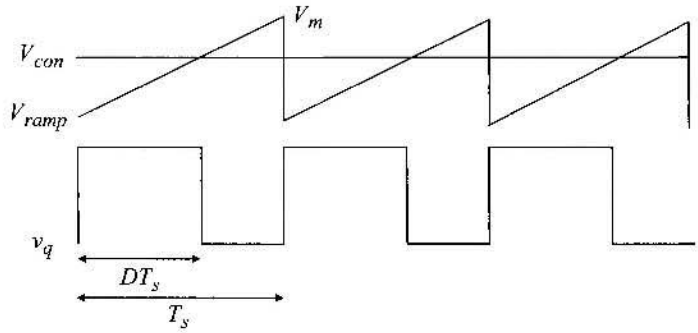


Figure 3.28 PWM block waveforms.

where V_m represents the magnitude of the ramp signal and V_{con} is the steady-state control voltage. The above expression is simplified to $V_{con} = DV_m$. With the given operational conditions, the initial value for the control voltage is evaluated as

$$V_{con} = DV_m = \frac{V_O}{V_S} V_m = \frac{4}{16} 3.8 = 0.95 \text{ V}$$

The control voltage contains a ripple component on top of the dc value evaluated above. The switch drive signal v_q shows the duty ratio of the active switch. The ramp signal, control voltage, and switch drive signal altogether demonstrate the principles of the PWM control.

When the input voltage steps down from 16 V to 8 V at $t = 0.6$ ms, several changes occur in the converter waveforms. First, the output voltage exhibits a transitional undershoot before it returns to the nominal value $V_O = 4$ V. Upon a sudden decrease in V_S, the feedback controller responds to the change with a certain response time. Before the feedback controller establishes a new steady state, the change in the input voltage influences the output voltage as follows. When the input voltage is reduced, the energy delivered from the input source to the output capacitor is also reduced, incurring an energy deficit in the output capacitor. This energy deficit causes the capacitor voltage to drop, resulting in a transitional undershoot in the output voltage. As time elapses, the feedback controller establishes a new steady state and the output voltage tracks back to the nominal value. The behavior of the inductor current can be similarly explained.

With the reduced input voltage $V_S = 8$ V, the ripple component of the inductor current is decreased to

$$\Delta i_L = \frac{V_S - V_O}{L} DT_s = \frac{8 - 4}{40 \times 10^{-6}} \frac{4}{8} 20 \times 10^{-6} = 1 \text{ A}$$

The control voltage gradually increases to produce a larger duty ratio, required to regulate the output voltage with the reduced input voltage. The new value for the control voltage is determined as

$$V_{con} = \frac{V_O}{V_S} V_m = \frac{4}{8} 3.8 = 1.9 \text{ V}$$

The duty ratio of the switch drive signal also gradually grows based on the PWM principle.

The transient behavior of the converter due to a step increase in the input voltage can be interpreted in the opposite way to the step-down case. The instantaneous increase of the input voltage causes the output voltage and inductor current to go through a transitional overshoot until the feedback controller settles into a new steady-state equilibrium. As the control signal gradually decreases, thereby reducing the duty ratio to $D = 4/16 = 0.25$, the output voltage returns to the nominal value.

The buck converter exhibits very stable and well-controlled transient behavior. In fact, the feedback circuit parameters are carefully selected to result in optimal transient behavior. Detailed discussions about the feedback circuit parameters will be given in Chapter 8.

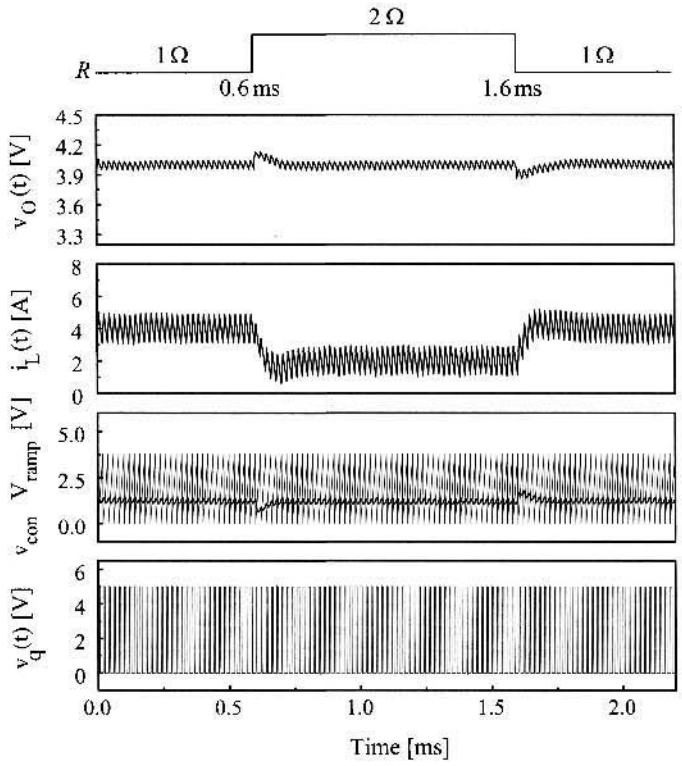


Figure 3.29 Step load response of buck converter.

Step Load Response

Now the converter goes through a series of step changes in the load resistance, $R = 1\ \Omega \Rightarrow 2\ \Omega \Rightarrow 1\ \Omega$, while the input voltage is fixed at $V_S = 16$ V. The pattern of the step changes and the simulated waveforms are shown in Fig. 3.29. With a step load change from $R = 1\ \Omega$ to $2\ \Omega$ at $t = 0.6$ ms, the energy release from the capacitor to the load resistor suddenly becomes smaller than the previous value, thereby resulting in an energy surplus at the output capacitor. Accordingly, the capacitor voltage momentarily exceeds the nominal value, thereby producing an output voltage overshoot. The inductor current clearly shows a decrease in the load current. The inductor current indicates that the converter still remains in CCM operation with $R = 2\ \Omega$. The resistance that places the converter on the borderline between CCM and DCM operations is given by

$$R_{crit} = \frac{2L}{(1-D)T_s} = \frac{2 \cdot 40 \times 10^{-6}}{(1-0.25)\,20 \times 10^{-6}} = 5.33\ \Omega$$

Figure 3.29 also shows the transient waveforms of the control voltage and switch drive signal. After passing through a short transition period, the control voltage and switch drive signal return to their original waveforms – the duty ratio is invariant to the load resistance value, as far as the converter operates in CCM while retaining the output voltage regulation.

The transient behavior in response to the step load change from $R = 2\ \Omega$ to $1\ \Omega$ can be understood in the opposite way to the previous case. In this case, the output voltage exhibits an undershoot due to the transitional energy deficit.

Operational Mode Change Response

For this case, the load resistance temporarily steps up to a higher value, $R = 8\ \Omega$, well above the critical value of $R_{crit} = 5.3\ \Omega$, while the input voltage remains constant at $V_S = 16$ V. The converter is expected to undergo transitions in the operational mode because it crosses the CCM/DCM boundary. The simulated transient responses of the converter are shown in Fig. 3.30.

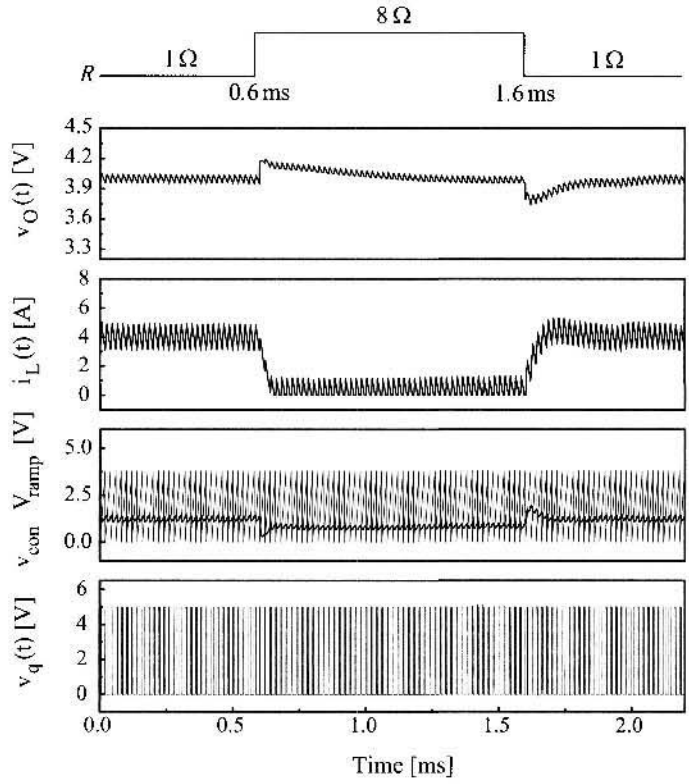


Figure 3.30 Operational mode change response of buck converter.

With the step increase from $R = 1\ \Omega$ to $8\ \Omega$ at $t = 0.6$ ms, the output voltage exhibits an overshoot, and at the same time the converter enters a DCM operation within a few switching cycles, as demonstrated by the inductor current waveform. The output voltage then gradually settles to the target value $V_O = 4$ V because the feedback controller guarantees dc regulation regardless of the change in the operational mode. It is important to notice that, unlike the previous step load response case where the converter remains in CCM operation all the time and the control voltage retains the same value in steady state, the values of both the control voltage and duty ratio decrease when the converter enters DCM operation. This is because the gain formula in DCM operation differs from the CCM case. As such, the converter must settle in a new duty ratio pertinent to the DCM operation. In fact, the DCM gain is larger than the CCM gain for the same duty ratio. Thus, when the converter enters DCM operation, the duty ratio should be lessened to produce the same output voltage, as shown in Fig. 3.30. With the step decrease in the load resistance from $8\ \Omega$ to $1\ \Omega$ at $t = 1.6$ ms, the converter returns to CCM operation after a short transition period.

3.7 SUMMARY

A step-down dc-to-dc power conversion is achieved by altering a dc input into a rectangular waveform and filtering the resulting rectangular waveform into a dc output. The buck converter is the simplest circuit that can perform the step-down dc-to-dc power conversion.

The buck converter employs an active-passive switch pair and LC low pass filter. The output of a buck converter contains a ripple component. However, the magnitude of the ripple component is so small that the output voltage can be considered as a pure dc, given by the product of the input voltage and the duty ratio of the active switch – this presumption is called the small-ripple approximation. The small-ripple approximation is very useful for the steady-state analysis.

The piecewise linear analysis is adapted to describe the circuit behavior of the buck converter during the start-up transient period and in steady state. In the piecewise linear analysis, the converter is decomposed into the on-time and off-time subcircuits. The operation of the converter is investigated by studying each subcircuit individually and later considering the behavior of the two subcircuits collectively. The piecewise linear analysis, when applied along with the small-ripple approximation, readily offers accurate predictions for the steady-state converter waveforms. Readers will further appreciate the usefulness of this analysis method in the next chapter which deals with various dc-to-dc converter circuits.

The performance of a dc-to-dc converter is influenced by the non-ideal characteristics of the circuit components. In particular, the equivalent series resistance (esr) of the output capacitor determines the magnitude of the output ripple. Furthermore, it will be shown in Chapter 6 that the esr of the output capacitor has rather significant impacts on the dynamic characteristics of the converter.

Most dc-to-dc converters employ unidirectional switches which only deliver the current in one direction. Accordingly, the switch current cannot alter its direction

regardless of any changes in operational conditions. This constraint forces dc-to-dc converters to move into a new operational mode, referred to as a discontinuous conduction mode (DCM), when the operational conditions cross certain boundaries. In DCM operation, there exists a time interval in which the inductor current stays at zero value. The converter operation in DCM differs from the continuous conduction mode (CCM) operation in which the inductor current is present all the time. This operational difference causes notable changes in the steady-state characteristics and transient response of the converter.

A dc-to-dc converter should provide a fixed output voltage for all the operational conditions. For this purpose, the feedback control is employed to adaptively adjust the duty ratio so that the converter produces a desired output voltage regardless of the changes in the input voltage, load current, or operational mode – CCM or DCM. The feedback controller consists of the PWM block and voltage feedback circuit. The PWM block generates a pulsewidth-modulated switch drive signal, using the control voltage provided by the voltage feedback circuit. To regulate the output voltage at a fixed value, the voltage feedback circuit should satisfy the specific condition given by (3.56), $|Z_2(j0)|/|Z_1(j0)| = \infty$, as is the case with the three-pole two-zero circuit shown in Fig. 3.25(b).

PSpice®simulations have proved very useful in visualizing converter operations and substantiating theoretical predictions. The simulations shown in Section 3.6.2 provide valuable insights on both steady-state and transient responses of a closed-loop controlled PWM dc-to-dc converter.

REFERENCES

1. R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, Kluwer Academic Publishers, 2001.

2. L. Dixon, "Spice Simulation of Switching Power Supply Performance," Unitrode Power Supply Design Seminar Manual: SEM-800, pp.1-1–1-14, 1991.

3. D. W. Hart, *Power Electronics*, McGraw-Hill, New York, NY, 2011.

PROBLEMS

3.1* Listed below are some useful circuit theorems or analysis techniques that are frequently applied to dc-to-dc power conversion circuits. For each item, give a brief description, mathematical expression, or illustrative example.

i) volt-sec balance condition **ii)** amp-sec balance condition
iii) small-ripple approximation **iv)** piecewise linear analysis
v) flux balance condition **vi)** charge balance condition

3.2** A secondary filter stage is added to a conventional buck converter, yielding a buck converter with a two-stage output filter. The resulting buck converter is shown in Fig. P3.2. Circuit analyses reveal that the transfer function of the

two-stage filter can be approximated as

$$\frac{v_o(s)}{v_x(s)} \approx \frac{1}{\left(1 + \frac{s}{Q_1\omega_{o1}} + \frac{s^2}{\omega_{o1}^2}\right)\left(1 + \frac{s}{Q_2\omega_{o2}} + \frac{s^2}{\omega_{o2}^2}\right)}$$

$$Q_1 = R\sqrt{\frac{C_1}{L_1}} \qquad \omega_{o1} = \frac{1}{\sqrt{L_1C_1}}$$

$$Q_2 = R\sqrt{\frac{C_2}{L_2}} \qquad \omega_{o2} = \frac{1}{\sqrt{L_2C_2}}$$

when the conditions $L_1 \gg L_2$ and $C_1 \gg C_2$ are met.

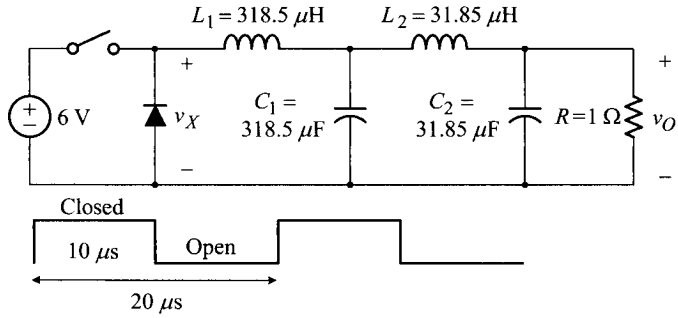


Fig. P3.2

a) Perform the frequency-domain analysis to predict the magnitude of the output voltage ripple at the presence of the two-stage output filter. Consider only the first harmonic component of the output voltage.

b) Now assume that the secondary filter stage is removed, $L_2 = C_2 = 0$. For this case, find new values for L_1 and C_1 so that the converter produces the same output voltage ripple as that of **a)**. Assume $Q_1 = R\sqrt{C_1/L_1} = 1$ for this problem.

c) Based on the results of **a)** and **b)**, state the advantage of using a two-stage output filter rather than a single-stage output filter.

3.3* Shown in Fig. P3.3 is the generic structure of a buck converter. A variety of low-pass filter circuits can be placed inside the Box to accomplish the desired step-down dc-to-dc power conversion. Typical examples are also shown in Fig. P3.3(b). For each low-pass filter circuit, estimate the magnitude of the output voltage ripple by performing the frequency-domain analysis. Consider only the first harmonic component of the output voltage.

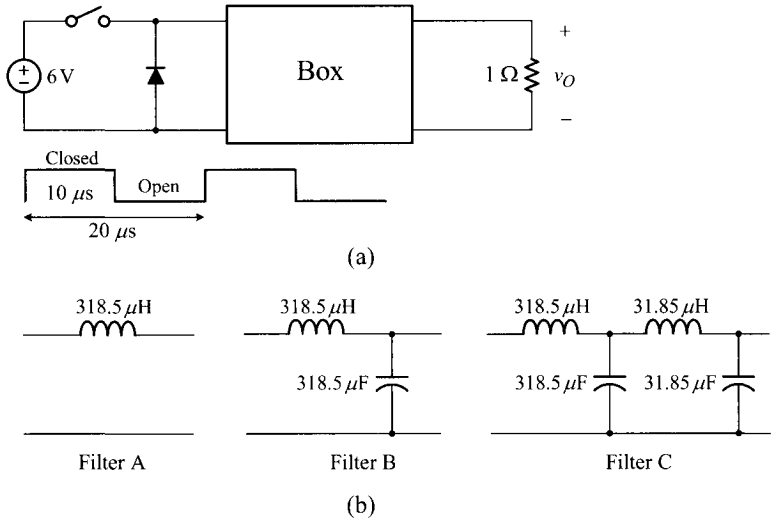


Fig. P3.3

3.4* Figure P3.4 shows a buck converter along with its switch drive signal.

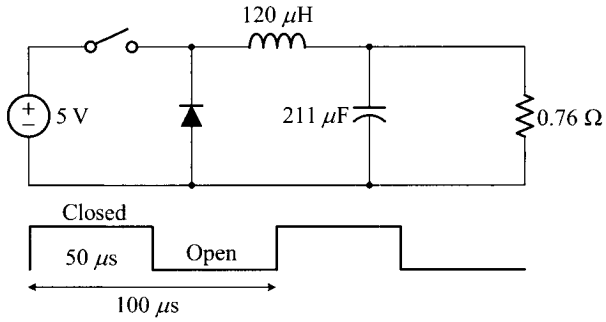


Fig. P3.4

a) Perform the frequency-domain analysis illustrated in Example 3.1, in order to predict the magnitude of the output voltage ripple.

b) Use the equation (3.27) to estimate the size of the output voltage ripple. Compare the result with the outcome of **a)**.

3.5 Consider the circuit diagram of a buck converter and its inductor current waveform, shown in Fig. P3.5.

a) Evaluate the output voltage V_O.

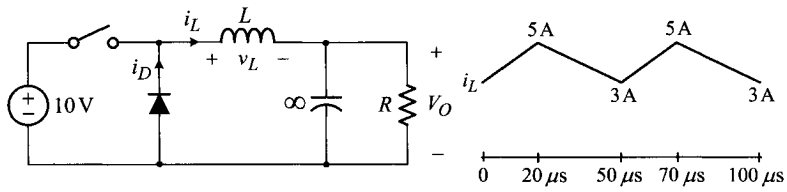


Fig. P3.5

b) Sketch the steady-state waveforms of the inductor voltage v_L and diode current i_D for the two operational periods. Label the maximum and minimum values on your sketch.

c) Evaluate the inductance L and the load resistance R.

3.6** Consider the dc-to-dc conversion system shown in Fig. P3.6. Referring to the switch drive signals for Q_1 and Q_2, answer the questions.

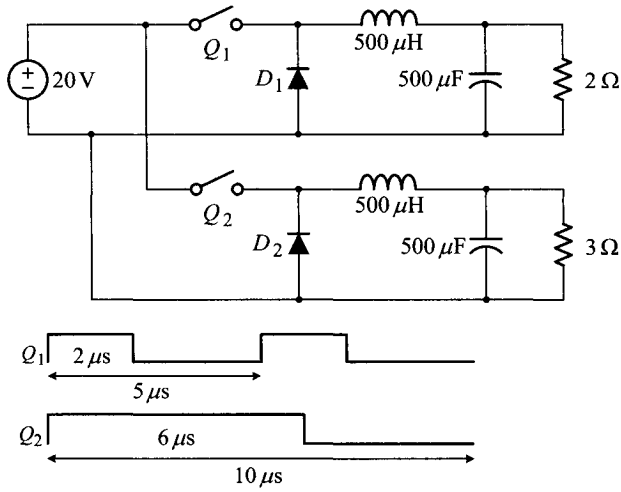


Fig. P3.6

a) First assume that all the circuit components are ideal and the power conversion is performed losslessly. Evaluate the average current flowing through each semiconductor switch, $\bar{i}_{Q1}$, $\bar{i}_{D1}$, $\bar{i}_{Q2}$, and $\bar{i}_{D2}$.

b) Now, assume the following practical devices for the semiconductor switches
Q_1 and Q_2: MOSFET with the channel resistance of $R_{DS}(on) = 0.5\ \Omega$
D_1 and D_2: Schottky diode with the turn-on voltage of $V_D(on) = 0.5$ V
Calculate the average power dissipated at each practical switch.

c) Lastly, estimate the overall efficiency of the system using the following formula

$$\eta \approx \frac{P_{out}}{P_{out} + P_{loss}}$$

where P_{out} is the power delivered to the output resistors and P_{loss} is the sum of the power losses, each evaluated in **b)** for the respective practical switch.

3.7 Figure P3.7 shows two buck converters. Referring to the circuit diagrams, answer the questions.

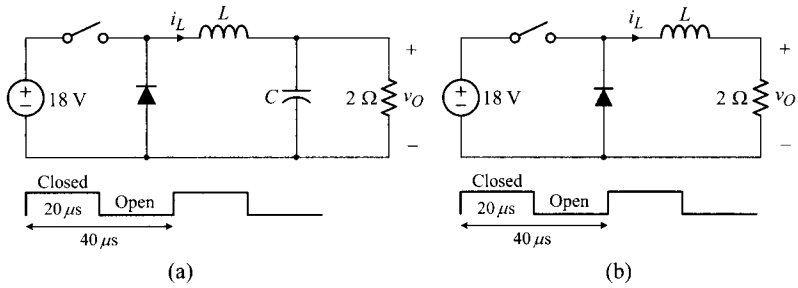


Fig. P3.7

a) For Converter (a), determine the values for L and C to meet the design specifications of $\Delta i_L/I_L = 0.2$ and $\Delta v_O/V_O = 0.02$.

b) For Converter (b), determine the value for L to comply with the design specification of $\Delta v_O/V_O = 0.02$.

3.8** Shown in Fig. P3.8(a) are a buck converter and the Bode plot of its output filter transfer function, $|F_f| = |v_o|/|v_x|$.

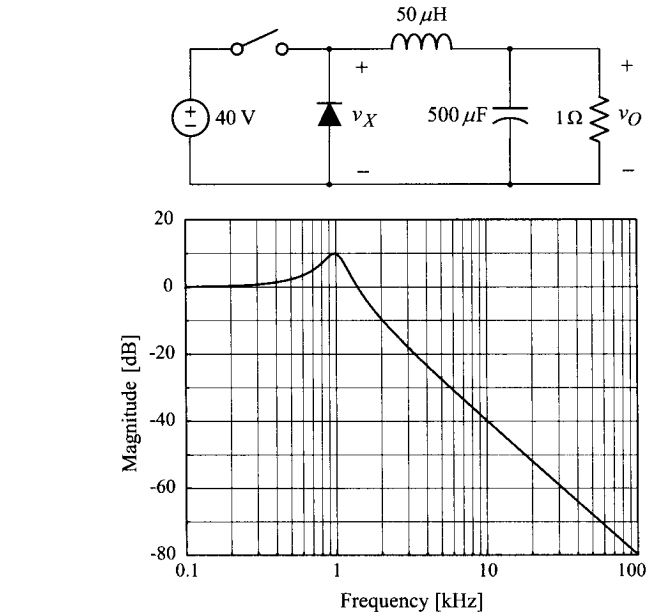
a) Estimate the magnitude of the output voltage ripple when the buck converter operates at 30 kHz with $D = 0.5$. Use the information given in the Bode plot.

b) Now assume the buck converter is modified into two converter circuits shown in Fig. P3.8(b). For each of these two converter circuits, repeat **a)**.

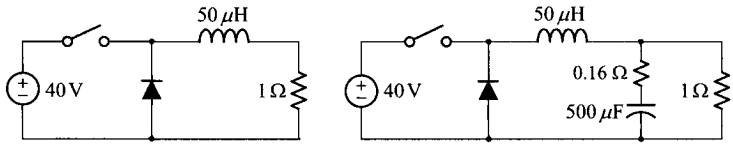
3.9** Figure P3.9 shows the inductor current of a buck converter that operates at the boundary between CCM and DCM.

a) Assume that the converter operates in an open-loop condition with a fixed duty ratio. The load resistance is increased beyond the critical value that places the converter at the CCM/DCM borderline, while the input voltage remains the same. Sketch a family of inductor currents, each with a different load resistance, to illustrate the transition pattern of the inductor current as the load resistance is increased.

b) The converter is now closed-loop controlled, thereby achieving output voltage regulation, and again operates at the CCM/DCM boundary. Assuming the load resistance is increased beyond the critical value, while the input voltage remains the same, sketch a family of inductor currents to show the change in the inductor current.



(a)



(b)

Fig. P3.8

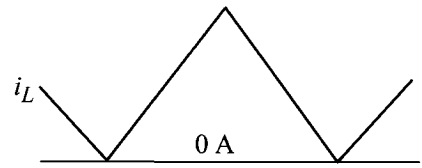


Fig. P3.9

c) Again assume the closed-loop control and the borderline operation for the converter. For this case, the input voltage is increased beyond the critical value for the CCM/DCM boundary, while the load resistance remains the same. Sketch a family of the inductor currents that exhibits the transition of the inductor current as the input voltage is increased.

3.10* Consider the three buck converters shown in Fig. P3.10 and answer the questions. The common switch signal is applied to the three converters.

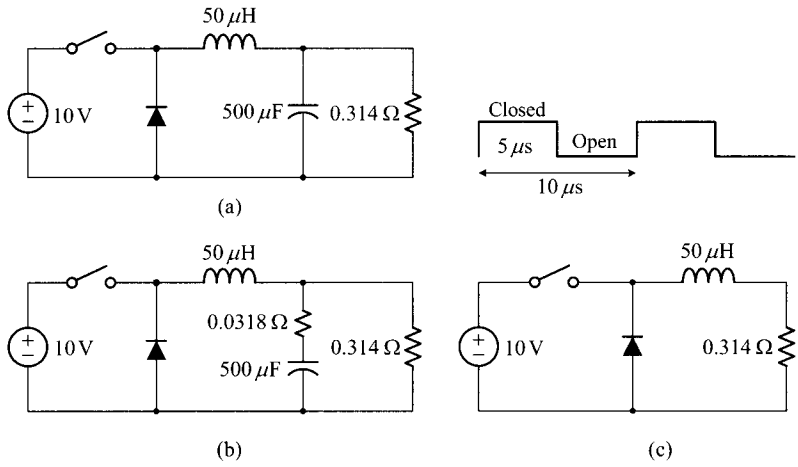


Fig. P3.10

a) For each converter circuit, perform the frequency-domain analysis to predict the magnitude of the output voltage ripple.

b) Now, perform the time-domain analysis to estimate the magnitude of the output voltage ripple of each converter.

3.11 Referring to the buck converter in Fig. P3.11, answer the following questions.

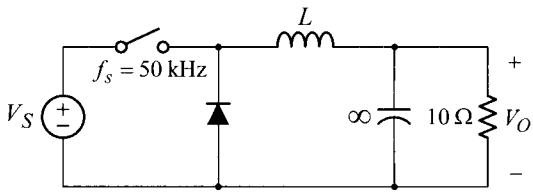


Fig. P3.11

a) Determine the inductance L so that the converter operates at the CCM/DCM borderline with $D = 0.6$.

b) Find the minimum inductance L that ensures CCM operation of the converter for all $0 < D < 1$.

c) Now assume $L = 60\,\mu$H and sketch the general shape of the dc voltage gain curve, V_O/V_S vs. D, for all $0 < D < 1$.

3.12 Figure P3.12 shows a family of voltage conversion curves of a buck converter, as a function of the duty ratio D and dimensionless parameter $\tau = 2L/(RT_s)$. The converter operates with $T_s = 20\,\mu$s.

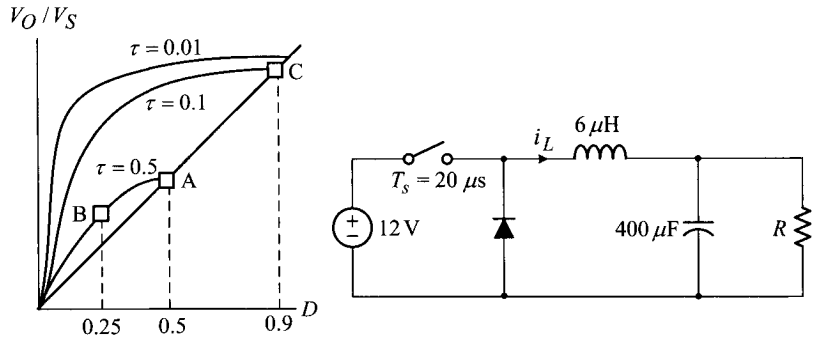


Fig. P3.12

a) Sketch the steady-state waveform of i_L when the operational condition of the converter is located at Point A. Show the maximum, minimum, and average values of the waveform on your sketch.

b) Assume that the operational condition is located at Point B, and repeat **a)**.

c) Repeat **a)** for Point C.

3.13* Shown in Fig. P3.13 are the circuit diagram of a buck converter and its inductor current waveform.

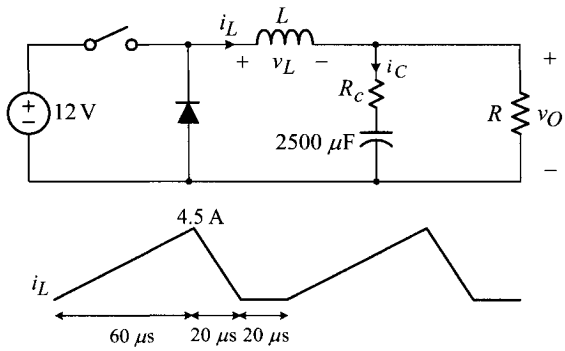


Fig. P3.13

a) Referring to the inductor current i_L, sketch the inductor voltage v_L for the two switching periods. Show the maximum and minimum values on your sketch.

b) Find values for the inductance L and resistance R.

c) Sketch the capacitor current i_C for the two switching periods. Show the maximum and minimum values.

d) Evaluate the output voltage ripple Δv_O when $R_c = 0.12\ \Omega$. Assume $C = 2500\ \mu$F is sufficiently large.

e) Evaluate Δv_O when $R_c = 0$.

3.14* Figure P3.14 shows two different buck converters. Converter (a) operates in an open-loop fashion while Converter (b) operates with a closed-loop control.

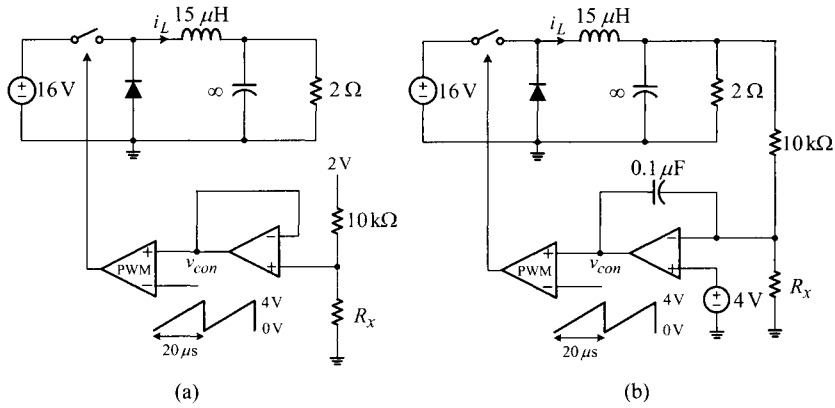


Fig. P3.14

a) For Converter (a), answer the following questions.
i) Assume $R_x = \infty$ and sketch the steady-state waveforms of i_L and v_{con} for the two operational periods.
ii) Now assume $R_x = 10$ kΩ and repeat **i)**.

b) Repeat **a)** for Converter (b).

3.15* Consider the closed-loop controlled buck converter shown in Fig. P3.15 and answer the questions. Assume $R_1 = \infty$ for Problems **a)** and **b)**.

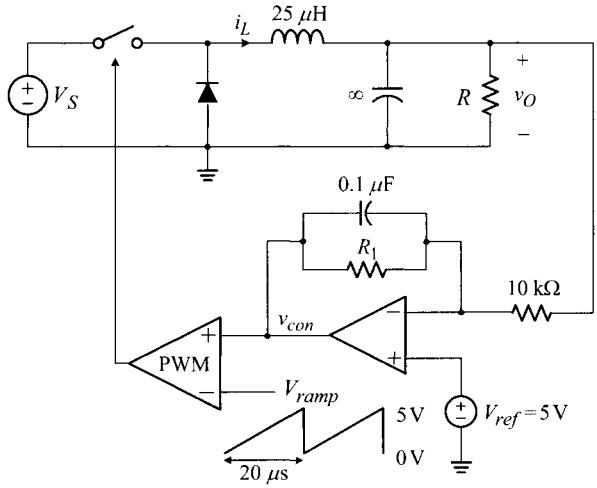


Fig. P3.15

a) With $V_S = 20$ V, $R = 1\ \Omega$, and $R_1 = \infty$, sketch the steady-state waveforms of the inductor current i_L and control voltage v_{con} for the two switching periods. Label the maximum and minimum values on your sketches.

b) When the operational conditions of the converter are varied as $15\text{ V} < V_S < 25\text{ V}$ and $0.5\ \Omega < R < 2\ \Omega$ with $R_1 = \infty$, find the range of the control voltage v_{con} for the entire operating range: ( ) $< v_{con} <$ ( ).

Now assume $R_1 = 10\text{ k}\Omega$ for Problems **c)** and **d)**.

c) With $R_1 = 10\text{ k}\Omega$, the converter fails to achieve dc regulation. Explain the reason for this.

d) When $V_S = 20$ V and $R = 1\ \Omega$ with $R_1 = 10\text{ k}\Omega$, find the steady-state values of the output voltage v_O and control voltage v_{con}.

3.16 Figure P3.16 shows a closed-loop controlled buck converter and its voltage gain curve. Answer the following questions.

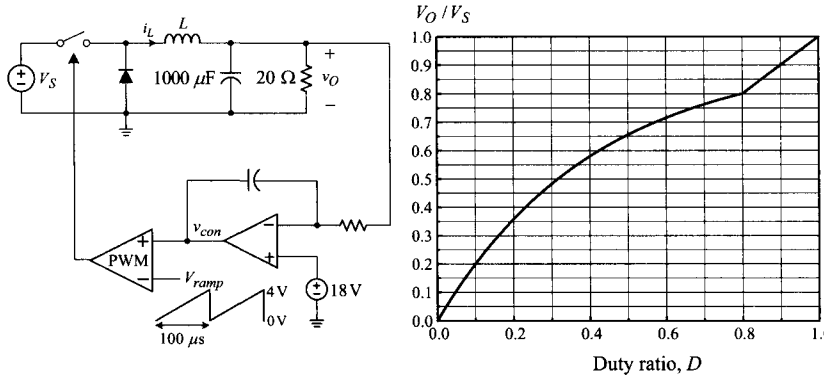


Fig. P3.16

a) Find the ranges for the duty ratio D and control voltage v_{con}, when the input voltage is varied between $20\text{ V} < V_S < 60\text{ V}$.

b) Find the inductance of the filter inductor L.

c) Sketch the inductor current i_L for the two switching periods for the three cases of $V_S = 20$ V, $V_S = 22.5$ V, and $V_S = 60$ V. Show the maximum and minimum values of i_L.

3.17** Consider the buck converter shown in Fig. P3.17 and answer the following questions.

a) Assume that the input voltage is varied between $8\text{ V} < V_S < 20\text{ V}$. For this condition, the converter could operate in either CCM or DCM, depending on the input voltage range. Fill in the blanks in the following descriptions which summarize the operation of the closed-loop controlled buck converter.

i) The converter operates in CCM for ( ) $< V_S <$ ( ) and the control voltage varies between ( ) $< v_{con} <$ ( ) in this CCM operation.

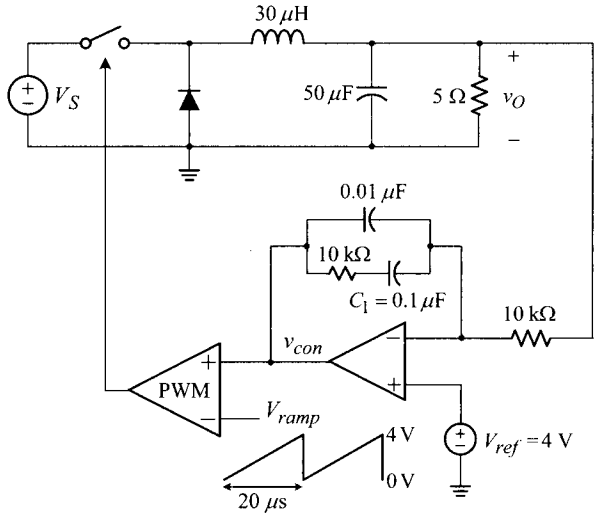


Fig. P3.17

ii) The converter operates in DCM for ( ) < V_S < ( ) and the control voltage varies between ( ) < v_{con} < ( ) in this DCM operation.

b) Now assume V_S = 10 V and answer the questions.

i) Find the steady-state values of the output voltage v_O and control voltage v_{con}.

ii) Assume that the capacitor C_1 is accidentally open-circuited. Do you expect any change in the steady-state waveform of v_O or v_{con}? If you do not expect any change, give the reason for your claim. If you do predict a change in v_O or v_{con}, evaluate the average value of the corresponding waveform in the new steady state.

iii) Assume the compensation capacitor C_1 is accidentally short-circuited and repeat **ii)**.

3.18 Shown in Fig. P3.18 are the transient responses of the major circuit waveforms of a closed-loop controlled buck converter. Case (a) is the transient response of the inductor current i_L and control voltage v_{con} in response to the step changes in the input voltage, $V_{S1} \Rightarrow V_{S2} \Rightarrow V_{S1}$ with $V_{S1} > V_{S2}$. Case (b) is the transient responses due to the step changes in the load resistor, $R_1 \Rightarrow R_2 \Rightarrow R_1$ with $R_1 < R_2$.

Table P3.18 summarizes 1) the prominent behavior of the inductor current i_L and control voltage v_{con}, observed in the period circled on the corresponding circuit waveform, and 2) a brief explanation for the cause/origin of the respective circuit behavior. Based on the given information and operational principle of the converter, fill in the blanks in Table P3.18.

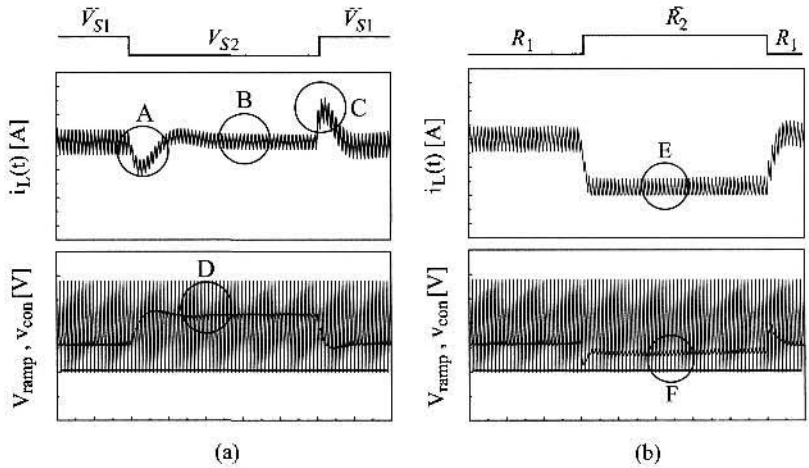


Fig. P3.18

Table P3.18

Circled period	Observed behavior	Cause/origin of behavior
A	undershoot in i_L	( )
B	decrease in the ripple of i_L	( )
C	overshoot in i_L	( )
D	increase in v_{con}	( )
E	discontinuity in i_L	DCM operation with $R > R_{crit}$
F	decrease in v_{con}	( )

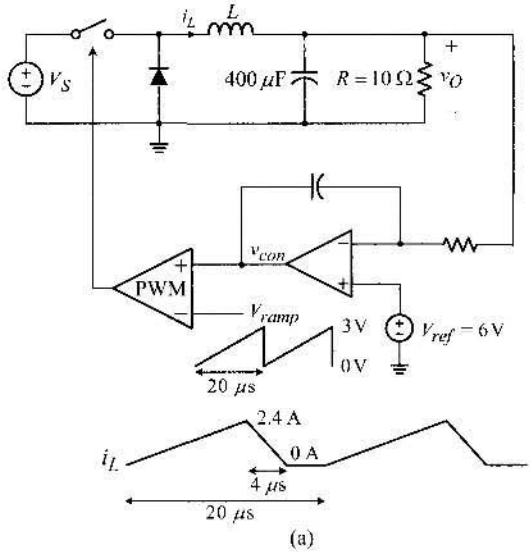
3.19* Figure P3.19 shows a closed-loop controlled buck converter and its inductor current waveform.

a) Referring to the information given in the circuit diagram and inductor current i_L in Fig. P3.19(a), find values for the inductance L, control voltage v_{con}, input voltage V_S, and output voltage ripple Δv_O.

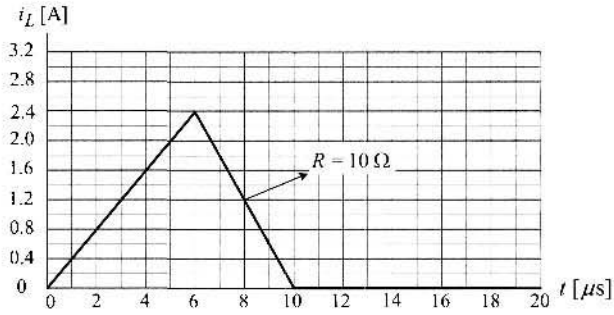
b) Shown in Fig. P3.19(b) is the inductor current of the converter with $R = 10\ \Omega$. Assume that the load resistance is increased to $R = 40\ \Omega$ while the other circuit parameters retain the values you found in **a)**. Under this assumption, sketch the inductor current i_L. Use Fig. P3.19(b) as a reference to show the steps of constructing the new inductor current waveform.

c) Repeat **b)** for $R = 90\ \Omega$.

d) Now assume that the input voltage is increased to $V_S = 16$ V while the load resistor retains the original value of $R = 10\ \Omega$. Under this assumption, sketch the inductor i_L using Fig. P3.19(b) as a reference.


i_L
L
V_S
400 μF
$R = 10\,\Omega$
v_O
v_{con}
PWM
V_{ramp}
3 V
0 V
$V_{ref} = 6$ V
20 μs
2.4 A
0 A
i_L
4 μs
20 μs

(a)


i_L [A]
3.2
2.8
2.4
2.0
1.6
1.2
0.8
0.4
0
0 2 4 6 8 10 12 14 16 18 20
t [μs]
$R = 10\,\Omega$

(b)

Fig. P3.19

CHAPTER 4

DC-TO-DC POWER CONVERTER CIRCUITS

Numerous dc-to-dc converters are currently being employed in various electronic equipment and systems. These converters outwardly look so varied in their topologies and operations that the diversity of dc-to-dc converters is seemingly amazing, even mysterious. Despite the variety and dissimilarity in topological structures, most dc-to-dc converters have evolved from the *three basic converters* known as the buck converter, boost converter, and buck/boost converter. Furthermore, among these three basic converters, the buck converter is the forerunner of the other two converters – specifically, the boost converter is derived, at least in its functional abstraction, from the buck converter and the buck/boost converter is created by combining the buck converter and boost converter. The buck converter was studied in the previous chapter.

In this chapter, we study an important class of dc-to-dc converters including the boost converter, buck/boost converter, and other converters derived from the three basic converters. For each converter, the origin of the circuit topology is first illustrated by showing how the converter circuit has evolved from its respective forerunning converter. This chapter then investigates the operational details of the converter and presents steady-state waveforms for both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) operations. Because the feedback controller

Pulsewidth Modulated Dc-to-Dc Power Conversion. By Byungcho Choi

covered in Section 3.6.1 is commonly applicable to all the PWM dc-to-dc converters, the current chapter only deals with the power stage operation.

There are many ways to classify dc-to-dc converters, each with a different criterion for classification. One way is to divide PWM dc-to-dc converters into non-isolated converters and isolated converters. In a non-isolated converter, the input port of the converter shares a common ground with the output port of the converter. The buck converter is an example of the non-isolated converter. On the other hand, in an isolated converter, the input and output ports of the converter are electrically isolated. A transformer is commonly used to provide the galvanic isolation. In this chapter, we study the important classes of non-isolated and isolated dc-to-dc converters.

4.1 BOOST CONVERTER

The boost converter is a step-up dc-to-dc power conversion circuit that invariably produces a higher output voltage than the input voltage. In this section, the topological structure of the boost converter is first analyzed. The steady-state operation in both CCM and DCM is then investigated using the analysis techniques established in Chapter 3.

4.1.1 Evolution to Boost Converter

The boost converter can be viewed as a modification of the buck converter, specially configured to offer a larger output voltage than the input voltage. Figure 4.1 illustrates the procedure of transforming the buck converter into the boost converter through steps of circuit manipulations. The buck converter is shown in Fig. 4.1(a) where **a** represents the node to which the active switch is connected, while **p** is the node where the passive switch is present. Figure 4.1(a) is transformed to Fig. 4.1(b) by replacing the active-passive switch pair with a single-pole double-throw (SPDT) switch. The SPDT switch is connected to **a** for DT_s and **p** for $(1 - D)T_s$. As shown in Fig. 4.1(b), the circuit is partitioned into the source section, middle section, and load section. The middle section includes the SPDT switch and inductor. Referring to the voltage across the left-hand side of the middle section as v_1 and that of the right-hand side as v_2, the volt-sec balance condition is applied to the inductor

$$(v_1 - v_2)DT_s = v_2(1 - D)T_s \tag{4.1}$$

resulting in

$$v_2 = v_1 D \tag{4.2}$$

As the first step of the circuit manipulation, one can interchange the location of the source section and load section, while keeping the middle section unchanged, as shown in Fig. 4.1(c). With this modification, v_2 can be viewed as the input voltage associated with the source section, while v_1 becomes the output voltage across the load section. Now, the following two facts need to be kept in mind before continuing the circuit manipulation.

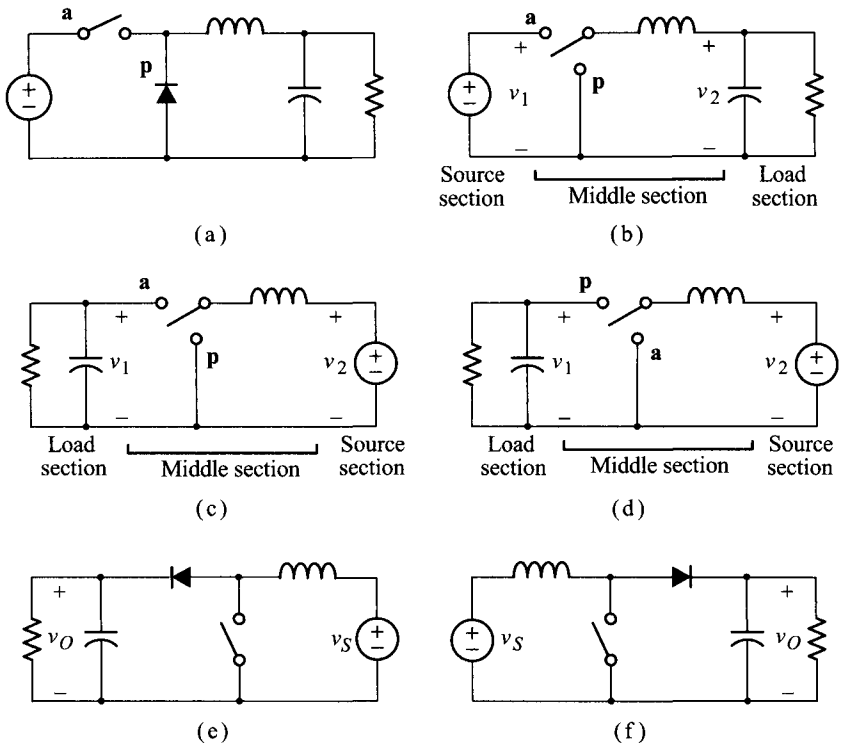


Figure 4.1 Derivation of boost converter. (a) Buck converter. (b) Alternative representation. (c) Interchange of source section and load section. (d) Interchange of passive switch and active switch. (e) Realization of SPDT switch. (f) Boost converter.

1) The relation (4.2), derived from the volt-sec balance condition on the inductor, is also valid in Fig. 4.1(c), regardless of the position change between the source and load sections.

2) The parameter D in (4.2) denotes the fraction of the switching period in which the SPDT switch is connected to the positive side of v_1.

As the second step, for the purpose of allowing energy flow from the source section to load section, the locations of the active and passive switches are interchanged,† resulting in the circuit shown in Fig. 4.1(d). Here, the fraction of the switching period

†For proper operation as a dc-to-dc converter, the circuit should transfer energy from the source section to the inductor when the active switch is turned-on, and release the transferred energy to the load section when the active switch is turned-off. Although the on-time energy transfer is achieved in Fig. 4.1(c), the off-time energy release is not feasible. The on-time energy transfer and off-time energy release both become possible when the locations of the active and passive switches are interchanged, as shown in Fig. 4.1(d). Additional discussions about this feature are given in Section 4.3.

in which the SPDT switch resides on the positive side of v_1 is $(1 - D)$ rather than D. Accordingly, the parameter D in (4.2) should be replaced with $(1 - D)$, resulting in a new relationship

$$v_2 = v_1(1 - D) \tag{4.3}$$

Figure 4.1(d) is then transformed to Fig. 4.1(e), where the SPDT switch is represented by an active-passive switch pair, v_1 is renamed as v_O for the output voltage, and v_2 is renamed as v_S for the input voltage. Finally, Fig. 4.1(e) is rearranged into the standard form shown in Fig. 4.1(f). This new converter circuit is called the boost converter because its voltage gain $v_O/v_S = 1/(1 - D)$ is always larger than unity for all $0 < D < 1$, thereby boosting the input voltage to a higher value.

As illustrated above, the boost converter can be viewed as an evolution from the buck converter, created by interchanging the source and load connections and rearranging the switches in such a way that allows energy flow from the source section to the load section. During this modification, the step-up feature of the boost converter has naturally arisen.

4.1.2 Steady-State Analysis in CCM

The steady-state analysis of the boost converter in CCM operation is now performed using the analysis techniques established in Chapter 3.

Steady-State Operation in CCM

Figure 4.2 shows the boost converter, on-time and off-time subcircuits, and major circuit waveforms in CCM operation. The standard techniques used in Chapter 3, such as the small-ripple approximation, flux balance condition, and charge balance condition, are employed in Fig. 4.2. This figure also incorporates that the output voltage is always larger than the input voltage, $V_O > V_S$. The volt-sec balance condition is now applied to the inductor

$$V_S DT_s = (V_O - V_S)(1 - D)T_s \tag{4.4}$$

resulting in the voltage gain expression

$$\frac{V_O}{V_S} = \frac{1}{1 - D} \tag{4.5}$$

The gain expression indicates that the voltage gain increases from unity to infinity when the duty ratio is varied between $0 < D < 1$.

During an on-time period, the inductor current ramps up with a slope V_S/L. Meanwhile, during an off-time period, the inductor current ramps down with a slope $(V_S - V_O)/L$. The excursion of the inductor current is thus determined as

$$\Delta i_L = \frac{V_S}{L} DT_s = \frac{V_O - V_S}{L}(1 - D)T_s \tag{4.6}$$

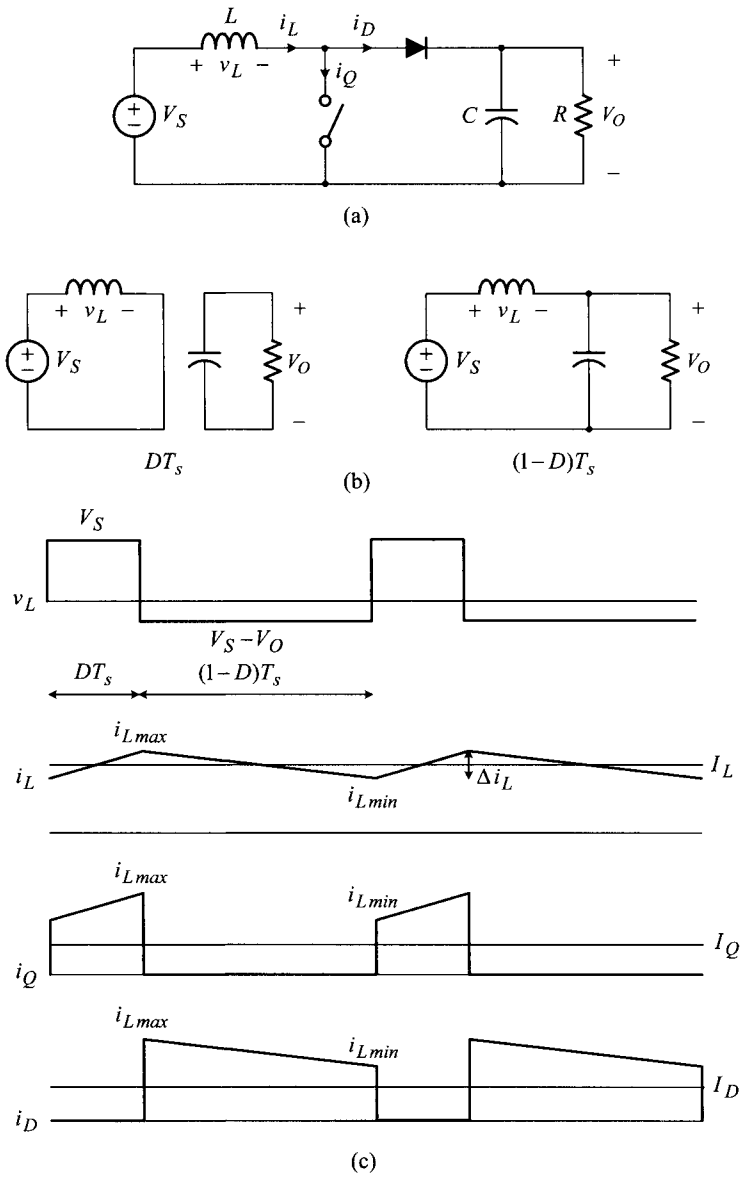


Figure 4.2 Steady-state analysis of boost converter in CCM. (a) Boost converter. (b) On-time and off-time subcircuits. (c) Major waveforms.

As illustrated in Fig. 4.2(c), the inductor current flows through the active switch during the on-time period and freewheels through the diode during the off-time period. Accordingly, the following relationships hold among the average value of the switch current, I_Q, average value of the diode current, I_D, and average value of the inductor current, I_L

$$I_Q = DI_L \tag{4.7}$$

$$I_D = (1 - D)I_L \tag{4.8}$$

In the boost converter, the diode is connected to the load, whereas the inductor is located at the source side. For this case, the average value of the inductor current is determined as explained below. Due to the charge balance condition, the average value of the capacitor current is zero. Accordingly, the average value of the diode current is to be equal to the load current, which is given by the ratio of the output voltage to load resistance

$$I_D = I_O = \frac{V_O}{R} \tag{4.9}$$

Using (4.8) and (4.9), the average value of the inductor current is found as

$$I_L = \frac{1}{1 - D} I_D = \frac{1}{1 - D} \frac{V_O}{R} \tag{4.10}$$

The maximum and minimum values of the inductor current are expressed as

$$i_{L\,max} = I_L + \frac{1}{2}\Delta i_L \tag{4.11}$$

and

$$i_{L\,min} = I_L - \frac{1}{2}\Delta i_L \tag{4.12}$$

where I_L is given by (4.10) and Δi_L is determined by (4.6).

■ EXAMPLE 4.1 Steady-State Operation of Boost Converter

This example shows the steady-state analysis and circuit waveforms of the boost converter. The operational conditions and circuit parameters are $V_S = 12$ V, $L = 160\ \mu$H, $C = 400\ \mu$F, $T_s = 20\ \mu$s, and $D = 0.4$. The steady-state values of the major voltage and current waveforms are evaluated as shown in Table 4.1. The simulated steady-state circuit waveforms are given in Fig. 4.3.

Estimation of Output Voltage Ripple

The magnitude of the output voltage ripple is evaluated from the waveforms shown in Fig. 4.4. The diode current i_D is split into the capacitor current i_C and load current I_O. As discussed in Section 3.4.3, the load current I_O carries the dc component of i_D while the capacitor current i_C absorbs the ac component of i_D: $I_O = I_D$ and $i_C = i_D - I_D$. This situation is illustrated in Fig. 4.4(b).

Table 4.1 Steady-State Analysis of Boost Converter

Circuit variable	Expression
V_O	$\frac{1}{1-D}V_S = \frac{1}{1-0.4}12 = 20$ V
$v_{L\,max}$	$V_S = 12$ V
$v_{L\,min}$	$V_S - V_O = 12 - 20 = -8$ V
I_L	$\frac{1}{1-D}\frac{V_O}{R} = \frac{1}{1-0.4}\frac{20}{5} = 6.67$ A
Δi_L	$\frac{V_S}{L}DT_s = \frac{12}{160\times 10^{-6}}0.4 \cdot 20 \times 10^{-6} = 0.6$ A
$i_{L\,max}$	$I_L + \frac{1}{2}\Delta i_L = 6.67 + \frac{0.6}{2} = 6.97$ A
$i_{L\,min}$	$I_L - \frac{1}{2}\Delta i_L = 6.67 - \frac{0.6}{2} = 6.37$ A

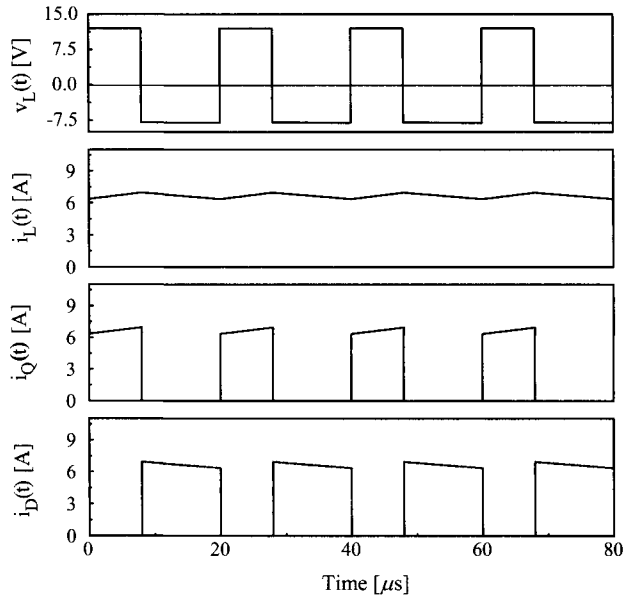


Figure 4.3 Circuit waveforms of boost converter.

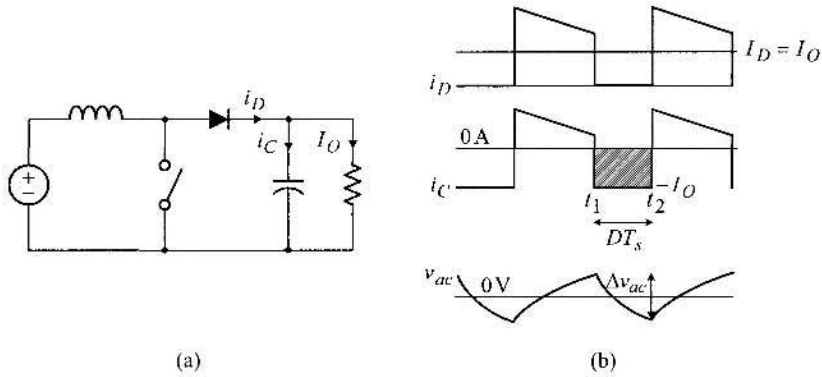


Figure 4.4 Estimation of output ripple. (a) Circuit diagram. (b) Current waveforms and output ripple.

The peak-to-peak value of the capacitor voltage, Δv_{ac}, or the magnitude of the output voltage ripple, Δv_O, can be found by integrating i_C over the time period in which i_C remains negative and by dividing the resulting value by the capacitance

$$\Delta v_{ac} = \Delta v_O = \frac{1}{C}\int_{t_1}^{t_2} i_C(\tau)\,d\tau \tag{4.13}$$

The operation of (4.13) is equivalent to evaluating the area of the highlighted rectangle in Fig. 4.4(b) and dividing the area by the capacitance. By noting that $|t_2 - t_1| = DT_s$, the magnitude of the output voltage ripple is given by

$$\Delta v_O = \frac{1}{C} I_O DT_s = \frac{1}{C}\frac{V_O}{R} DT_s \tag{4.14}$$

It should be noted that (4.14) is only valid when the boost converter is operating in CCM and the output capacitor does not contain an equivalent series resistance (esr). When the esr R_c is present in the capacitor, the output ripple is given by

$$\Delta v_O \approx \Delta i_D R_c = i_{D\,max} R_c = i_{L\,max} R_c \tag{4.15}$$

for the boost converter operating in either CCM or DCM. The output ripple of the boost converter, given by $\Delta v_O \approx i_{L\,max} R_c$ in (4.15), is significantly larger than that of the buck converter, given by $\Delta v_O \approx \Delta i_L R_c$ in (3.31).

4.1.3 Steady-State Analysis in DCM

The boost converter operates at the borderline between CCM and DCM when the condition $I_L = \Delta i_L/2$ is satisfied. The CCM/DCM boundary condition is expressed in terms of circuit parameters and operating conditions

$$\frac{1}{1-D}\frac{V_O}{R} = \frac{1}{2}\frac{V_S}{L} DT_S \tag{4.16}$$

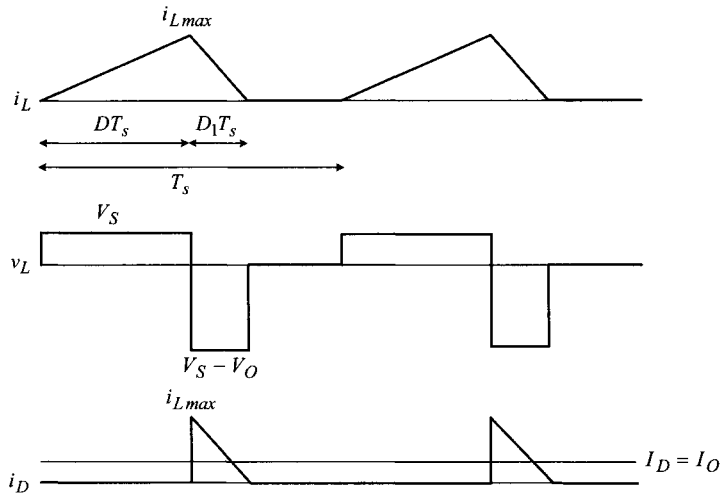


Figure 4.5 Circuit waveforms of boost converter in DCM operation.

based on (4.10) and (4.6). The expression (4.16) is used to find the critical value for the load resistance

$$R_{crit} = \frac{2L}{D(1-D)^2 T_s} \tag{4.17}$$

that determines the operational mode. When the load resistance is larger than R_{crit}, the converter enters DCM operation. Otherwise, the converter remains in CCM operation.

Figure 4.5 shows the major circuit waveforms of a boost converter operating in DCM. Application of the volt-sec balance condition to the inductor yields

$$V_S DT_s = (V_O - V_S) D_1 T_s \tag{4.18}$$

which indicates that

$$\frac{V_O}{V_S} = \frac{D + D_1}{D_1} \tag{4.19}$$

The unknown variable D_1 should be removed from (4.19) to yield a complete voltage gain expression.

For the boost converter, the average value of the diode current should be the same as the load current, $I_D = I_O$, because the diode is connected to the output of the converter. From the waveform of the diode current i_D, the following equation is set forth

$$\frac{\frac{1}{2} i_{Lmax} D_1 T_s}{T_s} = I_O \tag{4.20}$$

By incorporating the fact

$$i_{Lmax} = \frac{V_S}{L} DT_s \tag{4.21}$$

and

$$I_O = \frac{V_O}{R} \tag{4.22}$$

the equation (4.20) is rearranged as

$$\frac{1}{2}\frac{V_S}{L}DT_sD_1 = \frac{V_O}{R} \tag{4.23}$$

to yield the expression for D_1

$$D_1 = \frac{V_O}{V_S}\frac{2L}{RDT_s} \tag{4.24}$$

Now, the expressions (4.19) and (4.24) are combined together, resulting in a quadratic equation for V_O/V_S

$$\left(\frac{V_O}{V_S}\right)^2 - \left(\frac{V_O}{V_S}\right) - \frac{D^2RT_s}{2L} = 0 \tag{4.25}$$

The solution to (4.25) becomes the DCM gain of the boost converter

$$\frac{V_O}{V_S} = \frac{1}{2}\left(1 + \sqrt{1 + \frac{2D^2RT_S}{L}}\right) \tag{4.26}$$

The DCM voltage gain is a nonlinear function of circuit parameters and operational conditions. The following two observations, previously found in the buck converter case, also hold true for the boost converter.

1) The voltage gain grows larger as the load resistance is increased.

2) For most practical converter parameters, the DCM voltage gain is larger than the CCM counterpart when the same duty ratio is assumed.

4.1.4 Effects of Parasitic Resistance on Voltage Gain

The voltage gain of the ideal boost converter in CCM operation, $V_O/V_S = 1/(1 - D)$, predicts that the output voltage increases without limits as the duty ratio D approaches unity, thereby yielding an infinite output voltage with $D = 1$. However, the operational principle of the boost converter contradicts this scenario. With $D = 1$, the active switch remains closed all the time and the diode never conducts. This implies that the output section of the converter is isolated from the source. For this case, the output voltage is zero because no energy is delivered from source to load.

The conflict between the ideal voltage gain and the operational principle of the converter can be resolved when the non-ideal characteristics of the circuit components are incorporated. Figure 4.6 shows a boost converter along with its on-time and off-time subcircuits, where the winding resistance R_l is included to a practical inductor, while the other circuit components are still assumed ideal. The voltage gain expression of the converter with the presence of R_l is now derived to investigate the behavior of the *non-ideal* boost converter.

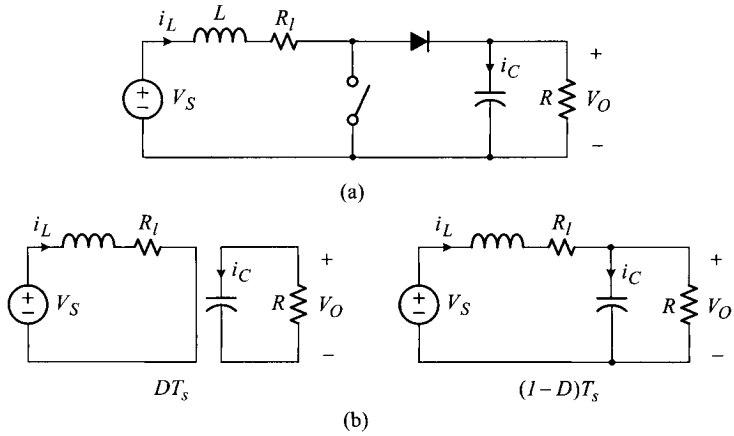


Figure 4.6 Boost converter with inductor winding resistance. (a) Circuit diagram. (b) On-time and off-time subcircuits.

The volt-sec balance condition of the inductor is formulated as

$$(V_S - \bar{i}_L(t)R_l)DT_s = -(V_S - \bar{i}_L(t)R_l - V_O)(1 - D)T_s \tag{4.27}$$

where $\bar{i}_L$ represents the average value of the inductor current: $\bar{i}_L = I_L$. The average inductor current $\bar{i}_L$ has the same effect as the original inductor current i_L, as far as the volt-sec balance condition is concerned. The expression (4.27) is simplified to

$$V_S = I_L R_l + (1 - D)V_O \tag{4.28}$$

On the other hand, the amp-sec balance condition on the output capacitor is written as

$$\frac{V_O}{R}DT_s = \left(\bar{i}_L(t) - \frac{V_O}{R}\right)(1 - D)T_s \tag{4.29}$$

which is simplified to

$$\frac{V_O}{R} = (1 - D)I_L \tag{4.30}$$

The desired expression for the voltage gain is now obtained by simultaneously solving (4.28) and (4.30) to eliminate I_L. The resulting voltage gain is arranged as the product of the voltage gain of the ideal boost converter and the correction factor that accounts for the effect of the winding resistor R_l

$$\frac{V_O}{V_S} = \frac{1}{1 - D}\left(\frac{1}{1 + \dfrac{1}{(1 - D)^2}\dfrac{R_l}{R}}\right) \tag{4.31}$$

The key parameter in the correction factor is the ratio of the winding resistance to the load resistance, R_l/R. Figure 4.7 shows the voltage gain curves, calculated using

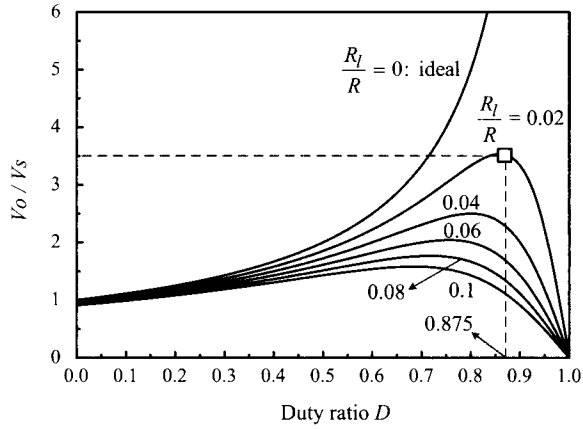


Figure 4.7 Voltage gain of non-ideal boost converter.

(4.31) with different values for R_l/R. The voltage gain curves reveal substantial deviations from the ideal case. The deviation intensifies as the R_l/R ratio increases, showing a wide gap between the actual voltage gain and the ideal voltage gain when the duty ratio is large. In particular, all the voltage gain curves merge to *zero* as the duty ratio approaches unity, rather than growing boundlessly. This phenomenon is actually consistent with the operation of the boost converter. With $D = 1$, the output of the converter is never connected to the source, and the output capacitor thus remains uncharged producing *zero* output voltage.

It is noteworthy that the R_l/R ratio limits the maximum voltage gain that a boost converter can produce. For example, with $R_l/R = 0.02$, Fig. 4.7 indicates that the maximum voltage gain is approximately 3.5 at the duty ratio of $D = 0.875$. If a voltage gain larger than 3.5 is required, R_l/R should be reduced to be smaller than 0.02.

■ EXAMPLE 4.2 Output Voltage with Inductor Winding Resistance

This example substantiates the results of the preceding gain analysis. The boost converter introduced in Example 4.1 has the parameters of $V_S = 12$ V, $L = 160\,\mu$H, $C = 400\,\mu$F, and $R = 5\,\Omega$. Now, a 0.1 Ω winding resistance is included in the inductor, resulting in $R_l/R = 0.1/5 = 0.02$. Under this condition, a series of simulations is performed with four different values for the duty ratio: $D = 0.875$, 0.900, 0.925, and 0.950. The output voltage waveforms of the boost converter are shown in Fig. 4.8. As expected from Fig. 4.7, the output voltage attains its peak value at $D = 0.875$ and decreases as the duty ratio is further increased. The theoretical predictions of the output voltage based on (4.31) are given in Table 4.2.

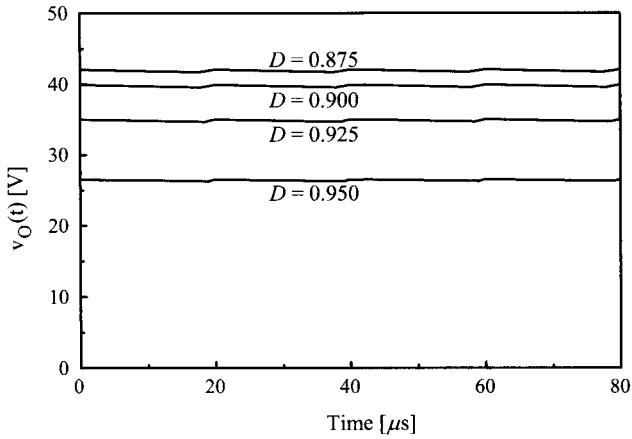


Figure 4.8 Output voltage waveforms of boost converter with $R_l/R = 0.02$.

Table 4.2 Output Voltage Analysis

Duty ratio	Output voltage
$D = 0.875$	$V_O = \frac{1}{1-D}\left(\frac{1}{1+\frac{1}{(1-D)^2}\frac{R_l}{R}}\right)V_S$
	$= \frac{1}{1-0.875}\left(\frac{1}{1+\frac{1}{(1-0.875)^2}\frac{0.1}{5}}\right)12 = 42$ V
$D = 0.900$	40 V
$D = 0.925$	35 V
$D = 0.950$	27 V

4.2 BUCK/BOOST CONVERTER

The buck/boost converter is a dc-to-dc power conversion circuit that can either step-up or step-down the input voltage. In this sense, the buck/boost converter is also called the up-down converter. This section discusses the circuit topology and steady-state operation of the buck/boost converter.

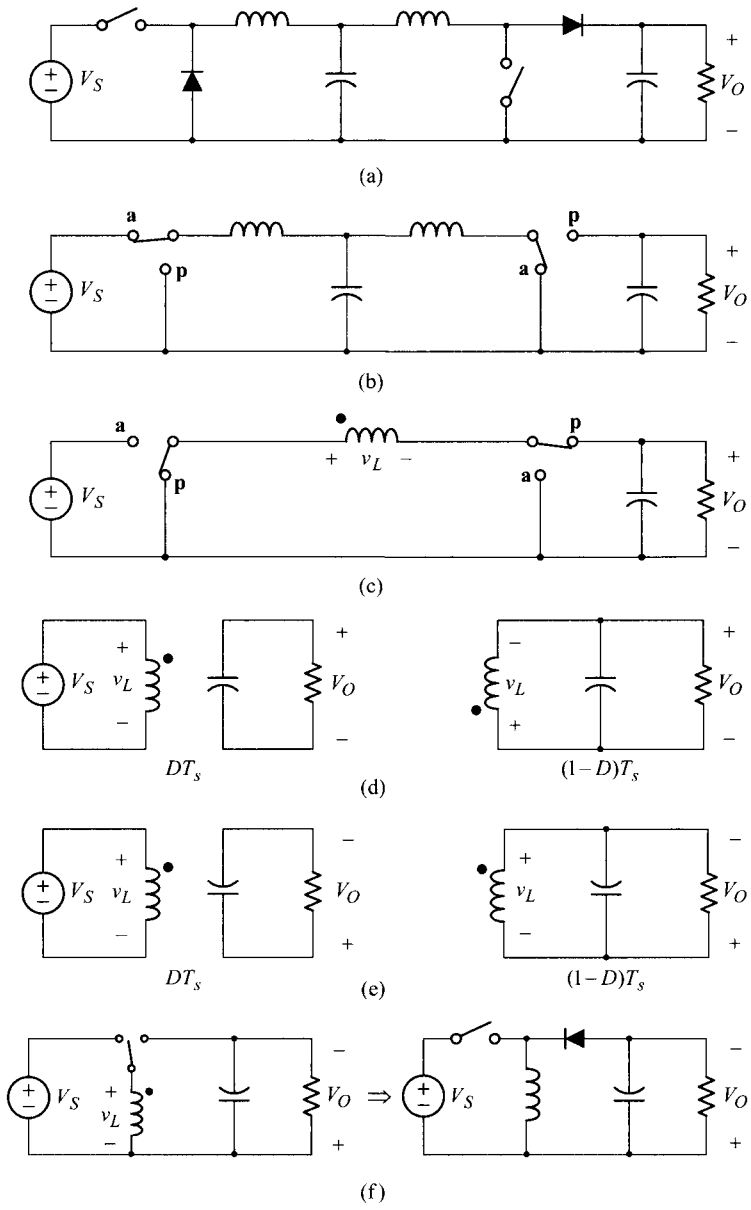


Figure 4.9 Derivation of buck/boost converter. (a) Cascaded connection of buck converter and boost converter. (b) Alternative representation using two synchronized SPDT switches. (c) Non-inverting buck/boost converter. (d) Subcircuits of non-inverting buck/boost converter. (e) Modification of subcircuits. (f) Buck/boost converter.

4.2.1 Evolution to Buck/Boost Converter

The buck/boost converter is created by cascading a buck converter and boost converter and simplifying the cascaded circuit. Figure 4.9(a) shows the buck converter connected to a boost converter downstream. Figure 4.9(a) is changed to Fig. 4.9(b) by replacing the active-passive switch pairs with SPDT switches. It is now assumed that the two SPDT switches are synchronized so that both SPDT switches are held at position **a** for DT_s and position **p** for $(1 - D)T_s$.

It should be noted that the upstream buck converter in Fig. 4.9(b) will be functioning even if its output filter capacitor is removed. The output filter capacitor, employed to enhance the filtering performance in a standalone buck converter, becomes redundant when the buck converter is connected to a boost converter which has its own output capacitor.

Once the output capacitor of the buck converter is removed, the inductor of the buck converter and that of the boost converter can be merged together, resulting in the circuit shown in Fig. 4.9(c). In Fig. 4.9(c), the left-hand side of the inductor terminal is marked • to highlight the polarity of the inductor voltage. This circuit is referred to as the non-inverting buck/boost converter for reasons that will become clear shortly.

Application of the volt-sec balance condition to the inductor in Fig. 4.9(c) yields

$$V_S DT_s = V_O(1 - D)T_s \tag{4.32}$$

which is simplified to result in the voltage gain of the buck/boost converter

$$\frac{V_O}{V_S} = D\frac{1}{1 - D} \tag{4.33}$$

The first term D originates from the buck converter upstream, while the second term $1/(1 - D)$ comes from the boost converter downstream.

The on-time and off-time subcircuits of the non-inverting buck/boost converter are shown in Fig. 4.9(d). The subcircuits in Fig. 4.9(d) are redrawn into Fig. 4.9(e) keeping the circuit properties unchanged. A new circuit is now synthesized from the two subcircuits in Fig. 4.9(e). The resulting circuit is shown in Fig. 4.9(f) in two different forms; one is with the SPDT switch and the other is with an active-passive switch pair. It is easy to see that the new circuit reduces to the two subcircuits in Fig. 4.9(e) with the two different conditions of the SPDT switch.

The converter circuit shown in Fig. 4.9(f) is named as the buck/boost converter because the converter is derived from the connection of the buck converter and the boost converter. The polarity of the output voltage of the buck/boost converter is opposite to that of the input voltage. Meanwhile, in the converter circuit in Fig. 4.9(c), the output voltage has the same polarity as the input voltage, as such, the converter is referred to as the non-inverting buck/boost converter.

4.2.2 Steady-State Analysis in CCM

The steady-state analysis of the buck/boost converter is performed in the same manner as that of the buck converter and boost converter cases.

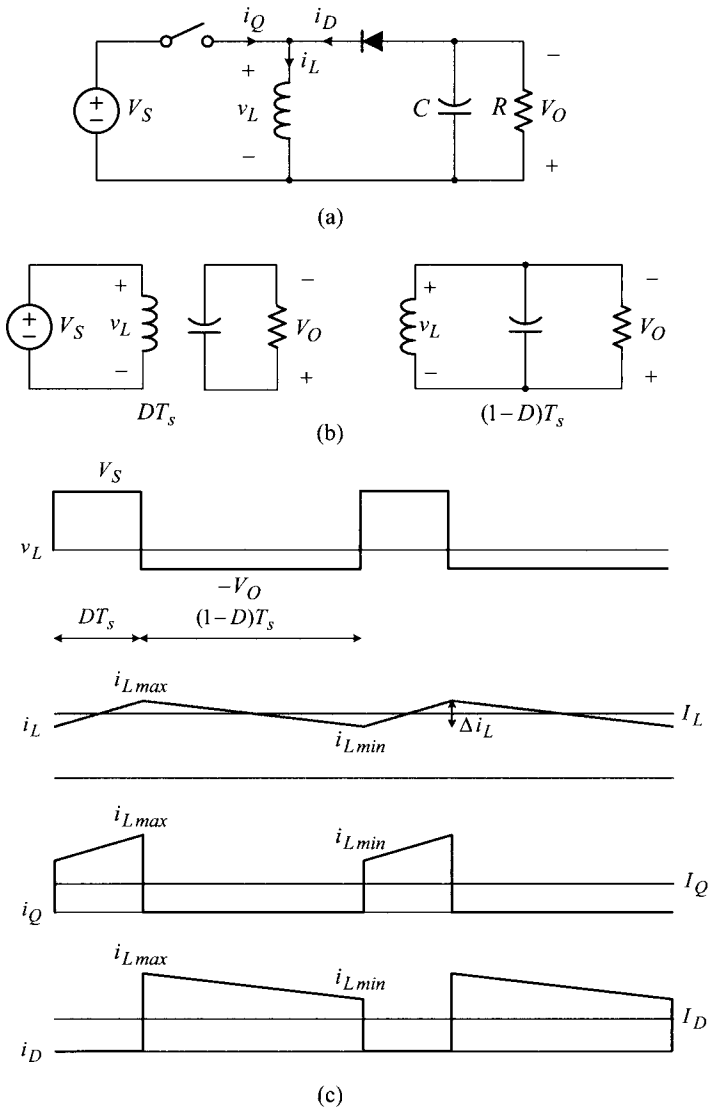


Figure 4.10 Steady-state analysis of buck/boost converter in CCM. (a) Buck/boost converter. (b) On-time and off-time subcircuits. (c) Major circuit waveforms.

Steady-State Operation in CCM

Figure 4.10 shows the buck/boost converter, on-time and off-time subcircuits, and major circuit waveforms. The steady-state operation of the converter is illustrated with the circuit waveforms in Fig. 4.10(c). Application of the volt-sec balance

condition to the inductor

$$V_S DT_s = V_O(1 - D)T_s \tag{4.34}$$

yields the voltage gain of the buck/boost converter

$$\frac{V_O}{V_S} = \frac{D}{1 - D} \tag{4.35}$$

The gain formula predicts that the output voltage varies from zero to infinity when the duty ratio is varied between $0 < D < 1$. However, as is the case with the boost converter, the voltage gain deviates from the ideal one when non-ideal circuit components are considered. It can be shown that the voltage gain is modified as

$$\frac{V_O}{V_S} = \frac{D}{1 - D}\left(\frac{1}{1 + \dfrac{1}{(1 - D)^2}\dfrac{R_l}{R}}\right) \tag{4.36}$$

at the presence of the inductor winding resistance R_l. The structure of (4.36) is the same as that of the voltage gain of the practical boost converter given in (4.31). Accordingly, the actual buck/boost converter will resemble the behavior of the practical boost converter discussed in Section 4.1.4.

The excursion of the inductor current is given by

$$\Delta i_L = \frac{V_S}{L} DT_s = \frac{V_O}{L}(1 - D)T_s \tag{4.37}$$

The average values of the switch current and diode current are determined as

$$I_Q = DI_L$$

$$I_D = (1 - D)I_L \tag{4.38}$$

Same as the boost converter case, the load current is supported by the diode current. Thus, the average diode current becomes the load current: $I_D = I_O = V_O/R$. Accordingly, the average value of the inductor current is given as

$$I_L = \frac{1}{1 - D} I_D = \frac{1}{1 - D}\frac{V_O}{R} \tag{4.39}$$

The maximum value of the inductor current then becomes

$$i_{L\,max} = I_L + \frac{1}{2}\Delta i_L \tag{4.40}$$

The minimum value is given by

$$i_{L\,min} = I_L - \frac{1}{2}\Delta i_L \tag{4.41}$$

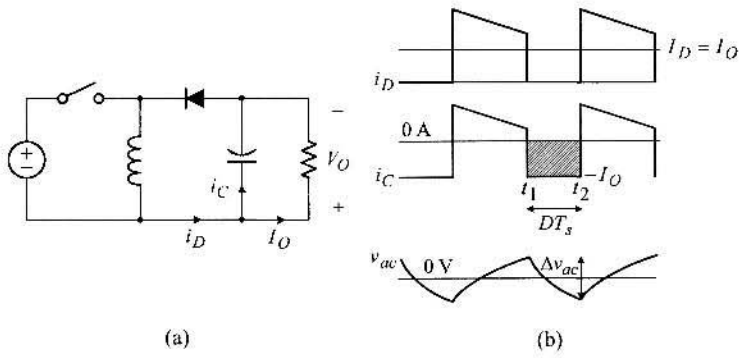


Figure 4.11 Estimation of output ripple. (a) Circuit diagram. (b) Current waveforms and output ripple.

Estimation of Output Voltage Ripple

Figure 4.11 shows the circuit diagram and waveforms that are used in predicting the magnitude of the output voltage ripple. The waveforms are identical to those of the boost converter shown in Fig. 4.4. This is because the output stage of the buck/boost converter retains the circuit properties of the boost converter. Consequently, the output voltage ripple of the buck/boost converter is the same as the boost converter case

$$\Delta v_{ac} = \Delta v_O = \frac{1}{C}\frac{V_O}{R}DT_s \tag{4.42}$$

This expression only holds true when the converter is in CCM operation and no esr is present in the output capacitor. When the esr of the output capacitor is considered, the output ripple is approximated to

$$\Delta v_O \approx \Delta i_D R_c = i_{D\,max} R_c = i_{L\,max} R_c \tag{4.43}$$

for the converter operating in either CCM or DCM.

■ EXAMPLE 4.3 Steady-State Operation of Buck/Boost Converter

This example demonstrates the circuit waveforms of a buck/boost converter. The circuit parameters of the buck/boost converter are $V_S = 12$ V, $L = 160\,\mu$H, $C = 400\,\mu$F, $R = 5\,\Omega$, $T_s = 20\,\mu$s, and $D = 0.4$. Table 4.3 summarizes the steady-state values of major circuit variables. Figure 4.12 shows the simulated waveforms of important circuit variables.

Table 4.3 Steady-State Analysis of Buck/Boost Converter

Circuit variable	Expression
V_O	$\frac{D}{1-D}V_S = \frac{0.4}{1-0.4}12 = 8$ V
$v_{L\,max}$	$V_S = 12$ V
$v_{L\,min}$	$-V_O = -8$ V
I_L	$\frac{1}{1-D}\frac{V_O}{R} = \frac{1}{1-0.4}\frac{8}{5} = 2.67$ A
Δi_L	$\frac{V_S}{L}DT_s = \frac{12}{160\times 10^{-6}}0.4\cdot 20\times 10^{-6} = 0.6$ A
$i_{L\,max}$	$I_L + \frac{\Delta i_L}{2} = 2.67 + \frac{0.6}{2} = 2.97$ A
$i_{L\,min}$	$I_L - \frac{\Delta i_L}{2} = 2.67 - \frac{0.6}{2} = 2.37$ A

4.2.3 Steady-State Analysis in DCM

For the buck/boost converter, the CCM/DCM borderline condition, $I_L = \Delta i_L/2$, is written as

$$\frac{1}{1-D}\frac{V_O}{R} = \frac{1}{2}\frac{V_S}{L}DT_s \tag{4.44}$$

using (4.39) and (4.37). From (4.44) and (4.35), the critical value for the load resistor is given by

$$R_{crit} = \frac{2L}{(1-D)^2T_s} \tag{4.45}$$

The converter enters DCM operation with the load resistance larger than R_{crit}.

Figure 4.13 shows the major DCM waveforms of the buck/boost converter. Application of the volt-sec balance condition to the inductor yields

$$V_S DT_s = V_O D_1 T_s \tag{4.46}$$

which is simplified to

$$\frac{V_O}{V_S} = \frac{D}{D_1} \tag{4.47}$$

By equating the average diode current I_D to the load current, it follows that

$$\frac{1}{2}\frac{V_S}{L}DT_s D_1 = \frac{V_O}{R} \tag{4.48}$$

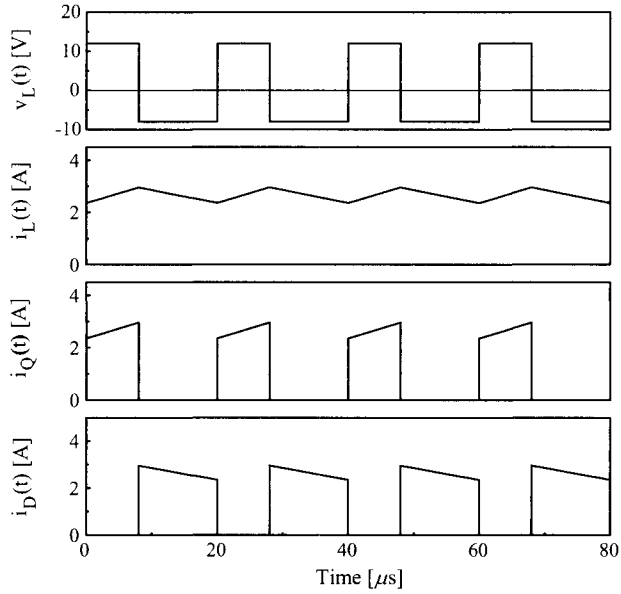


Figure 4.12 Circuit waveforms of buck/boost converter.

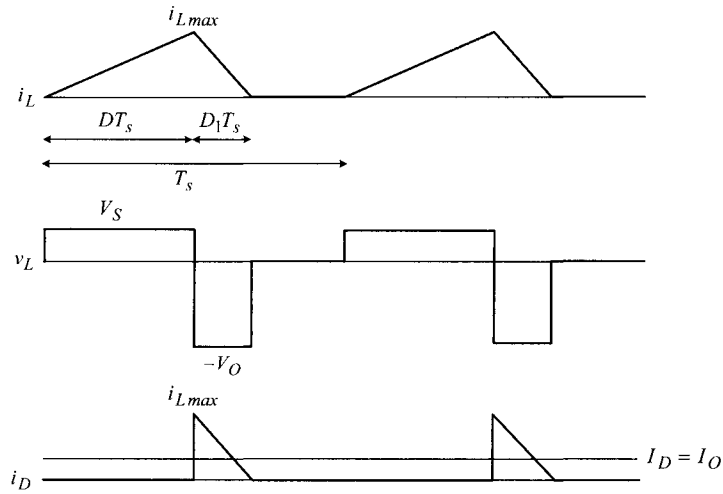


Figure 4.13 Circuit waveforms of buck/boost converter in DCM operation.

which provides an expression for D_1

$$D_1 = \frac{V_O}{V_S}\frac{2L}{RDT_s} \tag{4.49}$$

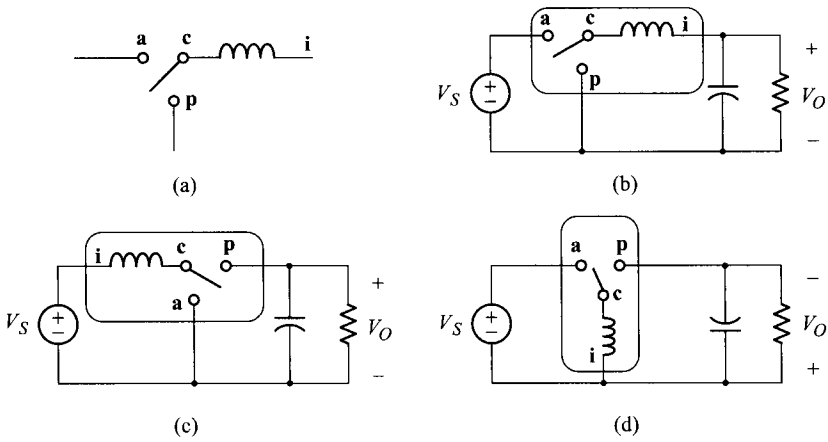


Figure 4.14 Three-terminal cell and basic converters. (a) Three-terminal cell. (b) Buck converter. (c) Boost converter. (d) Buck/boost converter.

Finally, by combining (4.47) and (4.49), the DCM voltage gain is given by

$$\frac{V_O}{V_S} = D\sqrt{\frac{RT_s}{2L}} \tag{4.50}$$

As is the case with the buck and boost converters, the voltage gain is proportional to the load resistance. Also, the DCM voltage gain is usually larger than the CCM counterpart when the same duty ratio is assumed.

4.3 STRUCTURE AND VOLTAGE GAIN OF THREE BASIC CONVERTERS

We have studied the three basic dc-to-dc converter topologies: the buck converter, the boost converter, and the buck/boost converter. The structure and voltage gain of these three converters are now reviewed from a more general perspective.

Structure of Three Basic Converters

The three basic converters contain a common circuit block, consisting of an SPDT switch and inductor. This common circuit block is shown in Fig. 4.14(a). This circuit block is referred to as the *three-terminal cell.* The node **a** denotes the active switch terminal and **p** indicates the passive switch terminal. The node **c** stands for the common terminal to which the filter inductor is connected. The other end of the filter inductor is denoted as the inductor terminal, **i**.

The three-terminal cell is inserted between the source and load in three different ways for the three basic converters. As shown in Fig. 4.14, the inductor terminal **i** is

directed to the output port in the buck converter, while the inductor terminal is linked to the input port in the boost converter. In the buck/boost converter, the inductor terminal is connected to the ground.

Despite the different configurations, the three converters have a common aspect that enables each circuit to function as a dc-to-dc power converter. In each converter, energy is transferred from the source to inductor when the common terminal is connected to the active terminal. On the other hand, when the common terminal is tied to the passive terminal, energy is released from the inductor to load. Thus, the switching action of the SPDT switch provides an energy transfer from the source to load. The amount of the energy transfer is determined by the duty ratio of the active switch. The inductor is used as an intermediate energy storage component.

To summarize, in the three basic converters, the three-terminal cell is positioned to link the source and the load, while allowing a controlled energy transfer between them by using the inductor as the transitional energy reservoir. In fact, the buck converter, boost converter, and buck/boost converter are the only three possible topological structures that can perform the dc-to-dc power conversion using the three-terminal cell shown in Fig. 4.14(a).

Voltage Gain of Three Basic Converters

The three basic dc-to-dc converters offer the different input-to-output voltage gains. Figure 4.15 shows the voltage gain characteristics of the three converters. For each converter, the voltage gain is displayed for both CCM and DCM operations using

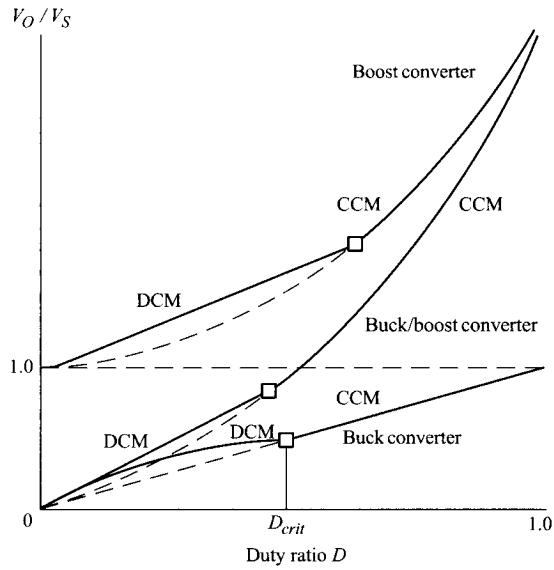


Figure 4.15 Voltage gain curves of three basic converters.

Table 4.4 DCM Voltage Gain and D_{crit} of Three Basic Converters

	DCM voltage gain	D_{crit}
Buck converter	$\frac{2D}{D+\sqrt{D^2+\frac{8L}{RT_s}}}$	$\frac{1}{2}(1-D_{crit})=\frac{L}{RT_s}$
Boost converter	$\frac{1}{2}\left(1+\sqrt{1+\frac{2D^2RT_s}{L}}\right)$	$\frac{1}{2}D_{crit}(1-D_{crit})^2=\frac{L}{RT_s}$
Buck/boost converter	$D\sqrt{\frac{RT_s}{2L}}$	$\frac{1}{2}(1-D_{crit})^2=\frac{L}{RT_s}$

D_{crit} as the borderline. The converter operates in DCM when its duty ratio is less than D_{crit} and moves to CCM operation when the duty ratio grows larger than D_{crit}. The expressions for the DCM voltage gain and D_{crit} of the three converters are summarized in Table 4.4.

4.4 FLYBACK CONVERTER: TRANSFORMER-ISOLATED BUCK/BOOST CONVERTER

For many dc-to-dc converter applications, electrical isolation between the input and output ports is required by law for practical reasons such as safety. One simple way to provide such an input-output isolation is to insert an isolation transformer in the middle section of dc-to-dc converters. Indeed, numerous isolated converter topologies are proliferated by adding a transformer to the three basic dc-to-dc converters. The flyback converter is a typical example of them.

The flyback converter is evolved from the buck/boost converter by adding an isolation transformer and simplifying the resulting circuit. The flyback converter has a very simple structure with a minimal component count, while providing the desired input-output isolation. Accordingly, the flyback converter is widely used as a cost-effective dc-to-dc conversion circuit for consumer electronics. This section presents the topological origin and steady-state operation of the flyback converter.

4.4.1 Evolution to Flyback Converter

Figure 4.16 shows the evolution of the flyback converter from the forerunning buck/boost converter. The buck/boost converter is shown in Fig. 4.16(a). A practical transformer is now inserted in the middle section of the buck/boost converter, resulting in the circuit shown in Fig. 4.16(b). After replacing the practical transformer with a combination of the magnetizing inductance L_m and ideal transformer, as shown in Fig. 4.16(c), the active switch and diode are relocated without affecting the operation

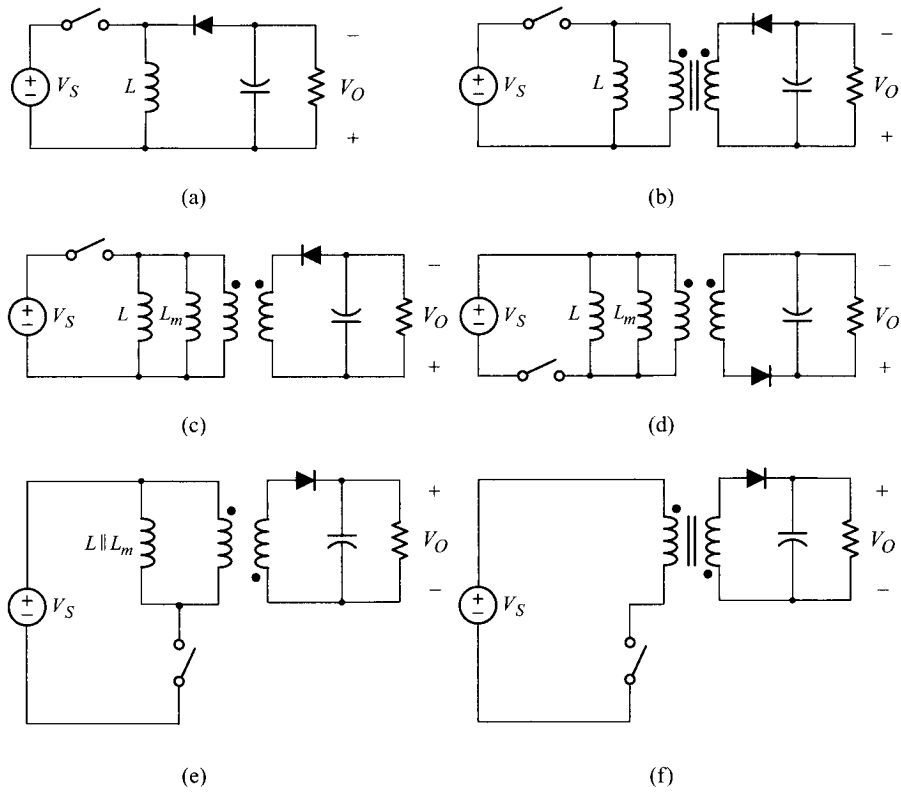


Figure 4.16 Evolution to flyback converter. (a) Buck/boost converter. (b) Insertion of isolation transformer. (c) Circuit model. (d) Equivalent circuit model. (e) Modified circuit model. (f) Flyback converter.

of the converter, as shown in Fig. 4.16(d). Figure 4.16(d) is now changed to Fig. 4.16(e) by combining the inductor of the buck/boost converter and the magnetizing inductance of the transformer, and vertically flipping the circuitry located in the secondary side of the ideal transformer. The final form of the flyback converter is shown in Fig. 4.16(f), where the composite inductance, $L \parallel L_m$, is considered as the magnetizing inductance of the practical transformer.

The flyback converter utilizes the magnetizing inductance of the isolation transformer as its functional inductance. Therefore, the isolation transformer should be fabricated in such a way that could offer a controllable magnetizing inductance. One easy method to achieve this goal is to create a gap in the magnetic path of the transformer. This is commonly implemented by introducing an air gap between the magnetic cores, which effectively determines the magnetizing inductance of the isolation transformer.

4.4.2 Steady-State Analysis in CCM

Functionally speaking, the flyback converter is a buck/boost converter with transformer isolation. Thus, the flyback converter closely mimics the buck/boost converter in its operation. Figure 4.17 illustrates the operation of the flyback converter in CCM, where a $1:n$ turns ratio is assumed for the transformer. The transformer is represented by the parallel connection of magnetizing inductance and ideal transformer.

During an on-time period in which the active switch is closed, the diode is reverse-biased by the sum of the output voltage and the voltage across the secondary transformer winding: $V_O + nV_S$. Accordingly, the on-time subcircuit for DT_s is resulted as shown in Fig. 4.17(b).

The operation of the converter during the on-time period DT_s is explained as follows. The voltage across the magnetizing inductance, v_m in Fig. 4.17, is the input voltage V_S. The current through the magnetizing inductance, i_m, thus ramps up with a slope V_S/L_m. The magnetizing current i_m flows through the switch, $i_m = i_Q$, while both the primary and secondary currents of the ideal transformer are zero, thereby meeting the current equation of the ideal transformer. During this period, energy is transferred from the source to the magnetizing inductance of the transformer. As the magnetizing current i_m increases linearly, so does the energy stored in the transformer. As i_m reaches its maximum value, the energy stored in the transformer attains its peak value.

When the active switch is turned-off, the magnetizing current i_m directs towards the primary winding of the transformer and this in turn pushes a positive current into the diode at the secondary side. Accordingly, the diode is turned-on and the circuit presents the off-time subcircuit for $(1 - D)T_s$, as shown in Fig. 4.17(b). In this period, the magnetizing current i_m runs into the *undotted* terminal of the primary winding, while the diode current i_D leaves from the *undotted* terminal of the secondary winding. The diode current in this period is given by $i_D = i_m/n$, according to the current equation of the $1:n$ ideal transformer.

During the off-time period, the output voltage V_O is reflected through the $1:n$ transformer and applied to the magnetizing inductance L_m in the negative polarity. Thus, the magnetizing current i_m ramps down with a slope $(-V_O/n)/L_m$. As i_m linearly decreases, the energy piled up in the transformer during the on-time period is delivered to the load resistor and output capacitor. Figure 4.17(c) shows the circuit waveforms of the flyback converter, constructed based on the operational principles explained above.

Application of the volt-sec balance condition to the magnetizing inductance L_m yields

$$V_S DT_s = \frac{V_O}{n}(1 - D)T_s \tag{4.51}$$

which leads to the voltage gain for the flyback converter

$$\frac{V_O}{V_S} = \frac{D}{1 - D}n \tag{4.52}$$

The voltage gain is given by the product of the voltage gain of the buck/boost converter and the turns ratio of the transformer.

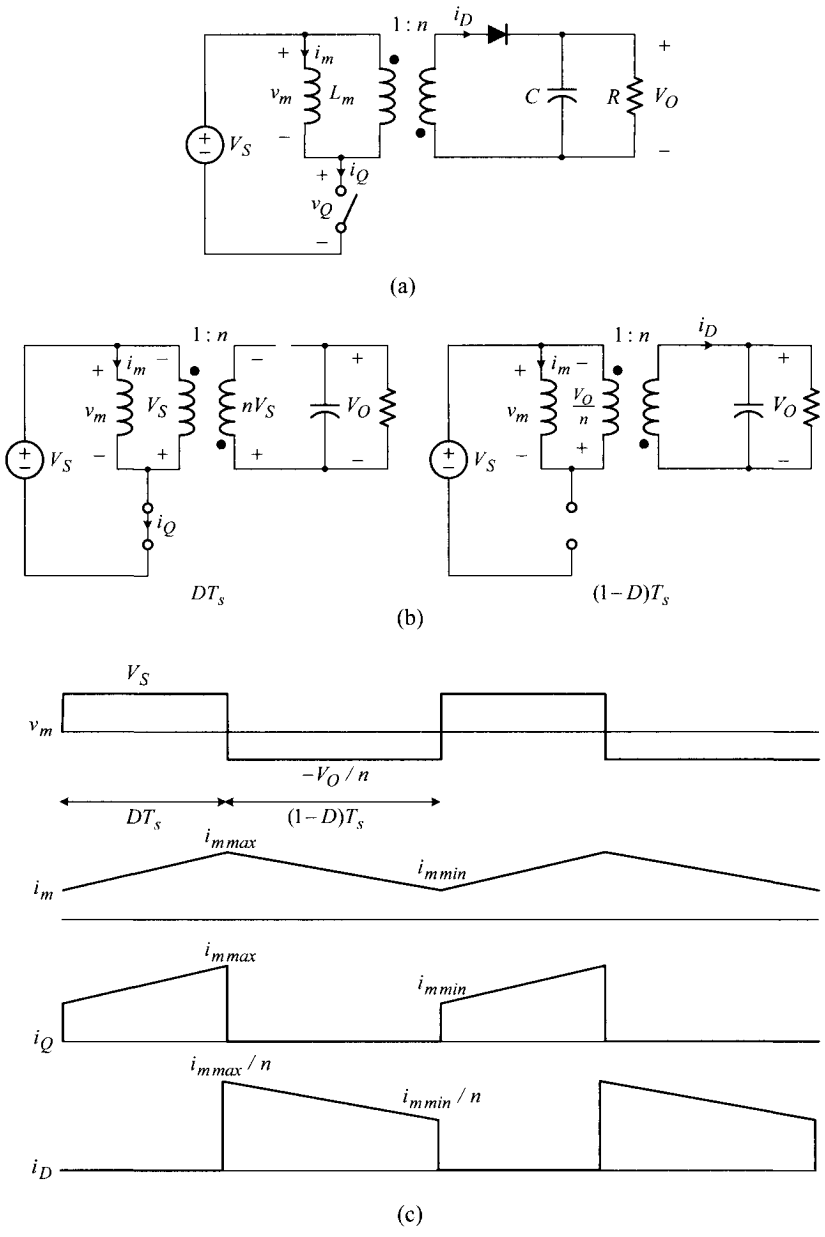


Figure 4.17 Steady-state analysis of flyback converter with $1 : n$ transformer. (a) Flyback converter. (b) On-time and off-time subcircuits. (c) Major circuit waveforms.

The excursion of the magnetizing current is given by

$$\Delta i_m = \frac{V_S}{L_m} DT_s = \frac{V_O/n}{L_m}(1 - D)T_s \tag{4.53}$$

The average value of the magnetizing current is found as follows. The average value of the diode current is equal to the load current because the diode is connected to the load

$$I_D = \frac{V_O}{R} \tag{4.54}$$

The average diode current I_D is related to the average magnetizing current I_M by the following equation

$$I_D = (1 - D)I_M \frac{1}{n} \tag{4.55}$$

From (4.54) and (4.55), the average magnetizing current is given by

$$I_M = \frac{1}{1 - D} n I_D = \frac{1}{1 - D} n \frac{V_O}{R} \tag{4.56}$$

The maximum value of the magnetizing current is determined as

$$i_{m\,max} = I_M + \frac{1}{2}\Delta i_m \tag{4.57}$$

and the minimum value is given by

$$i_{m\,min} = I_M - \frac{1}{2}\Delta i_m \tag{4.58}$$

The voltage across the active switch, v_Q in Fig. 4.17(a), is zero during the on-time period. During the off-time period, v_Q is given by the sum of the input voltage and the reflected output voltage

$$v_Q = V_S + \frac{V_O}{n} \tag{4.59}$$

■ EXAMPLE 4.4 Steady-State Operation of Flyback Converter

This example shows the results of the steady-state analysis and circuit waveforms of a flyback converter. The operational conditions and power stage parameters of the flyback converter are $V_S = 24$ V, $L_m = 160\,\mu$H, $n = 0.5$, $C = 400\,\mu$F, $R = 2.5\,\Omega$, $T_s = 20\,\mu$s, and $D = 0.4$. The results of the steady-state analysis are summarized in Table 4.5. The simulated circuit waveforms are shown in Fig. 4.18.

Table 4.5 Steady-State Analysis of Flyback Converter

Circuit variable	Expression
V_O	$\frac{D}{1-D}nV_S = \frac{0.4}{1-0.4}0.5 \cdot 24 = 8$ V
$v_{m\,max}$	$V_S = 24$ V
$v_{m\,min}$	$-\frac{V_O}{n} = -\frac{8}{0.5} = -16$ V
I_M	$\frac{1}{1-D}n\frac{V_O}{R} = \frac{1}{1-0.4}0.5\frac{8}{2.5} = 2.67$ A
Δi_m	$\frac{V_S}{L_m}DT_s = \frac{24}{160 \times 10^{-6}}0.4 \cdot 20 \times 10^{-6} = 1.2$ A
$i_{m\,max}$	$I_M + \frac{1}{2}\Delta i_m = 2.67 + \frac{1.2}{2} = 3.27$ A
$i_{m\,min}$	$I_M - \frac{1}{2}\Delta i_m = 2.67 - \frac{1.2}{2} = 2.07$ A
$i_{Q\,max}$	$i_{m\,max} = 3.27$ A
$i_{D\,max}$	$\frac{i_{m\,max}}{n} = \frac{3.27}{0.5} = 6.54$ A
$v_{Q\,max}$	$V_S + \frac{V_O}{n} = 24 + \frac{8}{0.5} = 40$ V

4.4.3 Steady-State Analysis in DCM

For the flyback converter, the CCM/DCM borderline condition $I_M = \Delta i_m/2$ is expressed as

$$\frac{1}{1-D}n\frac{V_O}{R} = \frac{1}{2}\frac{V_S}{L_m}DT_s \tag{4.60}$$

based on (4.56) and (4.53). By incorporating (4.52) into (4.60), the critical load resistance is found as

$$R_{crit} = 2n^2\frac{L_m}{(1-D)^2T_s} \tag{4.61}$$

If the load resistance is increased beyond R_{crit}, the converter encounters DCM operation.

Figure 4.19 shows the major waveforms of the flyback converter in DCM operation. When i_m becomes zero, the diode at the secondary side of the transformer is turned-off.

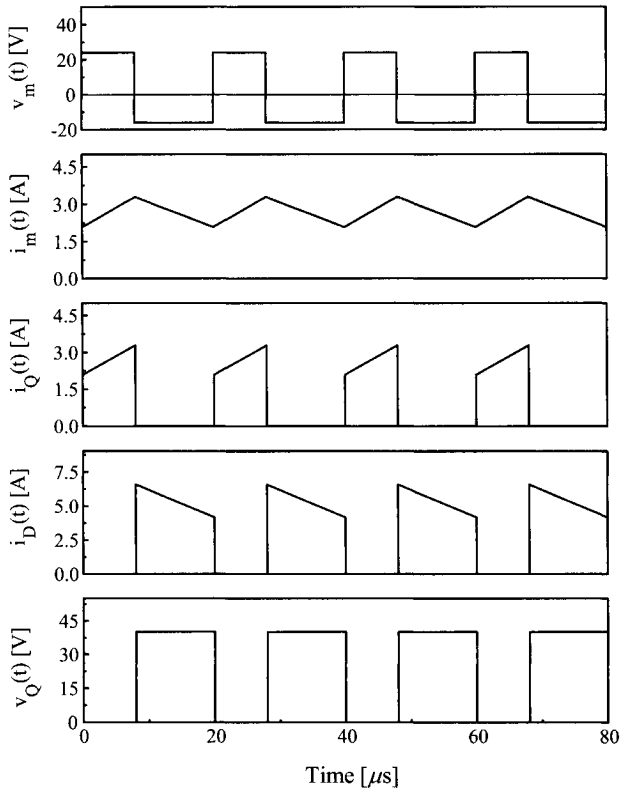


Figure 4.18 Circuit waveforms of flyback converter.

Under this condition, i_m remains at zero and thus v_m also becomes zero. Accordingly, the voltage across the active switch equals to the input voltage, $v_Q = V_S$.

Application of the volt-sec balance condition to the magnetizing inductance yields

$$V_S D T_s = \frac{V_O}{n} D_1 T_s \tag{4.62}$$

which leads to

$$\frac{V_O}{V_S} = \frac{D}{D_1} n \tag{4.63}$$

By equating the average value of the diode current to the load current

$$\frac{\frac{1}{2}\left(i_{m\,max}\right)\frac{1}{n} D_1 T_s}{T_s} = \frac{\frac{1}{2}\left(\frac{V_S}{L_m} D T_s\right)\frac{1}{n} D_1 T_s}{T_s} = \frac{V_O}{R} \tag{4.64}$$

an expression for D_1 is obtained

$$D_1 = \frac{V_O}{V_S} \frac{2L_m}{RDT_s} n \tag{4.65}$$

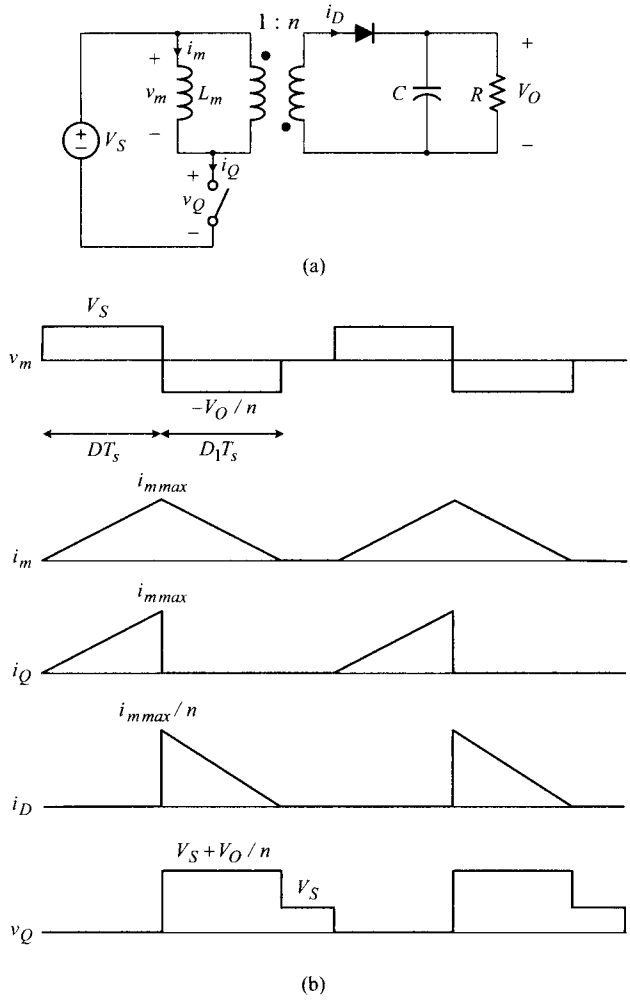


Figure 4.19 Steady-state analysis of flyback converter in DCM. (a) Circuit diagram. (b) Major circuit waveforms.

Finally, by combining (4.63) and (4.65), the DCM voltage gain is given by

$$\frac{V_O}{V_S} = D\sqrt{\frac{RT_s}{2L_m}} \tag{4.66}$$

The voltage gain expression is independent of the transformer turns ratio n, and in fact is the same as the DCM gain of the buck/boost converter.

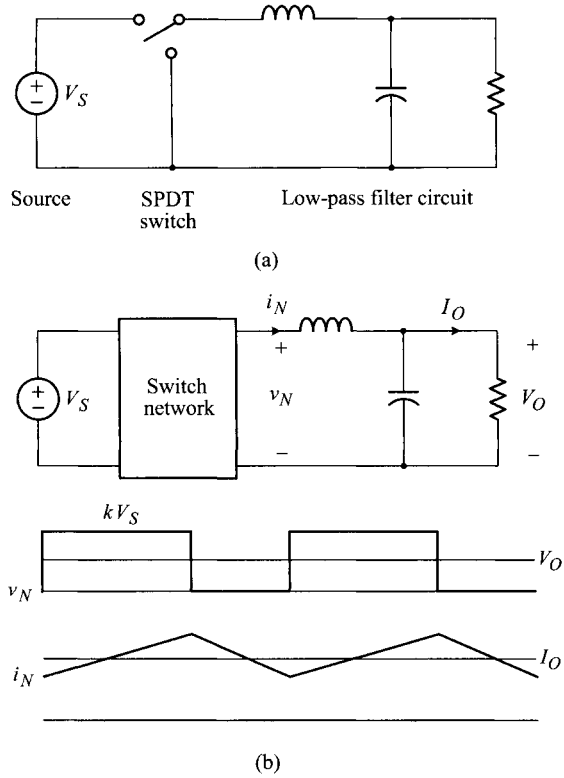


Figure 4.20 Derivation of isolated dc-to-dc converter from buck converter. (a) Buck converter. (b) Buck-derived isolated dc-to-dc converter and switch network waveforms.

4.5 BRIDGE-TYPE BUCK-DERIVED ISOLATED DC-TO-DC CONVERTERS

Most isolated dc-to-dc converters evolved from the three basic converters. We studied the flyback converter which was derived from the buck/boost converter by adding an isolation transformer.

Among isolated converter topologies, the dc-to-dc converters derived from the buck converter are widely used in medium-to-high power applications. In this section, a family of buck-derived isolated dc-to-dc converters, called bridge-type converters due to their circuit structures, will be studied. Another family of buck-derived isolated converters will be studied in the next section, which is referred to as forward converters based on their operational principles.

The derivation of an isolated dc-to-dc converter from the buck converter is illustrated in Fig. 4.20, where the buck converter is divided into three functional blocks: the source, SPDT switch, and low pass filter circuit in Fig. 4.20(a). The functions of the SPDT switch and low pass filter were explained in Section 3.2.1.

Isolated dc-to-dc converters are derived from the buck converter shown in Fig. 4.20(a), by replacing the SPDT switch with a *switch network* which performs the same function while providing an input-output isolation. This concept is illustrated in Fig. 4.20(b). The requirements of the switch network are summarized below.

1) The switch network should provide a rectangular voltage waveform, v_N in Fig. 4.20(b), as the input voltage to the low-pass filter circuit. The top value v_N is proportionate to the source voltage V_S and the bottom value is zero. The low-pass filter circuit smooths v_N, thereby producing the average value of v_N as the output voltage of the converter: $\bar{v}_N(t) = V_O$.

2) The switch network should deliver a triangular current waveform, i_N in Fig. 4.20(b), to the input terminal of the low-pass filter circuit. In particular, the switch network should provide a freewheeling path for i_N when v_N is zero. The average value of i_N is the output current of the converter: $\bar{i}_N(t) = I_O$.

3) The switch network should provide the input-output isolation. Most switch networks employ a transformer for the input-output isolation.

In this section, we first investigate the circuit configurations of the switch network. Then, this section reviews the circuit models for multi-winding transformers which are frequently employed as an isolation transformer in the switch network. Finally, we study the operation of three important buck-derived isolated converters: the full-bridge converter, half-bridge converter, and push-pull converter. It will be shown that, although named differently due to the difference in the switch network, the operation of these three buck-derived converters is all functionally equivalent to that of the buck converter.

4.5.1 Switch Network and Multi-Winding Transformer

This section introduces circuit configurations for the switch network. Because most switch networks contain a multi-winding transformer, the circuit models for multi-winding transformers are also discussed.

Switch Network Structure

Figure 4.21 shows the generic structure of the switch network. The switch network is divided into two circuits using the isolation boundary as the borderline. The circuit located at the left-hand side of the isolation boundary is referred to as the primary circuit, while the circuit appearing at the other side is denoted as the rectification circuit.

There are numerous circuit configurations that can be employed as the primary circuit or rectification circuit for the switch network. If a particular circuit configuration is selected each for the primary circuit and rectification circuit, a specific switch network will be created. This concept is illustrated in Fig. 4.21, where three

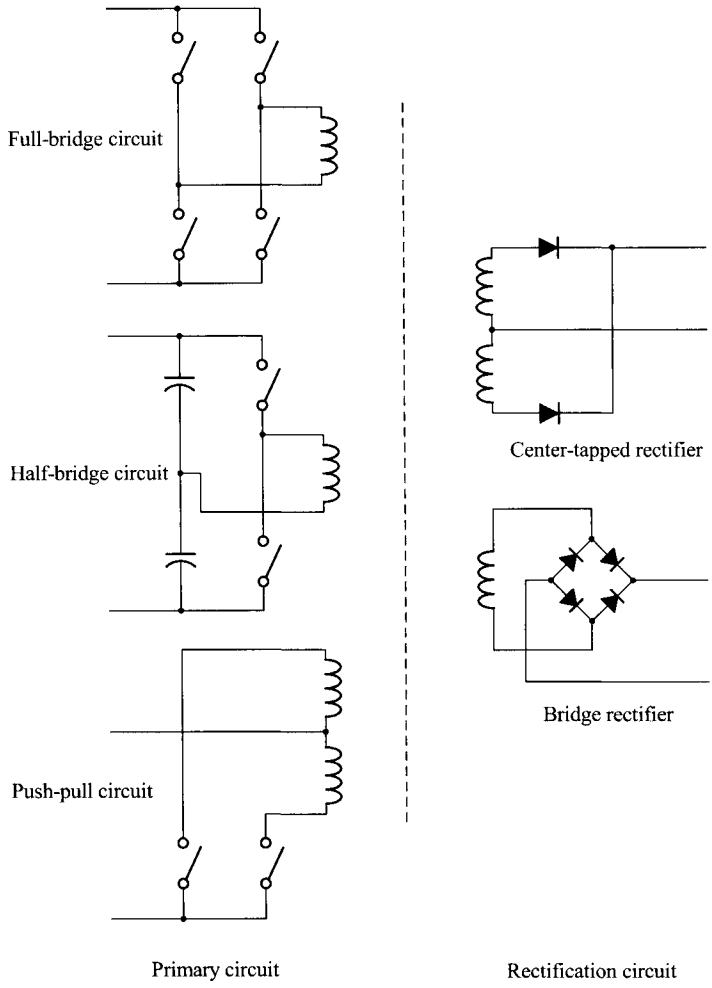


Figure 4.21 Structure of switch network.

primary circuits and two rectification circuits are shown across the isolation boundary. An arbitrary pair of these circuits, one from the primary circuits and the other from the rectification circuits, can be merged to function as a switch network for a transformer-isolated buck-derived dc-to-dc converter.

The primary circuits are named as the full-bridge circuit, half-bridge circuit, and push-pull circuit. The name *full-bridge* stems from the structure of the circuit, which has a pair of vertical legs configured with two active switches connected in series. In the *half-bridge* circuit, only one active switch leg exists while the other leg is replaced with two capacitors connected in series. On the other hand, the *push-pull* circuit is named after its operational principle; one switch pushes the current into

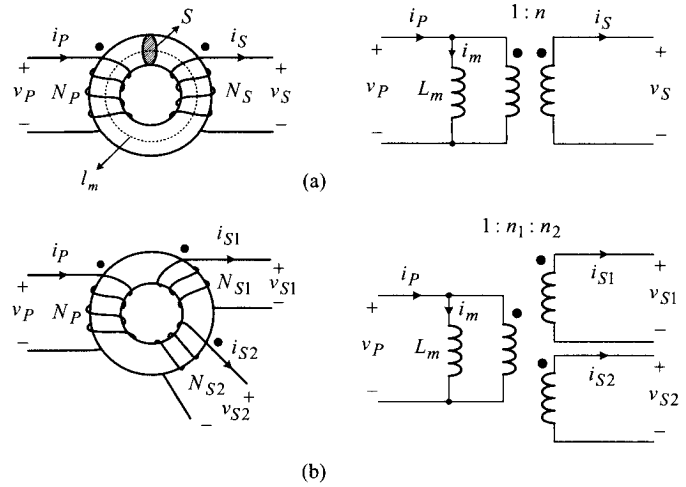


Figure 4.22 Practical transformers and circuit models. (a) Two-winding transformer. (b) Three-winding transformer.

the transformer, while the other switch pulls the current out of the transformer. The two rectifications circuits in Fig. 4.21 are called the center-tapped rectifier and bridge rectifier. It will be shown that these two rectifiers are equivalent in their function and thus can be used interchangeably. A switch network could employ a two-, three-, or four-winding transformer depending on the topologies of the primary and rectification circuits.

Circuit Models for Multi-Winding Transformers

The switch network usually contains a multi-winding transformer. Thus, it is necessary to review the circuit models for transformers before investigating the operations of transformer-isolated dc-to-dc converters. Figure 4.22(a) shows a two-winding transformer and its circuit model. The circuit model contains the magnetizing inductance and ideal transformer. Details about the transformer model were covered in Section 2.2.3. Using the transformer circuit model, the following relationships can be written

$$v_P(t) : v_S(t) = 1 : n \tag{4.67}$$

$$i_P(t) = i_m(t) + n\, i_S(t) \tag{4.68}$$

with

$$n = \frac{N_S}{N_P} \tag{4.69}$$

where N_P is the turns of the primary winding and N_S is that of the secondary winding. The magnetizing current i_m is given by

$$i_m(t) = \frac{1}{L_m} \int v_P(t)\, dt \tag{4.70}$$

The magnetizing inductance L_m is expressed as

$$L_m = \mu_r \mu_o \frac{S}{l_m} N_P^2 \tag{4.71}$$

in terms of the transformer parameters shown in Fig. 4.22(a).

Figure 4.22(b) shows a three-winding transformer and its circuit model. The circuit model consists of the magnetizing inductance and ideal three-winding transformer. While the circuit model can be considered as an extension of the two-winding transformer model, the model can also be derived based on the electro-magnetic phenomena inside the three-winding transformer. Equations (4.67) and (4.68) are modified for the three-winding transformer

$$v_P(t) : v_{S1}(t) : v_{S2}(t) = 1 : n_1 : n_2 \tag{4.72}$$

$$i_P(t) = i_m(t) + n_1 i_{S1}(t) + n_2 i_{S2}(t) \tag{4.73}$$

with

$$n_1 = \frac{N_{S1}}{N_P} \quad \text{and} \quad n_2 = \frac{N_{S2}}{N_P} \tag{4.74}$$

where N_P, N_{S1}, and N_{S2} represent the respective turns of each transformer winding. Expressions for the magnetizing current i_m and magnetizing inductance L_m are the same as those of the previous two-winding transformer. Polarity/direction of the winding voltage/current is consistent with Lenz's law and the dot convention discussed in Section 2.2.3. The circuit model and circuit equations for the three-winding transformer can readily be extended for the transformers with four or more windings.

When the magnetizing inductance L_m is assumed to be infinite, the circuit model reduces to the ideal three-winding transformer. The voltage equation of the ideal three-winding transformer is the same as (4.72). On the other hand, the current equation is modified to

$$i_P(t) = n_1 i_{S1}(t) + n_2 i_{S2}(t) \tag{4.75}$$

because i_m in (4.70) becomes zero with $L_m = \infty$.

4.5.2 Full-Bridge Converter

As the first example of bridge-type isolated converters, Fig. 4.23 shows a circuit diagram of the full-bridge converter along with its major waveforms. The full-bridge circuit is employed as the primary circuit, as its name indicates. For the rectification circuit, the center-tapped rectifier is selected in this specific example.

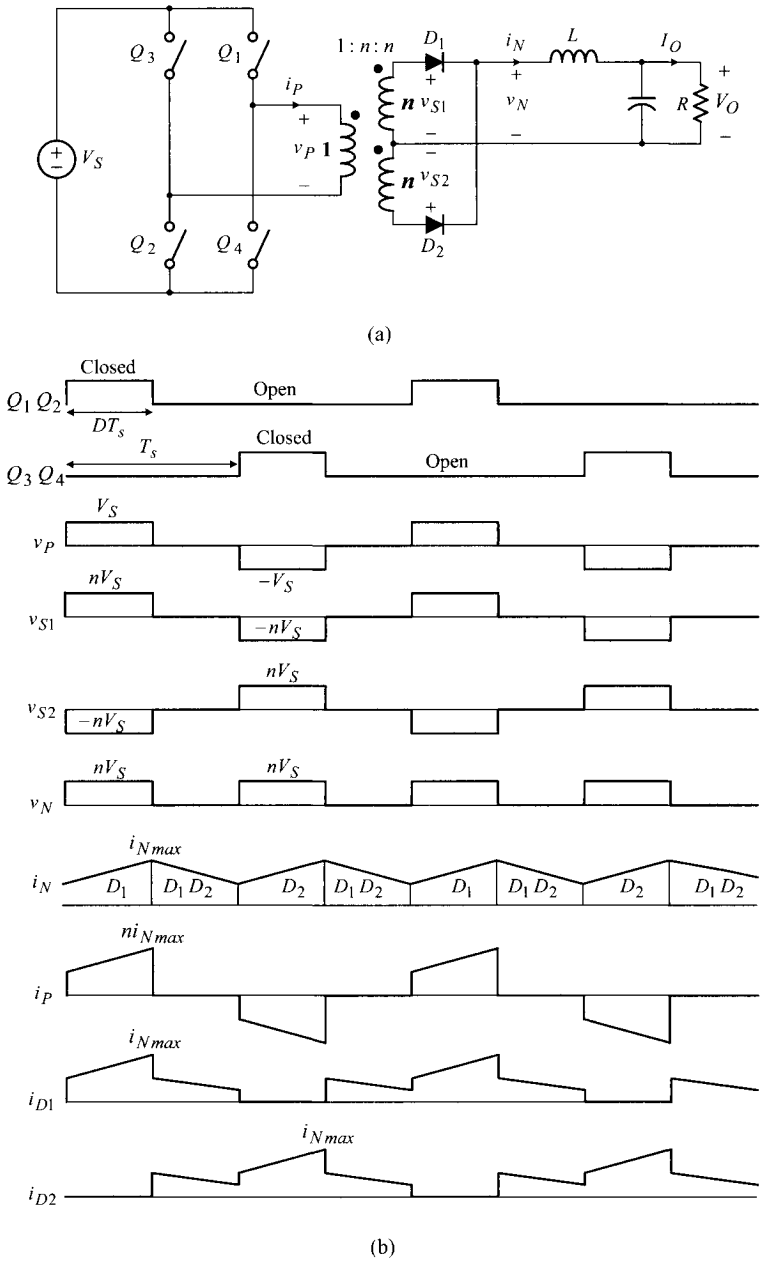


Figure 4.23 Full-bridge converter. (a) Circuit diagram. (b) Major circuit waveforms.

Operation with Ideal Transformer

The three-winding transformer in the middle of the switch network is assumed to be an ideal three-winding transformer with an $N_P : N_{S1} : N_{S2} = 1 : n : n$ turns ratio. This assumption simplifies the description of the converter operation. The effects of non-ideal characteristics of a practical transformer will be later discussed. With the assumption of the $1 : n : n$ turns ratio, the transformer equations are expressed as

$$v_P(t) : v_{S1}(t) : -v_{S2}(t) = 1 : n : n \tag{4.76}$$

$$i_P(t) = n\,(i_{D1}(t) - i_{D2}(t)) \tag{4.77}$$

based on the polarity/direction of the voltage/current waveforms shown in Fig. 4.23.

Four active switches in the primary circuit, $Q_1 - Q_4$, are grouped into the two switch pairs, $\{Q_1\ Q_2\}$ and $\{Q_3\ Q_4\}$. Two individual switches in each switch pair are driven synchronously while the two switch pairs are operated alternatively, as illustrated by the switch drive signals in Fig. 4.23(b). The time interval in which either the switches $\{Q_1\ Q_2\}$ or $\{Q_3\ Q_4\}$ are closed is referred to as the on-time period, while the time interval in which none of the switches is conducting is called the off-time period.

During an on-time period, the primary winding of the transformer is connected to the source, and the other two windings develop their terminal voltages according to the circuit equation of the ideal three-winding transformer. During an off-time period, the primary winding is isolated from the source, thereby making the terminal voltages of the three transformer windings identically zero.

The rectification circuit performs a full-wave rectification, thus providing the desired switch network voltage waveform, v_N, for the low pass filter circuit. The on-time value of v_N is given by the product of the input voltage and transformer turns ratio. The width of v_N is determined by the *effective* duty ratio of the active switches, represented by D in the switch drive signals. Accordingly, the output voltage of the converter is given by

$$V_O = \bar{v}_N(t) = nDV_S \tag{4.78}$$

During an on-time period, the output current of the switch network, i_N, linearly increases with a slope $(nV_S - V_O)/L$. When $\{Q_1\ Q_2\}$ are closed, the primary current i_P flows into the *dotted* end of the primary winding and the secondary current i_N circulates through the upper diode D_1, while the lower diode D_2 is reverse-biased by the voltage of $2nV_S$. Conversely, when $\{Q_3\ Q_4\}$ are closed, i_P reverses its direction and i_N now circulates through D_2, while D_1 is reverse-biased. The specific diode, which is conducting during the respective operational period, is labeled on the waveform of i_N.

During an off-time period in which all four switches are open and the primary current i_P is zero, the filter inductor current i_N turns on D_1 and D_2 simultaneously to create a freewheeling path. The transformer winding voltages are zero during the off-time period. Accordingly, i_N ramps down with a slope $-V_O/L$. The declining freewheeling current i_N is equally divided into i_{D1} and i_{D2}. Because i_{D1} comes out of the *dotted* terminal and i_{D2} enters the *dotted* terminal while i_P remains zero, the

current equation for the ideal three-winding transformer, given by (4.77), is satisfied. The current waveforms are shown in Fig. 4.23(b).

The switch network produces the desired waveforms for v_N and i_N, and the ideal three-winding transformer satisfies the circuit equations defined by (4.72) and (4.75). The average value of i_N becomes the load current

$$I_O = \bar{i}_N(t) = \frac{V_O}{R} \tag{4.79}$$

Two underlying assumptions are employed in the previous analysis. First, CCM operation is assumed, which is true only when the condition $I_O > \Delta i_N/2$ is satisfied. Yet, Fig. 4.23(b) can readily be modified to yield the circuit waveforms for DCM operation. In fact, the DCM operation of the buck converter, covered in Section 3.5.3, can be extended to the full-bridge converter with minor modifications. The second assumption is the ideal characteristics of the three-winding transformer. When a practical transformer is employed, the converter operation will be altered due to the presence of the magnetizing inductance. The operation with a magnetizing inductance is covered in the next section.

Effects of Magnetizing Inductance

Figure 4.24(a) shows the circuit model of a practical three-winding transformer. The practical transformer is modeled as a parallel connection of the magnetizing inductance L_m and an ideal three-winding transformer. The primary winding current of the ideal transformer is renamed as i'_p. The current i_P now denotes the input current to the practical transformer. It can easily be deduced that the filter inductor current i_N remains the same because the switch network voltage v_N is the same as that of the ideal transformer case. On the other hand, the other current waveforms will be altered due to the magnetizing current i_m running through L_m.

The voltage waveform across the magnetizing inductance L_m naturally meets the volt-sec balance condition and the magnetizing current i_m thus is symmetrical. During an on-time period, i_m increases or decreases depending on the polarity of the voltage across L_m. The magnetizing current, commutating via the closed primary-side switches, runs through L_m and does not enter the primary winding of the ideal transformer. Accordingly, during the on-time period, the winding currents of the ideal transformer, i'_p, i_{D1}, and i_{D2}, are identical to those of the previous case.

During an off-time period in which all the active switches are open, the magnetizing current i_m now circulates through the primary winding of the ideal transformer. In this period, i_m remains constant because the voltage across the magnetizing inductance is clamped at zero. With the presence of i_m in the primary winding, the secondary currents, i_{D1} and i_{D2}, are altered to meet the current equation of the ideal three-winding transformer

$$i'_p(t) = -i_m(t) = n(i_{D1}(t) - i_{D2}(t)) \tag{4.80}$$

while maintaining their sum unchanged

$$i_N(t) = i_{D1}(t) + i_{D2}(t) \tag{4.81}$$

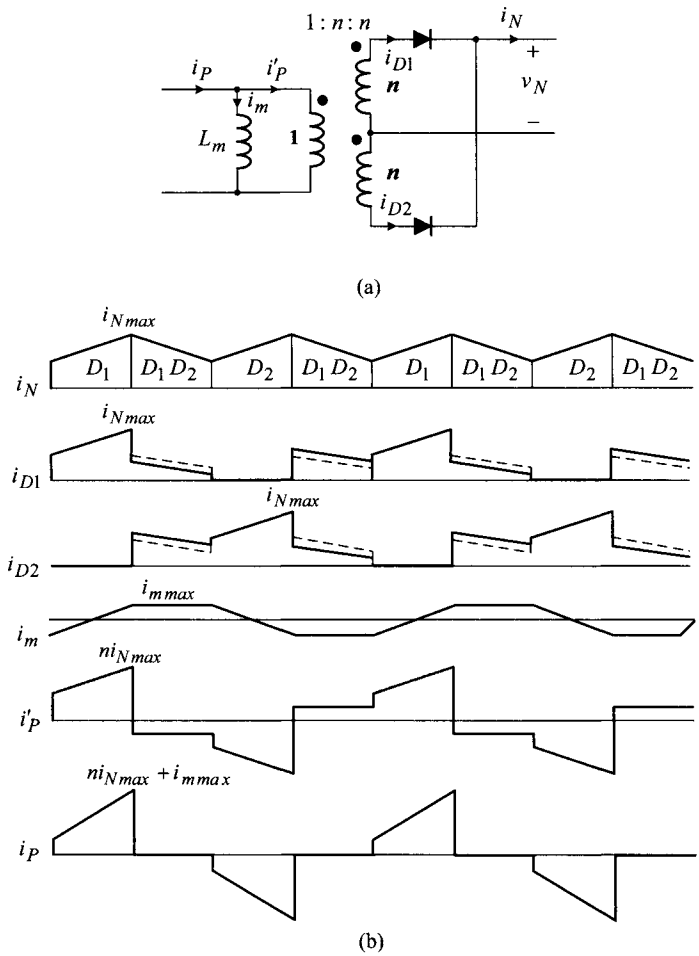


Figure 4.24 Switch network with practical transformer. (a) Practical three-winding transformer. (b) Major waveforms.

Figure 4.24(b) illustrates the current waveforms under this situation. The diode currents, i_{D1} and i_{D2}, are unevenly distributed during the off-time period to satisfy the equations (4.80) and (4.81) at the presence of the magnetizing current. The dashed lines show the original i_{D1} and i_{D2} waveforms at the absence of the magnetizing current. The effects of the magnetizing current can readily be seen by comparing the original and redistributed diode currents. The current waveform i'_P is constructed using the fact $i'_P = ni_{D1}$ or $i'_P = ni_{D2}$ for the on-time period, and $i'_P = -i_m$ for the off-time period. The i_P is obtained using the fact $i_P = i'_P + i_m$ for the on-time period and $i_P = 0$ for the off-time period.

Table 4.6 Steady-State Analysis of Full-Bridge Converter

Circuit variable	Expression
V_O	$nDV_S = 0.5 \cdot 0.25 \cdot 64 = 8$ V
$v_{N\,max}$	$nV_S = 32$ V
Δi_N	$\frac{nV_S - V_O}{L} D T_s = \frac{0.5 \cdot 64 - 8}{40 \times 10^{-6}} 0.25 \cdot 20 \times 10^{-6} = 3$ A
$i_{N\,max}$	$\frac{V_O}{R} + \frac{1}{2}\Delta i_N = \frac{8}{1} + \frac{1}{2}3.0 = 9.5$ A
$i_{N\,min}$	$\frac{V_O}{R} - \frac{1}{2}\Delta i_N = \frac{8}{1} - \frac{1}{2}3.0 = 6.5$ A
$i_{D1\,max}$	$i_{N\,max} = 9.5$ A
$i_{D2\,max}$	$i_{N\,max} = 9.5$ A

When the magnetizing inductance L_m approaches infinity, i_m reduces to zero and the current waveforms return to those of the previous ideal transformer case. For most transformer fabrications, the magnetizing inductance is maximized within practical limits to enhance efficiency and performance of transformers. Accordingly, the magnetizing inductance is sufficiently large and the magnetizing current is negligibly small. For this reason, it is common practice to assume the ideal characteristics for transformers employed in bridge-type isolated dc-to-dc converters.

Another justification for not considering the magnetizing inductance is that the input voltage of the switch network automatically meets the volt-sec balance condition on L_m. If this is not the case, the magnetizing inductance L_m, however large it might be, will eventually saturate to cause a fatal failure of the converter. This transformer saturation will not happen to the bridge-type isolated converters. The assumption of the ideal transformer will be implicitly used in the upcoming discussions about bridge-type isolated converters.

■ EXAMPLE 4.5 Steady-State Operation of Full-Bridge Converter

This example shows the steady-state analysis and circuit waveforms of a full-bridge converter. The operational conditions and circuit parameters of the full-bridge converter are $V_S = 64$ V, $n = 0.5$, $L = 40\,\mu$H, $C = 400\,\mu$F, $R = 1\,\Omega$, $T_s = 20\,\mu$s, and $D = 0.25$. For the given operational conditions, the steady-state values for major circuit variables are calculated in Table 4.6, while the corresponding PSpice® simulations are shown in Fig. 4.25.

4.5.3 Half-Bridge Converter

The half-bridge converter can be configured by combining the half-bridge circuit with either the bridge rectifier or center-tapped rectifier. The bridge rectifier is employed in the half-bridge converter in Fig. 4.26(a). The two capacitors, C_1 and C_2 in Fig. 4.26(a), function as a voltage divider and each capacitor develops a dc voltage $V_S/2$ at its terminals.

The switch drive signals and voltage waveforms across the primary and secondary windings of the two-winding transformer are shown in Fig. 4.26(b). When Q_1 is turned-on, v_P and v_S both become positive. Conversely, when Q_2 is closed, v_P and v_S are negative. During an off-time period in which both Q_1 and Q_2 are open, the transformer is functionally isolated from the switch network, thereby yielding the conditions $v_P = v_S = 0$ and $i_P = i_S = 0$.

As shown in Fig. 4.26(b), the bridge rectifier circuit generates v_N that alternates between $nV_S/2$ and zero. The output voltage of the converter then becomes

$$V_O = \bar{v}_N(t) = \frac{nDV_S}{2} \tag{4.82}$$

The shape of i_N is the same as the previous full-bridge converter case, yet the commutation of the diodes is different. When Q_1 is closed, D_1 and D_2 carry i_N. Conversely, when Q_2 is closed, D_3 and D_4 conduct. During an off-time period in which the transformer is functionally separated from the other part of the circuit, i_N turns on all the four diodes simultaneously and freewheels through them. It is apparent that the converter could employ a center-tapped rectifier instead of the bridge rectifier. When a center tapped rectifier is used, the current waveforms are identical to those of Fig. 4.23.

4.5.4 Push-Pull Converter

Another variation of the bridge-type converter is the push-pull converter shown in Fig. 4.27. The converter uses two active switches and one four-winding transformer. While a center-tapped rectifier is used in Fig. 4.27, the bridge rectifier can be used as an alternative, provided that the four-winding transformer is replaced with a three-winding transformer.

When the switch Q_1 is closed, v_{P1} and v_{S1} become positive while v_{P2} and v_{S2} are negative. Conversely, when Q_2 is turned-on, v_{P2} and v_{S2} now become positive while the other two windings develop a negative voltage. The terminal voltages of the four windings are shown in Fig. 4.27. The rectification circuit performs a full-wave rectification, thus yielding the desired v_N waveform. The current waveforms associated with the four-winding transformer are also shown in Fig. 4.27. It can be confirmed that the voltage and current waveforms in Fig. 4.27 satisfy the circuit equations for the four-winding transformer.

The operation of the push-pull converter is functionally the same as that of the full-bridge converter. In fact, the push-pull converter replicates the operation of the full-bridge converter using two active switches and a transformer two primary windings.

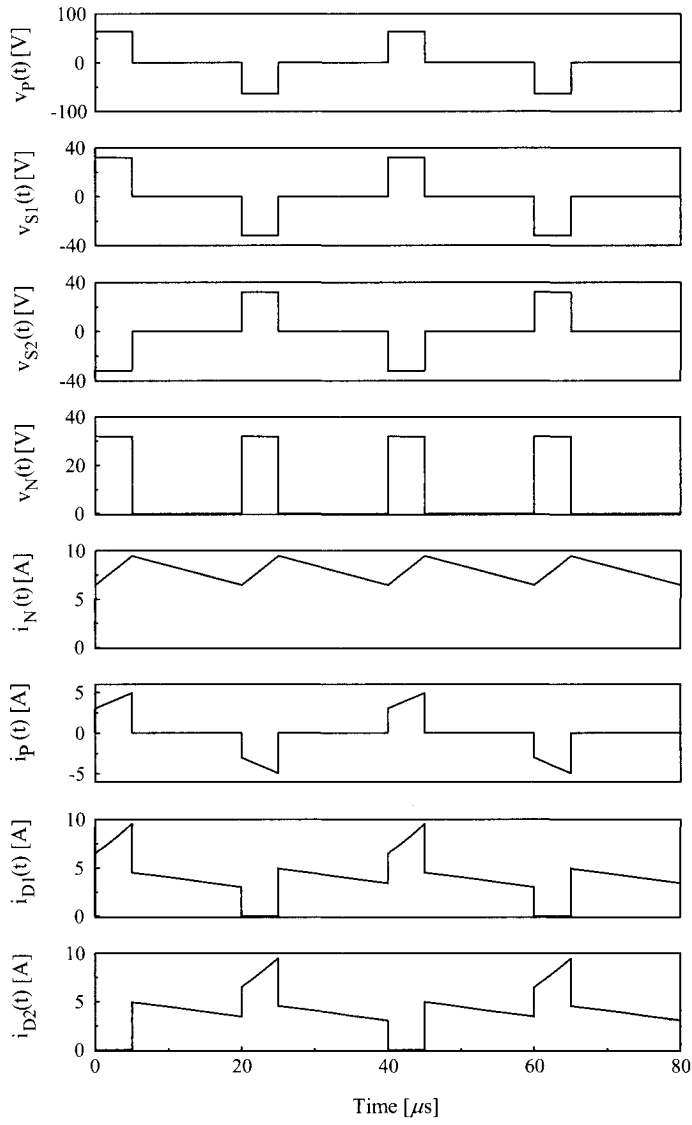


Figure 4.25 Circuit waveforms of full-bridge converter.

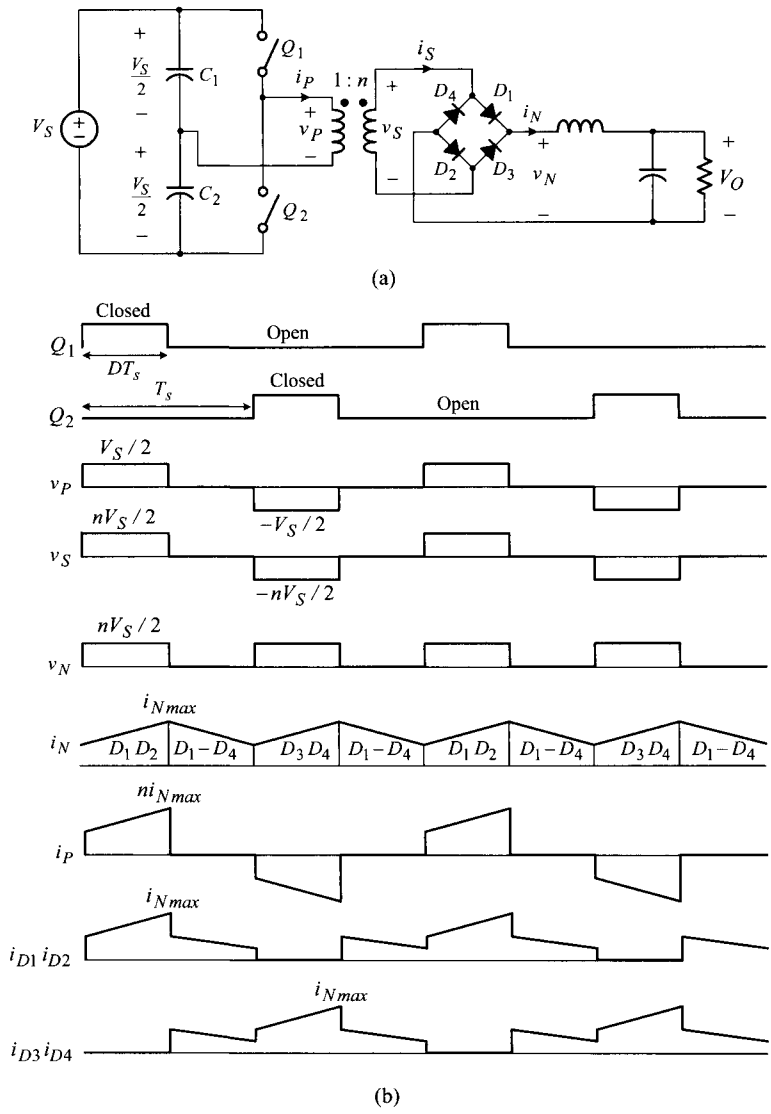


Figure 4.26 Half-bridge converter. (a) Circuit diagram. (b) Major circuit waveforms.

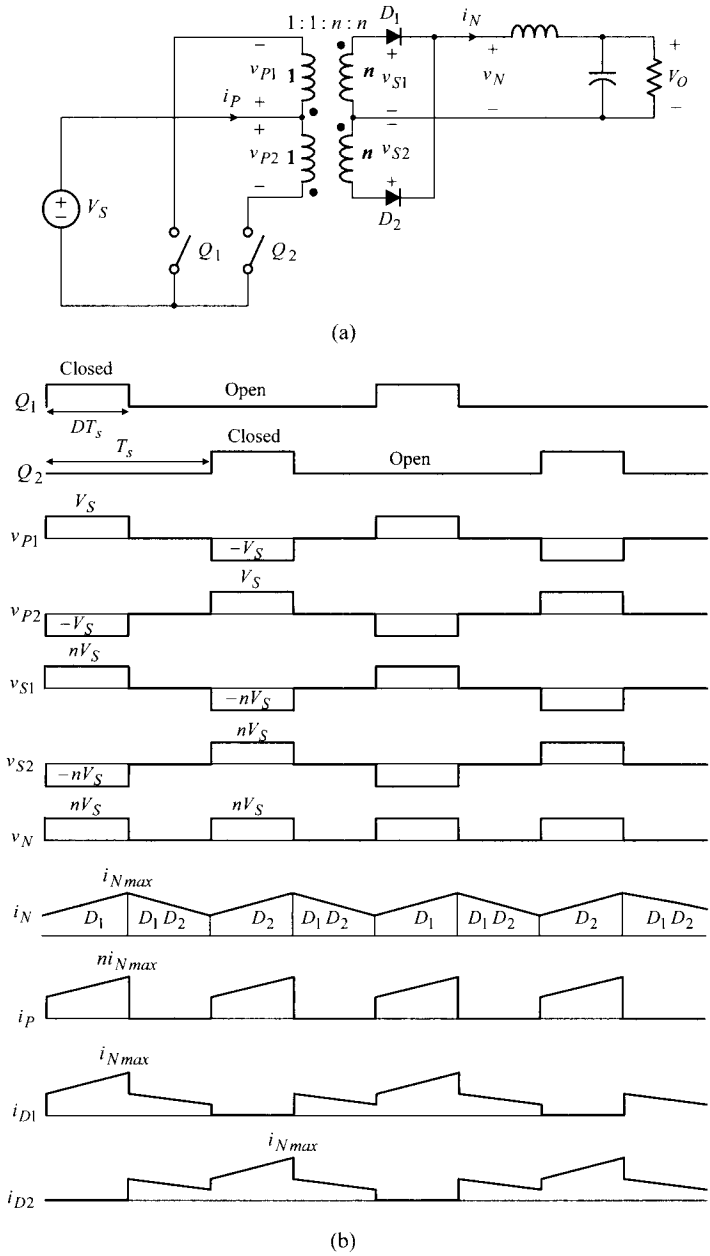


Figure 4.27 Push-pull converter. (a) Circuit diagram. (b) Major circuit waveforms.

4.6 FORWARD CONVERTERS

The forward converter is another class of buck-derived isolated dc-to-dc converters. While also derived from the buck converter, the forward converter has unique circuit characteristics, not found in the previous bridge-type converters. Distinctive features of the forward converter will become apparent as we study the operation of the converter.

4.6.1 Basic Operational Principles

Functional basics of the forward converter are first explained using a conceptual converter configured with an ideal transformer. Figure 4.28(a) shows the circuit diagram of a conceptual forward converter that employs a 1 : 1 ideal transformer. The converter also has the configuration of the buck-derived isolated converter shown in Fig. 4.20(b). However, the structure of the switch network differs from that of the previous bridge-type converters. The switch network contains one active switch, one ideal two-winding transformer, and two diodes. This switch network is the simplest among all the switch networks used in buck-derived isolated converters.

The operation of the conceptual forward converter is illustrated in Fig. 4.28(b). When the switch is closed, the positive voltage appears at the *dotted* terminal of the secondary transformer winding. During this period, D_1 is turned-on and D_2 is reverse-biased by the secondary winding voltage v_S. Therefore, the switch network current, i_N, flows through D_1 and the switch network voltage, v_N, equals to the input voltage V_S. During this period, energy is delivered in the *forward* direction through the ideal transformer.

When the switch is opened, both the primary current and secondary current are identically zero according to the current equation of the ideal two-winding transformer. In this period, the ideal transformer is functionally isolated from the converter circuit. The switch network current i_N now freewheels through D_2 and v_N thus becomes zero. The switch network produces the required waveforms for v_N and i_N, and the output voltage is given by

$$V_O = \bar{v}_N(t) = DV_S \tag{4.83}$$

and the output current is given by

$$I_O = \bar{i}_N(t) = \frac{V_O}{R} \tag{4.84}$$

The operation of the conceptual forward converter is identical to that of the buck converter.

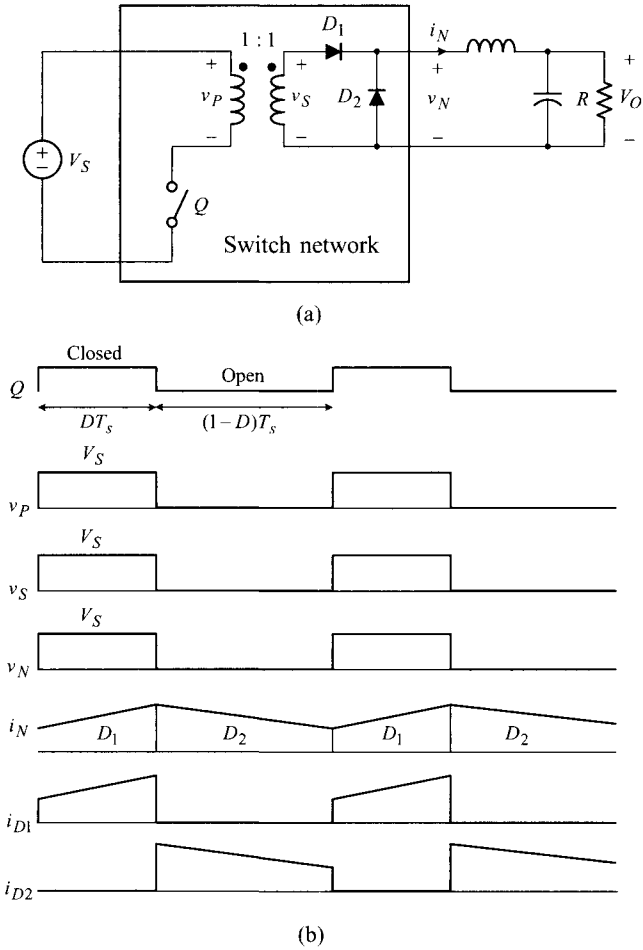


Figure 4.28 Conceptual forward converter with ideal transformer. (a) Circuit diagram. (b) Major circuit waveforms.

Reset Problem and Reset Circuit

When the ideal transformer is replaced with a practical transformer, the conceptual forward converter in Fig. 4.28 immediately becomes inoperative. Figure 4.29(a) shows the switch network including the magnetizing inductance of a practical transformer. Now, the problem of the converter can readily be seen with the presence of the magnetizing inductance L_m. As shown in Fig. 4.29(b), the voltage across the magnetizing inductance, v_m, does not meet the volt-sec balance requirement. More seriously, the magnetizing current, elevated by the equation $i_m(t) = (V_S/L_m)t$ during an on-time period, instantly loses its path when the active switch is opened. The only way for i_m to maintain its continuity is to divert into the *undotted* terminal of the

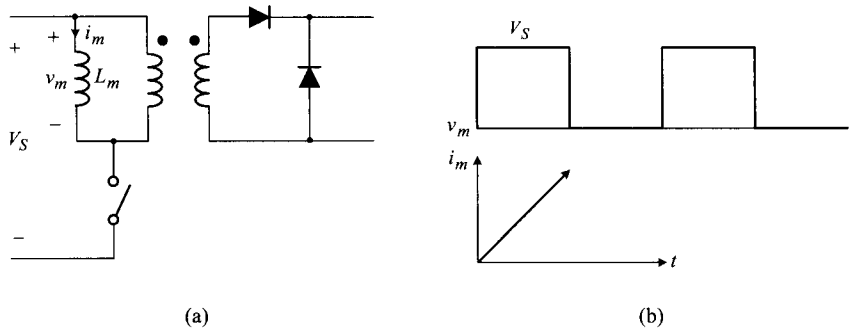


Figure 4.29 Switch network with practical transformer. (a) Circuit diagram. (b) Reset problem.

primary winding of the ideal transformer. If this is the case, the secondary current then must run into the *dotted* terminal of the secondary winding. However, this current flow is not possible because the diode cannot deliver the current from cathode to anode.

As emphasized in Chapter 2, a sudden interruption of i_m incurs a large voltage spike that will destroy the semiconductor switch and other circuit components. The problem associated with the volt-sec balance condition on L_m or the continuity in i_m is termed as the reset problem, indicating the problem of resetting the magnetic flux inside the core to its original state.

A variety of auxiliary circuits are employed as a means of meeting the volt-sec balance condition on L_m while providing a continuous path for i_m. The auxiliary circuits, applied to practical forward converters to solve the reset problem, are called reset circuits.

Switch Network with Zener Diode Reset

A Zener diode is often employed to meet the volt-sec balance condition on L_m, while providing the freewheeling path for i_m. Figure 4.30 shows the Zener diode reset circuit which utilizes a pair of Zener and regular diodes across the primary winding of the transformer. During an on-time period, the regular diode is reverse-biased and the Zener diode reset circuit does not interfere with the circuit operation. The magnetizing current linearly increases with a slope V_S/L_m during this period.

During an off-time period, the magnetizing current i_m *activates* the Zener diode and circulates through the loop formed by the magnetizing inductance, Zener diode, and regular diode. In this period, the primary and secondary currents of the ideal transformer are both zero: $i'_p = i_{D1} = 0$. The breakdown voltage of the Zener diode, V_Z, is applied to L_m in the negative polarity and i_m thus linearly decreases with a slope $-V_Z/L_m$. When i_m is reduced to zero, the regular diode turns off and remains off until the onset of the next off-time period. The waveforms for v_m and i_m are shown in Fig. 4.30(b). The volt-sec balance condition on L_m implies

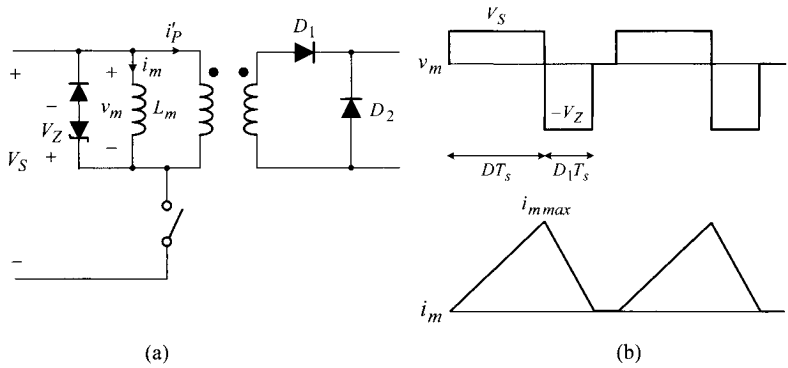


Figure 4.30 Switch network with Zener diode reset. (a) Circuit diagram. (b) Major circuit waveforms.

$$V_S DT_s = V_Z D_1 T_s \tag{4.85}$$

where D_1T_s is the fraction of the off-time period in which the magnetizing current is present. The magnetizing current i_m attains its peak value at the end of the on-time period and returns to zero during the off-time period, thus resetting the magnetic flux to its initial state.

While the Zener diode reset circuit is simple in structure and operation, it provides a lossy reset. The energy transferred to L_m during the on-time period is dissipated at the Zener diode during the off-time period. Accordingly, the Zener diode reset circuit is rarely used for applications where efficiency is an important consideration.

Many alternative reset circuits are available for forward converters. Some reset circuits offer a lossy reset while others operate losslessly. All these reset circuits do not alter the basic operation of the forward converter, yet only function during the off-time period to meet the volt-sec balance condition on L_m while maintaining the continuity in i_m. In other words, the forward converter follows the simple operation of the conceptual converter shown in Fig. 4.28, while bypassing the reset problem with an appropriate reset circuit.

Switch Network with Tertiary Winding Reset

It is also possible to reset the transformer using an additional winding. This alternative reset scheme is shown in Fig. 4.31. The reset is performed by the tertiary winding wound on the same magnetic core on which the original transformer is built. Figure 4.31(a) shows a switch network employing the tertiary winding reset. The structure of the three-winding transformer is also shown. For simplicity of discussions, a turns ratio of $N_P : N_S : N_T = 1 : 1 : 1$ is assumed for the three-winding transformer. Figure 4.31(b) shows the major circuit waveforms of the switch network. Referring to Fig. 4.31, the operational cycle of the switch network is divided into three periods.

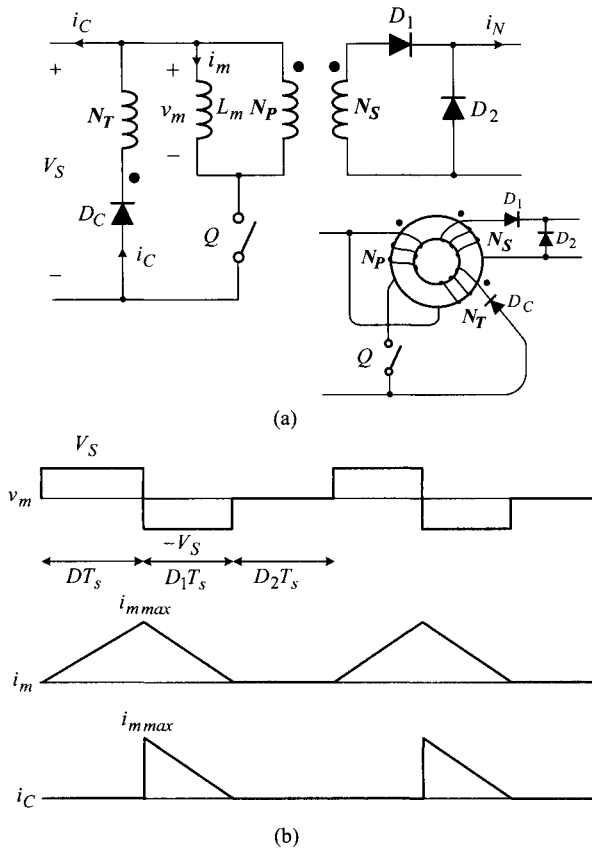


Figure 4.31 Switch network with tertiary winding reset. (a) Circuit diagram. (b) Major circuit waveforms.

On-Time Period DT_s: This period corresponds to the interval in which the active switch Q is closed. The input voltage V_S appears at all the three transformer windings in a positive polarity (with the positive voltage at the *dotted* winding terminal). Accordingly, the diode D_1 is forward-biased while other two diodes are reverse-biased. In particular, the diode at the tertiary winding, the *reset diode* D_C, is reversed-biased by $2V_S$ – the input voltage V_S plus the voltage across the tertiary winding, which is V_S for the 1 : 1 : 1 transformer turns ratio. The output current of the switch network, i_N, flows out of D_1 while the same current runs into the *dotted* terminal of the primary winding. The magnetizing current i_m increases linearly with a slope V_S/L_m. The sum of the magnetizing current and primary winding current passes through Q_1. The energy in the magnetizing inductance gradually increases and reaches the peak value at the end of this period.

Reset Period D_1T_s: This period starts when the active switch is opened, and ends when the magnetizing current i_m is reduced to zero. Opening the active switch triggers the reset diode D_C to conduct and deliver i_C through the tertiary winding. The tertiary winding current i_C flows into the voltage source V_S connected across the left-hand side of the switch network. This enables the magnetizing current i_m to run continuously while satisfying the current equation of the 1 : 1 : 1 ideal transformer. The magnetizing current i_m now circulates through the loop formed by the magnetizing inductance and primary transformer winding. This current is coming out of the *dotted* terminal of the primary winding. The continuous flow of i_m is possible because the same current flows into the *dotted* terminal of the tertiary winding, $i_C = i_m$, while the secondary winding carries *zero* current, as illustrated in Fig. 4.31(b). The turn-on of D_C also forces all the three windings to take V_S in a negative polarity (with the negative voltage at the *dotted* terminal). Accordingly, D_1 is reverse-biased and i_N now freewheels through D_2.

The input voltage V_S is applied to the magnetizing inductance L_m in the negative polarity and i_m thus decreases linearly with a slope $-V_S/L_m$. As i_m decays from its peak, the energy stored in L_m is transferred back to the voltage source located at the left-hand side of the switch network. Thus, the circuit provides a lossless reset – all the energy delivered to the magnetizing inductance L_m during the on-time period is fully recovered by the voltage source during the reset period.

Recess Period D_2T_s: When the condition $i_C = i_m = 0$ is reached, the reset diode D_C turns off and remains off until the next reset period. All the currents and voltages associated with the switch network are zero in this period.

With the 1 : 1 : 1 transformer turns ratio, the rising slope of i_m during the on-time period is the same as the decaying slope during the reset period. This implies that the maximum duty ratio of the active switch should be limited to 0.5 ($0 < D < 0.5$) for proper operation of the converter. When the duty ratio exceeds 0.5, the magnetizing current will increase cycle-by-cycle, and the magnetizing inductance will eventually saturate, leading to a fatal circuit failure.

4.6.2 Tertiary-Winding Reset Forward Converter

A forward converter is configured by combining the switch network discussed in the previous section and low-pass filter circuit. The resulting converter is shown in Fig. 4.32, which is referred to as the tertiary-winding reset forward converter. In the tertiary-winding reset circuit in Fig. 4.32(a), the primary and tertiary windings retain the $N_P : N_T = 1 : 1$ turns ratio, yet the primary and secondary windings have an $N_P : N_S = 1 : n$ turns ratio. The tertiary winding is also called the *reset winding*. Figure 4.32(a) also shows the typical magnetizing current i_m. Figure 4.32(b) depicts three subcircuits of the converter, each representing the converter circuit during the on-time, reset, or recess period. Expressions of major circuit waveforms, derived from these three subcircuits, are listed in Table 4.7.

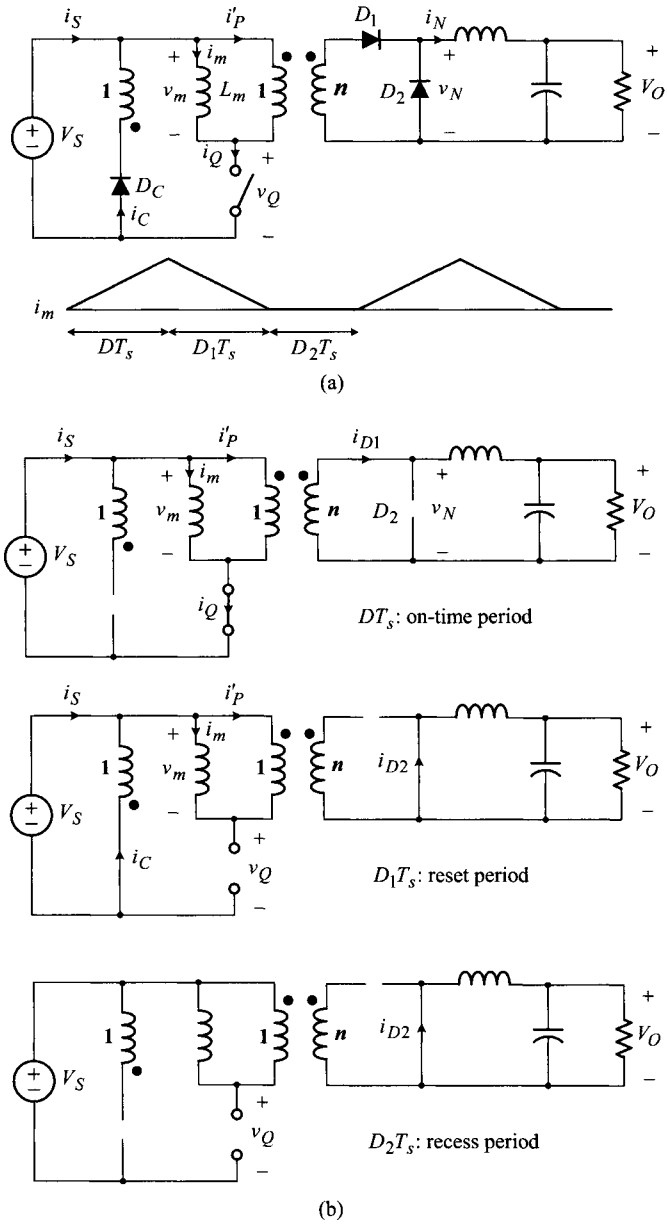


Figure 4.32 Tertiary-winding reset forward converter. (a) Circuit diagram and magnetizing current. (b) Three subcircuits.

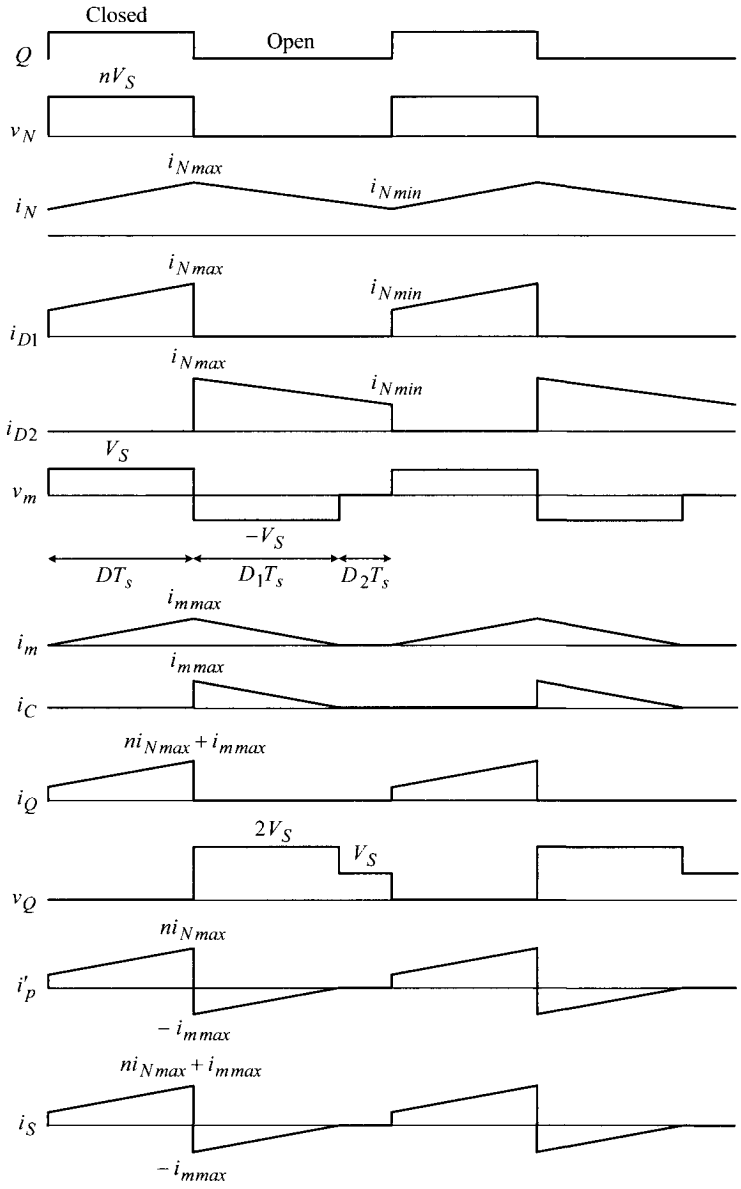


Figure 4.33 Waveforms of tertiary-winding reset forward converter.

Table 4.7 Expressions for Circuit Variables of Tertiary-Winding Reset Forward Converter

	On-time period	Reset period	Recess period
v_N	nV_S	0	0
v_m	V_S	$-V_S$	0
i_m	$\frac{V_S}{L_m}t$	$-\frac{V_S}{L_m}t$	0
i_C	0	$-\frac{V_S}{L_m}t$	0
i_N	$\frac{nV_S - V_O}{L}t$	$-\frac{V_O}{L}t$	$-\frac{V_O}{L}t$
i_{D1}	i_N	0	0
i_{D2}	0	i_N	i_N
i'_P	ni_N	$-i_m$	0
i_Q	$i_m + i'_P$	0	0
i_S	i_Q	$-i_C$	0
v_Q	0	$2V_S$	V_S

Figure 4.33 shows the circuit waveforms, constructed using the equations in Table 4.7. The waveforms indicate that the operation of the forward converter is identical to that of the conceptual converter in Fig. 4.28, except for the waveforms associated with the magnetizing inductance and reset winding. The output voltage of the converter is given by

$$V_O = \bar{v}_N(t) = nDV_S \tag{4.86}$$

with the $1 : n$ turns ratio between the primary and secondary windings.

The peak value of i_m is given by

$$i_{m\,max} = \frac{V_S}{L_m}DT_S \tag{4.87}$$

The maximum value for the the switch network current i_N is given by

$$i_{N\,max} = \frac{V_O}{R} + \frac{1}{2}\frac{nV_S - V_O}{L}DT_s \tag{4.88}$$

Table 4.8 Steady-State Analysis of Tertiary-Winding Reset Forward Converter

Circuit variable	Expression
V_O	$nDV_S = 0.5 \cdot 0.25 \cdot 64 = 8$ V
$v_{N\,max}$	$nV_S = 0.5 \cdot 64 = 32$ V
I_N	$\frac{V_O}{R} = \frac{8}{1} = 8$ A
Δi_N	$\frac{nV_S - V_O}{L} DT_s = \frac{0.5 \cdot 64 - 8}{40 \times 10^{-6}} 0.25 \cdot 20 \times 10^{-6} = 3.0$ A
$i_{N\,max}$	$I_N + \frac{1}{2}\Delta i_N = 8.0 + \frac{1}{2}3.0 = 9.5$ A
$i_{N\,min}$	$I_N - \frac{1}{2}\Delta i_N = 8.0 - \frac{1}{2}3.0 = 6.5$ A
$v_{m\,max}$	$V_S = 64$ V
$v_{m\,min}$	$-V_S = -64$ V
$i_{m\,max}$	$\frac{V_S}{L_m} DT_s = \frac{64}{200 \times 10^{-6}} 0.25 \cdot 20 \times 10^{-6} = 1.6$ A
$v_{Q\,max}$	$2V_S = 2 \cdot 64 = 128$ V

The minimum value of i_N is given by

$$i_{N\,min} = \frac{V_O}{R} - \frac{1}{2}\frac{nV_S - V_O}{L} DT_s \tag{4.89}$$

From these values, the peak and valley values of the other current waveforms can readily be evaluated.

The tertiary-winding reset forward converter is one of most popular converter topologies. Advantages of this converter include the lossless reset and minimal component count. Due to the lossless reset, efficiency of the converter can be high, compared with other forward converters with a lossy reset scheme. This converter uses only one active switch, while handling the power level comparable to that of the half-bridge converter.

There are many other variations of the forward converter with lossless reset. One popular converter topology with lossless reset is the forward converter that employs two active switches and one two-winding transformer, known as the two-switch forward converter. The operation of this converter is described in the next section.

■ **EXAMPLE 4.6 Steady-State Operation of Forward Converter**

This example illustrates the steady-state analysis and major circuit waveforms of a tertiary-winding reset forward converter. The operational conditions and circuit parameters of the forward converter are $V_S = 64$ V, $L_m = 200\,\mu$H, $N_P : N_S : N_T = 1 : 0.5 : 1$, $L = 40\,\mu$H, $C = 400\,\mu$F, $R = 1\,\Omega$, $T_s = 20\,\mu$s, and $D = 0.25$. For the given power stage parameters and operating conditions, steady-state values of major circuit variables are evaluated using the previous analysis results. The steady-state values are listed in Table 4.8 and the simulated circuit waveforms are given in Fig. 4.34.

4.6.3 Two-Switch Forward Converter

As another variation of the forward converter, Fig. 4.35(a) shows the two-switch forward converter. The converter employs two synchronized active switches, Q_1 and Q_2, and two diodes, D_1 and D_2, in the primary side of the switch network. The remaining part of the switch network contains a two-winding transformer and two other rectification diodes. When the two synchronized active switches are turned-on, the converter presents the on-time subcircuit. The on-time subcircuit of this converter is identical to that of the previous tertiary-winding reset forward converter.

When the two synchronized switches are turned-off, the magnetizing current i_m turns on the two diodes, D_1 and D_2, in the primary side of the circuit, and freewheels through the loop formed by L_m, D_1, D_2, and the voltage source V_S. When D_1 and D_2 conduct, the input voltage V_S is applied to the magnetizing inductance L_m in the negative polarity. Thus, the magnetizing current ramps down with a slope $-V_S/L_m$. This period is referred to as the reset period, and D_1 and D_2 are called the reset diodes. In the reset period, the energy stored in the magnetizing inductance is recovered by the voltage source V_S, thereby offering a lossless reset.

When the condition $i_m = i_D = 0$ is reached, the reset diodes turn off and the recess period starts. Figure 4.35(b) shows the three subcircuits, each valid in the respective operational period of the converter. Figure 4.36 shows the circuit waveforms of the converter, constructed using the subcircuits in Fig. 4.35(b). The shapes and peak values of the circuit waveforms are nearly identical to those of the tertiary-winding reset forward converter. The only difference is the peak value of the switch voltage v_Q during the reset and recess periods, which is half the previous case.

4.7 SUMMARY

In this chapter, we studied an important family of dc-to-dc converters, focusing on their topological origins, operational principles, and circuit waveforms. We discussed the evolution of the buck converter into two other basic converters. The boost converter is viewed as an inverse buck converter, while the buck/boost converter is derived from the cascaded connection of the buck converter and boost converter.

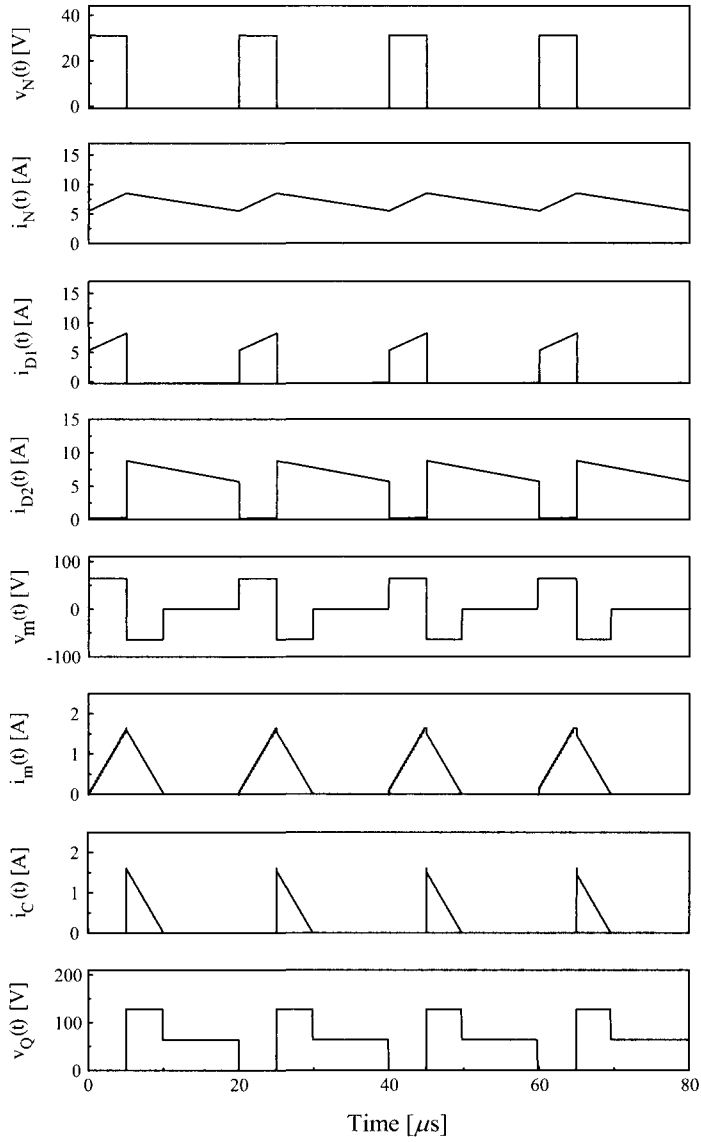


Figure 4.34 Circuit waveforms of tertiary-winding reset forward converter.

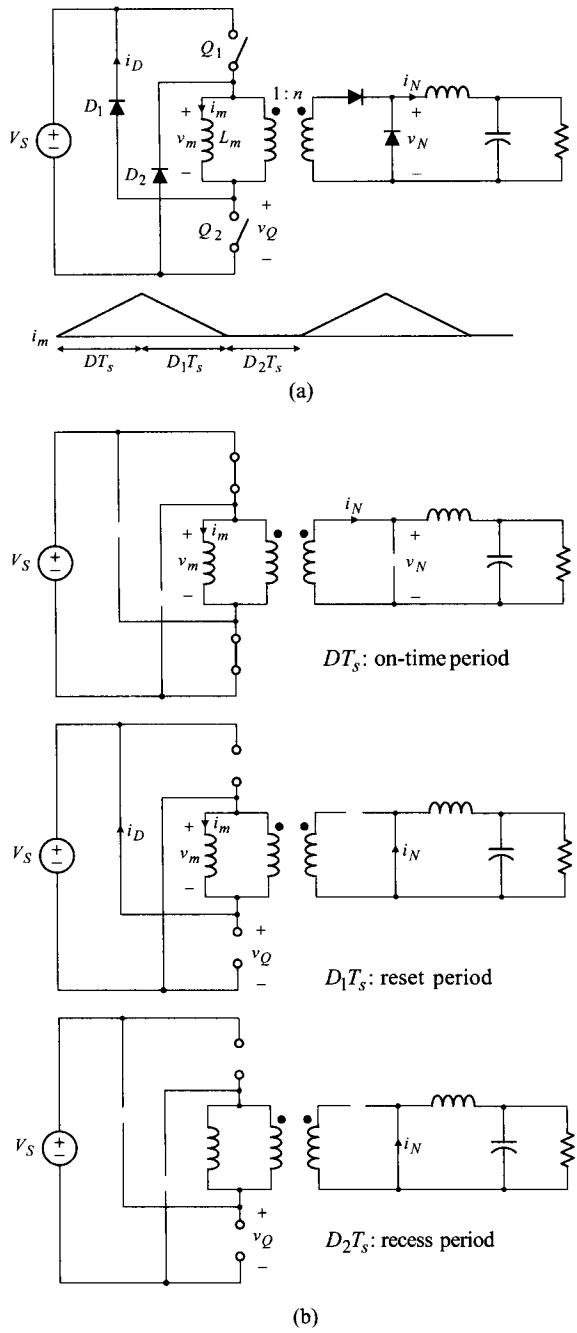


Figure 4.35 Two-switch forward converter. (a) Circuit diagram. (b) Three subcircuits.

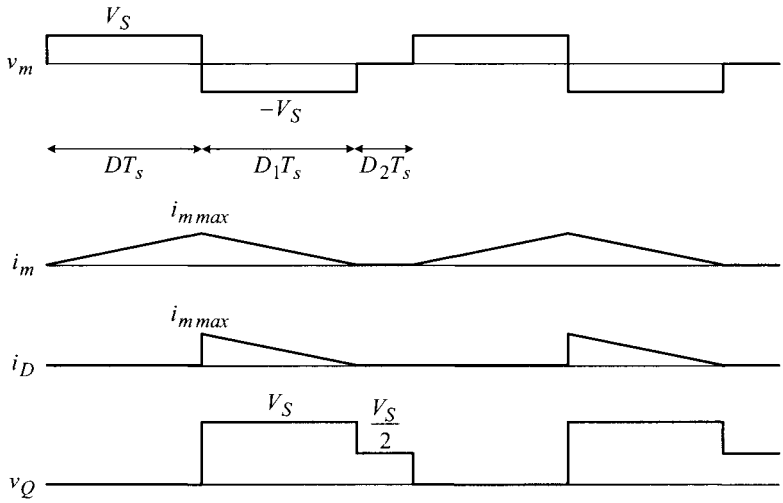


Figure 4.36 Circuit waveforms of two-switch forward converter.

The operations of these newly introduced basic converters are studied using the circuit analysis techniques developed in Chapter 3.

Addition of a transformer to the three basic converters creates a number of new isolated dc-to-dc converters. The simplest among them is the flyback converter whose operation closely mimics that of the buck/boost converter while providing an input-output isolation. A number of isolated dc-to-dc converters are derived from the buck converter by replacing the single-pole double-throw (SPDT) switch with a switch network. Depending on the structure of the switch network, these converters are classified as the full-bridge, half-bridge, and push-pull converter. The operation of these bridge-type buck-derived converters has proven to be equivalent to that of the buck converter. As the second example of buck-derived isolated converters, the forward converter is studied, which employs a variety of auxiliary circuits to reset the transformer in the switch network. The two most widely-used forward converters, the tertiary-winding reset forward converter and two-switch forward converter, are studied in detail.

REFERENCES

1. R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, Kluwer Academic Publishers, 2001.
2. R. Severns and G. Bloom, *Modern Dc-to-Dc Switchmode Power Converter Circuits*, Van Nostrand Reinhold, 1985.
3. M. K. Kazimierczuk, *Pulse-width Modulated DC-DC Power Converters*, John Wiley & Sons, Hoboken, NJ, 2008.

PROBLEMS

4.1* Consider the circuits shown in Fig. P4.1 and answer the questions.

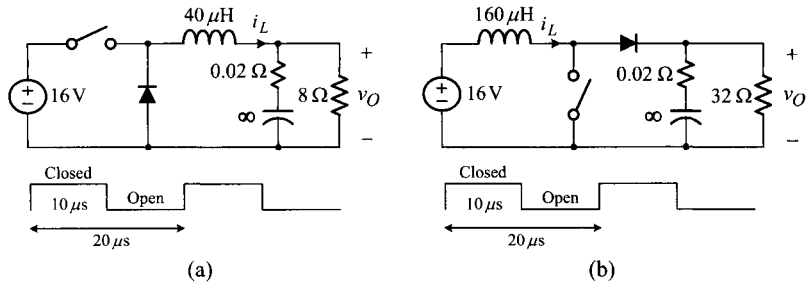


Fig. P4.1

a) For Circuit (a), sketch the steady-state waveforms of the inductor current, i_L, and output voltage ripple, $\tilde{v}_O = v_O - V_O$, for the two switching periods. Show the maximum and minimum values of the waveforms.

b) Repeat **a)** for Circuit (b).

4.2** In the two circuits shown in Fig. P4.2, Q_1 and Q_2 are ideal bidirectional switches which deliver the current in the forward and reverse directions. The switch drive signals shown in Fig. P4.2 are commonly applied to Circuit (a) and Circuit (b).

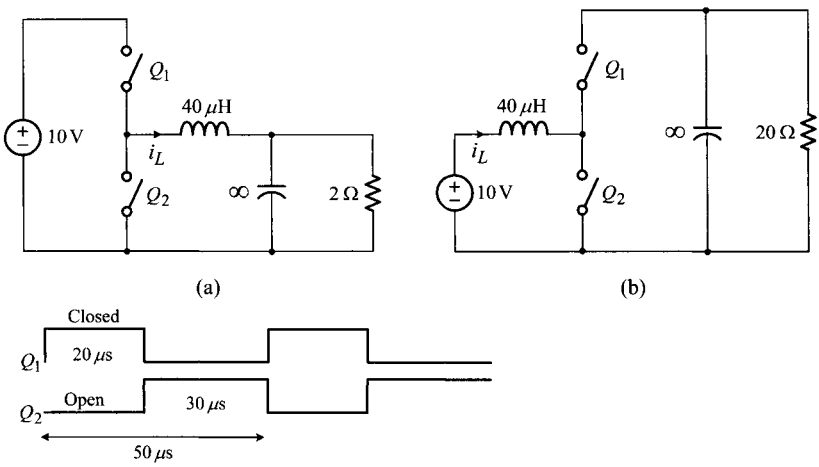


Fig. P4.2

a) For Circuit (a), sketch i_L for the two operational periods. Show the maximum and minimum values of the waveform.

b) Repeat **a)** for Circuit (b).

4.3 Figure P4.3 shows a boost converter along with its switch drive signal.

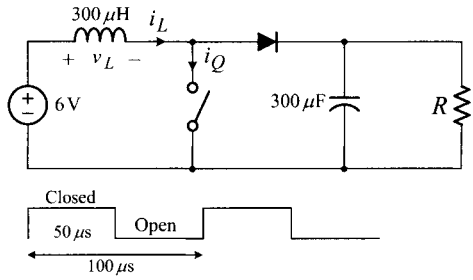


Fig. P4.3

a) Sketch the steady-state waveforms for i_L and v_L when $R = 3\ \Omega$. Show the maximum, minimum, and average values of each waveform.

b) Now assume the load resistor is accidentally disconnected so that $R = \infty$.
i) Sketch the i_Q waveform. Show the maximum value of i_Q.
ii) Explain the behavior of the output voltage. What would happen to the output capacitor and converter circuit?

4.4* Consider the two converters shown in Fig. P4.4 and answer the questions.

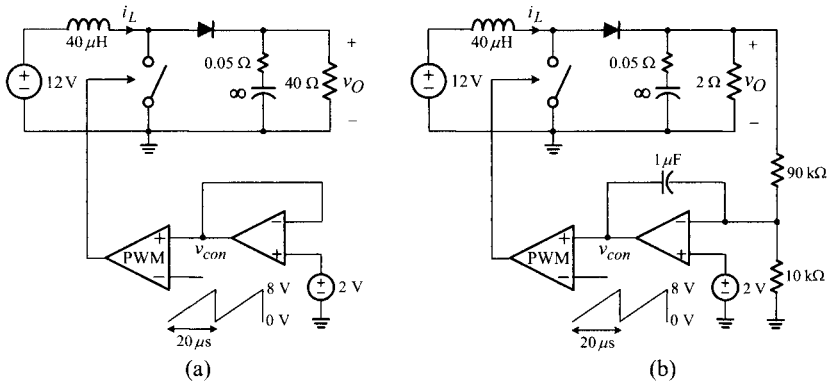


Fig. P4.4

a) For Converter (a), determine the following items:
i) operational mode, CCM or DCM **ii)** average inductor current, I_L
iii) inductor current ripple, Δi_L **iv)** output voltage ripple, Δv_O
v) average control voltage, $\bar{v}_{con}$

b) Repeat **a)** for Converter (b).

4.5** The maximum voltage that a switching device should block during the operation is called the voltage stress. Similarly, the maximum current that a

switching device should carry is called the current stress. Referring to the boost converter shown in Fig. P4.5, answer the questions.

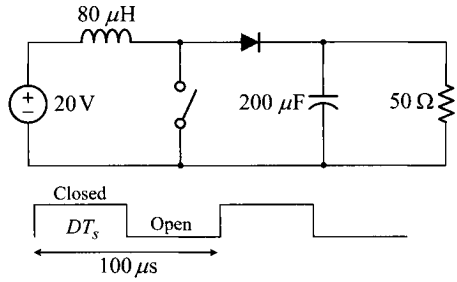


Fig. P4.5

a) Find the voltage stress and current stress of the MOSFET and diode when $D = 0.6$.

b) Repeat **a)** for $D = 0.9$.

4.6* Consider the dc-to-dc power conversion system shown in Fig. P4.6. All the converters operate in CCM with a duty ratio of $D = 0.4$. Evaluate the average values of the inductor currents: $\bar{i}_{L1}$, $\bar{i}_{L2}$, and $\bar{i}_{L3}$.

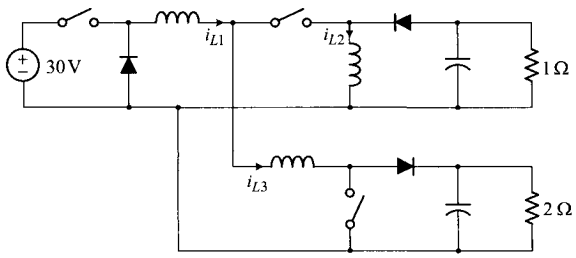


Fig. P4.6

4.7** Assume all the circuit components are ideal in the converter circuits shown in Fig. P4.7. For each converter circuit, calculate the average values for the control voltage v_{con} and output voltage V_O in CCM operation.

4.8 Figure P4.8 shows a closed-loop controlled boost converter. Answer the questions.

a) Sketch the steady-state waveforms for v_{con}, i_L, i_D, and $\tilde{v}_o = v_O - V_O$ when $R = 2\ \Omega$.

b) Show that $R = 16\ \Omega$ is the critical resistance that places the converter on the CCM/DCM boundary.

c) Now assume that R is increased beyond R_{crit}. Sketch a family of i_L waveforms, each with a successively increasing R, to show the transition pattern of the inductor current in DCM operation.

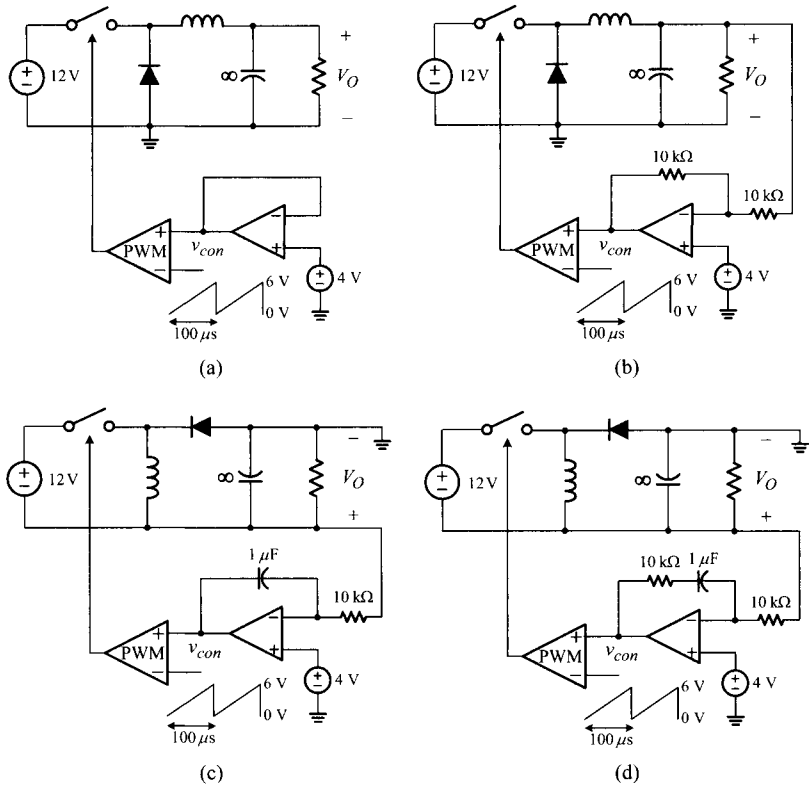


Fig. P4.7

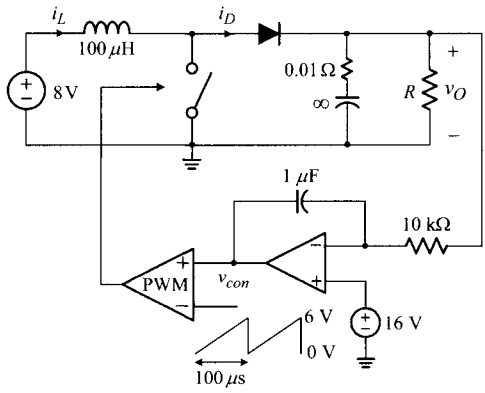


Fig. P4.8

4.9* Consider the four converter circuits shown in Fig. P4.9. For each converter circuit, calculate the reference voltage V_{ref} that is required to produce the output voltage V_O = 20 V in CCM operation.

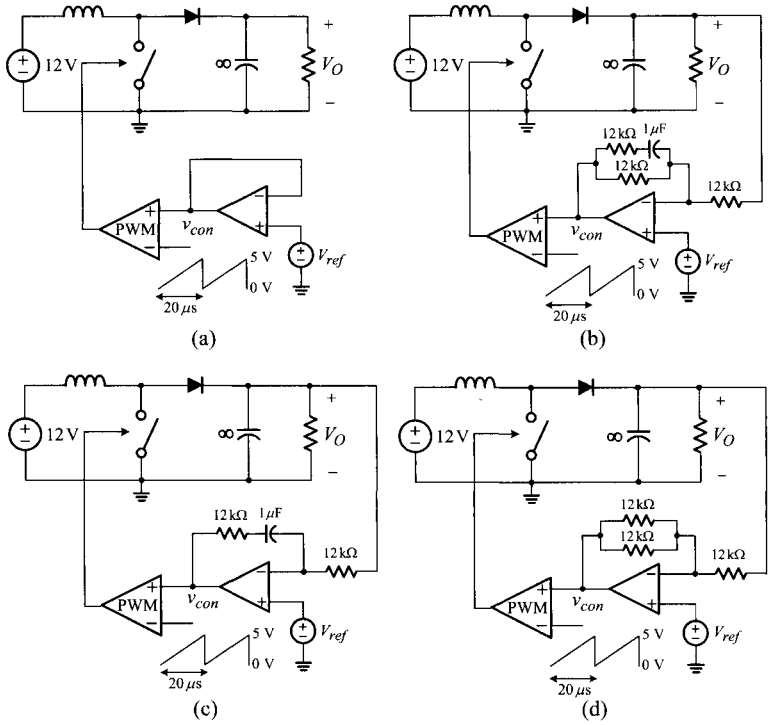


Fig. P4.9

4.10* In the dc-to-dc conversion system shown in Fig. P4.10, assume that all the active switches are driven from the same switch drive signal. Also, assume CCM operation for all three converters. Evaluate the average current running through each semiconductor switch: $\bar{i}_{Q1}$, $\bar{i}_{D1}$, $\bar{i}_{Q2}$, $\bar{i}_{D2}$, $\bar{i}_{Q3}$, and $\bar{i}_{D3}$.

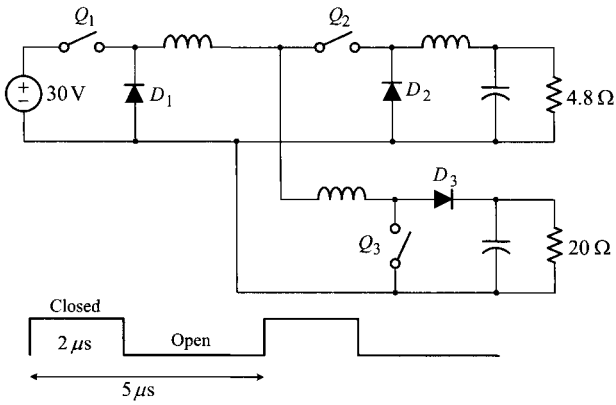


Fig. P4.10

4.11* Consider the four converter circuits shown in Fig. P4.11. For each converter circuit, find the average values of the control voltage, $\bar{v}_{con}$, and output voltage, $\bar{v}_O$.

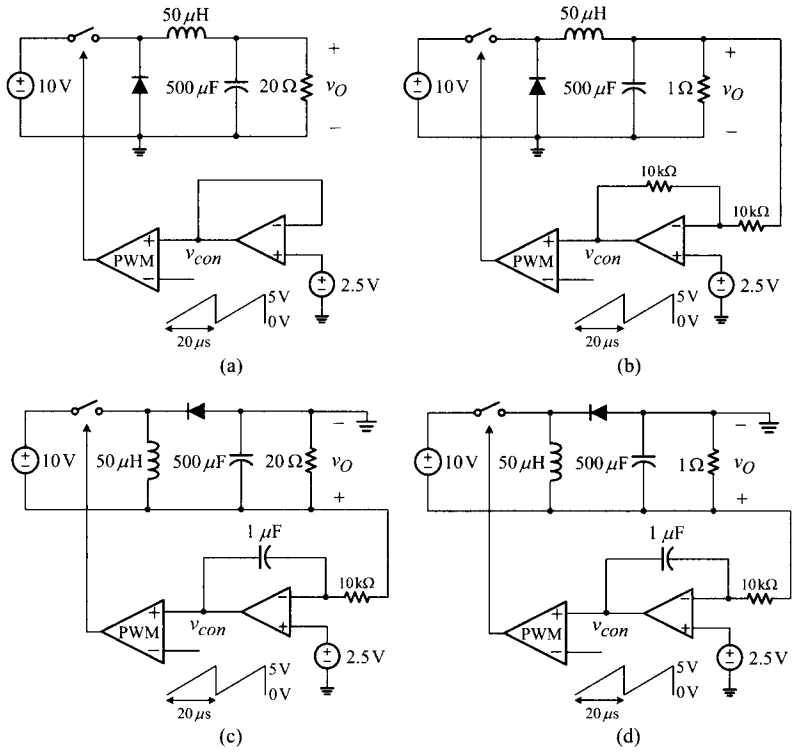


Fig. P4.11

4.12** Figure P4.12 shows three converter circuits. Assume the same switch drive signal for the three converters.

a) Evaluate the average values of the three diode currents: $\bar{i}_{D1}$, $\bar{i}_{D2}$, and $\bar{i}_{D3}$.

b) Evaluate the average values of the three switch currents: $\bar{i}_{Q1}$, $\bar{i}_{Q2}$, and $\bar{i}_{Q3}$.

c) Find the voltage stress of the three switches: $v_{Q1\,max}$, $v_{Q2\,max}$, and $v_{Q3\,max}$.

4.13 Referring to the converter circuit shown in Fig. P4.13(a), answer the following questions.

a) For the switch drive signals in Fig. P4.13(b), sketch the steady-state waveform of i_L for the two switching periods. Label the maximum and minimum values on your sketch.

b) Repeat **a)** for the switch drive signals in Fig. P4.13(c).

c) Repeat **a)** for the switch drive signals in Fig. P4.13(d).

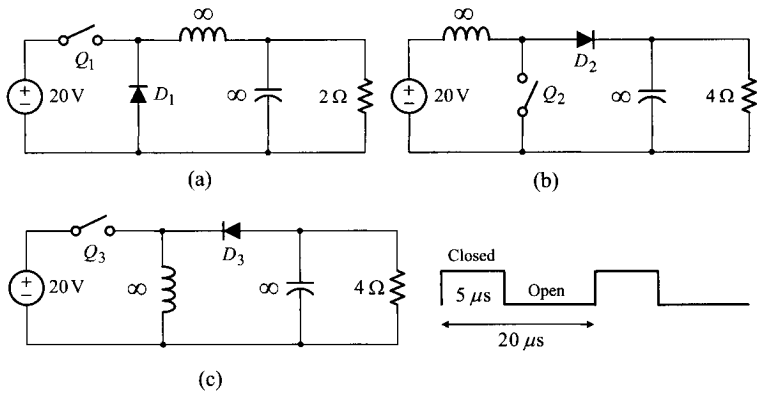


Fig. P4.12

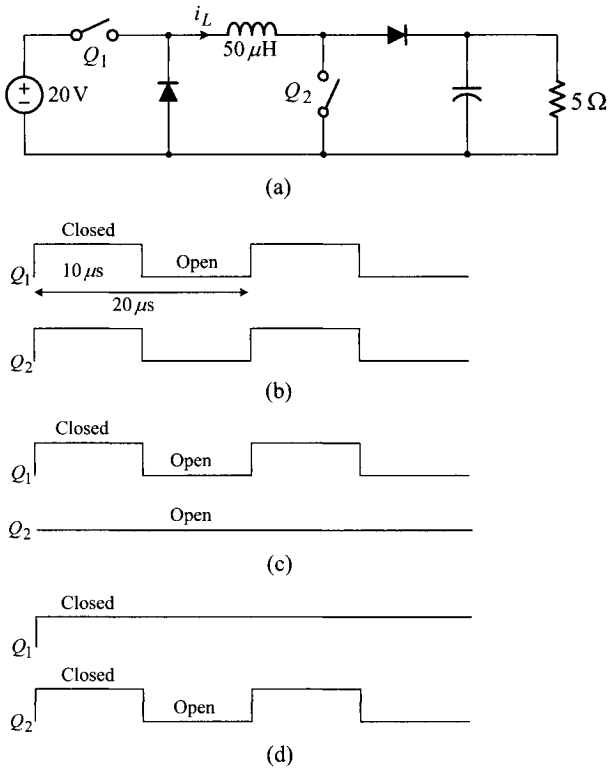


Fig. P4.13

4.14** Figure P4.14 depicts the circuit diagram of a composite converter which is built by cascading the boost converter and buck converter. Referring to the switch drive signals for Q_1 and Q_2, answer the questions.

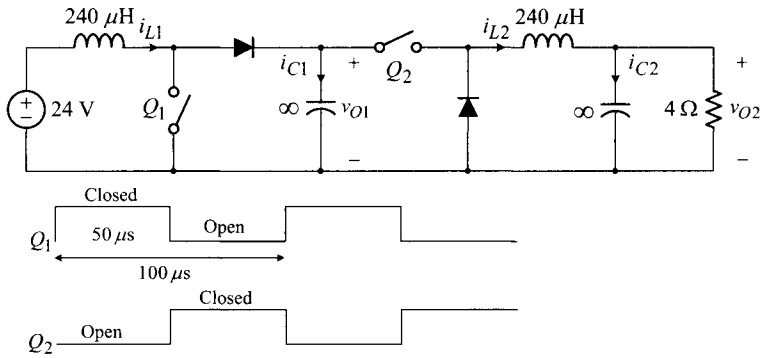


Fig. P4.14

a) Find the average values for v_{O1} and v_{O2}.

b) Sketch the steady-state waveforms of i_{L1} and i_{L2} for the two switching periods. Label the maximum, minimum, and average values of each waveform.

c) Sketch the steady-state waveforms of i_{C1} and i_{C2} for the two switching periods. Label the maximum, minimum, and average values of each waveform.

4.15** Shown in Fig. P4.15 is a buck/boost converter built using the non-ideal switches and practical passive components.

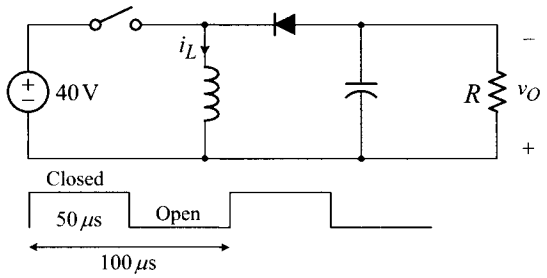


Fig. P4.15

a) During the normal operation, the load resistor is accidentally disconnected so that $R = \infty$. What do you think will happen to the circuit? If you claim a new steady-state operation, find the average values for the output voltage v_O and inductor current i_L. If you claim a catastrophic failure of the circuit, identify the component that is responsible for the failure and state the origin/reason for the component breakdown.

b) Now assume that the load resistor is accidentally shorted, $R = 0$, during the normal operation of the converter. Repeat Problem **a)** under this assumption.

4.16 Figure P4.16 is the circuit diagram of a closed-loop controlled buck/boost converter. Assume that the load resistance R is varied between $6\ \Omega < R < 24\ \Omega$ and find the range of the following operational condition and circuit variables of the converter:

( ) $< D <$ ( ) ( ) $< \bar{v}_{con} <$ ( )

( ) $< i_{Lmax} <$ ( ) ( ) $< \Delta v_{esr} <$ ( )

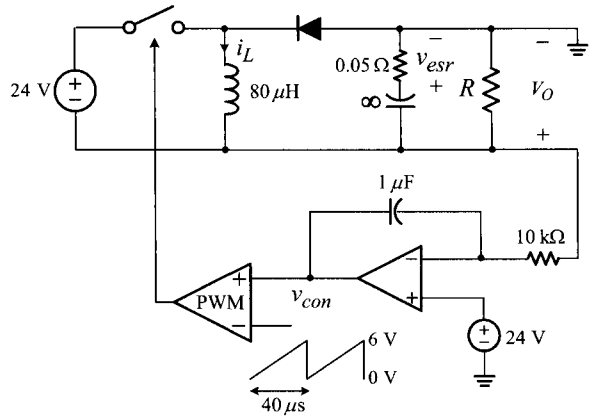


Fig. P4.16

4.17* Figure P4.17 depicts a composite converter circuit and its switch drive signals.

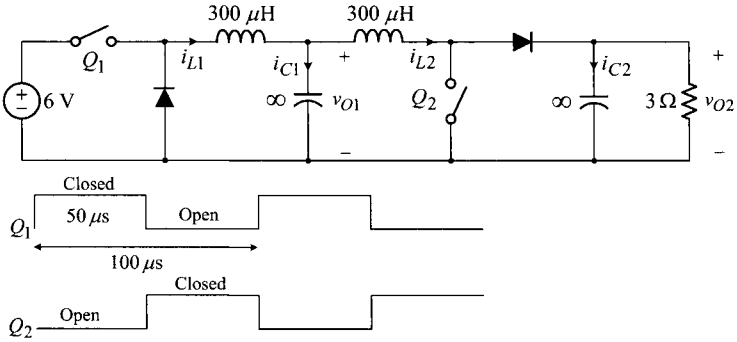


Fig. P4.17

a) Find the average values for v_{O1} and v_{O2}.

b) Sketch the steady-state waveforms of i_{L1} and i_{L2} for the two operational periods. Label the maximum and minimum values of each waveform.

c) Draw the steady-state waveforms of i_{C1} and i_{C2} for the two operational periods. Label the maximum and minimum values of each waveform.

4.18** The three converters in Fig. P4.18 generate the same inductor current waveform shown at the bottom of the figure. For each converter, evaluate the output voltage V_O, load resistance R, and inductance L.

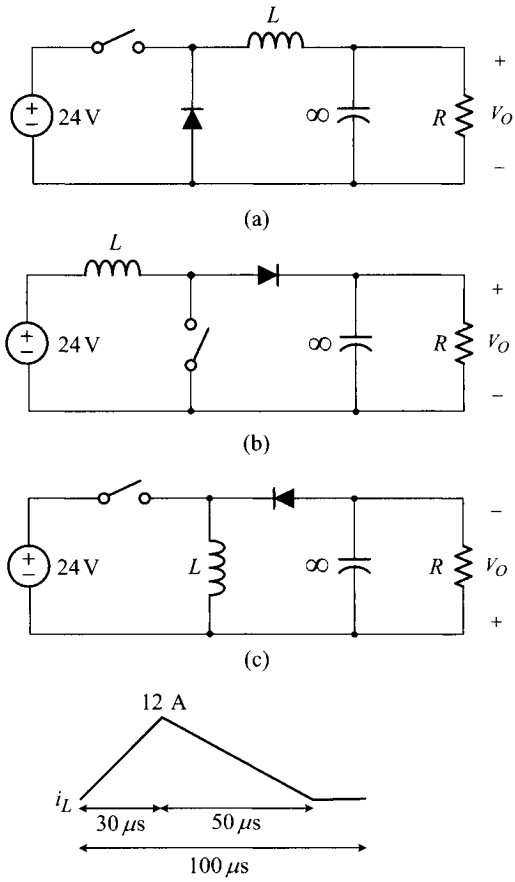


Fig. P4.18

4.19* For the three circuits shown in Fig. P4.19(a), assume that Q_1 and Q_2 are ideal *bidirectional* switches which deliver the current in both the forward and reverse directions.

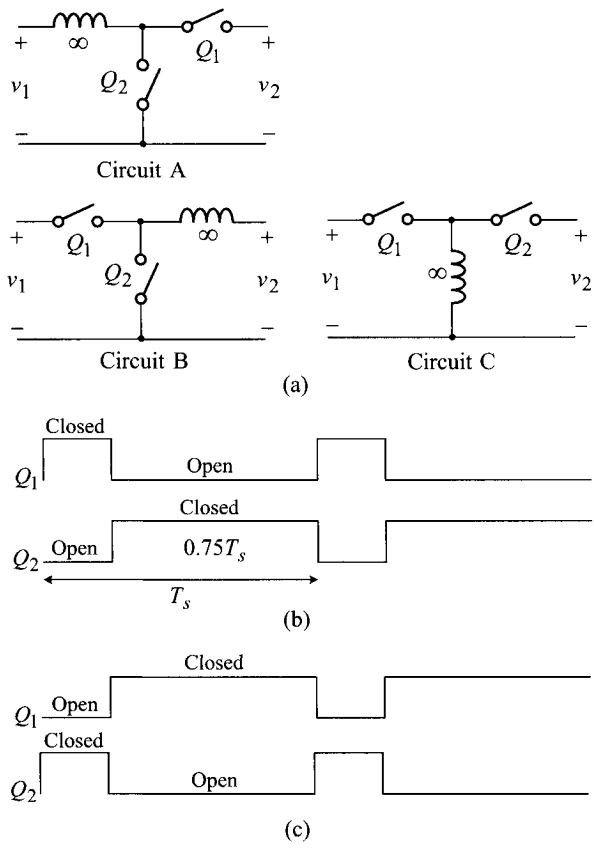


Fig. P4.19

a) Assume that the average value of v_2 is 14 V for all the three circuits. For the switch drive signals in Fig. P4.19(b), find the average value of v_1 in the three circuits in Fig. P4.19(a).

b) Repeat **a)** for the switch drive signals in Fig. P4.19(c).

4.20** The flyback converter discussed in Section 4.4 is modified as shown in Fig. P4.20(a).

a) Figure P4.20(b) illustrates the switch drive signal and other major circuit waveforms labeled in the circuit diagram. Referring to the switch drive signal and circuit parameters, evaluate the numerical values for A, B, C, and D, specified in Fig. P4.20(b).

b) Estimate the time instant at which v_C will increase to 400 V.

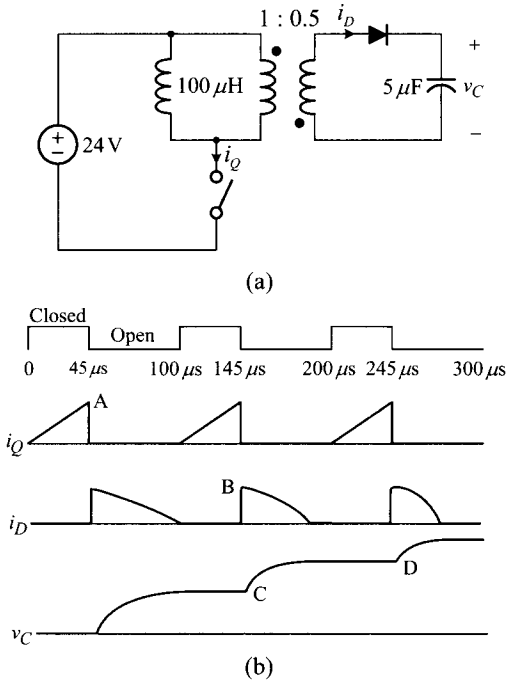


Fig. P4.20

4.21 Consider the half-bridge converter shown in Fig. P4.21 along with its switch drive signals.

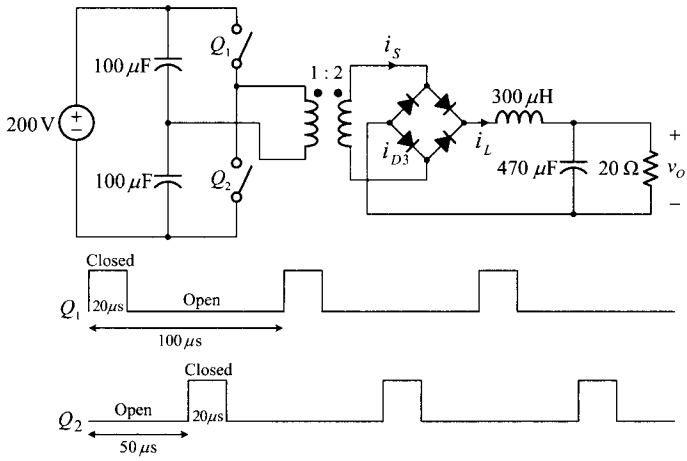


Fig. P4.21

a) Find the average value of the output voltage v_O.

b) Referring to the switch drive signals, sketch i_L, i_S, and i_{D3} for the two switching periods. Show the maximum, minimum, and average values on your sketch.

4.22* Use the flux balance condition and charge balance condition to derive the voltage gain expression

$$\frac{V_O}{V_S} = \frac{D}{1-D}\left(\frac{1}{1+\dfrac{1}{(1-D)^2}\dfrac{R_l}{R}}\right)$$

for the buck/boost converter with inductor winding resistance R_l. This expression was given in (4.36) in the text.

4.23 Consider the circuit shown in Fig. P4.23 and answer the questions.

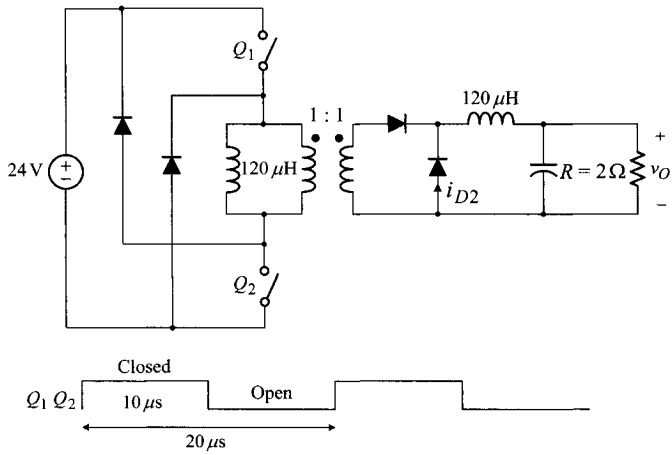


Fig. P4.23

a) Referring to the circuit diagram and switch drive signals, sketch i_{D2} for the two switching periods. Show the maximum, minimum, and average values on your sketch.

b) Now assume that the load resistance R is increased while the other circuit parameters and switch drive signals remain unchanged. With the new load resistor, the output voltage of the converter is enhanced to V_O = 15 V. Under this situation, sketch i_{D2} for the two switching periods. Show the maximum, minimum, and average values on your sketch.

4.24 Figure P4.24 shows a push-pull converter circuit. Referring to the switch drive signals and circuit components values, sketch the steady-state waveforms of v_N, i_N and i_{D1} for the two switching periods. Label the maximum and minimum values on your sketch.

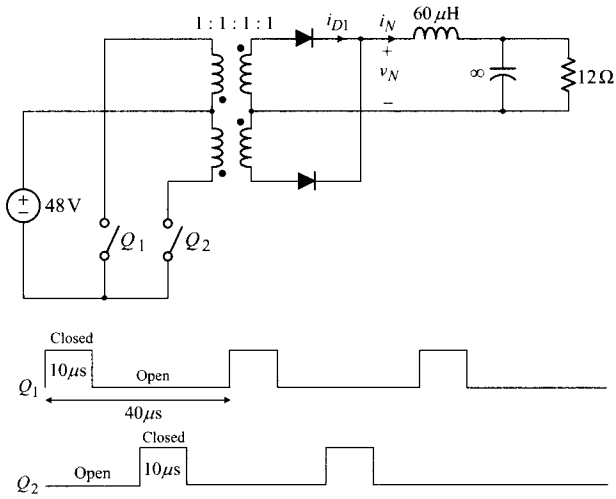


Fig. P4.24

4.25** The forward converter shown in Fig. P4.25 is built using a practical transformer. The number of turns of the three-winding transformer is $N_P = N_S = N_T = 48$. The converter had established steady-state operation with a duty ratio $D = 0.4$. Now assume that the following failure or change occurred to the converter during its steady-state operation:

i) open-circuit failure of D_c **ii)** open-circuit failure of D_2

iii) open-circuit failure of C **iv)** decrease in the duty ratio to $D = 0.15$

v) increase in the duty ratio to $D = 0.65$

For each failure/change listed above, what do you think will happen to the converter? If you claim a catastrophic failure of the circuit, identify the component responsible to the failure and state the origin/reason of the component breakdown. If you claim a new steady-state operation, describe the major change in the circuit operation.

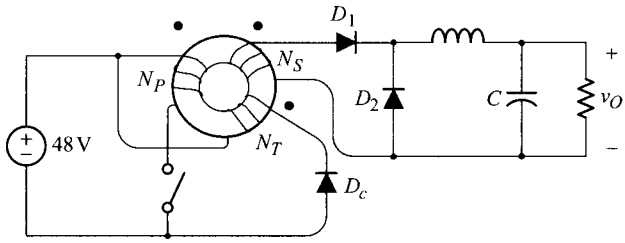


Fig. P4.25

4.26** In the four isolated dc-to-dc converters shown in Fig. P4.26, assume that the transformer has a finite magnetizing inductance.

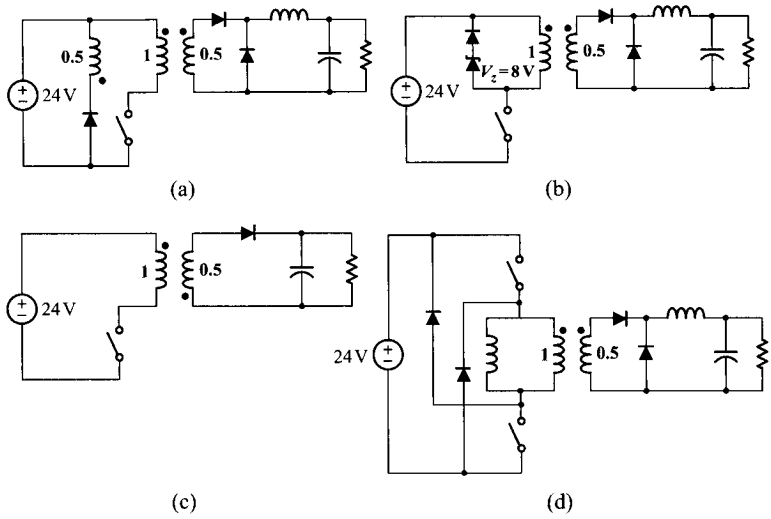


Fig. P4.26

a) Answer the following questions.
i) Which converter would result in the worst power conversion efficiency?
ii) Which converter would offer the largest power handling capacity?
iii) Which converter would minimize the manufacturing cost?

b) For each dc-to-dc converter, find the range of the duty ratio that guarantees proper operation of the converter. Express your answer in the form of ( ) < D < ( ).

c) Now assume that all the converters are closed-loop controlled to produce an output voltage of 2.4 V. Evaluate the voltage stress of the active switch employed in each circuit.

4.27** The following questions concern the topological structure, circuit components, and operational principles of various PWM converters. Answer the questions in a brief and precise manner.

a) The transformer employed in a flyback converter is typically built on the magnetic core to which an air gap is intentionally introduced. Explain the necessity of this practice.

b) While an appropriate reset circuit is required for the forward converter, the flyback converter and bridge-type converters do not require any reset circuit. Explain the reasons for this.

c) Figure P4.27 shows five different converter topologies. For each converter, find the maximum possible value for the output voltage and the voltage stress of the active switch employed in the circuit.

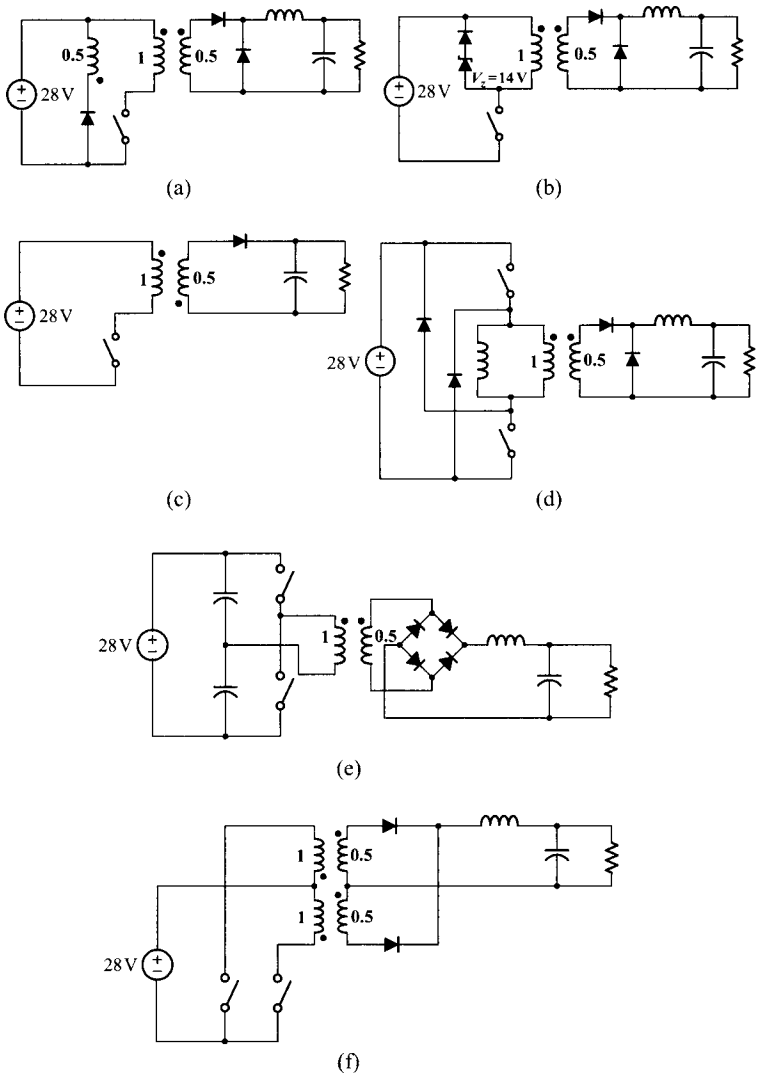

0.5
1
0.5
28 V
(a)
1
0.5
28 V
V_z = 14 V
(b)
1
0.5
28 V
(c)
28 V
1
0.5
(d)
28 V
1
0.5
(e)
1
0.5
1
0.5
28 V
(f)

Fig. P4.27

PART II

MODELING, DYNAMICS, AND DESIGN OF PWM DC-TO-DC CONVERTERS

CHAPTER 5

MODELING PWM DC-TO-DC CONVERTERS

The first part of this book dealt with the power stage configuration and steady-state operation of PWM dc-to-dc converters. This static analysis constitutes one essential part of the dc-to-dc power conversion technology. As introduced in Chapter 1, the dynamic analysis is another critical area in studying the dc-to-dc power conversion. In the dynamic analysis, the dc-to-dc converter is viewed as a closed-loop controlled dynamic system and its characteristics are investigated using an appropriate model. As the prerequisite for the dynamic analysis, this chapter presents the modeling of PWM dc-to-dc converters.

Dc-to-dc converters are a time-variant system in the sense that the topological structure of their power stage constantly varies with time. Depending on the status of the semiconductor switches, dc-to-dc converters exhibit different power stage configurations during operation. In addition, dc-to-dc converters employ the pulsewidth modulation (PWM) process to generate dedicated switch drive signals. The PWM process is a well-known nonlinear process in which the input and output variables are linked by a nonlinear relationship. The time variance of the power stage configuration and nonlinearity of the PWM process collectively classify dc-to-dc converters as a nonlinear time-variant system.

Pulsewidth Modulated Dc-to-Dc Power Conversion. By Byungcho Choi

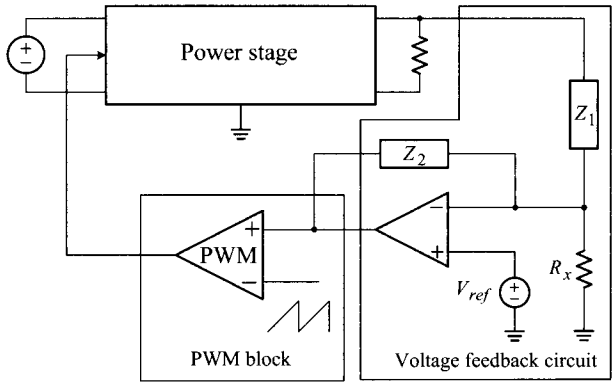


Figure 5.1 Closed-loop controlled PWM converter.

The dynamic analysis of a nonlinear time-variant system is known to be difficult. Conventional circuit analysis techniques are mainly intended for linear time-invariant systems and therefore cannot be directly applied to PWM dc-to-dc converters. While certain analytical methods are available for nonlinear systems, the analysis becomes intractably complicated when adapted into PWM dc-to-dc converters. Accordingly, the analysis of the converter dynamics in the original form can be a very challenging task. The purpose of this chapter is to develop an analytical process, referred to as the modeling in this book, which enables us to overcome the obstacles presented by the time variance and nonlinearity of PWM dc-to-dc converters.

Modeling in general refers to the procedure of describing the dynamic characteristics of a given system in a desired format. The desired format is determined by the object of the modeling. For example, to develop a *simplified model* for a complicate system, the system behavior is expressed by the simple equations that only capture the major system dynamics while ignoring unimportant details. The object of the dc-to-dc converter modeling herein is to establish a systematic method of describing the dynamics of nonlinear time-variant dc-to-dc converters using the *language* and *format* that have been used for linear time-invariant systems. If we achieve this aim, we can analyze the dynamics of dc-to-dc converters in the exact same manner as we analyze linear time-invariant systems.

5.1 OVERVIEW OF PWM CONVERTER MODELING

In this chapter, we study a series of modeling techniques that eventually provides a small-signal model for PWM dc-to-dc converters. The small-signal model is a linear time-invariant circuit model to which all the standard circuit analysis techniques can directly be applied. Figure 5.1 shows a general structure of a closed-loop controlled

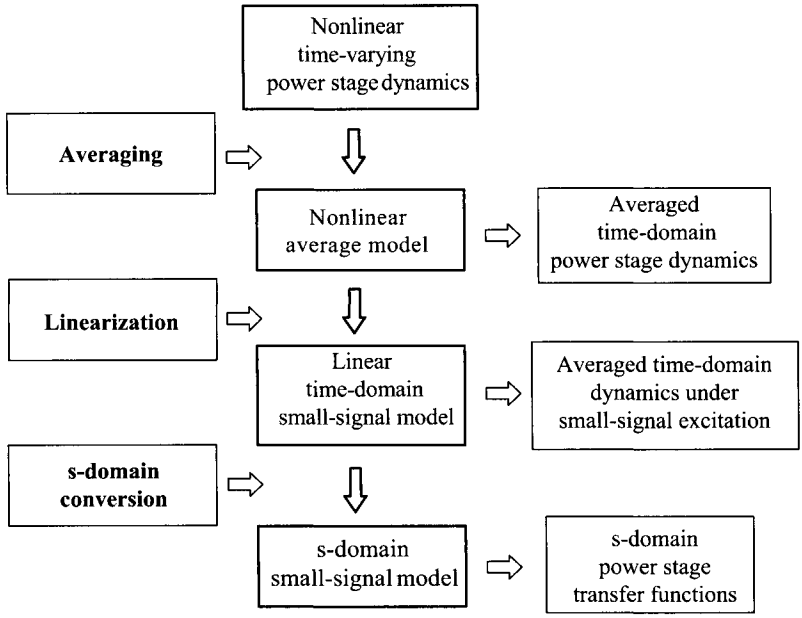


Figure 5.2 Steps of power stage modeling.

PWM converter. Discussions about the converter structure were given in Section 3.6.1.

The converter is divided into three functional blocks for the convenience of modeling: the power stage, PWM block, and voltage feedback circuit. First, each functional block is transformed into the respective small-signal model using various modeling techniques. The small-signal models of the three functional blocks are later merged to yield a complete small-signal model for the closed-loop controlled PWM converter.

Power Stage Modeling

Figure 5.2 illustrates the procedures of power stage modeling. The method of averaging is first applied to the time-varying power stage dynamics. This method provides an average model in which the time variance is removed. In the process of averaging, however, certain nonlinear relationships among circuit variables arise and are embedded into the average model. Thus, the average model is a time-invariant but nonlinear model. The average model describes the averaged time-domain power stage dynamics.

As the second step, the linearization is invoked to deal with the nonlinear relationships incurred during the averaging process. The linearization is a process of approximating the nonlinear relationships among the circuit variables to linear descriptions under small-signal assumption. The linearization thus produces a linear time-invariant small-signal model. This model describes the averaged time-domain

dynamics at the presence of small-signal excitation. As the last step, the time-domain small-signal model is converted into a frequency-domain, or *s-domain*, small-signal model, which provides transfer functions of power stage dynamics. The resulting transfer functions embrace all the standard s-domain analysis techniques and reveal the frequency-domain small-signal dynamics of power stage.

PWM Block Modeling

The PWM process employed in dc-to-dc converters is a typical nonlinear operation. The PWM block receives the input signal from the voltage feedback circuit and produces the switch drive signal as its output. While the input of the PWM block is a continuous analog signal, the output is a periodic pulse waveform, whose cycle-by-cycle pulsewidth is modulated by the input signal. This highly nonlinear functionality can be approximated by a linear expression, given that the input signal only changes *narrowly* and *slowly* within the period of the output of the PWM block. Because most dc-to-dc converters meet this assumption, there exists a simple linear relationship between the input and output signals of the PWM block. This linear relationship is the small-signal gain of the PWM block, called the PWM gain or modulator gain. Details about the modulator gain will be given in Section 5.5.

Voltage Feedback Circuit and Small-Signal Model of PWM Converter

The voltage feedback circuit is a linear time-invariant circuitry which can readily be converted into the small-signal model using standard circuit analysis techniques. The small-signal model for the voltage feedback circuit will be described in Section 5.6.1.

The complete small-signal model for dc-to-dc converters can now be constructed by merging the small-signal models of the power stage, PWM block, and voltage feedback circuit. The resulting small-signal model allows us to perform the dynamic analysis of the nonlinear time-variant dc-to-dc converter using the conventional s-domain analysis techniques.

5.2 AVERAGING POWER STAGE DYNAMICS

Figure 5.3 illustrates the averaging process of the power stage dynamics. Figure 5.3(a) is a conceptual diagram of a PWM dc-to-dc converter containing one single-pole double-throw (SPDT) switch. For the purpose of dynamic modeling, the duty ratio of the SPDT switch is allowed to change with time. This time-varying duty ratio is represented by $\boldsymbol{d}$ to differentiate it from the fixed steady-state duty ratio $\boldsymbol{D}$. For simplicity of ensuing discussions, only the continuous conduction mode (CCM) operation is considered for the PWM converter. The averaging process of PWM converters in discontinuous conduction mode (DCM) operation will be separately discussed in Chapter 9.

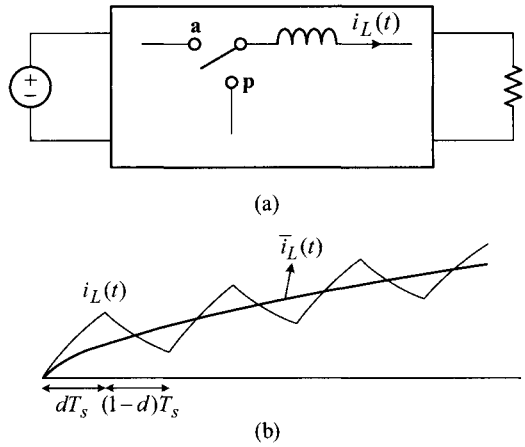


Figure 5.3 Averaging power stage dynamics. (a) Diagram of PWM dc-to-dc converter. (b) Concept of averaging.

Referring to Fig. 5.3, the method of averaging is explained as follows. When the SPDT switch is held at position **a** during dT_s, the power stage presents the on-time subcircuit. Likewise, with the SPDT switch at position **p** during $(1-d)T_s$, the power stage becomes the off-time subcircuit. Figure 5.3(b) illustrates the time variance of the power stage dynamics and concept of averaging. During the on-time period dT_s, the inductor current $i_L(t)$ develops according to the circuit equations of the on-time subcircuit. During the off-time period $(1-d)T_s$, $i_L(t)$ evolves based on the circuit equations of the off-time subcircuit. Accordingly, the inductor current $i_L(t)$ changes its pattern at every switching instant.

The method of averaging is an analytical approach that attempts to produce a smooth waveform that follows the time-averaged trajectory of the inductor current, as illustrated with $\bar{i}_L(t)$ in Fig. 5.3(b). In other words, the method of averaging provides the circuit equations or circuit models that produce the continuous circuit waveforms which track the original waveforms.

As the outcome of past research efforts, two useful averaging methods have been developed for PWM dc-to-dc converters. The first method manipulates the state-space description of the power stage so that the manipulated state-space description predicts the time-averaged dynamics of the power stage. This method is known as the *state-space averaging*.

The second method uses the time-averaged behavior of the circuit variables to develop an average model of the power stage. The average power stage model produces the continuous circuit waveforms that follow the original waveforms. This method is referred to as the *circuit averaging* because it directly averages the circuit variables associated with power stage components.

This section presents both the state-space averaging method and circuit averaging technique, focusing on their theoretical basis and application to the PWM converter

modeling. The relative merit of each method and the equivalence between the two methods are also discussed.

5.2.1 State-Space Averaging

In the method of state-space averaging, an exact state-space description of the power stage is initially formulated, using the concept of the *switching function* which can have different values depending on time. The resulting state-space description is called the switched state-space model. Although the switched state-space model precisely describes the power stage dynamics, it is a time-variant model due to the presence of the switching function. The switched state-space model is then appropriately averaged to yield an averaged state-space model that describes the time-averaged power stage dynamics.

Switched State-Space Model

As the initial step of deriving the switched state-space model, the power stage dynamics are described by separately formulating the state-space description of the on-time subcircuit and the state-space description of the off-time subcircuit. The power stage dynamics during an on-time period are expressed in the form of a state equation

$$\begin{aligned} \frac{d\boldsymbol{x}(t)}{dt} &= \boldsymbol{A}_{on}\boldsymbol{x}(t) + \boldsymbol{B}_{on}v_S(t) \\ v_O(t) &= \boldsymbol{C}_{on}\boldsymbol{x}(t) \end{aligned} \tag{5.1}$$

where $\boldsymbol{x}$ is the state vector, v_S is the input voltage, v_O is the output voltage, and $\{\boldsymbol{A}_{on}\,\boldsymbol{B}_{on}\,\boldsymbol{C}_{on}\}$ are the coefficient matrices of the on-time subcircuit. Similarly, another state equation is written for an off-time period

$$\begin{aligned} \frac{d\boldsymbol{x}(t)}{dt} &= \boldsymbol{A}_{off}\boldsymbol{x}(t) + \boldsymbol{B}_{off}v_S(t) \\ v_O(t) &= \boldsymbol{C}_{off}\boldsymbol{x}(t) \end{aligned} \tag{5.2}$$

where $\{\boldsymbol{A}_{off}\ \boldsymbol{B}_{off}\ \boldsymbol{C}_{off}\}$ are the coefficient matrices of the off-time subcircuit.

The two state equations (5.1) and (5.2) are merged into one single state equation

$$\begin{aligned} \frac{d\boldsymbol{x}(t)}{dt} &= (q(t)\boldsymbol{A}_{on} + (1 - q(t))\boldsymbol{A}_{off})\boldsymbol{x}(t) \\ &\quad + (q(t)\boldsymbol{B}_{on} + (1 - q(t))\boldsymbol{B}_{off})v_S(t) \\ v_O(t) &= (q(t)\boldsymbol{C}_{on} + (1 - q(t))\boldsymbol{C}_{off})\boldsymbol{x}(t) \end{aligned} \tag{5.3}$$

using the notation of the switching function $q(t)$, defined as

$$q(t) = \begin{cases} 1 & \text{for on-time period } dT_s \\ 0 & \text{for off-time period } (1-d)T_s \end{cases} \tag{5.4}$$

The equation (5.3) is called the *switched state-space model* because it contains the switching function $q(t)$.

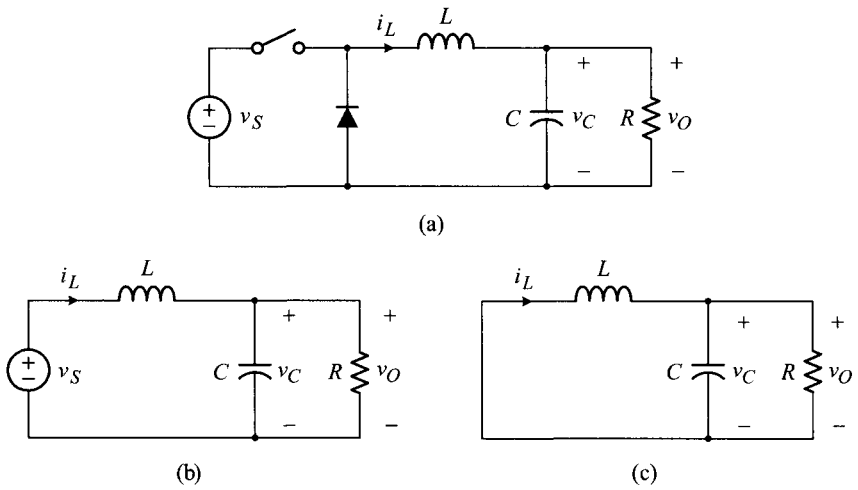


Figure 5.4 Ideal buck converter. (a) Circuit diagram. (b) On-time subcircuit. (c) Off-time subcircuit.

■ EXAMPLE 5.1 Switched State-Space Model of Ideal Buck Converter

This example illustrates the formation of the switched state-space model for the buck converter. The circuit diagram of an *ideal* buck converter without any parasitic resistances is shown in Fig. 5.4, along with its on-time and off-time subcircuits. When the state vector is defined as $\boldsymbol{x} = [i_L \; v_C]^T$, the coefficient matrices of the on-time and off-time subcircuits become

$$\boldsymbol{A}_{on} = \boldsymbol{A}_{off} = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{CR} \end{bmatrix} \tag{5.5}$$

$$\boldsymbol{B}_{on} = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} \tag{5.6}$$

$$\boldsymbol{B}_{off} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{5.7}$$

$$\boldsymbol{C}_{on} = \boldsymbol{C}_{off} = [\,0 \quad 1\,] \tag{5.8}$$

Readers are encouraged to confirm the above coefficient matrices by formulating the state equations of the on-time and off-time subcircuits of the buck converter.

The switched state-space model is obtained by plugging the appropriate coefficient matrices into (5.3)

$$\frac{d\boldsymbol{x}(t)}{dt} = \left[q(t) \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} + (1 - q(t)) \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \right] \boldsymbol{x}(t)$$

$$+ \left[q(t) \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} + (1 - q(t)) \begin{bmatrix} 0 \\ 0 \end{bmatrix} \right] v_S(t) \tag{5.9}$$

$$v_O(t) = \left[q(t) [\, 0 \quad 1 \,] + (1 - q(t)) [\, 0 \quad 1 \,] \right] \boldsymbol{x}(t) \tag{5.10}$$

■ **EXAMPLE 5.2 Coefficient Matrices of Three Basic Converters**

The coefficient matrices of the boost converter and buck/boost converter can readily be formulated from their circuit diagrams. For the ideal boost and buck/boost converters, the converter circuit is transformed into the on-time and off-time subcircuts. The state equation for each subcircuit is then written. From the state equations of the two subcircuits, the coefficient matrices are extracted. The coefficient matrices of the three basic dc-to-dc converters are summarized in Table 5.1. The coefficient matrices can be used to construct the switched state-space model of the respective converter.

Continuous Duty Ratio and Averaged State-Space Model

This section discusses the averaging process of the switched state-space model. As the first step towards obtaining an averaged version of the switched state-space model, averaging operation is performed on the switching function $q(t)$

$$d(t) = \frac{1}{T_s} \int_{t-T_s}^{t} q(\tau)\, d\tau \tag{5.11}$$

where T_s is the switching period. The $d(t)$ defined in (5.11) represents the averaged expression of $q(t)$, evaluated while sliding the averaging period T_s in time. In this sense, $d(t)$ is interpreted as the *moving average* or *local average* of $q(t)$. The $d(t)$ is also called a *continuous duty ratio*. The implications of the continuous duty ratio $d(t)$ are summarized as follows.

1) It is recognized that $d(t)_{t=kT_s} = d(kT_s) \equiv d_k$ is the actual duty ratio in the kth switching period.

Table 5.1 Coefficient Matrices of Three Basic Converters

	On-time subcircuit	Off-time subcircuit
Buck converter	$\boldsymbol{A}_{on} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix}$	$\boldsymbol{A}_{off} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix}$
	$\boldsymbol{B}_{on} = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix}^T$	$\boldsymbol{B}_{off} = [\,0 \quad 0\,]^T$
	$\boldsymbol{C}_{on} = [\,0 \quad 1\,]$	$\boldsymbol{C}_{off} = [\,0 \quad 1\,]$
Boost converter	$\boldsymbol{A}_{on} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{CR} \end{bmatrix}$	$\boldsymbol{A}_{off} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix}$
	$\boldsymbol{B}_{on} = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix}^T$	$\boldsymbol{B}_{off} = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix}^T$
	$\boldsymbol{C}_{on} = [\,0 \quad 1\,]$	$\boldsymbol{C}_{off} = [\,0 \quad 1\,]$
Buck/boost converter	$\boldsymbol{A}_{on} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{CR} \end{bmatrix}$	$\boldsymbol{A}_{off} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix}$
	$\boldsymbol{B}_{on} = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix}^T$	$\boldsymbol{B}_{off} = [\,0 \quad 0\,]^T$
	$\boldsymbol{C}_{on} = [\,0 \quad 1\,]$	$\boldsymbol{C}_{off} = [\,0 \quad 1\,]$

2) If $q(t)$ is periodic with a fixed on-time period, then it becomes that $d_k = d(t) = D$, where D is the steady-state duty ratio.

3) If $q(t)$ is non-periodic with a time-varying on-time period, then the actual duty ratio differs from the continuous duty ratio: $d_k \neq d(t)$. However, if the cycle-by-cycle variation in the on-time period is sufficiently small, the actual duty ratio can be approximated by the continuous duty ratio: $d_k \approx d(t)$.

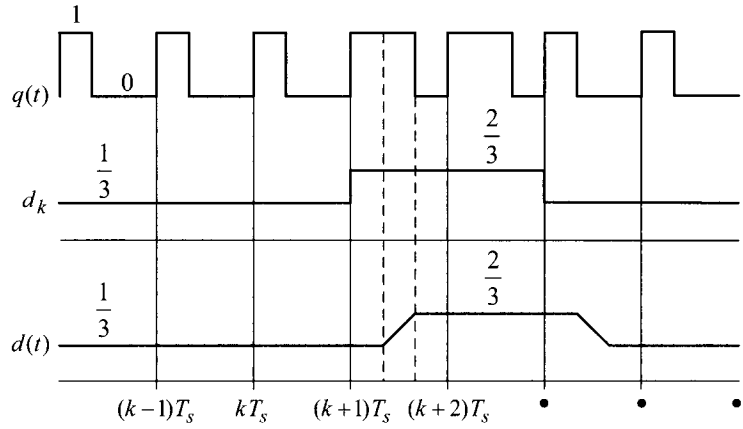


Figure 5.5 Relationships among switching function $q(t)$, cycle-by-cycle duty ratio d_k, and continuous duty ratio $d(t)$.

Figure 5.5 illustrates the relationship among the switching function $q(t)$, cycle-by-cycle duty ratio d_k, and continuous duty ratio $d(t)$. The continuous duty ratio $d(t)$ is recognized as a continuous-time approximation of the discontinuous cycle-by-cycle duty ratio d_k. The error due to this approximation becomes negligible when the cycle-by-cycle variation in d_k is sufficiently small.

As the second step, an averaging operation is performed on the switched state-space model of (5.3)

$$\begin{aligned} \frac{\mathrm{d}\bar{\boldsymbol{x}}(t)}{\mathrm{d}t} &= \overline{(q(t)\boldsymbol{A}_{on} + (1-q(t))\boldsymbol{A}_{off})\,\boldsymbol{x}(t)} \\ &\quad \overline{+ (q(t)\boldsymbol{B}_{on} + (1-q(t))\boldsymbol{B}_{off})\,v_S(t)} \\ \bar{v}_O(t) &= \overline{(q(t)\boldsymbol{C}_{on} + (1-q(t))\boldsymbol{C}_{off})\,\boldsymbol{x}(t)} \end{aligned} \tag{5.12}$$

where the *overbar* denotes the moving average of the corresponding item over the switching period T_s. For example, the *overbar* on $x(t)$ indicates

$$\bar{\boldsymbol{x}}(t) = \frac{1}{T_s}\int_{t-T_s}^{t} \boldsymbol{x}(\tau)\,\mathrm{d}\tau \tag{5.13}$$

The expression (5.12) is approximated to

$$\begin{aligned} \frac{\mathrm{d}\bar{\boldsymbol{x}}(t)}{\mathrm{d}t} &= (\bar{q}(t)\boldsymbol{A}_{on} + (1-\bar{q}(t))\boldsymbol{A}_{off})\,\bar{\boldsymbol{x}}(t) \\ &\quad + (\bar{q}(t)\boldsymbol{B}_{on} + (1-\bar{q}(t))\boldsymbol{B}_{off})\,\bar{v}_S(t) \\ \bar{v}_O(t) &= (\bar{q}(t)\boldsymbol{C}_{on} + (1-\bar{q}(t))\boldsymbol{C}_{off})\,\bar{\boldsymbol{x}}(t) \end{aligned} \tag{5.14}$$

based on the following facts and assumption.

- The averaging is a linear operation.
- The coefficient matrices in (5.12) are constant matrices.
- If the state variables and input variable do not deviate widely from their local averages, it becomes $\overline{q(t)x(t)} \approx \bar{q}(t)\bar{x}(t)$ and $\overline{q(t)v_S(t)} \approx \bar{q}(t)\bar{v}_S(t)$.

Finally, (5.14) is rewritten as

$$\begin{aligned} \frac{d\bar{x}(t)}{dt} &= (d(t)\boldsymbol{A}_{on} + (1 - d(t))\boldsymbol{A}_{off})\,\bar{x}(t) \\ &\quad + (d(t)\boldsymbol{B}_{on} + (1 - d(t))\boldsymbol{B}_{off})\,\bar{v}_S(t) \\ \bar{v}_O(t) &= (d(t)\,\boldsymbol{C}_{on} + (1 - d(t))\boldsymbol{C}_{off})\,\bar{x}(t) \end{aligned} \tag{5.15}$$

by noting that $\bar{q}(t)$ corresponds to the continuous duty ratio $d(t)$ defined in (5.11). The description (5.15) is called the averaged state-space model. The averaged state-space model takes the continuous duty ratio $d(t)$ as the input variable and describes the time-averaged power stage dynamics. Namely, the averaged state-space model is a continuous-time approximation of the switched state-space model.

The continuous duty ratio $d(t)$ is used as an instrumental variable in transforming the switched state-space model into the averaged state-space model. In fact, the averaged state-space model is obtained by simply replacing the switching function $q(t)$ with the continuous duty ratio $d(t)$, and replacing the circuit variables with their local averages. It should be emphasized that the averaged state-space model is a nonlinear model because the time-dependent variable $d(t)$ is multiplied with the coefficient matrices. The averaged state-space model is also called the *averaged state equation.*

The averaged state equation has been extensively used in the analysis of PWM dc-to-dc converters as well as other switching power converters. The steady-state equilibrium is found by solving the averaged state equation with the condition that all the state and input variables are frozen at constant: $d\boldsymbol{x}(t)/dt = 0$, $v_S(t) = V_S$, and $d(t) = D$.

More importantly, the averaged state equation has been used to simulate the converter waveforms, while focusing only on the time-averaged dynamics of the converter. Time-domain simulations on the averaged state equation provide the same information as the cycle-by-cycle simulations, yet with a greatly reduced simulation time.

Most importantly, the averaged state equation constitutes the foundation for developing small-signal models for dc-to-dc converters. By linearizing the averaged state equation at a given operating point, a linear time-invariant small-signal model is developed for dc-to-dc converters.

One disadvantage of the state-space averaging is the necessity of formulating and manipulating the state equation of the entire power stage, which can be time-consuming and tedious when the power stage contains a large number of reactive components. Another potential disadvantage is that the method only yields the final

result in the format of the state equation, which is not directly programmable with standard circuit simulation softwares.

■ EXAMPLE 5.3 Averaged State-Space Model of Ideal Buck Converter

The averaged state-space model of an ideal buck converter can be obtained from the switched state-space model, given in Example 5.1, by simply replacing $q(t)$ with $d(t)$ and also replacing the circuit variables with their average values.

$$\frac{d\bar{\mathbf{x}}(t)}{dt} = \left[d(t) \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} + (1 - d(t)) \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \right] \bar{\mathbf{x}}(t)$$

$$+ \left[d(t) \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} + (1 - d(t)) \begin{bmatrix} 0 \\ 0 \end{bmatrix} \right] \bar{v}_S(t) \qquad (5.16)$$

$$\bar{v}_O(t) = [\, d(t)[\, 0 \quad 1\,] + (1 - d(t))[\, 0 \quad 1\,]\,]\,\bar{\mathbf{x}}(t) \qquad (5.17)$$

with $\bar{\mathbf{x}} = [\bar{i}_L \; \bar{v}_C]^T$. The above expression is simplified to

$$\begin{bmatrix} \frac{d\bar{i}_L(t)}{dt} \\ \frac{d\bar{v}_C(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \begin{bmatrix} \bar{i}_L(t) \\ \bar{v}_C(t) \end{bmatrix} + \begin{bmatrix} \frac{d(t)}{L} \\ 0 \end{bmatrix} \bar{v}_S(t) \qquad (5.18)$$

$$\bar{v}_O(t) = \bar{v}_C(t) \qquad (5.19)$$

5.2.2 Circuit Averaging

The method of the circuit averaging deals with the circuit variables associated with power stage components. The circuit averaging technique might be best described by illustrating the steps of the modeling process.

1) Formulate an equation that describes the time-averaged behavior of the circuit variables associated with an individual component in the power stage. This equation is referred to as the averaged circuit equation.

2) Synthesize a circuit model that satisfies the averaged circuit equation formulated in the previous step. This model is called the average model of a specific circuit component.

3) Put the resulting average model into the power stage in place of the original circuit component.

4) Repeat the above process for all the components in the power stage. When all the circuit components are replaced with their average models, the resulting circuit configuration becomes an *average circuit model* of the entire power stage. The average power stage model generates the circuit waveforms that track the moving averages of the original waveforms.

In the circuit averaging, it is not always necessary to individually apply the averaging process to every single circuit component. In fact, several circuit components can be grouped together and treated as one composite circuit component. This practice will be explored in the next section.

PWM Switch

In principle, all the circuit components in the power stage should be replaced with their average models to yield an average model for the entire power stage. However, the linear circuit components, including the voltage source, inductor, and capacitor, remain invariant during the averaging process. In other words, linear circuit components can be used in their original forms at their initial locations when constructing an average model for the power stage. Accordingly, the circuit components that need to go through the formal averaging process are only the active and passive switches.

Figure 5.6 shows the circuit diagrams of the three basic PWM converters, where the active-passive switch pair is identified as the circuit component that is subjected to the averaging operation. The active-passive switch pair functions as a single-pole double-throw (SPDT) switch that periodically changes its structure based on the PWM principle. This active-passive switch pair is named as the *PWM switch*, in order to highlight its function as a three-terminal switching device operating under the principle of PWM.

Figure 5.7 shows the functional description, circuit symbol, and polarity/direction of the terminal circuit variables of the PWM switch. The node **a** stands for the active terminal directed to the active switch, **p** represents the passive terminal, and **c** denotes the common terminal. The circuit symbol also signifies that the common terminal is connected to the active terminal **a** for dT_s and to the passive terminal **p** for $d'T_s = (1-d)T_s$.

The PWM switch has the characteristic features on its terminal waveforms, regardless of the converter topology in which the PWM switch is embedded. First, referring to Fig. 5.6, a dc voltage is applied across the active and passive terminals. For the three basic dc-to-dc converters, the voltage between **a** and **p** terminals is

$$v_{ap}(t) = \begin{cases} v_S & \text{for buck converter} \\ -v_O & \text{for boost converter} \\ v_S + v_O & \text{for buck/boost converter} \end{cases} \tag{5.20}$$

which can be considered as a dc under the small-ripple approximation. The voltage across **c** and **p** terminals, v_{cp}, is a sampled replica of v_{ap}; v_{cp} equals to v_{ap} during dT_s and becomes zero during $d'T_s$.

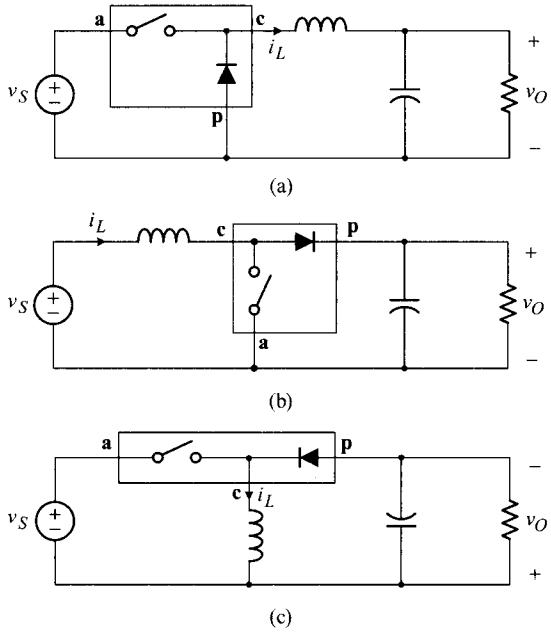


Figure 5.6 Circuit diagrams of three basic converters. (a) Buck converter. (b) Boost converter. (c) Buck/boost converter.

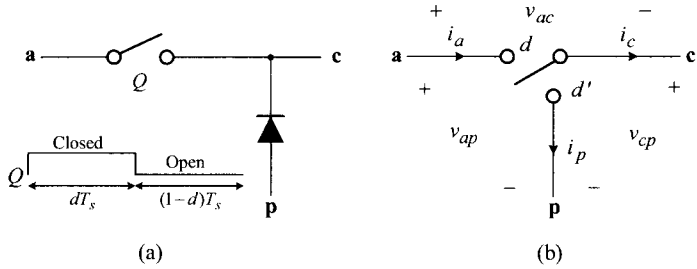


Figure 5.7 PWM switch. (a) Active-passive switch pair operating under PWM principle. (b) Circuit symbol for PWM switch.

Second, the common terminal carries the inductor current, which is a continuous triangular waveform,

$$i_c(t) = \begin{cases} i_L(t) & \text{for buck and buck/boost converters} \\ -i_L(t) & \text{for boost converter} \end{cases} \tag{5.21}$$

The active terminal current i_a is a sampled version of i_c, thus a pulsating discontinuous waveform. These facts will be used later in formulating the circuit equations for the PWM switch.

Averaging PWM Switch

The PWM switch, identified as the three-terminal switching device embedded in all the three basic PWM converters, can be treated as an individual circuit component and its average model is derived based on the terminal circuit behavior. The circuit equations for the PWM switch are written as

$$\begin{aligned} v_{cp}(t) &= v_{ap}(t)q(t) \\ i_a(t) &= i_c(t)q(t) \end{aligned} \tag{5.22}$$

using the switching function $q(t)$

$$q(t) = \begin{cases} 1 & \text{for} \quad dT_s \\ 0 & \text{for} \quad d'T_s \end{cases} \tag{5.23}$$

Equation (5.22) indicates that the continuous circuit variables v_{ap} and i_c are multiplied by the switching function $q(t)$, yielding the discontinuous circuit variables v_{cp} and i_a. This equation is actually a compact expression for the circuit variables of the PWM switch, formulated using the switching function $q(t)$.

By taking the local average of (5.22), it follows that

$$\begin{aligned} \bar{v}_{cp}(t) &= \overline{v_{ap}(t)q(t)} \\ \bar{i}_a(t) &= \overline{i_c(t)q(t)} \end{aligned} \tag{5.24}$$

These expressions are approximated to

$$\begin{aligned} \bar{v}_{cp}(t) &\approx \bar{v}_{ap}(t)\bar{q}(t) \\ \bar{i}_a(t) &\approx \bar{i}_c(t)\bar{q}(t) \end{aligned} \tag{5.25}$$

based on the assumption that the circuit variables do not significantly deviate from their local averages.

Because the local average of the switching function $q(t)$ is actually the continuous duty ratio $d(t)$ defined in (5.11), the expressions (5.25) are rewritten as

$$\begin{aligned} \bar{v}_{cp}(t) &= d(t)\bar{v}_{ap}(t) \\ \bar{i}_a(t) &= d(t)\bar{i}_c(t) \end{aligned} \tag{5.26}$$

yielding the desired expressions for averaged circuit variables.

The average equations for the PWM switch, given by (5.26), describe the relationships among the averaged circuit variables $\bar{v}_{cp}$, $\bar{v}_{ap}$, $\bar{i}_a$, and $\bar{i}_c$. The averaged relationships of other circuit variables can be evaluated based on Kirchhoff's voltage and current laws

$$\begin{aligned} \bar{v}_{ac}(t) &= \bar{v}_{ap}(t) - \bar{v}_{cp}(t) \\ \bar{i}_p(t) &= \bar{i}_a(t) - \bar{i}_c(t) \end{aligned} \tag{5.27}$$

The PWM switch is a lossless switching device, so it obeys the power balance condition in terms of the averaged circuit variables

$$\bar{v}_{ap}(t)\,\bar{i}_a(t) = \bar{v}_{cp}(t)\,\bar{i}_c(t) \tag{5.28}$$

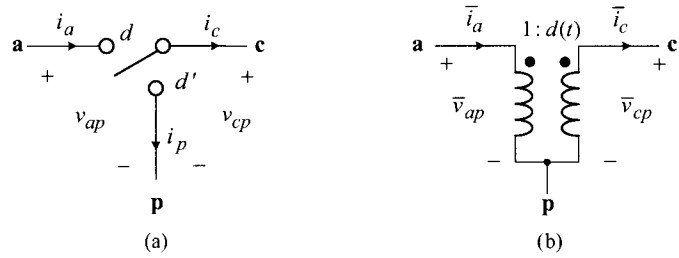


Figure 5.8 PWM switch and its average model. (a) PWM switch. (b) Average model.

The averaged equations of the PWM switch in (5.26) are identical to the circuit equations of an ideal two-winding transformer with a turns ratio $d(t)$. Accordingly, the ideal two-winding transformer can be used as an average model for the PWM switch. Figure 5.8 shows the PWM switch and its average model representation using an ideal transformer. The ideal transformer in Fig. 5.8(b) has the following properties. First, the turns ratio is a time-dependent variable $d(t)$ rather than a constant. Second, the primary and secondary windings are tied together at the passive terminal. Therefore, the average model for the PWM switch is a time-variant three-terminal device which has the structure of a two-winding ideal transformer.

■ EXAMPLE 5.4 Average Equations of PWM Switch in Buck Converter

This example illustrates the average equations for the PWM switch. Figure 5.9 shows the circuit waveforms of the PWM switch embedded in a buck converter. From the circuit waveforms, the average values of v_{ap} and i_c are written as

$$\begin{aligned} \bar{v}_{ap}(t) &= V_S \\ \bar{i}_c(t) &= I_L \end{aligned} \tag{5.29}$$

On the other hand, the average values of v_{cp} and i_a are expressed as

$$\begin{aligned} \bar{v}_{cp}(t) &= d(t)V_S \\ \bar{i}_a(t) &= d(t)I_L \end{aligned} \tag{5.30}$$

using the definition of the continuous duty ratio. It becomes apparent from the above expressions that

$$\begin{aligned} \bar{v}_{cp}(t) &= d(t)\bar{v}_{ap}(t) \\ \bar{i}_a(t) &= d(t)\bar{i}_c(t) \end{aligned} \tag{5.31}$$

which are the average equations for the PWM switch given in (5.26).

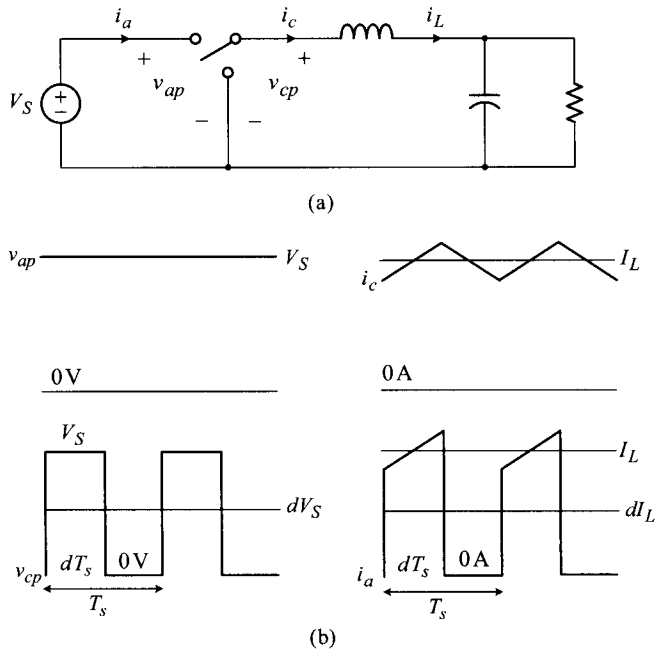


Figure 5.9 PWM switch in buck converter. (a) Circuit diagram. (b) Circuit waveforms.

Average Models for Three Basic PWM Converters

The average model for the PWM switch is derived considering the PWM switch as a standalone individual device. Accordingly, the average model can universally be used for all the three basic PWM converters, which commonly contain the PWM switch. The average models are simply obtained with a pin-to-pin replacement of the active-passive switch pair with the average model of the PWM switch. Figure 5.10 shows the average models for the buck, boost, and buck/boost converters. Each average model describes the time-averaged circuit behavior of the respective PWM converter.

■ EXAMPLE 5.5 Responses of Switch Model and Average Model

This example illustrates the implication of the average model of dc-to-dc converters. Figure 5.11 compares the responses of the switch model and average model of a buck converter. Figure 5.11(a) is the simulation result using the switch model. For this simulation, the switch drive signal is appropriately modulated to produce the switching function $q(t)$ whose cycle-by-cycle duty ratio is varied in a sinusoidal fashion. With this switching function, the induc-

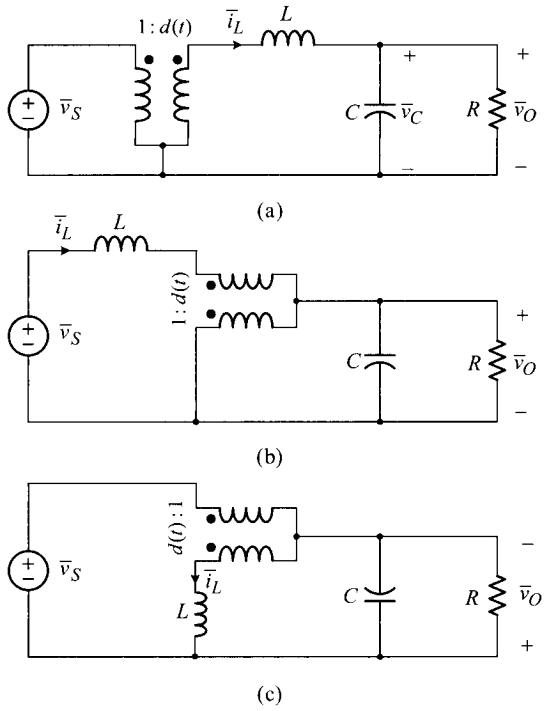


Figure 5.10 Average models for three basic converters. (a) Buck converter. (b) Boost converter. (c) Buck/boost converter.

tor current $i_L(t)$ shows a low-frequency sinusoidal oscillation, as well as the high-frequency switching ripple.

Simulations with the average model are shown in Fig. 5.11(b). For this case, the switching function $q(t)$ is first converted into the continuous duty ratio $d(t)$ by performing the averaging operation

$$d(t) = \frac{1}{T_s}\int_{t-T_s}^{t} q(\tau)\,d\tau \tag{5.32}$$

The resulting continuous duty ratio $d(t)$, shown in Fig. 5.11(b), is then used as a time-varying turns ratio of the ideal transformer. The average model produces the continuous inductor current $\bar{i}_L(t)$ that traces the moving average of the actual inductor current $i_L(t)$ of the switch model

$$\bar{i}_L(t) = \frac{1}{T_s}\int_{t-T_s}^{t} i_L(\tau)\,d\tau \tag{5.33}$$

As shown in the previous example, the average model generates continuous circuit waveforms that track the moving average of the actual responses of the dc-to-dc

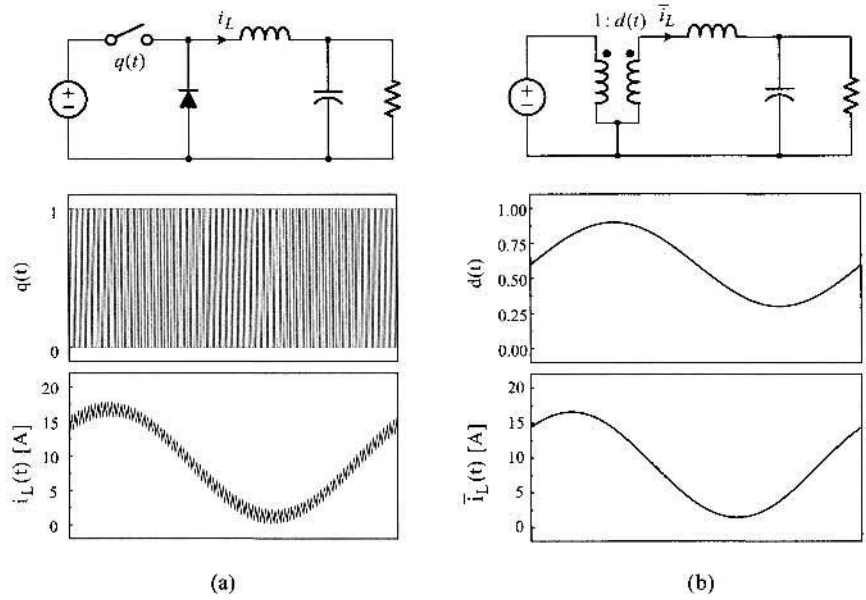


Figure 5.11 Responses of buck converter. (a) Switch model response. (b) Average model response.

converter. Accordingly, the average models are often used to simulate the time-averaged circuit waveforms during transition periods.

The average model is also used to study the steady-state circuit operation. In the steady-state equilibrium, all the circuit variables denote dc quantities and the continuous duty ratio becomes the steady-state duty ratio D. In addition, the inductor behaves as a short circuit, while the capacitor functions as an open circuit. Under these conditions, the average model of the buck converter in Fig. 5.10(a) indicates that $V_O = DV_S$; namely, the dc voltage gain of the converter equals to D. The use of the average model for the steady-state analysis is further illustrated in the following example.

■ EXAMPLE 5.6 Voltage Gain of Non-Ideal Boost Converter

The average model for the boost converter is shown in Fig. 5.12(a). In the average model, the resistance R_l represents the esr of the inductor. As will be discussed later, the esr of the inductor does not affect the averaging process. Thus, the esr is placed in the original location in the average model. The average model is transformed into a dc model, shown in Fig. 5.12(b), by shorting the inductor, opening the capacitor, and replacing the continuous duty ratio $d(t)$ with the steady-state duty ratio D. Figure 5.12(b) is further modified to Fig.

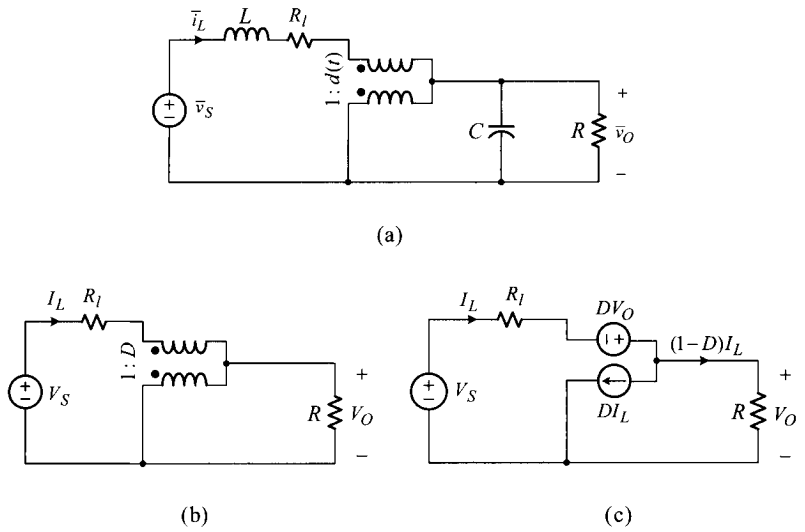


Figure 5.12 Average and dc models of boost converter. (a) Average model. (b) Dc model. (c) Modified model.

5.12(c) by replacing the ideal transformer with a pair of voltage source and current source.

The dc model can be used for the steady-state analysis at the presence of the esr of the inductor. For example, the voltage gain of the converter is evaluated as follows. Referring to the circuit variables in Fig. 5.12(c), the average inductor current is given by

$$I_L = \frac{V_S + DV_O - V_O}{R_l} = \frac{V_S + (D-1)V_O}{R_l} \tag{5.34}$$

On the other hand, the output voltage is given by

$$V_O = (1-D)I_L R \tag{5.35}$$

From (5.34) and (5.35), it becomes

$$V_O = (1-D)\left(\frac{V_S + (D-1)V_O}{R_l}\right)R \tag{5.36}$$

which can be rearranged as

$$\frac{V_O}{V_S} = \frac{1}{1-D}\frac{1}{1 + \dfrac{1}{(1-D)^2}\dfrac{R_l}{R}} \tag{5.37}$$

yielding the voltage gain expression. This expression is the same as the gain formula derived in Section 4.1.4 using the flux and charge balance conditions.

5.2.3 Generalization of Circuit Averaging Technique

In the previous section, the circuit averaging technique is adapted to develop the average models for the three basic PWM converters. Relatively simple modeling procedures are applied to the buck, boost, and buck/boost converters operating in continuous conduction mode (CCM). These modeling procedures can be extended to cover the following general cases:

- the cases where the reactive circuit components include parasitic resistances,
- the cases where dc-to-dc converters operate in discontinuous condition mode (DCM), and
- the cases where other isolated PWM converters are employed.

The extension of the modeling technique to the general cases requires lengthy discussions, as such, the topic is postponed to a later chapter. This section briefly introduces some of the results of the forthcoming model generalization, in order to facilitate the use of the basic average models developed in this chapter.

Effects of Parasitic Resistances

One practical issue in the model generalization is the effects of the parasitic circuit components on the average model. As mentioned earlier, linear circuit components remain invariant during the averaging process. Accordingly, parasitic resistances of reactive components can be included in the average models. In Example 5.6, the equivalent series resistance (esr) of the inductor was added to the average model of the boost converter and the resulting model was used to find the voltage gain of the converter.

Unlike the esr of the inductor, which can be added to the average model without affecting the average model of other circuit components, the esr of the capacitor could alter the circuit waveforms of the PWM switch. Accordingly, the average model of the PWM switch needs to be modified at the existence of the esr of the capacitor, even though the esr itself can be added at its original place. The effects of the esr of the capacitor will be covered in Chapter 9, yet it is now emphasized that the consequence of this modification is negligible for most situations. Correspondingly, it can broadly be considered that the esrs of the reactive components do not cause any practical changes to the average model. Therefore, all the parasitic resistances can be included in the average model at their original places without causing any notable error. Figure 5.13 shows a buck converter and its average model, where the esrs of the inductor and capacitor are both included.

Average Models in DCM Operation

Throughout this chapter, it was assumed that dc-to-dc converters operate in CCM and their average models were derived based on the CCM waveforms. As a dc-to-dc converter departs from CCM operation and enters DCM operation, the circuit wave-

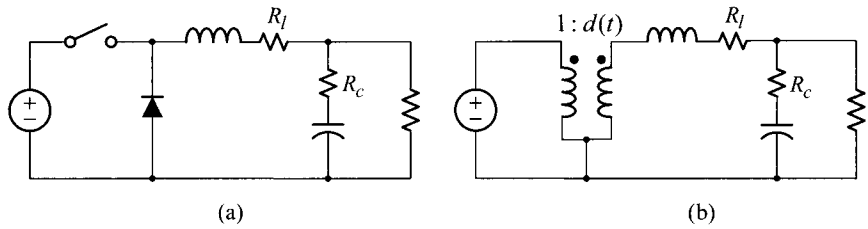


Figure 5.13 Buck converter with parasitic resistances. (a) Buck converter. (b) Average model.

forms of the PWM switch are altered and its average model should be reformulated. Average models for PWM converters operating in DCM can be derived in a similar manner to the CCM case. Converter modeling in DCM operation will be treated in Chapter 9, along with other advanced topics of the PWM converter modeling.

Average Models for Isolated PWM Converters

In addition to the three basic converters, Chapter 4 introduced several isolated PWM dc-to-dc converters. The average modeling, established for non-isolated basic converters, needs to be extended to the isolated dc-to-dc converters.

As discussed in Chapter 4, each isolated converter has a forerunning non-isolated converter; for instance, the isolated full-bridge converter is evolved from the non-isolated buck converter. The average model of a non-isolated converter can be modified to yield the average model of the affiliated isolated converter. The average model of the buck converter can readily be altered to the average model of the full-bridge converter. Similarly, the average model for the buck/boost converter can be modified to yield the average model of the flyback converter. The development of average models for isolated PWM dc-to-dc converters will be covered in Chapter 9.

5.2.4 Circuit Averaging and State-Space Averaging

Circuit averaging has several advantages over the state-space averaging. First, the circuit averaging performs the averaging operation directly on the power stage circuit. Thus, this technique does not require the manipulation of the state equation, which is the case for state-space averaging, thereby greatly reducing the computational burden. Second, the circuit averaging provides the average model in the structure that closely resembles the original power stage circuit diagram, which is not the case for state-space averaging. Thus, the resulting average model can readily be programmed with standard circuit simulation software.

In spite of the differences in the modeling approaches, the circuit averaging is functionally identical to the state-space averaging. A simple confirmation of the equivalence between these two techniques is given as follows.

The average model of the buck converter shown in Fig. 5.10(a) yields the circuit equation

$$\begin{aligned} L\frac{d\bar{i}_L(t)}{dt} &= d(t)\bar{v}_S(t) - \bar{v}_C(t) \\ C\frac{d\bar{v}_C(t)}{dt} &= \bar{i}_L(t) - \frac{\bar{v}_C(t)}{R} \end{aligned} \tag{5.38}$$

This equation is rearranged into a matrix form

$$\begin{bmatrix} \frac{d\bar{i}_L(t)}{dt} \\ \frac{d\bar{v}_C(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \begin{bmatrix} \bar{i}_L(t) \\ \bar{v}_C(t) \end{bmatrix} + \begin{bmatrix} \frac{d(t)}{L} \\ 0 \end{bmatrix} \bar{v}_S(t) \tag{5.39}$$

which is identical to the result of the state-space averaging given in Example 5.3.

The average models, derived from either state-space averaging or circuit averaging, can be transformed into small-signal models through the linearization process. In this book, however, the average models derived from the circuit averaging are only considered for the linearization, primarily due to the simplicity in the linearization process. The derivation of average models using the state-pace averaging technique and linearization of the resulting average models can be found in [2].

5.3 LINEARIZING AVERAGED POWER STAGE DYNAMICS

While the averaging eliminates the time variance from the power stage dynamics, it brings in certain nonlinearities to the average model of the power stage. In this section, we employ the linearization process to remove nonlinearities brought in during the averaging process. The linearized average model constitutes the small-signal model of the power stage.

5.3.1 Linearization of Nonlinear Function and Small-Signal Model

Linearization is the process of approximating a nonlinear function to a linear relationship under certain assumptions. One can expand a nonlinear function into Taylor series and retain only the constant and the first-order term of the series, leading to a linear approximation of the nonlinear equation around the point of expansion. More specifically, a nonlinear function $y = f(x)$, when $x = X + \hat{x}$ with $\hat{x} = |x - X| \ll 1$, can be approximated by

$$y = f(X + \hat{x}) \approx f(X) + \left.\frac{df}{dx}\right|_{x=X} \hat{x} \tag{5.40}$$

in the vicinity of the quiescent point $(X, f(X))$. The variable $\hat{x}$ represents a *small* variation in x around a fixed value X. In this book, $\hat{x}$ denotes a sinusoidal variation

$$\hat{x}(t) = x_s \sin \omega_s t \tag{5.41}$$

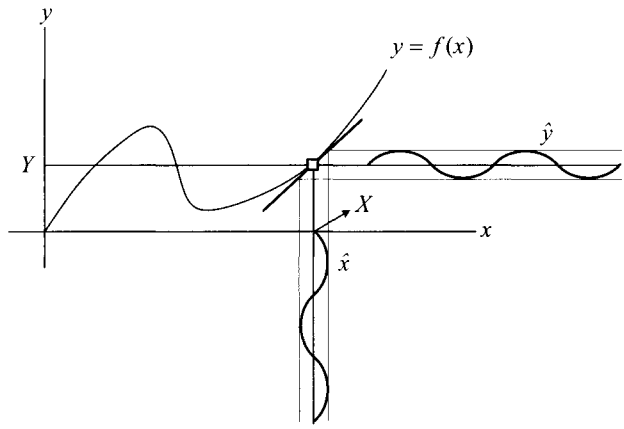


Figure 5.14 Linearization of nonlinear function.

Thus, $\hat{x}$ is called the sinusoidal component or ac component, while X is referred to as the dc component. Figure 5.14 graphically illustrates the linearization process. It can be envisaged that the linearization described by (5.40) is equivalent to replacing the nonlinear curve with its tangential line segment evaluated at $x = X$. In other words, the nonlinear relationship is locally linearized using the tangential line at the quiescent point. The assumption $\hat{x} = |x - X| \ll 1$ is necessary to ensure that the length of the tangential line segment is so short that the deviation between the nonlinear curve and the line segment is negligibly small.

With the input variable consisting of the dc and ac components, $x = X + \hat{x}$, the output variable y can also be decomposed into a dc component Y and an ac component $\hat{y}$: $y = Y + \hat{y}$. From (5.40), the dc component of y is given by $Y = f(X)$, and the ac component then becomes

$$\hat{y} = \left.\frac{df}{dx}\right|_{x=X} \hat{x} \tag{5.42}$$

The *small-signal gain* or *small-signal model* of the nonlinear equation is defined as the ratio of the ac variables

$$\frac{\hat{y}}{\hat{x}} = \left.\frac{df}{dx}\right|_{x=X} \tag{5.43}$$

The small-signal gain relates the ac components of input and output variables in the vicinity of a given dc operating point. The condition $\hat{x} = |x - X| \ll 1$ is called the small-signal assumption because it indicates that the ac component of the input variable is substantially smaller than the dc component. In this context, $\hat{x}(t) = x_s \sin \omega t$ is referred to as the small signal, while X is called the large signal. The small-signal assumption is the necessary condition for the accuracy of the small-signal model.

The process of finding a small-signal model is called the *small-signal modeling* of a nonlinear process. As illustrated in Fig. 5.14, the small-signal modeling can be

considered as the process of evaluating the slope or derivative of a nonlinear function at a given quiescent point.

The small-signal modeling can also be performed in an alternative manner. For simple algebraic nonlinear equations, the small-signal model can be found by

1) evaluating the nonlinear equation with the variables consisting of dc and ac components, and

2) equating only the ac components of input and output variables from the resulting expression.

As a simple example, the small-signal gain of a nonlinear equation $y = x^2$ at $x = X = 2$ can be found as follows. By evaluating the equation with the input and output variables consisting of both dc and ac components, it follows that

$$Y + \hat{y} = (X + \hat{x})^2 = X^2 + 2X\hat{x} + \hat{x}^2 \tag{5.44}$$

The first term in the right-hand side of (5.44), X^2, is a dc quantity and thus is irrelevant to the small-signal modeling. The third term $\hat{x}^2$ is a second-order function of the small ac variable, and thus is small enough to be ignored. Accordingly, the small-signal relationship of the given equation becomes

$$\hat{y} = 2X\hat{x} \tag{5.45}$$

The evaluation of (5.45) at $X = 2$ leads to the desired small-signal gain

$$\frac{\hat{y}}{\hat{x}} = 2X|_{X=2} = 4 \tag{5.46}$$

On the other hand, a direct application of (5.43) to $y = x^2$ in the neighborhood of $x = X = 2$ yields the small-signal gain

$$\frac{\hat{y}}{\hat{x}} = \left.\frac{dx^2}{dx}\right|_{x=X=2} = 2x|_{x=X=2} = 4 \tag{5.47}$$

which is identical to (5.46).

5.3.2 Small-Signal Model for PWM Switch — PWM Switch Model

The linearization can be adapted to either the averaged state equation of the power stage, obtained from the state-space averaging, or the average model of the PWM switch, derived from the circuit averaging. Because the latter is more convenient for linearization, the small-signal modeling is now employed to the average model of the PWM switch, shown in Fig. 5.15(a). The circuit equations for the average model of the PWM switch are repeated below

$$\begin{aligned} \bar{v}_{cp}(t) &= d(t)\bar{v}_{ap}(t) \\ \bar{i}_a(t) &= d(t)\bar{i}_c(t) \end{aligned} \tag{5.48}$$

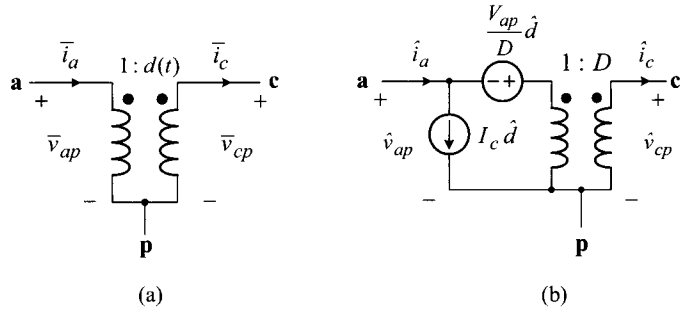


Figure 5.15 Dynamic models for PWM switch. (a) Average model of PWM switch. (b) Small-signal model of PWM switch.

Although the symbol *overbar* will be omitted in following developments, all the circuit variables represent the averaged variables.

Using the alternative linearization process discussed earlier, the small-signal modeling of (5.48) is preformed as follows. Application of the linearization process to (5.48) yields

$$\begin{aligned} \underbrace{V_{cp}}_{\text{dc}} + \underbrace{\hat{v}_{cp}(t)}_{\text{ac}} &= (D + \hat{d}(t))(V_{ap} + \hat{v}_{ap}(t)) \\ &= \underbrace{D\,V_{ap}}_{\text{dc}} + \underbrace{\hat{d}(t)V_{ap} + D\,\hat{v}_{ap}(t)}_{\text{ac}} \\ &\quad + \underbrace{\hat{d}(t)\,\hat{v}_{ap}(t)}_{\text{second-order}} \end{aligned} \tag{5.49}$$

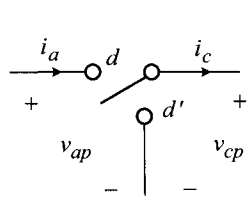
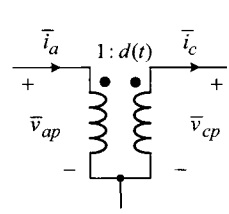
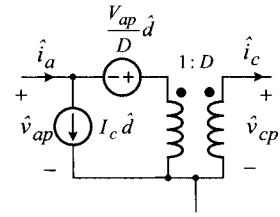
$$\begin{aligned} \underbrace{I_a}_{\text{dc}} + \underbrace{\hat{i}_a(t)}_{\text{ac}} &= (D + \hat{d}(t))(I_c + \hat{i}_c(t)) \\ &= \underbrace{D\,I_c}_{\text{dc}} + \underbrace{\hat{d}(t)\,I_c + D\,\hat{i}_c(t)}_{\text{ac}} \\ &\quad + \underbrace{\hat{d}(t)\,\hat{i}_c(t)}_{\text{second-order}} \end{aligned} \tag{5.50}$$

where the capitalized variables are dc components and the variables with the superscript ^ are ac components. For example, D is the steady-state duty ratio, whereas the quantity $\hat{d}(t)$ denotes the small-signal ac component of the continuous duty ratio $d(t)$. Discussions about the ac components of $d(t)$ and other ac variables are given in the next section.

By equating the ac components in (5.49) and (5.50), the small-signal representation of (5.48) is obtained

$$\begin{aligned} \hat{v}_{cp}(t) &= V_{ap}\,\hat{d}(t) + D\,\hat{v}_{ap}(t) \\ \hat{i}_a(t) &= I_c\,\hat{d}(t) + D\,\hat{i}_c(t) \end{aligned} \tag{5.51}$$

Table 5.2 Models for PWM Switch

Switch model	Average model	Small-signal model
		
$v_{cp}(t) = q(t)\, v_{ap}(t)$	$\overline{v}_{cp}(t) = d(t)\, \overline{v}_{ap}(t)$	$\hat{v}_{cp}(t) = V_{ap}\hat{d}(t) + D\hat{v}_{ap}(t)$
$i_a(t) = q(t)\, i_c(t)$	$\overline{i}_a(t) = d(t)\, \overline{i}_c(t)$	$\hat{i}_a(t) = I_c\hat{d}(t) + D\hat{i}_c(t)$
$q(t) = \begin{cases} 1 & \text{for } dT_s \\ 0 & \text{for } (1-d)T_s \end{cases}$	$d(t) = \frac{1}{T_s}\int_{t-T_s}^{t} q(\tau)\mathrm{d}\tau$	

Equation (5.51) constitutes the small-signal model or small-signal representation of the PWM switch. In (5.51), in the left-hand side circuit variables are expressed as a linear combination of the dc and ac components of other variables. In particular, V_{ap}, D, and I_c are the dc values of the corresponding circuit variables. Thus, the small-signal representation of (5.51) depends on the dc operating point of the PWM switch, as is always the case with the small-signal model of any nonlinear system.

The small-signal relationship (5.51) can be converted into an equivalent circuit model. The circuit representation is shown in Fig. 5.15(b). It is straightforward to show that this model satisfies the circuit equations of (5.51). The circuit model was named the *PWM switch model* by Dr. Vatché Vorpérion who first proposed this model. The PWM switch model thus refers to the small-signal model of the PWM switch. As shown in Fig. 5.15(b), the PWM switch model contains two dependent signal sources, both controlled by the small-signal continuous duty ratio $\hat{d}$. It also includes an ideal transformer whose turns ratio is given by the steady-state duty ratio D of the converter.

Table 5.2 compares the three different models for the PWM switch: the switch model, average model, and small-signal model. The switch model is a time-variant model in which the switching function $q(t)$ represents the time dependency of the PWM switch. The switch model is converted into the time-invariant but nonlinear average model by adopting the continuous duty ratio $d(t)$, which is defined as the moving average of the switching function $q(t)$. Finally, the nonlinear average model is linearized under small-signal assumption, leading to the linear time-invariant small-signal model of the PWM switch — the PWM switch model. The circuit equations for the switch model, average model, and PWM switch model are also shown in Table 5.2.

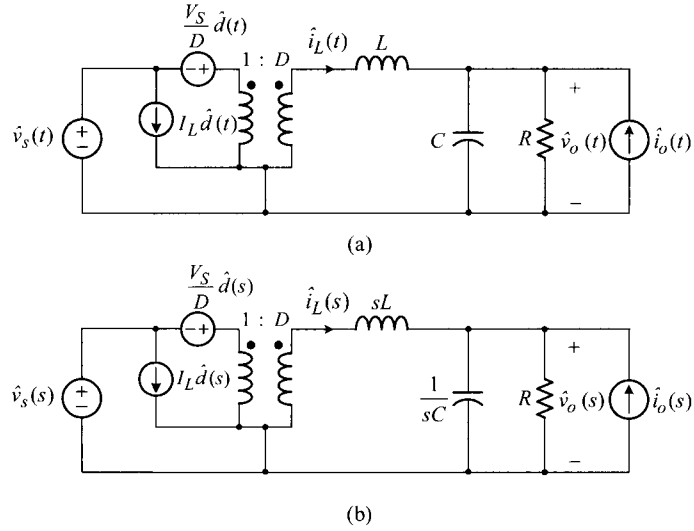


Figure 5.16 Small-signal models of buck converter. (a) Time-domain small-signal model. (b) s-domain small-signal model.

5.3.3 Small-Signal Model of Converter Power Stage

The same as with the averaging process case, the linear circuit components are invariant to the linearization process and can be used in their original shapes at their initial positions in constructing a small-signal model from the average model. Accordingly, the small-signal model for the converter power stage is obtained from the respective average model of the power stage, by simply replacing the PWM switch with its small-signal model and introducing appropriate small-signal sources as the input variables to the model.

Figure 5.16(a) shows the small-signal model of the buck converter. In this model, $\hat{v}_s(t)$ is the small-signal input voltage, $\hat{d}(t)$ denotes the small-signal continuous duty ratio, and $\hat{i}_o(t)$ is the small-signal current source that represents the sinusoidal current deviation from the dc output current. The small-signal model shows that $V_{ap} = V_S$ and $I_c = I_L$ for the buck converter.

The small-signal power stage model in Fig. 5.16(a) is a time-domain model in which all the excitation sources and circuit variables are defined as time-dependent quantities. This time-domain small-signal model exhibits the transient response of the power stage at the presence of small-signal time-domain excitations. The small-signal model becomes far more useful when converted into the frequency-domain, or s-domain, model. The time-domain small-signal model is now transformed into the s-domain small-signal model, as shown in Fig. 5.16(b), by using s-domain expressions for the circuit variables and circuit components.

Figure 5.17 shows the s-domain small signal models for the three basic converters. The models are constructed from the average models by following the procedures

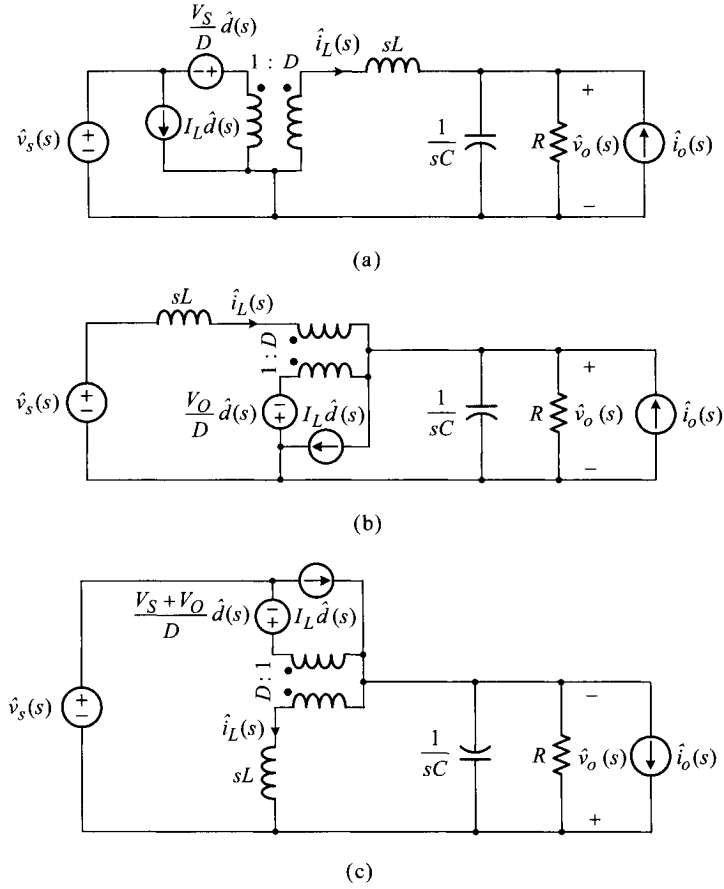


Figure 5.17 Small-signal models of three basic converters. (a) Buck converter. (b) Boost converter. (c) Buck/boost converter.

explained above. The small-signal model of the boost converter incorporates that $V_{ap} = -V_O$ and $I_c = -I_L$, thus altering the polarity/direction of the dependent voltage/current source in the PWM switch model. The buck/boost converter model reflects that $V_{ap} = V_S + V_O$ and $I_c = I_L$. The s-domain small-signal models are a linear time-invariant model to which all classical circuit analysis techniques can directly be applied. In Chapter 6, the power stage dynamics of the three basic dc-to-dc converters will be investigated using these models.

5.4 FREQUENCY RESPONSE OF CONVERTER POWER STAGE

The s-domain small-signal models can be used to study the frequency response of the PWM converter. While the frequency response of linear time-invariant systems is

well known, the frequency response of the PWM converter may require explanations about its origin.

The concept of the frequency response is evolved from the sinusoidal response. Thus, this section first discusses the sinusoidal response and later presents the frequency response of the converter power stage.

5.4.1 Sinusoidal Response of Power Stage

The sinusoidal response is initially established for linear time-invariant systems. When a sinusoidal input is applied to a linear time-invariant system, the output of the system is a sinusoid with the same frequency as that of the input sinusoid. However, the magnitude and phase of the output sinusoid are usually altered. The changes in the magnitude and phase are referred to as the sinusoidal response of a linear time-invariant system. The concept of the sinusoidal response is now extended to PWM dc-to-dc converters.

First, it is presumed that the switch drive signal $q(t)$ is periodic with a fixed duty ratio, resulting in a constant continuous duty ratio, $d(t) = D$. However, it is also assumed that the input voltage of the converter contains an ac component, $\hat{v}_s$, on top of the dc component V_S

$$v_S(t) = V_S + \hat{v}_s(t) \tag{5.52}$$

The ac component is further assumed to be a sinusoid at frequency ω_s

$$\hat{v}_s(t) = v_s \sin \omega_s t \tag{5.53}$$

When the condition $v_s \ll V_S$ is imposed, the output voltage v_O will exhibit a sinusoidal excursion around a dc value, with the switching ripple superimposed on it. This situation is illustrated in Fig. 5.18, where the switch drive signal $q(t)$ is periodic while the input voltage $v_S(t)$ contains a sinusoidal component. When the switching ripple is ignored, the output voltage is expressed as a combination of dc and ac components

$$v_O(t) = V_O + \hat{v}_o(t) \tag{5.54}$$

The ac component will be a sinusoid at frequency ω_s

$$\hat{v}_o(t) = v_o \sin(\omega_s t + \theta_s) \tag{5.55}$$

From (5.53) and (5.55), the input-to-output sinusoidal response at ω_s is defined as

- magnitude response at $\omega_s = \dfrac{|\hat{v}_o(t)|}{|\hat{v}_s(t)|} = \dfrac{v_o}{v_s}$
- phase response at $\omega_s = \angle\hat{v}_o(t) - \angle\hat{v}_s(t) = \theta_s$ (5.56)

Another example of the sinusoidal response is shown in Fig. 5.19. For this case, the input voltage is fixed at $v_S = V_S$ but the switch drive signal is modulated cycle-by-cycle, as illustrated by the switching function $q(t)$ in Fig. 5.19. The modulation

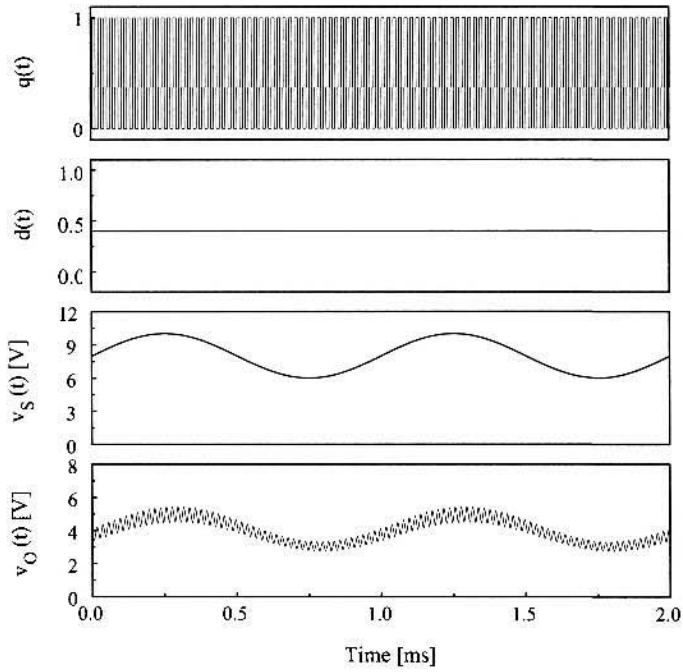


Figure 5.18 Output voltage response due to sinusoidal change in input voltage.

in the switch drive signal has occurred in a sinusoidal fashion so that the continuous duty ratio $d(t)$ is expressed as

$$d(t) = D + \hat{d}(t) \tag{5.57}$$

with

$$\hat{d}(t) = d \sin \omega_d t \tag{5.58}$$

When the switching ripple is ignored, the output voltage can also be represented by the sum of dc and ac components

$$v_o(t) = V_O + \hat{v}_o(t) \tag{5.59}$$

with

$$\hat{v}_o(t) = v_o \sin(\omega_d t + \theta_d) \tag{5.60}$$

The sinusoidal response between the continuous duty ratio and output voltage is defined as

- magnitude response at $\omega_d = \dfrac{|\hat{v}_o(t)|}{|\hat{d}(t)|} = \dfrac{v_o}{d}$
- phase response at $\omega_d = \angle \hat{v}_o(t) - \angle \hat{d}(t) = \theta_d$ (5.61)

The sinusoidal response from the load current to the output voltage is defined in the same manner.

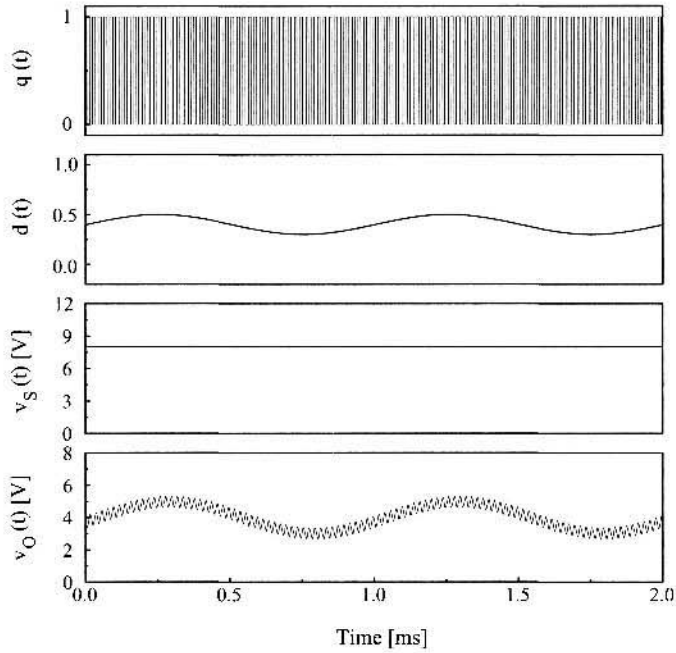


Figure 5.19 Output voltage response due to sinusoidal change in continuous duty ratio.

5.4.2 Frequency Response and s-Domain Small-Signal Model of Power Stage

The sinusoidal response of the power stage is now extended to the frequency response. When the sinusoidal response is continuously evaluated in frequency, two continuous curves are obtained, which are referred to as the gain response curve and phase response curve. The gain and phase response curves are collectively called the frequency response plot. The frequency response plot is usually displayed in the Bode plot format. Details about the Bode plot representation are given in Chapter 6.

The most significant value of the s-domain small-signal model is the generation of the power stage transfer functions, which can readily be converted into frequency response plots. The transfer functions are derived from the s-domain small-signal model using conventional circuit analysis techniques. The resulting transfer functions are then converted into Bode plots to portray the frequency response of the power stage.

The frequency response carries the whole information about the power stage dynamics, as is the case with linear time-invariant systems. The frequency response reveals the static and dynamic behaviors of the power stage, and constitutes the foundation for the feedback controller design. Construction of the frequency response

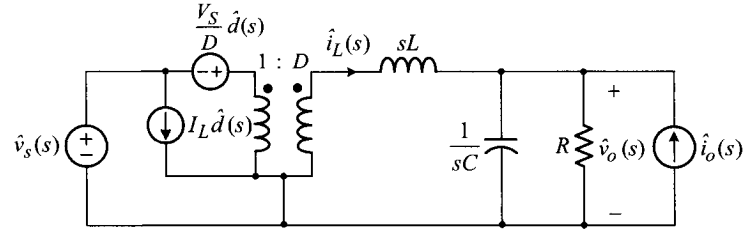


Figure 5.20 s-domain small-signal model of buck converter.

plots and analysis of the frequency response of dc-to-dc converters will be covered in Chapter 6.

■ EXAMPLE 5.7 Power Stage Transfer Functions of Buck Converter

This example illustrates the use of the s-domain small-signal model of the converter power stage. Figure 5.20 shows the s-domain small-signal model of the ideal buck converter. Considering the small-signal output voltage as the output variable, three power stage transfer functions are defined as follows.

- $G_{vs}(s) \equiv \dfrac{\hat{v}_o(s)}{\hat{v}_s(s)}$: input-to-output transfer function
- $G_{vd}(s) \equiv \dfrac{\hat{v}_o(s)}{\hat{d}(s)}$: duty ratio-to-output transfer function
- $Z_p(s) \equiv \dfrac{\hat{v}_o(s)}{\hat{i}_o(s)}$: load current-to-output transfer function

Expressions for these transfer functions are readily determined from the s-domain small-signal model in Fig. 5.20. For example, the duty ratio-to-output transfer function, $G_{vd}(s)$, is found by evaluating $\hat{v}_o(s)/\hat{d}(s)$ with the condition $\hat{v}_s(s) = \hat{i}_s(s) = 0$

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{V_S}{D} D \frac{\frac{1}{sC} \parallel R}{sL + \frac{1}{sC} \parallel R} = \frac{V_S}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \tag{5.62}$$

with

$$Q = R\sqrt{\frac{C}{L}} \tag{5.63}$$

and

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{5.64}$$

The input-to-output transfer function is given by

$$G_{vs}(s) = \frac{\hat{v}_o(s)}{\hat{v}_s(s)} = D\frac{\dfrac{1}{sC} \parallel R}{sL + \dfrac{1}{sC} \parallel R} = \frac{D}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{5.65}$$

The load current-to-output transfer function becomes

$$Z_p(s) = \frac{\hat{v}_o(s)}{\hat{i}_o(s)} = sL \parallel \frac{1}{sC} \parallel R = \frac{sL}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{5.66}$$

The transfer functions can be converted into Bode plots to reveal frequency response characteristics of the power stage, as will be demonstrated in the next chapter.

5.5 SMALL-SIGNAL GAIN OF PWM BLOCK

This section presents the small-signal modeling of the PWM block. While the procedure and outcome of the modeling are relatively straightforward, the PWM block is an essential ingredient of the small-signal model of closed-loop controlled PWM converters.

Figure 5.21 illustrates the operation of the PWM block in a closed-loop controlled PWM converter. The PWM block compares the control signal v_{con} against the ramp signal, V_{ramp}, to generate the pulsewidth modulated switch drive signal. The PWM output is represented by the switching function $q(t)$, while the cycle-by-cycle duty ratio of the PWM output is depicted as d_{k-1}, d_k, d_{k+1}, and d_{k+2}. From the PWM waveforms highlighted with thick lines in Fig. 5.21, the following relationship can be seen

$$d_k T_s : T_s = v_{con}(t^*) : V_m \tag{5.67}$$

where d_k denotes the duty ratio in the kth switching cycle, V_m is the height of the ramp signal, and t^* is the time instant the ramp signal V_{ramp} intersects with the control voltage v_{con}.

The relationship (5.67) is rearranged as $d_k = v_{con}(t^*)/V_m$ and subsequently approximated to

$$d_k = \frac{v_{con}(t)}{V_m} \tag{5.68}$$

with the assumption that v_{con} does not change widely within the kth switching period. If v_{con} is further restricted to change slowly over several switching periods, the cycle-by-cycle variation in the on-time period is small and d_k thus can be approximated by the continuous duty ratio $d(t)$: $d_k \approx d(t)$. By replacing d_k with $d(t)$ and taking the local average of v_{con}, (5.68) becomes

$$d(t) = \frac{\bar{v}_{con}(t)}{V_m} \tag{5.69}$$

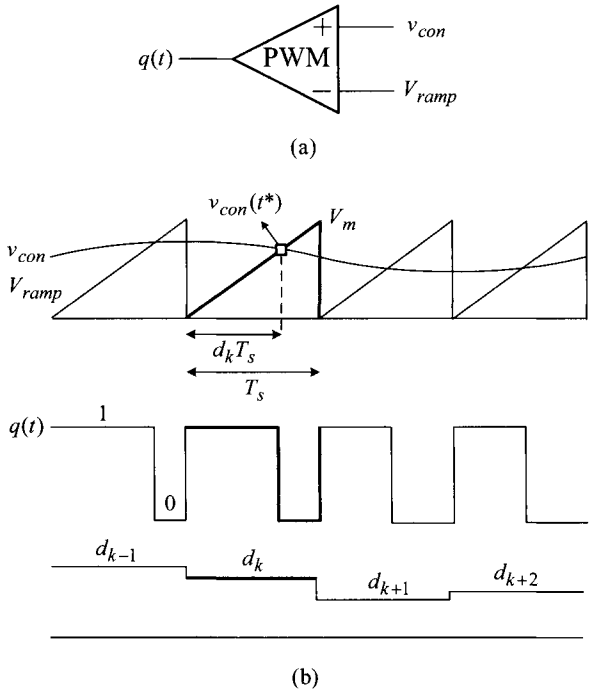


Figure 5.21 PWM block and its major waveforms. (a) PWM block. (b) PWM waveforms.

resulting in an averaged functional description of the PWM block.

Application of the linearization process to (5.69) yields

$$D + \hat{d}(t) = \frac{1}{V_m}(V_{con} + \hat{v}_{con}(t)) \tag{5.70}$$

The small-signal equation of the PWM process is now given by

$$\hat{d}(t) = \frac{1}{V_m}\hat{v}_{con}(t) \tag{5.71}$$

leading to the s-domain small-signal gain of the PWM block

$$\frac{\hat{d}(s)}{\hat{v}_{con}(s)} \equiv F_m = \frac{1}{V_m} \tag{5.72}$$

The constant small-signal gain of the PWM block is termed as the *PWM gain* or *modulator gain* F_m. The PWM gain is given by the inverse of the height of the ramp signal: $F_m = 1/V_m$. This simple result is the outcome of the fundamental assumption that the control voltage v_{con} does not vary widely within one switching period and only changes slowly over several switching periods.

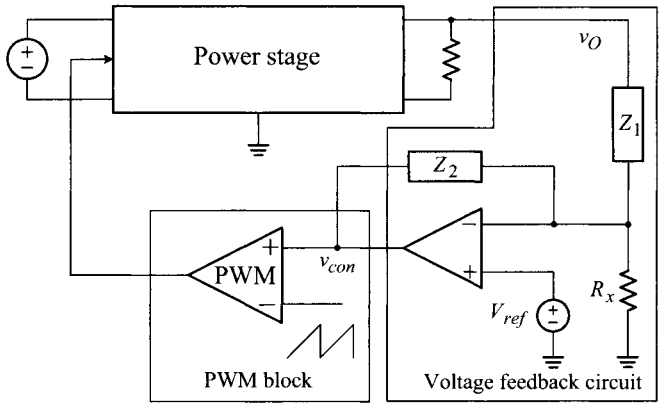


Figure 5.22 PWM converter and voltage feedback circuit.

5.6 SMALL-SIGNAL MODEL FOR PWM DC-TO-DC CONVERTERS

Figure 5.22 shows the block diagram representation of a closed-loop controlled PWM converter. Because the small-signal models for the power stage and PWM block are already developed, the modeling for the entire PWM converter will be completed if the small-signal characteristics of the voltage feedback circuit are incorporated. This section discusses the voltage feedback circuit and presents the small-signal models of the three basic PWM converters.

5.6.1 Voltage Feedback Circuit

The general structure of the voltage feedback circuit is shown in Fig. 5.22. While the voltage feedback circuit retains the same configuration as that of Section 3.6.1, it has an additional resistance R_x. When R_x is not present, the output voltage is regulated at the reference voltage, $V_O = V_{ref}$, as discussed in Section 3.6.1. The resistance R_x provides a means of controlling the output voltage with a fixed reference voltage V_{ref}. This section first discusses the output voltage control and subsequently presents the small-signal transfer function of the voltage feedback circuit.

Output Voltage Control

Referring to Fig. 5.22, the node equation at the inverting terminal of the error amplifier is given by

$$\frac{v_O - V_{ref}}{Z_1(s)} - \frac{V_{ref}}{R_x} = \frac{V_{ref} - v_{con}}{Z_2(s)} \tag{5.73}$$

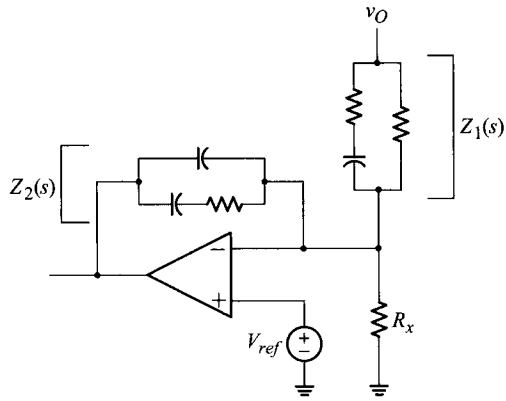


Figure 5.23 Voltage feedback circuit in which $|Z_2(j0)|$ is infinite while $|Z_1(j0)|$ is finite.

which is rearranged as

$$V_{ref} - v_{con} = \frac{Z_2(s)}{Z_1(s)}\left(v_O - V_{ref}\left(1 + \frac{Z_1(s)}{R_x}\right)\right) \tag{5.74}$$

The output voltage control is explained using the expression in the right-hand side of (5.74). If the magnitude of the impedance ratio $|Z_2(j0)/Z_1(j0)|$ is infinite, the term '$V_O - V_{ref}(1 + |Z_1(j0)|/R_x)$' should converge to zero, in order to make their product finite. Justifications for this argument were given in Section 3.6.1. When $Z_1(s)$ and $Z_2(s)$ are selected such that $|Z_2(j0)| = \infty$, while $|Z_1(j0)|$ is finite, the steady-state output voltage is determined as

$$V_O - V_{ref}\left(1 + \frac{Z_1(j0)}{R_x}\right) = 0 \quad \Rightarrow V_O = V_{ref}\left(1 + \frac{|Z_1(j0)|}{R_x}\right) \tag{5.75}$$

An example of the voltage feedback circuit, in which $|Z_2(j0)| = \infty$ and $|Z_1(j0)|$ is finite, is shown in Fig. 5.23. In fact, this circuit was introduced in Section 3.6.1 as the voltage feedback circuit for the buck converter.

Equation (5.75) indicates that the output voltage is controlled by varying R_x. While alternative schemes can be employed, the feedback circuit structure in Fig. 5.22 has an advantage over other methods. This advantage will become clear when its small-signal transfer function is analyzed in the next section.

Voltage Feedback Compensation

The transfer function of the voltage feedback circuit is readily found by noting that the inverting terminal of the op amp in Fig. 5.22 is an ac ground. For the small-signal ac analysis, V_{ref} is replaced with a short circuit and the inverting terminal thus becomes a virtual ground for ac signal. With this observation, a node equation is written at the

inverting terminal of the op amp

$$\frac{v_o(s) - 0}{Z_1(s)} = \frac{0 - v_{con}(s)}{Z_2(s)} \tag{5.76}$$

which is rearranged to yield the transfer function of the voltage feedback circuit

$$\frac{v_{con}(s)}{v_o(s)} = -\frac{Z_2(s)}{Z_1(s)} \equiv -F_v(s) \tag{5.77}$$

with

$$F_v(s) = \frac{Z_2(s)}{Z_1(s)} \tag{5.78}$$

The transfer function $F_v(s)$ is called *voltage feedback compensation*. The condition for the dc regulation now becomes

$$|Z_2(j0)| = \infty \tag{5.79}$$

implicitly assuming $|Z_1(j0)|$ is finite. Equation (5.78) indicates that the voltage feedback compensation is not affected by the output voltage-controlling resistor R_x. Accordingly, the voltage feedback circuit could control the output voltage without altering its transfer function. This desirable feature may not exist if other structures are selected for the voltage feedback circuit.

5.6.2 Small-Signal Model for PWM Converters

Figure 5.24 shows a general functional diagram of closed-loop controlled PWM converters. The PWM switch is combined with the inductor, and the resulting circuitry is considered as a single circuit element. The outward terminal at the inductor side is denoted as **i**. Figure 5.24 could represent any of the three basic PWM converters by using different power stage connections. With the connections {a–X p–Y i–Z }, Fig. 5.24 represents the buck converter. Similarly, the connections {i–X a–Y p–Z } lead to the boost converter, while the connections {a–X i–Y p–Z } yield the buck/boost converter.

The small-signal model for the PWM converters can be obtained from Fig. 5.24 by replacing the PWM switch, PWM block, and voltage feedback circuit with their respective small-signal models, and by introducing appropriate small-signal excitations. Figure 5.25 shows the small-signal model derived as outlined above. This figure can be arranged to represent the small-signal model of the buck, boost, or buck/boost converter. For example, Fig. 5.25 becomes the small-signal model of the buck converter when the connections {a–X p–Y i–Z } are assumed.

The small-signal model in Fig. 5.25 is converted into a block diagram representation shown in Fig. 5.26. In the block diagram, the small-signal sources $\hat{v}_s(s)$ and $\hat{i}_o(s)$ are the input variables, $\hat{v}_o(s)$ is the output variable, and $\hat{d}(s)$ is the control variable. Regarding the gain blocks, F_m is the PWM gain, $F_v(s)$ is the voltage feedback compensation, and the other gain blocks represent the power stage transfer functions: $G_{vs}(s) = \hat{v}_o(s)/\hat{v}_s(s)$, $G_{vd}(s) = \hat{v}_o(s)/\hat{d}(s)$, and $Z_p(s) = \hat{v}_o(s)/\hat{i}_o(s)$. The – sign in

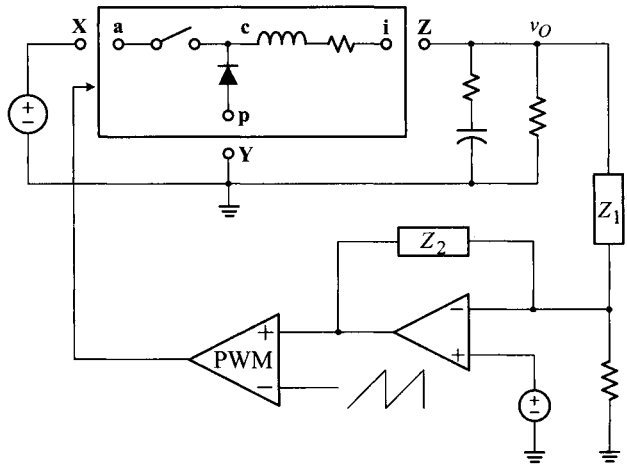


Figure 5.24 General functional diagram for three basic PWM converters.

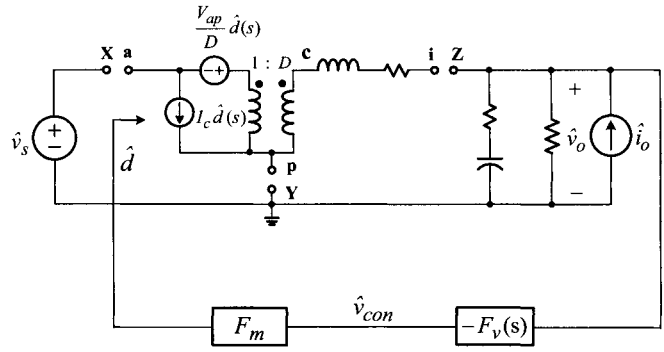


Figure 5.25 Small-signal model for three basic PWM converters.

front of the voltage feedback compensation, $F_v(s)$, signifies the *negative* feedback control embedded in the control scheme.

The small-signal model of the closed-loop controlled converter or its block diagram representation is a linear time-invariant model to which all the conventional s-domain analysis techniques can be directly applied. The utility and versatility of the small-signal model will be demonstrated in the later chapters which deal with the small-signal analysis and control design of closed-loop controlled PWM dc-to-dc converters.

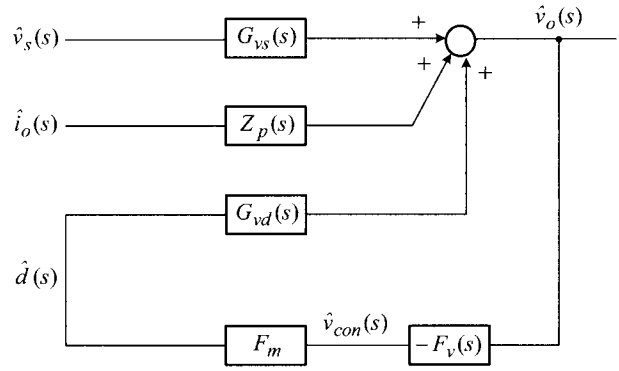


Figure 5.26 Block diagram representation of small-signal model.

5.7 SUMMARY

In this chapter, we developed the s-domain small-signal model for the three basic PWM dc-to-dc converters. As a linear time-invariant model, the small-signal model allows us to investigate the dynamics of the PWM converters using standard s-domain analysis techniques. The small-signal model is derived in a general and unified way so that a single model could represent all the three basic PWM converters.

We employed several modeling techniques to derive the small-signal model for the PWM converters. The averaging method is used to eliminate the time variance from the power stage configuration and the linearization process is employed to remove nonlinearities from the power stage dynamics and PWM process.

Two very important averaging methods, the state-space averaging and circuit averaging, are studied for the power stage modeling. The linearization process is then employed. Application of the circuit averaging to the PWM switch and ensuing linearization led to the PWM switch model, which is utilized as an instrumental tool in deriving a universal small-signal model for the three basic PWM converters.

The small-signal model for the PWM block was found to be a constant PWM gain, under the assumption that the control signal only varies narrowly and slowly within the switching period of the converter. The PWM switch model and PWM gain are combined with the voltage feedback compensation, leading to the complete small-signal model for closed-loop controlled PWM dc-to-dc converters. With this small-signal model, we can perform the dynamic analysis of the nonlinear time-variant PWM converters in the manner that has been used for conventional linear time-invariant systems. The value of the small-signal model will be demonstrated in the later chapters dealing with the dynamic analysis and control design of PWM dc-to-dc converters.

REFERENCES

1. J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, *Principles of Power Electronics*, Addison-Wesley Publishing Co, 1991.
2. R. D. Middlebrook and S. Ćuk, *Advances in Switch-Mode Power Conversion*, TESLAco, Pasadena, CA, 1983.
3. V. Vorpérian, *Fast Analytical Techniques for Electrical and Electronic Circuits*, Cambridge University Press, 2002.

PROBLEMS

5.1* Consider the circuits shown in Fig. P5.1 and answer the questions.

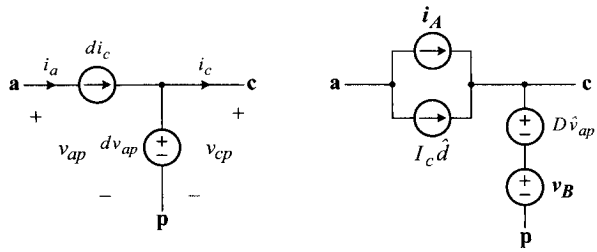


Fig. P5.1

a) Shown in Fig. P5.1(a) is an average model of a nonlinear switching device. The variable d represents the continuous duty ratio of the active switch. Construct the nonlinear switching device using semiconductor switches.

b) Prove that the small-signal equations of the nonlinear switching device can be represented by the circuit model in Fig. P5.1(b). Find the expressions for the dependent current source i_A and voltage source v_B.

c) Construct a small-signal model of the buck converter using Fig. P5.1(b). Express the dependent sources in terms of the operating conditions and circuit variables of the buck converter.

d) Construct an average model of the boost converter using Fig. P5.1(a). Show all the model parameters.

e) Build a small-signal model of the boost converter using Fig. P5.1(b). Show all the model parameters.

5.2* Figure P5.2 shows the circuit diagrams of the three basic PWM converters with the parasitic resistances.

a) Formulate the switched state-space model for each of the three basic converters.

b) Convert the switched state-space models you derived in **a)** into the averaged state-space models for the three basic converters.

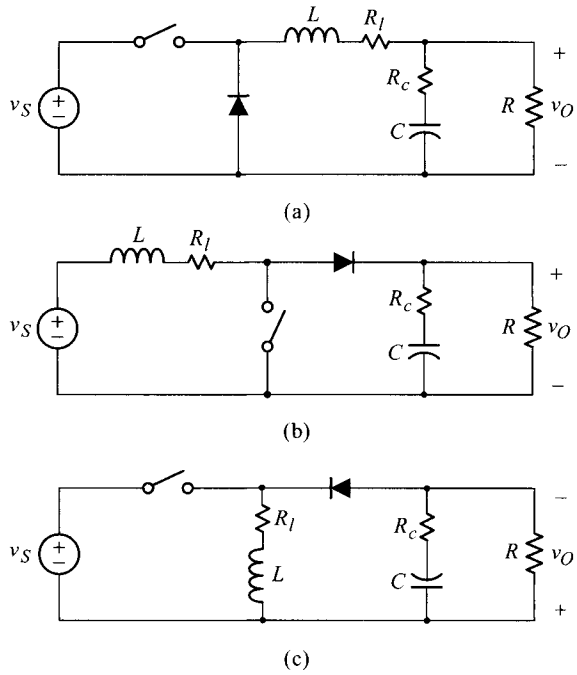


Fig. P5.2

5.3** A cascaded converter shown in Fig. P5.3 is configured by connecting a boost converter and buck converter. Answer the questions.

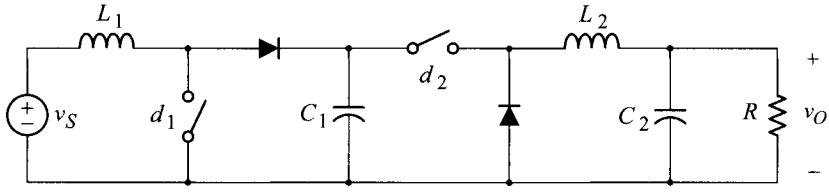


Fig. P5.3

a) Construct a nonlinear circuit model that predicts the time-averaged power stage dynamics of the converter during both transition period and steady state.

b) Draw a linear circuit model that predicts the small-signal dynamics of the converter under the small-signal assumption. Express all the circuit components as functions of circuit variables and operational conditions of the converter.

5.4* Referring to the circuit shown in Fig. P5.4(a), answer the questions.

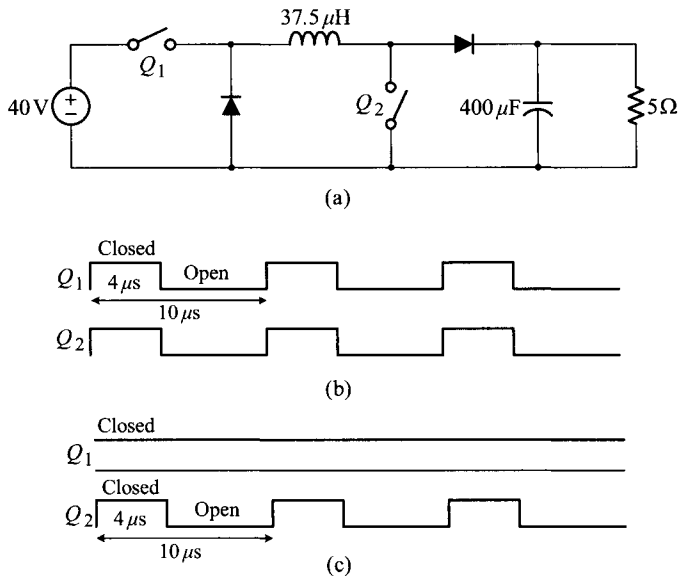


Fig. P5.4

a) The switch drive signals shown in Fig. P5.4(b) are applied to the circuit. Draw an average circuit model that predicts the time-averaged behavior of the converter. Show all the model parameters.

b) Repeat **a)** for the switch drive signal in Fig. P5.4(c).

5.5 Figure P5.5 shows the circuit diagram of a buck/boost converter with the parasitic resistance of the inductor.

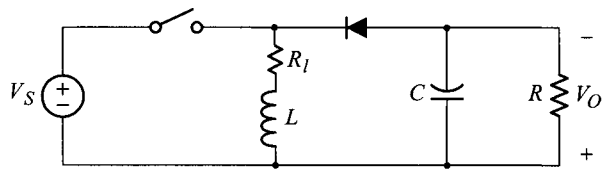


Fig. P5.5

a) Use the flux balance and charge balance conditions to find the expression for the voltage gain V_O/V_S of the converter.

b) Use the averaged model of the power stage to derive the voltage gain expression of the converter.

5.6* Assume that the functional relationship between the duty ratio d and the control voltage v_{con} of a certain PWM converter is given by

$$d(t) = 1 - \frac{0.2}{v_{con}(t)}$$

a) Find the expression for the small-signal modulator gain, $F_m = \hat{d}/\hat{v}_{con}$.

b) Find the numeric value for $F_m = \hat{d}/\hat{v}_{con}$ when $V_{con} = 2$ V.

5.7 Figure P5.7 shows the small-signal model of the buck converter with the parasitic resistances of reactive components. Find the accurate expressions for the three power stage transfer functions, $G_{vs}(s)$, $G_{vd}(s)$, and $Z_p(s)$.

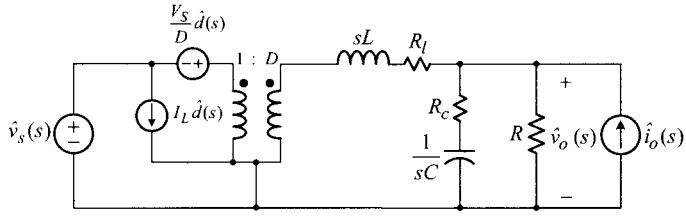


Fig. P5.7

5.8** Shown in Fig. P.5.8 is a PWM converter configured using a nonlinear switching network. The time-averaged expressions for the circuit variables associated with the nonlinear switching network are given by

$$\bar{v}_{ac}(t) = \big(1 - d(t)\big)\bar{v}_{bc}(t)$$
$$\bar{i}_b(t) = \big(1 - d(t)\big)\bar{i}_a(t)$$

where d represents the continuous duty ratio of the active switch.

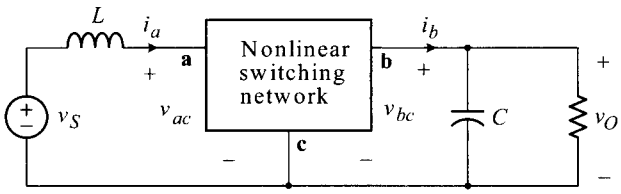


Fig. P5.8

a) Derive a set of equations that describe the small-signal dynamics of the nonlinear switching network.

b) Draw a small-signal circuit model for the nonlinear switching network. Show all model parameters.

c) Sketch the small-signal circuit model of the entire power converter. Show all model parameters.

d) Derive the input-to-output transfer function, $G_{vs}(s) = \hat{v}_o(s)/\hat{v}_s(s)$, in terms of the circuit parameters of the small-signal model.

5.9* The PWM can be performed by comparing the control signal v_{con} against the carrier signal. Different carrier signals can be used to implement various PWM schemes. Three examples of such PWM schemes are shown in Fig. P5.9. For each PWM scheme, find the expression for the modulator gain F_m.

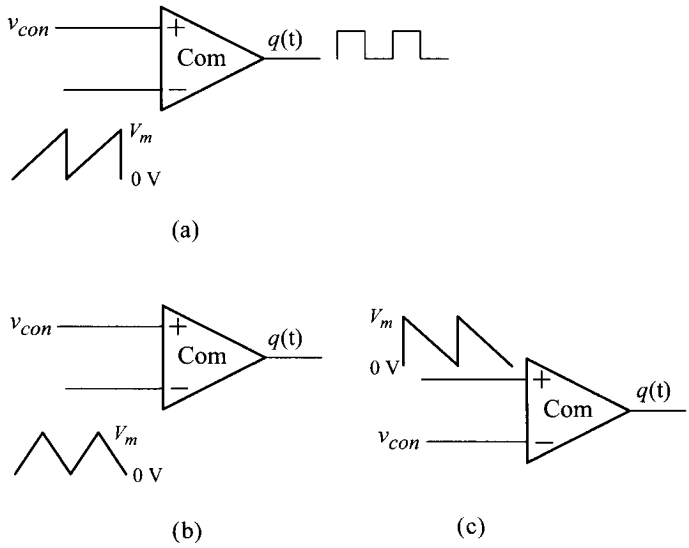


Fig. P5.9

5.10** Figure P5.10 shows the $v-i$ characteristics of a nonlinear device. Answer the questions.

a) Find the small-signal gain, $\hat{\imath}/\hat{v}$, at the operating point of $v = 4$ V and $i = 2$ mA.

b) Estimate the maximum magnitude of $\hat{v}(t)$ which validates the accuracy of the small-signal gain you found in **a)**.

c) Assume $v(t) = 4 + 0.1 \sin 20t$ and find the expression for $i(t)$.

d) Now assume $v(t) = 4 + 0.5 \sin 20t$ and evaluate the range of $|i(t)|$: ( ) < $|i(t)|$ < ( ).

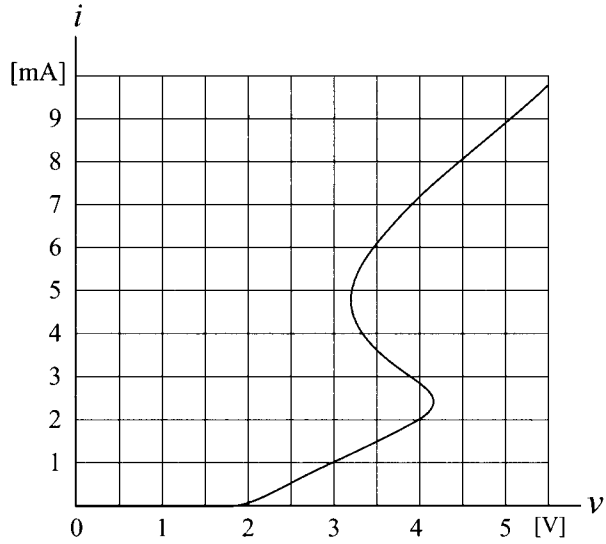


Fig. P5.10

CHAPTER 6

POWER STAGE TRANSFER FUNCTIONS

In the previous chapter, we developed s-domain small-signal models for the three basic PWM dc-to-dc converters: the buck converter, boost converter, and buck/boost converter. Using these small-signal models, we could perform the dynamic analysis and control design of nonlinear time-variant PWM dc-to-dc converters, in the same way as we do for conventional linear time-invariant systems.

In preparation for the analysis and design of PWM dc-to-dc converters, this chapter analyzes power stage transfer functions focusing on their frequency response characteristics. The first section covers the Bode plot representation of s-domain transfer functions. The later sections then present analytical expressions, Bode plot representations, and salient features of power stage transfer functions of the three basic PWM dc-to-dc converters. This chapter also discusses empirical approaches to the power stage dynamic analysis.

6.1 BODE PLOT FOR TRANSFER FUNCTIONS

The most useful outcome of the s-domain small-signal model is the transfer function which allows us to investigate the frequency response characteristics of the converter power stage. From the s-domain small-signal model, power stage transfer functions

Pulsewidth Modulated Dc-to-Dc Power Conversion. By Byungcho Choi

are derived using standard circuit analysis techniques. The resulting s-domain transfer functions are then transformed into Bode plots to reveal the frequency response characteristics. This section deals with the construction of Bode plots for s-domain transfer functions, thereby providing the underlying basics for the forthcoming converter power stage analysis.

6.1.1 Basic Definitions

Discussions start with the basic definitions which constitute the basis in constructing frequency response plots for s-domain transfer functions. These basic definitions include the transfer function, frequency response, and Bode plot representation.

Transfer Function

The transfer function is defined for linear time-invariant systems or circuits as the ratio of the Laplace transform of the output to the Laplace transform of the input, under the assumption that all initial conditions are zero

$$T(s) \equiv \frac{v_o(s)}{v_s(s)} \tag{6.1}$$

where $v_o(s)$ is the s-domain expression, or Laplace transform, of the output variable while $v_s(s)$ is the s-domain expression of the input variable. For general cases, the transfer function is obtained by performing the Laplace transform operation on the differential equation or state equation of the system. However, for linear time-invariant circuits, the transfer function can be directly derived from the circuit diagram by adopting s-domain representations for circuit components and variables and applying basic circuit theorems.

Although originally defined for linear time-invariant systems, the transfer function can be extended to nonlinear time-variant PWM converters to describe the frequency response of power stage circuit variables. For this case, the transfer functions are derived from the s-domain small-signal power stage model, as illustrated in Example 5.7. Readers may refer to Section 5.4 for the concept of the frequency response and transfer function for PWM dc-to-dc converters.

Frequency Response

The frequency response denotes the input-output relationship of linear or linearized systems, under the assumption that the system is excited by a sinusoidal input. Accordingly, the frequency response is evaluated from the s-domain transfer function by replacing the complex frequency s with $j\omega$

$$T(j\omega) \equiv \frac{v_o(j\omega)}{v_s(j\omega)} \tag{6.2}$$

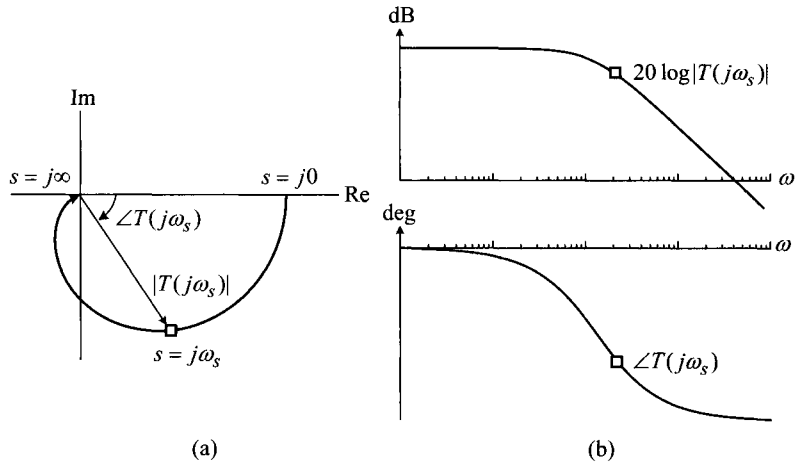


Figure 6.1 Graphical representation of frequency response. (a) Polar plot. (b) Bode plot.

where ω is the frequency of the sinusoidal excitation. The magnitude relationship of (6.2) becomes the magnitude response

$$|T(j\omega)| \equiv \frac{|v_o(j\omega)|}{|v_s(j\omega)|} \tag{6.3}$$

and the phase relationship of (6.2) is the phase response of the system

$$\angle T(j\omega) \equiv \angle v_o(j\omega) - \angle v_s(j\omega) \tag{6.4}$$

The magnitude and phase responses are collectively called the frequency response. Equations (6.3) and (6.4) indicate that the frequency response is found by evaluating the magnitude and phase of the transfer function with $s = j\omega$, while sweeping the frequency ω for the range of interest.

Bode Plot Representation

The frequency response can be graphically displayed in the polar plot format or Bode plot format. Each of these graphical representations has its own value in s-domain analysis. Figure 6.1(a) illustrates the polar plot representation of the frequency response, where the frequency response is converted into the polar form and portrayed as a single curve in s-plain. Each point in the polar plot represents the frequency response in the polar coordinate, from which the magnitude and phase responses at a specific frequency ω_s are defined, as illustrated in Fig. 6.1(a).

Figure 6.1(b) shows the Bode plot representation of the frequency response. The magnitude response is first calculated in dB scale, $20 \log|T(j\omega)|$, while the phase is expressed in degree °. The magnitude and phase responses are then individually

displayed on the two separate plots. In the magnitude plot, the dB-scale magnitude is shown on the y-axis, while the frequency ω is displayed in the log scale on the x-axis. In the phase plot, the linear-scale phase is shown against the log-scale frequency axis. Each point in the magnitude or phase plot represents the corresponding magnitude or phase response evaluated at a specific frequency ω_s, as shown in Fig. 6.1(b).

6.1.2 Bode Plots for Multiplication Factors

It is assumed that the transfer function $T(s)$ for the Bode plot construction has been factorized into the following format

$$T(s) = K\frac{1}{s^{\pm j}}\frac{1}{1+\dfrac{s}{\omega_p}} \cdots \left(1+\frac{s}{\omega_z}\right)\cdots \frac{1}{1+\dfrac{s}{Q_p\omega_o}+\dfrac{s^2}{\omega_o^2}} \cdots \left(1+\frac{s}{Q_z\omega_o}+\frac{s^2}{\omega_o^2}\right)\cdots \tag{6.5}$$

which is known as the time constant form. Each term in (6.5) is called the multiplication factor. The Bode plot for the transfer function $T_s(s)$ can be constructed by

1) finding the Bode plot of each individual multiplication factor, and

2) combining the resulting individual Bode plots.

This section discusses Bode plots of multiplication factors. The construction of the composite Bode plot for the transfer function will be treated in the next section.

Constant

Figure 6.2 shows the Bode plot for a constant K. The magnitude plot is a flat line of $20\log K$ for both positive K and negative K. However, the phase is $0°$ for $K > 0$ and $-180°$ for $K < 0$.

Single and Double Integration Functions

The single integration function

$$F(s) = \frac{K_i}{s} \tag{6.6}$$

is evaluated with $s = j\omega$

$$F(j\omega) = \frac{K_i}{j\omega} \tag{6.7}$$

for the Bode plot construction. The above expression is split into the magnitude response

$$20\log|F(j\omega)| = 20\log\left(\frac{K_i}{\omega}\right) \tag{6.8}$$

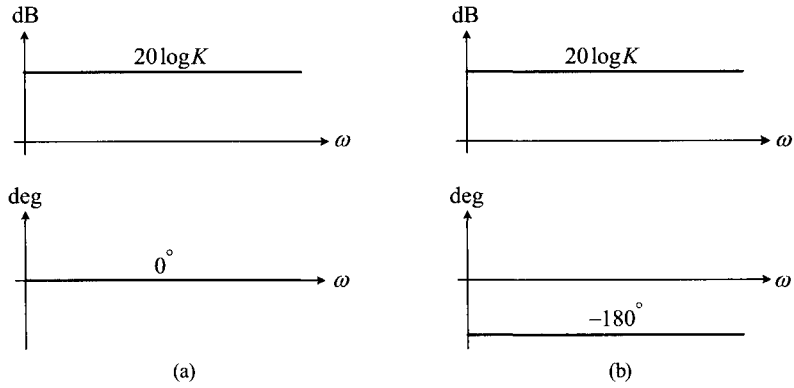


Figure 6.2 Bode plots for constant K. (a) $K > 0$. (b) $K < 0$.

and the phase response

$$\angle F(j\omega) = -90^\circ \tag{6.9}$$

Figure 6.3(a) shows the Bode plot based on (6.8) and (6.9). The magnitude linearly decays with a −20 dB/dec slope while the phase stays at −90°. The magnitude plot crosses the 0 dB line at $\omega = K_i$: $20 \log K_i/K_i = 0$ dB.

For notational simplicity, the following numeric symbols will be used to represent the slope of the magnitude curve

- −2 slope: −40 dB/dec slope
- −1 slope: −20 dB/dec slope
- +1 slope: +20 dB/dec slope
- +2 slope: +40 dB/dec slope

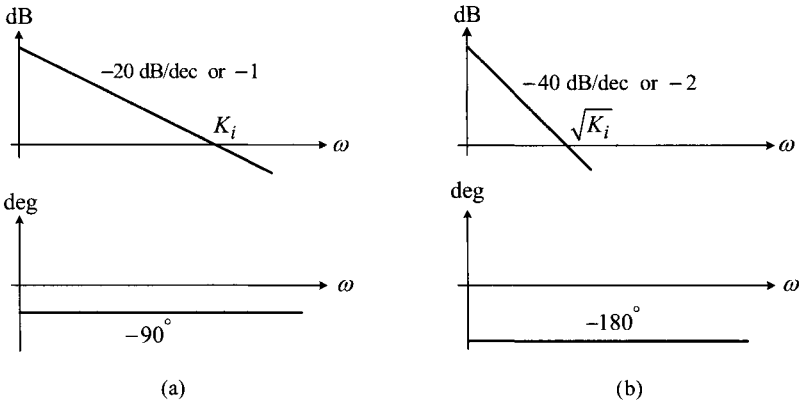


Figure 6.3 Bode plots for single and double integration functions. (a) $F(s) = K_i/s$. (b) $F(s) = K_i/s^2$.

The double integration function

$$F(s) = \frac{K_i}{s^2} \tag{6.10}$$

is evaluated as

$$F(j\omega) = -\frac{K_i}{\omega^2} \tag{6.11}$$

leading to

$$20\log|F(j\omega)| = 20\log\left(\frac{K_i}{\omega^2}\right) \tag{6.12}$$

and

$$\angle F(j\omega) = -180^\circ \tag{6.13}$$

The Bode plot is shown in Fig. 6.3(b). The descending slope of the magnitude plot is −40 dB/dec slope, or −2 slope, and the phase remains at −180°. The 0 dB crossover now occurs at $\omega = \sqrt{K_i}$: $20\log K_i/\sqrt{K_i}^2 = 0$ dB.

Single and Double Differentiation Functions

The single differentiation function $F(s) = K_d s$ is evaluated as $F(j\omega) = K_d j\omega$, yielding the magnitude response

$$20\log|F(j\omega)| = 20\log(K_d\,\omega) \tag{6.14}$$

and phase response

$$\angle F(j\omega) = 90^\circ \tag{6.15}$$

The Bode plot for the single differentiation is shown in Fig. 6.4(a). The magnitude plot linearly increases with a 20 dB/dec slope, or +1 slope, and crosses the 0 dB line at $\omega = 1/K_d$, while the phase stays at 90°.

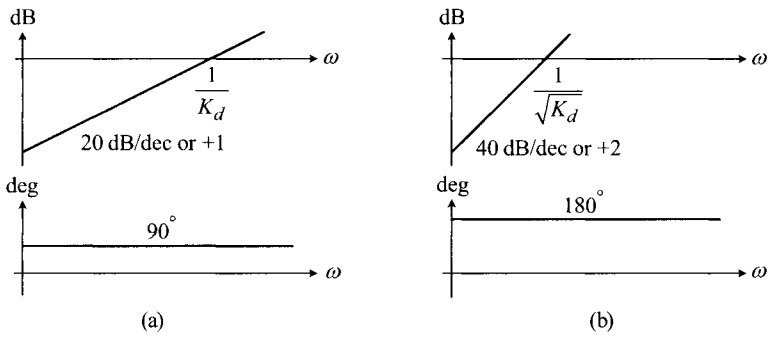


Figure 6.4 Bode plots for single and double differentiation functions. (a) $F(s) = K_d s$. (b) $F(s) = K_d s^2$.

The double differentiation function $F(s) = K_d s^2$ is converted into $F(j\omega) = K_d(j\omega)^2$ for the Bode plot construction. The magnitude and phase responses respectively become

$$20\log|F(j\omega)| = 20\log(K_d\,\omega^2) \tag{6.16}$$

and

$$\angle F(j\omega) = 180^\circ \tag{6.17}$$

leading to the Bode plot shown in Fig. 6.4(b). The magnitude plot increases with 40 dB/dec slope, or +2 slope, and the 0 dB crossover occurs at $\omega = 1/\sqrt{K_d}$. The phase remains at 180° for this case.

Single Pole and Single Zero Functions

The single pole function

$$F(s) = \frac{1}{1 + \dfrac{s}{\omega_p}} \tag{6.18}$$

is evaluated with $s = j\omega$

$$F(j\omega) = \frac{1}{1 + \dfrac{j\omega}{\omega_p}} \tag{6.19}$$

yielding the magnitude response

$$20\log|F(j\omega)| = 20\log\frac{1}{\sqrt{1 + \left(\dfrac{\omega}{\omega_p}\right)^2}} \tag{6.20}$$

and phase response

$$\angle F(j\omega) = -\tan^{-1}\left(\frac{\omega}{\omega_p}\right) \tag{6.21}$$

Although the Bode plot can accurately be drawn from (6.20) and (6.21), it is usually unnecessary to find the exact Bode plot. Instead, the asymptotic plot that describes the asymptotic behavior of the Bode plot is sufficient for most situations. The asymptotic plots can quickly be sketched from the transfer function and provide all the important information about the frequency response. Furthermore, an asymptotic plot can readily be refined so that the resulting plot closely resembles the actual frequency response.

For the asymptotic Bode plot construction, (6.19) is split into three expressions

$$F(j\omega) = \frac{1}{1 + \dfrac{j\omega}{\omega_p}} \approx \begin{cases} 1 & \text{at frequencies where} \quad \omega < \omega_p \\ \dfrac{1}{1+j} & \text{at frequency} \quad \omega = \omega_p \\ \dfrac{\omega_p}{j\omega} & \text{at frequencies where} \quad \omega > \omega_p \end{cases} \tag{6.22}$$

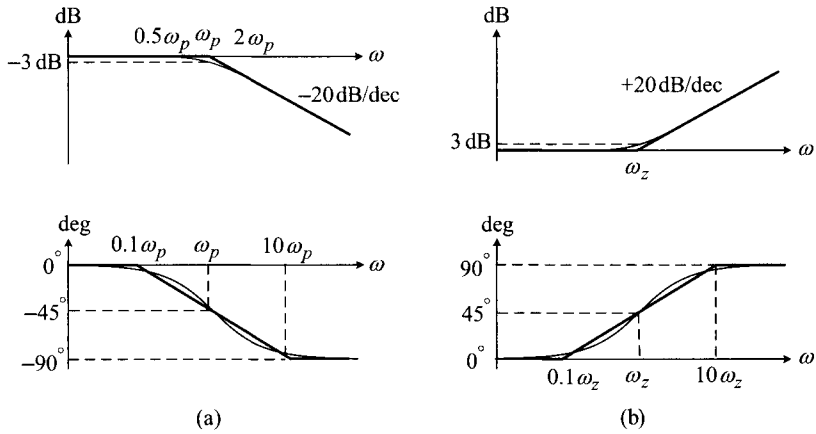


Figure 6.5 Bode plots for single pole and single zero functions. (a) Single pole function. (b) Single zero function.

using the pole frequency ω_p as the borderline for approximations.

The top expression in the right-hand side of (6.22) describes the asymptotic behavior of $F(j\omega)$ at frequencies below ω_p, while the bottom expression approximates $F(j\omega)$ at frequencies beyond ω_p. In other words, the top expression provides the low-frequency asymptotes for the magnitude and phase plots: $|F| = 0$ dB and $\angle F = 0°$. Similarly, the bottom expression produces the high-frequency asymptotes: $20\log|F(j\omega)| = 20\log(\omega_p/\omega)$ and $\angle F(j\omega) = -90°$. The high-frequency asymptotes are the same as those of a single integration function passing through the 0 dB line at ω_p. The middle equation is the exact frequency response evaluated at ω_p

$$20\log|F(j\omega_p)| = 20\log\left|\frac{1}{1+j}\right| = 20\log\left(\frac{1}{\sqrt{2}}\right) \approx -3 \text{ dB} \tag{6.23}$$

$$\angle F(j\omega_p) = \angle\frac{1}{1+j} = -45° \tag{6.24}$$

Figure 6.5(a) shows the asymptotic plots of the single pole function, in comparison with the exact plots. The thick line represents the asymptotic plots while the thin line describes the exact plots. The asymptotic magnitude plot is formed by merging the low- and high-frequency asymptotes at ω_p. The asymptotic phase plot is constructed by bridging the low- and high-frequency asymptotes through a line segment that ramps down linearly from $0.1\,\omega_p$ to $10\,\omega_p$ with $-45°$/dec slope. The asymptotic magnitude plot shows small deviations from the exact plot in the frequency range $0.5\,\omega_p < \omega < 2\,\omega_p$ with a maximum 3 dB error at ω_p; for this reason, the pole frequency ω_p is called the 3 dB *frequency*. The asymptotic phase plot also provides a good approximation for the exact plot. In particular, the asymptotic plot shows the exact $-45°$ phase at ω_p.

As illustrated in Fig. 6.5(a), an accurate Bode plot can be constructed, with negligible and predictable errors, by smoothly connecting the low- and high-frequency asymptotes so that the combined curves pass the exact values at ω_p: -3 dB for $|F(j\omega_p)|$ and $-45°$ for $\angle F(j\omega_p)$.

The single zero function

$$F(s) = 1 + \frac{s}{\omega_z} \tag{6.25}$$

is approximated to

$$F(j\omega) = 1 + \frac{j\omega}{\omega_z} \approx \begin{cases} 1 & \text{at frequencies where } \omega < \omega_z \\ 1 + j & \text{at frequency } \omega = \omega_z \\ j\dfrac{\omega}{\omega_z} & \text{at frequencies where } \omega > \omega_z \end{cases} \tag{6.26}$$

for the asymptotic Bode plot construction. The bottom term in (6.26) constitutes the high-frequency asymptote, which is a single differentiation function crossing the 0 dB line at ω_z. The middle term is the exact frequency response at ω_z

$$20\log|F(j\omega_z)| = 20\log|1 + j| \approx 3 \text{ dB} \tag{6.27}$$

and

$$\angle F(j\omega_z) = \angle(1 + j) = 45° \tag{6.28}$$

Figure 6.5(b) shows the asymptotic and exact Bode plots of the single zero function.

Double Pole and Double Zero Functions

The double pole and double zero functions frequently appear in the upcoming small-signal analysis of power stage transfer functions. The double pole function is given by

$$F(s) = \frac{1}{1 + \dfrac{s}{Q_p\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{6.29}$$

where ω_o is the double pole frequency and Q_p is the damping ratio. The double pole function with $Q_p > 0.5$ is approximated to

$$F(j\omega) = \frac{1}{1 + \dfrac{j\omega}{Q_p\omega_o} - \dfrac{\omega^2}{\omega_o^2}} \approx \begin{cases} 1 & \text{at frequencies where } \omega < \omega_o \\ \dfrac{Q_p}{j} & \text{at frequency } \omega = \omega_o \\ -\dfrac{\omega_o^2}{\omega^2} & \text{at frequencies where } \omega > \omega_o \end{cases} \tag{6.30}$$

The low-frequency asymptote is the 0 dB line, as is the case with the single pole

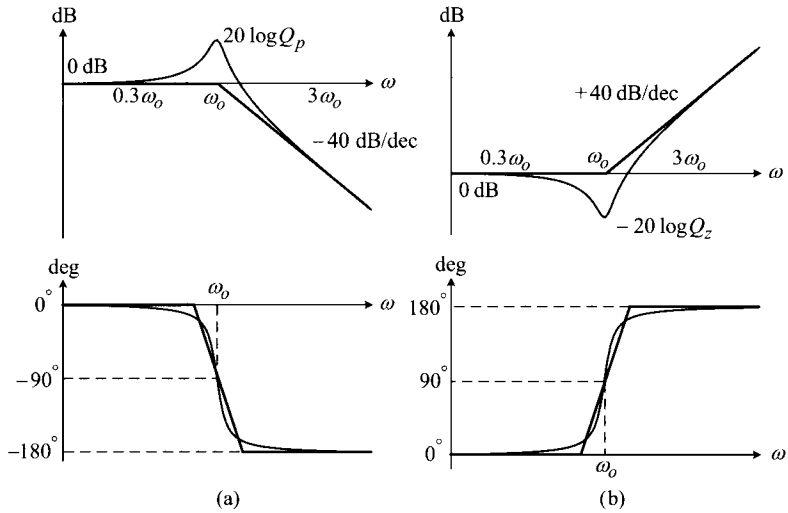


Figure 6.6 Bode plots for double pole and double zero functions. (a) Double pole function. (b) Double zero function.

function. On the other hand, the high-frequency asymptote is a double integration function passing through the 0 dB line at ω_o. The exact response at ω_o is

$$20 \log |F(j\omega_o)| = 20 \log \left| \frac{Q_p}{j} \right| = 20 \log Q_p \tag{6.31}$$

and

$$\angle F(j\omega_o) = \angle \frac{Q_p}{j} = -90° \tag{6.32}$$

Figure 6.6(a) shows the asymptotic plots of the double pole function, in parallel with the exact plots. The asymptotic magnitude plot is formed by merging low- and high-frequency asymptotes at ω_o. The phase plot is created by connecting the low- and high-frequency asymptotes with a line segment linearly declining at frequencies around ω_o.

The asymptotic magnitude plot shows a noticeable difference from the exact plot in the frequency range $0.3\,\omega_o < \omega < 3\,\omega_o$. In particular, the exact magnitude plot shows a peaking of $20 \log Q_p$ at ω_o, which is not accounted for in the asymptotic plot. On the other hand, the asymptotic phase plot passes the exact $-90°$ point at ω_o, while producing some error at neighboring frequencies.

The accurate magnitude and phase characteristics of the double pole function can be determined by evaluating (6.29) at frequencies around ω_o. Such an analysis reveals that the transition patterns of the magnitude and phase curves are strongly influenced by the value of the damping ratio Q_p. Figure 6.7 shows the exact Bode plots of the double pole function in the frequency range $0.3\,\omega_o < \omega < 3\,\omega_o$ with different Q_p values

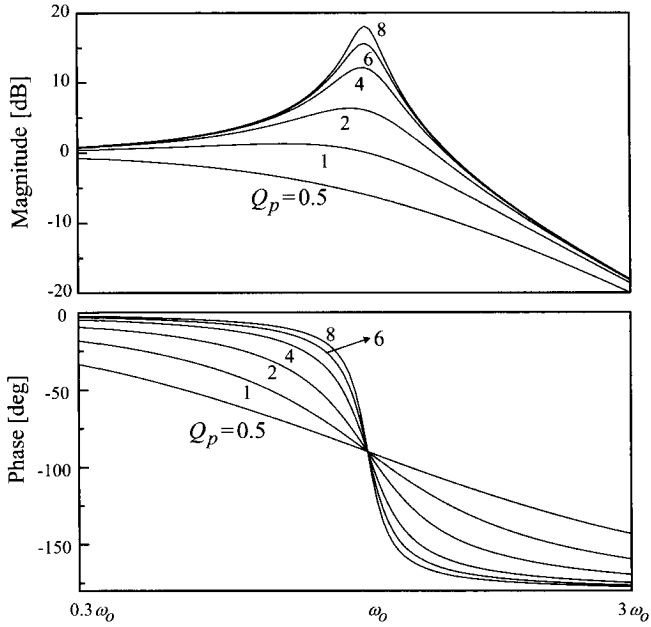


Figure 6.7 Exact Bode plots of double pole function with $0.5 < Q_p < 8$.

of $0.5 < Q_p < 8$. In the magnitude response, a larger Q_p generates a higher peaking at ω_o, resulting in a wider gap between the asymptote and exact plots. Regarding the phase response, a larger Q_p accelerates the decaying rate of the phase plot around ω_o, thereby exhibiting a more abrupt phase change in the narrower frequency range. These characteristics need to be incorporated when the actual frequency response is predicted from the asymptotic plots.

The double zero function

$$F(s) = 1 + \frac{s}{Q_z\omega_o} + \frac{s^2}{\omega_o^2} \tag{6.33}$$

with $Q_z > 0.5$ is approximated to

$$F(j\omega) = 1 + \frac{j\omega}{Q_z\omega_o} - \frac{\omega^2}{\omega_o^2} \approx \begin{cases} 1 & \text{at frequencies where } \omega < \omega_o \\ \dfrac{j}{Q_z} & \text{at frequency } \omega = \omega_o \\ -\dfrac{\omega^2}{\omega_o^2} & \text{at frequencies where } \omega > \omega_o \end{cases} \tag{6.34}$$

The bottom term in (6.34) indicates that the high-frequency asymptote is a double differentiation function crossing the 0 dB line at ω_o. Figure 6.6(b) shows the asymptotic

and exact plots for the double zero function. The construction and accuracy of the asymptotic plots are very similar to those of the double pole case. The magnitude plot shows a dipping of $20\log Q_z$ at ω_o, which was not accounted for in the asymptotic plot.

RHP Pole and RHP Zero Functions

The single pole function given by

$$F(s) = \frac{1}{1 - \dfrac{s}{\omega_p}} = \frac{1}{1 + \dfrac{s}{-\omega_p}} \tag{6.35}$$

is called the right-half plane (RHP) pole function in the sense that the pole $s = \omega_p$ is located in the right-half side of s-plane.

The RHP pole has unique characteristics and thus deserves special attentions. For the frequency response analysis, the transfer function is evaluated with $s = j\omega$

$$F(s) = \frac{1}{1 + \dfrac{j\omega}{-\omega_p}} \tag{6.36}$$

yielding the magnitude response

$$20\log|F(j\omega)| = 20\log\frac{1}{\sqrt{1 + \left(\dfrac{\omega}{-\omega_p}\right)^2}} = 20\log\frac{1}{\sqrt{1 + \left(\dfrac{\omega}{\omega_p}\right)^2}} \tag{6.37}$$

and phase response

$$\angle F(j\omega) = -\tan^{-1}\left(\frac{\omega}{-\omega_p}\right) = \tan^{-1}\left(\frac{\omega}{\omega_p}\right) \tag{6.38}$$

The above equations indicate that the magnitude response is the same as that of a regular pole function. However, the phase response follows the pattern of a zero function, rather than a pole function. Figure 6.8(a) shows the asymptotic and exact plots of the RHP pole function. The flat magnitude asymptote breaks at ω_p and rolls down by -20 dB/dec, or -1, slope thereafter, while the phase increases from 0° to 90° over the frequency range $0.1\,\omega_p < \omega < 10\,\omega_p$.

The frequency response of an RHP zero function

$$F(s) = 1 - \frac{s}{\omega_z} = 1 + \frac{s}{-\omega_z} \tag{6.39}$$

is evaluated as

$$|F(j\omega)| = 20\log\sqrt{1 + \left(\frac{\omega}{-\omega_z}\right)^2} = 20\log\sqrt{1 + \left(\frac{\omega}{\omega_z}\right)^2} \tag{6.40}$$

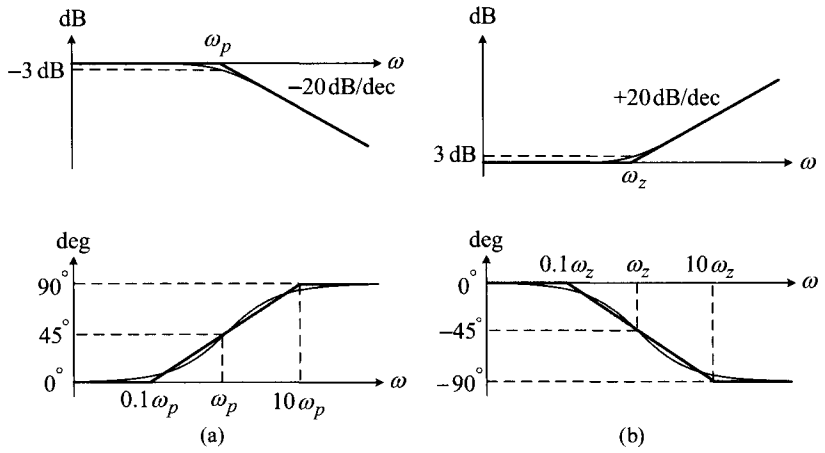


Figure 6.8 Bode plots for RHP pole and RHP zero functions. (a) RHP pole function. (b) RHP zero function.

and

$$\angle F(j\omega) = \tan^{-1}\left(\frac{\omega}{-\omega_z}\right) = -\tan^{-1}\left(\frac{\omega}{\omega_z}\right) \tag{6.41}$$

Regarding the phase characteristics, the RHP zero follows the pattern of a single pole function, not a zero function. Figure 6.8(b) shows the asymptotic and exact plots for the RHP zero function. In the neighborhood of the RHP zero ω_z, the 0 dB magnitude plot starts to ramp up with 20 dB/dec, or +1, slope, while the phase drops linearly from 0° to −90°. The RHP zero frequently appears in the power stage transfer functions of PWM dc-to-dc converters, as will be discussed later in this chapter.

6.1.3 Bode Plot Construction for Transfer Functions

Bode plots for transfer functions are constructed by combining Bode plots of individual multiplication factors. Techniques for the Bode plot construction are illustrated with several examples.

Examples of Bode Plot Construction

The first example considers the Bode plot for the following transfer function

$$T(s) = 10s\frac{1}{1+\frac{s}{10^2}}\frac{1}{1+\frac{s}{10^5}} \tag{6.42}$$

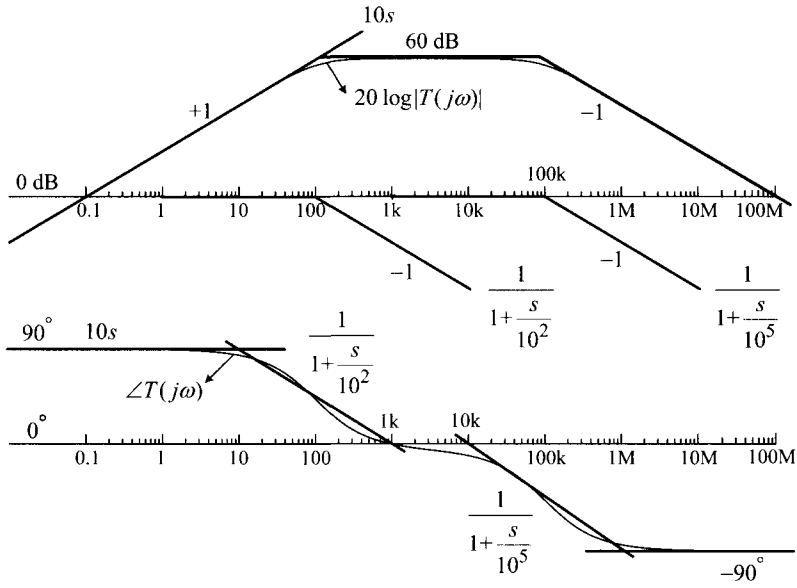


Figure 6.9 Example of Bode plot construction: $\frac{10s}{(1+s/10^2)(1+s/10^5)}$.

The magnitude and phase responses are evaluated as

$$20\log|T(j\omega)| = 20\log|10j\omega| + 20\log\left|\frac{1}{1+\frac{j\omega}{10^2}}\right| + 20\log\left|\frac{1}{1+\frac{j\omega}{10^5}}\right| \tag{6.43}$$

and

$$\angle T(j\omega) = \angle 10j\omega + \angle\frac{1}{1+\frac{j\omega}{10^2}} + \angle\frac{1}{1+\frac{j\omega}{10^5}} \tag{6.44}$$

Figure 6.9 illustrates the procedure of creating asymptotic plots for the transfer function. The magnitude plots for the multiplication factors are first drawn individually and then added together to create the composite magnitude plot for the transfer function. The magnitude plot initially ramps up with a 20 dB/dec, or +1, slope due to the single differentiation function. After passing through the 0 dB line at $\omega = 0.1$, the magnitude plot becomes flat at the first pole $\omega = 10^2$. The flat mid-band magnitude is evaluated as $20\log|10j\omega|_{\omega=10^2} = 60$ dB. The 60 dB mid-band magnitude starts declining by −20 dB/dec, or −1, slope at the second pole $\omega = 10^5$, thereby crossing the 0 dB line at $\omega = 10^8$.

The phase plot is constructed by adding the phase plots of the individual multiplication factors. The phase starts with 90° due to the single differentiation function. The 90° low-frequency phase decreases to 0° over the first pole $\omega = 10^2$. The 0°

phase reduces to the $-90°$ final phase over the second pole $\omega = 10^5$. Figure 6.9 also shows the exact Bode plots of the transfer function.

From the previous example, the general transition patterns of Bode plots can be described as follows. The Bode plot initially starts with a differentiation function, integration function, or constant. Then, the evolution of the Bode plot is changed by the poles or zeros of the transfer function.

1) A single pole ω_p decreases the magnitude slope by 20 dB/dec at the pole frequency, while causing a 90° phase lag over the frequency range $0.1\,\omega_p < \omega < 10\,\omega_p$.

2) A double pole ω_o reduces the magnitude slope by 40 dB/dec, while lagging the phase by 180° over the frequencies around ω_o.

3) A single zero ω_z boosts the magnitude slope by 20 dB/dec, while causing a 90° phase lead over the frequency range $0.1\,\omega_z < \omega < 10\,\omega_z$.

4) A double zero ω_o increases the magnitude slope by 40 dB/dec, while leading the phase by 180° over the frequencies around ω_o.

The pole or zero frequency is called the corner frequency because the magnitude asymptote shapes a corner at pole and zero frequencies by changing the ascending and descending slopes. The aforementioned evolution patterns serve as the general rules in constructing Bode plots for given transfer functions.

Now, the second example deals with the following transfer function

$$T(s) = \frac{s(s+10)}{(s+25)(s+100)} \tag{6.45}$$

The transfer function is first written in the time constant form

$$T(s) = \frac{s}{250}\frac{1+\dfrac{s}{10}}{\left(1+\dfrac{s}{25}\right)\left(1+\dfrac{s}{100}\right)} \tag{6.46}$$

The asymptotic plot is created as shown in Fig. 6.10 by applying the Bode plot construction rules. The high-frequency magnitude is found from (6.45)

$$\lim_{\omega\to\infty} |T(j\omega)| = \left|\frac{j\omega(j\omega+10)}{(j\omega+25)(j\omega+100)}\right|_{\omega=\infty} = 1 \quad \Rightarrow 0\,\text{dB} \tag{6.47}$$

while the high-frequency phase is evaluated as

$$\begin{aligned}\lim_{\omega\to\infty} \angle T(j\omega) &= \lim_{\omega\to\infty} \angle \frac{j\omega(j\omega+10)}{(j\omega+25)(j\omega+100)} \\ &= (90° + 90°) - (90° + 90°) = 0°\end{aligned} \tag{6.48}$$

By incorporating the actual frequency response characteristics near the corner fre-

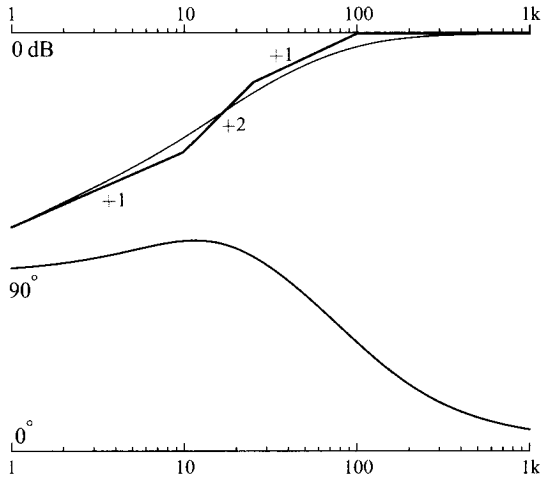


Figure 6.10 Example of Bode plot construction: $\frac{s(s+10)}{(s+25)(s+100)}$.

quencies, each asymptotic Bode plot can be modified to a smooth curve that closely resembles the exact Bode plot, as shown in Fig. 6.10.

For another example, the following transfer function is considered

$$T(s) = \frac{s}{1 + \frac{s}{0.5} + \frac{s^2}{0.1^2}} \tag{6.49}$$

whose denominator is the double pole function at $\omega_o = 0.1$ with $Q_p = 5$. Figure 6.11(a) shows the Bode plot, obtained by adding the $20 \log 5$ peaking at $\omega_o = 0.1$ to the asymptotic plot.

As an additional example, the Bode plot of the transfer function

$$T(s) = \frac{50}{s} \frac{1 + \frac{s}{800} + \frac{s^2}{200^2}}{1 + \frac{s}{400} + \frac{s^2}{100^2}} \tag{6.50}$$

can be constructed as shown in Fig. 6.11(b) by recognizing $Q_p = 4$ and $\omega_o = 100$ for the denominator, and $Q_z = 4$ and $\omega_o = 200$ for the numerator.

Non-Minimum Phase System

The dynamic system containing a right-half plane (RHP) zero or RHP pole in its transfer function is called the non-minimum phase system. To be specific, the

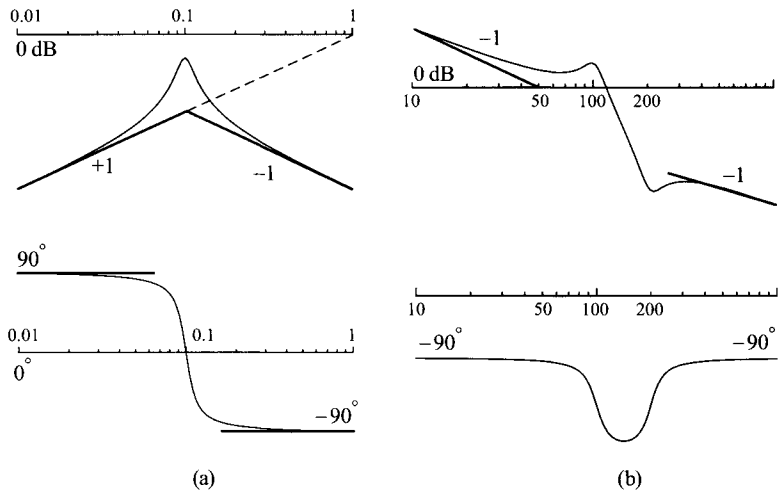


Figure 6.11 Examples of Bode plots. (a) $\frac{s}{1+s/0.5+s^2/0.1^2}$. (b) $\frac{50}{s}\frac{1+s/800+s^2/200^2}{1+s/400+s^2/100^2}$.

following transfer function

$$T(s) = \frac{1 + \dfrac{s}{\omega_z}}{1 + \dfrac{s}{Q_p\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{6.51}$$

is a regular second-order system. In contrast, the transfer function given by

$$T(s) = \frac{1 - \dfrac{s}{\omega_z}}{1 + \dfrac{s}{Q_p\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{6.52}$$

is a non-minimum phase second-order system, due to the presence of an RHP zero function in the numerator.

Figure 6.12 compares the Bode plots of the regular second-order system and the non-minimum phase second-order system with the assumption $\omega_o < \omega_z$. The magnitude plots of the two systems are identical, but the phase responses differ from each other. Due to the presence of the RHP zero at ω_z, which causes a 90° phase delay, the phase of the non-minimum phase system decreases from −180° to −270° over ω_z, resulting in the overall phase variation between 0° and −270°. On the other hand, the phase of the regular system only changes between 0° and −180°. The non-minimum phase system is named so because the phase variation is wider than that of the regular system.

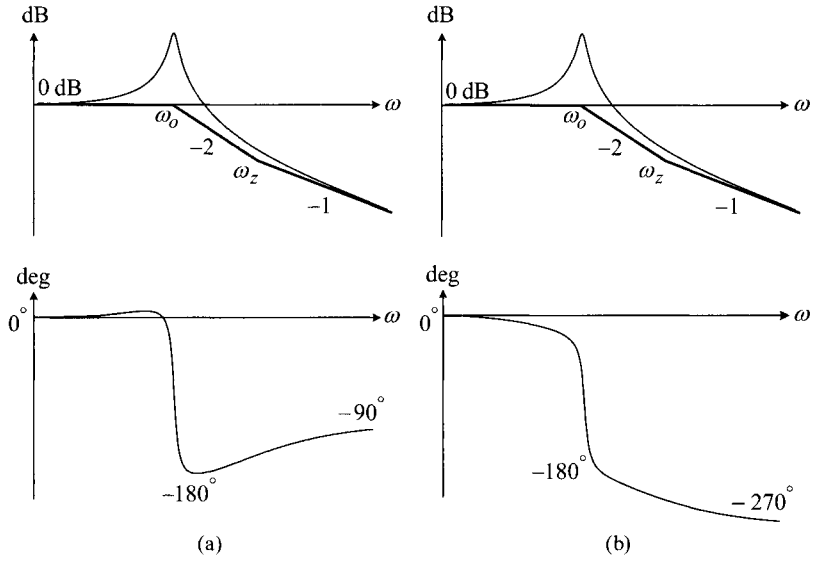


Figure 6.12 Bode plots for regular and non-minimum phase second-order systems. (a) Regular second-order system. (b) Non-minimum phase second-order system.

6.1.4 Identification of Transfer Function from Bode Plot

In many dynamic system analyses, the asymptotic plots of certain transfer functions are determined in advance and it then becomes necessary to extract analytical expressions of those transfer functions from their preexisting asymptotic plots. This task is fulfilled by taking the inverse steps of the Bode plot construction. From the given asymptotic plot, the structure of the transfer function is first determined. The transfer function is written in a time constant form which includes the leading coefficient in front. The general structure of the time constant form is given in (6.5). The leading coefficient is then calculated from the value of the low-frequency asymptote, high-frequency asymptote, 0 dB frequency, or one of the corner frequencies. This technique is frequently used in the later chapters that deal with the dynamic analysis and control design of dc-to-dc converters.

■ EXAMPLE 6.1 Identification of Transfer Function

This example illustrates the procedures of identifying the transfer function from its asymptotic plot. The first illustration considers the asymptotic plot shown in Fig. 6.13(a), where the mid-frequency asymptote is given by 20 log K_m. The

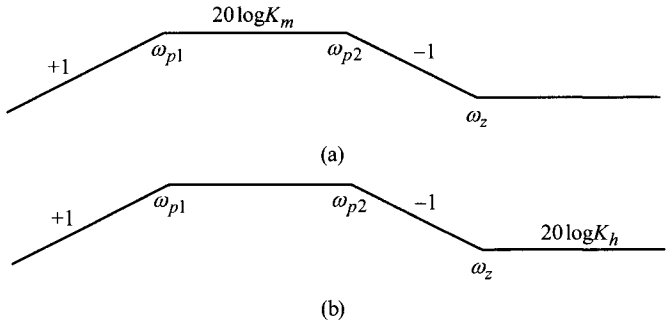


Figure 6.13 Example of asymptotic plots. (a) Case where mid-band gain is given. (b) Case where high-frequency asymptote is known.

asymptotic plot is converted into an analytic equation

$$T(s) = K_d s \frac{1 + \dfrac{s}{\omega_z}}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)} \tag{6.53}$$

by taking the inverse steps of the Bode plot construction. The mid-frequency magnitude of the asymptotic plot is determined as

$$|K_d s|_{s=j\omega_{p1}} = 20\log(K_d\,\omega_{p1}) = 20\log K_m \tag{6.54}$$

which indicates

$$K_d\,\omega_{p1} = K_m \tag{6.55}$$

The expression for the leading coefficient is now given by

$$K_d = \frac{K_m}{\omega_{p1}} \tag{6.56}$$

The second example deals with the asymptotic plot shown in Fig. 6.13(b). The expression for the transfer function is the same, but the leading coefficient K_d is different. The value for K_d is now found from the high-frequency asymptote of the transfer function. The high-frequency asymptote is evaluated from the $T(s)$ expression

$$\begin{aligned} \lim_{\omega\to\infty} |T(j\omega)| &= \left| K_d j\omega \frac{1 + \dfrac{j\omega}{\omega_z}}{\left(1 + \dfrac{j\omega}{\omega_{p1}}\right)\left(1 + \dfrac{j\omega}{\omega_{p2}}\right)} \right|_{\omega=\infty} \\ &= 20\log\left(K_d \frac{\omega_{p1}\omega_{p2}}{\omega_z}\right) \end{aligned} \tag{6.57}$$

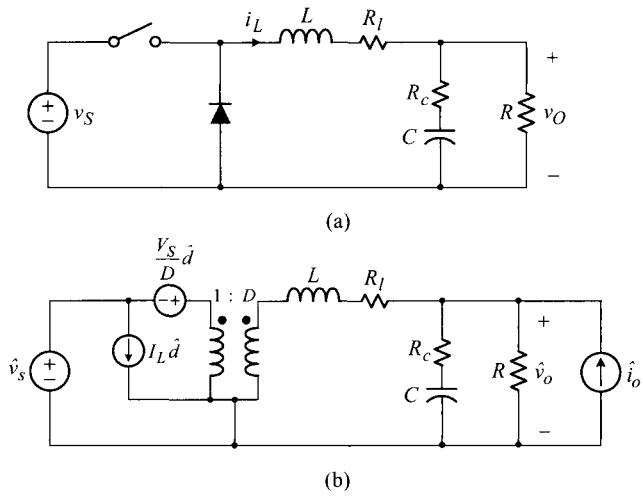


Figure 6.14 Small-signal model of buck converter. (a) Circuit diagram. (b) Small-signal model.

On the other hand, the asymptotic plot indicates that

$$|T(j\infty)| = 20 \log K_h \tag{6.58}$$

By equating (6.57) and (6.58), the leading coefficient is given by

$$K_d = K_h \frac{\omega_z}{\omega_{p1}\omega_{p2}} \tag{6.59}$$

The techniques illustrated in the previous examples will be adopted in later parts of this book. Further details about this method will be covered in Chapter 8.

6.2 POWER STAGE TRANSFER FUNCTIONS OF BUCK CONVERTER

Power stage transfer functions of PWM dc-to-dc converters can be derived from the s-domain small-signal model of power stage. The Bode plot construction techniques are then applied to the power stage transfer functions to reveal the frequency response characteristics. This section deals with the power stage transfer functions of the buck converter while succeeding sections cover the boost and buck/boost converters.

Figure 6.14(a) shows the circuit diagram of the buck converter where the parasitic resistances of the inductor and capacitor are both included. Figure 6.14(b) is the small-signal model of Fig. 6.14(a), obtained by replacing the PWM switch with its small-signal model and introducing appropriate small-signal sources. Readers may refer to Section 5.3.3 for the details about the small-signal model.

6.2.1 Input-to-Output Transfer Function

The standard circuit analysis of Fig. 6.14(b) with the condition $\hat{d}(s) = \hat{i}_o(s) = 0$ yields the input-to-output transfer function

$$G_{vs}(s) = \frac{\hat{v}_o(s)}{\hat{v}_s(s)} = K_{vs} \frac{1 + \dfrac{s}{\omega_{esr}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{6.60}$$

with

$$K_{vs} = \frac{D}{1 + \dfrac{R_l}{R}} \approx D \tag{6.61}$$

and

$$\omega_{esr} = \frac{1}{CR_c} \tag{6.62}$$

The ω_{esr}, appearing in the numerator due to the equivalent series resistance (esr) of the output capacitor, is named the *esr zero*. The power stage double pole ω_o and the damping ratio Q are given by

$$\omega_o = \sqrt{\frac{1}{LC}\frac{R + R_l}{R + R_c}} \approx \frac{1}{\sqrt{LC}} \tag{6.63}$$

and

$$Q = \frac{1}{\omega_o} \frac{R + R_l}{L + C(R_l R_c + R_l R + R_c R)} \approx R\sqrt{\frac{C}{L}} \tag{6.64}$$

The approximations in (6.61), (6.63), and (6.64) become accurate with the conditions $R \gg R_l$ and $R \gg R_c$.

When the expression (6.60) is compared with the $G_{vs}(s)$ of an ideal buck converter, given by (5.65) in Example 5.7, the effects of the parasitic resistances can be seen. Most notably, the esr of the output capacitor introduces the esr zero. The effects of the esr zero on the frequency response will be described shortly.

While the parasitic resistances also alter the expressions for the pole frequency and damping ratio, these changes are usually insignificant. When the parasitic resistances are sufficiently small, the pole frequency and damping ratio can be approximated to those of the ideal buck converter, as shown in (6.63) and (6.64).

Figure 6.15 shows the asymptotic plot of $|G_{vs}|$ and $\angle G_{vs}$, created by following the Bode plot construction rules with assumptions $\omega_o \ll \omega_{esr}$ and $Q > 0.5$. The low-pass filter characteristics, originating from the circuit structure and operational principle of the buck converter, are apparent in Fig. 6.15. As a typical second-order low pass filter, the flat low-frequency asymptote of $|G_{vs}|$ falls off at the double pole frequency ω_o with a -40 dB/dec, or -2, slope. At the esr zero ω_{esr}, the -40 dB/dec slope is changed to the -20 dB/dec, or -1, slope. The low-frequency asymptote of $|G_{vs}|$ is the voltage gain of the buck converter: $|G_{vs}(j0)| = 20 \log K_{vs} \approx 20 \log D$.

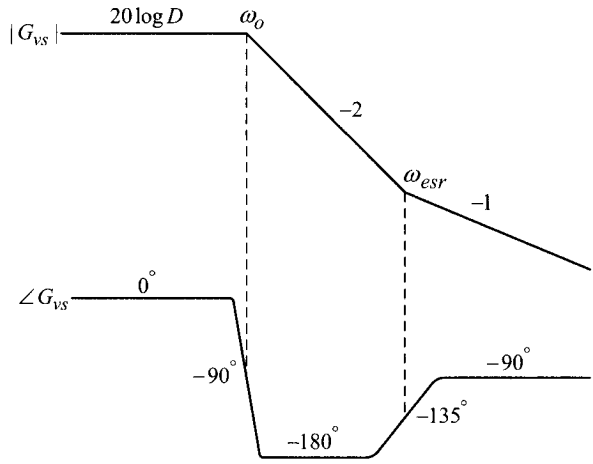


Figure 6.15 Asymptotic plot of input-to-output transfer function.

The $\angle G_{vs}$ starts with 0° at low frequencies, drops down to −180° in the mid-frequency band, and finally converges to −90° at high frequencies. The esr zero in effect provides a 90° phase boost for $\angle G_{vs}$.

The frequency response of the input-to-output transfer function should be interpreted based on the definition discussed in Section 5.4. The frequency response only describes the ac component of the circuit variables, as such, the dc component and switching ripple component should be considered separately.

■ EXAMPLE 6.2 Input-to-Output Transfer Function

This example shows the input-to-output transfer function of a buck converter and illustrates its relationship with time-domain circuit variables. Consider a buck converter operating with $V_S = 16$ V, $L = 40\,\mu$F, $R_l = 0.1\,\Omega$, $C = 470\,\mu$F, $R_c = 0.05\,\Omega$, $R = 1\,\Omega$, $f_s = 20$ kHz, and $D = 0.25$. The input-to-output transfer function of the converter is given by

$$G_{vs}(s) \approx K_{vs} \frac{1 + \dfrac{s}{\omega_{esr}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{6.65}$$

with

$$K_{vs} = D = 0.25 \quad \Rightarrow -12\text{ dB}$$

and

$$Q = R\sqrt{\frac{C}{L}} = 1\sqrt{\frac{470 \times 10^{-6}}{40 \times 10^{-6}}} = 3.43$$

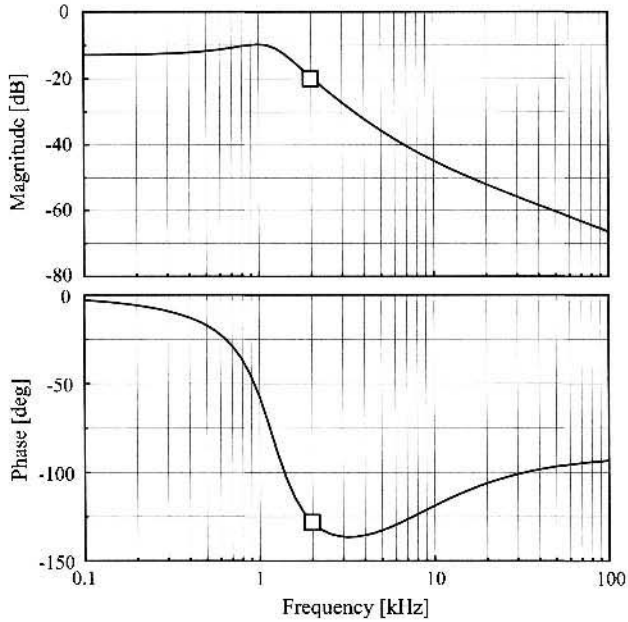


Figure 6.16 Input-to-output transfer function of buck converter.

and

$$\omega_o = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{40 \times 10^{-6}\, 470 \times 10^{-6}}} = 2\pi \cdot 1.16 \times 10^3 \text{ rad/s}$$

and

$$\omega_{esr} = \frac{1}{CR_c} = \frac{1}{470 \times 10^{-6}\, 0.05} = 2\pi \cdot 6.77 \times 10^3 \text{ rad/s}$$

Figure 6.16 shows the input-to-output transfer function obtained from the PSpice® simulation using the s-domain small-signal model. The magnitude and phase responses at $f = 2$ kHz or $\omega = 2\pi \cdot 2 \times 10^3$ rad/s, highlighted with a rectangle in Fig. 6.16, are used to illustrate the implication of the frequency response. When a 2 kHz sinusoid is added to the dc input voltage, it will propagate to the output with about a 20 dB attenuation in magnitude and 130° delay in phase. The output voltage is given by the sum of the dc value, switching ripple, and sinusoidal component originating from the input sinusoid. To verify this prediction, the time-domain simulation is performed with

$$v_S(t) = 16 + 0.5 \sin 2\pi \cdot 2 \times 10^3 t$$

Based on the converter operation and prediction of $G_{vs}(j2\pi \cdot 2 \times 10^3)$, the output voltage will be

$$v_O(t) = 0.25 \cdot 16 + 0.1 \cdot 0.5 \sin(2\pi \cdot 2 \times 10^3 t - 130°) + \text{switching ripple}$$

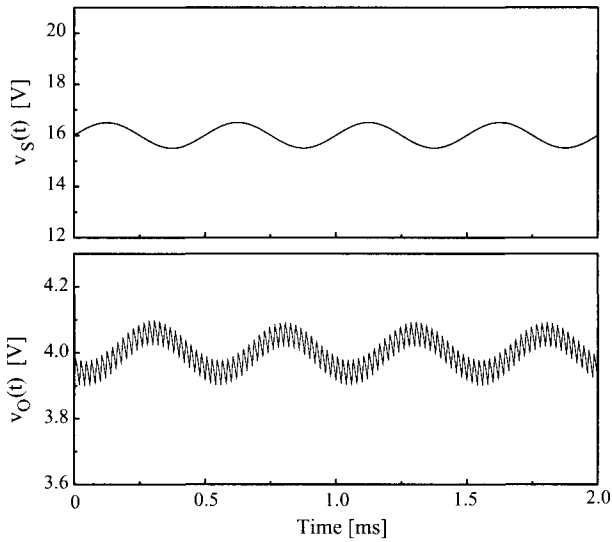


Figure 6.17 Time-domain response of input voltage v_S and output voltage v_O of buck converter.

$$= 4 + 0.05\sin(2\pi \cdot 2 \times 10^3 t - 130^\circ) + \text{switching ripple}$$

Figure 6.17 shows the simulation results. When the switching ripple is ignored, the output voltage exhibits a 0.1 V sinusoidal swing as predicted from the input-to-output transfer function.

6.2.2 Duty Ratio-to-Output Transfer Function

The duty ratio-to-output transfer function is evaluated from Fig. 6.14(b) with the condition $\hat{v}_s(s) = \hat{\imath}_o(s) = 0$

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = K_{vd}\frac{1 + \dfrac{s}{\omega_{esr}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{6.66}$$

with

$$K_{vd} = \frac{V_S}{1 + \dfrac{R_l}{R}} \approx V_S \tag{6.67}$$

Figure 6.18 shows a typical $|G_{vd}|$ in comparison with $|G_{vs}|$. While the structure is identical to $|G_{vs}|$, the low-frequency asymptote of the transfer function, $|G_{vd}(j0)| \approx 20\log V_S$, can be significantly larger than $|G_{vs}(j0)| \approx 20\log D$.

Because $G_{vd}(s)$ is the transfer function from the duty ratio to output voltage, the transfer function is located in the middle of the voltage feedback path. Accordingly,

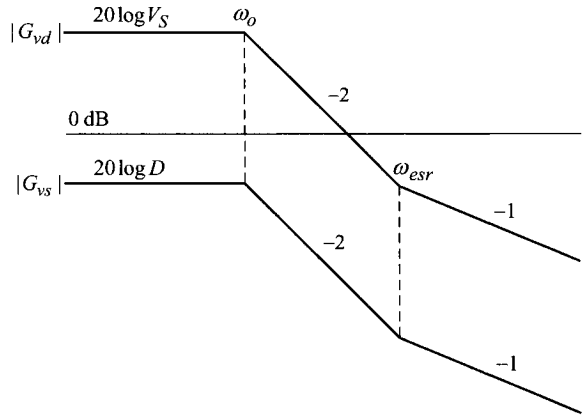


Figure 6.18 Asymptotic plot of input-to-output transfer function and duty ratio-to-output transfer function.

$G_{vd}(s)$ directly influences stability and performance of the closed-loop controlled converter. Thus, $G_{vd}(s)$ is critical in determining the structure and components of the voltage feedback circuit, as will be demonstrated in Chapter 8.

■ EXAMPLE 6.3 Duty Ratio-to-Output Transfer Function

This example shows the duty ratio-to-output transfer function of the buck converter introduced in Example 6.2. The implication of the $G_{vd}(s)$ on the time-domain circuit waveforms is also illustrated. The duty ratio-to-output transfer function is given by

$$G_{vd}(s) \approx K_{vd} \frac{1 + \dfrac{s}{\omega_{esr}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{6.68}$$

with $K_{vd} = V_S = 16 \Rightarrow 24$ dB. Other parameters are the same as those of Example 6.2. Figure 6.19 shows the simulation of $G_{vd}(s)$. Similar to Example 6.2, the time-domain relationship between the duty ratio and output voltage can be predicted from Fig. 6.19. As highlighted with a rectangle in Fig. 6.19, the 5 kHz sinusoidal variation in the duty ratio will propagate to the output voltage with the same magnitude but with about 135° phase delay. When the switch drive signal is modulated to produce the following continuous duty ratio

$$d(t) = 0.25 + 0.05 \sin 2\pi \cdot 5 \times 10^3 t$$

the output voltage will be

$$\begin{aligned} v_O(t) &= 0.25 \cdot 16 + 1 \cdot 0.05 \sin(2\pi \cdot 5 \times 10^3 t - 135°) + \text{switching ripple} \\ &= 4 + 0.05 \sin(2\pi \cdot 5 \times 10^3 t - 135°) + \text{switching ripple} \end{aligned}$$

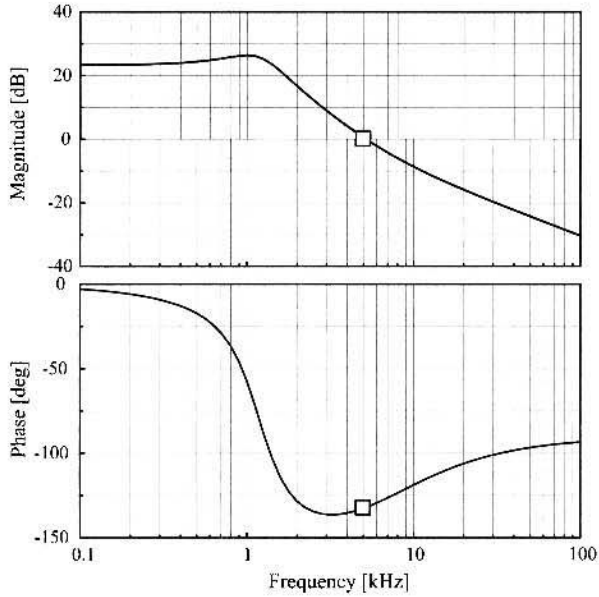


Figure 6.19 Duty ratio-to-output transfer function of buck converter.

Figure 6.20 shows the time-domain response of the converter, simulated with the aforementioned operational conditions. It can be seen that the switch drive signal $q(t)$ is modulated to produce a 5 kHz sinusoidal variation in $d(t)$ around the steady-state duty ratio. When the switching ripple is neglected, the magnitude of the sinusoidal variation in the output voltage is approximately the same as that of the duty ratio, as predicted from the duty ratio-to-output transfer function.

6.2.3 Load Current-to-Output Transfer Function

The load current-to-output voltage transfer function is derived from Fig. 6.14(b) with the condition $\hat{v}_s(s) = \hat{d}(s) = 0$

$$Z_p(s) = \frac{\hat{v}_o(s)}{\hat{i}_o(s)} = R \parallel R_l \frac{\left(1 + \frac{s}{\omega_z}\right)\left(1 + \frac{s}{\omega_{esr}}\right)}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \approx R_l \frac{\left(1 + \frac{s}{\omega_z}\right)\left(1 + \frac{s}{\omega_{esr}}\right)}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \tag{6.69}$$

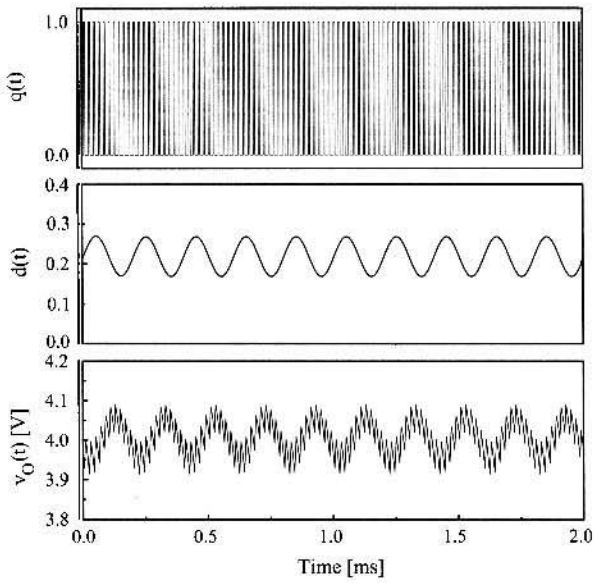


Figure 6.20 Time-domain response of switch drive signal $q(t)$, continuous duty ratio $d(t)$, and output voltage v_O.

with

$$\omega_z = \frac{R_l}{L} \tag{6.70}$$

In addition to ω_{esr}, the transfer function has another zero ω_z, created by the esr of the inductor. While ω_{esr} appears at high frequencies, ω_z is usually located at lower frequencies. Accordingly, the low-frequency characteristics of the transfer function are mainly influenced by the esr of the inductor.

Figure 6.21 shows the asymptotic plots for $|Z_p|$ and $\angle Z_p$. The low-frequency asymptote of $|Z_p|$ is the parallel connection of the load resistor and esr of the inductor, which can be practically approximated to $|Z_p(j0)| = 20\log R \parallel R_l \approx 20\log R_l$. The high-frequency asymptote can be found from the small-signal circuit model in Fig. 6.14(b). At high frequencies, the inductance behaves open-circuited and the capacitance presents very low impedance. Thus, the high-frequency asymptote is the parallel combination of the load resistor and esr of the output capacitor, which can be approximated to $|Z_p(j\infty)| = 20\log R \parallel R_c \approx 20\log R_c$ for most cases.

6.3 POWER STAGE TRANSFER FUNCTIONS OF BOOST CONVERTER

Figure 6.22(a) shows the power stage of the boost converter and Fig. 6.22(b) depicts its small-signal model. Details about the small-signal model were presented in Section 5.3.3.

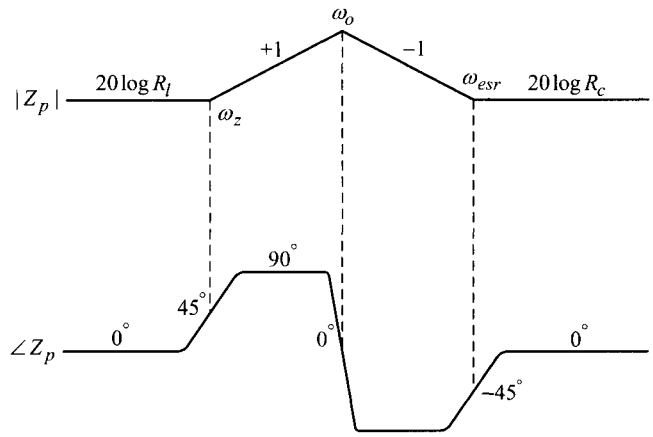


Figure 6.21 Asymptotic plot of load current-to-output transfer function.

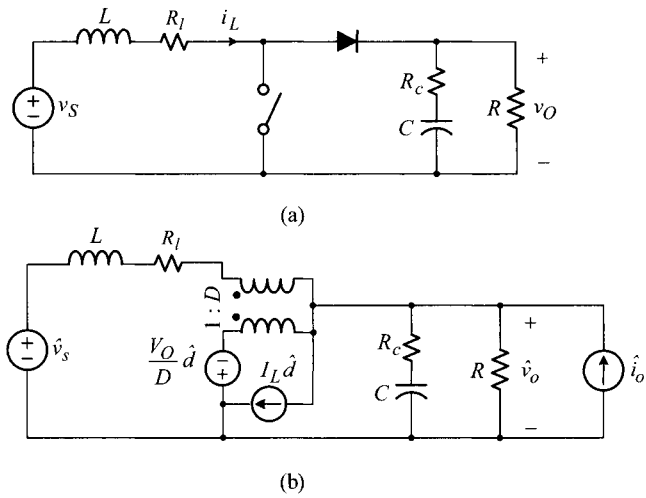


Figure 6.22 Small-signal model of boost converter. (a) Circuit diagram. (b) Small-signal model.

6.3.1 Input-to-Output Transfer Function

The input-to-output transfer function is derived from Fig. 6.22(b) with the condition $\hat{d}(s) = \hat{i}_o(s) = 0$

$$G_{vs}(s) = K_{vs}\frac{1 + \dfrac{s}{\omega_{esr}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{6.71}$$

with

$$K_{vs} = \frac{1}{D'\left(1+\dfrac{R_l}{RD'^2}\right)} \approx \frac{1}{D'} \tag{6.72}$$

$$\omega_{esr} = \frac{1}{CR_c} \tag{6.73}$$

$$\omega_o = \sqrt{\frac{1}{LC}\frac{RD'^2+R_l}{R+R_c}} \approx \frac{D'}{\sqrt{LC}} = \frac{1}{\sqrt{L_eC}} \tag{6.74}$$

$$Q = \frac{1}{\omega_o}\frac{RD'^2+R_l}{L+C(R_lR_c+R_lR+R_cRD'^2)} \approx R\sqrt{\frac{C}{L_e}} \tag{6.75}$$

with

$$L_e = \frac{L}{D'^2} \tag{6.76}$$

and

$$D' = 1 - D \tag{6.77}$$

An interesting property of the boost converter is observed from the input-to-output transfer function. The transfer function shows the low-pass filter characteristics, as is the case with the buck converter. However, the inductive parameter appears as $L_e = L/D'^2$ in the double pole frequency ω_o and damping ratio Q, instead of the original inductance L. This is attributed to the fact that the inductor is not directly connected to the output capacitor but separated by the PWM switch. The inductance located at one side of the PWM switch should be altered when the filter transfer function is evaluated from the other side. The transfer function expression also indicates that the pole frequency and damping ratio depend on the duty ratio of the converter. Thus, the power stage dynamics will be changed when the duty ratio of the converter varies.

The low-frequency value of the transfer function is approximated to $|G_{vs}(j0)| = 20\log K_{vs} \approx 20\log(1/D')$, which corresponds to the voltage gain of an ideal boost converter. The asymptotic plots for $|G_{vs}|$ and $\angle G_{vs}$ are essentially the same as those of the buck converter case.

6.3.2 Duty Ratio-to-Output Transfer Function and RHP Zero

With the condition $\hat{v}_s(s) = \hat{\imath}_o(s) = 0$, the duty ratio-to-output transfer function is derived as

$$G_{vd}(s) = K_{vd}\frac{\left(1-\dfrac{s}{\omega_{rhp}}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}} \tag{6.78}$$

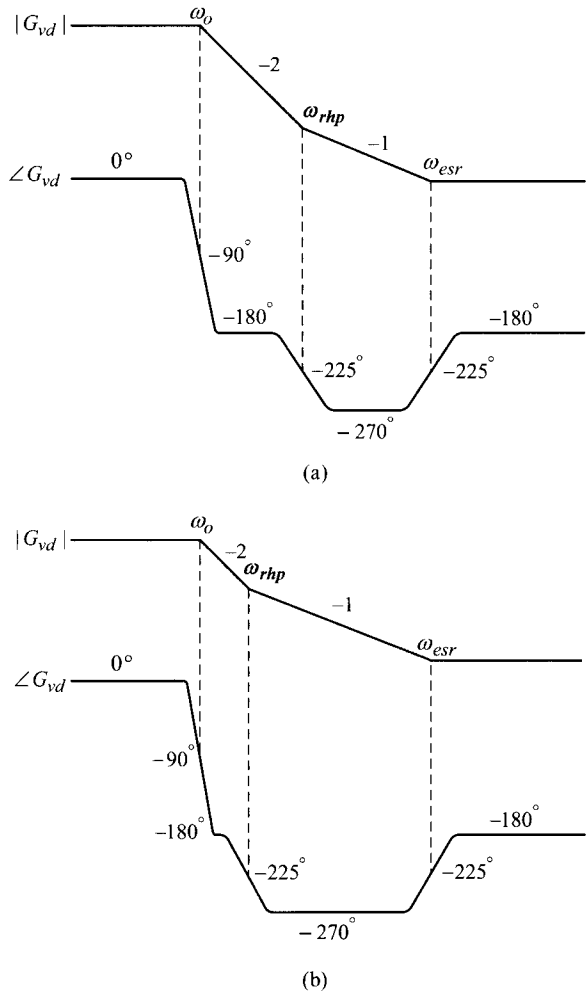


Figure 6.23 Effects of ω_{rhp} on duty ratio-to-output transfer function. (a) Case with nominal duty ratio. (b) Case with increased duty ratio.

with

$$K_{vd} = \frac{V_S}{D'^2} \frac{1 - \dfrac{R_l}{RD'^2}}{1 + \dfrac{R_l}{RD'^2}} \approx \frac{V_S}{D'^2} \tag{6.79}$$

and

$$\omega_{rhp} = \frac{D'^2 R}{L}\left(1 - \frac{R_l}{RD'^2}\right) \approx \frac{D'^2 R}{L} = \frac{R}{L_e} \tag{6.80}$$

with $L_e = L/D'^2$.

The most distinctive feature of the transfer function is the presence of a right-half plane (RHP) zero, ω_{rhp}, in the numerator of (6.78). The zero, $s = \omega_{rhp}$, is located in the right-hand side of s-plane and the subscript *rhp* is used to signify this fact. The expression for the RHP zero, $\omega_{rhp} = (1-D)^2R/L$, indicates that the zero frequency is affected by the duty ratio. Accordingly, the zero frequency will move around when the duty ratio is changed; for this reason, ω_{rhp} is called the *moving* RHP zero.

The impacts of the moving RHP zero, ω_{rhp}, on the transfer function are explained in Fig. 6.23. As far as the magnitude of the transfer function is concerned, ω_{rhp} has the same effect as that of a regular zero. However, ω_{rhp} causes a 90° phase delay to $\angle G_{vd}$, in contrast to the 90° phase boost in the case of a regular zero. Thus, ω_{rhp} increases the slope of $|G_{vd}|$ by 20 dB/dec, while bringing down $\angle G_{vd}$ by 90°.

Typical asymptotic plots for $|G_{vd}|$ and $\angle G_{vd}$ are shown in Fig. 6.23(a), with the assumption $\omega_o \ll \omega_{rhp} \ll \omega_{esr}$. At frequencies beyond ω_o, $\angle G_{vd}$ mainly stays below −180°, with a −270° basin in the frequency range of $\omega_{rhp} < \omega < \omega_{esr}$. When the duty ratio is increased from the previous value, ω_{rhp} shifts towards lower frequencies, resulting in the asymptotic plots shown in Fig. 6.23(b). For this case, $\angle G_{vd}$ would stay at the −270° basin for a wider frequency range. As will be detailed in Section 8.4.7, these phase characteristics present considerable difficulties to the design of the voltage feedback circuit. Accordingly, the control design of the boost converter is more challenging than that of the buck converter. The impact of ω_{rhp} on the control design and converter performance will be covered in later chapters.

■ EXAMPLE 6.4 Duty Ratio-to-Output Transfer Function

In order to confirm the existence of the RHP zero, this example derives the duty ratio-to-output transfer function of the boost converter. Figure 6.24(a) shows the small-signal model of an ideal boost converter. This model is derived from Fig. 6.22(b) for the evaluation of $G_{vd}(s)$ with the conditions $\hat{v}_s(s) = \hat{i}_o(s) = 0$ and $R_l = R_c = 0$. Figure 6.24(a) is modified to Fig. 6.24(b) by replacing the ideal transformer with a pair of voltage source v_T and current source i_T

$$v_T = -\left(\hat{v}_o + \frac{V_O}{D}\hat{d}\right)D = -(D\hat{v}_o + V_O\hat{d}) \tag{6.81}$$

$$i_T = D\hat{i}_L \tag{6.82}$$

The inductor current $\hat{i}_L$ is then given by

$$\hat{i}_L = -\left(\frac{\hat{v}_o + v_T}{sL}\right) = \frac{-(1-D)\hat{v}_o + V_O\hat{d}}{sL} \tag{6.83}$$

The current coming out of the passive terminal of the PWM switch, $\hat{i}_p$ in Fig. 6.24(b), is given by

$$\hat{i}_p = \hat{i}_L - i_T - I_L\hat{d} = \hat{i}_L - D\hat{i}_L - I_L\hat{d} = (1-D)\hat{i}_L - I_L\hat{d} \tag{6.84}$$

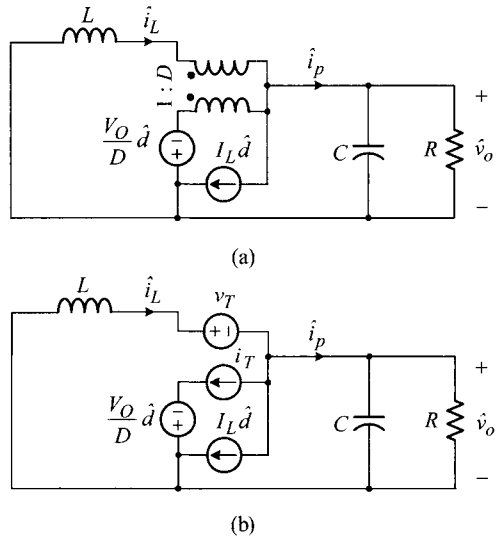


Figure 6.24 Small-signal model of ideal boost converter. (a) Original model. (b) Modified model.

with $I_L = V_O/((1 - D)R)$. The output voltage $\hat{v}_o$ is now determined as

$$\hat{v}_o = \hat{i}_p \left(\frac{1}{sC} \parallel R \right) \tag{6.85}$$

By substituting (6.84) and (6.83) into (6.85), it follows that

$$\hat{v}_o = \left((1 - D) \frac{-(1 - D)\hat{v}_o + V_O\hat{d}}{sL} - I_L\hat{d} \right) \frac{R}{1 + sCR} \tag{6.86}$$

which can be arranged in a transfer function form

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{V_O}{1 - D} \frac{1 - \dfrac{sL}{(1 - D)^2 R}}{1 + \dfrac{sL}{(1 - D)^2 R} + \dfrac{s^2 LC}{(1 - D)^2}} \tag{6.87}$$

The presence of the RHP zero, $\omega_{rhp} = (1 - D)^2 R/L = R/L_e$, is explicit in (6.87). While the derivation becomes somewhat complicated when the parasitic resistances are included, the same procedure leads to the equation (6.78).

■ EXAMPLE 6.5 Duty Ratio-to-Output Transfer Function

This example shows the duty ratio-to-output transfer function of a boost converter. The operational conditions of the boost converter are $V_S = 12$ V,

$L = 800\ \mu\text{H}$, $R_l = 0.01\ \Omega$, $C = 1000\ \mu\text{F}$, $R_c = 0.05\ \Omega$, $R = 2\ \Omega$, $f_s = 10$ kHz, and $D = 0.25$. The duty ratio-to-output transfer function is given by

$$G_{vd}(s) \approx K_{vd} \frac{\left(1 - \frac{s}{\omega_{rhp}}\right)\left(1 + \frac{s}{\omega_{esr}}\right)}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \tag{6.88}$$

with

$$\begin{aligned}
K_{vd} &= \frac{V_S}{(1-D)^2} = \frac{12}{(1-0.25)^2} = 21.3 \quad \Rightarrow 26.6\ \text{dB} \\
\omega_o &= \sqrt{\frac{(1-D)^2}{LC}} = \sqrt{\frac{(1-0.25)^2}{800 \times 10^{-6}\, 1000 \times 10^{-6}}} \\
&= 2\pi \cdot 133\ \text{rad/s} \\
Q &= R\sqrt{\frac{(1-D)^2 C}{L}} = 2\sqrt{\frac{(1-0.25)^2 1000 \times 10^{-6}}{800 \times 10^{-6}}} = 1.68 \\
\omega_{rhp} &= \frac{(1-D)^2}{L} R = \frac{(1-0.25)^2}{800 \times 10^{-6}} 2 \\
&= 2\pi \cdot 224\ \text{rad/s} \\
\omega_{esr} &= \frac{1}{CR_c} = \frac{1}{1000 \times 10^{-6}\, 0.05} = 2\pi \cdot 3.18 \times 10^3\ \text{rad/s}
\end{aligned}$$

Figure 6.25 shows the duty ratio-to-output transfer function obtained from PSpice® simulations using Fig. 6.22(b). The impact of the RHP zero at $\omega_{rhp} = 2\pi \cdot 224$ rad/s is clearly seen in the Bode plot. In particular, the phase remains lower than $-200°$ after mid-frequencies. As will be demonstrated in Section 8.4.7, these phase characteristics complicate the control design and hinder the boost converter from acceptable closed-loop performance.

6.3.3 Load Current-to-Output Transfer Function

The load current-to-output transfer function is evaluated as

$$Z_p(s) = K_p \frac{\left(1 + \frac{s}{\omega_z}\right)\left(1 + \frac{s}{\omega_{esr}}\right)}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \tag{6.89}$$

with

$$K_p = R \parallel \frac{R_l}{(1-D)^2} \approx \frac{R_l}{(1-D)^2} \tag{6.90}$$

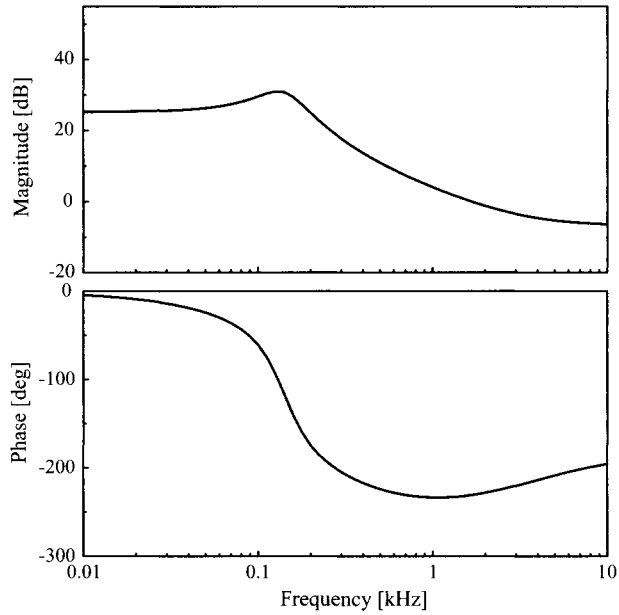


Figure 6.25 Duty ratio-to-output transfer function of boost converter.

and

$$\omega_z = \frac{R_l}{L} \tag{6.91}$$

The asymptotic plots for $|Z_p|$ and $\angle Z_p$ are the same as those of the buck converter, except for the low-frequency magnitude of Z_p: $|Z_p(0)| = 20\log(R_l/(1-D)^2)$.

6.3.4 Physical Origin of RHP Zero

As the most salient feature, the boost converter has an RHP zero in its duty ratio-to-output transfer function. While the direct evaluation of the transfer function led to the expression of the RHP zero, the existence of the RHP zero can also be confirmed from the operational principle of the boost converter. For this purpose, it is necessary to investigate the time-domain response of the system with an RHP zero in its transfer function – this type of system was previously referred to as the non-minimum phase system. To be specific, assume the following second-order equation as the transfer function of a non-minimum phase system

$$\frac{v_o(s)}{v_s(s)} = T(s) = \frac{1 - \dfrac{s}{\omega_z}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{6.92}$$

The unit step input response of the system is given by

$$v_O(t) = \mathcal{L}^{-1}(v_s(s)T(s)) = \mathcal{L}^{-1}\left(\frac{1}{s}\frac{1-\frac{s}{\omega_z}}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}}\right) \tag{6.93}$$

using the fact $v_s(s) = 1/s$ for the unit step input. The above equation is split into two parts

$$\begin{aligned} v_O(t) &= \mathcal{L}^{-1}\left(\frac{1}{s}\frac{1}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}}\right) \\ &- \frac{1}{\omega_z}\mathcal{L}^{-1}\left(s\left(\frac{1}{s}\frac{1}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}}\right)\right) \end{aligned} \tag{6.94}$$

where $\mathcal{L}^{-1}$ denotes the inverse Laplace transform operation.

By noting that the multiplication with s in s-domain corresponds to the derivative operation in time-domain, the expression (6.94) is written as

$$v_O(t) = \tilde{v}_O(t) - \frac{1}{\omega_z}\frac{d\tilde{v}_O(t)}{dt} \tag{6.95}$$

with

$$\tilde{v}_O(t) = \mathcal{L}^{-1}\left(\frac{1}{s}\frac{1}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}}\right) \tag{6.96}$$

The transient response is expressed as the sum of two terms. The first term is a transient waveform given by (6.96). The second term is generated by taking the derivative of the first term and multiplying it by the negative inverse of the RHP zero frequency. Figure 6.26 illustrates the construction of v_O based on (6.95). As shown in this figure, v_O dips into the negative direction before it proceeds towards the positive direction. As the RHP zero frequency, ω_z, moves closer to the origin, the dip becomes deeper. This initial dip is the distinctive transitional behavior of a non-minimum phase system and thus can be used as a criterion to judge the existence of the RHP zero.

The presence of an RHP zero in the duty ratio-to-output transfer function can be deduced from the transient waveforms of the boost converter. Figure 6.27 illustrates the circuit waveforms of a boost converter experiencing a step increase in its duty

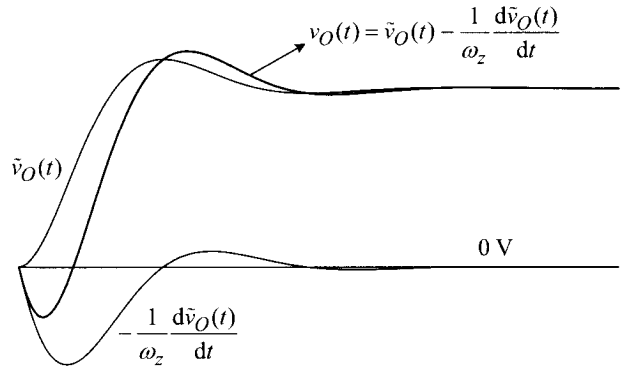


Figure 6.26 Unit step response of non-minimum phase system.

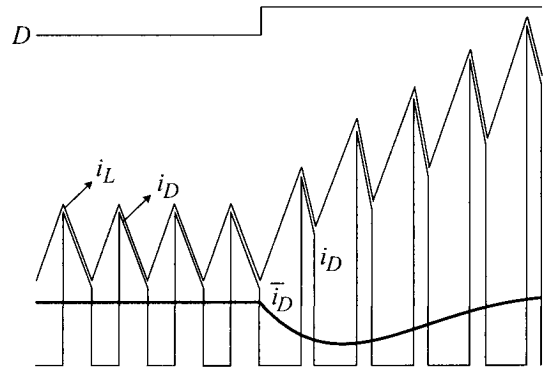


Figure 6.27 Transient response of boost converter with step increase in duty ratio.

ratio. Although the duty ratio is instantly increased, the inductor current slowly rises towards the final value based on the power stage dynamics. The diode current i_D, which corresponds to the off-time inductor current, gradually increases in its peak value but abruptly decreases in width. Accordingly, the moving average of the diode current, $\bar{i}_D$, initially droops before the inductor current becomes sufficiently large, as illustrated in Fig. 6.27.

The droop in $\bar{i}_D$ in turn causes the transitional undershoot to the output voltage at the beginning of the transition period, because the output voltage is proportional to the moving average of the diode current, $\bar{i}_D$. This validates the presence of an RHP zero in the duty ratio-to-output transfer function. This phenomenon commonly occurs in all the PWM converters in which the load current is supported by the diode current, such as the boost converter, buck/boost converter, and all isolated converters derived from these two converters.

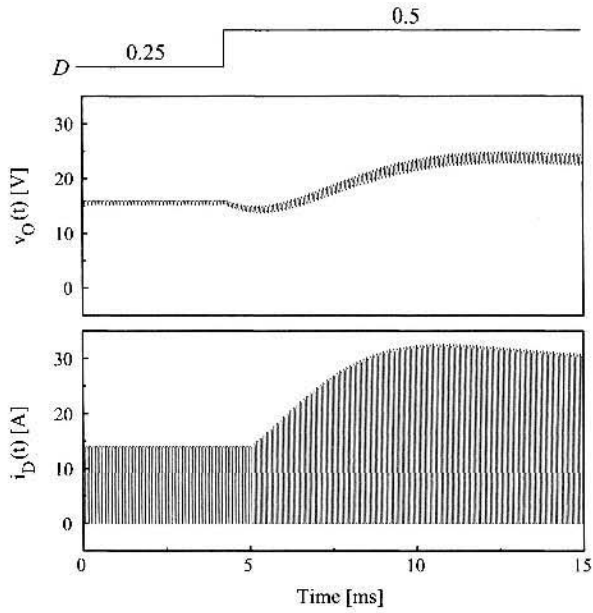


Figure 6.28 Transient waveform of output voltage v_O and diode current i_D of boost converter.

■ EXAMPLE 6.6 Transient Response of Boost Converter

The transitional behavior of a boost converter, illustrated in Fig. 6.27, is verified by time-domain simulations. Figure 6.28 shows the transient response of the boost converter introduced in Example 6.5. The boost converter has an RHP zero at $\omega_{rhp} = 2\pi \cdot 224$ rad/s. The duty ratio of the boost converter undergoes a step increase from $D = 0.25$ to $D = 0.5$ at $t = 5$ ms. As shown in Fig. 6.28, the output voltage v_O reveals an initial droop before it proceeds towards a new steady-state value, thereby verifying the existence of the RHP zero. Figure 6.28 also shows the diode current i_D during the transient period. The abrupt decrease in the width of the diode current is responsible for the initial droop in the output voltage.

6.4 POWER STAGE TRANSFER FUNCTIONS OF BUCK/BOOST CONVERTER

Figure 6.29(a) depicts the power stage of the buck/boost converter and Fig. 6.29(b) is the small-signal model obtained by adopting the PWM switch model. Section 5.3.3 presented the details about the small-signal model of the buck/boost converter. With

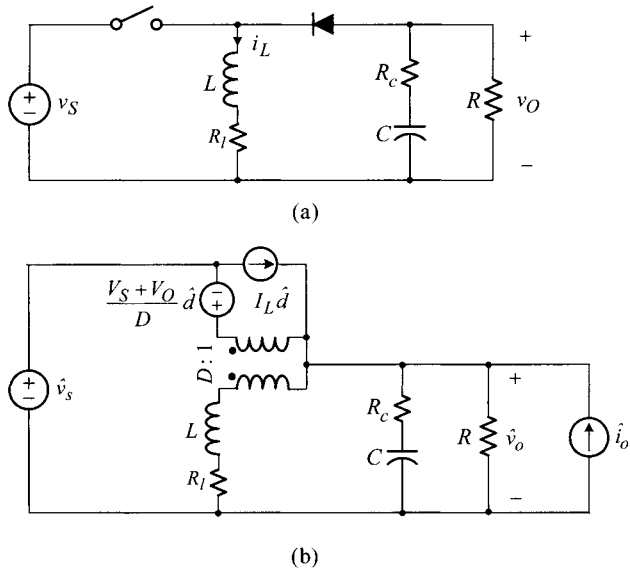


Figure 6.29 Small-signal model of buck/boost converter. (a) Circuit diagram. (b) Small-signal.

the condition $\hat{d}(s) = \hat{i}_o(s) = 0$, the input-to-output transfer function is derived as

$$G_{vs}(s) = K_{vs}\frac{1 + \dfrac{s}{\omega_{esr}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{6.97}$$

with

$$K_{vs} = \frac{D}{D'\left(1 + \dfrac{R_l}{RD'^2}\right)} \approx \frac{D}{D'} \tag{6.98}$$

$$\omega_{esr} = \frac{1}{CR_c} \tag{6.99}$$

$$\omega_o = \sqrt{\frac{1}{LC}\frac{RD'^2 + R_l}{R + R_c}} \approx \frac{D'}{\sqrt{LC}} = \frac{1}{\sqrt{L_eC}} \tag{6.100}$$

$$Q = \frac{1}{\omega_o}\frac{RD'^2 + R_l}{L + C(R_lR_c + R_lR + R_cRD'^2)} \approx R\sqrt{\frac{C}{L_e}} \tag{6.101}$$

with

$$L_e = \frac{L}{D'^2} \tag{6.102}$$

The low-frequency value of the transfer function is the voltage gain of the ideal buck/boost converter: $|G_{vs}(j0)| = 20\log K_{vs} \approx 20\log(D/D')$.

The duty ratio-to-output transfer function is given by

$$G_{vd}(s) = K_{vd}\frac{\left(1-\frac{s}{\omega_{rhp}}\right)\left(1+\frac{s}{\omega_{esr}}\right)}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \tag{6.103}$$

with

$$K_{vd} = \frac{V_S}{D'^2}\frac{1-\frac{R_l D}{RD'^2}}{1+\frac{R_l}{RD'^2}} \approx \frac{V_S}{D'^2} \tag{6.104}$$

and

$$\omega_{rhp} = \frac{D'^2 R}{DL}\left(1-\frac{R_l D}{RD'^2}\right) \approx \frac{D'^2 R}{DL} = \frac{R}{DL_e} \tag{6.105}$$

with $L_e = L/D'^2$. As expected from the circuit structure and operational principle of the converter, the transfer function has a moving RHP zero, ω_{rhp}, as is the case with the boost converter.

Finally, the load current-to-output transfer function is derived as

$$Z_p(s) = K_p\frac{\left(1+\frac{s}{\omega_z}\right)\left(1+\frac{s}{\omega_{esr}}\right)}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \tag{6.106}$$

with

$$K_p = R \parallel \frac{R_l}{D'^2} \approx \frac{R_l}{D'^2} \tag{6.107}$$

and

$$\omega_z = \frac{R_l}{L} \tag{6.108}$$

Asymptotic plots for the power stage transfer functions of the buck/boost converter are shown in Fig. 6.30.

6.5 EMPIRICAL METHODS FOR SMALL-SIGNAL ANALYSIS

In addition to the analytical method discussed in the previous sections, there are empirical approaches to investigating the frequency response of the converter. These empirical methods can be employed as a means of verifying theoretical predictions or as a substitute for analytical analyses.

Figure 6.31 shows an empirical construction to investigate the duty ratio-to-output transfer function. When the small-signal source $\hat{v}_p$ is *not* excited, a fixed dc voltage

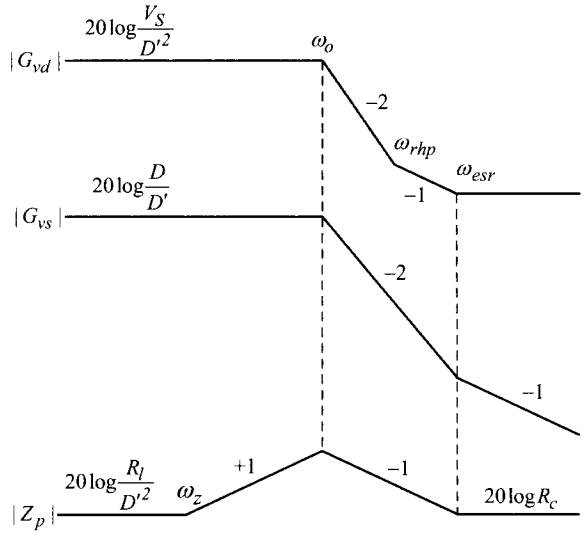


Figure 6.30 Asymptotic plots for transfer functions of buck/boost converter.

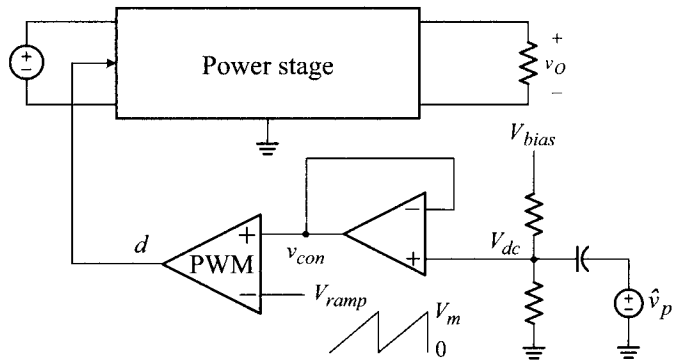


Figure 6.31 Experimental set-up for duty ratio-to-output transfer function measurement.

V_{dc} is applied as the control voltage v_{con} to the PWM block. For this case, the switch drive signal is periodic and the converter establishes a steady-state equilibrium with a constant duty ratio D.

When the small-signal source $\hat{v}_p$ is activated, the control signal is perturbed

$$v_{con}(t) = V_{dc} + \hat{v}_p(t) \tag{6.109}$$

thereby introducing a sinusoidal ac component in the duty ratio

$$d(t) = D + \hat{d}(t) \tag{6.110}$$

The agitated duty ratio in turn generates a perturbed output voltage, consisting of the dc and small-signal components

$$v_O(t) = V_O + \hat{v}_o(t) \tag{6.111}$$

By evaluating the ratio $\hat{v}_o(s)$ to $\hat{v}_p(s)$

$$\frac{\hat{v}_o(s)}{\hat{v}_p(s)} = \frac{\hat{d}(s)}{\hat{v}_p(s)} \frac{\hat{v}_o(s)}{\hat{d}(s)} \tag{6.112}$$

and incorporating the small-signal gain of the PWM block

$$\frac{\hat{d}(s)}{\hat{v}_p(s)} = F_m \tag{6.113}$$

the desired duty ratio-to-output transfer function is now obtained

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{1}{F_m} \frac{\hat{v}_o(s)}{\hat{v}_p(s)} \tag{6.114}$$

where $F_m = 1/V_m$ with V_m being the magnitude of the ramp signal.

The evaluation of the $\hat{v}_o(s)/\hat{v}_p(s)$ ratio can be performed by two different empirical methods – one is an experimental method and the other is a computational method. The first experimental method is to measure the $\hat{v}_o(s)/\hat{v}_p(s)$ ratio from the operational converter using an impedance analyzer. The impedance analyzer injects the input sinusoid while sweeping the perturbation frequency, extracts the output sinusoid in order to compare it with the input sinusoid, and finally generates the magnitude and phase plots for the $\hat{v}_o(s)/\hat{v}_p(s)$ ratio.

The second computational method is to calculate the $\hat{v}_o(s)/\hat{v}_p(s)$ ratio based on time-domain simulations using a circuit simulation software. In this method, the circuit simulation software is employed as a functional equivalent to the impedance analyzer. The simulation software performs a series of time-domain simulations while sweeping the perturbation frequency for the range of interest. The simulation software processes the simulation results to yield the magnitude and phase plots for the $\hat{v}_o(s)/\hat{v}_p(s)$ ratio. Some commercial circuit simulation softwares offer an automated execution of this computational procedure. In this book, the computational method will be used as a means of verifying the analytical results of the small-signal analysis. Whenever appropriate and informative, theoretical results of small-signal analysis will be compared and correlated with the empirical results of the computational method. Further details about the computational method will be given in Chapter 8.

■ EXAMPLE 6.7 Comparison of Duty Ratio-to-Output Transfer Functions

This example compares the prediction of the s-domain small-signal model with the outcomes of the two empirical methods. Figure 6.32 shows the duty ratio-to-output transfer function of the buck converter operating with $V_S = 15$ V,

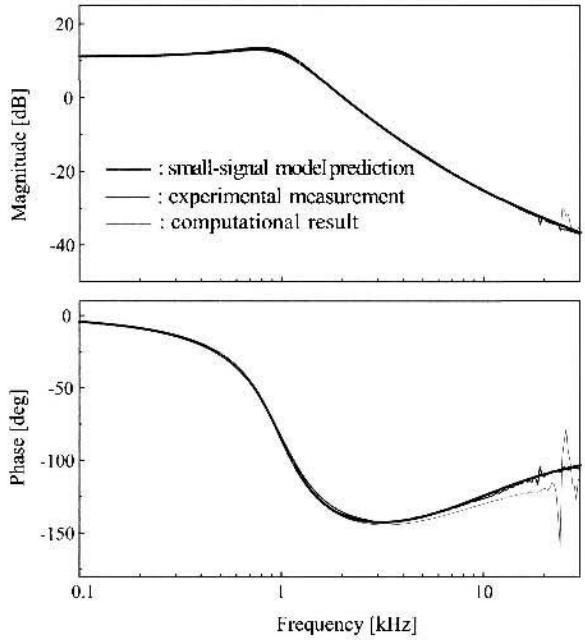


Figure 6.32 Duty ratio-to-output transfer function of buck converter.

$L = 68\ \mu$H, $R_l = 0.16\ \Omega$, $C = 430\ \mu$F, $R_c = 0.05\ \Omega$, $R = 1\ \Omega$, $f_s = 50$ kHz, and $D = 0.33$. The analytical prediction of the small-signal model is compared with both the experimental measurement using an impedance analyzer and the computational result using a circuit simulation software. The close match among the transfer functions confirms the validity and accuracy of the analytical and empirical methods discussed in this section. Example 8.5 in Chapter 8 provides further discussions about the results of the computational method.

6.6 SUMMARY

This chapter investigated the power stage transfer functions of the three basic PWM converters. The input-to-output transfer function, duty ratio-to-output transfer function, and load current-to-output transfer function are analyzed, focusing on their frequency response characteristics.

The three basic PWM converters commonly revealed the low-pass filter characteristics. For buck converter, the power stage inductor L directly combines with the output capacitor to form a low pass filter. For boost and buck/boost converters, an effective inductance $L_e = L/(1-D)^2$ appears in the power stage transfer functions as the inductive parameter.

The boost and buck/boost converters contain a right-half plane (RHP) zero in their duty ratio-to-output transfer function. In addition to the direct evaluation of the transfer function, functional explanations are given to support the existence of the RHP zero. The impact of the RHP zero is analyzed concentrating on the phase characteristics of the duty ratio-to-output transfer function. As will be demonstrated in Section 8.4.7, the RHP zero presents in considerable difficulties to the feedback compensation design and prevents the converters from securing a stable operation with good performance.

Analytical expressions and asymptotic plots for power stage transfer functions are given for the buck, boost, and buck/boost converters. These results will be used in later chapters for the feedback compensation design and closed-loop analysis. Table 6.1 summarizes the expressions for power stage transfer functions of the three basic PWM converters.

This chapter also presented the construction of Bode plots for transfer functions, which was used throughout the chapter to illustrate the frequency response characteristics of the converters. This chapter also introduced the experimental and computational approaches to the power stage dynamic analysis. The computational method will be used in later chapters as a method of verifying predictions of the small-signal analysis and control design.

REFERENCES

1. R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, Kluwer Academic Publishers, 2001.
2. V. Vorpérian, *Fast Analytical Techniques for Electrical and Electronic Circuits*, Cambridge University Press, 2002.
3. K. Ogata, *Modern Control Engineering*, Prentice Hall, 4th ed., 2002.

Table 6.1 Transfer Functions of Three Basic Converters

Buck converter		
$G_{vs} = D\dfrac{1+\dfrac{s}{\omega_{esr}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$	$G_{vd} = V_S\dfrac{1+\dfrac{s}{\omega_{esr}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$	$Z_p = R_l\dfrac{\left(1+\dfrac{s}{\omega_z}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$
$Q = R\sqrt{\dfrac{C}{L}}$	$\omega_o = \dfrac{1}{\sqrt{LC}}$	
$\omega_{esr} = \dfrac{1}{CR_c}$	$\omega_z = \dfrac{R_l}{L}$	
Boost converter		
$G_{vs} = \frac{1}{D'}\dfrac{1+\dfrac{s}{\omega_{esr}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$	$G_{vd} = \frac{V_S}{D'^2}\dfrac{\left(1-\dfrac{s}{\omega_{rhp}}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$	$Z_p = \frac{R_l}{D'^2}\dfrac{\left(1+\dfrac{s}{\omega_z}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$
$D' = 1 - D$	$Q = D'R\sqrt{\dfrac{C}{L}}$	$\omega_o = D'\dfrac{1}{\sqrt{LC}}$
$\omega_{esr} = \dfrac{1}{CR_c}$	$\omega_z = \dfrac{R_l}{L}$	$\omega_{rhp} = D'^2\dfrac{R}{L}$
Boost/boost converter		
$G_{vs} = \frac{D}{D'}\dfrac{1+\dfrac{s}{\omega_{esr}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$	$G_{vd} = \frac{V_S}{D'^2}\dfrac{\left(1-\dfrac{s}{\omega_{rhp}}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$	$Z_p = \frac{R_l}{D'^2}\dfrac{\left(1+\dfrac{s}{\omega_z}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$
$D' = 1 - D$	$Q = D'R\sqrt{\dfrac{C}{L}}$	$\omega_o = D'\dfrac{1}{\sqrt{LC}}$
$\omega_{esr} = \dfrac{1}{CR_c}$	$\omega_z = \dfrac{R_l}{L}$	$\omega_{rhp} = \dfrac{D'^2}{D}\dfrac{R}{L}$

The transfer functions are approximations whose accuracy improves with the conditions $R \gg R_c$ and $R \gg R_l$.

PROBLEMS

6.1 For each of the asymptotic magnitude curves shown in Fig. P6.1, derive the expression for the corresponding transfer function in the time constant form.

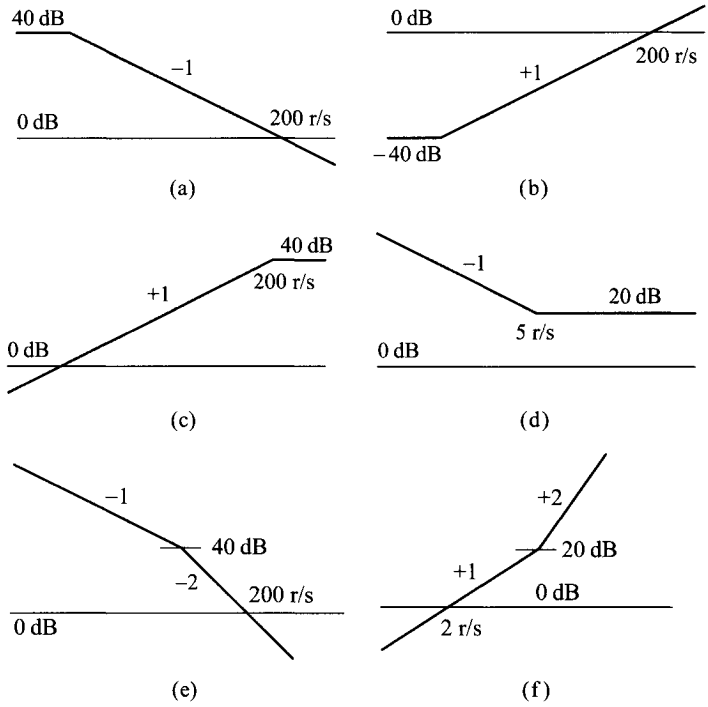


Fig. P6.1

6.2* The input-to-output transfer function of a two-port network is given by

$$\frac{v_o(s)}{v_i(s)} = \frac{\left(1 + \frac{s}{\omega_z}\right)\left(1 + \frac{s^2}{\omega_{o1}^2}\right)}{\left(1 + \frac{s}{\omega_p}\right)\left(1 + \frac{s^2}{\omega_{o2}^2}\right)}$$

For each of the following different input signals, find the expression for amplitude of $v_O(t)$.

i) $v_I(t) = V_m \sin \omega_z t$
ii) $v_I(t) = V_m \sin \omega_{o1} t$
iii) $v_I(t) = V_m \sin \omega_p t$
iv) $v_I(t) = V_m \sin \omega_{o2} t$

6.3* For each asymptotic magnitude curve in Fig. P6.3, derive the expression for the corresponding transfer function in the time constant form.

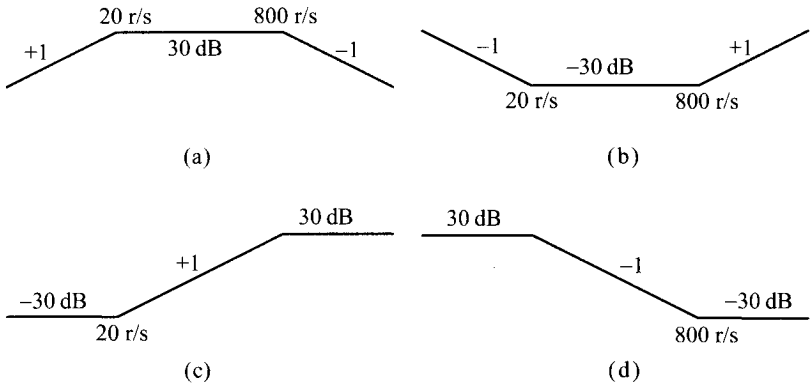


Fig. P6.3

6.4* Consider the following transfer function

$$T(s) = K_t \frac{(s + \omega_{z1})(s + \omega_{z2})}{(s + \omega_{p1})(s + \omega_{p2})}$$

a) Assume $K_t > 1$, $\omega_{p1} < \omega_{z1} < \omega_{z2} < \omega_{p2}$, and $|\omega_{z1} - \omega_{p1}| < |\omega_{p2} - \omega_{z2}|$. Sketch the asymptotic plot of $|T|$. Find the expressions for the maximum and minimum values of $|T|$.

b) Assume $K_t < 1$, $\omega_{z1} < \omega_{p1} < \omega_{z2} < \omega_{p2}$, and $|\omega_{p1} - \omega_{z1}| > |\omega_{p2} - \omega_{z2}|$. Repeat **a)**.

6.5 Sketch the asymptotic plot for $|T|$ of the following transfer functions. Find the expression of the maximum value of $|T|$. Show the corner frequencies of $|T|$.

a) $T(s) = K_t s \dfrac{1}{1 + \dfrac{s}{\omega_p}}$

b) $T(s) = K_t s \dfrac{1}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)}$ with $\omega_{p1} \ll \omega_{p2}$.

c) $T(s) = K_t s \dfrac{1 + \dfrac{s}{\omega_z}}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)}$ with $\omega_{p1} \ll \omega_z \ll \omega_{p2}$.

d) $T(s) = K_t s \dfrac{1 + \dfrac{s}{\omega_z}}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)}$ with $\omega_{p1} \ll \omega_{p2} \ll \omega_z$.

6.6** For the asymptotic plots shown in Fig. P6.6, find the numerical values for X and Y specified in the blanks.

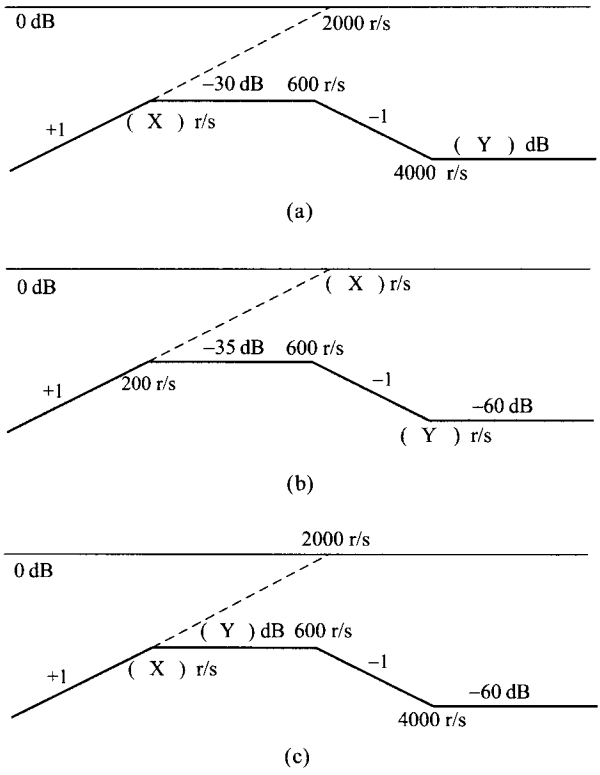


Fig. P6.6

6.7 Sketch the asymptotic magnitude plot $|T|$ of the following transfer function for three cases listed below.

$$T(s) = \frac{K_t}{s} \frac{\left(1 + \dfrac{s}{\omega_{z1}}\right)\left(1 + \dfrac{s}{\omega_{z2}}\right)}{\left(1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}\right)\left(1 + \dfrac{s}{\omega_p}\right)}$$

i) $\omega_{z1} < \omega_o < \omega_{z2} < \omega_p$ **ii)** $\omega_{z1} < \omega_{z2} < \omega_o < \omega_p$

iii) $\omega_o < \omega_{z1} < \omega_{z2} < \omega_p$

6.8 Referring to the asymptotic magnitude plots shown in Fig. P6.8, find the numerical values for X and Y specified in the blanks.

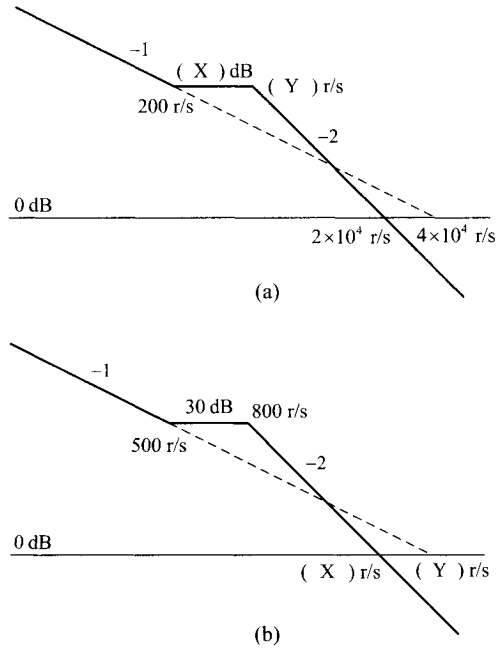


Fig. P6.8

6.9 Sketch the asymptotic magnitude plot for the following transfer functions. Show the corner frequency, 0 dB crossover frequency, and slopes of asymptotes.

i) $T_1(s) = \dfrac{\omega_o^2}{s^2}$ **ii)** $T_2(s) = \dfrac{s^2}{\omega_o^2}$

iii) $T_3(s) = 1 + \dfrac{\omega_o}{s}$ **iv)** $T_4(s) = \dfrac{1}{1 + \dfrac{\omega_o}{s}}$

6.10 Construct the magnitude and phase asymptotic plots for the following transfer functions. Show the corner frequency, 0 dB crossover frequency, and slopes of magnitude asymptotes, as appropriate.

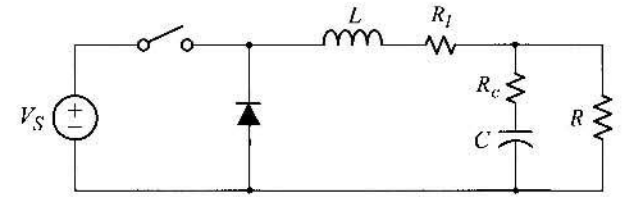
i) $T_1(s) = \dfrac{1 - s}{1 + s}$

ii) $T_2(s) = \dfrac{1 - \dfrac{s}{2}}{1 + s}$

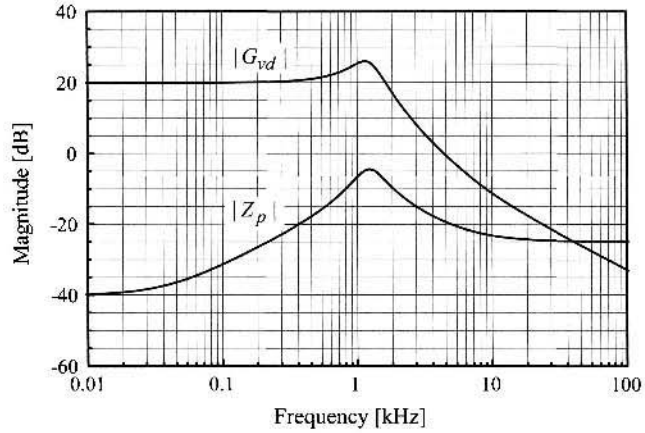
iii) $T_3(s) = \dfrac{1 - s + s^2}{1 + s + s^2}$

iv) $T_4(s) = \dfrac{1 - \dfrac{s}{2} + \dfrac{s^2}{4}}{1 + s + s^2}$

6.11** Figure P6.11 shows the circuit diagram of a buck converter and its duty ratio-to-output transfer function, $G_{vd}(s)$, and load current-to-output transfer function, $Z_p(s)$. Based on the information given in the Bode plots, estimate the values of the circuit components $\{L\ R_l\ C\ R_c\ R\}$ and the input voltage V_S of the buck converter. Assume $R \gg R_l$ and $R \gg R_c$.



(a)



(b)

Fig. P6.11

6.12* Follow the procedure shown in Example 6.4 in order to derive the duty ratio-to-output transfer function, $G_{vd}(s)$, of the boost converter and buck/boost converter with the parasitic resistances of the reactive components: $R_l \neq 0$ and $R_c \neq 0$.

6.13 Figure P6.13 shows the circuit diagrams of the three basic dc-to-dc converters. Sketch the asymptotic plots for the magnitude and phase responses of the three transfer functions of $G_{vs}(s)$, $G_{vd}(s)$, and $Z_p(s)$. Note that $R_l = 0$, yet $R_c \neq 0$.

Express the corner frequencies and asymptotic values of the magnitude plot in terms of the circuit parameters and operating conditions. Assume $Q > 0.5$ and $\omega_o \ll \omega_{esr}$ for the buck converter, and $\omega_o \ll \omega_{rhp} \ll \omega_{esr}$ for boost and buck/boost converters.

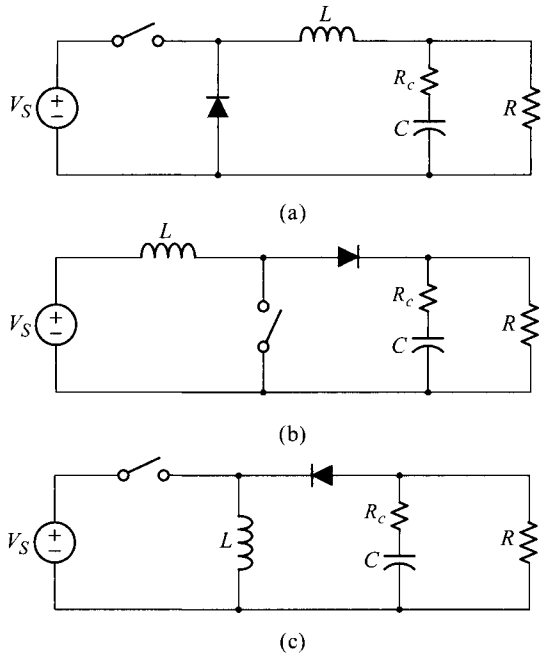


Fig. P6.13

6.14** An experimental circuit is built to extract the frequency response of a buck converter power stage. Using the experimental set-up in Fig. P6.14(a), the frequency response of $\hat{v}_o(s)/\hat{v}_p(s)$ is measured as shown in Fig. P6.14(b).

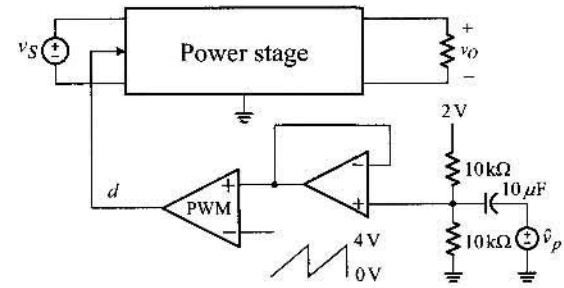
a) Find an analytical expression for the duty ratio-to-output transfer function, $G_{vd}(s) = \hat{v}_o(s)/\hat{d}(s)$, of the buck power stage.

b) Find an analytical expression for the input-to-output transfer function, $G_{vs}(s) = \hat{v}_o(s)/\hat{v}_s(s)$, of the converter operating in the experimental set-up.

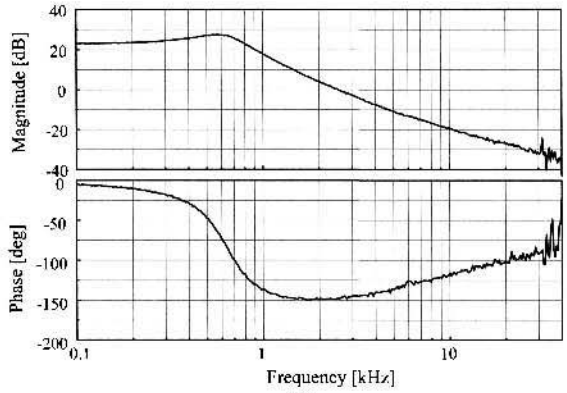
6.15* This problem deals with the identification of the transfer function from the given Bode plot.

a) Assume that the Bode plot in Fig. P6.15(a) is generated from the transfer function

$$T(s) = \frac{K_t}{s} \frac{1 + \dfrac{s}{\omega_z}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}}$$



(a)



(b)

Fig. P6.14

Find the numerical values for the parameters $\{K_t\ \omega_z\ Q\ \omega_o\}$.

b) Figure P6.15(b) is the Bode plot of the transfer function

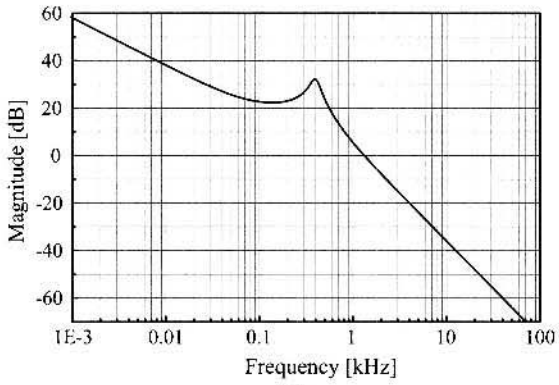
$$T(s) = K_t s \frac{1}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

Determine the numerical values for the parameters $\{K_t\ \omega_{p1}\ \omega_{p2}\}$.

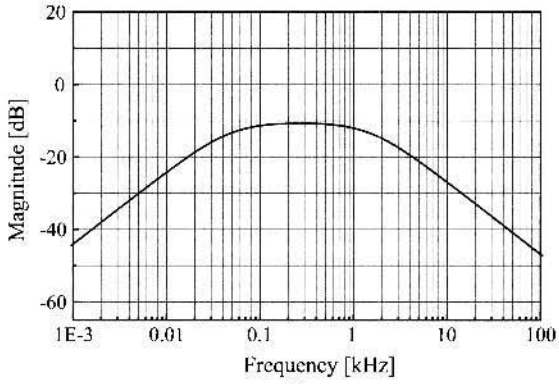
c) Figure P6.15(c) is generated from the transfer function

$$T(s) = \frac{K_t}{s} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}$$

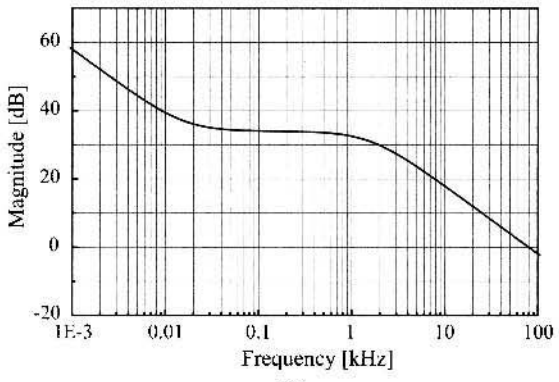
Find the numerical values for the parameters $\{K_t\ \omega_z\ \omega_p\}$.


60
40
20
0
-20
-40
-60
Magnitude [dB]
1E-3
0.01
0.1
1
10
100
Frequency [kHz]

(a)


20
0
-20
-40
-60
Magnitude [dB]
1E-3
0.01
0.1
1
10
100
Frequency [kHz]

(b)


60
40
20
0
-20
Magnitude [dB]
1E-3
0.01
0.1
1
10
100
Frequency [kHz]

(c)

Fig. P6.15

CHAPTER 7

DYNAMIC PERFORMANCE OF PWM DC-TO-DC CONVERTERS

Dc-to-dc converters are intended to function as an effective and reliable voltage source. Accordingly, there are certain criteria to assess the performance of dc-to-dc converters as a voltage source. These performance criteria are typically classified into two categories. The first category is the static or dc criteria which characterize the converters' performance in steady state. The static performance criteria include the power handing capacity, current and voltage stresses of switches, and output voltage ripple. These criteria are determined by power stage parameters and are irrelevant to the feedback controller.

The second category is the dynamic or ac performance criteria which describe the converters' ability to withstand the external and internal disturbances or transient behavior at the presence of certain changes in the operational conditions. The dynamic performance criteria include stability, frequency-domain transfer functions, and time-domain transient responses. In contrast to the static performance, the dynamic performance is solely determined by the feedback controller. Thus, two dc-to-dc converters with identical power stage parameters could show entirely different dynamic performance, depending on the characteristics of their feedback controller.

There are several requirements for engineers to build dc-to-dc converters for satisfactory dynamic performance. The first requirement is the comprehension about

Pulsewidth Modulated Dc-to-Dc Power Conversion. By Byungcho Choi

the small-signal dynamics of the power stage. Chapters 5 and 6, which dealt with the small-signal modeling and analysis of the converter power stage, would serve this purpose. The second requirement is to understand the nature and implication of the dynamic performance of closed-loop controlled dc-to-dc converters. The final requirement is the implementation of the feedback controller which could provide good dynamic performance. The purpose of this chapter is to cover the second requirement, namely, investigating the dynamic performance of dc-to-dc converters. The design and implementation of the feedback controller are explored in Chapter 8.

7.1 STABILITY

In previous chapters, it is implicitly considered that dc-to-dc converters always establish a periodic operation in steady state. However, this is only the case when dc-to-dc converters operate in an open-loop fashion with a fixed duty ratio. When a closed-loop feedback control is employed to regulate the output voltage, dc-to-dc converters reach a periodic steady-state operation, given only that their feedback controller is properly designed to meet the stability criterion.

Figure 7.1(a) shows the circuit diagram of a closed-loop controlled buck converter. This converter will be used throughout this chapter to illustrate stability and other dynamic performance of the closed-loop controlled dc-to-dc converter. Figure 7.1(b) shows the output voltage v_O and inductor current i_L of the buck converter which goes through a transition from stable operation to unstable operation. Initially, the feedback controller is duly designed to secure a stable operation. In the middle of the stable operation, the circuit parameters of the feedback compensation are altered to new values that violate the stability criterion. With the new unstable compensation parameters, the circuit waveforms start to show a growing oscillation as the token of instability.

Stability analysis can be performed using the familiar classical control theory because we have already developed the s-domain small-signal model for dc-to-dc converters. As will be explained in Section 7.5, stability is judged by investigating the loop gain characteristics of the converter. First, we evaluate the loop gain from the small-signal model of the converter. Then, the loop gain is portrayed either in the Bode plot format to assess stability margins or in the polar plot format to apply the Nyquist stability criterion. While the detailed stability analysis using the s-domain small-signal model will be covered later in this chapter, the results of such an analysis are shown in the following example, in order to highlight the utility of the s-domain small-signal model.

■ EXAMPLE 7.1 Stability Analysis of Buck Converter

This example provides an introductory overview of the upcoming stability analysis based on the classical control theory. The simplicity and accuracy of the stability analysis are demonstrated using the buck converter shown in Fig.

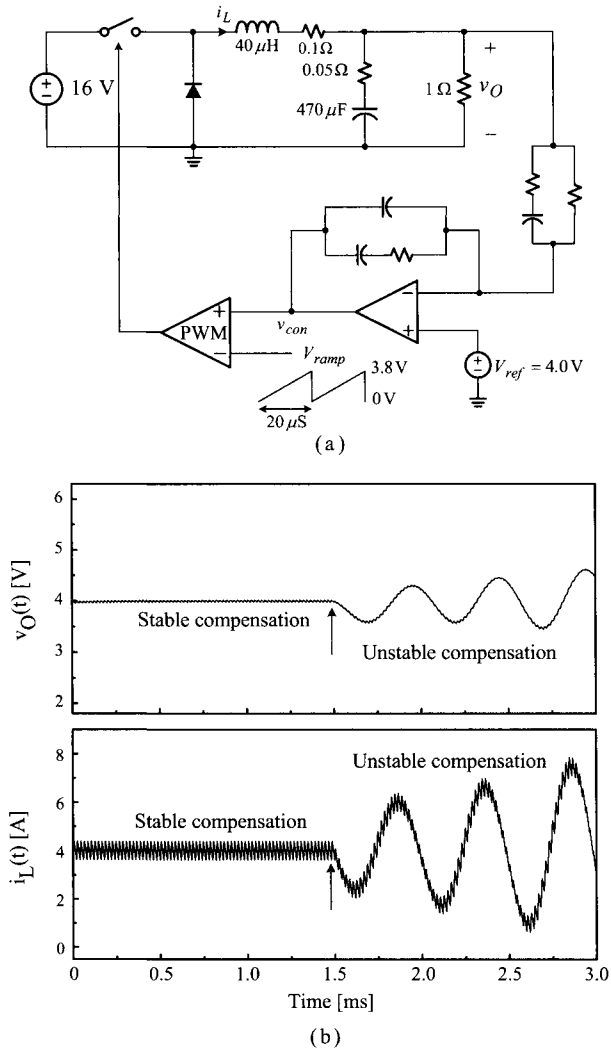
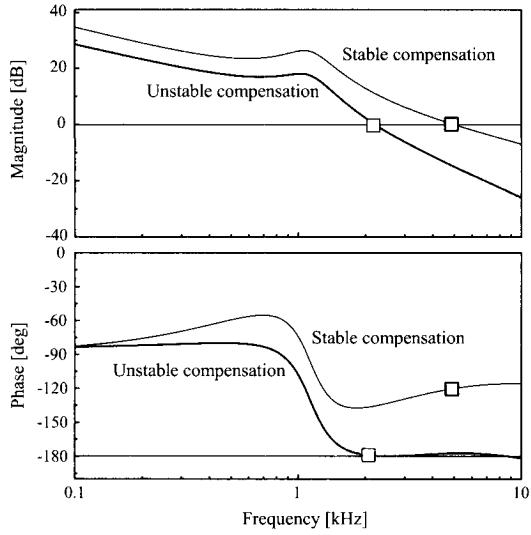
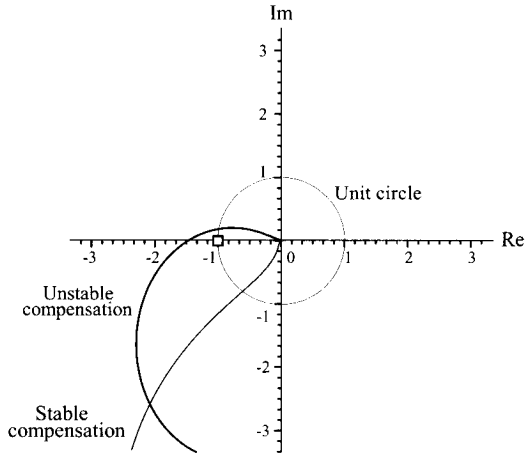


Figure 7.1 Closed-loop controlled buck converter. (a) Circuit diagram. (b) Circuit waveforms showing transition from stable operation to unstable operation.

7.1. The loop gain of the converter, obtained from the s-domain small-signal model, is employed as the analytical basis for the stability analysis. Figure 7.2(a) shows the loop gain of the buck converter in the Bode plot format, while Fig. 7.2(b) depicts the same loop gain in the polar plot format. The loop gain is evaluated with the two different feedback compensations: the original stable compensation and the modified unstable compensation. With the original compensation, the Bode plot indicates that the converter is stable



(a)



(b)

Figure 7.2 Stability analysis of buck converter. (a) Bode plot of loop gain. (b) Polar plot of loop gain.

with a sufficient phase margin and the polar plot well satisfies the Nyquist stability criterion. With the modified compensation, by contrast, the phase margin vanishes and the polar plot encircles the $(-1, 0)$ point, thereby both indicating that the converter is unstable. The prediction of Fig. 7.2 is surely consistent with the circuit waveforms in Fig. 7.1.

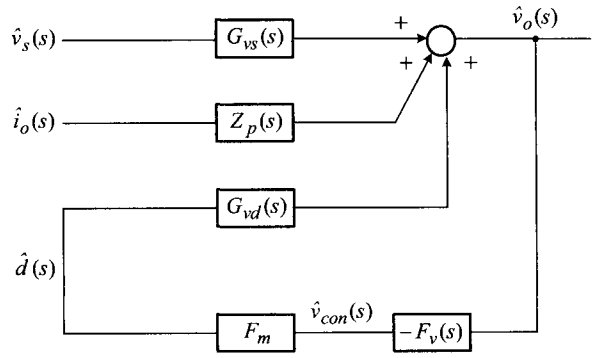


Figure 7.3 Small-signal block diagram of closed-loop controlled dc-to-dc converter.

Although the stability analysis is rather straightforward and standard, readers should be reminded that this simple analysis is possible due to the existence of the s-domain small-signal model. If the small-signal model were not available, the stability analysis would be a very challenging task.

7.2 FREQUENCY-DOMAIN PERFORMANCE CRITERIA

There are three frequency-domain transfer functions that are meaningful and useful as the dynamic performance for a closed-loop controlled converter. They are the loop gain, audio-susceptibility, and output impedance. This section describes the definition and implication of these performance criteria.

7.2.1 Loop Gain

As demonstrated in Example 7.1, the loop gain carries the whole information about the converter stability. Figure 7.3 is the small-signal block diagram of a closed-loop controlled dc-to-dc converter. The gain block F_m represents the small-signal gain of the PWM block, $F_v(s)$ is the voltage feedback compensation, and the other gain blocks denote the small-signal transfer functions of the power stage. The power stage transfer functions for the three basic PWM converters were studied in Chapter 6.

The loop gain is defined as the *negative* product of all the gain blocks located along the feedback path. From Fig. 7.3, the loop gain is determined as

$$T_m(s) \equiv (-)\frac{\hat{v}_o(s)}{\hat{d}(s)}\frac{\hat{v}_{con}(s)}{\hat{v}_o(s)}\frac{\hat{d}(s)}{\hat{v}_{con}(s)} = (-)G_{vd}(s)(-)F_v(s)F_m$$
$$= G_{vd}(s)F_v(s)F_m \qquad (7.1)$$

where $G_{vd}(s)$ is the duty ratio-to-output transfer function. Once evaluated from the individual gain blocks, the loop gain can be converted into the Bode plot or polar plot for stability analysis. Examples of the loop gain plots were shown in Example 7.1.

In addition to stability, the loop gain is also closely related with other frequency-domain transfer functions – the audio-susceptibility and output impedance. Thus, the loop gain lies at the center of the small-signal analysis and control design, and governs all the dynamic performance of the converter. For the given duty ratio-to-output transfer function and PWM gain, the voltage feedback compensation $F_v(s)$ is the only gain block that can be freely designed for good loop gain characteristics. Thus, the dynamic analysis and control design are eventually directed by the design of $F_v(s)$. This topic will be treated in Chapter 8.

7.2.2 Audio-Susceptibility

Dc-to-dc converters usually receive the input from a non-ideal voltage source, rather than a pure dc source. For example, the input of an off-line dc-to-dc converter is the rectified utility line, which usually contains line-frequency ripple component. Also, in distributed power systems where several dc-to-dc converters are employed together, the input of one dc-to-dc converter may pick up various noises generated by the other converters in the system.

A dc-to-dc converter is required to generate a constant dc voltage as its output, regardless of the ripple or noise component in the input voltage. Thus, it becomes necessary to define the input-to-output noise rejection as one of the performance criteria. The *audio-susceptibility* refers to the input-to-output voltage transfer function, which in fact represents the input-to-output noise rejection capacity of dc-to-dc converters.

In the past, dc-to-dc converters operated with the switching frequency that falls into the audible frequency range, for example f_s = 10 kHz. When excited by the 10 kHz switching frequency, the magnetic components generate audible noises that would propagate to the converter output. Although the switching frequency of modern dc-to-dc converters now extends far beyond the audible frequency range, the audio-susceptibility is still used to describe the noise transmission characteristics of dc-to-dc converters.

By applying Mason's gain rule to Fig. 7.3, the audio-susceptibility is evaluated as

$$A_u(s) \equiv \left.\frac{\hat{v}_o(s)}{\hat{v}_s(s)}\right|_{\text{closed}} = \frac{G_{vs}(s)}{1 + T_m(s)} \tag{7.2}$$

where $G_{vs}(s)$ is the input-to-output transfer function and $T_m(s)$ is the loop gain defined in (7.1). With a given input-to-output transfer function, the audio-susceptibility can be altered by changing the loop gain. One objective of the loop gain design would be minimizing the audio-susceptibility for all frequencies, thereby providing a constant output voltage with minimal noise contamination.

■ EXAMPLE 7.2 Audio-Susceptibility of Buck Converter

Figure 7.4 shows the audio-susceptibility of the buck converter introduced in Example 7.1. The prediction of the small-signal model is shown in comparison

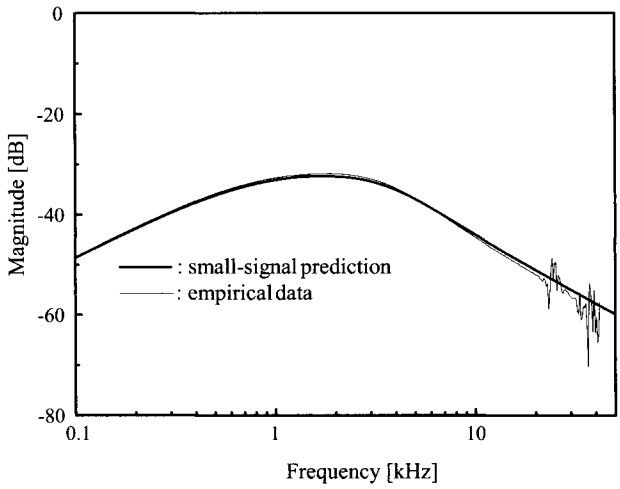


Figure 7.4 Audio-susceptibility of buck converter.

with the empirical result obtained from the computational method discussed in Section 6.5. The use and accuracy of the computational method for the dynamic analysis of dc-to-dc converters will be described in detail in Example 8.5. The audio-susceptibility curve indicates that the converter provides sufficient noise rejection at low and high frequencies yet it passes the mid-frequency noise components with about 33 dB attenuation.

7.2.3 Output Impedance

Dc-to-dc converters are also required to maintain the output voltage constant at the presence of variations or fluctuations in the load current. One way to characterize this feature is to investigate the closed-loop transfer function from the load current to output voltage. This transfer function is referred to as the *output impedance*.

Same as the audio-susceptibility case, the output impedance should be minimized for all frequencies. As the output impedance becomes smaller, the dc-to-dc converter resembles an ideal voltage source more closely, which has *zero* output impedance. Thus, minimizing the output impedance is another important objective of the controller design.

From the small-signal block diagram of Fig. 7.3, the output impedance is evaluated as

$$Z_o(s) \equiv \left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\text{closed}} = \frac{Z_p(s)}{1 + T_m(s)} \tag{7.3}$$

where $Z_p(s)$ is the open-loop load current-to-output transfer function. The loop gain affects the output impedance in the same manner as that of the audio-susceptibility case.

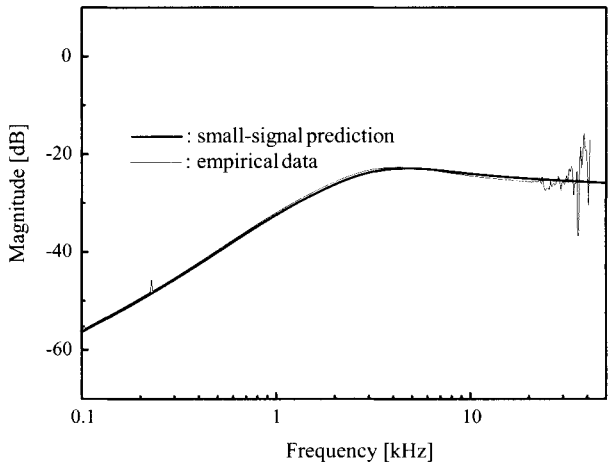


Figure 7.5 Output impedance of buck converter.

■ EXAMPLE 7.3 Output Impedance of Buck Converter

Figure 7.5 shows the theoretical and empirical output impedances of the buck converter used in Example 7.1. The output impedance starts with a very small magnitude at low frequencies and gradually increases until it approaches a constant value at high frequencies. As will be shown in Section 8.2.2, the high-frequency asymptote is determined by the equivalent series resistance (esr) of the output capacitor: $|Z_o(j\infty)| = 20 \log R_c$. For the power stage parameters shown in Fig. 7.1(a), the high-frequency asymptote is given by $20 \log 0.05 = -26$ dB.

7.3 TIME-DOMAIN PERFORMANCE CRITERIA

Besides the frequency-domain performance, the time-domain performance is also important when evaluating dc-to-dc converters as a voltage source. The time-domain performance includes the transient response of the output voltage due to a sudden change in the load current or input voltage.

Transient responses of a buck converter have already been presented in Section 3.6.2, in order to illustrate the principles of the closed-loop control using PWM scheme. In the current section, the transient responses are investigated as the dynamic performance of dc-to-dc converters.

7.3.1 Step Load Response

The step load response refers to the transient response of the output voltage due to a step change in the load current. The step load response has been of concern for two reasons. First, in many applications, dc-to-dc converters often encounter step changes in the load current. For example, dc-to-dc converters powering digital equipment downstream will frequently experience sudden changes in the load current. Second, the step load response is usually used as a means of evaluating the transient performance in general. The converter producing a good step load response will also offer good transient responses upon other changes in operational conditions.

The time-domain transient response can be analyzed using the *appropriate* s-domain transfer function. Especially, the step load response is investigated using the output impedance, which is the closed-loop load current-to-output transfer function. First, the s-domain expression of the output voltage is obtained by multiplying the output impedance by the s-domain expression of the step change in the load current

$$v_o(s) = \frac{I_{step}}{s} Z_o(s) \tag{7.4}$$

where I_{step} is the magnitude of the load current change. Now, the inverse Laplace transform is performed on (7.4) to yield the time-domain expression for the output voltage

$$v_O(t) = \mathcal{L}^{-1}\left(\frac{I_{step}}{s} Z_o(s)\right) \tag{7.5}$$

where $\mathcal{L}^{-1}$ represents the inverse Laplace transform. This relationship will be used in later chapters to investigate the transient behavior of the output voltage.

■ **EXAMPLE 7.4 Step Load Response of Buck Converter**

This example shows the step load response of the buck converter used in the previous examples. Figure 7.6 shows the output voltage of the converter going through a series of step changes in the load current: I_O = 4 A ⇒ 8 A ⇒

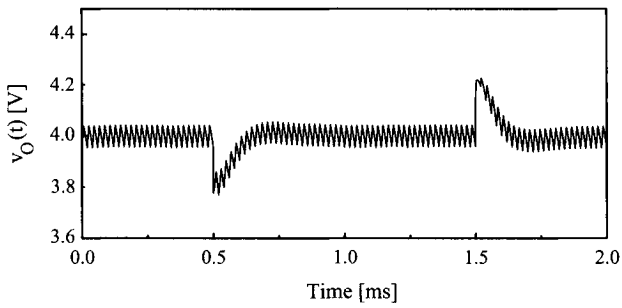


Figure 7.6 Step load response of buck converter.

4 A. The load current change is introduced by altering the load resistance accordingly. Qualitative explanations about the output voltage response were given in Section 3.6.2.

The step load response is mainly characterized by two parameters: the peak overshoot/undershoot and settling time. The peak overshoot/undershoot is the maximum transitional deviation of the output voltage from the steady-state value. The settling time is the time interval before the output voltage settles within ±5% of the final value. Figure 7.6 indicates that the peak overshoot/undershoot is limited by ±0.2 V and the settling time is less than 0.2 ms.

7.3.2 Step Input Response

The step input response is the transient behavior of the output voltage due to a step change in the input voltage. Examples of the step input response were presented in Section 3.6.2. Similar to the step load response case, the step input response is analyzed using the audio-susceptibility

$$v_o(t) = \mathcal{L}^{-1}\left(\frac{V_{step}}{s}A_u(s)\right) \tag{7.6}$$

where V_{step} is the magnitude of the step change in the input voltage.

■ **EXAMPLE 7.5 Step Input Response of Buck Converter**

This example shows the step input response of the previous buck converter. Figure 7.7 is the output voltage of the buck converter experiencing a series of step changes in the input voltage: V_S = 16 V ⇒ 8 V ⇒ 16 V. Same as the step load response case, the peak overshoot/undershoot and settling time are the two important parameters for the step input response. Figure 7.7 shows a ±0.4 V peak overshoot/undershoot which returns to the steady-state value within a 0.7 ms settling time.

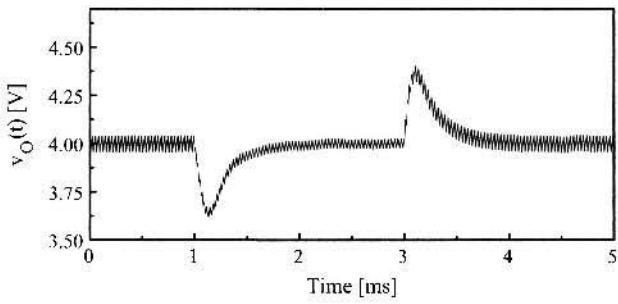


Figure 7.7 Step input response of buck converter.

7.4 STABILITY OF DC-TO-DC CONVERTERS

Section 7.1 introduced the concept of stability and demonstrated the behavior of an unstable dc-to-dc converter. In this section, we study the stability theory adapted to dc-to-dc converters. The classical stability theory, originally established for linear time-invariant (LTI) systems, is reviewed. Then, we will discuss how the classical stability theory is extended to nonlinear time-variant PWM dc-to-dc converters. This section starts with discussions about the stability of LTI systems.

7.4.1 Stability of Linear Time-Invariant Systems

Stability theory for LTI systems is closely related with the transfer function and characteristic equation. The transfer function of an LTI system is defined as the ratio of the Laplace transform of the output to the Laplace transform of the input under the assumption that all initial conditions are zero. The transfer function is given by a ratio of s-domain polynomials

$$F(s) = \frac{b_o + b_1 s + b_2 s^2 + \cdots\cdots + b_{m-1} s^{m-1} + b_m s^m}{a_o + a_1 s + a_2 s^2 + \cdots\cdots + a_{n-1} s^{n-1} + a_n s^n} \tag{7.7}$$

The characteristic equation is then defined as

$$a_o + a_1 s + a_2 s^2 + \cdots\cdots + a_{n-1} s^{n-1} + a_n s^n = 0 \tag{7.8}$$

from the denominator of the transfer function. The characteristic equation contains all the important information about the dynamic properties of the system. Most significantly, the solutions of the characteristic equation are called the poles or natural modes of the system. The location of the poles in s-plane determines stability of the system.

LTI systems are defined *unstable* if any of their poles is located in the right-hand plane (RHP) of s-plane or on the imaginary axis. An unstable system would produce exponentially or sinusoidally growing responses if it has any poles in RHP of s-plane. Also, the system would exhibit a sustained oscillation if its poles are located on the imaginary axis.

Conversely, an LTI system is defined *stable* if all the poles are located in the left-hand plane (LHP) of s-plane. A stable LTI system does not contain any growing or oscillating terms and all transient responses will eventually settle down to their steady-state values. Accordingly, a stable LTI system establishes a stationary operating point in steady state. Furthermore, if the system is perturbed by certain external or internal disturbance, a stable system always returns to the original operating point.

7.4.2 Small-Signal Stability of Dc-to-Dc Converters

The classical stability theory is now extended to nonlinear time-variant PWM dc-to-dc converters as explained below. We consider a dc-to-dc converter stable if the converter produces periodic circuit waveforms in steady state. A stable inductor current settles

into a periodic triangular waveform and a stable output voltage periodically *ripples* on top of the desired dc component. If the averaging operation discussed in Section 5.2 is executed on the stable periodic waveforms, the resulting waveforms will not show any behavior of an unstable LTI system. In other words, the averaged circuit waveforms of a stable dc-to-dc converter do not resemble the circuit waveforms produced by an unstable LTI system. Conversely, the averaged circuit waveforms of an unstable dc-to-dc converter will exhibit the circuit behavior of an unstable LTI system.

As elaborated in Section 5.2, the average model of dc-to-dc converters is developed to accurately predict the averaged circuit waveforms of the converter. Accordingly, we could adapt the stability theory to the average model of a dc-to-dc converter to test whether the converter establishes a periodic steady-state operation, or equivalently, to determine stability of the converter. However, the classical stability theory cannot be directly applied to the average model of the converter, because the average model is still nonlinear although it is time invariant. As a functional alternative, the s-domain small-signal model obtained by linearizing the average model is used for stability analysis.

The small-signal model is a linear approximation of the nonlinear average model. The approximation is based on the condition that the converter remains in close proximity to the initial operating point. Therefore, the validity of the small-signal model is limited to the neighborhood of the given operating point. This implies that the result of the stability analysis using the small-signal model can only be used for the *local stability*. In other words, the stability theory only provides the information about the converter's behavior near the given operating point and is not suited to judge the stability of the converter that experiences large excursions. In this sense, the stability defined on the small-signal model is also called the *small-signal stability*. Despite the aforementioned restrictions and limitations, the small-signal stability still is a very useful and viable method for analyzing the stability of the nonlinear time-variant dc-to-dc converters.

Based on the preceding discussions, we now apply the classical stability theory to the small-signal model of the converter. If the small-signal model is found to be stable, we are assured that the converter would attain a periodic steady-state operation. In addition, the converter will withstand external and internal disturbances and return to the original state if the magnitude of the disturbance is not too large.

7.5 NYQUIST CRITERION

The Nyquist criterion plays the central role in the classical stability theory. The Nyquist criterion provides a graphical means of determining the number of RHP roots in the equation of the following specific form

$$1 + T(s) = 0 \tag{7.9}$$

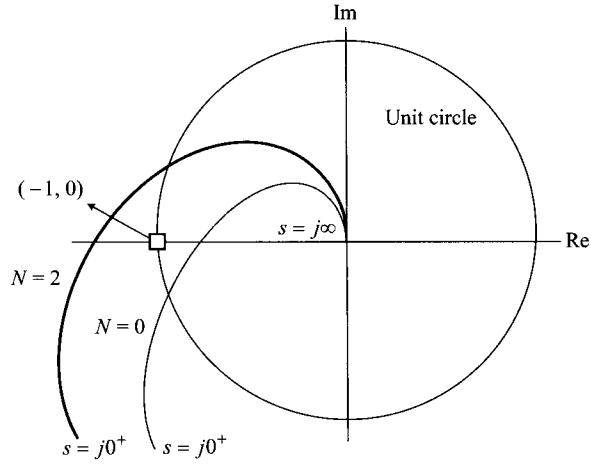


Figure 7.8 Polar plots of $T(s)$.

where $T(s)$ is an s-domain rational function. The Nyquist criterion is based on the well-known relationship

$$\mathcal{Z} = \mathcal{N} + \mathcal{P} \tag{7.10}$$

where $\mathcal{Z}$ is the number of RHP roots in $1 + T(s) = 0$, $\mathcal{N}$ represents the number of encirclements of the $(-1, 0)$ point made by the polar plot of $T(s)$, and $\mathcal{P}$ is the number of RHP poles in $T(s)$ itself.

Figure 7.8 shows the polar plots of $T(s)$, drawn under the assumption that $|T(s)|$ monotonically decreases when the frequency is swept from $s = j0^+$ to $j\infty$. The polar plot displayed with the thin line does not encircle the $(-1, 0)$ point and consequently $\mathcal{N} = 0$ for this case. On the other hand, the polar plot depicted with the thick line encircles the $(-1, 0)$ point. It should be noted that the polar plot in Fig. 7.8 is sketched only for the positive frequency. The complementary part of the plot, evaluated for the negative frequency, is the symmetric mirror image of the original plot reflected on the real axis. When both positive and negative frequencies are considered, the polar plot thus encircles the $(-1, 0)$ point twice. Accordingly, it becomes that $\mathcal{N} = 2$ for this case. Now, if the number of RHP poles in $T(s)$, $\mathcal{P}$, is known, the number of RHP roots in $1 + T(s) = 0$, $\mathcal{Z}$, is determined from (7.10).

The Nyquist criterion is now adapted to the stability analysis of dc-to-dc converters. The audio-susceptibility of the closed-loop controlled converter is determined as

$$A_u(s) = \left.\frac{\hat{v}_o(s)}{\hat{v}_s(s)}\right|_{\text{closed}} = \frac{G_{vs}(s)}{1 + G_{vd}(s)F_v(s)F_m} \tag{7.11}$$

by applying Mason's gain rule to the small-signal model of the converter in Fig. 7.3.

When the input-to-output transfer function $G_{vs}(s)$ is denoted as

$$G_{vs}(s) = \frac{\mathcal{N}(s)}{\mathcal{D}(s)} \tag{7.12}$$

the audio-susceptibility becomes

$$A_u(s) = \frac{\mathcal{N}(s)}{\mathcal{D}(s)\left(1 + G_{vd}(s)F_v(s)F_m\right)} \tag{7.13}$$

The characteristic equation is then given by

$$\mathcal{D}(s)\left(1 + G_{vd}(s)F_v(s)F_m\right) = 0 \tag{7.14}$$

If the equation $\mathcal{D}(s) = 0$ does not contain any RHP roots, stability is determined by investigating the existence of any RHP root in $1 + G_{vd}(s)F_v(s)F_m = 0$, that is, by applying the Nyquist criterion to $1 + T_m(s) = 0$ where $T_m(s) = G_{vd}(s)F_v(s)F_m$ is the loop gain defined in the previous section.

There are several remarks regarding the preceding discussions. First, while the audio-susceptibility is used in the previous analysis, any closed-loop transfer function can be used for the stability analysis because all transfer functions have the same denominator. Second, the power stage transfer functions of the three basic converters indeed do not have any RHP pole; more specifically, the equation $\mathcal{D}(s) = 0$ does not have any RHP roots as presumed in the previous discussions. Finally, the loop gain, $T_m(s) = G_{vd}(s)F_v(s)F_m$, of the three basic converters does not contain any RHP poles: $\mathcal{P} = 0$. Accordingly, the Nyquist criterion is simplified as follows. The number of the RHP roots in the characteristic equation is the same as the number of $(-1, 0)$ point encirclements made by the polar plot of the loop gain: $\mathcal{Z} = \mathcal{N}$. In this case, stability is simply tested using the polar plot drawn only for positive frequencies; for stability, the polar plot should not encircle the $(-1, 0)$ point.

The preceding discussions about the Nyquist criterion provide a graphical method for the stability analysis using the converter loop gain. Figure 7.9 shows the four different cases of the polar plot of the converter loop gain, $T_m(s) = G_{vd}(s)F_v(s)F_m$.

Figure 7.9(a) shows the stable case in which the polar plot of the converter loop gain does not encircle the $(-1, 0)$ point. Figure 7.9(b) is the unstable polar plot, encircling the $(-1, 0)$ point. Figure 7.9(c) is the marginally stable case where the polar plot just passes the $(-1, 0)$ point. The marginally stable case is the borderline between stability and instability. For this case, the system has a pair of poles on the imaginary axis and develops sustained oscillations in time-domain responses. The behavior of a marginally stable dc-to-dc converter will be analyzed in Example 7.6.

Finally, Fig. 7.9(d) shows a special case where the polar plot of the converter loop gain does not encircle the $(-1, 0)$ point but exhibits a distinctive pattern. The polar plot initially crosses the – real axis outside the unit circle. Later, the polar plot passes the – real axis again before intersecting the unit circle, and finally approaches the origin without encircling the $(-1, 0)$ point. The system with these loop gain characteristics is called *conditionally stable system*. Although stable, the conditionally stable system

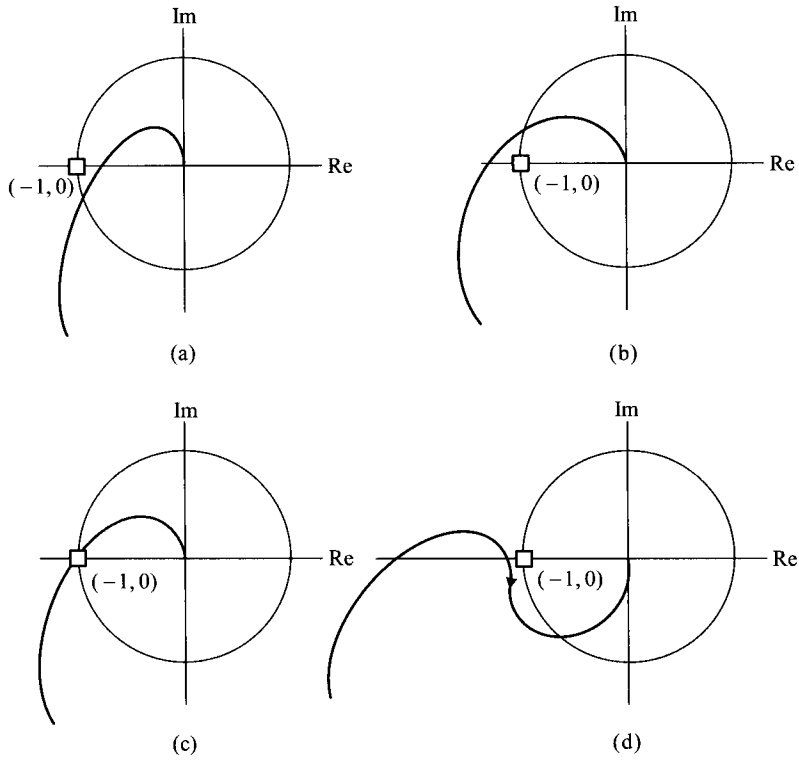


Figure 7.9 Polar plot of converter loop gain and stability. (a) Stable system. (b) Unstable system. (c) Marginally stable system. (d) Conditionally stable system.

can be problematic in real applications due to the distinguishing polar plot pattern. The feature of the conditionally stable system, along with its potential stability problem in practical applications, will be analyzed in Example 7.7.

The Nyquist criterion can also be applied to the converter loop gain portrayed in the Bode plot format. To illustrate this, the first three cases in Fig. 7.9 are redrawn in Fig. 7.10 in both the Bode plot and polar plot formats.

1) **Stable case in Fig. 7.10(a):** The polar plot passes the − real axis through a point located between the $(-1, 0)$ point and the origin. In other words, the polar plot crosses the − real axis with its magnitude smaller than unity: $|T_m| < 0$ dB at the frequency where $\angle T_m$ becomes $-180°$. This situation is illustrated in the Bode plot in Fig. 7.10(a).

2) **Unstable case in Fig. 7.10(b):** The polar plot crosses the − real axis with its magnitude larger than unity: $|T_m| > 0$ dB at the frequency where $\angle T_m$ is $-180°$. This condition is depicted in the Bode plot in Fig. 7.10(b). For this case, the

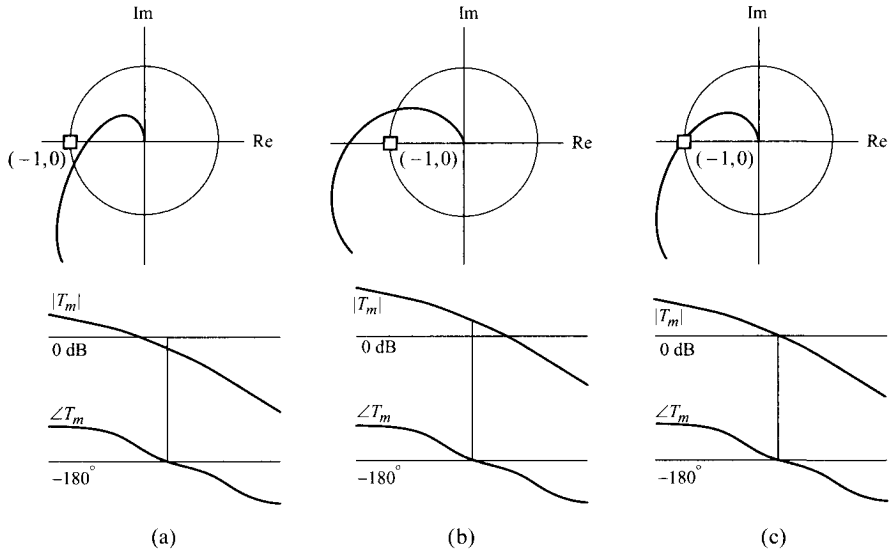


Figure 7.10 Stability analysis using polar plot and Bode plot of converter loop gain. (a) Stable case. (b) Unstable case. (c) Marginally stable case.

polar plot crosses the − real axis through a point between $(-1, 0)$ and $(-\infty, 0)$, thereby encircling the critical $(-1, 0)$ point.

3) **Marginally stable case in Fig. 7.10(c):** The polar plot passes the − real axis with its magnitude exactly being unity. This situation corresponds to the case where $|T_m|$ crosses the 0 dB line with $\angle T_m = -180°$, as shown in the Bode plot in Fig. 7.10(c).

As illustrated in Fig. 7.10, stability can also be judged directly from the Bode plot of the loop gain. For stability, $|T_m|$ should be smaller than 0 dB when $\angle T_m$ falls to $-180°$, or equivalently $\angle T_m$ should be larger than $-180°$ (less negative than $-180°$) when $|T_m|$ reduces to 0 dB. This condition is identical to the requirement of *not* encircling the $(-1, 0)$ point in the polar plot. Example 7.1 illustrated the application of this stability theory to a practical dc-to-dc converter.

■ EXAMPLE 7.6 Marginally Stable Buck Converter

The purpose of this example is to demonstrate the loop gain characteristics and time-domain response of a marginally stable buck converter. The feedback compensation parameters used in the previous buck converter example are modified to yield a marginally stable case. Figure 7.11 shows the loop gain curves of the buck converter. The Bode plot in Fig. 7.11(a) indicates that $|T_m| =$ 0 dB and $\angle T_m = -180°$ at the frequency $f_c = 2$ kHz. Figure 7.11(b) shows that the polar plot traverses the critical $(-1, 0)$ point. Thus, the buck converter is

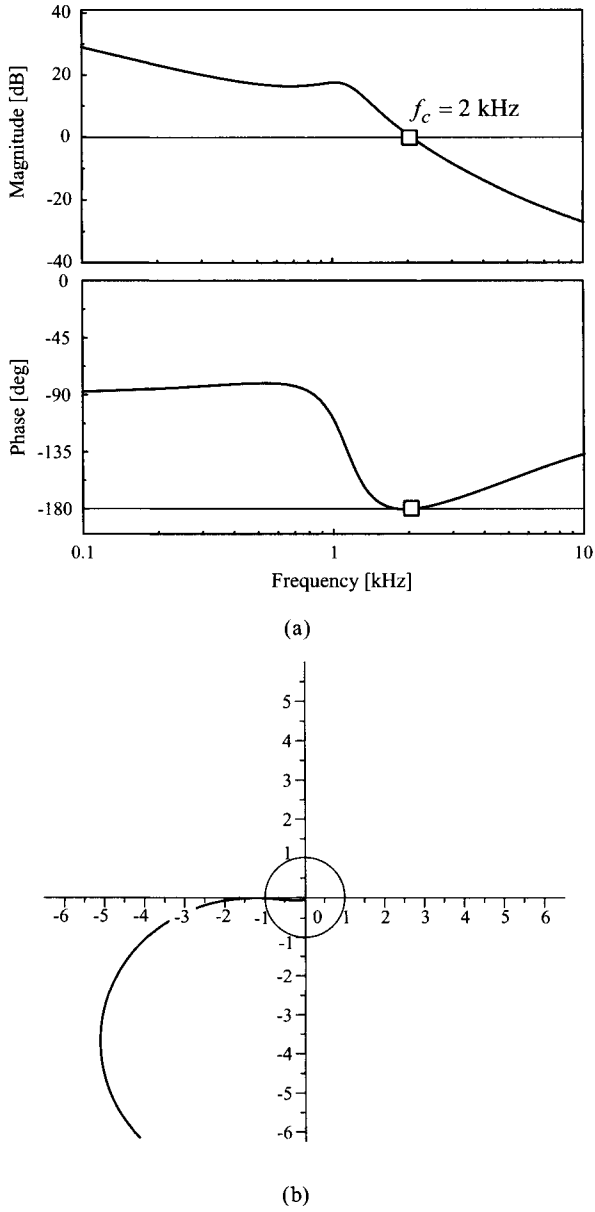


Figure 7.11 Loop gain of marginally stable buck converter. (a) Bode plot of loop gain. (b) Polar plot of loop gain.

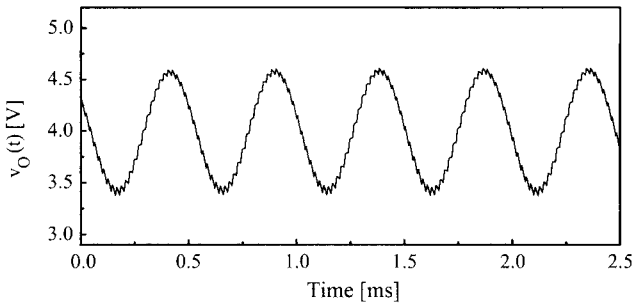


Figure 7.12 Output voltage of marginally stable buck converter.

marginally stable according to the definition of stability. Furthermore, the loop gain indicates that

$$\begin{aligned} T_m(j\omega_c) &= T_m(j2\pi f_c) = T_m(j2\pi \cdot 2 \times 10^3) \\ &= 1\angle -180^\circ = -1 \end{aligned} \tag{7.15}$$

which is rearranged as

$$1 + T_m(j2\pi \cdot 2 \times 10^3) = 0 \tag{7.16}$$

Equation (7.16) implies that $s = j2\pi \cdot 2 \times 10^3$ is one root of the characteristic equation. Then, $s = -j2\pi \cdot 2 \times 10^3$ becomes another root of the characteristic equation. With a pair of poles at $s = \pm j2\pi \cdot 2 \times 10^3$, the buck converter would reveal a sustained oscillation at the frequency $\omega_c = 2\pi \cdot 2 \times 10^3$ rad/s.

Figure 7.12 is the output voltage of the converter, which indeed oscillates at the expected frequency $\omega_c = 2\pi \cdot 2 \times 10^3$ rad/s, or equivalently with the period $t_{os} = 2\pi/\omega_c = 0.5$ ms. This example again confirms that the classical stability theory, when applied to the s-domain small-signal model, accurately predicts the dynamics of the nonlinear time-variant dc-to-dc converters.

■ EXAMPLE 7.7 Conditionally Stable System

This example illustrates the potential problem of a conditionally stable system. A conditionally stable system exhibits stability at the given operating point. However, when the operating point is altered, the conditionally stable system could become unstable. This destabilizing effect could take place in real applications and threaten the system operation.

Figure 7.13(a) shows a family of loop gain plots for a conditionally stable system under the assumption that the magnitude of the loop gain is successively decreased, while its phase characteristics remain unchanged. As shown in this figure, the decrease in the loop gain magnitude results in a contraction in the polar plot. The contraction in the polar plot in turn incurs the encirclement of

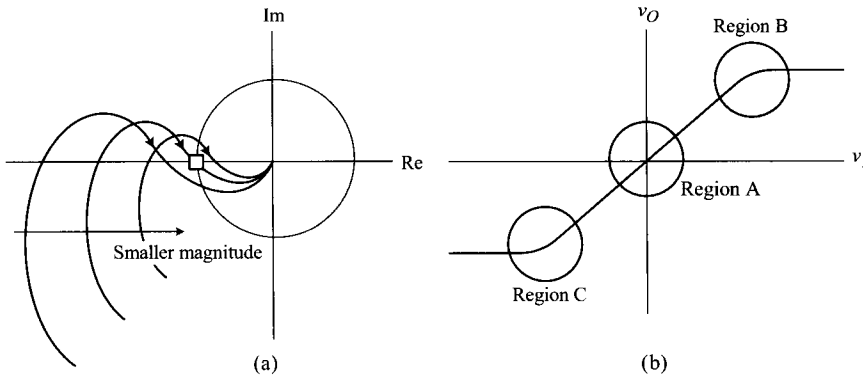


Figure 7.13 Problem of conditionally stable system. (a) Loop gain of conditionally stable system. (b) Input-to-output characteristics of practical amplifier.

the $(-1, 0)$ point. Thus, a conditionally stable system becomes unstable when the loop gain magnitude is unduly lessened.

Most closed-loop controlled systems employ an amplifier in their feedback path. For this case, the loop gain magnitude can inadvertently be decreased when the operating point shifts from the initial position. Figure 7.13(b) shows the input-output transfer characteristics of a practical amplifier which encounters saturations when the operating point is moved largely away from the origin. The slope of the input-output transfer curve is the incremental gain of the amplifier. With the initial operating point lying in Region A, the incremental gain of the amplifier is large. However, when the operating point shifts towards Region B or Region C, the amplifier starts being saturated. Consequently, the slope of the input-output curve will be decreased, resulting in considerable decline in the loop gain magnitude. The reduction in gain could destabilize the system as explained earlier. This unstable shift in the operating point could readily occurs when the operational conditions undergo large fluctuations during the start-up procedures, protective operations, or large-scale load/input changes.

Most stable systems also become unstable when the magnitude of the loop gain is sufficiently increased so that the polar plot stretches out to encircle the $(-1, 0)$ point. This would occur when the amplifier gain is overly increased. However, such a large gain increase will not take place in practice because the maximum allowable gain of the amplifier is mostly limited by the amplifier design. Thus, unlike the case for conditionally stable systems, the destabilizing effect of the gain increase in stable systems will not be a real problem.

7.6 RELATIVE STABILITY: GAIN MARGIN AND PHASE MARGIN

Stability is the most important issue for any closed-loop controlled dynamic systems. Accordingly, we are concerned with the absolute stability – we primarily want to

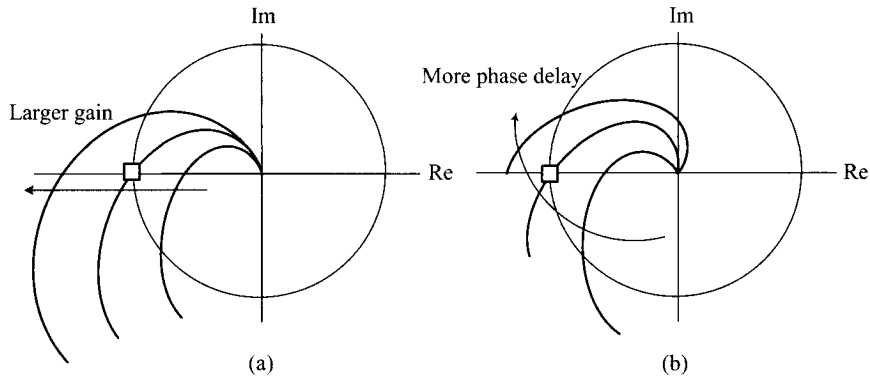


Figure 7.14 Destabilizing effect of gain increase and phase delay. (a) Increase in gain. (b) Increase in phase delay.

know whether the system is currently stable or not. In addition to the absolute stability, it is also important to know the *firmness* of stability. We may want to know 1) how easily a currently stable system could become unstable or 2) whether one system is more or less stable than the other system.

The absolute stability is determined by applying the Nyquist criterion to the loop gain. The polar plot of a stable loop gain does not encircle the $(-1, 0)$ point. However, the increase either in the loop gain magnitude or in the phase delay would cause the polar plot to violate the Nyquist stability criterion. Figure 7.14 shows the effects of these increases on the polar plot.

1) An increase in gain with a fixed phase delay results in a proportional expansion of the polar plot. As shown in Fig. 7.14(a), a continuous gain increase eventually ends up with the encirclement of the $(-1, 0)$ point, thus making the system unstable.

2) An increase in phase delay with a fixed gain causes a clockwise rotation of the polar plot. An excessive phase delay also brings in the encirclement of the $(-1, 0)$ point, as shown in Fig. 7.14(b).

Because the increase in the loop gain magnitude or in the phase delay could destabilize the system, the relative stability needs to be specified by two separate margins, the gain margin and the phase margin.

Gain Margin: The gain margin is the amount of gain increase that can be added to $|T_m|$ before a stable system becomes marginally stable or unstable, with the assumption that phase characteristics remain the same. Figure 7.15 is an illustration of the gain margin. Figure 7.15(a) indicates that the polar plot currently crosses the $(-0.5, 0)$ point. The polar plot will pass the $(-1, 0)$ point, as shown with the thick line, when the loop gain magnitude is doubled. For this case, the gain margin is given by $20 \log 2 \approx 6$ dB. Figure 7.15(b) is the Bode

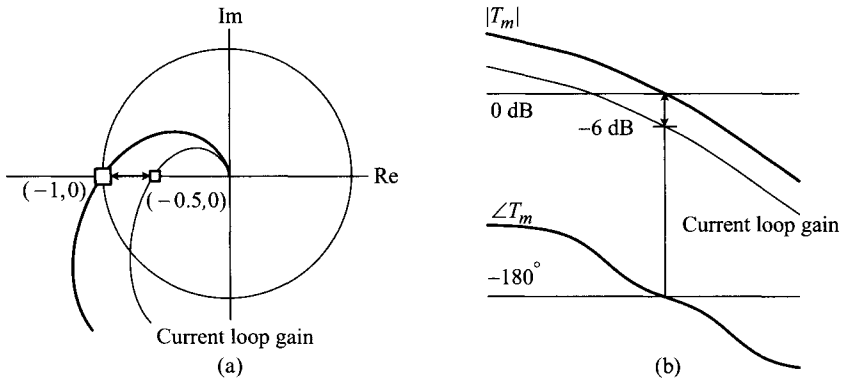


Figure 7.15 Gain margin representation. (a) Polar plot. (b) Bode plot.

plot of the same loop gain. It can be inferred that $|T_m|$ should be −6 dB at the frequency where $\angle T_m$ falls to −180° so that the Bode plot also predicts a 6 dB gain margin. In other words, when $|T_m|$ is raised by 6 dB as shown with the thick line, the system confronts the condition $|T_m| = 0$ dB with $\angle T_m = -180°$, which implies the polar plot passing the $(-1, 0)$ point.

Phase Margin: The phase margin denotes the amount of phase delay that can be added to $\angle T_m$ with fixed $|T_m|$, while retaining stability. Figure 7.16 shows the loop gain plots with a 45° phase margin. Figure 7.16(a) indicates that the polar plot crosses the unit circle with a −135° phase angle. When the polar plot is rotated by 45° in the clockwise direction, the polar plot passes the $(-1, 0)$ point and the system loses stability. Figure 7.16(b) shows that $\angle T_m$ becomes −135° when $|T_m|$ curve crosses the 0 dB line. If $\angle T_m$ is lowered by 45°, the loop gain again encounters the condition $|T_m| = 0$ dB with $\angle T_m = -180°$ and the system thus becomes marginally stable.

The gain margin and phase margin, individually shown in Figs. 7.15 and 7.16, are simultaneously displayed on the loop gain plots in Fig. 7.17. Figure 7.17(a) depicts the gain margin and phase margin on the polar plot.

1) **Gain margin, GM = 20 log(1/k):** The gain margin specifies to the distance between the $(-1, 0)$ point and the point at which the polar plot passes the − real axis. When the polar plot crosses the $(-k, 0)$ point, the gain margin is given by $20 \log(1/k)$.

2) **Phase margin, PM:** The phase margin denotes the angle measured between the − real axis and the line stretched from the origin to the point at which the polar plot intersects the unit circle.

Figure 7.17(b) illustrates the gain margin and phase margin on the Bode plot.

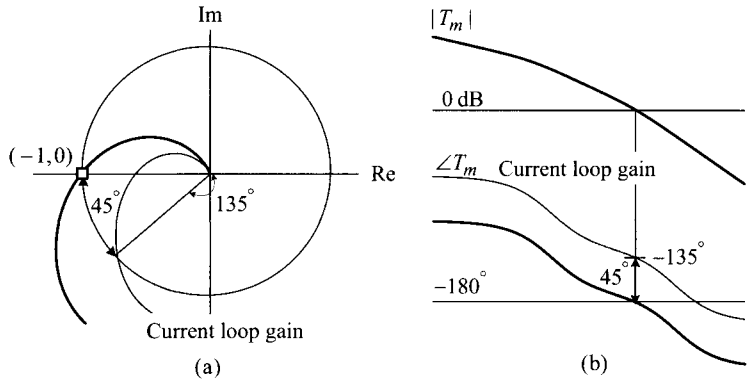


Figure 7.16 Phase margin representation. (a) Polar plot. (b) Bode plot.

1) **Gain margin GM:** The gain margin is the difference between 0 dB and $|T_m|$ evaluated at the frequency where $\angle T_m$ falls to $-180°$.

2) **Phase margin PM:** The phase margin corresponds to the difference between $-180°$ and $\angle T_m$ evaluated at the frequency where $|T_m|$ reduces to 0 dB.

It is easily inferred from Fig. 7.17 that both the gain margin and phase margin reduce to zero for marginally stable systems and become negative for unstable systems.

Although the stability margins are originally intended to quantify the relative stability, they also serve as criteria for the frequency- and time-domain performance of closed-loop controlled systems. The relationship between the stability margins and dynamic performance is based on the following arguments. From the definition of the relative stability, it is evident that the stability margins account for the nearness

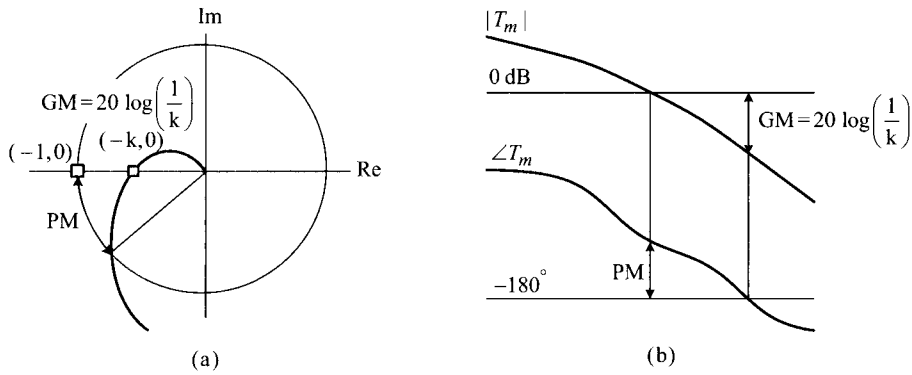


Figure 7.17 Gain margin and phase margin representation. (a) Polar plot. (b) Bode plot.

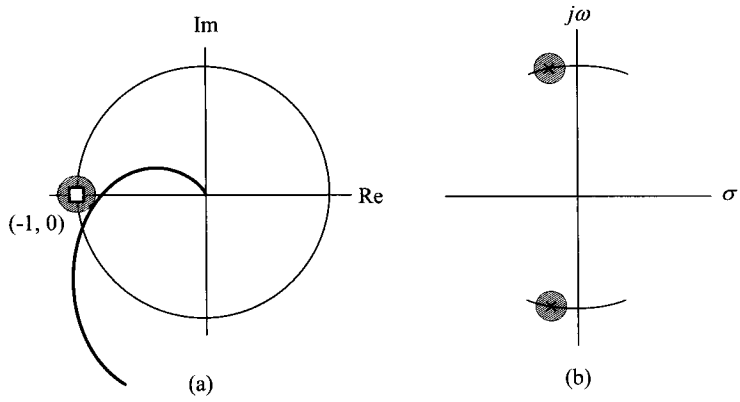
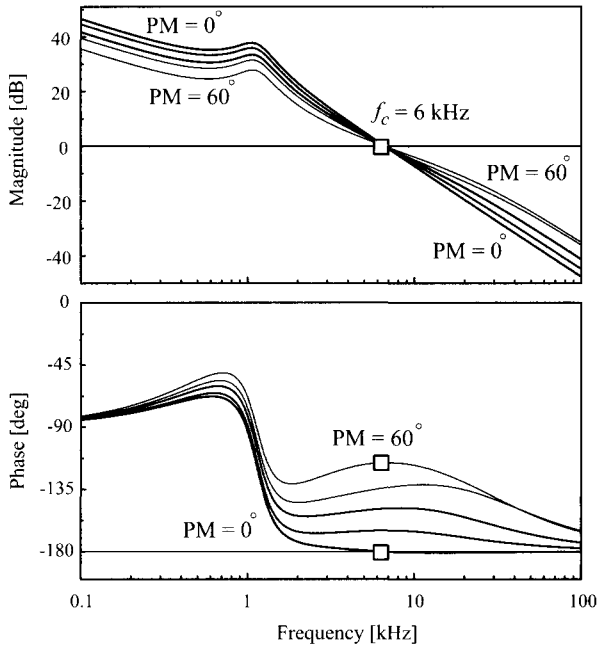


Figure 7.18 System with small stability margins. (a) Polar plot. (b) Pole location.

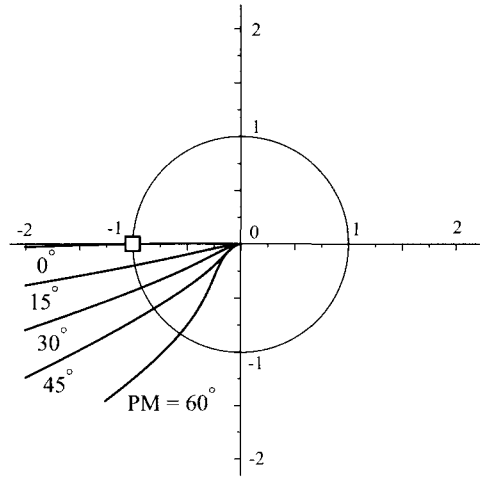
of the polar plot to the $(-1, 0)$ point. When the polar plot passes the $(-1, 0)$ point, the system is marginally stable and the stability margins reduce to zero. For this case, the system has a pair of poles on the imaginary axis, as demonstrated in Example 7.6. When the polar plot bypasses the $(-1, 0)$ point, in close proximity to but not encircling the $(-1, 0)$ point, the system is barely stable with small stability margins. For this case, the system poles locate near the imaginary axis although they are in the LHP of s-plane. This situation is illustrated in Fig. 7.18.

The position of the system poles influences both the frequency- and time-domain performance. First, the poles located nearby $s = \pm j\omega_c$ points induce a peaking at the frequency ω_c in s-domain transfer functions. The nearer the poles to $s = \pm j\omega_c$ points, the larger the peaking at ω_c in transfer functions. When the system poles are located at $s = \pm j\omega_c$ points, the peaking becomes infinite. Proof of these statements can be found in most textbooks on control theory or circuit analysis. Second, the pole location affects the transient behavior of time-domain responses. As demonstrated in Example 7.6, the poles located at $s = \pm j\omega_c$ points cause a sustained oscillation. The period of this oscillation is given by $t_{os} = 2\pi/\omega_c$. When the poles are located in the LHP neighborhood of $s = \pm j\omega_c$ points, the system exhibits a decaying sinusoidal oscillation at the period of $t_{os} = 2\pi/\omega_c$.

The peaking in transfer functions or oscillation in transient responses worsen the closed-loop performance of the system. These detrimental effects become more pronounced as the poles move closer to the imaginary axis, or equivalently the stability margins become smaller. Accordingly, the stability margins can be considered as a barometer for the frequency- and time-domain performance. For this reason, the lower limits of the stability margins are recommended for acceptable closed-loop performance. As a rule of thumb, a 45° limit is generally accepted for the phase margin, while a 12 dB threshold is adopted for the gain margin.



(a)



(b)

Figure 7.19 Loop gains with different phase margins. (a) Bode plot. (b) Polar plot.

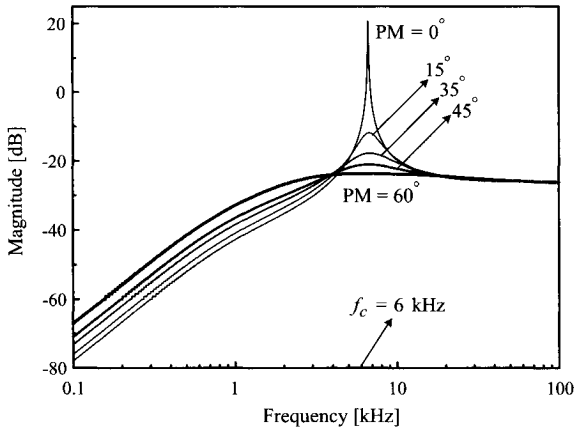


Figure 7.20 Output impedance with different phase margins.

■ EXAMPLE 7.8 Phase Margin and Closed-Loop Performance

This example illustrates the consequences of a small phase margin on the dynamic performance of the buck converter used in the previous examples. Figure 7.19(a) shows the Bode plots of the converter loop gain. For this example, the feedback compensation is selected to produce five different phase margins, decreasing successively from PM = 60° to 0° by a 15° step, while maintaining the 0 dB crossover frequency at f_c = 6 kHz. Figure 7.19(b) shows the loop gains displayed in the polar plot format. The decrease in the phase margin is evident in the polar plot.

Figure 7.20 shows the output impedances of the converter with the five different phase margins. When the phase margin is lower than 60°, the output impedance shows a peaking due to the nearness of the system poles to the imaginary axis. The peaking occurs at the loop gain crossover frequency, f_c = 6 kHz. The magnitude of the peaking is inversely proportional to the phase margin – the smaller the phase margin, the nearer the system poles to the imaginary axis and the larger the peaking. In fact, there is an exact relationship between the magnitude of the peaking, |peaking|, and the phase margin, PM

$$|\text{peaking}| = 20\log\left(\frac{1}{\sqrt{2-2\cos \text{PM}}}\right) \tag{7.17}$$

This expression will be discussed in detail in Section 8.4.4.

Finally, Fig. 7.21 shows the transient responses of the output voltage v_O due to a step change in the load current: I_O = 4 A ⇒ 2 A. As the phase margin is lessened, the transient response becomes increasingly oscillatory until it develops a full oscillation with PM = 0°. The frequency of the transitional or

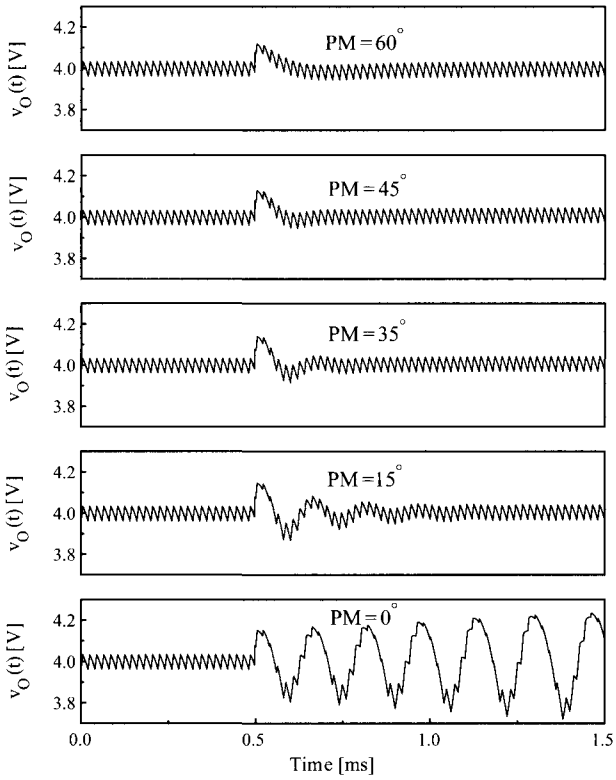


Figure 7.21 Step load response of output voltage v_O with different phase margins.

sustained oscillation coincides with the loop gain crossover frequency: $\omega_{os} = 2\pi \cdot 6 \times 10^3$ rad/s $\Rightarrow$ $t_{os} = 1/6 \times 10^3 = 0.17$ ms.

7.7 SUMMARY

Dc-to-dc converters are intended to function as a voltage source that resembles the ideal voltage source as closely as possible. Accordingly, a dc-to-dc converter is required to possess certain properties as its dynamic performance.

1) A dc-to-dc converter should establish a periodic steady-state operation, thereby producing a predetermined output voltage. In addition, when perturbed by certain external or internal disturbances, the converter should return to the original operating point.

2) A dc-to-dc converter should maintain the output voltage as cleanly as possible in the presence of the high-frequency noises or sinusoidal variations either in the input voltage or load current.

3) A dc-to-dc converter should minimize the fluctuation in the output voltage in response to sudden changes in the load current or input voltage.

The first property among these three items is defined as the stability of the dc-to-dc converter. The second requirement is quantified by the audio-susceptibility or output impedance. Finally, the third aspect is specified by the step load response or step input response. This chapter presented practical examples to illustrate the implication and importance of these performance criteria.

We demonstrated that all the aforementioned criteria can be analyzed using the conventional control theory or circuit analysis techniques. The s-domain small-signal model of dc-to-dc converters is the instrumental tool that links the conventional techniques, originally developed for linear systems, to the dynamic analysis of nonlinear time-variant dc-to-dc converters. While the dynamic analysis of dc-to-dc converters can mostly be performed in the exact same manner as that of linear time-invariant systems, the results should be interpreted based on the assumptions and limitations of the small-signal analysis; that is, the analysis results are only valid when dc-to-dc converters do not significantly depart from the initial operating point.

This chapter provided a selective summary of the classical control theory, in preparation for upcoming details about the converter dynamic analysis. The current chapter reviewed the Nyquist stability criterion and presented the loop gain analysis using both the polar plot and Bode plot. The implication and significance of stability margins are addressed. The role of the stability margins as the performance index for dc-to-dc converters is emphasized. While this chapter highlighted theoretical essentials, further details about the classical control theory can be found in most standard textbooks.

REFERENCES

1. K. Ogata, *Modern Control Engineering*, Prentice Hall, 4th Ed., 2002.
2. B. H. Cho and F. C. Lee, *VPEC Power Electronics Professional Seminar*, Course I–Control Design, VPEC, 1991.
3. R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, Kluwer Academic Publishers, 2001.
4. R. D. Middlebrook and S. Ćuk, *Advances in Switch-Mode Power Conversion*, TESLAco, Pasadena, CA, 1983.

PROBLEMS

7.1 Shown in Fig. P7.1 is the circuit diagram of a closed-loop controlled buck converter.

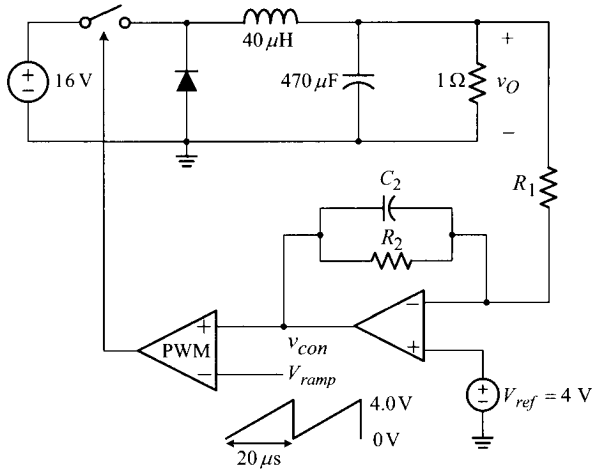


Fig. P7.1

a) Assume $R_1 = 10\ \text{k}\Omega$, $R_2 = 100\ \text{k}\Omega$, and $C_2 = 0$ and answer the questions.
i) Find the expression for the loop gain $T_m(s)$.
ii) Sketch the asymptotic plots for $|T_m|$ and $\angle T_m$.
iii) Find the average values for v_O and v_{con}.

b) Repeat **a)** for $R_1 = 10\ \text{k}\Omega$, $R_2 = \infty$, and $C_2 = 32\ \text{nF}$.

c) Repeat **a)** for $R_1 = 10\ \text{k}\Omega$, $R_2 = 100\ \text{k}\Omega$, and $C_2 = 32\ \text{nF}$.

7.2** Figure P7.2 is the Bode plot of the audio-susceptibility of a closed-loop controlled buck converter. The buck converter is operating at $f_s = 50$ kHz with the duty ratio $D = 0.25$. Assume that the audio-susceptibility is expressed as

$$A_u(s) = K_a s \frac{1}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)} \quad \text{with} \quad \omega_{p1} \ll \omega_{p2}$$

a) Use the relationship (7.6) to derive an analytical expression for the output voltage v_O when a step increase of V_{step} is occurred in the input voltage. Sketch the general shape of v_O. Show all the important information on your sketch.

b) Based on the information given in Fig. P7.2, estimate the parameters $\{K_a\ \omega_{p1}\ \omega_{p2}\}$ which appeared in the audio-susceptibility expression.

c) Use the results of **a)** and **b)** to find the numeric expression for v_O with $V_{step} = 2$ V.

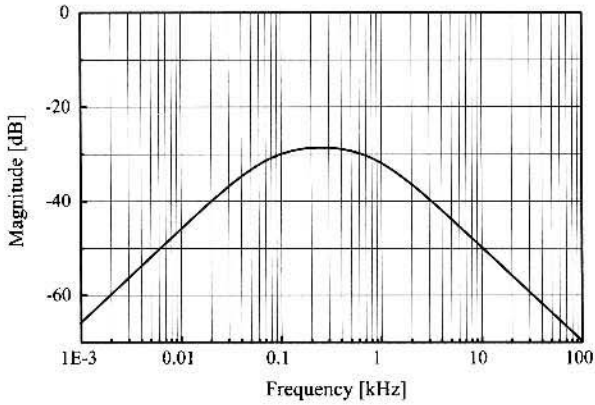


Fig. P7.2

d) Now assume that $v_S(t) = 12 + \sin 2\pi \cdot 20t$ is applied to the input of the converter. Find the expression for the output voltage while ignoring the switching ripple component.

7.3* Shown in Fig. P7.3 is the Bode plot of the output impedance of a closed-loop controlled buck converter. Assume that the output impedance is expressed by the equation

$$Z_o(s) = K_z s \frac{1}{1 + \frac{s}{\omega_p}}$$

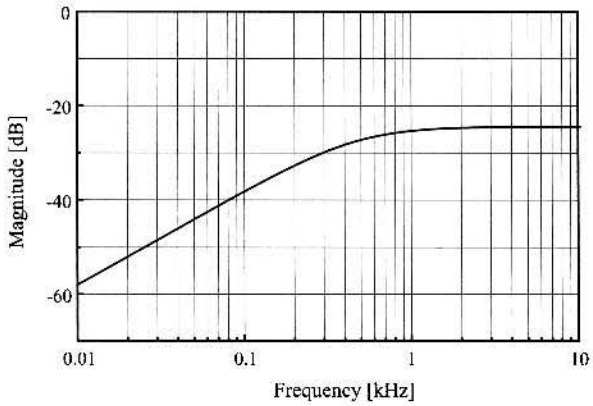


Fig. P7.3

a) Using the relationship (7.5), derive an analytic equation for the output voltage v_O when a step decrease of I_{step} occurred in the load current.

Sketch the general shape of v_O and show all the important information on your sketch.

b) Refer to the information given in the Bode plot to determine the parameters $\{K_z\ \omega_p\}$ used in the output impedance expression.

c) Using the results of **a)** and **b)**, find the numeric expression for v_O with $I_{step} = 2$ A.

7.4 Consider the following expressions as the output impedance of a closed-loop controlled buck converter.

i) $$Z_o(s) = K_z s \frac{1}{1 + \dfrac{s}{\omega_p}}$$

ii) $$Z_o(s) = K_z s \frac{1 + \dfrac{s}{\omega_z}}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)} \quad \text{with} \quad \omega_{p1} \ll \omega_z \ll \omega_{p2}$$

iii) $$Z_o(s) = K_z s \frac{1 + \dfrac{s}{\omega_z}}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)} \quad \text{with} \quad \omega_{p1} \ll \omega_{p2} \ll \omega_z$$

Now assume that a step decrease of I_{step} is occurred in the load current. For each of the above expressions, derive an analytic expression for the transient response of the output voltage v_O using the relationship (7.5). Also, sketch the general shape of the transitional output voltage.

7.5 Figure P7.5 is the magnitude plot of the loop gain $|T_m|$ and the load current-to-output transfer function $|Z_p|$ of a closed-loop controlled buck converter. As discussed in Section 7.2.3, the output impedance is expressed as

$$Z_o(s) = \frac{Z_p(s)}{1 + T_m(s)}$$

This relationship can be split into the approximations

$$Z_o(s) = \frac{Z_p(s)}{1 + T_m(s)} \approx \begin{cases} \dfrac{Z_p(s)}{T_m(s)} & \text{at frequencies where } |T_m| > 1 \\ Z_p(s) & \text{at frequencies where } |T_m| < 1 \end{cases}$$

to construct the asymptotic plot for $|Z_o|$.

a) Sketch the asymptotic plot of the output impedance $|Z_o|$. Label the corner frequency, slope, and peak value of $|Z_o|$.

b) Use the outcome of **a)** to find the expression for $Z_o(s)$.

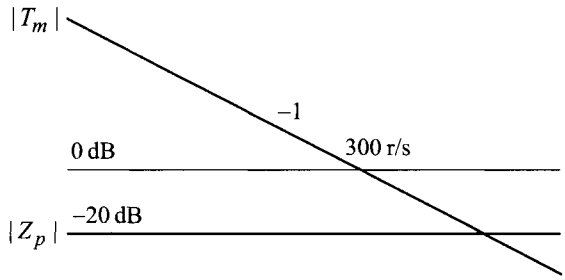


Fig. P7.5

c) Derive the equation for the output voltage v_O due to a 5 A step decrease in the load current. Sketch v_O and show the time constant and peak undershoot of v_O.

7.6** A composite system shown in Fig. P7.6 is configured using a voltage source and two two-port systems.

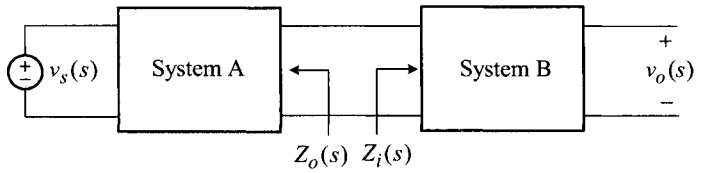


Fig. P7.6

a) Find the expression for the input-to-output transfer function of the composite system, $v_o(s)/v_s(s)$, in terms of the following transfer functions defined individually for System A and System B:
$F_A(s)$: the input-to-output transfer function of System A
$F_B(s)$: the input-to-output transfer function of System B
$Z_o(s)$: the output impedance of System A
$Z_i(s)$: the input impedance of System B

b) Assume that System A and System B are individually stable. Now argue that the stability of the composite system can be assessed by applying the Nyquist criterion to the impedance ratio $Z_o(s)/Z_i(s)$.

c) Derive a sufficient, but not necessary, condition to ensure the stability of the composite system.

d) State the condition which makes the composite system marginally stable.

7.7* The Bode plot shown in Fig. P7.7 is the loop gain of a closed-loop controlled dc-to-dc converter.

a) Determine the stability of the converter. Evaluate the gain margin (positive or negative), phase margin (positive or negative), and 0 dB crossover frequency of the loop gain.

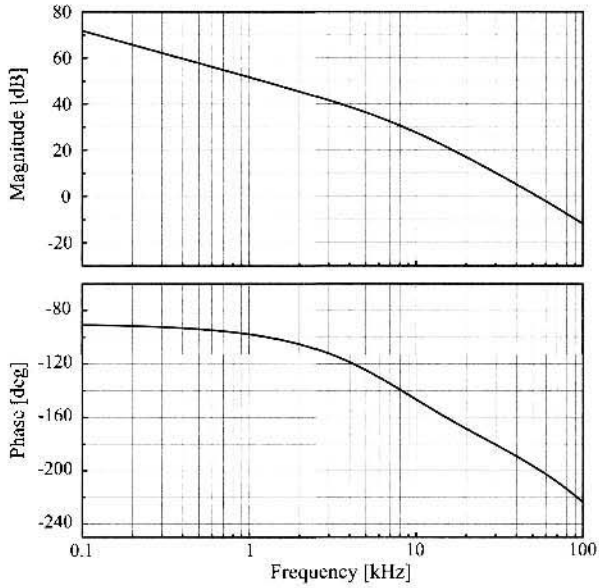


Fig. P7.7

b) You are only allowed to change the magnitude of the voltage feedback compensation to meet the following design objectives:
i) stability with the phase margin in the neighborhood of 20°,
ii) stability with the phase margin in the neighborhood of 60°, and
iii) stability with the gain margin in the neighborhood of 20 dB
What would you do to achieve each of the design specifications above?

7.8** Figure P7.8 is the polar plot of the loop gain of a PWM dc-to-dc converter.

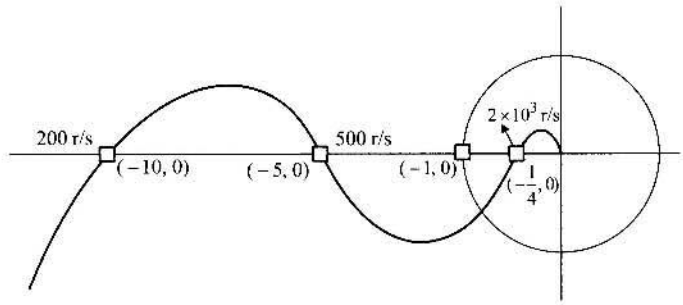


Fig. P7.8

a) Determine the stability of the converter.
b) The gain of the voltage feedback compensation is currently $K_v = 100$. Now assume that the gain is varied between $1 < K_v < 500$, while other

compensation parameters remain the same. Under this condition, find the range(s) of K_v in which the converter remains stable.

c) What would happen to the converter output when the magnitude of the current feedback gain, $K_v = 100$, is changed to $K_v = 10$, $K_v = 20$, and $K_v = 400$?

7.9** Shown in Fig. P7.9 is the polar plot for the loop gain of a closed-loop controlled dc-to-dc converter.

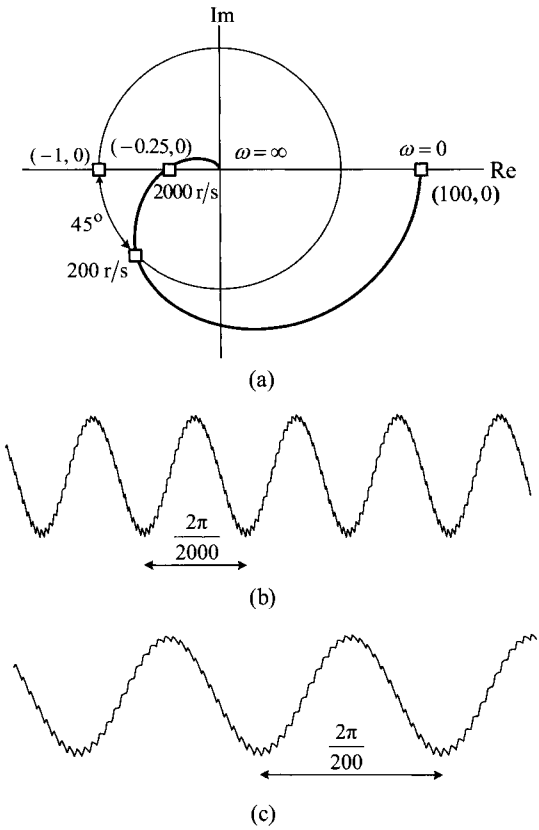


Fig. P7.9

a) Determine the stability of the converter. Evaluate the gain margin, phase margin, and 0 dB crossover frequency of the loop gain.

b) Convert the polar plot into the Bode plot for $|T_m|$ and $\angle T_m$. Show all the prominent features on the Bode plot.

c) Assume that the converter produces the output voltage waveform shown in Fig. P7.9(b). What do you think happened to the voltage feedback compensation of the converter?

d) Now assume that the converter output generates the waveform in Fig. P7.9(c). What do you think occurred in voltage feedback compensation?

7.10** Figure P7.10 is the Bode plot of the loop gain of a closed-loop controlled buck converter.

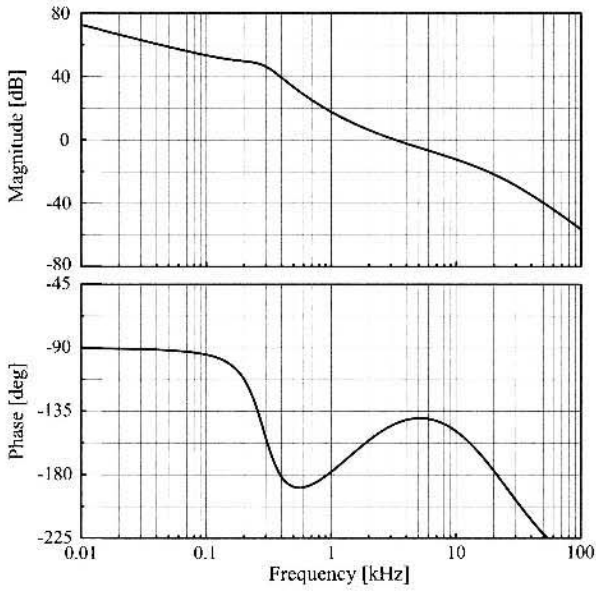


Fig. P7.10

a) Determine the stability of the converter.

b) Convert the Bode plot into the polar plot. Show all the prominent features of the loop gain on the polar plot.

c) Assume that the gain of the voltage feedback compensation is $K_v = 10^3$ for the current design. Now assume that the gain is varied between $1 < K_v < 10^5$. Find the range(s) of K_v which secure(s) the stability of the converter.

7.11** A marginally stable system shows unique characteristic features in the closed-loop performance. Describe or illustrate the characteristic feature(s) in the following closed-loop performance of a marginally stable system. For the definiteness of your argument, assume that 0 dB crossover frequency of the loop gain occurs at $\omega = \omega_c$.

i) Polar plot of loop gain
ii) Bode plot of loop gain
iii) Pole location in s-plane
iv) Time-domain waveforms
v) Closed-loop transfer functions

CHAPTER 8

CLOSED-LOOP PERFORMANCE AND FEEDBACK COMPENSATION

The dynamic performance of closed-loop controlled dc-to-dc converters is solely determined by the feedback controller. The ultimate goal of the small-signal modeling and dynamic analysis is to develop systematic procedures that allow us to design the feedback controller for optimal dynamic performance. This chapter covers the dynamic analysis and control design, and provides step-by-step design guidelines to achieve optimal closed-loop performance for PWM dc-to-dc converters.

The dynamic performance includes the loop gain, frequency-domain transfer functions, and time-domain transient responses. These performance criteria are closely related to each other and thus must be considered collectively when designing the voltage feedback compensation. Accordingly, the first step towards a successful controller design is to understand the relationships among various performance criteria and to analyze the impacts of the voltage feedback compensation on these criteria. Once these issues have been resolved, it then becomes possible to develop design principles for the voltage feedback compensation.

This chapter covers the dynamic analysis and feedback design of closed-loop controlled PWM dc-to-dc converters. The first two sections analyze the dynamic performance focusing on the relationship between the loop gain and frequency-domain performance criteria. The mid-portion of this chapter deals with the design

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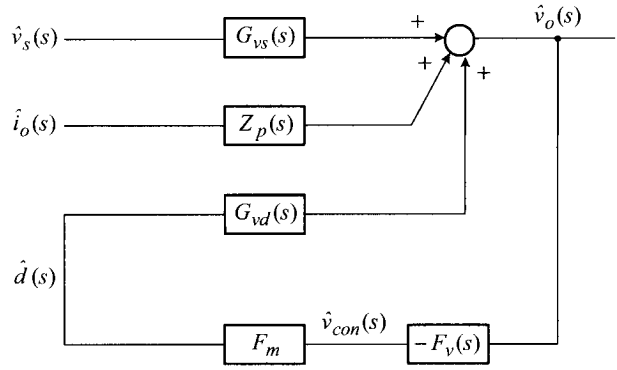


Figure 8.1 Small-signal block diagram of PWM converter.

of the voltage feedback compensation. The desired structure for the voltage feedback circuit is identified and step-by-step design guidelines for the compensation parameters are presented. Later sections illustrate the impacts of the voltage feedback compensation on the frequency- and time-domain performance.

The graphical asymptotic analysis method is used as an instrumental tool for the closed-loop analysis and feedback compensation design. The concept and examples of the asymptotic analysis are introduced in the first section of this chapter. The asymptotic analysis method is then used in the forthcoming sections to illustrate the outcomes of the closed-loop analysis, design of voltage feedback compensation, and impacts of the feedback compensation on the converter performance.

8.1 ASYMPTOTIC ANALYSIS METHOD

This section provides an analytical basis for the asymptotic analysis method. The motivation and concept of the asymptotic analysis are first introduced. Practical details about the proposed method then follow.

8.1.1 Concept of Asymptotic Analysis Method

As discussed in Chapter 7, the frequency-domain performance includes the loop gain, audio-susceptibility, and output impedance. This section presents a systematic approach to analyzing these performance criteria. The proposed approach is referred to as the asymptotic analysis method because it uses the asymptotic expressions of the transfer functions as the basis for the analysis.

Figure 8.1 shows the small-signal block diagram of a closed-loop controlled dc-to-dc converter. The gain block F_m is the PWM gain, $F_v(s)$ is the voltage feedback compensation, and the other small-signal gain blocks denote the power stage transfer

functions. From Fig. 8.1, the loop gain is determined as

$$T_m(s) = -\frac{\hat{v}_o(s)}{\hat{d}(s)}\frac{\hat{v}_{con}(s)}{\hat{v}_o(s)}\frac{\hat{d}(s)}{\hat{v}_{con}(s)} = (-)G_{vd}(s)(-)F_v(s)F_m = G_{vd}(s)F_v(s)F_m \tag{8.1}$$

The application of Mason's gain rule to Fig. 8.1 yields the expressions for the frequency-domain performance criteria. The audio-susceptibility is given by

$$A_u(s) = \left.\frac{\hat{v}_o(s)}{\hat{v}_s(s)}\right|_{\text{closed}} = \frac{G_{vs}(s)}{1 + T_m(s)} \tag{8.2}$$

If the small-signal gain blocks are all known, the expression (8.2) can be used to find an equation for the audio-susceptibility. However, this *direct method* would not yield any useful results that can readily be adapted to the feedback compensation design.

As an alternative to the direct method, an asymptotic analysis method is used to simplify the analysis and, more importantly, to obtain design information. The expression (8.2) is split into two asymptotic approximations

$$A_u(s) = \frac{G_{vs}(s)}{1 + T_m(s)} \approx \begin{cases} \dfrac{G_{vs}(s)}{T_m(s)} & \text{at frequencies where } |T_m| \gg 1 \\ G_{vs}(s) & \text{at frequencies where } |T_m| \ll 1 \end{cases} \tag{8.3}$$

For most practical converters, $|T_m|$ is very large at low frequencies, crosses the 0 dB line at mid-frequencies, and continuously decreases at high frequencies. Thus, the 0 dB crossover frequency of the loop gain serves as the borderline for the asymptotic approximation: $A_u(s) \approx G_{vs}(s)/T_m(s)$ at frequencies before the 0 dB crossover frequency and $A_u(s) \approx G_{vs}(s)$ thereafter.

The asymptotic approximation of (8.3) is combined with the graphical Bode plot analysis technique. The resulting analysis method will be referred to as the *asymptotic analysis method.* The asymptotic analysis method explicitly shows the impacts of the voltage feedback compensation on the audio-susceptibility $A_u(s)$, thereby providing easy and clear design information. This method does not require any complicated analytical treatments and quickly yields the expression for $A_u(s)$ in a factorized form. For most cases, a factorized expression for $A_u(s)$ can immediately be written by inspection.

The expression for the output impedance is found from Fig. 8.1 and put into the asymptotic approximation

$$Z_o(s) = \left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\text{closed}} = \frac{Z_p(s)}{1 + T_m(s)} \approx \begin{cases} \dfrac{Z_p(s)}{T_m(s)} & \text{at frequencies where } |T_m| \gg 1 \\ Z_p(s) & \text{at frequencies where } |T_m| \ll 1 \end{cases} \tag{8.4}$$

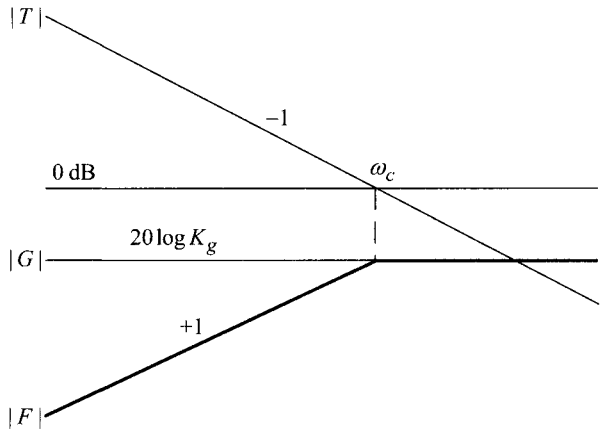


Figure 8.2 Asymptotic analysis for Case A.

for the asymptotic analysis. Because the expressions (8.3) and (8.4) have the same structure, the asymptotic analysis method can consistently be applied to both the audio-susceptibility and output impedance.

8.1.2 Examples of Asymptotic Analysis Method

Details about the asymptotic analysis are illustrated using the following equation

$$F(s) = \frac{G(s)}{1+T(s)} \approx \begin{cases} \dfrac{G(s)}{T(s)} & \text{at frequencies where } |T| \gg 1 \\ G(s) & \text{at frequencies where } |T| \ll 1 \end{cases} \tag{8.5}$$

with simple expressions for $G(s)$ and $T(s)$. Three different cases are considered to provide practical insights on the asymptotic analysis method.

Case A: $G(s) = K_g < 1$ and $T(s) = \dfrac{\omega_c}{s}$

As the simplest example, a constant is used for $G(s)$ while a single integration function is assumed for $T(s)$: $G(s) = K_g < 1$ and $T(s) = \omega_c/s$. Figure 8.2 illustrates the construction of the asymptotic plot for $|F|$ with the given $G(s)$ and $T(s)$. As previously discussed, the 0 dB crossover frequency of $|T|$, denoted as ω_c in Fig. 8.2, becomes the boundary for the approximations. For frequencies beyond ω_c, $|F|$ follows $|G|$. For frequencies below ω_c, $|F|$ is formed by subtracting $|T|$ from $|G|$ because the division in the linear scale corresponds to the subtraction in the log scale. As shown in Fig. 8.2, the ascending slope and corner frequency of $|F|$ are readily determined from the graphical analysis.

The asymptotic plot of $|F|$ is transformed into an analytic equation for $F(s)$

$$F(s)_{\text{asym}} = K_f s \frac{1}{1 + \dfrac{s}{\omega_c}} \tag{8.6}$$

by applying the inverse process of the Bode plot construction, as discussed in Section 6.1.4. The value for the leading coefficient K_f is found by equating $|F_{\text{asym}}|$ at ω_c to $|G|$

$$\begin{aligned} \left|F(s)_{\text{asym}}\right|_{s=j\omega_c} &= |K_f s|_{s=j\omega_c} = |K_f \omega_c| = |G| \\ &\Rightarrow \quad 20\log(K_f \omega_c) = 20\log K_g \end{aligned} \tag{8.7}$$

to yield the relationship

$$K_f\, \omega_c = K_g \tag{8.8}$$

The desired expression for K_f is obtained from (8.8)

$$K_f = \frac{K_g}{\omega_c} \tag{8.9}$$

resulting in the expression

$$F(s)_{\text{asym}} = \frac{K_g}{\omega_c} s \frac{1}{1 + \dfrac{s}{\omega_c}} \tag{8.10}$$

On the other hand, the direct evaluation of the left-hand side expression of (8.5) with $G(s) = K_g$ and $T(s) = \omega_c / s$ offers the exact equation for $F(s)$

$$F(s)_{\text{exec}} = \frac{K_g}{1 + \dfrac{\omega_c}{s}} = \frac{K_g}{\omega_c} s \frac{1}{1 + \dfrac{s}{\omega_c}} \tag{8.11}$$

For this particular case, the asymptotic analysis is the same as the exact analysis: $F(s)_{\text{asym}} = F(s)_{\text{exec}}$. However, the sameness is due to the simple structure of $T(s)$ and is not always true for general cases.

Case B: $G(s) = \frac{K_g}{1+s/\omega_p}$ with $K_g > 1$ and $T(s) = \frac{\omega_c}{s}$

In this case, a low pass filter is considered for $G(s)$ while the single integrator is used for $T(s)$: $G(s) = K_g/(1 + s/\omega_p)$ and $T(s) = \omega_c/s$. Figure 8.3 shows the construction of the asymptotic plot for $|F|$.

The asymptotic plot for $|F|$ in Fig. 8.3 is transformed into a factorized equation for $F(s)$

$$F(s)_{\text{asym}} = K_f s \frac{1}{\left(1 + \dfrac{s}{\omega_p}\right)\left(1 + \dfrac{s}{\omega_c}\right)} \tag{8.12}$$

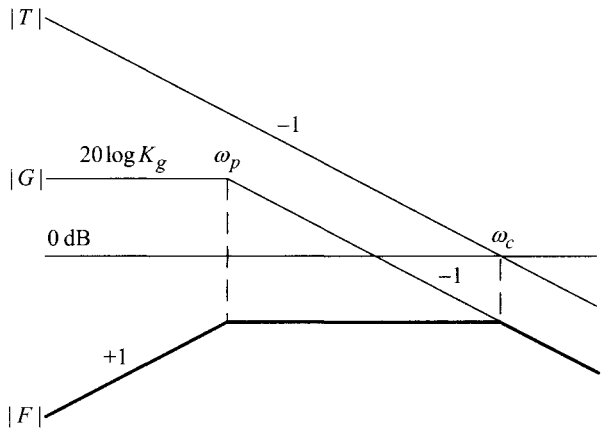


Figure 8.3 Asymptotic analysis for Case B.

The value for K_f is determined by evaluating the magnitude of $F(s)_{\text{asym}}$ at ω_p

$$\begin{aligned} \left|F(s)_{\text{asym}}\right|_{s=j\omega_p} &= |K_f s|_{s=j\omega_p} \\ &= |G(s)|_{s=j\omega_p} - |T(s)|_{s=j\omega_p} \end{aligned} \tag{8.13}$$

which is transformed to

$$K_f\,\omega_p = \frac{\dfrac{K_g}{\omega_c}}{\omega_p} \tag{8.14}$$

leading to the expression

$$K_f = \frac{K_g}{\omega_c} \tag{8.15}$$

On the other hand, the direct evaluation of the left-hand side expression of (8.5) with the given transfer functions produces the exact expression for the transfer function for $F(s)$

$$F(s)_{\text{exec}} = \frac{\dfrac{K_g}{1+\dfrac{s}{\omega_p}}}{1+\dfrac{\omega_c}{s}} = \frac{K_g}{\omega_c} s \frac{1}{\left(1+\dfrac{s}{\omega_p}\right)\left(1+\dfrac{s}{\omega_c}\right)} \tag{8.16}$$

which is identical to the result of the preceding asymptotic analysis.

From the procedures illustrated in Figs. 8.2 and 8.3, insights about the asymptotic analysis can be gained, leading to general analytical procedures for this graphical approach. The procedures and rules for the asymptotic analysis are discussed later in this section and the conclusions are summarized in Tables 8.1 and 8.2 at the end of this section.

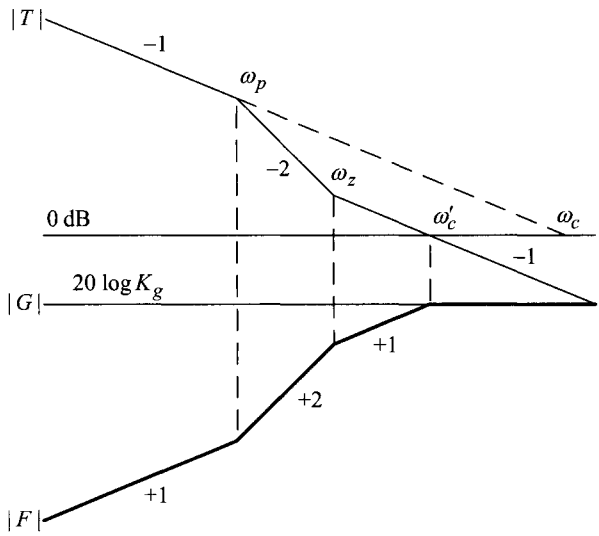


Figure 8.4 Asymptotic analysis for Case C.

Case C: $G(s) = K_g < 1$ and $T(s) = \frac{\omega_c}{s}\frac{1+s/\omega_z}{1+s/\omega_p}$ with $\omega_p < \omega_z$

As the last example, it is assumed that $G(s) = K_g < 1$ and $T(s) = (\omega_c/s)(1 + s/\omega_z)/(1 + \omega_p)$ with $\omega_p < \omega_z$. Figure 8.4 illustrates the construction of the asymptotic plot for $|F|$. The asymptotic plot is transformed into a factorized equation for $F(s)$

$$F(s)_{\text{asym}} = \frac{K_g}{\omega_c} s \frac{1 + \dfrac{s}{\omega_p}}{\left(1 + \dfrac{s}{\omega_z}\right)\left(1 + \dfrac{s}{\omega_c'}\right)} \tag{8.17}$$

based on the procedures in Table 8.2. The leading coefficient of (8.17) is determined using the same procedure as that of Case B. The direct evaluation of the left-hand side expression of (8.5) with the given $G(s)$ and $T(s)$ expressions yields

$$F(s)_{\text{exec}} = \frac{K_g}{1 + \dfrac{\omega_c}{s}\dfrac{1 + \dfrac{s}{\omega_z}}{1 + \dfrac{s}{\omega_p}}} = \frac{K_g}{\omega_c} s \frac{1 + \dfrac{s}{\omega_p}}{1 + \dfrac{s}{\omega_z} + \dfrac{s}{\omega_c} + \dfrac{s^2}{\omega_p \omega_c}} \tag{8.18}$$

By comparing (8.17) and (8.18), it becomes apparent that the asymptotic analysis is only an approximation to the exact evaluation. Even so, this approximation is practically accurate for the following reasons. First, the two equations have the

same leading coefficient and numerator. Because these terms determine the low-frequency characteristics, the two transfer functions will show the same behavior at low frequencies. Second, the high-frequency asymptote of the approximated equation $F(s)_{\text{asym}}$ is given by

$$|F(j\infty)_{\text{asym}}| = 20\log\left(\frac{K_g\,\omega_z\,\omega_c'}{\omega_c\,\omega_p}\right) \tag{8.19}$$

while that of the exact equation is given by

$$|F(j\infty)_{\text{exec}}| = 20\log\left(\frac{K_g}{\omega_c\,\omega_p}\omega_p\,\omega_c\right) = 20\log K_g \tag{8.20}$$

From the geometry of the asymptotic plot in Fig. 8.4, it can be shown that

$$\frac{\omega_z}{\omega_p} = \frac{\omega_c}{\omega_c'} \tag{8.21}$$

resulting in the relationship

$$|F(j\infty)_{\text{asym}}| = |F(j\infty)_{\text{exec}}| = 20\log K_g \tag{8.22}$$

which indicates that the high-frequency asymptotes of the two equations are also identical. The previous analysis concludes that the asymptotic approximation duplicates the exact equation at low and high frequencies, yet with some deviation in the mid-frequency range. This mid-frequency error is negligibly small for most cases.

■ EXAMPLE 8.1 Accuracy of Asymptotic Approximation

This example substantiates the accuracy of the asymptotic approximation. As an illustration, Case C in the previous three cases is selected with $G(s) = 0.01$ and

$$T(s) = \frac{4\times 10^4}{s}\,\frac{1+\dfrac{s}{400}}{1+\dfrac{s}{40}}$$

Figure 8.5 shows the Bode plot of the asymptotic approximation of (8.17) with $K_g = 0.01$, $\omega_c = 4\times 10^4$ rad/s, $\omega_c' = 4\times 10^3$ rad/s, $\omega_z = 400$ rad/s, and $\omega_p = 40$ rad/s, in comparison with that of the exact equation of (8.18). As predicted, the asymptotic approximation ideally matches with the exact equation at low and high frequencies, while showing only nearly-undetectable error in the mid-band. This confirms that the asymptotic analysis offers good accuracy and can generally be used for the closed-loop dynamic analysis of dc-to-dc converters.

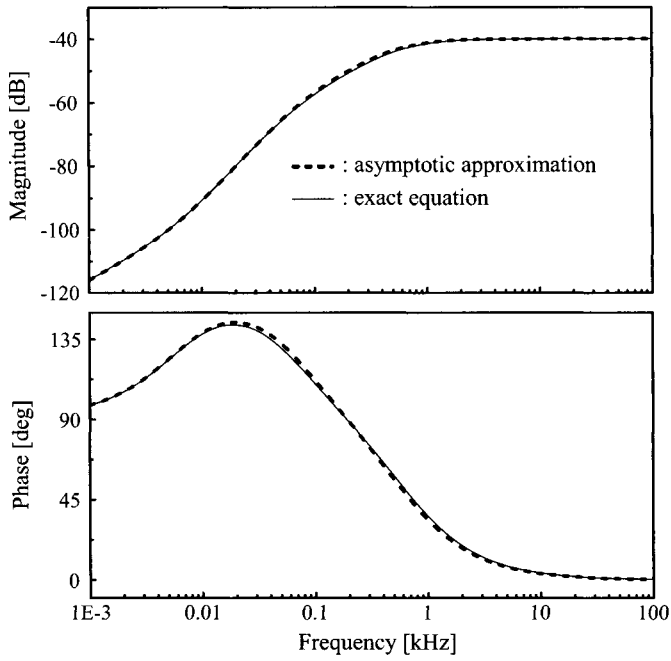


Figure 8.5 Accuracy of asymptotic approximation.

Procedures for Asymptotic Analysis

The graphical asymptotic analysis of $F(s) = G(s)/(1 + T(s))$ involves the following two steps.

1) The first step is to sketch the asymptotic plot for $|F(j\omega)| = |G(j\omega)|/|(1+T(j\omega))|$ for known $G(s)$ and $T(s)$ expressions.

2) The second step is to construct the $F(s)$ expression from the $|F(j\omega)|$ sketch obtained in the first step.

Tables 8.1 and 8.2 present the general rules for the asymptotic analysis. Table 8.1 illustrates the steps of sketching the asymptotic plot for $|F(j\omega)|$, while Table 8.2 summarizes the rules of writing the $F(s)$ expression from $|F(j\omega)|$ sketch. Readers are urged to review Tables 8.1 and 8.2 in preparation for upcoming details about the dynamic analysis and control design based on the asymptotic analysis.

8.2 FREQUENCY-DOMAIN PERFORMANCE

This section investigates the frequency-domain performance using the asymptotic analysis method. Relationships between the loop gain and closed-loop transfer functions are graphically illustrated. Factorized s-domain expressions for the transfer

Table 8.1 Procedures for $|F(j\omega)|$ Sketch

Basic equation
$F(s) = \dfrac{G(s)}{1+T(s)} \approx \begin{cases} \dfrac{G(s)}{T(s)} & \text{at frequencies where } \lvert T\rvert > 1 \\ G(s) & \text{at frequencies where } \lvert T\rvert < 1 \end{cases}$
Sketch rules for asymptotic plot of $\lvert F\rvert$
1) Sketch $\lvert G\rvert$ and $\lvert T\rvert$ for given equations.
2) Start sketching $\lvert F\rvert$ from high frequencies.
3) Sketch $\lvert F\rvert$ based on the following guidelines at different frequency ranges.
a) Frequencies beyond the 0 dB crossover frequency of $\lvert T\rvert$: $\lvert F\rvert$ duplicates $\lvert G\rvert$.
b) At the 0 dB crossover frequency of $\lvert T\rvert$: $\lvert F\rvert$ intersects with $\lvert G\rvert$.
c) Frequencies below the 0 dB crossover frequency of $\lvert T\rvert$: $\lvert F\rvert$ is constructed by subtracting $\lvert T\rvert$ from $\lvert G\rvert$. There is a simple relationship among the ascending and descending slopes of the transfer functions slope of $\lvert F\rvert$ = slope of $\lvert G\rvert$ − slope of $\lvert T\rvert$ For example, when $\lvert G\rvert$ decays with -1 slope and $\lvert T\rvert$ also declines with -1 slope, $\lvert F\rvert$ stays at a flat value with *zero* slope: $-1-(-1)=0$. Similarly, when $\lvert G\rvert$ ascends with $+1$ slope and $\lvert T\rvert$ descends with -1 slope, $\lvert F\rvert$ increases with $+2$ slope: $+1-(-1)=2$.

functions are provided. A closed-loop controlled buck converter is used as an illustrative example, nonetheless, the results can be extended to all PWM converters.

8.2.1 Audio-Susceptibility

Figure 8.6 shows the small-signal model of a closed-loop controlled buck converter. The input-to-output transfer function is found from Fig. 8.6

$$G_{vs}(s) = D\frac{1+\dfrac{s}{\omega_{esr}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}} \tag{8.23}$$

where

$$\omega_{esr} = \frac{1}{CR_c} \tag{8.24}$$

$$\omega_o \approx \sqrt{\frac{1}{LC}} \tag{8.25}$$

Table 8.2 Procedures for $F(s)$ Construction

Basic equation
$F(s) = K_f \frac{1}{s^{\pm j}} \frac{1}{1+\frac{s}{\omega_p}} \cdots \left(1+\frac{s}{\omega_z}\right) \cdots \frac{1}{1+\frac{s}{Q_p\omega_o}+\frac{s^2}{\omega_o^2}} \cdots \left(1+\frac{s}{Q_z\omega_o}+\frac{s^2}{\omega_o^2}\right) \cdots$
Construction rules for factorized equation of $F(s)$
1) Construct $F(s)$ in the time constant form.
2) Start writing the $F(s)$ expression from low-frequency terms.
3) Determine the poles and zeros for $F(s)$ from $\lvert F(j\omega)\rvert$ sketch. The poles and zeros appear at the frequencies where $\lvert F\rvert$ changes its slope. When the slope is changed by *one*, a single pole or single zero occurs. Similarly, when the slope is changed by *two*, a double pole or double zero appears.
4) Determine the value for the leading coefficient K_f. K_f can be determined from the low-frequency asymptote, high-frequency asymptote, 0 dB crossover frequency, or at one of corner frequencies of $\lvert F\rvert$.

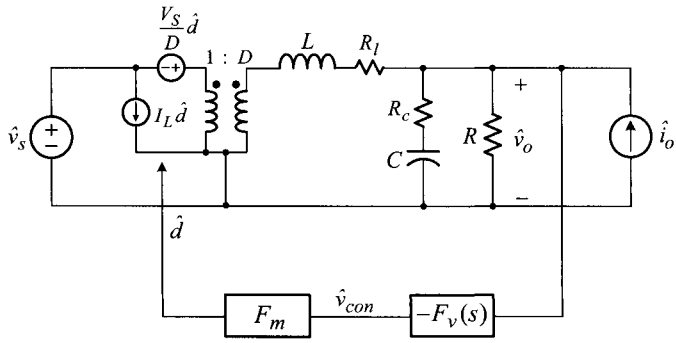


Figure 8.6 Small-signal model of buck converter.

and

$$Q \approx R\sqrt{\frac{C}{L}} \tag{8.26}$$

with assumptions $R \gg R_l$ and $R \gg R_c$.

Figure 8.7 shows the construction of the asymptotic plot for $|A_u|$ based on the rules described Table 8.1. While $|G_{vs}|$ is formed using (8.23), $|T_m|$ is drawn assuming a single integration function

$$T_m(s) = \frac{\omega_c}{s} \tag{8.27}$$

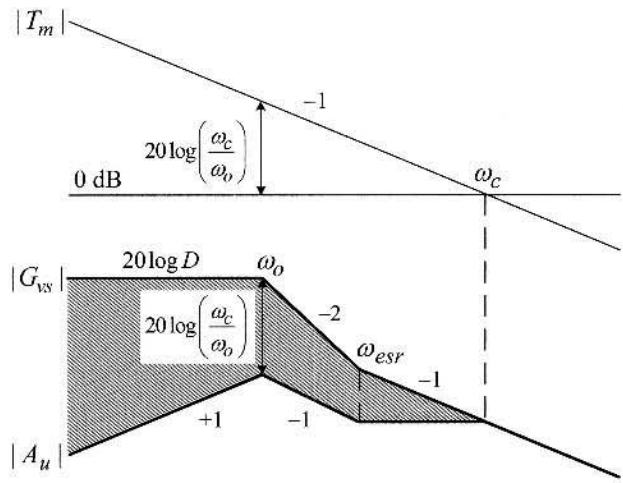


Figure 8.7 Construction of asymptotic plot for audio-susceptibility.

The ascending/descending slopes and corner frequencies of $|A_u|$ can readily be determined from the asymptote sketch rules given in Table 8.1.

The effects of the loop gain on the audio-susceptibility are clearly shown in Fig. 8.7. The loop gain provides attenuation up to the 0 dB crossover frequency. The amount of attenuation, highlighted by the shaded region in Fig. 8.7, is equal to the area of the triangle formed by connecting the $|T_m|$ curve and 0 dB line. The range and extent of the attenuation will be increased by pushing the loop gain crossover frequency towards higher frequencies, or equivalently, by increasing the integrator gain, ω_c.

The asymptotic plot of $|A_u|$ is converted into a factorized expression for $A_u(s)$ based on the rules presented in Table 8.2

$$A_u(s) = K_a s \frac{1 + \dfrac{s}{\omega_{esr}}}{\left(1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}\right)\left(1 + \dfrac{s}{\omega_c}\right)} \tag{8.28}$$

The leading coefficient K_a is found by evaluating the magnitude of the transfer function at the power stage double pole $s = j\omega_o$

$$|A_u(j\omega_o)| = |K_a s|_{s=j\omega_o} = |G_{vs}(j\omega_o)| - |T_m(j\omega_o)| \tag{8.29}$$

which is transformed to

$$20\log(K_a\omega_o) = 20\log D - 20\log\left(\frac{\omega_c}{\omega_o}\right) \tag{8.30}$$

This relationship is illustrated in Fig. 8.7. Equation (8.30) is converted to the linear relationship

$$K_a\omega_o = \frac{D}{\frac{\omega_c}{\omega_o}} \tag{8.31}$$

yielding the expression for K_a

$$K_a = \frac{D}{\omega_c} \tag{8.32}$$

8.2.2 Output Impedance

The load current-to-output transfer function is derived from Fig. 8.6

$$Z_p(s) = R_l \frac{\left(1 + \frac{s}{\omega_z}\right)\left(1 + \frac{s}{\omega_{esr}}\right)}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \tag{8.33}$$

where

$$\omega_z = \frac{R_l}{L} \tag{8.34}$$

Figure 8.8 shows the construction of the asymptotic plot for the output impedance $|Z_o|$ using the (8.33) and the assumption of $T_m(s) = \omega_c/s$. The asymptotic plot is converted into a factorized equation

$$Z_o(s) = K_z s \frac{\left(1 + \frac{s}{\omega_z}\right)\left(1 + \frac{s}{\omega_{esr}}\right)}{\left(1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}\right)\left(1 + \frac{s}{\omega_c}\right)} \tag{8.35}$$

The expression for K_z is found using the high-frequency asymptote of the output impedance, $|Z_o(j\infty)|$. As shown in Fig. 8.8, $|Z_o(j\infty)|$ converges to the high-frequency asymptote of $|Z_p|$ because $|T_m| \ll 1$ at high frequencies: $|Z_o(j\infty)| = |Z_p(j\infty)|$. Now, it can be deduced from the small-signal model in Fig. 8.6 that $|Z_p(j\infty)|$ is the parallel connection of the load resistor and esr of the output capacitor, because the inductor L behaves as an open circuit at high frequencies while the capacitor C practically becomes a short circuit. Accordingly, it follows that

$$|Z_o(j\infty)| = |Z_p(j\infty)| = 20\log(R \parallel R_c) \approx 20\log R_c \tag{8.36}$$

On the other hand, $|Z_o(j\infty)|$ is also found from (8.35)

$$|Z_o(j\infty)| = 20\log\left(\frac{K_z\,\omega_o^2\,\omega_c}{\omega_z\,\omega_{esr}}\right) \tag{8.37}$$

By equating (8.36) and (8.37), K_z is given by

$$K_z = R_c \frac{\omega_z\,\omega_{esr}}{\omega_o^2\,\omega_c} \tag{8.38}$$

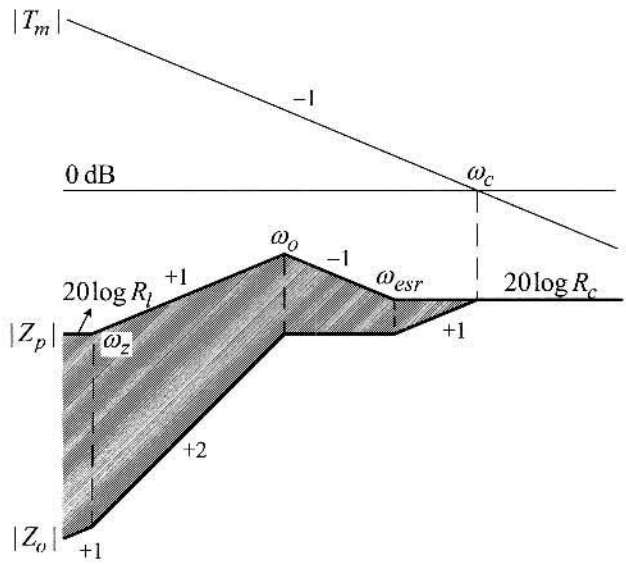


Figure 8.8 Construction of asymptotic plot for output impedance.

The influence of the loop gain on the output impedance can be understood in the same manner as the audio-susceptibility case.

8.3 VOLTAGE FEEDBACK COMPENSATION AND LOOP GAIN

In the previous section, we investigated the relationship between the loop gain and closed-loop transfer functions. To focus on the effects of the loop gain characteristics, a single integration function was assumed for the loop gain. However, the loop gain is the very quantity that must be properly designed in order to obtain good closed-loop transfer functions. Thus, it is first necessary to investigate the loop gain itself.

The loop gain is given by the product of the three factors: the duty ratio-to-output transfer function $G_{vd}(s)$, PWM gain F_m, and voltage feedback compensation $F_v(s)$. Among these three factors, the voltage feedback compensation is the only component that can be altered by design. For the given $G_{vd}(s)$ and F_m, the voltage feedback compensation $F_v(s)$ should be designed for good loop gain characteristics.

The objective of the voltage feedback compensation is to shape the loop gain into the desired structure. The primary consideration in this loop gain shaping is, of course, stability of the converter. In addition, the loop gain should provide good audio-susceptibility and output impedance characteristics. This section presents detailed steps of determining the structure and parameters of the voltage feedback compensation, in order to achieve the desired loop gain characteristics.

From Fig. 8.6, the duty ratio-to-output transfer function of the buck converter is given by

$$G_{vd}(s) = V_S \frac{1 + \dfrac{s}{\omega_{esr}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{8.39}$$

In Section 5.5, the PWM gain was found as

$$F_m = \frac{1}{V_m} \tag{8.40}$$

where V_m is the height of the PWM ramp signal. With the knowledge of the duty ratio-to-output transfer function and PWM gain, the structure of the voltage feedback compensation is now investigated.

8.3.1 Problems of Single Integrator

As discussed in Section 3.6.1, the voltage feedback compensation should have an infinite dc gain, $|F_v(j0)| = \infty$, in order to regulate the output voltage at the desired value. The simplest circuit with such a property is the single integrator. As an initial attempt, a single integrator is considered for the voltage feedback compensation

$$F_v(s) = \frac{K_v}{s} \tag{8.41}$$

The expression for the loop gain then becomes

$$\begin{aligned} T_m(s) = G_{vd}(s)\,F_v(s)\,F_m &= \underbrace{V_S \frac{1 + \dfrac{s}{\omega_{esr}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}}}_{G_{vd}(s)} \underbrace{\frac{K_v}{s}}_{F_v(s)} \underbrace{\frac{1}{V_m}}_{F_m} \\ &= \frac{K_t}{s} \frac{1 + \dfrac{s}{\omega_{esr}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \end{aligned} \tag{8.42}$$

with

$$K_t = \frac{V_S K_v}{V_m} \tag{8.43}$$

Figure 8.9 shows the asymptotic plots for $|T_m|$ and $\angle T_m$ in comparison with $|G_{vd}|$. Because of the integrator, $|T_m|$ starts with -1 slope. The initial -1 slope is altered to -3 slope at the double pole frequency, ω_o. The -3 mid-frequency slope is finally changed to the -2 high-frequency slope at the esr zero, ω_{esr}. Figure 8.9 assumes that

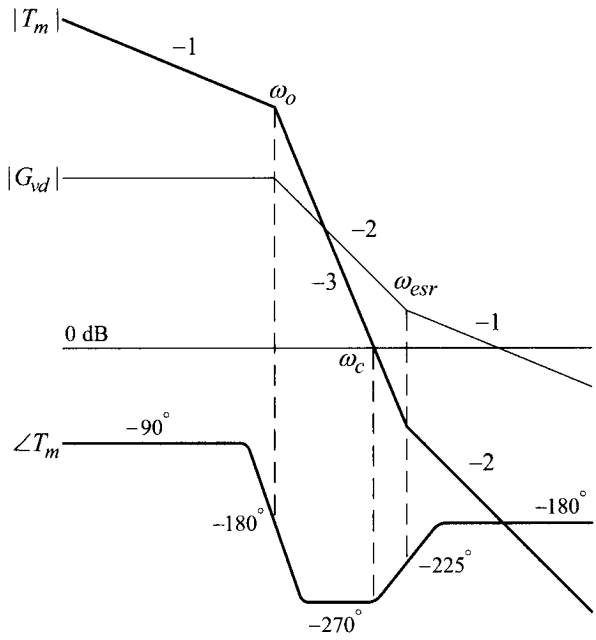


Figure 8.9 Unstable loop gain with $F_v(s) = K_v/s$.

the crossover frequency of the loop gain, ω_c, occurs at the frequency between the power stage double pole and esr zero: $\omega_o < \omega_c < \omega_{esr}$.

The phase of the loop gain starts with −90° due to the integrator. The initial −90° phase dips down to −270° over ω_o. At high frequencies, $\angle T_m$ settles into the −180° final phase, owing to the 90° phase boost at the esr zero.

The problem of the voltage feedback compensation is obvious in Fig. 8.9. Because $\angle T_m$ falls well below −180° at the loop gain crossover frequency, the loop gain violates the Nyquist stability criterion and the converter becomes unstable. The only way to secure stability is to significantly reduce the integrator gain K_v so that $|T_m|$ crosses the 0 dB line at the frequency before the power stage double pole: $\omega_c < \omega_o$. The loop gain with this modification is shown in Fig. 8.10. Even though the converter is stable, both the phase and gain margins will be very small. Furthermore, $|T_m|$ is significantly reduced with a small integrator gain. The reduced $|T_m|$ only provides limited attenuation for closed-loop transfer functions, as highlighted by the shaded triangle in Fig. 8.10. For this case, the magnitude of the closed-loop transfer functions would be large. The small stability margins and large closed-loop transfer function magnitude both make the voltage feedback compensation unacceptable for real applications.

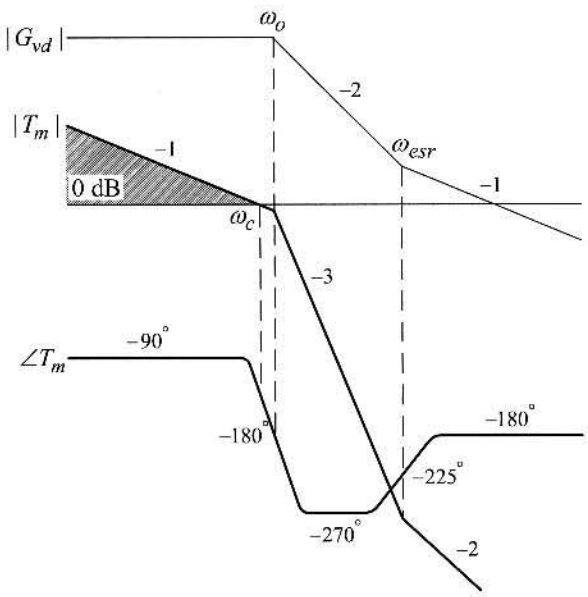


Figure 8.10 Stable loop gain with $F_v(s) = K_v/s$.

8.3.2 Voltage Feedback Compensation

The origin of the problem in the case of the single integrator compensation is the phase delay incurred by the integrator and power stage double pole. The integrator forces the loop gain to start with the −90° initial phase. The power stage double pole brings in additional −180° phase delay, causing $\angle T_m$ to decline to −270°. This makes the converter highly prone to instability. To secure stability under this situation, the loop gain crossover should occur before the power stage double pole at the expense of the poor closed-loop performance.

The voltage feedback compensation should always start with an integrator structure to achieve the output voltage regulation with the condition $|F_v(j0)| = \infty$. After the initial integrator, the voltage feedback compensation could incorporate two zeros to boost the phase of the loop gain. When placed in the neighborhood of the power stage double pole, the two zeros compensate for the −180° phase delay incurred by the power stage double pole. This allows the 0 dB crossover frequency to be placed at the frequencies beyond the power stage double pole, while maintaining good phase characteristics.

Besides the two zeros, two poles should be added to the voltage feedback compensation for the following reason. The voltage feedback circuit receives the input signal from the output of the converter, which abounds with high-frequency switching noises. The high-frequency noises will be transmitted to the PWM block through the voltage feedback compensation. To prevent malfunctions triggered by the high-frequency noises at the PWM block, the voltage feedback compensation must provide

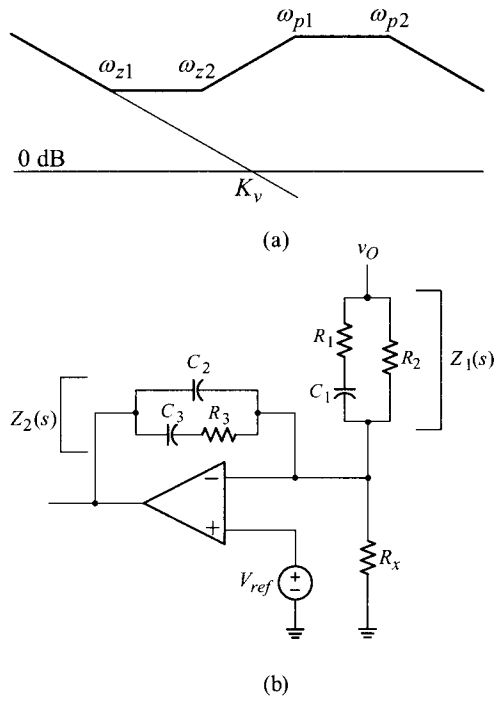


Figure 8.11 Three-pole two-zero feedback compensation. (a) Structure of voltage feedback compensation. (b) Circuit implementation.

a fair amount of attenuation at high frequencies. To provide this high-frequency noise attenuation, the magnitude of the voltage feedback compensation should have a descending high-frequency asymptote. At the presence of the two zeros, two poles are necessary to provide a −20 dB/dec roll-off at high frequencies.

From the preceding discussions, the desired structure of the voltage feedback compensation is identified as

$$F_v(s) = \frac{K_v}{s} \frac{\left(1 + \dfrac{s}{\omega_{z1}}\right)\left(1 + \dfrac{s}{\omega_{z2}}\right)}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)} \tag{8.44}$$

Figure 8.11(a) shows the asymptotic plot of the voltage feedback compensation. The exact locations of the zeros and poles must be determined in consideration of their impacts on stability margins and closed-loop transfer functions. This issue will be treated in Section 8.4.

The voltage feedback compensation in Fig. 8.11(a) can be constructed using an op amp and passive circuit components. Figure 8.11(b) shows such implementation, in which the impedance ratio $Z_2(s)/Z_1(s)$ constitutes the voltage feedback compensation.

The resistance R_x in Fig. 8.11(b) is added to control the magnitude of the output voltage: $V_O = V_{ref}(1+R_2/R_x)$. As discussed in Section 5.6.1, this resistance is irrelevant to the voltage feedback compensation. By directly evaluating $F_v(s) = Z_2(s)/Z_1(s)$, the compensation parameters are expressed in terms of the circuit components

$$F_v(s) = \frac{K_v}{s}\frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$$

$$\text{with} \quad K_v = \frac{1}{R_2(C_2+C_3)}$$

$$\omega_{z1} = \frac{1}{R_3C_3} \qquad \omega_{z2} = \frac{1}{(R_1+R_2)C_1}$$

$$\omega_{p1} = \frac{1}{R_1C_1} \qquad \omega_{p2} = \frac{1}{R_3\left(\frac{C_2C_3}{C_2+C_3}\right)} \tag{8.45}$$

Once the integrator gain and corner frequencies are selected, the circuit components in Fig. 8.11(b) are determined using the above equations. Among the six circuit components, one can be arbitrarily chosen and the other components are found using the equations in (8.45). This compensation circuit, named the three-pole two-zero compensation after its transfer function, was previously introduced in Sections 3.6.1 and 5.6.1.

8.4 COMPENSATION DESIGN AND CLOSED-LOOP PERFORMANCE

The design of the voltage feedback compensation involves with the selection of the five compensation parameters $\{\omega_{z1}\ \omega_{z2}\ \omega_{p1}\ \omega_{p2}\ K_v\}$ while simultaneously meeting the following design objectives:

- stability with adequate phase and gain margins,
- small audio-susceptibility, and
- small output impedance.

This section provides design principles to properly select the five compensation parameters.

8.4.1 Voltage Feedback Compensation and Loop Gain

This section investigates the selection of the compensation parameters focusing on loop gain characteristics. With the three-pole two-zero compensation, the loop gain

is expressed by

$$\begin{aligned} T_m(s) &= G_{vd}(s)F_v(s)F_m \\ &= \underbrace{V_S \frac{1+\dfrac{s}{\omega_{esr}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}}_{G_{vd}(s)} \underbrace{\frac{K_v}{s}\frac{\left(1+\dfrac{s}{\omega_{z1}}\right)\left(1+\dfrac{s}{\omega_{z2}}\right)}{\left(1+\dfrac{s}{\omega_{p1}}\right)\left(1+\dfrac{s}{\omega_{p2}}\right)}}_{F_v(s)} \underbrace{\frac{1}{V_m}}_{F_m} \end{aligned} \tag{8.46}$$

which can be arranged as

$$T_m(s) = \frac{K_t}{s}\frac{\left(1+\dfrac{s}{\omega_{esr}}\right)\left(1+\dfrac{s}{\omega_{z1}}\right)\left(1+\dfrac{s}{\omega_{z2}}\right)}{\left(1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}\right)\left(1+\dfrac{s}{\omega_{p1}}\right)\left(1+\dfrac{s}{\omega_{p2}}\right)} \tag{8.47}$$

with

$$K_t = \frac{V_S K_v}{V_m} \tag{8.48}$$

For the given power stage parameters and operational conditions, the zeros and poles of the voltage feedback compensation should be selected to provide desirable loop gain characteristics, which in turn offer good audio-susceptibility and output impedance characteristics.

Figure 8.12 shows the asymptotic plots for $|T_m|$, $|G_{vd}|$, and $\angle T_m$. The asymptotic plots are constructed with the assumption $\omega_{z1} < \omega_o < \omega_{z2} < \omega_c < \omega_{p1} = \omega_{esr} < \omega_{p2}$[†], where ω_c denotes the 0 dB crossover frequency of the loop gain. Justifications for the selection of the compensation parameters are given as follows.

1) The first compensation zero ω_{z1} should be placed prior to the power stage double pole ω_o: $\omega_{z1} < \omega_o$. This step is necessary to prevent the converter from being a conditionally stable system. If the compensation zero is not present until the power stage double pole appears, the initial $-90°$ loop gain phase will dip down well below $-180°$ over the power stage double pole ω_o. In this case, the two compensation zeros should be placed between ω_o and the 0 dB crossover frequency of the loop gain, ω_c, in order to provide the phase boost needed for a positive phase margin.

   Although the converter could maintain stability in this case, there surely is the frequency range in which $\angle T_m$ is less than $-180°$ while $|T_m|$ is larger than unity. Figure 8.13(a) is the polar plot of the loop gain for such a case. The polar plot indicates that the converter is a conditionally stable system which is

[†]The asymptotic plot in Fig. 8.12 is drawn with the assumption that the corner frequencies of the loop gain are *widely* separated so that the phase undergoes a complete 90° or 180° change over corner frequencies. However, the loop gain will not go through the *complete* phase change due to the finite distance among the corner frequencies. Thus, the phase does not reduce to $-180°$ after the power stage double pole ω_o and the phase margin at the crossover frequency ω_c does not increase to 90°.

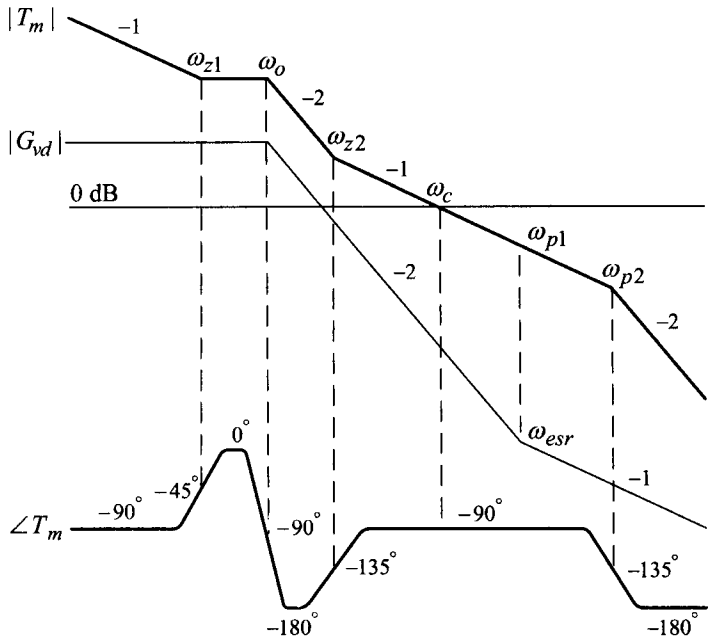


Figure 8.12 Construction of loop gain asymptotic plot.

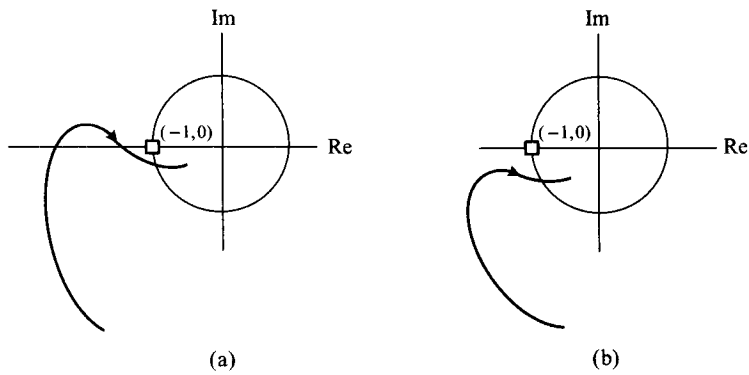


Figure 8.13 Polar plot of loop gain. (a) Conditionally stable loop gain with $\omega_o < \omega_{z1}$. (b) Stable loop gain with $\omega_{z1} < \omega_o$.

problematic in real operations, as illustrated in Example 7.7.

Conversely, if the first compensation zero precedes the power stage double pole, $\angle T_m$ stays above $-180°$ due to the early phase boost and the converter thus secures stability without being conditionally stable. Figure 8.13(b) is the loop gain plot for this case.

2) The second compensation zero ω_{z2} needs to be placed after the power stage double pole but before the loop gain crossover frequency ω_c ($\omega_o < \omega_{z2} < \omega_c$), in order to provide adequate phase boost at the crossover frequency. If ω_{z2} is placed after ω_c, it only makes limited contribution to the phase margin and its phase boosting effect is mostly wasted. The loop gain magnitude $|T_m|$ retains the initial −20 dB/dec slope after ω_{z2}, as shown in Fig. 8.12.

3) The first compensation pole ω_{p1} is placed at the esr zero, $\omega_{p1} = \omega_{esr}$, to maintain the −20 dB/dec slope by canceling the esr zero. The ideal structure of the loop gain is in fact the single integration function that has a fixed −20 dB/dec magnitude slope for all frequencies, as illustrated in Section 8.2. Although this ideal loop gain structure is not feasible due to the power stage dynamics, it is always desirable to increase the frequency range in which $|T_m|$ maintains a −20 dB/dec slope. This design objective is achieved by placing ω_{p1} at ω_{esr}.

4) Finally, the second compensation pole ω_{p2} is placed at high frequencies to provide the high-frequency noise attenuation.

With the compensation parameters described above, the loop gain crossover frequency can be placed at higher frequencies, while securing sufficient phase margin. Although Fig. 8.12 hints that the phase margin could reach 90°, this theoretical maximum cannot be obtained due to the finite distances among the corner frequencies of the loop gain. The actual phase margin is determined by the relative locations of the compensation parameters and usually falls in the range of 45° − 70°.

8.4.2 Feedback Compensation Design Guidelines

Based on the previous discussions, step-by-step compensation design guidelines are established as follows.

1) Place the first compensation pole ω_{p1} at the esr zero, $\omega_{p1} = \omega_{esr}$, to nullify the effects of the esr zero. This provides a −20 dB/dec loop gain roll-off for wider frequency range.

2) Locate the first compensation zero ω_{z1} before the power stage double pole ω_o to provide phase boost without becoming a conditionally stable system. As will be shown in Section 8.4.5, the location of this compensation zero determines the speed of the step input response. The response becomes faster as the zero is positioned at higher frequencies. Thus, ω_{z1} should be placed as high as possible, yet still should not exceed the power stage double pole. As a rule of thumb, it is recommended that $\omega_{z1} = (0.6 - 0.8)\,\omega_o$.

3) Place the second compensation zero ω_{z2} after the power stage double pole but before the loop gain crossover frequency, to obtain an adequate phase boost at the crossover frequency. As will be discussed in Section 8.4.6, the position of this zero determines the speed of the step load response. For faster responses, the zero should be placed at higher frequencies. However, the phase boosting

effect at the crossover frequency will be diminished as ω_{z2} is pushed towards higher frequencies. It is generally recommended that $\omega_{z2} = (1.5 - 3.0)\,\omega_o$ to trade off the phase boosting effect and speed of the step load response.

4) Locate the second compensation pole ω_{p2} at high frequencies. In general, ω_{p2} can be placed around 50 – 80% of the switching frequency ω_s: $\omega_{p2} = (0.5 - 0.8)\,\omega_s$.

5) Select the desired frequency for the loop gain crossover, ω_c. It is a good practice to place the crossover frequency around 10 – 30% of the switching frequency ω_s: $\omega_c = (0.1 - 0.3)\,\omega_s$. Detailed discussions about the selection of ω_c will be given in the next section. From the asymptotic plot of $|T_m|$ in Fig. 8.12 and the expression (8.47), the following relationship is derived

$$20\log\frac{V_S K_v}{V_m \omega_{z1}} - 40\log\frac{\omega_{z2}}{\omega_o} - 20\log\frac{\omega_c}{\omega_{z2}} = 0\ \text{dB} \tag{8.49}$$

where ω_c is the desired location of the crossover frequency. The preceding equation is converted into the design equation

$$\frac{V_S K_v}{V_m \omega_{z1}}\left(\frac{\omega_o}{\omega_{z2}}\right)^2\left(\frac{\omega_{z2}}{\omega_c}\right) = 1 \quad \Rightarrow \quad K_v = \frac{V_m}{V_S}\frac{\omega_{z1}\,\omega_{z2}\,\omega_c}{\omega_o^2} \tag{8.50}$$

This equation can be used to find K_v for a preselected ω_c.

6) Check the phase margin and adjust the integrator gain, if necessary, to secure a 45° – 70° phase margin.

The above design procedures are summarized in Table 8.3 for easy reference. An application of this design approach will be illustrated in Example 8.2.

8.4.3 Voltage Feedback Compensation and Closed-Loop Performance

Figure 8.14 illustrates the relationship among the loop gain, open-loop transfer functions, and closed-loop transfer functions. The asymptotic plots are constructed using the rules given in Table 8.1. The impacts of the loop gain characteristics, or equivalently the effects of the voltage feedback compensation, can clearly be seen in Fig. 8.14. The open-loop transfer functions are attenuated up to the loop gain crossover frequency. The power stage double pole does not appear in the closed-loop transfer functions because the second-order feature of the open-loop transfer functions is canceled by the loop gain, which itself carries the same second-order feature: $A_u(s) \approx G_{vs}(s)/T_m(s)$ and $Z_o(s) \approx Z_p(s)/T_m(s)$ for the frequencies where $|T_m| \gg 1$.

Table 8.3 Compensation Design Procedures

Loop gain expression

$$T_m(s) = G_{vd}(s)F_v(s)F_m = \underbrace{V_S \frac{1+\frac{s}{\omega_{esr}}}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}}}_{G_{vd}(s)} \underbrace{\frac{K_v}{s}\frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}}_{F_v(s)} \underbrace{\frac{1}{V_m}}_{F_m}$$

$$= \frac{V_S K_v/V_m}{s} \frac{\left(1+\frac{s}{\omega_{esr}}\right)\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}\right)\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$$

Compensation design guidelines

1) Set the first compensation pole: $\omega_{p1} = \omega_{esr}$.
2) Choose the first compensation zero: $\omega_{z1} = (0.6-0.8)\,\omega_o$.
3) Select the second compensation zero: $\omega_{z2} = (1.5-3.0)\,\omega_o$.
4) Choose the second compensation pole: $\omega_{p2} = (0.5-0.8)\,\omega_s$.
5) Select the loop gain crossover frequency: $\omega_c = (0.1-0.3)\,\omega_s$.
6) Evaluate the integrator gain: $K_v = \frac{V_m}{V_S}\frac{\omega_{z1}\,\omega_{z2}\,\omega_c}{\omega_o^2}$.
7) Check the phase margin and adjust K_v to secure a 45°–70° phase margin.
8) Evaluate the circuit components for the voltage feedback compensation using (8.45).

The asymptotic plot reveals the structure of the closed-loop transfer functions and also provides the information to judge the influence of each compensation parameter on the converter performance. For example, when the integrator gain K_v is increased within a limited range while other parameters remain unchanged, the following changes can be inferred:

- increase in the loop gain crossover frequency,
- decrease in the peak value of the audio-susceptibility $|A_u|_{peak}$, and
- decrease in the peak value of the output impedance and $|Z_o|_{peak}$.

On the other hand, an excessive increase in K_v lessens the phase margin. The

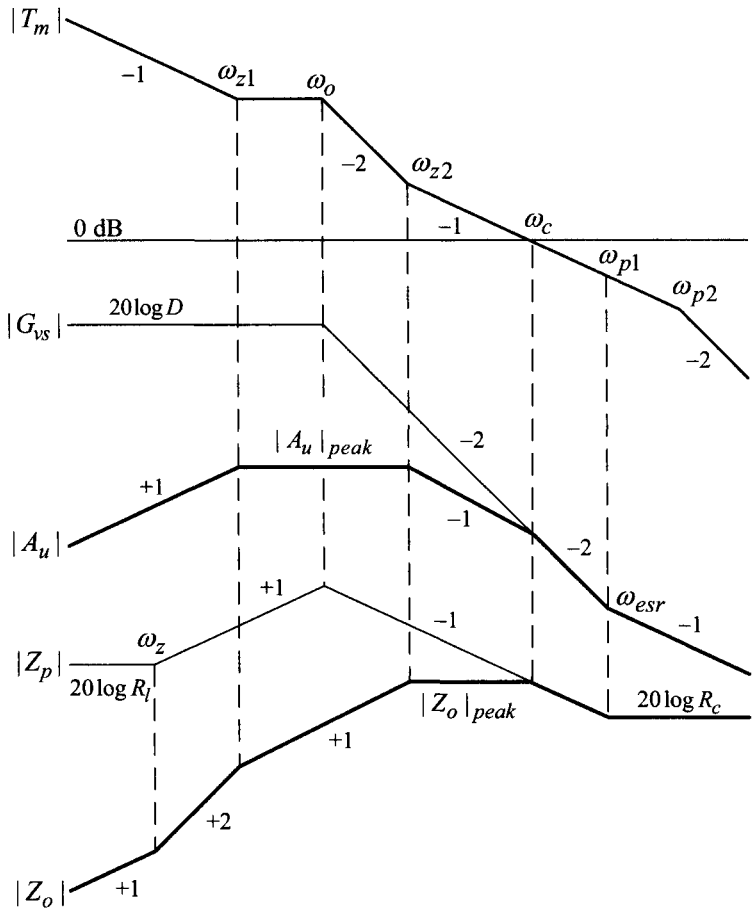


Figure 8.14 Voltage feedback compensation and closed-loop transfer functions.

converter could lose stability when the crossover frequency is pushed beyond ω_{p2} with a very large K_v.

The asymptotic plot of $|A_u|$ is converted into an analytical expression, based on the rules in Table 8.2

$$A_u(s) = K_a s \frac{1 + \dfrac{s}{\omega_{esr}}}{\left(1 + \dfrac{s}{\omega_{z1}}\right)\left(1 + \dfrac{s}{\omega_{z2}}\right)\left(1 + \dfrac{s}{\omega_c}\right)} \tag{8.51}$$

The expression for K_a is found from the magnitude relationship among the transfer functions at ω_{z1}

$$|A_u(j\omega_{z1})| = |K_a s|_{s=j\omega_{z1}} = |G_{vs}(j\omega_{z1})| - |T_m(j\omega_{z1})| \tag{8.52}$$

Referring to (8.23), (8.47), and (8.51), the above equation is translated as

$$K_a\omega_{z1} = \frac{D}{\frac{K_t}{\omega_{z1}}} \tag{8.53}$$

yielding the expression for K_a

$$K_a = \frac{D}{K_t} \tag{8.54}$$

where $K_t = (V_S K_v)/V_m$. The peak value of $|A_u|$ is approximated as

$$|A_u|_{peak} = |A_u|_{s=j\omega_{z1}} = |K_a s|_{s=j\omega_{z1}} = 20\log\left(\frac{D}{K_t}\omega_{z1}\right) \tag{8.55}$$

From Fig. 8.14, the closed-loop output impedance is expressed as

$$Z_o(s) = K_z s \frac{\left(1+\frac{s}{\omega_z}\right)\left(1+\frac{s}{\omega_{esr}}\right)}{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)\left(1+\frac{s}{\omega_c}\right)} \tag{8.56}$$

The value for K_z is found from the high-frequency asymptote of the output impedance. The high-frequency asymptote of $|Z_o|$ is given by

$$|Z_o(j\infty)| = 20\log\left(\frac{K_z\,\omega_{z1}\,\omega_{z2}\,\omega_c}{\omega_z\,\omega_{esr}}\right) \tag{8.57}$$

As discussed in Section 8.2.2, the high-frequency asymptote of $|Z_o|$ approaches the parallel connection of the load resistance and esr of the output capacitor

$$|Z_o(j\infty)| = 20\log(R \parallel R_c) \approx 20\log R_c \tag{8.58}$$

By equating (8.57) and (8.58), K_z is given by

$$K_z = R_c\frac{\omega_z\,\omega_{esr}}{\omega_{z1}\,\omega_{z2}\,\omega_c} \tag{8.59}$$

The peak value of the output impedance is found by evaluating $|Z_o|$ at ω_c

$$\begin{aligned} |Z_o|_{peak} &= |Z_o(j\omega_c)| = 20\log R_c + 20\log\left(\frac{\omega_{esr}}{\omega_c}\right) \\ &= 20\log\left(R_c\frac{\omega_{esr}}{\omega_c}\right) \end{aligned} \tag{8.60}$$

■ EXAMPLE 8.2 Compensation Design Example

This example demonstrates the application of the compensation design guidelines established in this section. Figure 8.15 shows the circuit diagram of a closed-loop controlled buck converter. The converter regulates the output voltage at 4 V using the three-pole two-zero compensation. From the circuit parameters, the power stage double pole and esr zero are determined as

$$\omega_o \approx \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{40\times10^{-6}\,470\times10^{-6}}} = 2\pi\cdot 1.16\times10^3 \text{ rad/s}$$

and

$$\omega_{esr} = \frac{1}{CR_c} = \frac{1}{470\times10^{-6}\,0.05} = 2\pi\cdot 6.77\times10^3 \text{ rad/s}$$

The switching frequency of the converter is set at $\omega_s = 2\pi\cdot 50\times10^3$ rad/s and the height of the ramp signal is $V_m = 3.8$ V. Based on the compensation design guidelines, the corner frequencies of the three-pole two-zero compensation are selected

- $\omega_{z1} = 0.8\,\omega_o = 2\pi\cdot 928$ rad/s
- $\omega_{z2} = 1.5\,\omega_o = 2\pi\cdot 1.74\times10^3$ rad/s
- $\omega_{p1} = \omega_{esr} = 2\pi\cdot 6.77\times10^3$ rad/s
- $\omega_{p2} = 0.8\,\omega_s = 2\pi\cdot 4\times10^4$ rad/s

The 0 dB crossover frequency is chosen at $\omega_c = 0.116\,\omega_s = 2\pi\cdot 5.80\times10^3$ rad/s. Based on the design equation, the integrator gain K_v is determined as

$$\begin{aligned} K_v &= \frac{V_m}{V_S}\frac{\omega_{z1}\,\omega_{z2}\,\omega_c}{\omega_o^2} \\ &= \frac{3.8}{16}\frac{(2\pi\cdot 928)(2\pi\cdot 1.74\times10^3)(2\pi\cdot 5.80\times10^3)}{(2\pi\cdot 1.16\times10^3)^2} \\ &= 1.04\times10^4 \end{aligned}$$

The loop gain characteristics with the selected parameters are shown in Fig. 8.16. The loop gain crossover occurs at the exact target frequency of 5.8 kHz with 65° phase margin. The loop gain, as well as other upcoming closed-loop transfer functions, is obtained from PSpice® simulations using the small-signal model of the converter.

From the loop gain in Fig. 8.16, it can be noticed that the integrator gain can be further increased to place the crossover frequency around 9 kHz where the largest phase margin is expected. However, this extreme design is not desirable in practice and could actually end up with inferior performance, compared with the current design of $K_v = 1.04\times10^4$. Justifications for *not* increasing K_v beyond the current value will be given in Example 8.4, which covers the issues related with the fidelity and limitation of the small-signal model.

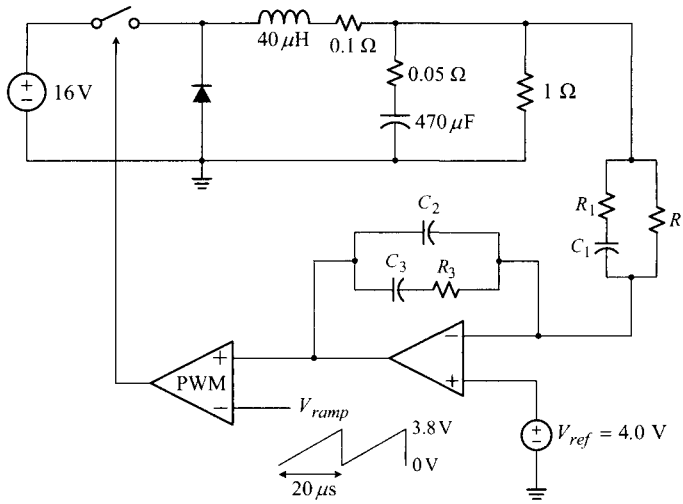


Figure 8.15 Closed-loop controlled buck converter: $R_1 = 2.2\ \text{k}\Omega$, $C_1 = 11\ \text{nF}$, $R_2 = 6.4\ \text{k}\Omega$, $C_2 = 365\ \text{pF}$, $R_3 = 11\ \text{k}\Omega$, and $C_3 = 15\ \text{nF}$.

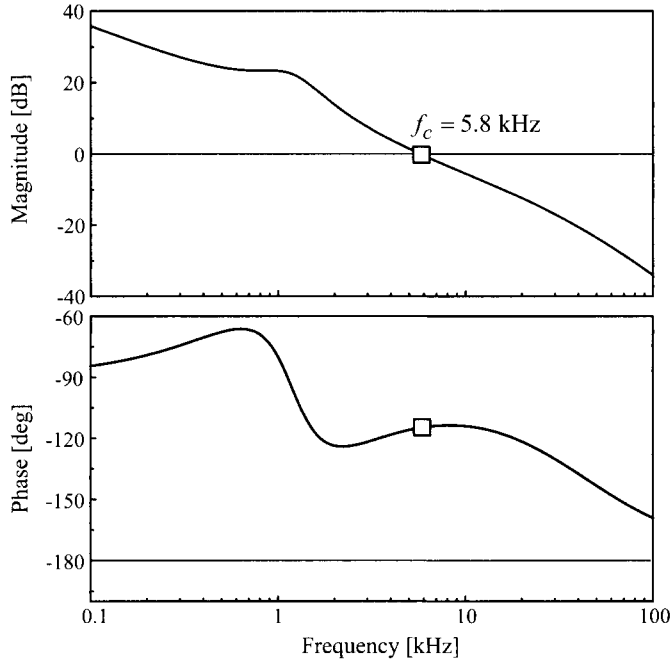


Figure 8.16 Loop gain characteristics with $K_v = 1.04 \times 10^4$.

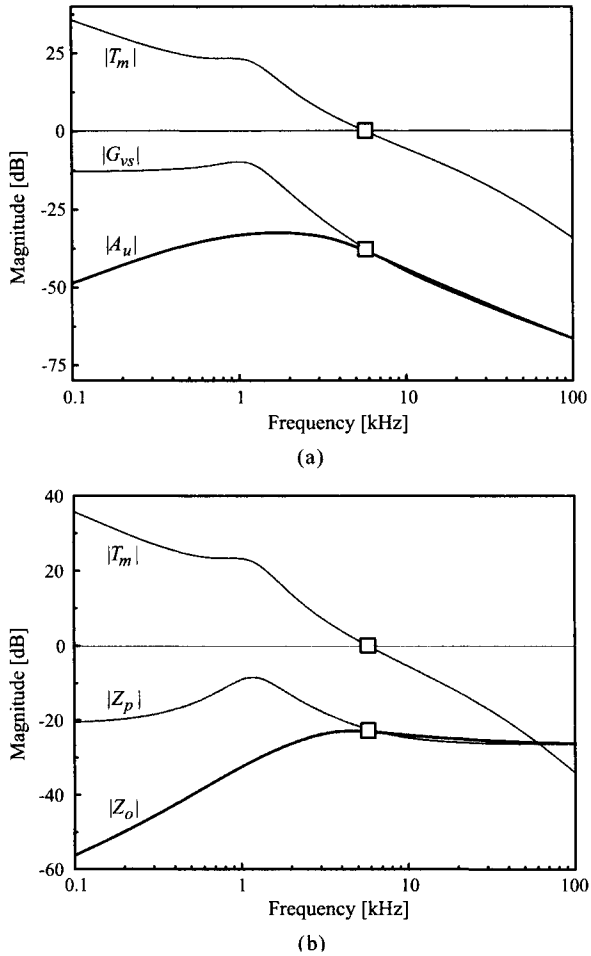


Figure 8.17 Closed-loop performance. (a) Audio-susceptibility. (b) Output impedance.

The integrator gain $K_v = 1.04 \times 10^4$ is now selected as the final design while other compensation parameters were chosen earlier. The circuit components for the voltage feedback circuit are determined from the selected compensation parameters. One circuit component is arbitrarily chosen as $R_1 = 2.2$ kΩ and the remaining circuit components are determined as $C_1 = 11$ nF, $R_2 = 6.4$ kΩ, $C_2 = 365$ pF, $R_3 = 11$ kΩ, and $C_3 = 15$ nF, based on the equations (8.45).

Figure 8.17 illustrates the closed-loop performance of the converter. Figure 8.17(a) shows the audio-susceptibility $|A_u|$ along with the input-to-output transfer function $|G_{vs}|$ and loop gain $|T_m|$. Figure 8.17(b) displays the output impedance $|Z_o|$, load current-to-output transfer function $|Z_p|$, and loop gain $|T_m|$.

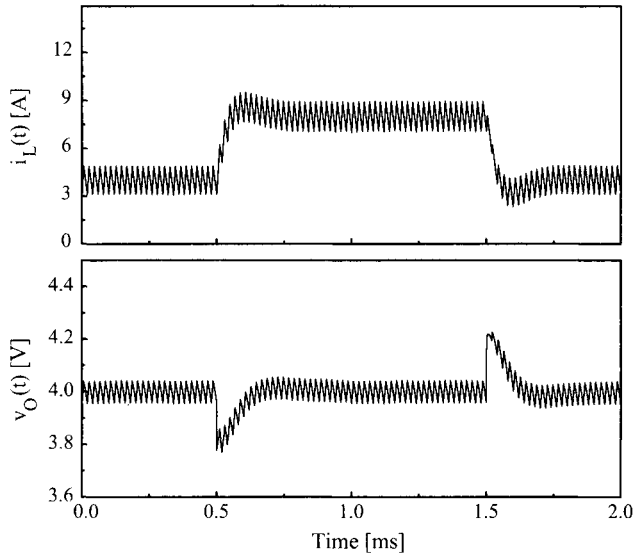


Figure 8.18 Step load transient response of inductor current i_L and output voltage v_O.

The validity and usefulness of the asymptotic analysis are confirmed when the Bode plots in Fig. 8.17 are compared with the asymptotic plots in Fig. 8.14.

The compensation design is also evaluated by time-domain simulations. Figure 8.18 shows the transient response of the inductor current and output voltage due to a series of step changes in the load current: $I_O = 4$ A $\Rightarrow$ 8 A $\Rightarrow$ 4 A. The transient waveforms exhibit very stable and well-controlled behavior. The detailed analysis of the step load response will be covered in Section 8.4.6. The compensation design presented in this example was used in Section 3.6.2 to illustrate the dc regulation and transient behavior of a closed-loop controlled buck converter.

■ EXAMPLE 8.3 Accuracy of Asymptotic Approximation

Based on the asymptotic analysis, the closed-loop transfer functions are expressed in a factorized analytical form. In this example, the accuracy of this asymptotic approximation is assessed using the buck converter used in the previous example. The audio-susceptibility was given by

$$A_u(s) = K_a s \frac{1 + \dfrac{s}{\omega_{esr}}}{\left(1 + \dfrac{s}{\omega_{z1}}\right)\left(1 + \dfrac{s}{\omega_{z2}}\right)\left(1 + \dfrac{s}{\omega_c}\right)} \tag{8.61}$$

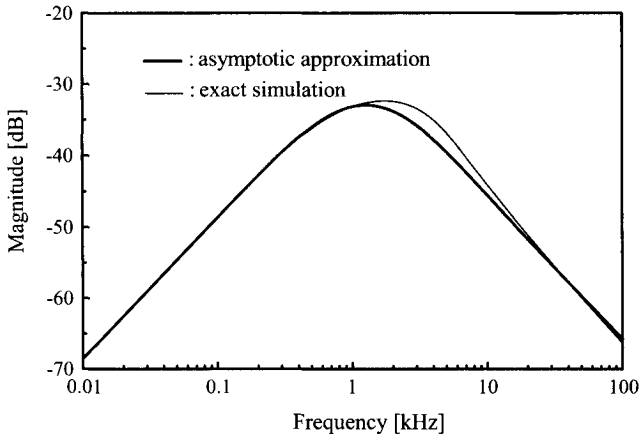


Figure 8.19 Audio-susceptibility comparison.

The leading coefficient K_a is determined as

$$K_a = \frac{V_m}{V_S}\frac{D}{K_v} \tag{8.62}$$

from (8.48) and (8.54). Based on the information shown in Fig. 8.15 and the integrator gain in Example 8.2, K_a is found as

$$K_a = \frac{V_m}{V_S}\frac{D}{K_v} = \frac{3.8}{16}\frac{0.25}{1.04 \times 10^4} = 5.71 \times 10^{-6}$$

The corner frequencies of (8.61) are given in Example 8.2: $\omega_{z1} = 2\pi \cdot 928$ rad/s, $\omega_{z2} = 2\pi \cdot 1.74 \times 10^3$ rad/s, $\omega_{esr} = 2\pi \cdot 6.77 \times 10^3$ rad/s, and $\omega_c = 2\pi \cdot 5.80 \times 10^3$ rad/s.

Figure 8.19 displays the Bode plot of (8.61) in comparison with the actual audio-susceptibility. The actual audio-susceptibility refers to the PSpice® simulation obtained directly from the small-signal model of the converter. The asymptotic transfer function shows a good correlation with the actual transfer function, except for some deviation in the frequency range of 1–20 kHz. The asymptotic analysis assumes that $|T_m| \gg 1$ for all the frequencies below the loop gain crossover, and $|T_m| \ll 1$ for all the frequencies thereafter. However, this assumption is not quite satisfied in the frequency range centered around the loop gain crossover frequency, because the condition $|T_m| \approx 1$ prevails in these frequencies. For the given converter, this range falls into the frequency region of 1–20 kHz and the asymptotic approximation produces a 3–4 dB maximum error in this region. The asymptotic analysis predicts the peak value of $|A_u|$

$$\begin{aligned} |A_u|_{peak} &= 20\log(K_a\omega_{z1}) \\ &= 20\log(5.71 \times 10^{-6}\ 2\pi \cdot 928) = -29.6\ \text{dB} \end{aligned}$$

The asymptotic approximation for the output impedance was given by

$$Z_o(s) = K_z s \frac{\left(1+\frac{s}{\omega_z}\right)\left(1+\frac{s}{\omega_{esr}}\right)}{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)\left(1+\frac{s}{\omega_c}\right)} \tag{8.63}$$

where

$$\omega_z = \frac{R_l}{L} = \frac{0.1}{40\times 10^{-6}} = 2\pi \cdot 398 \text{ rad/s}$$

$$\begin{aligned} K_z &= R_c \frac{\omega_z\,\omega_{esr}}{\omega_{z1}\omega_{z2}\,\omega_c} \\ &= 0.05 \frac{(2\pi\cdot 398)(2\pi\cdot 6.77\times 10^3)}{(2\pi\cdot 928)(2\pi\cdot 1.74\times 10^3)(2\pi\cdot 5.8\times 10^3)} \\ &= 2.29\times 10^{-6} \end{aligned}$$

The peak value of the output impedance is predicted as

$$\begin{aligned} |Z_o|_{peak} &= 20\log\left(R_c\frac{\omega_{esr}}{\omega_c}\right) \\ &= 20\log\left(0.05\,\frac{2\pi\cdot 6.77\times 10^3}{2\pi\cdot 5.8\times 10^3}\right) = -24.7 \text{ dB} \end{aligned}$$

Figure 8.20 compares the Bode plot of (8.63) with the actual output impedance. Same as the audio-susceptibility case, the asymptotic approximation exhibits good accuracy except for the frequency range of 1 – 20 kHz, where either the condition $|T_m| \gg 1$ or $|T_m| \ll 1$ is not quite satisfied.

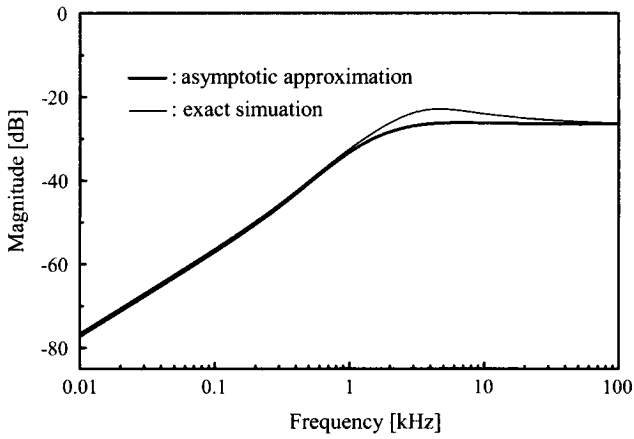


Figure 8.20 Output impedance comparison.

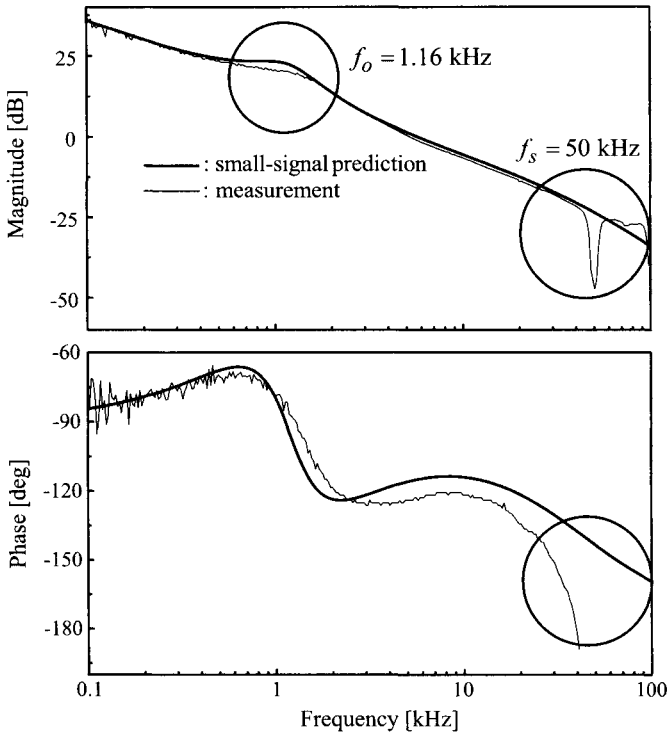


Figure 8.21 Loop gain comparison.

■ EXAMPLE 8.4 Accuracy of Small-Signal Model

The accuracy of the asymptotic analysis is verified in the previous example. This example investigates the accuracy of the small-signal model itself, which was derived under the small-signal assumption. The buck converter used in Example 8.2 was built and its loop gain is measured using an impedance analyzer. The measured loop gain characteristics are then compared with the predictions of the small-signal model. The comparison is shown in Fig. 8.21. While affected by some measurement noises, the experimental data clearly exhibit the loop gain characteristics of the converter.

The small-signal prediction shows a close correlation with the experimental data. However, the theoretical prediction deviates from the measurement in two different frequency ranges. The first deviation is observed in the neighborhood of the power stage double pole at $f_o = \omega_o/2\pi \approx 1.16$ kHz and the second disagreement is found at high frequencies.

The first deviation is due to the difference in the power stage damping. In the small-signal model, the esrs of the output capacitor and inductor are only considered as the parasitic resistances that contribute to the power stage damping.

In the experimental converter, there are many other parasitic resistances which are not accounted for in the small-signal model. These unaccounted parasitic resistances additionally contribute to the damping and the experimental data show less peaking in the magnitude and more gradual change in the phase. The accuracy of the small-signal prediction will be improved if the actual parasitic resistances are properly included in the small-signal model.

The second disagreement at the high frequencies stems from the limitation of the small-signal model of the PWM block. The constant modulator gain F_m, defined as the small-signal model of the PWM process in Section 5.5, is an approximation based on the presumption that the input signal to the PWM block does not significantly vary within one switching period. This presumption only holds true when the frequency response is evaluated at significantly lower frequencies than the switching frequency. As the evaluation frequency is increased, this assumption becomes less accurate and so does the PWM gain.

When the evaluation frequency becomes so high that the input signal to the PWM block varies substantially within one switching period, the nonlinear time-varying effect of the PWM process starts becoming pronounced. In this frequency range, the frequency response is strongly influenced by the sideband components of the PWM process; more specifically, the frequency response contains the sideband offshoots of the PWM process, as well as the response to the original small-signal excitation. This frequency-dependent nonlinear time-varying effect of the PWM process is not included in the small-signal PWM gain.

As shown in Fig. 8.21, the error in the small-signal prediction grows larger as the evaluation frequency is increased. In particular, the experimental phase curve drops noticeably as the evaluation frequency approaches half the switching frequency, $0.5f_s$ = 25 kHz. In addition, the experimental magnitude curve shows a dip at integer multiples of the switching frequency, 50 kHz and 100 kHz. In fact, these are the singular points where the nonlinear effect of the PWM process is most pronounced and the small-signal model produces the largest error.

Figure 8.21 illustrates that the danger of overly increasing the loop gain crossover frequency. The phase characteristics in Fig. 8.21 indicate that the phase margin of the actual converter is smaller than the estimation based on the small-signal model. The error becomes increasingly larger as the crossover frequency is pushed towards higher frequency. The crossover frequency is recommended to be placed around $10-30\%$ of the switching frequency, in order to avoid the risk of overestimating the phase margin and to secure the fidelity of the analysis results. In addition, it is good engineering practice to consider the additional phase drop at high frequencies when designing the loop gain. For example, in anticipation of the additional phase drop which is not accounted for in the small-signal model, the crossover frequency can be placed before the frequency at which the small-signal model predicts the maximum phase margin, as previously exercised in Example 8.2.

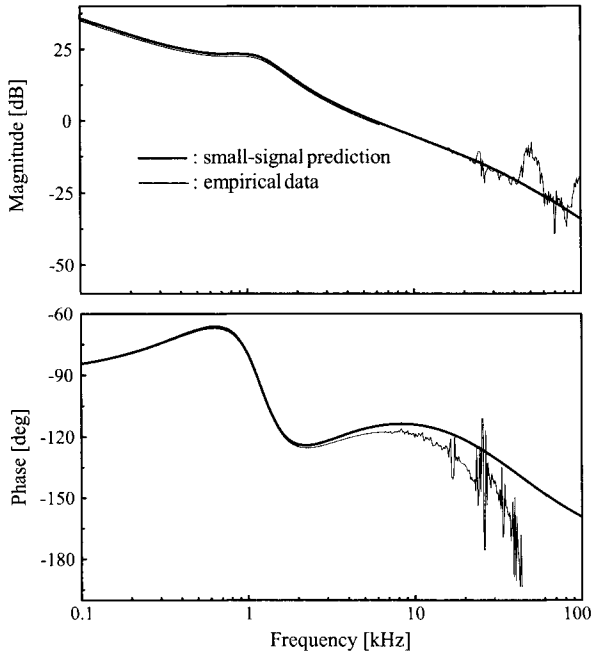


Figure 8.22 Computational method for loop gain evaluation.

■ EXAMPLE 8.5 Computational Method for Frequency-Domain Analysis

As introduced in Section 6.5, an empirical approach based on the computational method can be used as a means of verifying predictions of the small-signal model. In the computational method, the time-domain simulation is performed with a perturbed input signal, and the output at the perturbation frequency is extracted and compared with the input signal. By sweeping the perturbation frequency for the range of interest and recording the ratio between the input and output signals, the Bode plot of the corresponding frequency response is obtained. *This computational method is a functional duplication of the experimental measurement using an impedance analyzer.*

Some commercial circuit simulation softwares offer an automated process for the computational method. In this book, small-signal model predictions are compared with the empirical data obtained from the computational method using PSIM® from Powersim Inc [3].

Figure 8.22 shows the loop gain of the buck converter used in Example 8.2. The predictions of the small-signal model are compared with the empirical data of the computational method. At low frequencies, the disparity between the analytical and empirical results is practically undetectable. On the other hand, some discrepancies are noticeable at high frequencies. The

empirical data show irregular spikes in both magnitude and phase due to the sensitivity of the numerical algorithm. Even so, the computational data exhibit discernible patterns. The magnitude envelope follows the prediction of the small-signal model. Very interestingly, the high-frequency phase envelope deviates from the small-signal model prediction but tracks the measured phase response demonstrated in Fig. 8.21. This indicates that *the computational method duly captures the frequency-dependent nonlinear time-varying effects of the PWM process and provides accurate high-frequency dynamics of the converter.*

Figure 8.23 shows the audio-susceptibility and output impedance characteristics of the converter. This figure confirms the accuracy of the small-signal model prediction and utility of the empirical approach in the frequency-domain

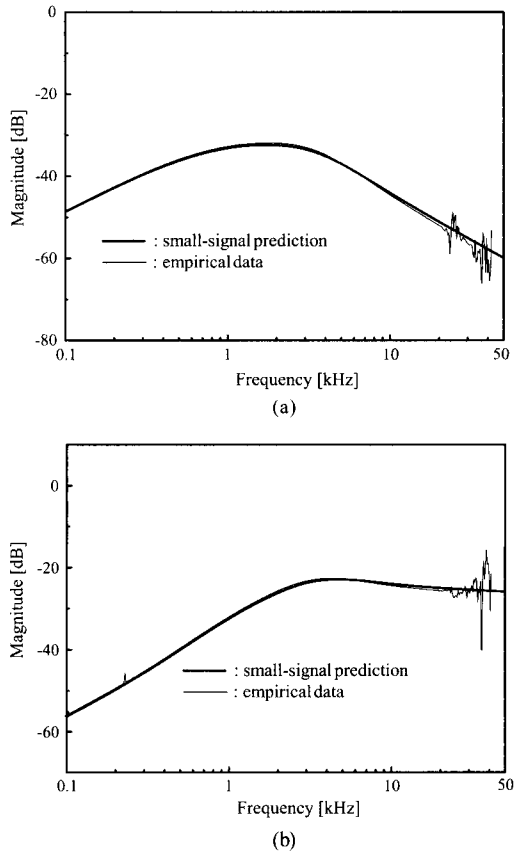


Figure 8.23 Computational method for closed-loop performance evaluation. (a) Audio-susceptibility. (b) Output impedance.

analysis. Unlike the loop gain analysis, the small-signal model predictions are a close match with the computational data for all frequencies, because the closed-loop transfer functions follow the open-loop transfer functions at high frequencies where the loop gain magnitude becomes very small.

8.4.4 Phase Margin and Closed-Loop Performance

As shown in the audio-susceptibility and output impedance analysis, the closed-loop transfer function $G(s)_{\text{closed}}$ is related with the open-loop transfer function $G(s)_{\text{open}}$ through the following equation

$$G(s)_{\text{closed}} = \frac{G(s)_{\text{open}}}{1 + T_m(s)} \tag{8.64}$$

where $T_m(s)$ is the loop gain. This equation is split into the two approximations

$$G(s)_{\text{closed}} = \frac{G(s)_{\text{open}}}{1 + T_m(s)} \approx \begin{cases} \dfrac{G(s)_{\text{open}}}{T_m(s)} & \text{at frequencies where } |T_m| \gg 1 \\ G(s)_{\text{open}} & \text{at frequencies where } |T_m| \ll 1 \end{cases} \tag{8.65}$$

for the asymptotic analysis. This asymptotic analysis is valid and accurate in the frequency range where either the condition $|T_m| \gg 1$ or $|T_m| \ll 1$ is met. However, neither of these assumptions is satisfied in the neighborhood of the loop gain crossover frequency where $|T_m| \approx 1$. The accuracy of the asymptotic approximation near the loop gain crossover was broadly discussed in Example 8.3. A more precise analysis around the crossover frequency is now given.

The exact behavior of the closed-loop transfer function can be investigated by evaluating the magnitude of the closed-loop transfer function

$$|G_{\text{closed}}| = \frac{|G_{\text{open}}|}{|1 + T_m|} \tag{8.66}$$

at the loop gain crossover frequency. Figure 8.24 illustrates the evaluation of the denominator of (8.66) based on the following facts.

- The denominator of (8.66) is the magnitude of the composite vector $|\vec{1} + \vec{T}_m|$.
- The magnitude of the loop gain is unity, $|T_m| = 1$, at the crossover frequency.
- The angle ϕ_m in Fig. 8.24, which corresponds to the difference between $-180°$ and $\angle T_m$ at the crossover frequency, is the phase margin of the loop gain.

From the vector addition rule and trigonometric relationships, the denominator of (8.66) becomes

$$|\vec{1} + \vec{T}_m| = \sqrt{\sin^2 \phi_m + (1 - \cos \phi_m)^2} = \sqrt{2 - 2\cos \phi_m} \tag{8.67}$$

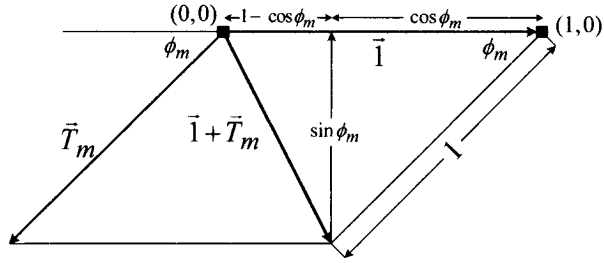


Figure 8.24 Evaluation of $|\vec{1} + \vec{T}_m|$ at loop gain crossover frequency.

Accordingly, the relationship (8.66) becomes

$$|G_{\text{closed}}| = \frac{|G_{\text{open}}|}{\sqrt{2 - 2\cos\phi_m}} \tag{8.68}$$

If the phase margin ϕ_m is smaller than 60°, the denominator of (8.68) is less than unity and $|G_{\text{closed}}|$ will surge from $|G_{\text{open}}|$ by the amount of

$$|G|_{\text{peaking}} = 20\log\left(\frac{1}{\sqrt{2 - 2\cos\phi_m}}\right) \tag{8.69}$$

The magnitude of the peaking is inversely proportional to the phase margin – the smaller the phase margin, the larger the peaking. If the phase margin is reduced to zero, the peaking becomes infinite.

When the phase margin ϕ_m is not significantly lower than 60°, the $|G_{\text{closed}}|$ curve can be obtained by smoothly connecting the asymptotes of $|G_{\text{open}}|/|T_m|$ and $|G_{\text{open}}|$ at the $|T_m|$ crossover frequency, as suggested in the asymptotic analysis rules in Table 8.1. If ϕ_m is noticeably lower than 60°, the peaking at the crossover frequency of $|T_m|$ should be considered when predicting the $|G_{\text{closed}}|$ curve.

■ EXAMPLE 8.6 Effects of Small Phase Margin

This example demonstrates the detrimental effects of a small phase margin. The small phase margin was shown to cause a peaking in the transfer function. It will also be argued that the peaking in turn results in an oscillatory behavior in the transient response.

The voltage feedback compensation, employed to the buck converter in the previous examples, is now modified to

$$F_v(s) = \frac{1.04 \times 10^4}{s} \frac{\left(1 + \frac{s}{2\pi \cdot 928}\right)\left(1 + \frac{s}{2\pi \cdot 9.9 \times 10^3}\right)}{\left(1 + \frac{s}{2\pi \cdot 6.77 \times 10^3}\right)\left(1 + \frac{s}{2\pi \cdot 4 \times 10^4}\right)}$$

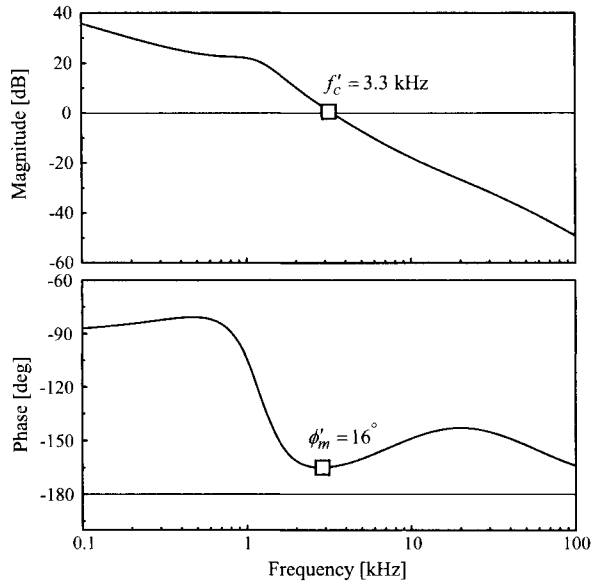


Figure 8.25 Loop gain characteristics with modified compensation design.

to produce the loop gain with a small phase margin. Compared to the original design, only the second compensation zero is increased from $\omega_{z2} = 2\pi \cdot 1.74 \times 10^3$ rad/s to $\omega'_{z2} = 2\pi \cdot 9.90 \times 10^3$ rad/s. The loop gain characteristics with this modification are shown in Fig. 8.25. The 0 dB crossover now occurs at $f_c' = 3.3$ kHz and the phase margin is reduced to $\phi'_m = 16°$. The magnitude of the peaking is calculated as

$$|G|_{\text{peaking}} = 20\log\left(\frac{1}{\sqrt{2-2\cos\phi'_m}}\right)$$
$$= 20\log\left(\frac{1}{\sqrt{2-2\cos 16°}}\right) \approx 11 \text{ dB}$$

This peaking is expected to occur at the loop gain crossover frequency, $f_c' = 3.3$ kHz. Figure 8.26 shows the output impedance $|Z_o|$ with the modified compensation design, along with the load current-to-output transfer function $|Z_p|$ and loop gain $|T_m|$. The output impedance $|Z_o|$ follows the curve formed by $|Z_p| - |T_m|$ at low frequencies and it converges to $|Z_p|$ at high frequencies. However, in the neighborhood of the loop gain crossover frequency, the output impedance deviates from the respective approximations, showing the expected 11 dB upsurge from $|Z_p|$ at the crossover frequency $f_c' = 3.3$ kHz. The effect of the small phase margin is clearly shown in Fig. 8.27, which compares the output impedance of the modified design with that of the original design. The

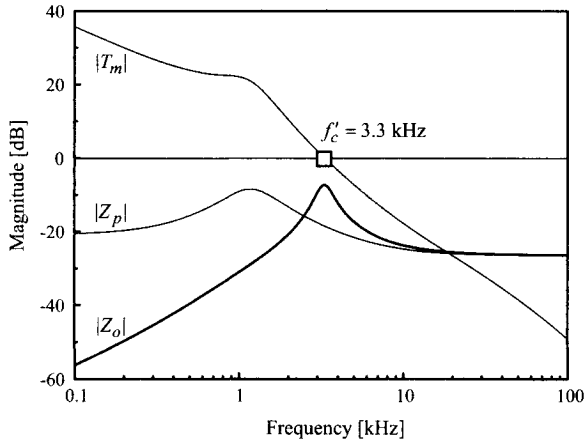


Figure 8.26 Output impedance characteristics with modified compensation design.

phase margin of the original design was $\phi_m = 65°$, while that of the modified design is $\phi_m' = 16°$.

As discussed in Section 7.3.1, the transient response of the output voltage due to the step change in the load current, I_{step}, is given by†

$$v_O(t) = \mathcal{L}^{-1}\left(\frac{I_{step}}{s} Z_o(s)\right) \tag{8.70}$$

where $\mathcal{L}^{-1}$ is the inverse Laplace transform operator. The impact of the output impedance peaking is deduced from this relationship. The peaking in $|Z_o|$ indicates the existence of an underdamped second-order term in the output impedance. When the inverse Laplace transform is taken, the underdamped second-order term produces a decaying sinusoidal component in the time-domain equation. Accordingly, the peaking in $|Z_o|$ signals an oscillatory behavior in the output voltage. The frequency of the oscillation coincides with the frequency of the output impedance peaking, which is the loop gain crossover frequency. Figure 8.28 shows the step load response of the modified design, in comparison with that of the original design. A series of step changes in the load current, $I_O = 4$ A $\Rightarrow$ 8 A $\Rightarrow$ 4 A, is used in Fig. 8.28. The output voltage of the modified design shows a decaying oscillation while the original design does not show any oscillatory behavior. The period of the oscillation is

†Strictly speaking, the relationship (8.70) is only valid when I_{step} is sufficiently small because the output impedance is derived under the small-signal assumption. Even so, the predictions of the output impedance exhibit markedly good correlations to transient responses with relatively large changes: for example, up to 50% change in the load current.

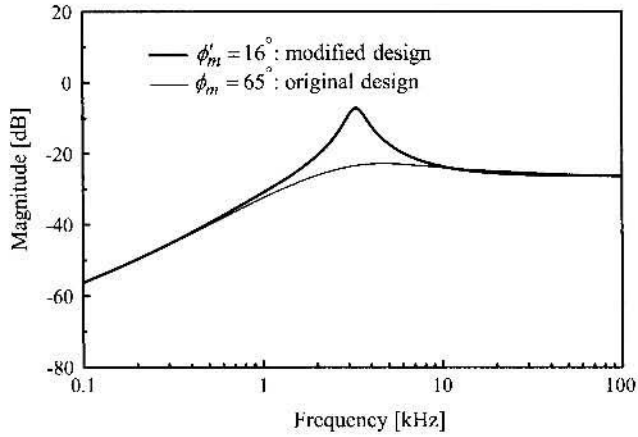


Figure 8.27 Phase margin and output impedance.

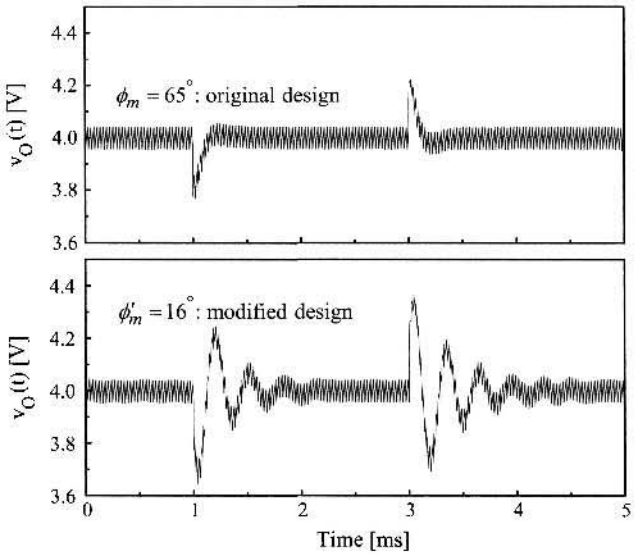


Figure 8.28 Phase margin and step load response of output voltage.

predicted as

$$t_{os} = \frac{1}{f_c'} = \frac{1}{3.3 \times 10^3} = 0.3 \text{ ms}$$

where $f_c' = 3.3$ kHz is the loop gain crossover frequency of the modified design.

As demonstrated in the previous example, there is an intimate relationship among the phase margin, output impedance peaking, and output voltage oscillation. A small

phase margin causes a peaking in the output impedance which in turn invokes an oscillation in the output voltage. The reduction in the phase margin intensifies the peaking and the intensified peaking makes the oscillation more persistent. When the phase margin is reduced to zero, the output impedance peaks to infinity and the output voltage shows a sustained oscillation as the sign of instability.

The effects of a small phase margin were previously addressed in Section 7.6. However, the perspective of Section 7.6 differs from that of the current section. Section 7.6 addressed the problem in a qualitative manner, in conjunction with the location of the system poles, while this section provided an explicit equation of (8.69). It is informative to compare the analytical results of this section with the qualitative discussions of Section 7.6. Readers are urged to review Example 7.8 which substantiates and reinforces the results of Example 8.6.

8.4.5 Compensation Zeros and Speed of Transient Responses

The three-pole two-zero circuit

$$F_v(s) = \frac{K_v}{s} \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \tag{8.71}$$

is identified as the optimal structure for the voltage feedback compensation. The selection of the compensation parameters is discussed focusing on the frequency-domain performance criteria. However, as will be shown in this section, the compensation parameters also affect the time-domain performance. In particular, the compensation zeros, ω_{z1} and ω_{z2}, determine the speed of transient responses. The first compensation zero ω_{z1} governs the speed of the step input response, while the second compensation zero ω_{z2} dictates the speed of the step load response. Accordingly, the location of the compensation zeros should be selected considering these facts. This section presents the selection of the first compensation zero ω_{z1}, while the next section deals with the second compensation zero ω_{z2}.

The impact of the first compensation zero ω_{z1} is explained using the audio-susceptibility and its relationship to the step input response. Figure 8.29 shows the asymptotic plot of the audio-susceptibility $|A_u|$, along with the asymptotic plots of $|T_m|$ and $|G_{vs}|$. The audio-susceptibility is written as

$$A_u(s) = K_a s \frac{1 + \frac{s}{\omega_{esr}}}{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)\left(1 + \frac{s}{\omega_c}\right)} \tag{8.72}$$

with the condition $\omega_{z1} \ll \omega_{z2} \ll \omega_c \ll \omega_{esr}$.

The first compensation zero ω_{z1} becomes a pole in the $A_u(s)$ expression in (8.72). The step input response of the output voltage is given by

$$v_O(t) = \mathcal{L}^{-1}\left(\frac{V_{step}}{s} A_u(s)\right) \tag{8.73}$$

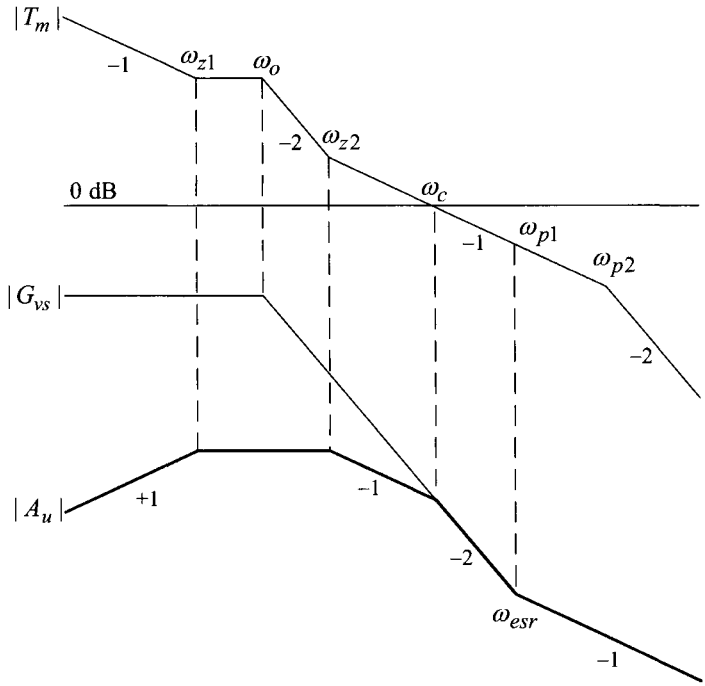


Figure 8.29 Construction of asymptotic plot for audio-susceptibility.

where V_{step} denotes the magnitude of the step input change. From (8.72) and (8.73), it follows that

$$v_O(t) = \mathcal{L}^{-1}\left(V_{step} \frac{K_a\left(1 + \dfrac{s}{\omega_{esr}}\right)}{\left(1 + \dfrac{s}{\omega_{z1}}\right)\left(1 + \dfrac{s}{\omega_{z2}}\right)\left(1 + \dfrac{s}{\omega_c}\right)} \right) \tag{8.74}$$

When the inverse Laplace transform is performed, the output voltage expression would contain three different exponential terms

$$\begin{aligned} v_O(t) \quad = \quad & \text{the term associated with } e^{-\omega_{z1}t} \\ & + \text{the term associated with } e^{-\omega_{z2}t} \\ & + \text{the term associated with } e^{-\omega_c t} \end{aligned} \tag{8.75}$$

The first term in (8.75) is the slowest mode due to the prevailing condition of $\omega_{z1} \ll \omega_{z2} \ll \omega_c$; in other words, the first compensation zero ω_{z1} becomes the dominant pole. Accordingly, the time constant of the transient response is $\tau = 1/\omega_{z1}$. The settling time of the transient response is determined as

$$t_s = 3\tau = 3\frac{1}{\omega_{z1}} \tag{8.76}$$

For faster response, ω_{z1} should be selected at higher frequencies. However, if ω_{z1} is placed after the power stage double pole ω_o, $\angle T_m$ could temporarily drop below $-180°$ making the converter conditionally stable, as discussed in Section 8.4.1. Thus, the compensation zero ω_{z1} should be placed at higher frequencies but still be located below the power stage double pole. In the previous section, it was recommended that $\omega_{z1} = (0.6–0.8)\,\omega_o$.

■ EXAMPLE 8.7 Compensation Zero and Step Input Response

This example substantiates the previous theoretical discussions about the impacts of the first compensation zero. The voltage feedback compensation of the buck converter is now modified to

$$F_v(s) = \frac{3.9 \times 10^3}{s} \frac{\left(1 + \frac{s}{2\pi \cdot 312}\right)\left(1 + \frac{s}{2\pi \cdot 1.74 \times 10^3}\right)}{\left(1 + \frac{s}{2\pi \cdot 6.77 \times 10^3}\right)\left(1 + \frac{s}{2\pi \cdot 4.0 \times 10^4}\right)}$$

Compared with the original design, the first compensation zero is reduced from $\omega_{z1} = 2\pi \cdot 928$ rad/s to $\omega'_{z1} = 2\pi \cdot 312$ rad/s and the integrator gain is also decreased from $K_v = 1.04 \times 10^4$ to $K'_v = 3.9 \times 10^3$, while the other compensation parameters are unchanged. Figure 8.30 shows the audio-susceptibility of the modified design in comparison with the original transfer function.

Figure 8.31 compares the output voltage of the buck converter in response to the step changes in the input voltage: $V_S = 16\text{ V} \Rightarrow 8\text{ V} \Rightarrow 16\text{ V}$. As expected, the modified design produces a slower response. The settling time of the modified design is predicted as

$$t'_s = 3\tau' = 3\frac{1}{\omega'_{z1}} = 3\frac{1}{2\pi \cdot 312} = 1.53\text{ ms}$$

while that of the original design is estimated as

$$t_s = 3\,\tau = 3\frac{1}{\omega_{z1}} = 3\frac{1}{2\pi \cdot 928} = 0.51\text{ ms}$$

8.4.6 Step Load Response

The step load response is a very important performance criterion for many dc-to-dc converters. As discussed in Section 7.3.1, the transient response of the output voltage can be analyzed using the output impedance. This section illustrates such an analysis with some simplifying assumptions on the output impedance characteristics. We will show that the speed of the step load response is determined by the position of the second compensation zero, ω_{z2} in (8.71).

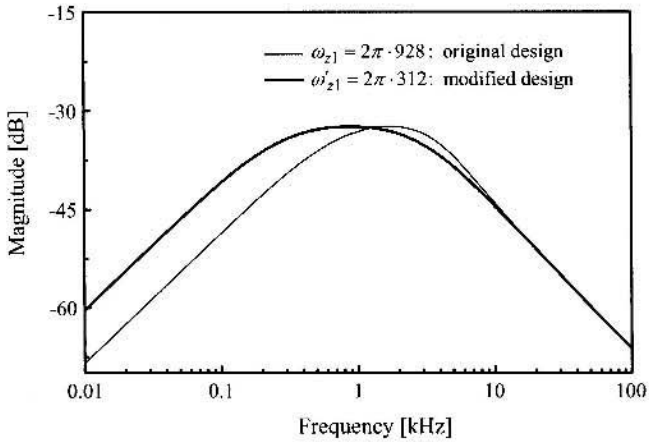


Figure 8.30 Compensation zero and audio-susceptibility.

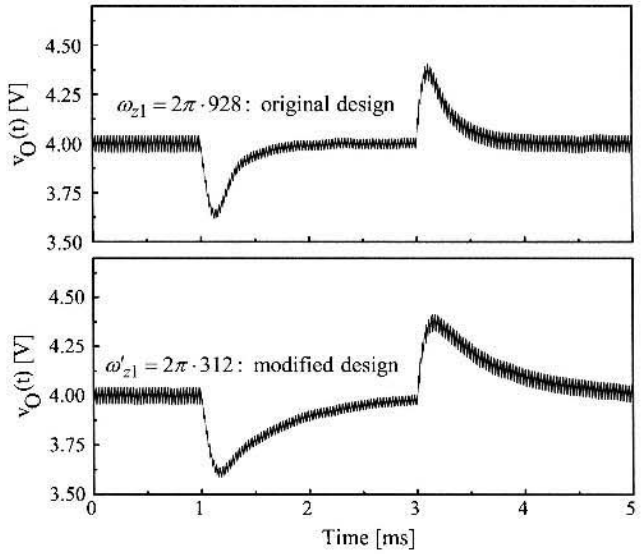


Figure 8.31 Compensation zero and step input response.

The asymptotic plot for the output impedance, originally introduced in Fig. 8.14, is modified in Fig. 8.32 with the following assumptions.

1) The first compensation zero ω_{z1} is placed at the low-frequency zero, ω_z, of the load current-to-output transfer function: $\omega_{z1} = \omega_z$.

2) The loop gain crossover frequency ω_c is placed at the esr zero ω_{esr}: $\omega_c = \omega_{esr}$.

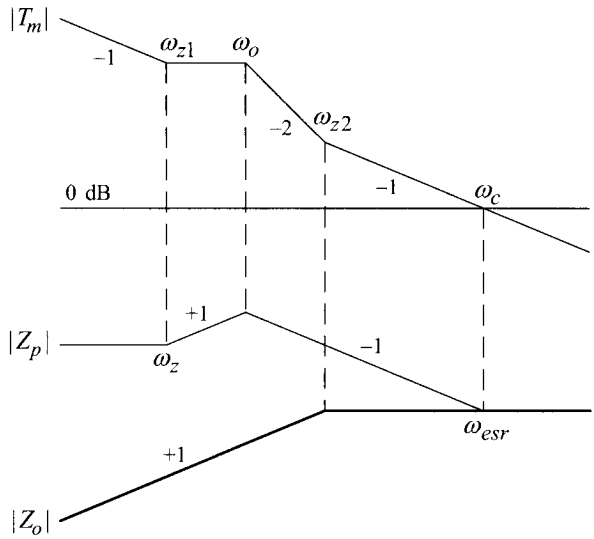


Figure 8.32 Construction of asymptotic plot for output impedance.

As will be shown in Example 8.8, these assumptions can broadly be justified in many practical dc-to-dc converters. The asymptotic plot for $|Z_o|$ is redrawn in Fig. 8.33(a). The first compensation zero ω_{z1}, which determines the speed of the step input response, does not appear in the output impedance. From Fig. 8.33(a), the output impedance is written as

$$Z_o(s) = \frac{s}{\omega_m} \frac{1}{1 + \dfrac{s}{\omega_{z2}}} \tag{8.77}$$

where ω_m represents the frequency at which the initial line segment of $|Z_o|$ crosses the 0 dB line. The peak magnitude of the output impedance is given by

$$|Z_o(j\omega)|_{peak} = |Z_o(j\infty)| = 20 \log\left(\frac{\omega_{z2}}{\omega_m}\right) \tag{8.78}$$

The transient response of the output voltage due to the step load change I_{step} is expressed as

$$\begin{aligned} v_O(t) &= \mathcal{L}^{-1}\left(\frac{I_{step}}{s} \frac{s}{\omega_m} \frac{1}{1 + \dfrac{s}{\omega_{z2}}}\right) \\ &= I_{step} \frac{\omega_{z2}}{\omega_m} e^{-\omega_{z2} t} \end{aligned} \tag{8.79}$$

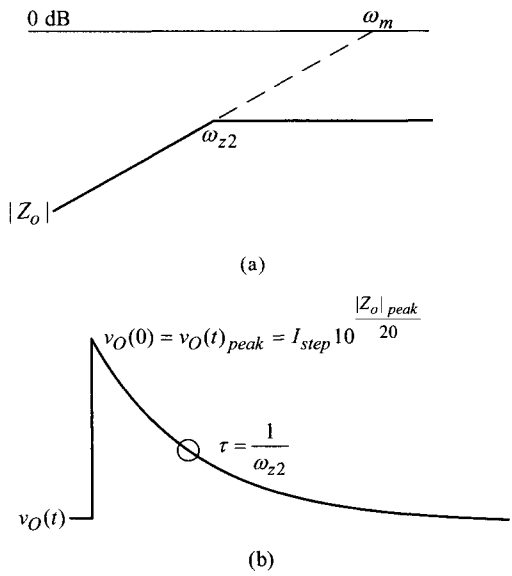


Figure 8.33 Output impedance and step load response. (a) Output impedance. (b) Step load response.

Figure 8.33(b) depicts the waveform of the output voltage. The peak overshoot of the output voltage is given by

$$\begin{aligned} v_O(t)_{peak} = v_O(0) &= I_{step}\frac{\omega_{z2}}{\omega_m} \\ &= I_{step}\, 10^{\frac{|Z_o|_{peak}}{20}} \end{aligned} \tag{8.80}$$

based on (8.78) and (8.79). The output voltage decays from the peak with a time constant of $\tau = 1/\omega_{z2}$. Thus, the settling time becomes

$$t_s = 3\tau = 3\frac{1}{\omega_{z2}} \tag{8.81}$$

As shown in the preceding analysis, there are simple, yet very practical and useful, relationships among the output impedance characteristics and step load transient response. The settling time of the output voltage is dictated by the second compensation zero, $t_s = 3/\omega_{z2}$. The peak value of the output voltage is determined by the product of the size of the step load change and the peak magnitude of the output impedance: $v_O(t)_{peak} = I_{step}\ 10^{|Z_o|_{peak}/20}$.

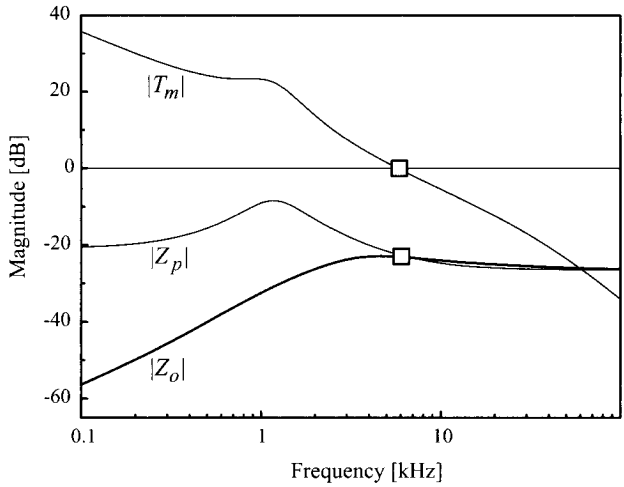


Figure 8.34 Output impedance of buck converter.

■ EXAMPLE 8.8 Output Impedance and Step Load Response

The accuracy of the preceding step load response analysis is confirmed in this example. For the buck converter in Example 8.2, the corner frequencies are given as $\omega_{z1} = 2\pi \cdot 928$ rad/s, $\omega_z = 2\pi \cdot 398$ rad/s, $\omega_c = 2\pi \cdot 5.80 \times 10^3$ rad/s, and $\omega_{esr} = 2\pi \cdot 6.67 \times 10^3$ rad/s, thereby broadly satisfying the conditions $\omega_{z1} \approx \omega_z$ and $\omega_c \approx \omega_{esr}$.

Figure 8.34 shows the output impedance $|Z_o|$, load current-to-output transfer function $|Z_p|$, and loop gain $|T_m|$ of the converter. The simulated output impedance shows a good correlation with the theoretical prediction of Fig. 8.32.

Figure 8.35 illustrates the transient response of the output voltage with $I_{step} = 4$ A. The peak value of the output voltage is predicted as

$$v_O(t)_{peak} = 4.0 + I_{step}\, 10^{\frac{|Z_o|_{peak}}{20}}$$

$$= 4.0 + 4 \cdot 10^{-26/20} = 4.2 \text{ V}$$

and the settling time is estimated as

$$t_s = 3\tau = 3\frac{1}{\omega_{z2}} = 3\frac{1}{2\pi \cdot 1.74 \times 10^3} = 0.27 \text{ ms}$$

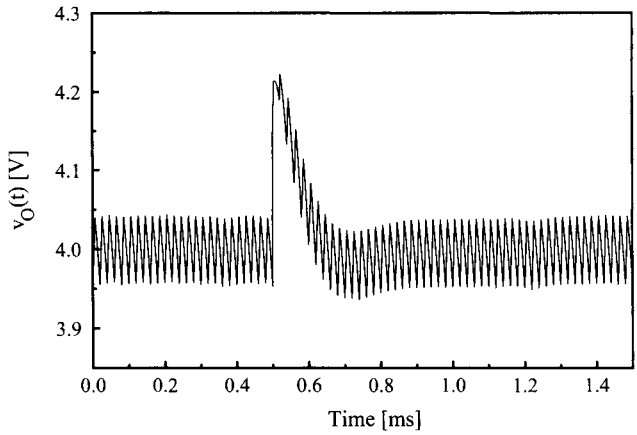


Figure 8.35 Step load response of buck converter.

8.4.7 Non-Minimum Phase System Case: Boost and Buck/Boost Converters

As discussed in Sections 6.3 and 6.4, the boost and buck/boost converters contain a right-half plane (RHP) zero in the duty ratio-to-output transfer function, $G_{vd}(s)$. The RHP zero induces a 90° phase delay to $\angle G_{vd}$ while increasing the slope of $|G_{vd}|$ by a 20 dB/dec. The dynamic system with an RHP zero is called the non-minimum phase system in the sense that the total phase variation in the transfer function becomes larger than that of the system with a regular left-half plane zero. Thus, the boost and buck/boost converters are a typical example of the non-minimum phase system.

The non-minimum phase system presents considerable difficulties to the feedback compensation design. The boost and buck/boost converters indeed do not render themselves to the application of the feedback control scheme presented in this chapter. In this section, we investigate the problem of the boost and buck/boost converters in regard to their control design. This section also introduces a new control scheme which can be applied to the boost and buck/boost converter to mitigate the problem of the RHP zero.

Boost and Buck/Boost Converters

The RHP zero imposes demanding constraints on the compensation design and hinders the boost and buck/boost converters from acceptable closed-loop performance. The problem of the RHP zero can readily be seen in Fig. 8.36, which shows the asymptotic plots for the $|G_{vd}|$ and loop gain of a boost or buck/boost converter. The previous three-pole two-zero circuit is assumed for the voltage feedback compensation.

The compensation parameters are selected based on the design strategy established in Section 8.4.2. In particular, the first compensation pole is placed at the RHP zero,

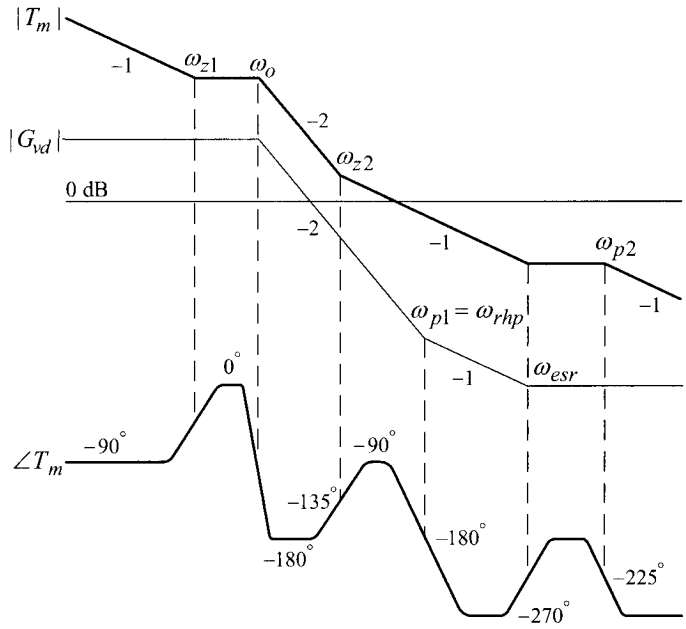


Figure 8.36 Loop gain characteristics of boost or buck/boost converter with three-pole two-zero compensation.

$\omega_{p1} = \omega_{rhp}$, in an attempt to extend the frequency range in which $|T_m|$ maintains the desirable −20 dB/dec slope.

The phase characteristics of the loop gain uncover the problem of the RHP zero. As shown in $\angle T_m$ in Fig. 8.36, the loop gain phase drops by 180° over the RHP zero, thereby worsening the high-frequency phase characteristics. The 90° phase drop caused by ω_{rhp} is augmented by the additional 90° phase delay brought in by ω_{p1}, resulting in 180° phase decay while $|T_m|$ stays in −20 dB/dec slope. Under this situation, $\angle T_m$ mainly remains near or below −180° from the mid-frequencies to high frequencies. Due to these unfavorable phase characteristics, it is very difficult to achieve satisfactory closed-loop performance while securing a reliable phase margin.

■ EXAMPLE 8.9 Boost Converter Example

This example demonstrates the difficulty in designing feedback compensation for a practical boost converter. Figure 8.37 shows the circuit diagram of a closed-loop controlled boost converter. The converter produces a 20 V output from a 12 V input source using the three-pole two-zero voltage feedback circuit.

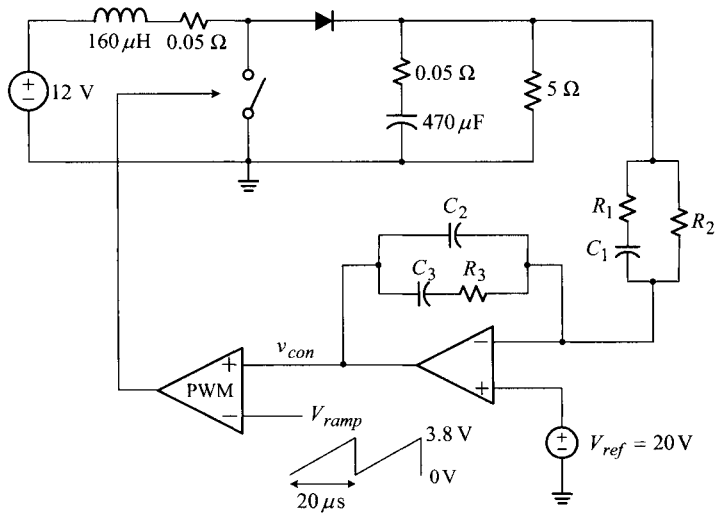


Figure 8.37 Closed-loop controlled boost converter: $R_1 = 2.2\ \text{k}\Omega$, $C_1 = 40.4\ \text{nF}$, $R_2 = 7.2\ \text{k}\Omega$, $C_2 = 1.7\ \text{nF}$, $R_3 = 2.4\ \text{k}\Omega$, and $C_3 = 0.28\ \mu\text{F}$.

The steady-state duty ratio of the converter is determined as

$$\frac{V_O}{V_S} = \frac{1}{1-D} \quad \Rightarrow \frac{20}{12} = \frac{1}{1-D} \quad \Rightarrow D = 0.4$$

From the duty ratio and power stage circuit parameters, the corner frequencies of the duty ratio-to-output transfer function are determined as

$$\begin{aligned} \omega_o &\approx \frac{1-D}{\sqrt{LC}} \\ &= \frac{1-0.4}{\sqrt{160\times10^{-6}470\times10^{-6}}} \\ &= 2\pi\cdot 348\ \text{rad/s} \end{aligned}$$

and

$$\begin{aligned} \omega_{rhp} &= \frac{(1-D)^2R}{L} \\ &= \frac{(1-0.4)^25}{160\times10^{-6}} \\ &= 2\pi\cdot 1.79\times10^3\ \text{rad/s} \end{aligned}$$

and

$$\omega_{esr} = \frac{1}{CR_c} = \frac{1}{470\times10^{-6}0.05} = 2\pi\cdot 6.77\times10^3\ \text{rad/s}$$

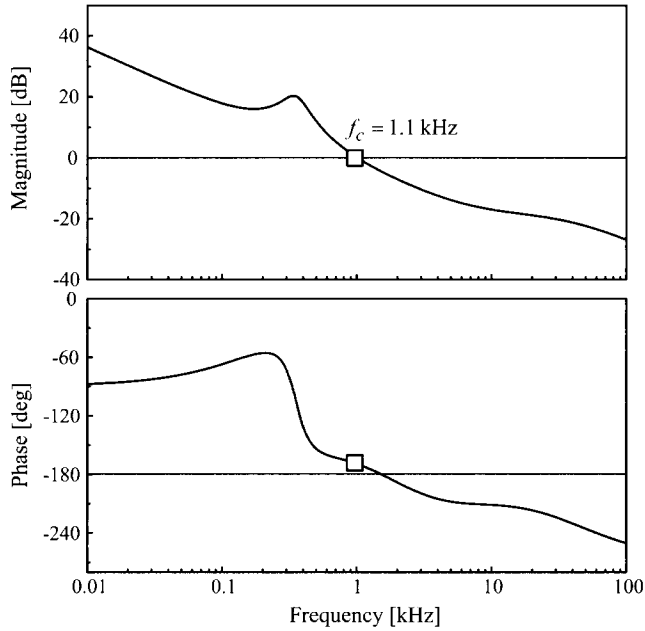


Figure 8.38 Loop gain characteristics of boost converter.

Based on the design guidelines for the three-pole two-zero compensation, the compensation parameters are selected as

- $\omega_{z1} = 0.7\omega_o = 2\pi \cdot 244$ rad/s
- $\omega_{z2} = 1.2\,\omega_o = 2\pi \cdot 418$ rad/s
- $\omega_{p1} = \omega_{rhp} = 2\pi \cdot 1.79 \times 10^3$ rad/s
- $\omega_{p2} = 0.8\,\omega_s = 2\pi \cdot 4.0 \times 10^4$ rad/s
- $K_v = 500$

The loop gain characteristics are shown in Fig. 8.38. When compared with the asymptotic plots in Fig. 8.36, $\angle T_m$ curve shows a rather gradual decay at the frequencies beyond the power stage double pole. This is because the corner frequencies of the voltage feedback compensation are not as widely separated as presumed in the asymptotic analysis. The loop gain crossover frequency is located at $\omega_c = 2\pi \cdot 1.1 \times 10^3$ rad/s with a 13° phase margin. This design would not be acceptable for most applications due to the insufficient phase margin. A possible design change for an adequate phase margin is to place the loop gain crossover frequency near or before the power stage double pole. However, such a design would end up with poor closed-loop performance with overly large output impedance and audio-susceptibility.

Alternative Control Scheme: Current Mode Control

The difficulty in the compensation design in Example 8.9 originates not from the structure of the feedback circuit but from the existence of the RHP zero in the duty ratio-to-output transfer function. While the previous example underscored the problem of the three-pole two-zero compensation circuit, it can readily be inferred that other compensation structures would worsen the situation.

The feedback control scheme covered in this chapter employs the output voltage as the only feedback signal. In this sense, this control scheme is referred to as voltage mode control. Example 8.9 proved that voltage mode control is not suitable for converters that have an RHP zero, such as the boost converter, the buck/boost converter, and all other isolated PWM converters derived from these two converters.

For dc-to-dc converters with the RHP zero, an alternative control method is adapted to resolve the aforementioned problem. The alternative control scheme employs the feedback signal not only from the output voltage but also from the inductor current. This control scheme is called current mode control because it employs an additional feedback from the inductor current. Current mode control could provide good closed-loop performance for the boost and buck/boost converters at the presence of the RHP zero. Current mode control deserves rigorous treatments and thus is the topic of the last two chapters of this book.

8.5 SUMMARY

This chapter presented the dynamic analysis and feedback design of closed-loop controlled PWM dc-to-dc converters. The graphical asymptotic analysis method is used to illustrate the results of the closed-loop analysis, principles of the feedback compensation design, and impacts of the compensation parameters. The asymptotic analysis has emerged as a systematic and viable tool for the dynamic analysis and control design. This method provides a graphical process for the compensation design and closed-loop analysis, and also yields factorized equations for transfer functions.

The three-pole two-zero circuit is identified as the optimal structure for the voltage feedback compensation for the buck converter. The relationship between the compensation parameters and performance criteria is investigated using the asymptotic analysis method. Simple and straightforward design procedures for the voltage feedback compensation are established.

The frequency-domain analysis based on the small-signal model is an approximation and the results should be interpreted with care. In particular, the small-signal model does not account for the high-frequency phase delay, incurred by the nonlinear time-varying dynamics of the PWM modulator. The small-signal model thus underestimates the phase delay and the actual phase characteristics can be worse than the predictions of the small-signal model. The error grows steadily as the evaluation frequency increases towards the switching frequency. This fact should be incorporated in the design and analysis of the converter loop gain, in order not to misinterpret the phase characteristics of the loop gain. Especially, the loop gain crossover frequency should be located at the frequencies sufficiently lower than the switching frequency,

typically 10 – 30% of the switching frequency, for the integrity of the information about the stability margins of the converter. Furthermore, the additional phase delay, which is not accounted for in the small-signal model, should be considered in assessing the phase margin.

The asymptotic analysis only uses the magnitude asymptotes while ignoring phase characteristics. This method is acceptable for most cases because the phase characteristics in general do not significantly affect the asymptotic analysis. However, there is one exception for this general trend. At the frequencies near the loop gain crossover where $|T_m| \approx 1$, the underlying assumption of $|T_m| \gg 1$ or $|T_m| \ll 1$ is infringed and the closed-loop transfer function is strongly affected by the phase margin. In particular, insufficient phase margins induce a peaking in transfer functions, which the asymptotic analysis cannot predict. To avoid an excessive peaking, the phase margin of $45° - 70°$ is recommended as a general guideline.

It was demonstrated that the results of the frequency-domain analysis can be used to predict and optimize the time-domain transient response. This chapter presented the three examples of such analyses.

1) The peaking in transfer functions, which appears at the loop gain crossover frequency when the phase margin is insufficient, can be translated to a damped oscillation in the transient response. The frequency of the oscillation is the same as the frequency of the peaking.

2) The location of the first compensation zero determines the speed of the step input response.

3) Finally, the location of the second compensation zero determines the speed of the step load response, while the peak value of the output impedance determines the magnitude of the output voltage excursion in the step load response.

Although these time-domain analyses are performed using the small-signal model derived under the small-signal assumption, the analysis results show good correlation with the transient responses produced by relatively large changes in operational conditions: for example, up to the 50% change in the load current or input voltage.

The feedback control scheme covered in this chapter is not suitable for the boost and buck/boost converters which have an RHP zero in their power stage transfer functions. For boost and buck/boost converters, an advanced feedback control technique, called current mode control, needs to be employed. Current mode control utilizes an additional feedback from the inductor current, as well as the output voltage feedback. Current mode control is now widely adapted to PWM dc-to-dc converters thanks to to its inherent advantages.

In contrast to current mode control, the control scheme covered in this chapter is called voltage mode control because it only utilizes the output voltage as the single feedback signal. Although voltage mode control has currently limited applications to buck and buck-derived PWM converters, it has profound significance in the area of the PWM converter modeling and analysis. Before the advent of current mode control, voltage mode control had virtually been the only available control scheme for PWM converters. Due to this long-time prevalence, the modeling and analysis of

PWM dc-to-dc converters have advanced centering around voltage mode control. As the outcomes of decades of research efforts, many important and valuable results are established for voltage mode control. Most of these achievements can be directly, or with minor modifications, adapted to current mode control. Current mode control will be treated in great details in the last two chapters of this book.

REFERENCES

1. R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, Kluwer Academic Publishers, 2001.
2. R. D. Middlebrook and S. Ćuk, *Advances in Switch-Mode Power Conversion*, TESLAco, Pasadena, CA, 1983.
3. *PSIM User's Guide*, Powersim Inc., Version 7.0, Mar. 2006.
4. B. H. Cho and F. C. Lee, *VPEC Power Electronics Professional Seminar*, Course I–Control Design, VPEC, 1991.
5. M. K. Marian, *Pulse-width Modulated DC-DC Power Converters*, Wiley, 2008.
6. V. Vorpérian, *Fast Analytical Techniques for Electrical and Electronic Circuits*, Cambridge University Press, 2002.
7. K. Ogata, *Modern Control Engineering*, Prentice Hall, 4th ed., 2002.

PROBLEMS

8.1* Consider the asymptotic plots for $|T|$ and $|G|$ shown in Fig. P8.1.

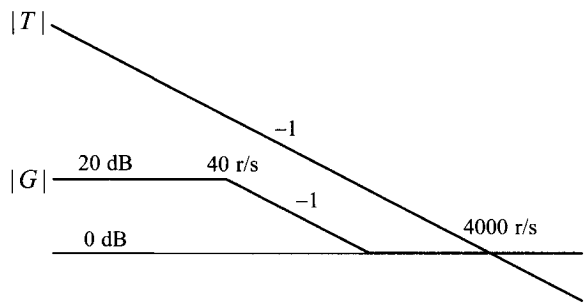


Fig. P8.1

a) Use the asymptotic analysis method to find an analytical expression for $F(s) = G(s)/(1 + T(s))$.

b) Directly evaluate $F(s) = G(s)/(1 + T(s))$ to find the analytical expression for $F(s)$.

8.2** Figure P8.2 shows the circuit diagram of a closed-loop controlled buck converter.

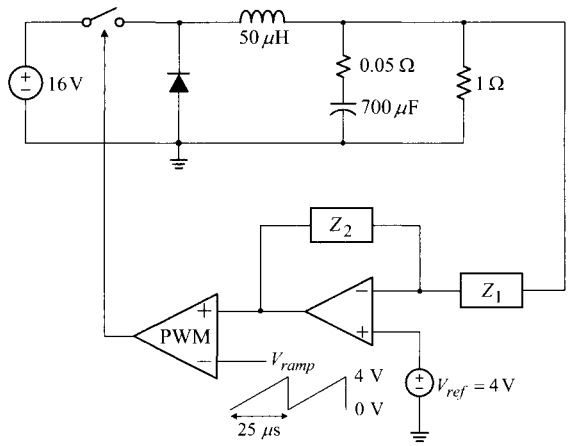


Fig. P8.2

a) Sketch the asymptotic plots for the power stage transfer functions of $|G_{vs}|$, $|G_{vd}|$, and $|Z_p|$. Show the values for the low- and high-frequency asymptotes and corner frequencies on your plots.

b) Assume that a single integrator $F_v(s) = Z_2(s)/Z_1(s) = K_v/s$ is employed as the voltage feedback compensation. Argue that the converter becomes marginally stable when the 0 dB crossover frequency of the loop gain occurs at the power stage double pole. Based on your argument, find the value for K_v that makes the converter marginally stable.

c) Assume that the following three-pole two-zero circuit is employed as the voltage feedback compensation

$$F_v(s) = \frac{K_v}{s} \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

i) Select the numerical values for $\{\omega_{z1}\ \omega_{z2}\ \omega_{p1}\ \omega_{p2}\}$ based on the compensation design procedures discussed in Section 8.4.2.

ii) Determine the integrator gain K_v in order to place the loop gain crossover frequency at the esr zero, while using the feedback compensation parameters determined in **i)**.

iii) Construct asymptotic plots for $|T_m|$, $|G_{vs}|$, and $|A_u|$ based on the results of **i)** and **ii)**. Find the expression for the audio-susceptibility in a factorized form. Specify the corner frequencies and leading coefficient of the audio-susceptibility. Evaluate the peak value of $|A_u|$.

8.3** The loop gain of a closed-loop controlled buck converter is shown in Fig. P8.3. Now assume that the three-pole two-zero compensation is used for the voltage feedback compensation. The feedback compensation parameters are selected as outlined in Section 8.4.2.

$$F_v(s) = \frac{K_v}{s} \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \qquad \text{with} \quad K_v = 2500$$

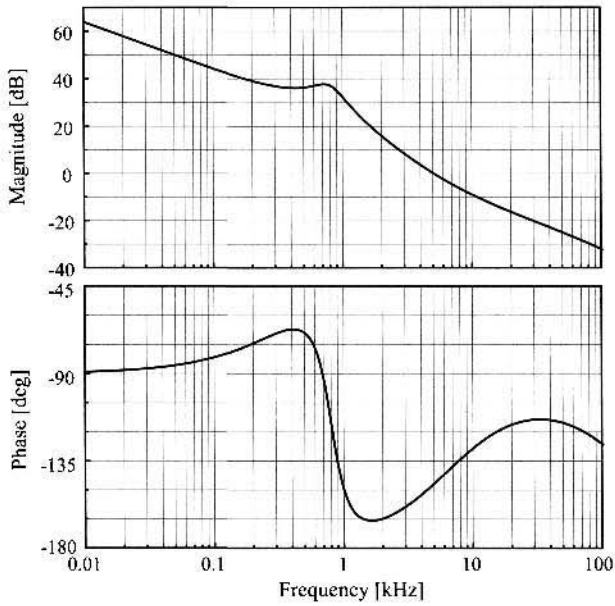


Fig. P8.3

a) Estimate the location of the power stage double pole.

b) Estimate the value for the first compensation zero, ω_{z1}.

c) Find the 0 dB crossover frequency and phase margin of the loop gain.

d) Sketch the polar plot of the loop gain. Show the 0 dB crossover frequency and phase margin on your plot.

e) Assume that the input voltage of the converter is $V_S = 12$ V. Find the modulator gain F_m of the PWM block. The current integrator gain is $K_v = 2500$.

f) Is it possible to make the converter unstable by changing only the integrator gain, K_v? Justify your answer.

g) Now assume that the integrator gain is varied between $250 < K_v < 25000$, while the other compensation parameters remain the same. The current

integrator gain is $K_v = 2500$. The change in the integrator gain will alter the loop gain characteristics. Find the range in the 0 dB crossover frequency f_c and phase margin ϕ_m of the loop gain. Arrange your answer in the form of ( ) < f_c < ( ) and ( ) < ϕ_m < ( ).

8.4* Figure P8.4 is the circuit diagram of a closed-loop controlled buck converter.

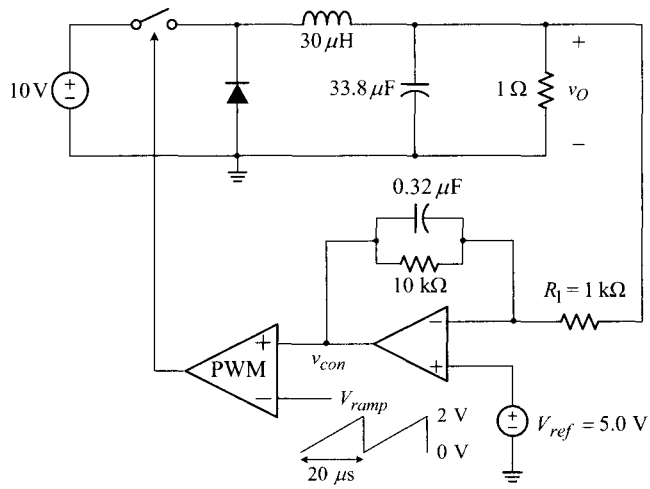


Fig. P8.4

a) Sketch the asymptotic plot for the loop gain magnitude. Show the values for the low-frequency asymptote, crossover frequency, and corner frequencies of the loop gain.

b) Find the average values for v_{con} and v_O. Specify your answer up to the three significant digits.

c) Sketch the asymptotic plot for the magnitude of the audio-susceptibility. Show the low-frequency asymptote value, peak value, and corner frequencies of the audio-susceptibility. Use the results of **a)** and **b)**.

d) Find the new value for R_1 that makes the converter marginally stable.

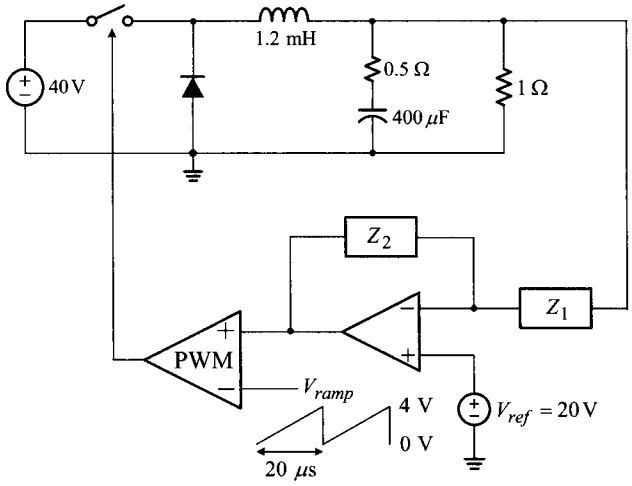
8.5 Shown in Fig. P8.5 are the circuit diagram of a closed-loop controlled buck converter and the asymptotic plots for its loop gain, input-to-output transfer function, and load current-to-output transfer function.

a) Find the numerical values for the frequencies X and Y specified in the blanks.

b) Determine the numerical values for A and B specified in the blanks.

c) Find the expression for voltage feedback compensation $F_v(s) = Z_2(s)/Z_1(s)$.

d) Sketch the asymptotic plots for $|A_u| = |G_{vs}|/|1 + T_m|$ and $|Z_o| = |Z_p|/|1 + T_m|$. Label the corner frequencies and peak value of the transfer functions.


1.2 mH
0.5 Ω
1 Ω
40 V
400 μF
Z_2
Z_1
PWM
V_{ramp}
4 V
0 V
20 μs
V_{ref} = 20 V

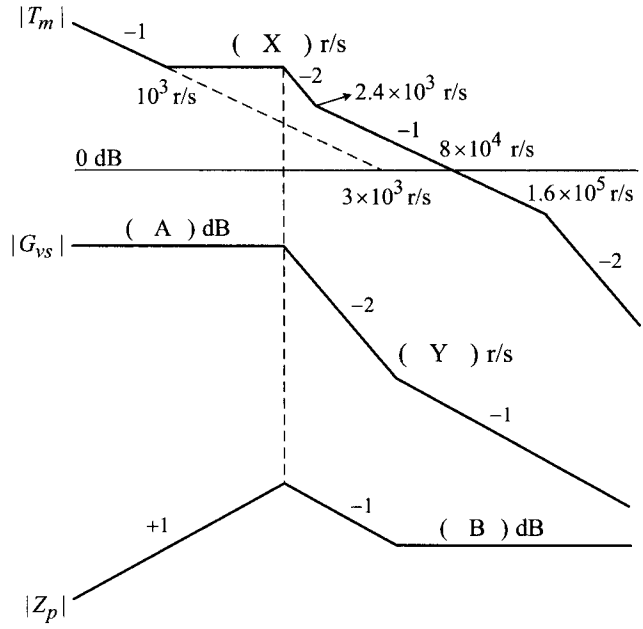

$|T_m|$
−1
(X) r/s
10^3 r/s
−2
2.4×10^3 r/s
−1
8×10^4 r/s
0 dB
3×10^3 r/s
1.6×10^5 r/s
$|G_{vs}|$
(A) dB
−2
−2
(Y) r/s
−1
+1
−1
(B) dB
$|Z_p|$

Fig. P8.5

8.6 The loop gain of a closed-loop controlled buck converter is shown in Fig. P8.6.

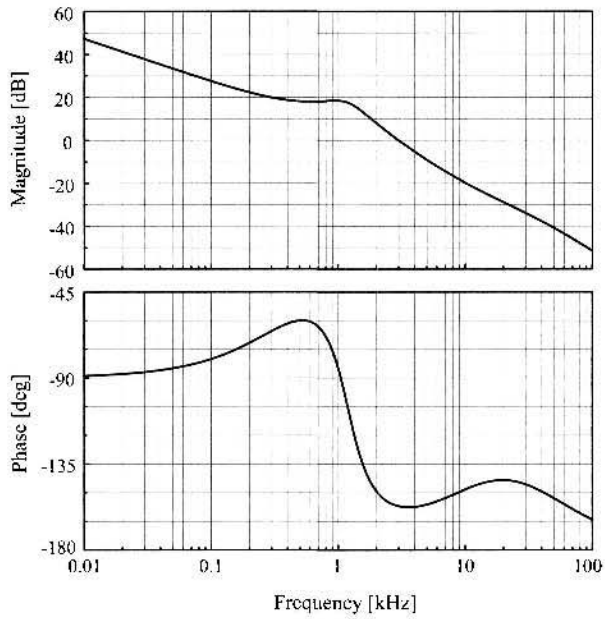


Fig. P8.6

a) Evaluate the phase margin and crossover frequency of the converter.

b) Assume the three-pole two-zero circuit is used for the voltage feedback compensation

$$F_v(s) = \frac{K_v}{s} \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

Identify the problems of the current compensation design and provide suggestions to improve the current design.

8.7* Figure P8.7 is the asymptotic magnitude plot for the loop gain of a buck converter. The buck converter employs the three-pole two-zero compensation, thus yielding the loop gain expression of

$$T_m(s) = \frac{K_t}{s} \frac{\left(1 + \frac{s}{\omega_{esr}}\right)\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}\right)\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

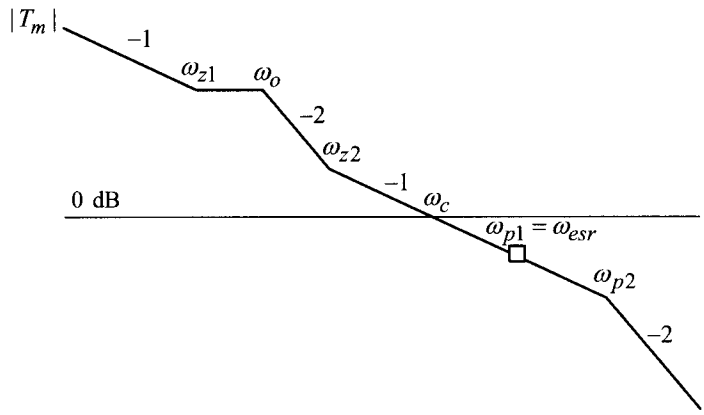


Fig. P8.7

a) Explain the reason for selecting $\omega_{z1} < \omega_o$.
b) Explain the considerations for choosing the position of ω_{z1}.
c) Describe the considerations for selecting the location of ω_{z2}.
d) Describe the reason for choosing $\omega_{p1} = \omega_{esr}$.
e) Why is the step load response always faster than the step input response?
f) Selections of the compensation parameters affect the performance of the converter in various ways. Table P8.7 table summarizes the impacts of changes in the value of the specific compensation parameters. Fill in the blanks in the table.

Table P8.7

	Benefits of moderate change	Side-effects due to excessive change
Increase in ω_{z1}	Fast step input response	( )
Increase in ω_{z2}	( )	( )
Decrease in ω_{p2}	( )	( )
Increase in K_m	( )	( )

8.8 Figure P8.8 is the functional block diagram of a closed-loop controlled buck converter. The voltage feedback compensation is given by

$$Z_1(s) = 500\frac{1 + \dfrac{s}{5 \times 10^4}}{1 + \dfrac{s}{5 \times 10^3}} \qquad Z_2(s) = \frac{7.5 \times 10^6\left(1 + \dfrac{s}{2 \times 10^4}\right)}{s\left(1 + \dfrac{s}{2 \times 10^5}\right)}$$

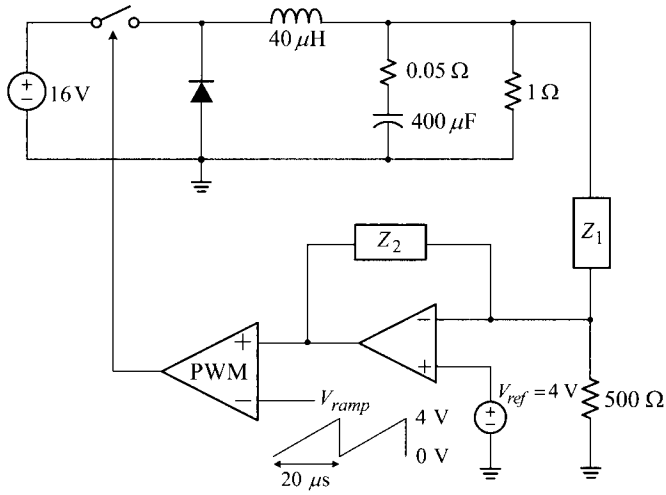


Fig. P8.8

a) Sketch the asymptotic plot of the loop gain $|T_m|$. Show all corner frequencies on your plot.

b) Sketch the asymptotic plot for the input-to-output transfer function $|G_{vs}|$. Show the low-frequency asymptote value and corner frequencies.

c) Assume that the 0 dB crossover frequency of $|T_m|$ occurs at $\omega_c = 5 \times 10^4$ rad/s. Sketch the asymptotic plot for the audio-susceptibility $|A_u|$ under this assumption. Show the peak value and the corner frequencies of the audio-susceptibility.

8.9* The loop gain of a closed-loop controlled buck converter is shown in Fig. P8.9.

a) Determine the stability of the converter.

b) Sketch the polar plot of the loop gain. Show all the prominent features of the loop gain on the polar plot.

c) Assume that the integrator gain K_v of the voltage feedback compensation is increased by 10 times. The other compensation parameters remain the same. What response is expected in the converter output?

d) Now assume that the integrator gain K_v is decreased by 10 times and the other compensation parameters remain the same. What will happen to the converter output?

8.10** Shown in Fig. P8.10 is the loop gain of a closed-loop controlled buck converter. Answer the questions.

a) Determine the stability of the converter.

b) Sketch the polar plot of the loop gain. Show all the important information on your sketch.

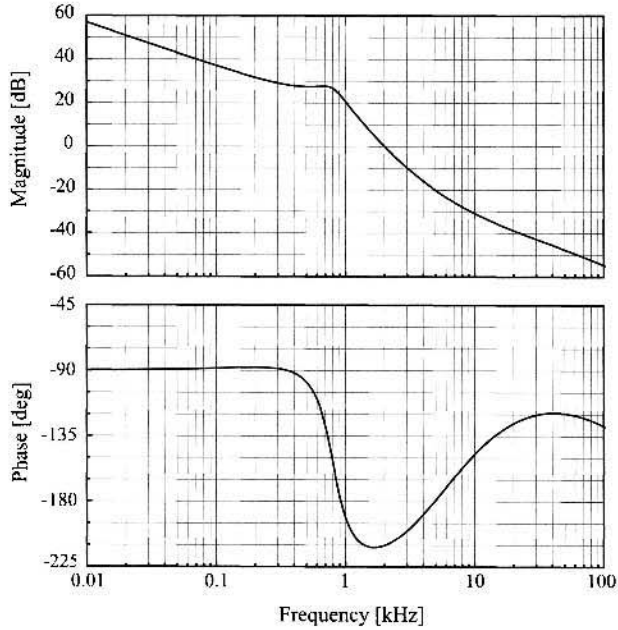


Fig. P8.9

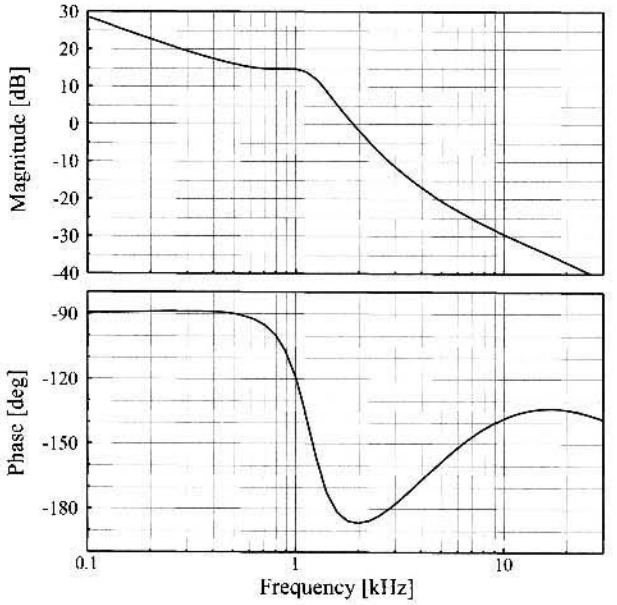


Fig. P8.10

c) The input voltage of the converter is $V_S = 16$ V and the magnitude of the PWM ramp signal is $V_m = 4$ V. Evaluate the integrator gain K_v of the current voltage feedback compensation.

d) What will happen to the converter output when the integrator gain K_v is increased by a factor of $20 \log 3.16 \approx 10$ dB? Assume the other compensation parameters remain the same.

e) Find two different values for K_v which would stabilize the converter with a 20° phase margin. Among these two values, which value would you prefer as your design choice? Justify your answer. Assume the other compensation parameters remain the same.

8.11* The loop gain of a closed-loop controlled buck converter is shown in Fig. P8.11.

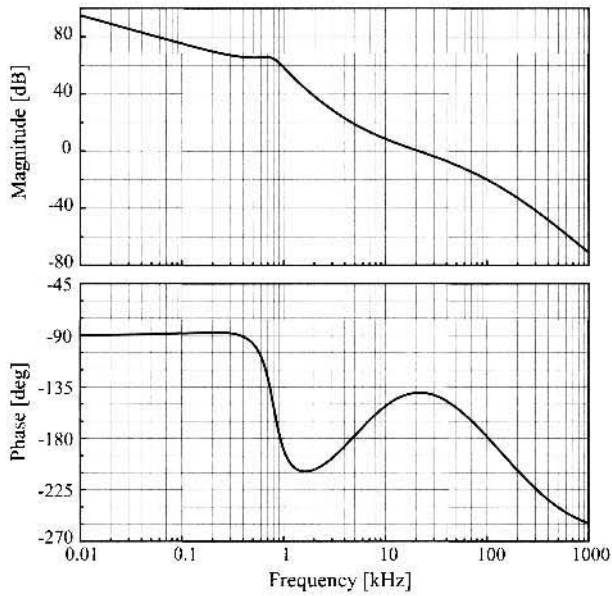


Fig. P8.11

a) Determine the stability of the converter.

b) Sketch the polar plot of the loop gain. Show all the prominent features of the polar plot.

Now assume the three-pole two-zero circuit is used for the voltage feedback compensation

$$F_v(s) = \frac{K_v}{s} \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

The current integrator gain is $K_v = 2500$. However, the integrator gain K_v will be varied in the following problems.

c) Find the ranges for K_v that destabilize the converter.

d) Find the value for K_v that produces a sustained oscillation at $\omega = 2\pi \cdot 10^5$ rad/s.

8.12** The audio-susceptibility $A_u(s)$ of a closed-loop controlled converter is given by $A_u(s) = G_{vs}(s)/(1+T_m(s))$ where $G_{vs}(s)$ is the input-to-output transfer function and $T_m(s)$ is the loop gain. Shown in Fig. P8.12 are asymptotic plots for $|G_{vs}|$ and $|T_m|$ of a closed-loop controlled converter.

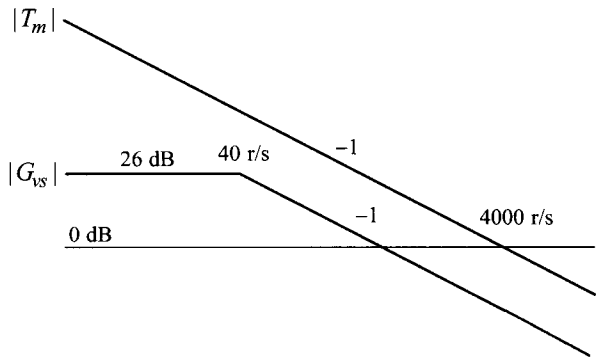


Fig. P8.12

a) Use the asymptotic analysis method to find an analytical expression for $A_u(s)$.

b) Directly evaluate the relationship $A_u(s) = G_{vs}(s)/(1 + T_m(s))$ to find the analytical expression for $A_u(s)$.

c) Now assume that a step increase of $V_{\text{step}} = 10$ V is occurred in the input voltage. Find the expression for the transitional waveform of the output voltage v_O. Also, draw the general shape of v_O and show all the important features of v_O.

8.13 Figure P8.13 shows the circuit diagram of a closed-loop controlled buck converter and the asymptotic plots of its loop gain $|T_m|$, duty ratio-to-output transfer function $|G_{vd}|$, and input-to-output transfer function $|G_{vs}|$. Answer the questions.

a) The duty ratio-to-output transfer function, $|G_{vd}|$, reveals a notable difference from the transfer function discussed in Section 8.3. What do you think causes the difference?

b) Estimate the phase margin and gain margin of the loop gain.

c) Evaluate the values for A, B, and C specified in the blanks.

d) Based on the information given in Fig. P8.13, find an expression for the voltage feedback compensation, $F_v(s) = Z_2(s)/Z_1(s)$. Express $F_v(s)$ in terms of the circuit and compensation parameters.

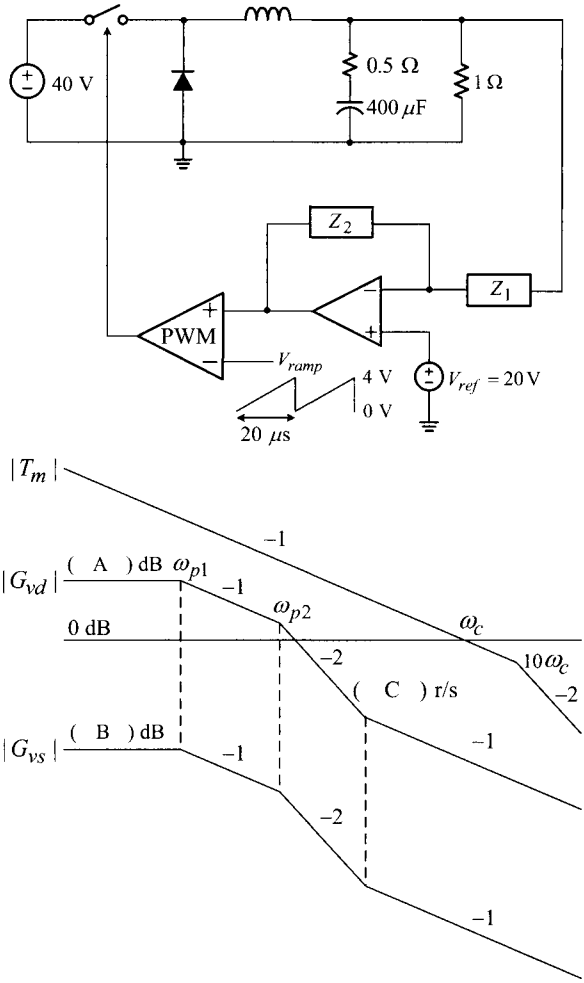


Fig. P8.13

e) Construct the asymptotic plot for the audio-susceptibility, $|A_u| = |G_{vs}|/|1 + T_m|$. Show the corner frequencies and slopes of asymptotes on your plot.

8.14** Consider Fig. P8.14 as the asymptotic plots for the load current-to-output transfer function $|Z_p|$ and the loop gain $|T_m|$ of a closed-loop controlled converter.

a) Sketch the asymptotic plot of the closed-loop output impedance $|Z_o|$. Show the peak value and corner frequencies of the asymptotic plot.

b) Derive an analytical expression for $Z_o(s)$.

c) Find an analytical expression for the output voltage in response to a 0.1 A step decrease in the load current.

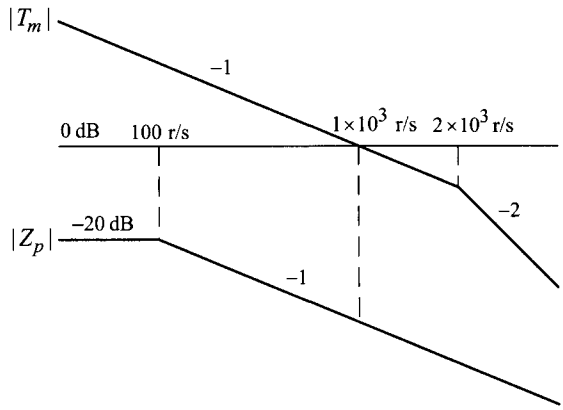


Fig. P8.14

8.15** Assume that the loop gain $T_m(s)$ of a certain closed-loop controlled converter is given by

$$T_m(s) = \frac{T_v(s)}{1 + T_i(s)}$$

where $T_v(s)$ and $T_i(s)$ are two different s-domain polynomials. The asymptotic plot for $|T_v|$ and $|T_i|$ are shown in Fig. P8.15.

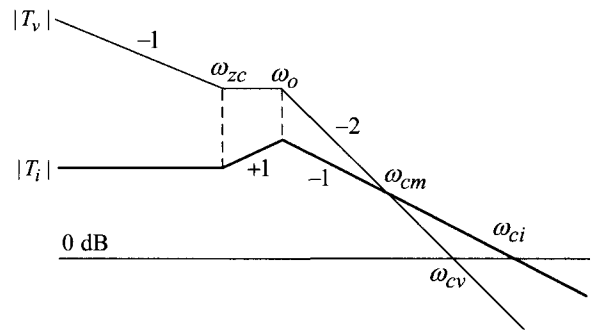


Fig. P8.15

a) Use the graphical asymptotic analysis method to find an analytical expression for the loop gain $T_m(s)$.

b) Evaluate the crossover frequency, phase margin, and gain margin of $T_m(s)$.

8.16* Figure P8.16 are the functional block diagram of a closed-loop controlled buck converter and the Bode plot of its loop gain. Assume that the Bode plot is evaluated with the parameters specified in the circuit diagram. Clearly, the converter is unstable with negative gain and phase margins. There are two different ways of changing the magnitude of the loop gain, while keeping its

phase characteristics unchanged. One way is to alter the resistance R_1 and the other way is to vary the magnitude of the ramp function, V_m. Currently, $R_1 = 10$ kΩ and $V_m = 1.6$ V are selected.

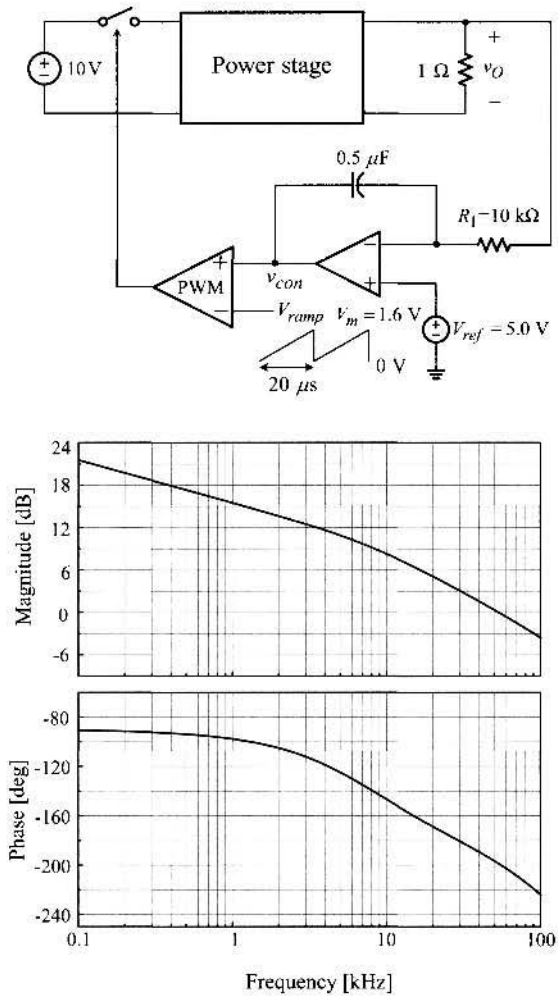


Fig. P8.16

a) Find a new value for R_1 that makes the converter marginally stable under the assumption that the other circuit parameters retain their original values. What do you think will be observed in the circuit waveforms of the converter? What will be observed in the transfer functions of the converter? Be specific and precise in your answer.

b) Find a new value for V_m that makes the converter stable with a phase margin of 60° under the assumption that the other circuit parameters maintain their original values.

8.17** The small-signal block diagram of a closed-loop controlled PWM converter is shown in Fig. P8.17.

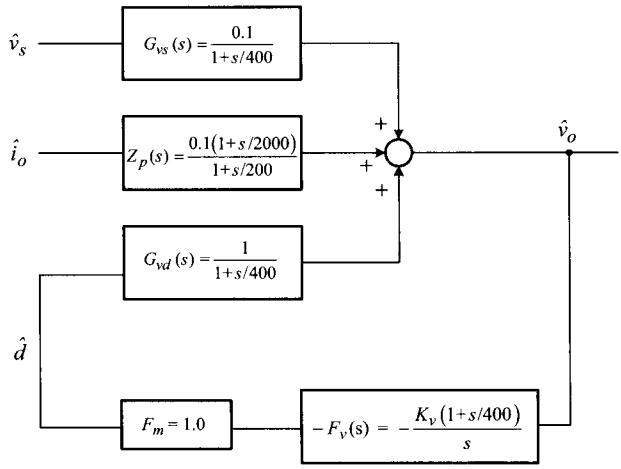


Fig. P8.17

a) Based on the information given in Fig. P8.17, sketch the asymptotic plots for the output impedance $|Z_o| = |\hat{v}_o/\hat{i}_o|$ for the following three cases of the integrator gain K_v in $F_v(s) = K_v(1 + s/400)/s$:

i) $K_v = 1000$ **ii)** $K_v = 2000$ **iii)** $K_v = 4000$

Show the corner frequencies and peak value of $|Z_o|$.

b) Now, sketch the asymptotic plots for the audio-susceptibility $|A_u| = |\hat{v}_o/\hat{v}_s|$ for the following three cases of K_v values:

i) $K_v = 1000$ **ii)** $K_v = 2000$ **iii)** $K_v = 4000$

Show the corner frequencies and the peak value of $|A_u|$.

8.18** Figure P8.18 shows the Bode plot of the load current-to-output transfer function $|Z_p|$ and output impedance $|Z_o|$ of a closed-loop controlled buck converter.

a) Find the 0 dB crossover frequency ω_c and phase margin ϕ_m of the converter loop gain.

b) Estimate the values for the esr and inductance of the power stage inductor.

c) Evaluate the values for the esr and capacitance of the power stage capacitor.

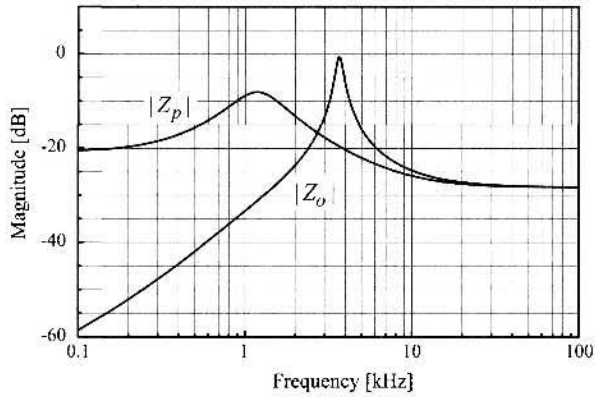


Fig. P8.18

8.19* The loop gain T_m of a closed-loop controlled dc-to-dc converter is shown in Fig. P8.19.

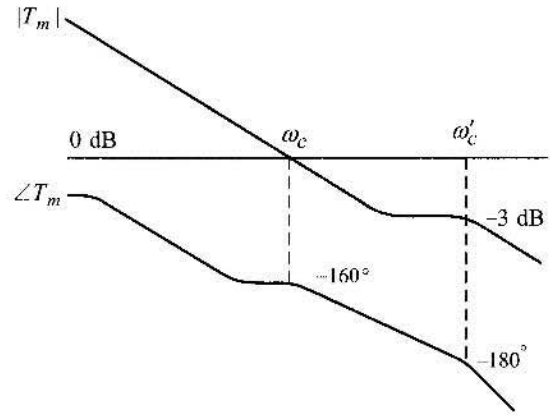


Fig. P8.19

a) Find the gain margin and phase margin of the converter.

b) As discussed in Section 8.4.4, the closed-loop transfer function exhibits a peaking at $\omega = \omega_c$ where $|T_m|$ crosses the 0 dB line. For the given system, evaluate the size of peaking in dB scale.

c) It can be shown that the closed-loop transfer function also shows a peaking at $\omega = \omega_c'$ where $\angle T_m$ becomes $-180°$. Derive an equation that describes the magnitude of the closed-loop transfer function at ω_c' and evaluate the size of the peaking in dB scale.

8.20** Figure P8.20 depicts the small-signal block diagram of a closed-loop controlled dc-to-dc converter. Assume the following transfer functions for the gain blocks:

$$G_{vd}(s) = \frac{20\left(1 + \frac{s}{4 \times 10^3}\right)}{\left(1 + \frac{s}{400}\right)\left(1 + \frac{s}{4 \times 10^4}\right)} \qquad G_{vs}(s) = \frac{0.5}{1 + \frac{s}{400}}$$

$$F_m = 0.25$$

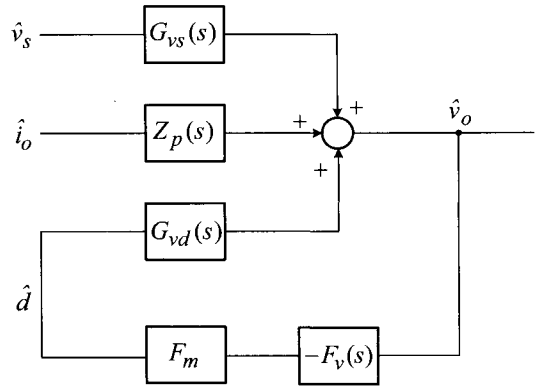


Fig. P8.20

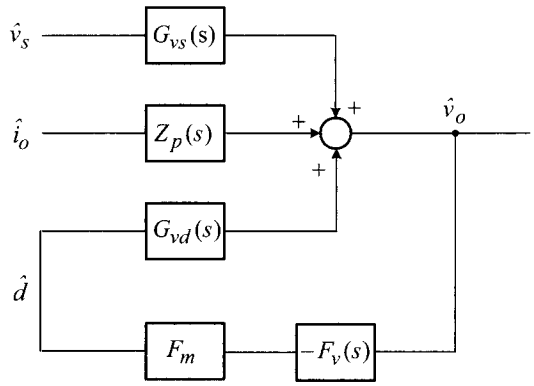
a) Find the expression for voltage feedback compensation, $F_v(s)$, which yields the following loop gain characteristics:
i) a −20 dB/dec slope from the *zero* frequency to the 0 dB crossover frequency located at $\omega_c = 4 \times 10^4$ rad/s, and
ii) a 45° phase margin.

b) Assuming the voltage feedback compensation found in **a)**, answer the following questions.
i) Sketch the asymptotic plot for the audio-susceptibility of the converter. Show the corner frequencies and peak value on your sketch.
ii) Find an expression for the output voltage $v_O(t)$ when the input voltage is given by $v_S(t) = 16 + 0.5 \sin 4000t$.

8.21** Shown in Fig. P8.21 are the small-signal block diagram of a closed-loop controlled buck converter and the asymptotic plot for its loop gain $|T_m|$. Assume the following transfer functions for the gain blocks in the block diagram:

$$G_{vd}(s) = \frac{50\left(1 + \dfrac{s}{2 \times 10^4}\right)}{\left(1 + \dfrac{s}{400}\right)\left(1 + \dfrac{s}{4 \times 10^5}\right)} \qquad Z_p(s) = \frac{10\left(1 + \dfrac{s}{8 \times 10^4}\right)}{1 + \dfrac{s}{400}}$$

$$F_m = 0.2$$



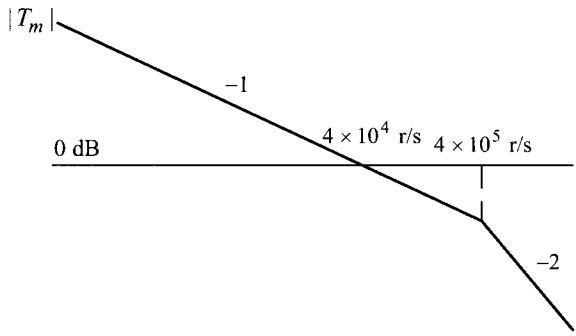


Fig. P8.21

a) Estimate the phase margin and gain margin of the converter.

b) Find an analytical expression for the voltage feedback compensation $F_v(s)$.

c) Sketch the asymptotic plot for the output impedance $|Z_o| = |Z_p|/|1 + T_m|$ and find the equation for $Z_o(s)$.

8.22** Shown in Fig. P8.22 are the Bode plot of the input-to-output transfer function $|G_{vs}|$ and audio-susceptibility $|A_u|$ of a closed-loop controlled buck converter.

a) Estimate the loop gain crossover frequency of the converter.

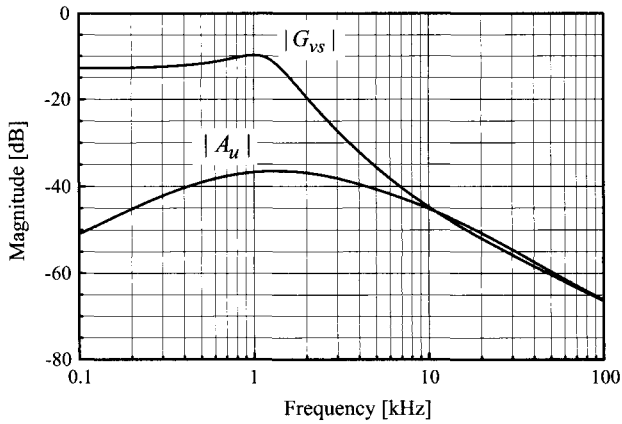


Fig. P8.22

b) Estimate the duty ratio of the converter.

c) Assume that $v_S(t) = 10 + 2\sin 2\pi \cdot 400t$ is applied to the input of the converter. Find an expression for the output voltage. Ignore the switching ripple component.

d) Estimate the settling time of the output voltage due to a step input change.

8.23** Figure P8.23 are the Bode plots of the load current-to-output transfer function $|Z_p|$ and output impedance $|Z_o|$ of a closed-loop controlled buck converter. Assume that the three-pole two-zero circuit is used for the voltage feedback compensation.

$$F_v(s) = \frac{K_v}{s} \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

Evaluate the following items based on the information given in the Bode plot of $|Z_p|$ and $|Z_o|$:

a) loop gain crossover frequency,

b) location of the first compensation zero ω_{z1},

c) location of the second compensation zero ω_{z2},

d) location of the esr zero of the power stage ω_{esr},

e) magnitude of the output voltage overshoot due to a 10 A step decrease in the load current, and

f) settling time of the output voltage due to a 10 A step decrease in the load current.

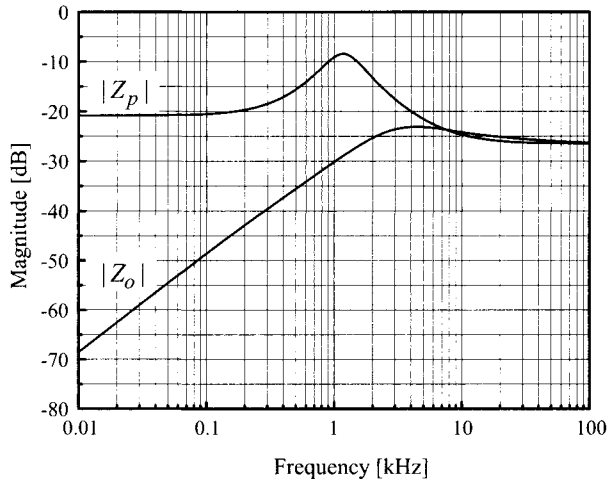


Fig. P8.23

8.24** Shown in Fig. P8.24 are the Bode plots of the input-to-output transfer function $|G_{vs}|$ and audio-susceptibility $|A_u|$ of another closed-loop controlled buck converter. Assume that the converter employs the same three-pole two-zero circuit discussed in the previous problem. Evaluate or illustrate the following items based on the information given in the Bode plot:

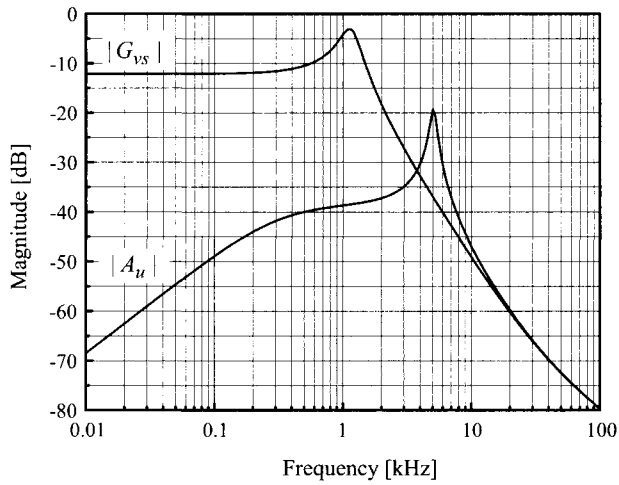


Fig. P8.24

a) loop gain crossover frequency,
b) phase margin of the loop gain,
c) location of the first compensation zero ω_{z1},

d) duty ratio of the converter D,

e) settling time of the output voltage due to a 10 V step increase in the input voltage, and

f) general shape of the output voltage due to a 10 V step increase in the input voltage.

8.25* The output impedance $Z_o(s)$ of a closed-loop controlled converter is given by $Z_o(s) = Z_p(s)/(1 + T_m(s))$ where $Z_p(s)$ is the load current-to-output transfer function and $T_m(s)$ is the loop gain. Shown in Fig. P8.25 are the asymptotic plots for $|Z_p|$ and $|T_m|$ of a closed-loop controlled converter.

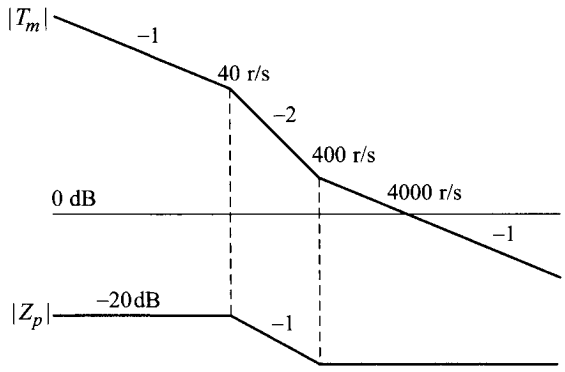


Fig. P8.25

a) Find the expressions for $Z_p(s)$ and $T_m(s)$.

b) Use the asymptotic analysis method to find the expression for $Z_o(s)$.

c) Now assume that a step decrease of $I_{step} = 10$ A is occurred in the load current. Find the expression for the transitional waveform of the output voltage v_O. Also, sketch v_O to show all important features of the waveform. Ignore the switching ripple component.

8.26* Figure P8.26 shows the loop gain characteristics of a closed-loop controlled buck converter. Assume the standard three-pole two-zero circuit for the voltage feedback compensation.

$$F_v(s) = \frac{K_v}{s} \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \qquad \text{with} \quad K_v = 1500$$

a) Evaluate the crossover frequency and phase margin of the loop gain.

b) Describe the characteristic features of the output impedance with the current design.

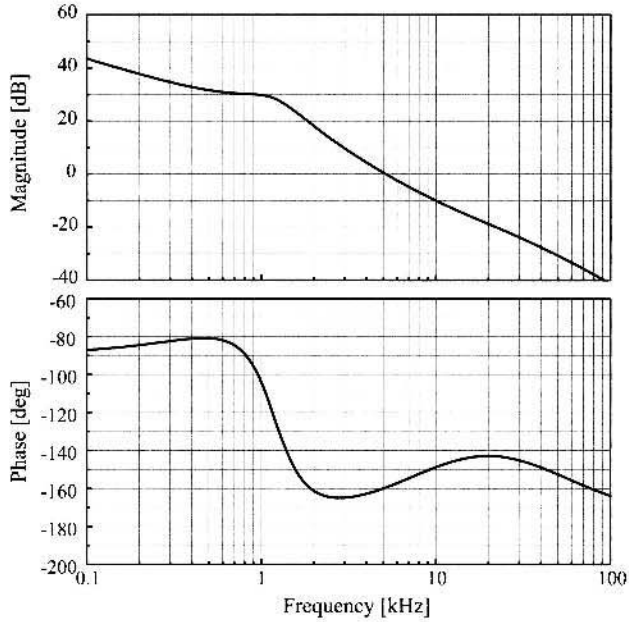


Fig. P8.26

c) Explain the characteristic features of the step load response with the current design.

d) Find the new value for K_v that offers a 60° phase margin. The current value of K_v is 1500. Assume the other compensation parameters remain unchanged. Although the new integrator gain provides the desired phase margin, the resulting design is considered unacceptable. State the reason for this.

e) Find the new value for K_v that offers the largest possible phase margin while locating the crossover frequency beyond the current position. Assume the other compensation parameters remain the same.

f) It is not feasible to practically obtain the largest phase margin evaluated in **e)**. Explain the reason for this and state the preferred design strategy.

CHAPTER 9

PRACTICAL CONSIDERATIONS IN MODELING, ANALYSIS, AND DESIGN OF PWM CONVERTERS

Up to this chapter, the modeling and control of dc-to-dc converters are discussed only for the three basic non-isolated converters operating in the continuous conduction mode (CCM) with an ideal voltage source and purely resistive load. However, real dc-to-dc converters encounter many other practical operational conditions. Practical considerations for realistic converter operations are listed below.

1) Although primarily intended for CCM operation, dc-to-dc converters enter discontinuous conduction mode (DCM) operation when the load current is reduced. Accordingly, dc-to-dc converters operate in both CCM and DCM, frequently crossing the borderline between them. The DCM operation should be accounted for in the analysis and design of dc-to-dc converters.

2) Isolated dc-to-dc converters are widely used for practical applications. The modeling and design method should be extended to isolated PWM dc-to-dc converters.

3) Dc-to-dc converters are usually powered by a non-ideal voltage source which presents a certain source impedance. The source impedance could deteriorate the converter dynamics and therefore should be incorporated in the analysis and design of dc-to-dc converters.

Pulsewidth Modulated Dc-to-Dc Power Conversion. By Byungcho Choi

4) The load of dc-to-dc converters is not a pure resistor but a combination of passive and active components which exhibit general impedance characteristics. The load impedance characteristics should be included in the analysis of converter performance.

The purpose of this chapter is to address the practical considerations in modeling, analysis, and design of dc-to-dc converters. This chapter illustrates the procedures of generalizing the outcomes of the earlier chapters and demonstrates the impacts of the departure from the *ideal* operational conditions on the dynamic performance of dc-to-dc converters. The analysis and design methodology, developed earlier in previous sections for the three basic converters under ideal conditions, will be proven to be adaptable to most real circumstances with non-ideal conditions.

9.1 GENERALIZATION OF PWM CONVERTER MODEL

In Chapters 5 and 6, the small-signal modeling and dynamic analysis were discussed based on several assumptions and restrictions on the converter operation. It was postulated that the parasitic resistances of the reactive components do not interfere with the modeling process and can be *freely* included in the small-signal model. This section will demonstrate that this is not an exact fact but is an acceptable presumption for most cases.

Earlier chapters only considered CCM operation in the small-signal modeling and dynamic analysis of dc-to-dc converters. When dc-to-dc converters enter DCM operation, the small-signal dynamics will be altered. The current section discusses the modeling and dynamic analysis in DCM operation.

The previous chapters exclusively dealt with the modeling and analysis of non-isolated converters. This section extends the earlier results to isolated PWM dc-to-dc converters, thereby allowing the existing techniques to be consistently adapted to all isolated/non-isolated PWM dc-to-dc converters.

9.1.1 Converter Modeling with Parasitic Resistances

The parasitic resistances of the reactive components affect the modeling process of dc-to-dc converters. This section presents the modeling of PWM converters at the presence of the parasitic resistances.

Buck Converter with Ideal Voltage Source

The buck converter powered by an ideal voltage source is one special case where the parasitic resistances *do not* affect the modeling process. Figure 9.1(a) shows the circuit diagram of a buck converter where the inductor and capacitor both contain parasitic resistances. Figure 9.1(b) illustrates the circuit waveforms of the PWM switch. It is evident from Fig. 9.1(b) that the equations for averaged circuit variables remain the same as those of Section 5.2.2

$$\bar{i}_a(t) = d\,\bar{i}_c(t)$$

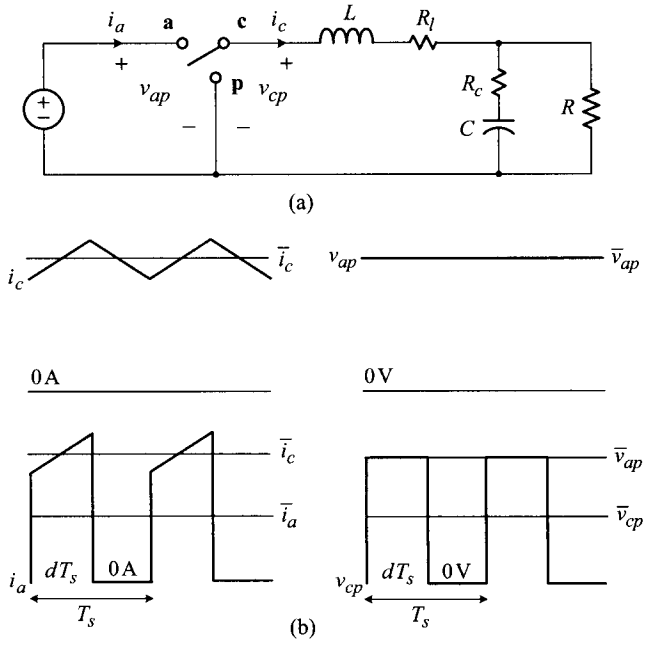


Figure 9.1 Buck converter with ideal voltage source. (a) Circuit diagram. (b) PWM switch waveforms.

$$\bar{v}_{cp}(t) = d\,\bar{v}_{ap}(t) \tag{9.1}$$

regardless of the presence of the parasitic resistances. Accordingly, the parasitic resistances can be included as add-ons to the small-signal model, as practiced in the previous chapters. This special case is only valid for the buck converter connected to an ideal voltage source.

Buck Converter with Input Filter

As shown in Fig. 9.1(b), the source current $i_a(t)$ delivered from the voltage source to the buck converter is a pulsating discontinuous current. For practical reasons including regulatory requirements, the buck converter usually employs a filter stage between the voltage source and power stage so that the voltage source only supplies the average or dc component of the input current.

The operation of an input filter is illustrated in Fig. 9.2, where the reactive filter components, L_f and C_f, are assumed to be sufficiently large. The voltage source supports the dc component of the input current, $\bar{i}_a(t)$, while the $R_d - C_f$ branch of the input filter carries the ac component of the input current, $\tilde{i}_a(t) = i_a(t) - \bar{i}_a(t)$. The resistance R_d provides an appropriate damping for the filter stage. The necessity and role of the input filter stage will be further discussed in Example 9.8 in Section 9.2.2.

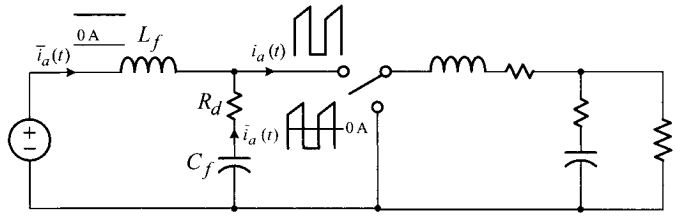


Figure 9.2 Buck converter with input filter.

The PWM switch waveforms with an input filter stage are shown in Fig. 9.3. As shown in Fig. 9.3(b), the input filter stage does not alter the current equation of the PWM switch, $\bar{i}_a(t) = d\,\bar{i}_c(t)$. However, the voltage equation is changed by the input filter stage. The voltage across the the active-passive terminal, v_{ap}, is divided into two components: the voltage across the filter capacitor, v_{C_f}, and the voltage across the damping resistor (in the opposite polarity to v_{C_f}), v_{R_d}. The filter capacitor voltage v_{C_f} supports the average value or dc portion of v_{ap}

$$v_{C_f}(t) = \bar{v}_{ap}(t) \tag{9.2}$$

On the other hand, the damping resistor voltage, v_{R_d}, is an ac voltage developed by the ac portion of $i_a(t)$

$$v_{R_d}(t) = \big(i_a(t) - \bar{i}_a(t)\big)R_d = \tilde{i}_a(t)R_d \tag{9.3}$$

The voltage v_{R_d} is a scaled replica of $i_a(t)$ with zero average value. The voltage waveforms v_{C_f} and v_{R_d} are illustrated in Fig. 9.3(c), where the voltage swing Δv_{R_d} is given by

$$\Delta v_{R_d} = \tilde{i}_c(t)R_d \tag{9.4}$$

The active-passive terminal voltage v_{ap} is now expressed as

$$v_{ap}(t) = v_{C_f}(t) - v_{R_d}(t) = \bar{v}_{ap}(t) - \tilde{i}_a(t)R_d \tag{9.5}$$

This waveform is shown in Fig. 9.3(d), where another dc voltage level, V_x, is defined to facilitate the derivation of the voltage equation. Lastly, the voltage across the common and passive terminals, $v_{cp}(t)$, is illustrated in Fig. 9.3(e).

It is evident from Fig. 9.3(e) that the average value of v_{cp} is given by

$$\bar{v}_{cp}(t) = d\,V_x \tag{9.6}$$

The above equation differs from the previous voltage equation of $\bar{v}_{cp} = d\,\bar{v}_{ap}$ because $V_x \neq \bar{v}_{ap}$. Now the remaining task is to find the expression for V_x, which is done using the detailed v_{ap} waveform in Fig. 9.4. From the graphical construction, it is recognized that the areas of the two shaded rectangles in Fig. 9.4 should be the same

$$(\bar{v}_{ap}(t) - V_x)dT_s = (V_x + \Delta v_{R_d} - \bar{v}_{ap}(t))d'T_s \tag{9.7}$$

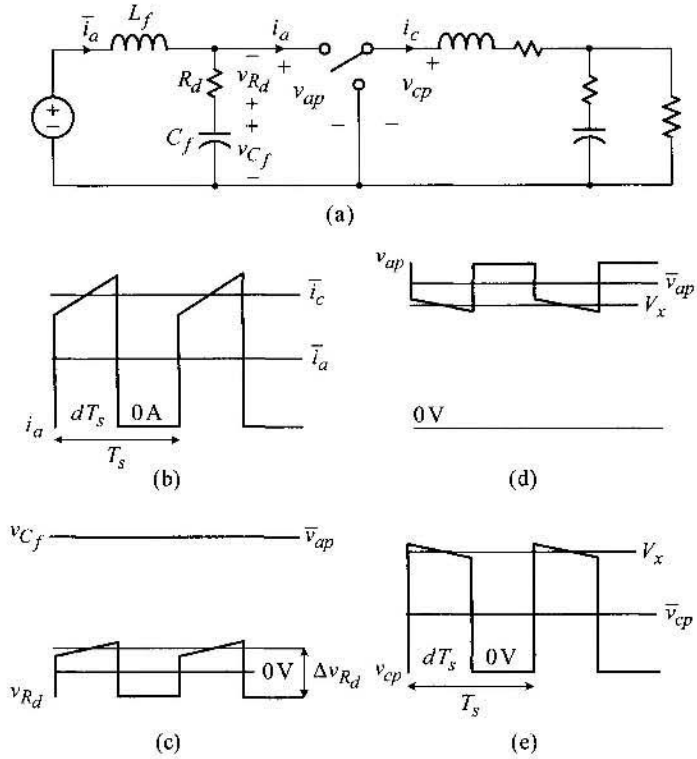


Figure 9.3 Buck converter with input filter stage. (a) Circuit diagram. (b)–(c) Circuit waveforms of PWM switch.

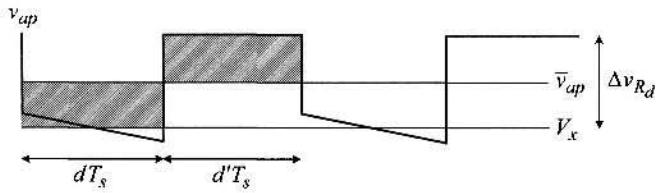


Figure 9.4 Active-passive terminal voltage waveform.

which is simplified to

$$V_x = \bar{v}_{ap}(t) - \Delta v_{R_d} d' = \bar{v}_{ap}(t) - R_d \bar{i}_c(t) d' \tag{9.8}$$

Using the notation of $R_d = r_{ap}$, the above expression is rewritten as

$$V_x = \bar{v}_{ap}(t) - r_{ap} \bar{i}_c(t) d' \tag{9.9}$$

The symbol r_{ap} signifies the ac resistance between the active and passive terminals, which can be found by opening L_f and shorting C_f. The final averaged voltage equation is then given by

$$\bar{v}_{cp}(t) = dV_x = d\left(\bar{v}_{ap}(t) - r_{ap}\bar{i}_c(t)d'\right) \tag{9.10}$$

Linearization of Averaged PWM Switch Equation

The results of the previous analysis are generalized for the three basic converters shown in Fig. 9.5. For all three converters, the averaged circuit equations are given by

$$\begin{aligned} \bar{i}_a(t) &= d\,\bar{i}_c(t) \\ \bar{v}_{cp}(t) &= d\left(\bar{v}_{ap}(t) - r_{ap}\bar{i}_c(t)d'\right) \end{aligned} \tag{9.11}$$

where

$$r_{ap} = \begin{cases} 0 & \text{for buck converter without input filter} \\ R_d & \text{for buck converter with input filter} \\ R_c \parallel R & \text{for boost and buck/boost converters} \end{cases}$$

The ac resistance between the active-passive terminal, r_{ap}, is identified from Fig. 9.5. The r_{ap} carries the ac component of the active terminal current, $\tilde{i}_a(t) = i_a(t) - \bar{i}_a(t)$, as shown in Fig. 9.5. For the standalone buck converter, it is obvious that $r_{ap} = 0$.

Application of the linearization process to (9.11) yields

$$\begin{aligned} I_a + \hat{i}_a(t) &= (D + \hat{d}(t))(I_c + \hat{i}_c(t)) \\ V_{cp} + \hat{v}_{cp}(t) &= \left(D + \hat{d}(t)\right) \\ &\quad \left((V_{ap} + \hat{v}_{ap}(t)) - r_{ap}(I_c + \hat{i}_c(t))(1 - (D + \hat{d}))\right) \end{aligned} \tag{9.12}$$

By equating the first-order ac components from (9.12), the small-signal representation of (9.11) is obtained

$$\begin{aligned} \hat{i}_a(t) &= D\,\hat{i}_c(t) + I_c\,\hat{d}(t) \\ \hat{v}_{cp}(t) &= D\,\hat{v}_{ap}(t) + V_D\,\hat{d}(t) - \hat{i}_c(t)\,DD'\,r_{ap} \end{aligned} \tag{9.13}$$

with

$$V_D = V_{ap} + I_c(D - D')r_{ap} \tag{9.14}$$

The circuit model for the above small-signal equations is given in Fig. 9.6. With $r_{ap} = 0$, the circuit model reduces to the previous small-signal model which does not incorporate the effects of r_{ap}.

Predictions of Refined Small-Signal Model

The ac resistance between the active-passive terminal, r_{ap}, alters the dependent voltage source and introduces an additional resistance to the small-signal model of

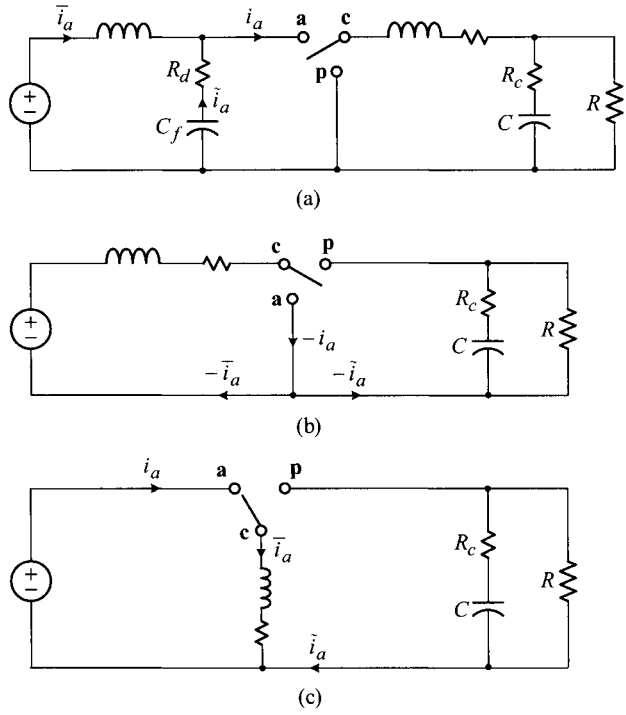


Figure 9.5 Circuit diagram of three basic converters. (a) Buck converter with input filter. (b) Boost converter. (c) Buck/boost converter.

the PWM switch. These changes only influence the dc gain and damping ratio of transfer functions and their consequential effects will not be substantial unless the ac resistance r_{ap} is unusually large. Accordingly, the transfer functions of the refined model will largely be the same as those of the previous model which ignores the impact of r_{ap}.

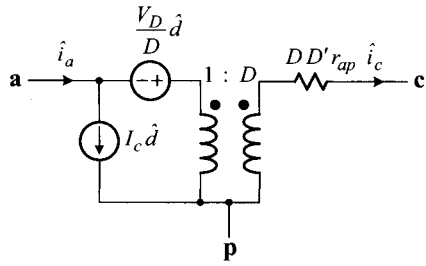


Figure 9.6 Refined small-signal model for PWM switch.

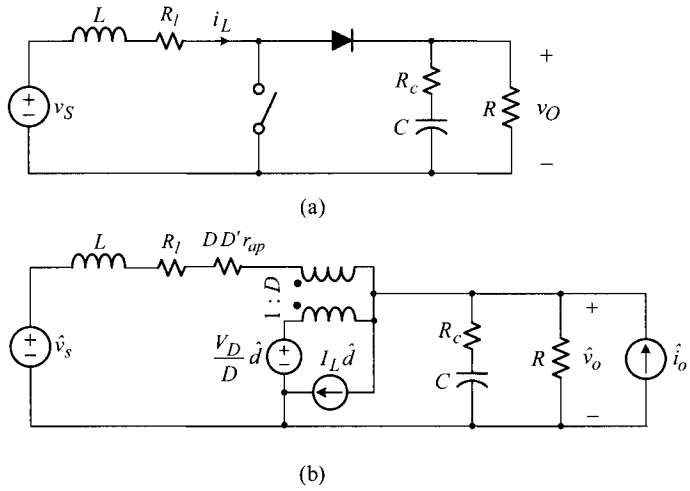


Figure 9.7 Boost converter. (a) Circuit diagram. (b) Small-signal model.

■ EXAMPLE 9.1 Boost Converter Example

This example illustrates the prediction of the refined small-signal model. Figure 9.7 shows a boost converter and its small-signal model. In the small-signal model, the ac resistance r_{ap} is given by

$$r_{ap} = R_c \parallel R$$

and the dc voltage source V_D is expressed as

$$V_D = -V_O - I_L(D - D')r_{ap}$$

The operational conditions and circuit parameters of the boost converter are $V_S = 15$ V, $L = 800\ \mu$H, $R_l = 0.01\ \Omega$, $C = 1000\ \mu$F, $R_c = 0.1\ \Omega$, $R = 2\ \Omega$, $f_s = 10$ kHz, and $D = 0.25$. Figure 9.8 compares the duty ratio-to-output transfer functions of the converter, simulated with two different conditions. One simulation is with $r_{ap} = R \parallel R_c$ and the other simulation is with $r_{ap} = 0$, that is, ignoring the consequence of r_{ap}. The difference between the transfer functions is nearly undetectable.

As demonstrated in the previous example, the impacts of r_{ap} are negligible for most cases. In this book, the earlier small-signal model without r_{ap} will be continuously used for notational simplicity. Nonetheless, the refined model with r_{ap} will be employed to all forthcoming PSpice® simulations.

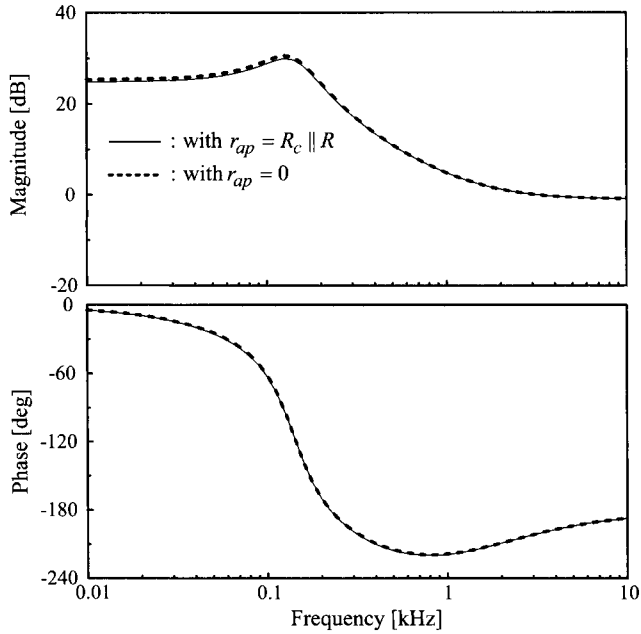


Figure 9.8 Duty ratio-to-output transfer function of boost converter.

9.1.2 Modeling and Analysis of PWM Converters in DCM Operation

The operation of practical dc-to-dc converters spans both CCM and DCM regions. As a dc-to-dc converter departs from CCM and enters DCM operation, its small-signal dynamics will be altered, thereby requiring a new small-signal model and new analysis.

Averaged Equations for PWM Switch in DCM

The buck/boost converter is selected to illustrate the modeling of DCM dynamics. The modeling results are invariant with the selected converter topology and thus can be extended to all the three basic dc-to-dc converters. In the buck/boost converter circuit in Fig. 9.9(a), the following relationships hold

$$\begin{aligned} \bar{v}_{ac}(t) &= V_S \\ \bar{v}_{cp}(t) &= V_O \end{aligned} \tag{9.15}$$

because the average value of the inductor voltage is zero, $\bar{v}_L = 0$, due to the volt-sec balance condition.

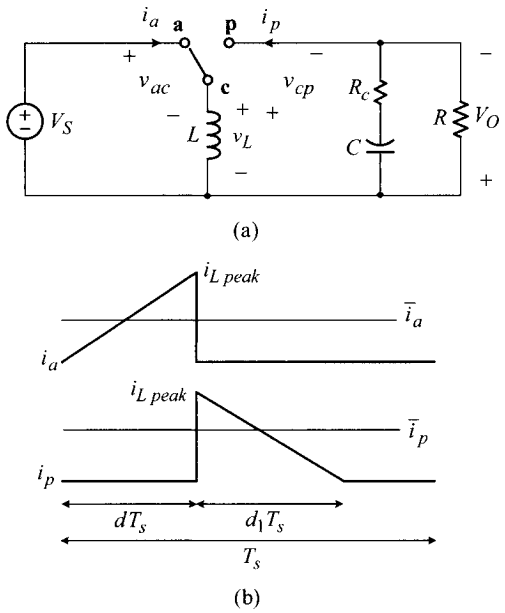


Figure 9.9 Buck/boost converter and DCM waveforms of PWM switch. (a) Buck/boost converter. (b) PWM switch waveforms in DCM.

The current waveforms of the PWM switch in Fig. 9.9(b) indicate that

$$\begin{aligned} \bar{i}_a(t) &= \frac{\frac{1}{2} i_{L\,peak}\, dT_s}{T_s} = \frac{i_{L\,peak}}{2} d \\ \bar{i}_p(t) &= \frac{\frac{1}{2} i_{L\,peak}\, d_1 T_s}{T_s} = \frac{i_{L\,peak}}{2} d_1 \end{aligned} \tag{9.16}$$

where $i_{L\,peak}$ is the peak value of the inductor current. Expressions (9.16) yield the averaged current equation

$$\bar{i}_a(t) = \frac{d}{d_1} \bar{i}_p(t) \tag{9.17}$$

Two different expressions for $i_{L\,peak}$ are formulated from Fig. 9.9

$$\begin{aligned} i_{L\,peak} &= \frac{V_S}{L} dT_s = \frac{\bar{v}_{ac}(t)}{L} dT_s \\ i_{L\,peak} &= \frac{V_O}{L} d_1 T_s = \frac{\bar{v}_{cp}(t)}{L} d_1 T_s \end{aligned} \tag{9.18}$$

to produce the averaged voltage equation for the PWM switch

$$\bar{v}_{ac}(t) = \frac{d_1}{d} \bar{v}_{cp}(t) \tag{9.19}$$

Using (9.16) and (9.18), the parameter d_1 is expressed in terms of the average circuit variables and operational conditions

$$d_1 = \frac{2Lf_s}{d}\frac{\bar{i}_a(t)}{\bar{v}_{cp}(t)} = \frac{2Lf_s}{d}\frac{\bar{i}_p(t)}{\bar{v}_{ac}(t)} \tag{9.20}$$

where $f_s = 1/T_s$ is the switching frequency. Expressions (9.17), (9.19), and (9.20) are combined together to establish a set of equations that describe the averaged dynamics of the PWM switch in DCM operation

$$\begin{aligned} \bar{i}_a(t) &= \mu\,\bar{i}_p(t) \\ \bar{v}_{cp}(t) &= \mu\,\bar{v}_{ac}(t) \end{aligned} \tag{9.21}$$

with

$$\mu = \frac{d}{d_1} = \frac{d^2\,\bar{v}_{cp}(t)}{2Lf_s\bar{i}_a(t)} = \frac{d^2\,\bar{v}_{ac}(t)}{2Lf_s\bar{i}_p(t)} \tag{9.22}$$

Linearization of Averaged Equation and Small-Signal Circuit Model

By combining (9.21) and (9.22) and linearizing the resulting equations, a set of small-signal equations are obtained [1]

$$\begin{aligned} \hat{i}_a(t) &= \frac{1}{r_i}\hat{v}_{ac}(t) + k_i\hat{d}(t) \\ \hat{i}_p(t) &= g_f\hat{v}_{ac}(t) + k_o\hat{d}(t) + \frac{1}{r_o}\hat{v}_{pc}(t) \end{aligned} \tag{9.23}$$

with

$$r_i = \frac{V_{ac}}{I_a} \qquad k_i = \frac{2I_a}{D}$$

$$g_f = \frac{2I_p}{V_{ac}} \qquad k_o = \frac{2I_p}{D} \quad \text{and} \quad r_o = \frac{V_{cp}}{I_p} \tag{9.24}$$

The above equations constitute the small-signal equation of the PWM switch in DCM operation. Derivations of (9.23) and (9.24) are discussed in Problem 9.1 at the end of this chapter.

A straightforward circuit representation of the small-signal equations in (9.23) is shown in Fig. 9.10. This circuit model is referred to as the *DCM PWM switch model*. The DCM PWM switch model includes two resistive parameters, r_i and r_o. These resistive parameters dictate the small-signal dynamics of the model, as will be demonstrated shortly. Now, DCM small-signal models for the three basic converters are obtained by replacing the PWM switch with the DCM PWM switch model. Figure 9.11 shows a buck/boost converter and its DCM small-signal model.

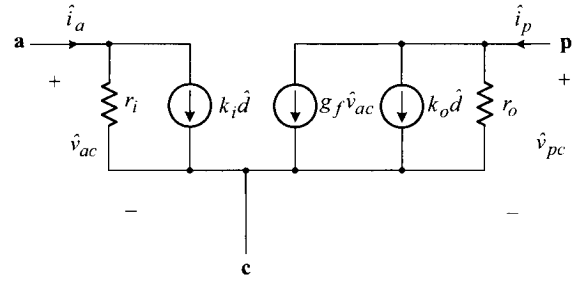


Figure 9.10 Small-signal model for PWM switch in DCM operation.

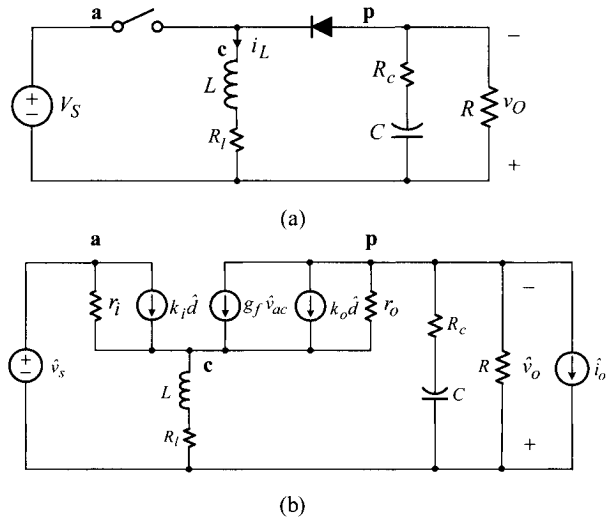


Figure 9.11 Buck/boost converter and DCM small-signal model. (a) Buck/boost converter. (b) DCM small-signal model.

■ EXAMPLE 9.2 DCM Small-Signal Model of Buck/Boost Converter

This example shows the prediction of the DCM small-signal model of a buck/boost converter. For the buck/boost converter, the parameters of DCM PWM switch model in (9.24) are given by

$$r_i = \frac{V_S}{DI_L} \qquad k_i = 2I_L \quad g_f = \frac{2M}{R}$$

$$k_o = \frac{2MV_S}{DR} \quad r_o = R \quad \text{with} \quad I_L = \frac{M^2V_S}{DR} \quad \text{and} \quad M = D\sqrt{\frac{RT_S}{2L}}$$

Readers are encouraged to prove the above expressions for the DCM PWM switch model parameters. The operational conditions of the buck/boost con-

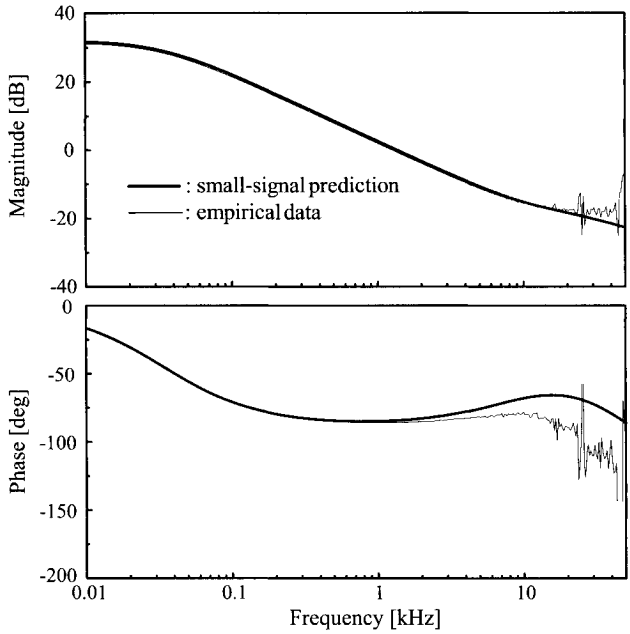


Figure 9.12 $G_{vd}(s)$ of buck/boost converter in DCM.

verter are $V_S = 18$ V, $L = 40\ \mu$H, $R_l = 0.01\ \Omega$, $C = 470\ \mu$F, $R_c = 0.03\ \Omega$, $R = 20\ \Omega$, $f_s = 50$ kHz, and $D = 0.25$. The critical resistance that places the converter on the CCM/DCM boundary is

$$R_{crit} = \frac{2L}{(1-D)^2 T_s} = \frac{2 \cdot 40 \times 10^{-6}}{(1-0.25)^2\, 20 \times 10^{-6}} = 7.1\ \Omega$$

With $R = 20\ \Omega$, the converter is in deep DCM operation. The duty ratio-to-output transfer function is simulated using the DCM small-signal model in Fig. 9.11(b). Figure 9.12 shows the prediction of the small-signal model, in comparison with the empirical result obtained using the computational method discussed in Example 8.5 in Chapter 8.

Analysis of DCM Small-Signal Dynamics

Although the DCM PWM switch model in Fig. 9.10 is well suited for the frequency-domain simulations, it is necessary to analyze the DCM PWM switch model, in order to obtain analytic expressions for transfer functions. Such analyses were performed in [1] and the results are summarized in Table 9.1. As shown in the table, the duty ratio-to-output transfer function, $G_{vd}(s)$, of all the three basic PWM converters has

Table 9.1 Expressions for $G_{vd}(s)$ for Three Basic Converters in DCM

$$G_{vd}(s) = K_d \frac{\left(1 - \frac{s}{\omega_{rhp}}\right)\left(1 + \frac{s}{\omega_{esr}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

Buck converter	
$K_d = \frac{2V_O}{D}\frac{1-M}{2-M}$ with $M = \frac{2D}{D + \sqrt{D^2 + \frac{8L}{RT_s}}}$	
$\omega_{p1} = \frac{1}{CR}\frac{2-M}{1-M}$	$\omega_{p2} = 2f_s\left(\frac{M}{D}\right)^2$
$\omega_{rhp} = \infty$	$\omega_{esr} = \frac{1}{CR_c}$
Boost converter	
$K_d = \frac{2V_O}{D}\frac{M-1}{2M-1}$ with $M = \frac{1}{2}\left(1 + \sqrt{1 + \frac{2D^2RT_s}{L}}\right)$	
$\omega_{p1} = \frac{1}{CR}\frac{2M-1}{M-1}$	$\omega_{p2} = 2f_s\left(\frac{1-1/M}{D}\right)^2$
$\omega_{rhp} = \frac{R}{M^2L}$	$\omega_{esr} = \frac{1}{CR_c}$
Buck/boost converter	
$K_d = \frac{V_O}{D}$	$M = D\sqrt{\frac{RT_s}{2L}}$
$\omega_{p1} = \frac{2}{CR}$	$\omega_{p2} = 2f_s\left(\frac{1/D}{1+1/M}\right)^2$
$\omega_{rhp} = \frac{R}{M(1+M)L}$	$\omega_{esr} = \frac{1}{CR_c}$

For the buck converter, ω_{rhp} does not exist so $\omega_{rhp} = \infty$ is used.

the common structure of

$$G_{vd}(s) = K_d \frac{\left(1 - \frac{s}{\omega_{rhp}}\right)\left(1 + \frac{s}{\omega_{esr}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \tag{9.25}$$

The denominator of the DCM $G_{vd}(s)$ consists of two real poles, in contrast to a complex double pole in the CCM case, thereby producing distinct DCM small-signal dynamics.

■ EXAMPLE 9.3 Analysis of DCM Dynamics

This example presents qualitative discussions about the DCM small-signal dynamics of the buck/boost converter. Figure 9.13 shows a family of the duty ratio-to-output transfer functions of the buck/boost converter used in Example 9.2. The DCM transfer functions, evaluated with $R = 7.1\ \Omega$, $10\ \Omega$, and $20\ \Omega$, are shown in comparison with the CCM transfer functions with $R = 0.2\ \Omega\,(Q = D'R\sqrt{C/L} = 0.5)$, $0.4\ \Omega\,(Q = 1)$, and $1\ \Omega\,(Q = 2.5)$. The critical resistance of the converter was $R_{crit} = 7.1\ \Omega$ in Example 9.2.

The CCM transfer functions demonstrate the presence of the double pole at $\omega_o = D'\sqrt{1/(LC)} = 2\pi \cdot 871$ rad/s with the respective peaking of $20 \log Q$. As the converter moves into DCM operation, the transfer function exhibits notable changes.

1) The double pole is heavily damped and split into two real poles, ω_{p1} and ω_{p2} in (9.25). The cause of this damping is the two resistive parameters, $r_i = V_S/(DI_L)$ and $r_o = R$, in the DCM PWM switch model. The damping will intensify as the load resistance R becomes larger. Referring to the $G_{vd}(s)$ expression of the buck/boost converter in Table 9.1, the behavior of the two real poles are described below.

   - The first real pole, $\omega_{p1} = 2/(RC)$, appears at lower frequencies and approaches the origin as R increases towards infinity.
   - The second pole ω_{p2} usually occurs at higher frequencies than ω_s/π.

2) Up to the frequency ω_s/π, the transfer function is dominated by the first pole and exhibits the first-order dynamics. The second pole only becomes influential at very high frequencies and virtually vanishes from the converter dynamics at the frequencies of practical importance. The first-order system behavior is apparent in both magnitude and phase characteristics.

3) Due to the emergence of the first pole at low frequencies, the magnitude of the transfer function is substantially reduced. The reduction in the magnitude will adversely affect the closed-loop performance in DCM, as will be shown later.

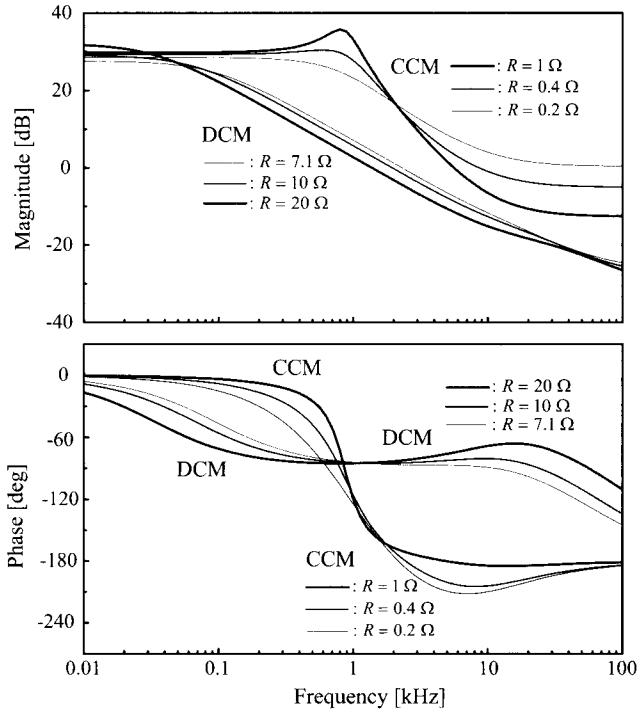


Figure 9.13 $G_{vd}(s)$ of buck/boost converter in CCM to DCM operations.

As demonstrated in the buck/boost converter example, the DCM operation effectively transforms the second-order system into the first-order system. By examining $G_{vd}(s)$ expressions in Table 9.1, the same conclusion is extended to buck and boost converters. This apparent change in power stage dynamics should be considered for dc-to-dc converters encountering both CCM and DCM operations.

Control Design and Closed-Loop Performance in DCM

For the control design purpose, it is necessary to investigate the duty ratio-to-output transfer function in both CCM operation and DCM operation. As illustrated in Fig. 9.13, the $G_{vd}(s)$ in CCM presents worse characteristics than the $G_{vd}(s)$ in DCM. The double pole in the CCM transfer function causes a 180° phase drop to $\angle G_{vd}$. This abrupt and large phase delay was the main concern in designing the voltage feedback compensation. In contrast, the DCM transfer function only exhibits a gradual 90° phase delay.

The $G_{vd}(s)$ in CCM operation should be used as the basis for the control design. If the control is designed for DCM operation, the converter becomes unstable when it enters CCM operations due to the excessive phase delay in CCM operation. On

the contrary, the control design tailored for the worst case CCM operation will offer stable operation for both CCM and DCM. Thus, the rational choice is to design the controller for CCM operation and to predict the closed-loop performance in DCM operation.

For CCM operations, the control can be optimally designed based on the CCM dynamics of the converter. When the converter enters DCM operations, $G_{vd}(s)$ will change as illustrated in Fig. 9.13. This change will affect the converter dynamics. In particular, the reduction in $|G_{vd}|$ will directly propagate to the loop gain characteristics and consequently alter other closed-loop performance. Even so, the change in $G_{vd}(s)$ does not jeopardize the stability of the converter, as will be demonstrated in the following example.

■ EXAMPLE 9.4 Performance of Buck Converter in DCM Operation

This example investigates the performance of the buck converter in both CCM and DCM operations, whose control is designed for one particular CCM operation. For this purpose, the buck converter used in Example 8.2 is revisited and its performance is evaluated over a wide operational range to include both CCM and DCM operations. As elaborated in Example 8.2, the control design is optimized for the CCM operation with $R = 1\ \Omega$. The critical resistance of the buck converter is determined as $R_{crit} = 2L/(D'T_s) = 5.33\ \Omega$.

Figure 9.14 shows the loop gain characteristics of the buck converter evaluated for both CCM and DCM operations. For CCM operations, $R = 0.5\ \Omega$, $R = 1\ \Omega$, and $R = 2\ \Omega$ are used. On the other hand, $R = R_{crit} = 5.33\ \Omega$, $R = 10\ \Omega$, and $R = 20\ \Omega$ are selected for DCM operations. The other conditions are the same as those of Example 8.2. The mid-band gain reduction in $|G_{vd}|$ flows into the DCM loop gain characteristics, producing much narrower crossover frequencies. Nonetheless, the loop gains demonstrate that the converter remains stable, even with larger phase margins, in DCM operations. This justifies the validity of the control design — *the control design offering a stable CCM operation also guarantees stability in DCM operations.*

The reduced mid-band gain and narrower crossover frequency provide only small attenuation for closed-loop transfer functions. Figure 9.15 compares the output impedances evaluated with the same conditions. As predicted, the DCM output impedances show inferior characteristics with a much larger $|Z_o|_{peak}$. In addition, the first pole of the DCM output impedances, labeled as ω_{pz} in Fig. 9.15, occurs at much lower frequencies.

The degradation in the output impedance in DCM operations is the predicted consequence of using the voltage feedback compensation designed for a CCM operation. The control might be initially optimized for the DCM operation for the improved output impedance characteristics. However, for that case, the converter instantly becomes unstable when it enters CCM operations.

As analyzed in Section 8.4.6, there is a direct correlation between the output impedance and step load response. The inferior output impedance in DCM

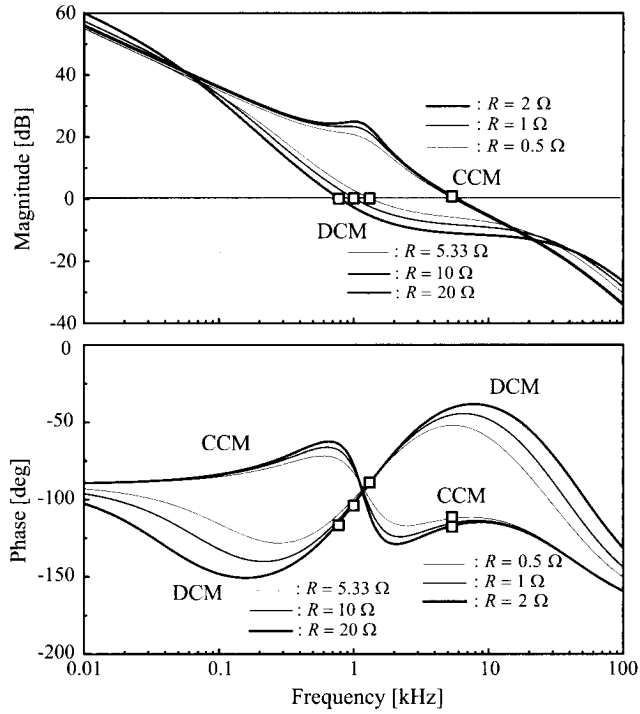


Figure 9.14 Loop gain characteristics of buck converter.

would deteriorate the step load response. The larger $|Z_o|_{peak}$ increases the transitional deviation of the output voltage, while the lower ω_{pz} slows down the transient response. Figure 9.16 compares the output voltage of the converter in response to step load changes in CCM and DCM operations. For CCM operation, step changes of $R = 0.8\ \Omega \Rightarrow 1\ \Omega \Rightarrow 0.8\ \Omega$ are introduced, yielding $\Delta I_{step} = 1$ A. On the other hand, step changes of $R = 5.3\ \Omega \Rightarrow 20\ \Omega \Rightarrow 5.3\ \Omega$ are exercised in DCM operation, thus producing $\Delta I_{step} = 0.55$ A. As predicted from the output impedance characteristics, the DCM operation shows a sluggish response with larger overshoot and undershoot.

The performance change over the transitions between CCM and DCM operations is related with not only the power stage dynamics but also the control scheme of the converter. The performance degradation in DCM operations is an innate limitation of voltage mode control. For voltage mode control, the fluctuation of the power stage dynamics over the CCM/DCM boundary directly propagates into the closed-loop performance. Although the converter would remain stable, other closed-loop performance will be degraded in DCM operations.

As introduced in Section 8.4.7, there exists an alternative control scheme for PWM converters — current model control, which employs an additional feedback from the

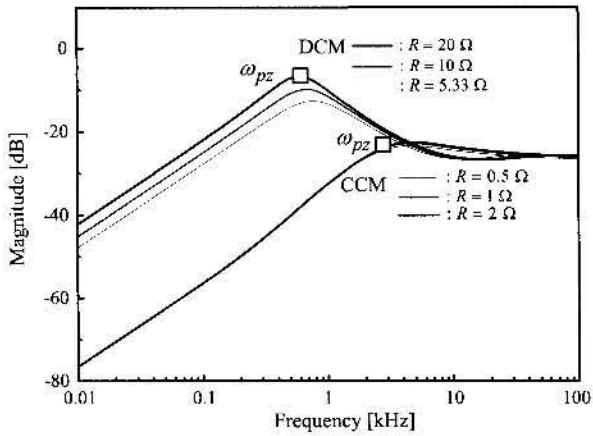


Figure 9.15 Output impedance characteristics of buck converter.

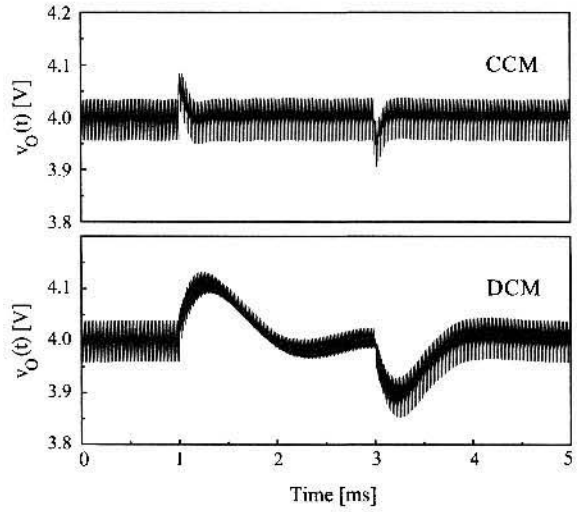


Figure 9.16 Step load responses of buck converter.

inductor current. It will be shown in the next chapter that current mode control effectively alleviates the sensitivity of the converter dynamics and could offer near uniform loop gain characteristics for both CCM and DCM operations.

9.1.3 Modeling of Isolated PWM Converters

Dynamic models for the three basic non-isolated PWM converters were derived using the concept of the PWM switch. The modeling procedures for these converters

are straightforward because each converter contains the PWM switch in its original structure. This section presents the extension of the modeling procedures to isolated dc-to-dc converters.

The isolated PWM converters contain a number of active and passive switches, separated by an isolation transformer. Thus, the PWM switch structure is not obvious in isolated converters. However, the operation of isolated converters reveals that the active and passive switches, even though located in distance with isolation, collectively execute the function of the PWM switch. Accordingly, the PWM switch can still be used as an effective tool in developing the dynamic models for isolated converters.

As demonstrated in Chapter 4, each isolated converter has a forerunning non-isolated converter from which that isolated converter is evolved. The modeling of an isolated converter is facilitated by using the existing model of the forerunning non-isolated converter. For example, the models of buck-derived dc-to-dc converters can readily be derived from the model of the buck converter. Similarly, the flyback converter can be conveniently modeled using the model of the buck/boost converter.

Modeling of Forward Converter and Other Bridge-Type Converters

The modeling of buck-derived isolated converters is illustrated using the forward converter. Figure 9.17 shows the modeling of the tertiary-winding reset forward converter. The original circuit of the forward converter in Fig. 9.17(a) is modified to the functional model in Fig. 9.17(b) by recognizing the following two facts.

1) The reset circuit, only employed to reset the magnetizing inductance of the isolation transformer, does not interfere with the converter dynamics. Thus, the reset circuit, along with the magnetizing inductance itself, can be removed for the purpose of modeling.

2) As far as the power stage operation is concerned, the forward converter is a functional equivalent of the buck converter combined with an isolation transformer upstream. The turns ratio of the isolation transformer is $1 : n$ with $n = N_S/N_P$.

The average model of the forward converter is constructed as shown in Fig. 9.17(c) by replacing the PWM switch with its average model. The two ideal transformers in Fig. 9.17(c), the $1 : n$ isolation transformer and the $1 : d$ transformer in the PWM switch, are merged into a single $1 : nd$ transformer in the simplified average model of Fig. 9.17(d). A set of averaged equations are written from Fig. 9.17(d)

$$\begin{aligned} \bar{i}_a(t) &= n\,d\,\bar{i}_c(t) \\ \bar{v}_{cp}(t) &= n\,d\,\bar{v}_{ap}(t) \end{aligned} \tag{9.26}$$

By linearizing (9.26), the small-signal expressions are obtained

$$\begin{aligned} \hat{i}_a(t) &= n\left(I_c\hat{d}(t) + D\hat{i}_c(t)\right) \\ \hat{v}_{cp}(t) &= n\left(D\hat{v}_{ap}(t) + V_{ap}\hat{d}(t)\right) \end{aligned} \tag{9.27}$$

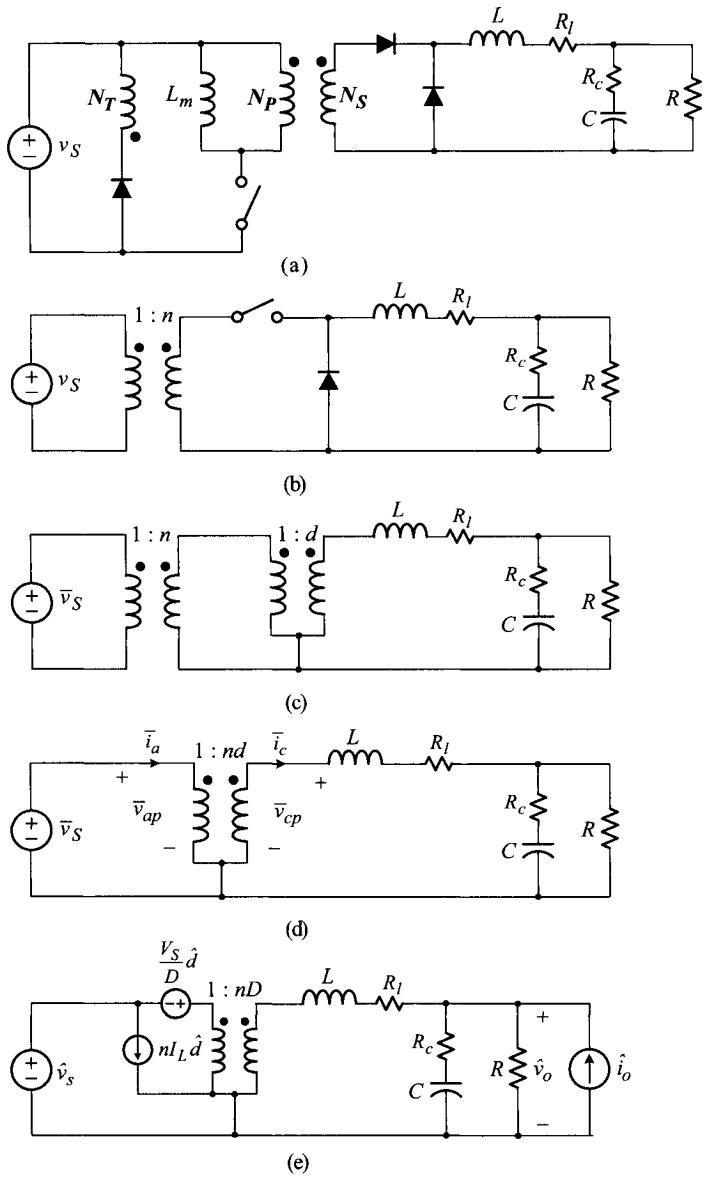


Figure 9.17 Modeling of tertiary-winding reset forward converter. (a) Original circuit. (b) Functional model. (c) Average model. (d) Simplified average model. (e) Small-signal model.

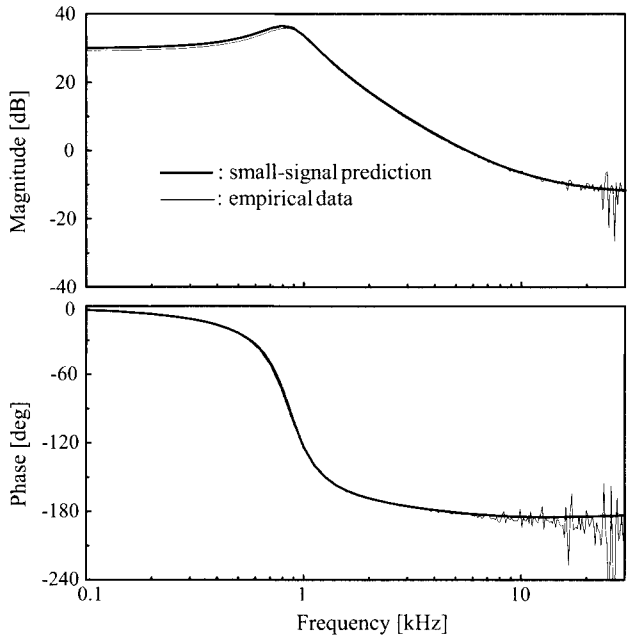


Figure 9.18 Prediction of small-signal model of forward converter.

With the incorporation of $I_c = I_L$ and $V_{ap} = V_S$, the final small-signal circuit model is shown in Fig. 9.17(e).

■ EXAMPLE 9.5 Small-Signal Model of Forward Converter

This example shows the prediction of the small-signal model of a tertiary-winding reset forward converter. The operational conditions and circuit parameters of the forward converter are $V_S = 64$ V, $L = 40$ μH, $R_l = 0.01$ Ω, $C = 400$ μF, $R_c = 0.02$ Ω, $R = 1$ Ω, $f_s = 50$ kHz, and $D = 0.25$. The turns ratio of the ideal three-winding transformer is $N_P : N_S : N_T = 36 : 18 : 36$ and the magnetizing inductance is $L_m = 200$ μH. The duty ratio-to-output transfer function is simulated using the small-signal model of Fig. 9.17(e). Figure 9.18 shows the prediction of the small-signal model, in comparison with the empirical result obtained from the original circuit of Fig. 9.17(a).

The small-signal model of Fig. 9.17(e) is also valid for other types of forward converters including the two-switch forward converter. Furthermore, the preceding procedures are also applicable to other buck-derived isolated converters. Figure 9.19(a) shows the full-bridge converter and its small-signal model, while Fig. 9.19(b) depicts those of the half-bridge converter. With these models, all the previous results

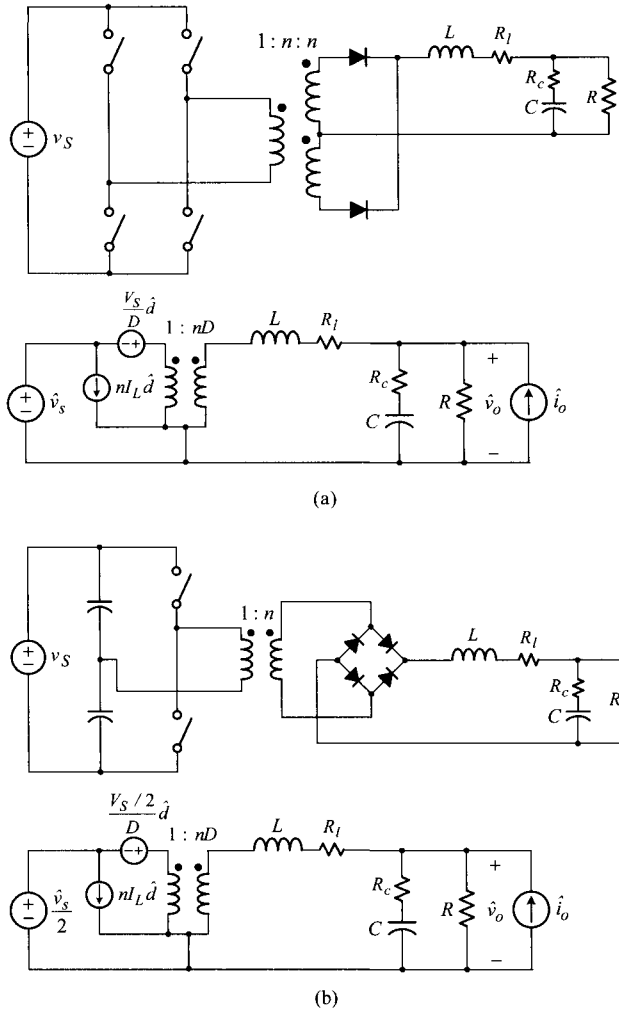


Figure 9.19 Modeling of bridge-type buck-derived converters. (a) Full-bridge converter. (b) Half-bridge converter.

of the modeling, analysis, and control, developed using the buck converter, are now extended to all buck-derived isolated converters.

Modeling of Flyback Converter

For the purpose of modeling, the flyback converter is successively modified as illustrated in Fig. 9.20. The original circuit of the flyback converter is shown in Fig. 9.20(a). Figure 9.20(a) is altered to Fig. 9.20(b), where the ideal transformer is removed by reflecting the magnetizing inductance and the voltage source into the

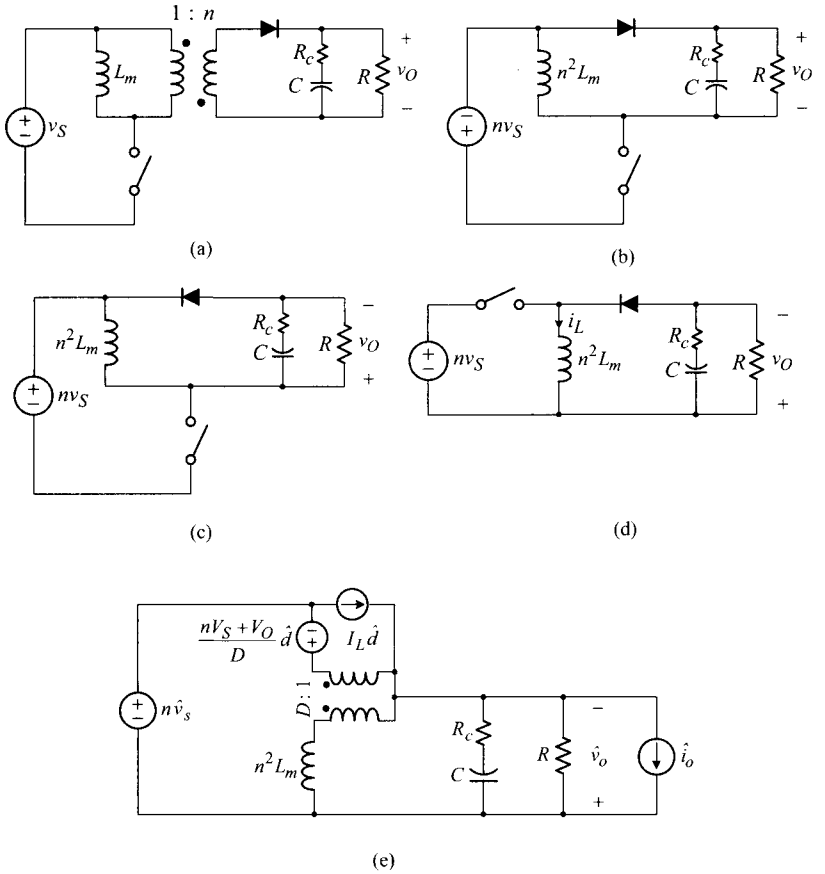


Figure 9.20 Modeling of flyback converter. (a) Original flyback converter. (b) Modified model. (c) Modified model. (d) Equivalent buck/boost converter. (e) Small-signal model.

secondary side. Figure 9.20(b) is modified to Fig. 9.20(c) by changing the polarity of the input and output voltages and reversing the direction of the diode. The power stage circuit is further modified into Fig. 9.20(d) by relocating the active switch without changing the circuit operation. Figure 9.20(d) is now recognized as a buck/boost converter whose input voltage and inductance are scaled by the turns ratio of the transformer. Finally, the small-signal model of the flyback converter is obtained as shown in Fig. 9.20(e) by adapting the small-signal model of the buck/boost converter.

■ EXAMPLE 9.6 Small-Signal Model of Flyback Converter

This example shows the prediction of the small-signal model of a flyback converter operating with $V_S = 180$ V, $L_m = 4.0$ mH, $C = 470\,\mu$F, $R_c = 0.03\,\Omega$,

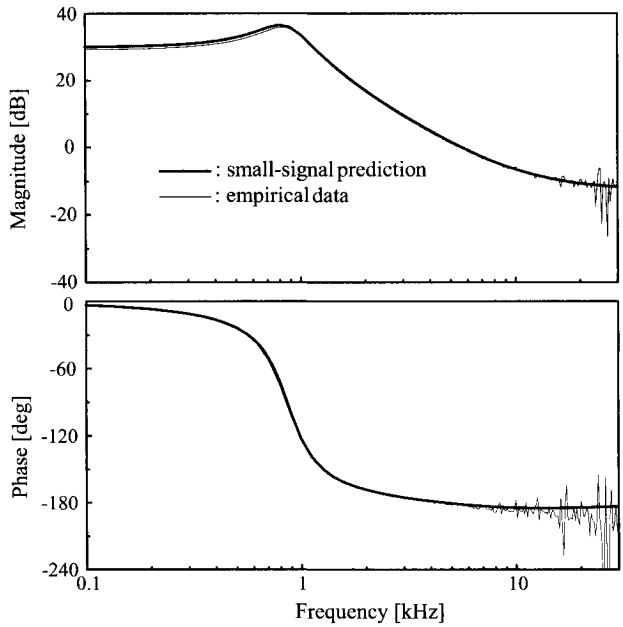


Figure 9.21 Prediction of small-signal model of flyback converter.

$R = 1\ \Omega$, $f_s = 50$ kHz, and $D = 0.25$. The turns ratio of the flyback transformer is 60 : 6. The duty ratio-to-output transfer function is simulated using the small-signal model in Fig. 9.20(e). Figure 9.21 compares the prediction of the small-signal model with the empirical result obtained from the circuit model of Fig. 9.20(a).

9.2 DESIGN AND ANALYSIS OF DC-TO-DC CONVERTERS WITH PRACTICAL SOURCE SYSTEM

In previous chapters, an ideal voltage source was assumed for dc-to-dc converters in order to simplify the control design and dynamic analysis. In reality, however, dc-to-dc converters are powered from a practical voltage source which presents a certain source impedance. The source impedance influences the dynamic performance of converters in various ways and thus should be considered in the dynamic analysis and control design.

Ideally, dc-to-dc converters should be designed for the actual source impedance. However, such a design is impracticable because the source impedance characteristics are usually unknown or even undefined at the design stage of the converter. One functional approach to resolving this problem is to design dc-to-dc converters for an ideal voltage source, while minimizing the chance of the performance change at

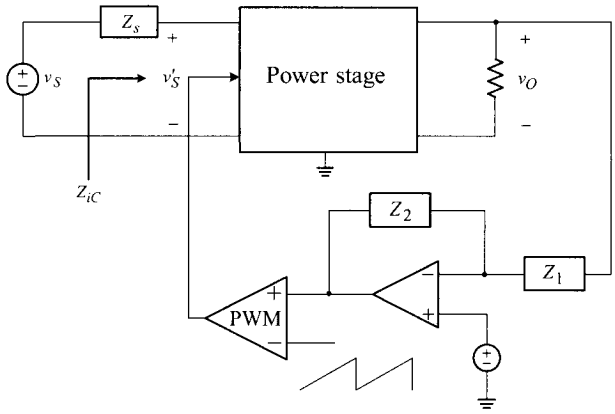


Figure 9.22 Dc-to-dc converter powered by non-ideal voltage source with finite source impedance.

the presence of an actual source impedance. This design is very preferable in that the preceding design methodology for an ideal voltage source can be adapted to real applications with minimal or no modification.

To implement the aforementioned design approach, it is imperative to investigate the impacts of the source impedance on the converter performance. Once this knowledge is acquired, the control design can be carried out in such a way that is least susceptible to the potential performance change at the presence of a certain source impedance. The converter performance with the actual source system can later be assessed by incorporating the source impedance characteristics whenever they become available. The dc-to-dc converter, designed as outlined above, would retain stability and undergo minimal performance change from the initial predictions made using the ideal voltage source.

With this background, we start discussions about the impacts of the source impedance on the converter performance. Figure 9.22 shows the dc-to-dc converter powered by a voltage source with a finite source impedance Z_s. The source impedance influences the closed-loop performance of the converter, including the audio-susceptibility, loop gain, output impedance, and most significantly stability. This section first analyzes the impact of the source impedance and later proposes a design strategy which would offer stability and minimal performance change at the presence of the source impedance.

9.2.1 Audio-Susceptibility Analysis

Referring to Fig. 9.22, the closed-loop input-to-output transfer function, or audio-susceptibility, of the converter with the source impedance $Z_s(s)$ is expressed as

$$A_u(s) = \frac{\hat{v}_o(s)}{\hat{v}_s(s)} = \frac{\hat{v}'_s(s)}{\hat{v}_s(s)} \frac{\hat{v}_o(s)}{\hat{v}'_s(s)}$$

$$= \frac{Z_{iC}(s)}{Z_{iC}(s) + Z_s(s)} A_{uC}(s) = \frac{1}{1 + \dfrac{Z_s(s)}{Z_{iC}(s)}} A_{uC}(s) \tag{9.28}$$

where $Z_{iC}(s)$ is the input impedance of the converter and $A_{uC}(s) = \hat{v}_o(s)/\hat{v}'_s(s)$ is the audio-susceptibility of the converter with *zero* source impedance, namely, with an ideal voltage source. Details about the input impedance of a closed-loop controlled dc-to-dc converter will be given in Section 9.2.3. It is obvious that the audio-susceptibility is practically unaffected by the source impedance if the condition $|Z_{iC}| \gg |Z_s|$ prevails for all frequencies.

For general cases, the audio-susceptibility expression is approximated to

$$A_u(s) = \frac{1}{1 + \dfrac{Z_s(s)}{Z_{iC}(s)}} A_{uC}(s) \approx \begin{cases} \dfrac{A_{uC}}{\dfrac{Z_s}{Z_{iC}}} & \text{at frequencies where } |Z_{iC}| \ll |Z_s| \\ A_{uC} & \text{at frequencies where } |Z_{iC}| \gg |Z_s| \end{cases} \tag{9.29}$$

Now, the impact of the source impedance is analyzed using this relationship.

■ EXAMPLE 9.7 Audio-Susceptibility with Source Impedance

This example demonstrates the impact of the source impedance on the audio-susceptibility of a closed-loop controlled buck converter. Figure 9.23 shows a buck converter powered by a practical source system. The operational conditions of the buck converter are $V_S = 16$ V, $L = 40\,\mu$H, $R_l = 0.1\,\Omega$, $C = 470\,\mu$F,

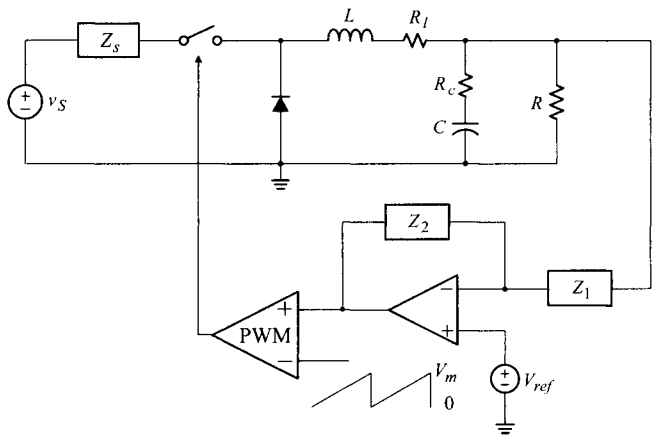


Figure 9.23 Buck converter with source impedance.

$R_c = 0.05\ \Omega$, $R = 1\ \Omega$, $V_{ref} = 4$ V, $f_s = 50$ kHz, and $V_m = 3.8$ V. The voltage feedback compensation is given by

$$F_v(s) = \frac{Z_2(s)}{Z_1(s)} = \frac{500}{s}\frac{\left(1 + \frac{s}{5.83 \times 10^3}\right)\left(1 + \frac{s}{1.09 \times 10^4}\right)}{\left(1 + \frac{s}{4.25 \times 10^4}\right)\left(1 + \frac{s}{2.51 \times 10^5}\right)}$$

The source impedance is expressed as

$$Z_s(s) = 0.1\frac{\left(1 + \frac{s}{500}\right)\left(1 + \frac{s}{1.25 \times 10^5}\right)}{1 + \frac{s}{62500} + \frac{s^2}{(7.9 \times 10^3)^2}}$$

Figure 9.24(a) shows the audio-susceptibility of the converter with the source impedance, $A_u(s)$, in comparison with the audio-susceptibility with the zero source impedance, $A_{uC}(s)$. The source impedance $Z_s(s)$ and input impedance $Z_{iC}(s)$ of the buck converter are shown in Fig. 9.24(b). As predicted from (9.29), the audio-susceptibility is only modified in the frequencies where $|Z_{iC}| \ll |Z_s|$. In fact, the overlap between $|Z_s|$ and $|Z_{iC}|$ is projected as an additional attenuation owing to the source impedance.

9.2.2 Stability Analysis

The source impedance exerts a direct influence on stability of the converter. More precisely, the source impedance could destablize the converter that was stable with the zero source impedance. This section discusses the origin of the stability problem and a later section provides design guidelines to avoid such a problem.

Source-Impedance Induced Instability

For the stability analysis, the previous audio-susceptibility expression with a source impedance is repeated

$$A_u(s) = \frac{v_o(s)}{v_s(s)} = \frac{1}{1 + \frac{Z_s(s)}{Z_{iC}(s)}} A_{uC}(s) \tag{9.30}$$

where $A_{uC}(s)$ is the audio-susceptibility with the zero source impedance. By denoting $A_{uC}(s)$ as

$$A_{uC}(s) = \frac{\mathcal{N}(s)}{\mathcal{D}(s)} \tag{9.31}$$

the audio-susceptibility is expressed as

$$A_u(s) = \frac{1}{1 + \frac{Z_s(s)}{Z_{iC}(s)}} \frac{\mathcal{N}(s)}{\mathcal{D}(s)} \tag{9.32}$$

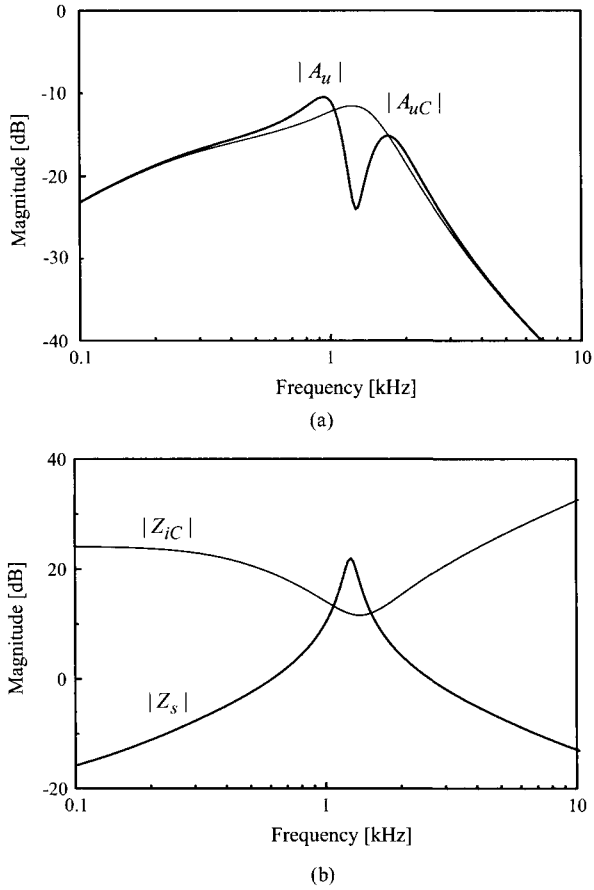


Figure 9.24 Audio-susceptibility of buck converter. (a) Audio-susceptibility. (b) Source impedance and input impedance of converter.

The characteristic equation of the system is then given by

$$\left(1 + \frac{Z_s(s)}{Z_{iC}(s)}\right) D(s) = 0 \tag{9.33}$$

When the converter is stable with the zero source impedance, the equation $\mathcal{D}(s) = 0$ does not contain any right-half plane (RHP) roots. Accordingly, stability is assessed by investigating the existence of any RHP root in the equation $1 + Z_s(s)/Z_{iC}(s) = 0$, that is, by applying the Nyquist criterion to $Z_s(s)/Z_{iC}(s)$. Illustrations of such analyses are given in Fig. 9.25. Figure 9.25(a) shows Bode plot of $|Z_{iC}|$ along with three different cases of $|Z_s|$. Figure 9.25(b) depicts the polar plots of the impedance ratio Z_s/Z_{iC} for the corresponding three cases.

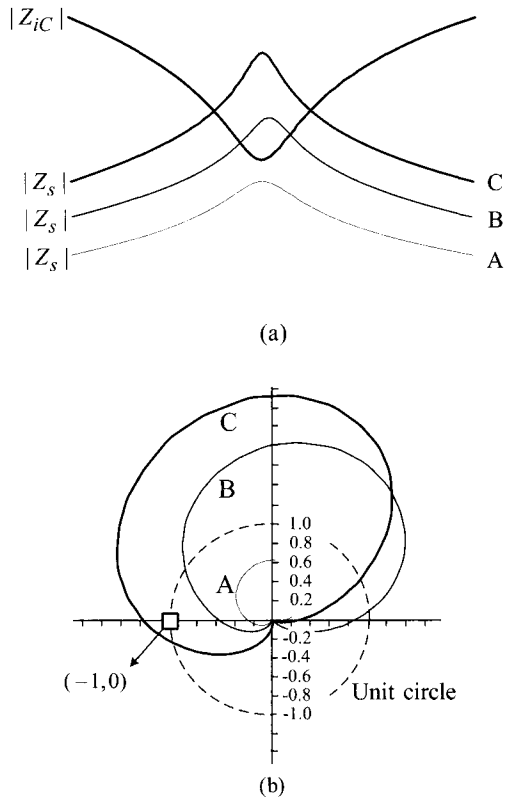


Figure 9.25 Bode plot and polar plot of Z_s and Z_{iC}. (a) Bode plot of Z_s and Z_{iC}. (b) Polar plot of Z_s/Z_{iC}.

1) Case A: The impedances satisfy the condition $|Z_{iC}| > |Z_s|$ for all frequencies. This condition is equivalent to $|Z_s/Z_{iC}| < 1$ for all frequencies. For this case, the polar plot of Z_s/Z_{iC} stays inside the unit circle, thereby excluding the possibility of encircling the $(-1, 0)$ point. The Nyquist criterion is automatically satisfied and the converter remains stable.

2) Case B: $|Z_s|$ exceeds $|Z_{iC}|$ in some frequencies. The polar plot partially departs from the unit circle. However, the polar plot *does not* encircle the $(-1, 0)$ point and the converter thus remains stable even though the condition $|Z_{iC}| > |Z_s|$ is not met at some frequencies.

3) Case C: The condition $|Z_{iC}| > |Z_s|$ is infringed more widely so that the polar plot *does* encircle the $(-1, 0)$ point, thereby violating the Nyquist stability criterion. The converter now becomes unstable due to the presence of the source impedance. The instability illustrated here is referred to as the *source-impedance induced instability.*

The sufficient condition for stability is $|Z_{iC}| > |Z_s|$ for all frequencies, as illustrated with Case A in the previous analysis. If the impedances do not meet the sufficient condition, thereby showing an impedance overlap, the Nyquist criterion may be applied to the polar plot of Z_s/Z_{iC} to assess stability. It is emphasized that the impedance overlap *does not* necessarily imply instability but *does* signal the necessity of the Nyquist analysis.

Input Filter and Source Impedance

Dc-to-dc converters usually employ a filter stage between the voltage source and power stage for the following reason. For most dc-to-dc converters, the input current to the power stage is a discontinuous pulsating current. If directly drawn from the voltage source, the pulsating input current forces the voltage source to deliver substantial harmonic current components. The harmonic current components in turn produce excessive conducted electromagnetic interference (EMI), thereby failing to meet regulatory EMI standards. To avoid such a situation, an input filter stage is usually employed between the voltage source and power stage so that the voltage source only delivers a smoothly-filtered continuous current waveform.

The input filter stage always has a finite output impedance. The converter power stage sees the output impedance of the input filter as the source impedance. Accordingly, dc-to-dc converters are naturally exposed to a substantial source impedance which could affect stability and performance of the converter.

■ EXAMPLE 9.8 Buck Converter with Input Filter

This example illustrates the operation of a buck converter with an input filter. Figure 9.26(a) shows a closed-loop controlled buck converter with an input filter. The operational conditions and power stage parameters are the same as those of Example 9.7. The input filter parameters are $L_f = 8\,\mu$H, $R_{lf} = 0.01\,\Omega$, $C_f = 320\,\mu$F, and $R_d = 0.05\,\Omega$. Figure 9.26(b) illustrates the waveforms of the input current to the power stage, i_Q, the voltage source current i_S, and the input filter branch current i_F. The voltage source mainly supports the dc component of the input current, while the parallel branch of the input filter carries the ac component. The current filtering effect is clearly seen. Figure 9.27 shows the source impedance Z_s and the input impedance Z_{iC} of the converter. The wide separation between impedances automatically meets the sufficient condition for stability.

Stability Analysis with Input Filter

The previous example showed the case in which the source impedance and input impedance are widely separated, thus precluding any chance of the stability problem. However, there are other cases where the source impedance does destablize a previously stable converter. In fact, this *source-impedance induced instability* is a

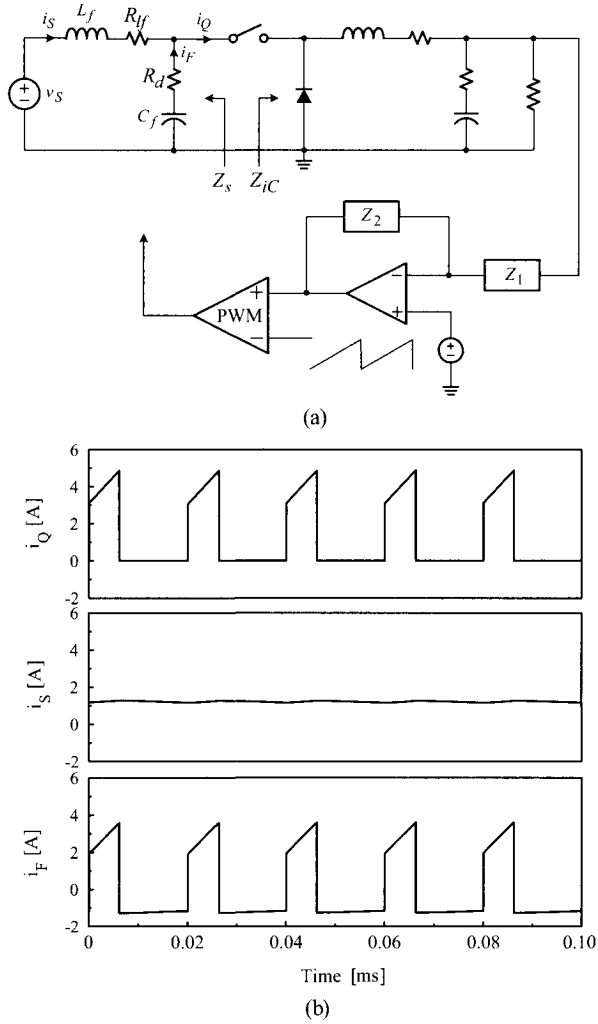


Figure 9.26 Buck converter with input filter. (a) Circuit diagram. (b) Current waveforms.

well-known problem of the input filter design, which has been researched in many papers [2–4]. This section illustrates an example of the source-impedance induced instability.

■ EXAMPLE 9.9 Stability of Buck Converter with Input Filter

The stability analysis of a buck converter with an input filter is illustrated in this example. The buck converter used in Examples 9.7 and 9.8 is revisited

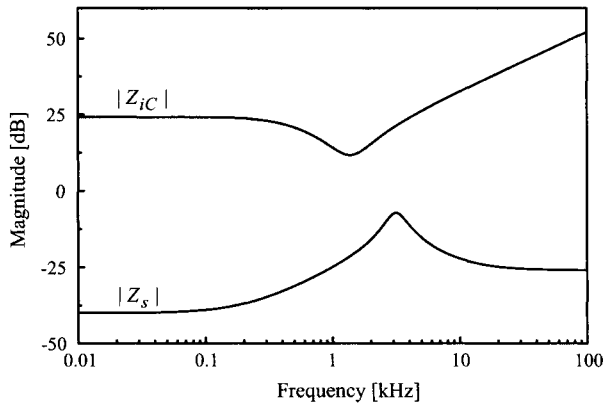


Figure 9.27 Converter input impedance and source impedance.

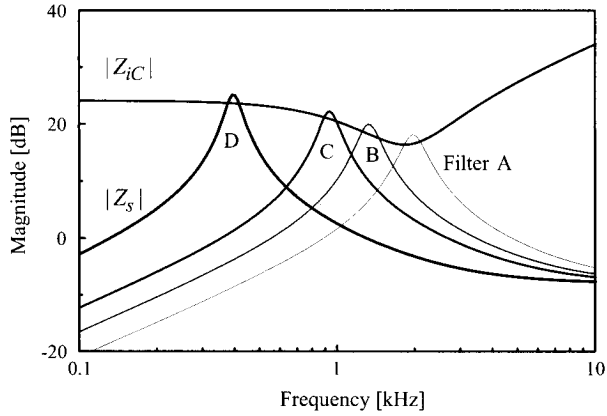
with a minor modification in the voltage feedback compensation

$$F_v(s) = \frac{2000}{s} \frac{\left(1 + \frac{s}{5.83 \times 10^3}\right)\left(1 + \frac{s}{1.09 \times 10^4}\right)}{\left(1 + \frac{s}{4.25 \times 10^4}\right)\left(1 + \frac{s}{2.51 \times 10^5}\right)}$$

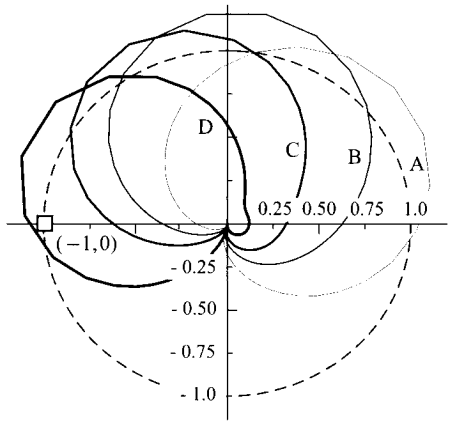
Figure 9.28(a) shows $|Z_{iC}|$ of the buck converter and $|Z_s|$ of the four different input filters, referred to as Filter A, B, C, and D

- Filter A: $L_f = 145\ \mu$H, $R_{lf} = 0.01\ \Omega$, $C_f = 45\ \mu$F, and $R_d = 0.4\ \Omega$
- Filter B: $L_f = 240\ \mu$H, $R_{lf} = 0.01\ \Omega$, $C_f = 60\ \mu$F, and $R_d = 0.4\ \Omega$
- Filter C: $L_f = 390\ \mu$H, $R_{lf} = 0.01\ \Omega$, $C_f = 75\ \mu$F, and $R_d = 0.4\ \Omega$
- Filter D: $L_f = 1100\ \mu$H, $R_{lf} = 0.01\ \Omega$, $C_f = 150\ \mu$F, and $R_d = 0.4\ \Omega$

All the four cases exhibit an impedance overlap and thus require the Nyquist stability analysis. Figure 9.28(b) shows the polar plots of Z_s/Z_{iC} with the four different input filters. As the region of the impedance overlap shifts from high frequencies to lower frequencies, from Filter A to Filter D, the circular-shaped polar plot rolls in the counter-clockwise direction until it encircles the $(-1, 0)$ point. The qualitative explanation about the behavior of the polar plot will be given in the next section. With Filter D, the polar plot encircles the $(-1, 0)$ point, indicating that the converter is unstable. Figure 9.29 displays the loop gain of the buck converter with the four different input filters, in parallel with the loop gain without any input filter. The loop gain with Filter C shows that the converter is barely stable with a small phase margin. With Filter D, the loop gain predicts instability with a negative phase margin.



(a)



(b)

Figure 9.28 Stability analysis of buck converter with input filter. (a) Bode plots of $Z_s(s)$ and $Z_{iC}(s)$. (b) Polar plots of $Z_s(s)/Z_{iC}(s)$.

Figure 9.30 exhibits the inductor current of the buck converter in response to the load changes of $R = 1\ \Omega \Rightarrow 1.5\ \Omega \Rightarrow 1\ \Omega$. The inductor current is displayed with the four different input filters, along with the case without any input filter. The inductor current becomes gradually oscillatory until it exhibits full instability with Filter D.

In order to investigate the cause of the source-impedance induced instability, it is first necessary to understand the input impedance characteristics of a closed-loop controlled dc-to-dc converter. The analysis of the input impedance is given in the next section. The origin of the instability and design strategy for unknown source

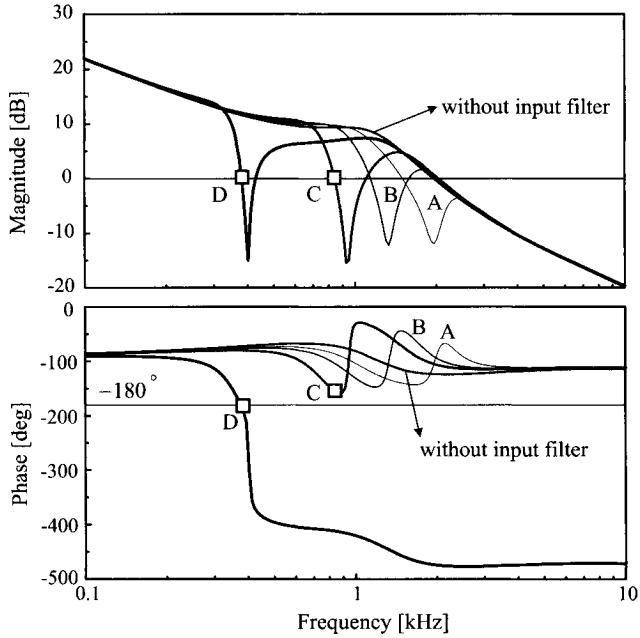


Figure 9.29 Loop gain of buck converter with different input filters.

impedance characteristics are discussed in Sections 9.2.4 and 9.2.5. It will be shown that the previous control design guidelines, developed in Section 8.4.2 for an ideal voltage source, are in fact the design strategy that minimizes the risk of the source-impedance induced instability.

9.2.3 Input Impedance of Regulated Dc-to-Dc Converter

The input impedance of a closed-loop controlled dc-to-dc converter, or *a regulated dc-to-dc converter*, exhibits a very distinctive property. At low frequencies, the input impedance Z_{iC} of a regulated converter is a *negative resistance*. When combined with a certain source impedance Z_s, the negative resistance causes the polar plot of Z_s/Z_{iC} to break the Nyquist stability criterion, as demonstrated in Example 9.9.

The negative resistance is attributed to the fact that a regulated dc-to-dc converter functions as a constant power load. Referring to Fig. 9.31(a), a regulated dc-to-dc converter adjusts the duty ratio to maintain the output voltage constant, $v_O = V_O$, for a given load resistance R, even if the input voltage v_S changes. In other words, a regulated converter is a constant power load that always draws a predetermined power, $P = V_O^2/R$. If the dc-to-dc converter operates losslessly with a 100% efficiency, it follows that

$$P = \frac{V_O^2}{R} = V_O I_O = v_S i_S \tag{9.34}$$

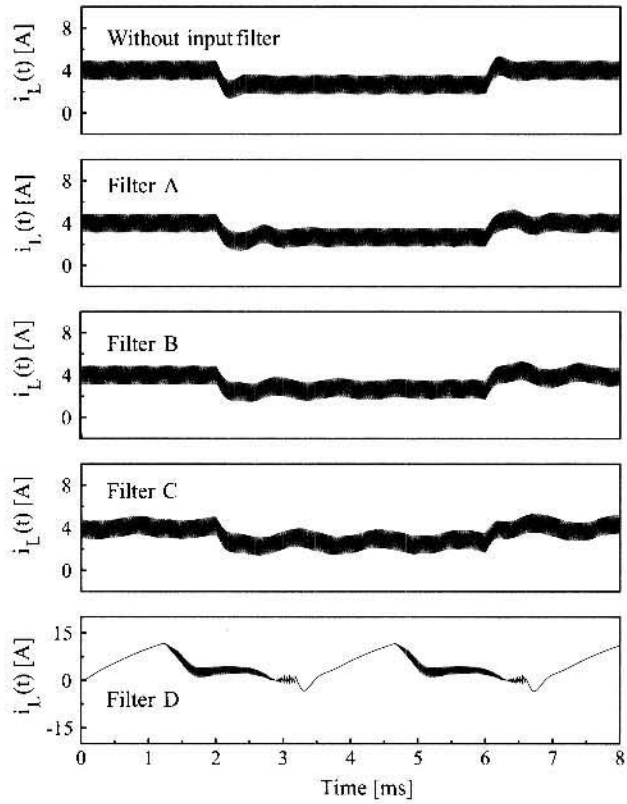


Figure 9.30 Step load response of buck converter.

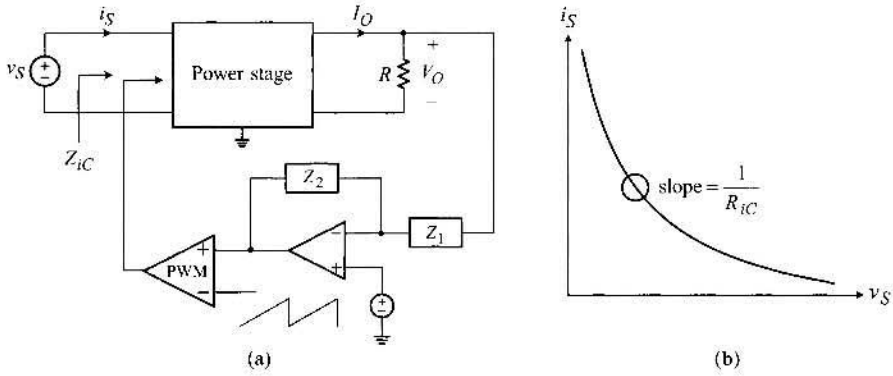


Figure 9.31 Negative input resistance of closed-loop controlled dc-to-dc converter. (a) Block diagram. (b) $v_S - i_S$ curve.

which indicates that

$$\frac{V_O}{v_S} = \frac{i_S}{I_O} = M \tag{9.35}$$

where M denotes the forward voltage gain or reverse current gain. The input resistance of the converter is evaluated as

$$R_{iC} = \frac{\mathrm{d}v_S}{\mathrm{d}i_S} = \frac{\mathrm{d}}{\mathrm{d}i_S}\left(\frac{P}{i_S}\right) = -\frac{P}{i_S^2} = -\frac{v_S}{i_S} = -\frac{1}{M^2}\frac{V_O}{I_O} = -\frac{1}{M^2}R \tag{9.36}$$

where the facts $P = v_S i_S$, $v_S = V_O/M$, $i_S = MI_O$, and $R = V_O/I_O$ are successively used. Equation (9.36) indicates that the input resistance R_{iC} is a negative resistance of $-R/M^2$.

The negative input resistance is also illustrated in Fig. 9.31(b) which depicts the $v_S - i_S$ curve of the regulated converter. Because the product of v_S and i_S is a predetermined constant, the slope of $v_S - i_S$ curve is negative, as shown in Fig. 9.31(b). For example, if v_S increases, i_S must decrease since the input power $P = v_S i_S$ always remains constant. The regulated dc-to-dc converter thus exhibits a negative incremental resistance, R_{iC} given in (9.36).

Detailed analyses [2, 4, 5] showed that the input impedance of a regulated converter is a negative resistance only at low frequencies, typically below the 0 dB crossover frequency of the converter loop gain. At high frequencies where the reactance of the power stage inductor becomes very large, the input impedance increases with a +20 dB/dec slope, thus showing inductive characteristics.

The input impedance characteristics of a regulated converter are mainly determined by the location of the 0 dB crossover frequency of the loop gain. Figure 9.32 shows typical structures of the input impedance of dc-to-dc converters. The general shape of the input impedance can be classified into three cases, as illustrated in Fig. 9.32, depending on the location of the loop gain crossover frequency, ω_c.

1) Case A with $\omega_c > Q\omega_o$, where ω_c is the loop gain crossover frequency, ω_o is the pole frequency, and Q is the damping ratio of the power stage double pole: The input impedance follows the negative resistance, $R_{iC} = -R/M^2$, up to the crossover frequency and increases with a +20 dB/dec slope thereafter. For this case, the minimum magnitude of the input impedance $|Z_{iC}|_{min}$ is limited to $20\log R_{iC}$.

2) Case B or B′ with $\omega_o < \omega_c < Q\omega_o$: The input impedance shows a dipping of $20\log(Q\omega_o/\omega_c)$ at the loop gain crossover frequency ω_c. The minimum magnitude of the input impedance, $|Z_{iC}|_{min} = 20\log R_{iC} - 20\log(Q\omega_o/\omega_c)$, occurs at the loop gain crossover frequency ω_c.

3) Case C with $\omega_c < \omega_o$: The input impedance produces the maximum dipping of $20\log Q$. This can be considered the worst input impedance characteristics. For this case, the minimum magnitude of the input impedance, $|Z_{iC}|_{min} = 20\log R_{iC} - 20\log Q$, occurs at the power stage pole frequency ω_o.

The expressions for the input impedance parameters in Fig. 9.32 are summarized in Table 9.2 for the three basic converters.

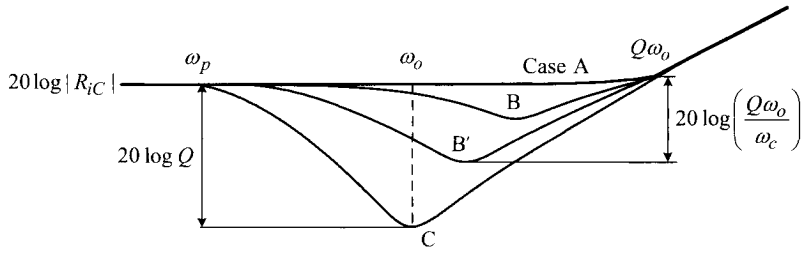


Figure 9.32 Input impedances of dc-to-dc converter with different loop gain crossover frequencies.

Table 9.2 Parameters for Converter Input Impedance Structure in Fig. 9.32

	Buck converter	Boost converter	Buck/boost converter
$\lvert R_{iC}\rvert$	$\frac{R}{D^2}$	$(1-D)^2R$	$\frac{(1-D)^2}{D^2}R$
ω_o	$\frac{1}{\sqrt{LC}}$	$\frac{1-D}{\sqrt{LC}}$	$\frac{1-D}{\sqrt{LC}}$
Q	$R\sqrt{\frac{C}{L}}$	$(1-D)R\sqrt{\frac{C}{L}}$	$(1-D)R\sqrt{\frac{C}{L}}$
ω_p	$\frac{1}{CR}$	$\frac{1}{CR}$	$\frac{1}{CR}$

■ EXAMPLE 9.10 Input Impedance of Buck Converter

This example shows the effect of the loop gain crossover frequency on the input impedance of the buck converter used in Examples 9.7 through 9.9. Figure 9.33 shows the loop gain and input impedance of the buck converter with four different voltage feedback compensation designs. The corner frequencies of the voltage feedback compensation are the same and only the integrator gain is varied to result in four different crossover frequencies. From the operational conditions and power stage parameters of the buck converter, the input impedance parameters shown in Table 9.2 are determined as

$$20\log R_{iC} = 20\log\left(\frac{R}{D^2}\right) = 20\log\left(\frac{1}{0.25^2}\right) = 24\ \text{dB}$$

$$\omega_o = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{40\times10^{-6}\cdot 470\times10^{-6}}} = 2\pi\cdot 1.16\times10^3\ \text{rad/s}$$

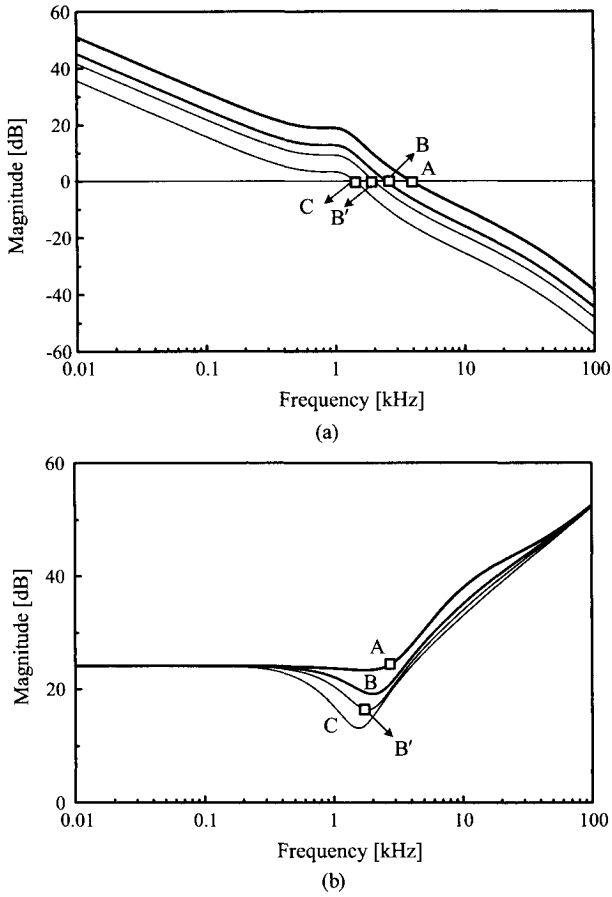


Figure 9.33 Loop gain and input impedance. (a) Loop gain. (b) Input impedance.

$$Q = R\sqrt{\frac{C}{L}} = 1\sqrt{\frac{470 \times 10^{-6}}{40 \times 10^{-6}}} = 3.43$$

$$\omega_p = \frac{1}{CR} = \frac{1}{470 \times 10^{-6}1} = 2\pi \cdot 388 \text{ rad/s}$$

The actual input impedances match well with the analytical predictions. For Case A with $\omega_c \approx \omega_o Q = 2\pi \cdot 1.16 \times 10^3 \cdot 3.43 = 2\pi \cdot 4 \times 10^3$ rad/s, the minimum value of the input impedance is indeed raised to the theoretical limit of $|Z_{iC}|_{min} = 20\log(R/D^2) = 24$ dB. For Case B′ with $\omega_c = 2\pi \cdot 2 \times 10^3$, the input impedance exhibits the minimum value of 16.3 dB, which is close to the theoretical prediction of $|Z_{iC}|_{min} = 20\log(R/D^2) - 20\log(Q\omega_o/\omega_c) = 18$ dB.

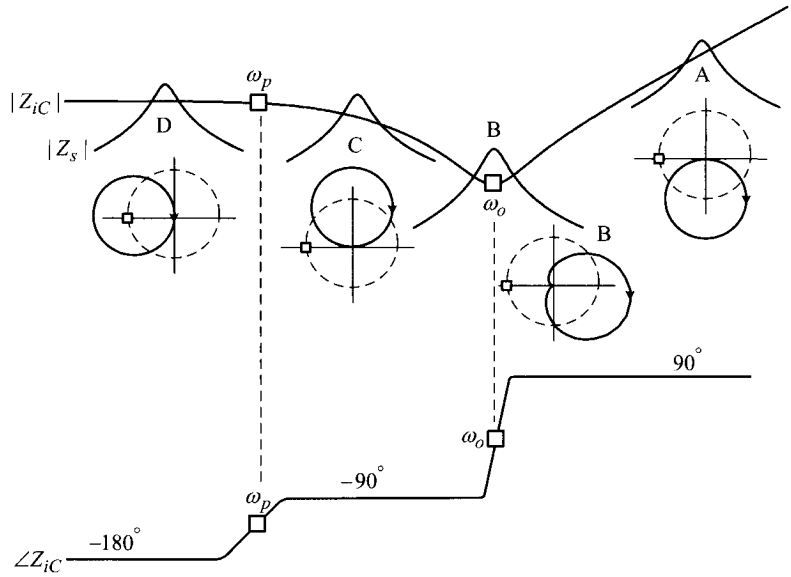


Figure 9.34 Impedance overlap and polar plot of Z_s/Z_{iC}.

9.2.4 Origin of Source-Impedance Induced Instability

A regulated converter becomes unstable when the impedance ratio Z_s/Z_{iC} breaks the Nyquist stability criterion. More precisely, the source impedance Z_s destabilizes a previously stable converter when the polar plot of Z_s/Z_{iC} encircles the $(-1, 0)$ point. The encirclement cannot happen if the condition $|Z_{iC}| > |Z_s|$ is satisfied for all frequencies because the polar plot of Z_s/Z_{iC} never stretches from the unit circle. On the other hand, when the condition $|Z_{iC}| > |Z_s|$ is violated at certain frequencies thereby showing an impedance overlap, the polar plot departs from the unit circle and is exposed to the risk of encircling the $(-1, 0)$ point. For this case, the phase characteristics of Z_s and Z_{iC} determine the encirclement of the $(-1, 0)$ point.

Figure 9.34 illustrates the stability analysis of a regulated converter when combined with four different cases of the source impedance. The input impedance of the converter belongs to Case C in Fig. 9.32 where the loop gain crossover frequency ω_c falls below the power stage double pole, $\omega_c < \omega_o$. The input impedance starts from a negative resistance. The input impedance has a pole at ω_p and a double zero at ω_o. Detailed analyses [2, 4] showed that the ω_p is a right-half plane (RHP) pole which boosts the phase by 90°. Thus, the phase of the input impedance, $\angle Z_{iC}$, starts from $-180°$, increases to $-90°$ over ω_p, and finally settles to 90° after ω_o.

The four different cases of $|Z_s|$ are shown in Fig. 9.34, each overlapping $|Z_{iC}|$ in the different frequency region. From the shape of $|Z_s|$, it is evident that $\angle Z_s$ changes from $+90°$ to $-90°$ over the overlap. To judge the encirclement of the $(-1, 0)$ point,

the boundaries of $\angle(Z_s/Z_{iC}) = \angle Z_s - \angle Z_{iC}$ are evaluated for the four different cases. From the $\angle Z_s$ and $\angle Z_{iC}$ characteristics, it can be inferred that

- Case A: $90° - 90° < \angle Z_s/Z_{iC} < -90° - 90°$
  $\Rightarrow 0° < \angle Z_s/Z_{iC} < -180°$
- Case B: $90° - (-90°) < \angle Z_s/Z_{iC} < -90° - 90°$
  $\Rightarrow 180° < \angle Z_s/Z_{iC} < -180°$
- Case C: $90° - (-90°) < \angle Z_s/Z_{iC} < -90° - (-90°)$
  $\Rightarrow 180° < \angle Z_s/Z_{iC} < 0°$
- Case D: $90° - (-180°) < \angle Z_s/Z_{iC} < -90° - (-180°)$
  $\Rightarrow 270° < \angle Z_s/Z_{iC} < 90°$

Figure 9.34 also shows the conceptual polar plot of Z_s/Z_{iC} based on the previous analysis. As the frequency of the impedance overlap shifts from high frequencies to low frequencies, the circular-shaped polar plot turns in the counter-clockwise direction, thus successively elevating the risk of encircling the $(-1, 0)$ point. When the overlap occurs at sufficiently low frequencies where $\angle Z_{iC} \approx -180°$, the polar plot encircles the $(-1, 0)$ point and the converter now becomes unstable.

This source-impedance induced instability is a direct consequence of the unique characteristics of the input impedance of a regulated converter, which behaves as a negative resistance at low frequencies. If the source impedance is coupled with a regular positive resistance, the system never becomes unstable, regardless of the magnitude of the source impedance or the extent of the impedance overlap. It should be noted that the analysis shown in Fig. 9.34 is consistent with the outcome of Example 9.9.

9.2.5 Control Design with Source Impedance

The design strategy to minimize the danger of instability at the presence of a certain source impedance is to increase the 0 dB crossover frequency of the loop gain. When the 0 dB crossover frequency occurs at higher frequencies than $Q\omega_o$, namely, Case A in Fig. 9.32, the minimum value of the input impedance is raised to the theoretical limit of $|Z_{iC}|_{min} = 20\log(R/M^2)$. For this case, the converter remains stable if the condition $|Z_s|_{peak} < 20\log(R/M^2)$ is satisfied. This situation is illustrated in Fig. 9.35.

The design object of placing the 0 dB *crossover frequency at higher frequencies is in fact the goal of the control design for an ideal voltage source.* Accordingly, the previous design guideline for ideal voltage sources is actually a very desirable strategy even with the existence of an unknown source impedance. Once the control is designed for a higher crossover frequency than $Q\omega_o$, the converter remains stable as long as the condition $|Z_s|_{peak} < 20\log(R/M^2)$ is met.

The source impedance Z_s can be controlled by the input filter design. The input filter should be designed for the minimum $|Z_s|_{peak}$ while meeting EMI specifications and other constraints. Design techniques for the input filter are given in [2, 6].

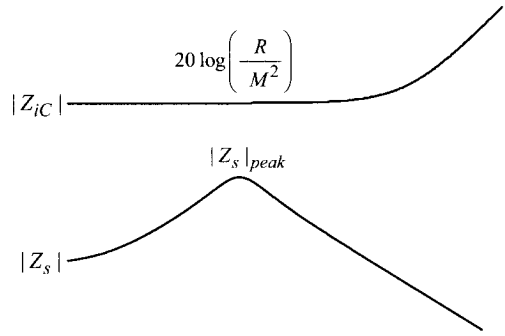


Figure 9.35 Input impedance and source impedance for properly designed dc-to-dc converters.

Examples of input filter design are provided in Problems 9.9 and 9.10 at the end of this chapter.

9.2.6 Impacts of Source Impedance on Loop Gain and Output Impedance

The source impedance also influences the output impedance and loop gain of the converter. It was shown [2, 4] that the output impedance $Z_o(s)$ with a source impedance $Z_s(s)$ is given by

$$Z_o(s) = Z_{oC}(s)\frac{1 + \dfrac{Z_s(s)}{Z'_{iC}(s)}}{1 + \dfrac{Z_s(s)}{Z_{iC}(s)}} \tag{9.37}$$

where $Z_{oC}(s)$ the output impedance of the converter with an ideal voltage source and $Z'_{iC}(s)$ is the input impedance of the converter evaluated with its feedback loop opened and the output port shorted. The output impedance won't be altered with the addition of the source impedance, if the conditions $|Z_s/Z_{iC}| \ll 1$ and $|Z_s/Z'_{iC}| \ll 1$ are met for all frequencies.

It was also shown that the loop gain $T_m(s)$ with $Z_s(s)$ is expressed as

$$T_m(s) = T_{mC}(s)\frac{1 + \dfrac{Z_s(s)}{Z''_{iC}(s)}}{1 + \dfrac{Z_s(s)}{Z'''_{iC}(s)}} \tag{9.38}$$

where $T_{mC}(s)$ is the loop gain with an ideal voltage source, and $Z''_{iC}(s)$ is the input impedance of the converter evaluated with its feedback loop closed and the output voltage nullified [2, 4, 5]. The quantity $Z'''_{iC}(s)$ denotes the input impedance of the converter evaluated with its feedback loop opened. The loop gain remains unaffected if the conditions $|Z_s/Z''_{iC}| \ll 1$ and $|Z_s/Z'''_{iC}| \ll 1$ are met for all frequencies.

The four different input impedance expressions, $Z_{iC}(s)$, $Z'_{iC}(s)$, $Z''_{iC}(s)$, and $Z'''_{iC}(s)$ appearing in (9.37) and (9.38), vary with the converter topology and control scheme. In fact, the input impedance analysis in the previous section is only valid for the three basic dc-to-dc converters that employ the conventional voltage mode control. Detailed analyses of the input impedances, output impedance, and loop gain of dc-to-dc converters with different control schemes are given in [2, 5, 7].

9.3 CONSIDERATION FOR NON-RESISTIVE LOAD

The control design of dc-to-dc converters has previously been investigated based on the assumption that the converter is feeding a resistive load. However, the actual load of dc-to-dc converters is commonly a combination of passive and active components, whose impedance characteristics could widely deviate from a pure resistor. For most applications, furthermore, advance information about the actual load impedance characteristics is unavailable.

Figure 9.36 shows a regulated dc-to-dc converter coupled with a general load impedance Z_L. Despite the uncertainty in Z_L characteristics, the low-frequency asymptote of Z_L is uniquely determined from the converter's output voltage V_O and the dc load current I_O

$$Z_L(j0) = R_{dc} = \frac{V_O}{I_O} \tag{9.39}$$

The quantity R_{dc} can be considered as an *equivalent resistive load* for the unknown Z_L. The equivalent resistive load R_{dc} is determined from the dc specification of the load, without the knowledge about the ac or impedance characteristics of the load. The control can be designed for its equivalent resistive load R_{dc} and the performance of the converter with the actual load impedance Z_L can be evaluated when the ac characteristics of Z_L are available.

■ EXAMPLE 9.11 Converter Performance with General Load Impedance

This example illustrates the effect of the load impedance on the closed-loop performance of the converter. Figure 9.37(a) shows three different non-resistive loads whose equivalent resistive load is all identical, $R_{dc} = 1\ \Omega$. Figure 9.37(b) shows the Bode plots of the three different load impedances. Apart from the low-frequency asymptote, the load impedances reveal very different characteristics. Figure 9.38(a) shows the loop gain and Fig. 9.38(b) depicts the output impedance of the converter with the three non-resistive loads, in comparison with that of the converter with a pure resistive load R_{dc}. It can be observed that the control design for a resistive load also provides good performance for the converter loaded with the non-resistive loads. Figure 9.39 shows the output voltage of the converter in response to the step changes of $R_{dc} = 0.5\ \Omega \Rightarrow 1\ \Omega \Rightarrow 0.5\ \Omega$. Same as the frequency-domain performance

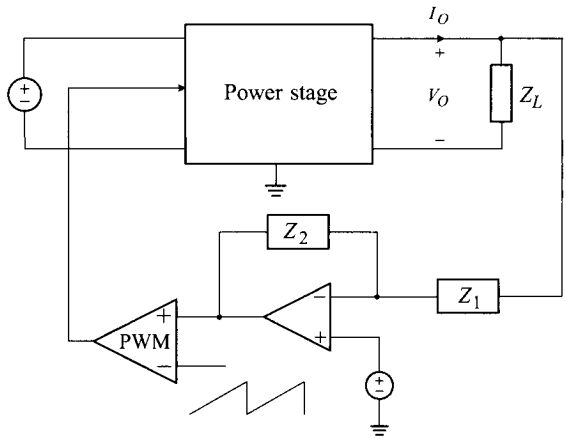
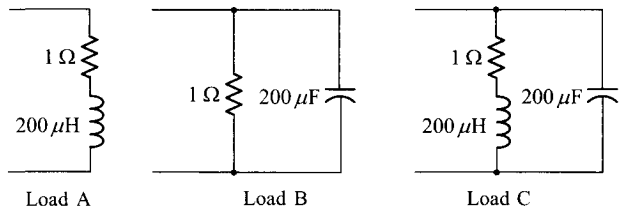
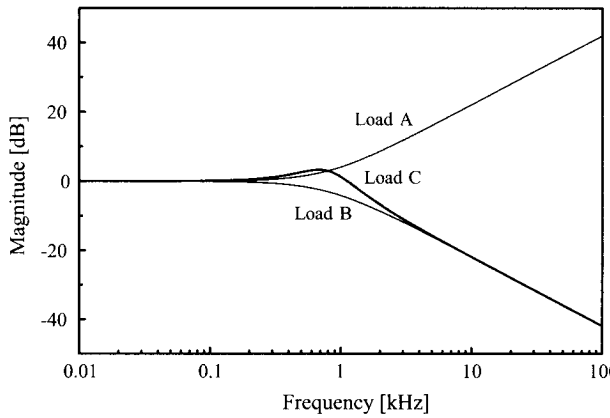


Figure 9.36 Converter loaded with general load impedance.



(a)



(b)

Figure 9.37 Three different load systems. (a) Circuit diagram. (b) Bode plot of load impedance Z_L.

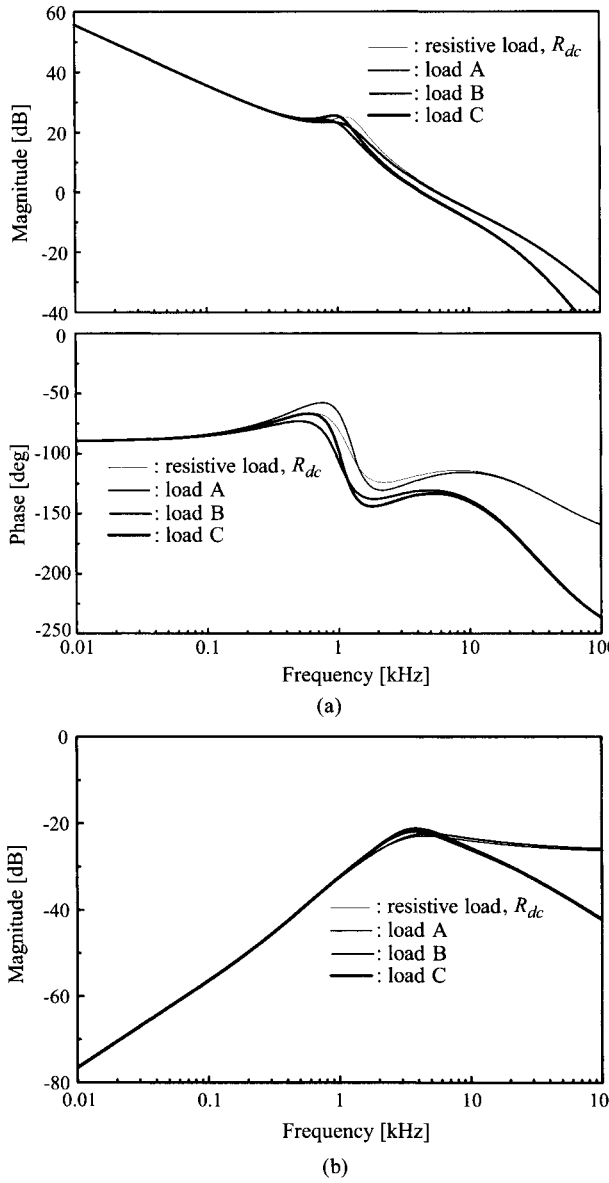


Figure 9.38 Frequency-domain performance with different load impedances. (a) Loop gain. (b) Output impedance.

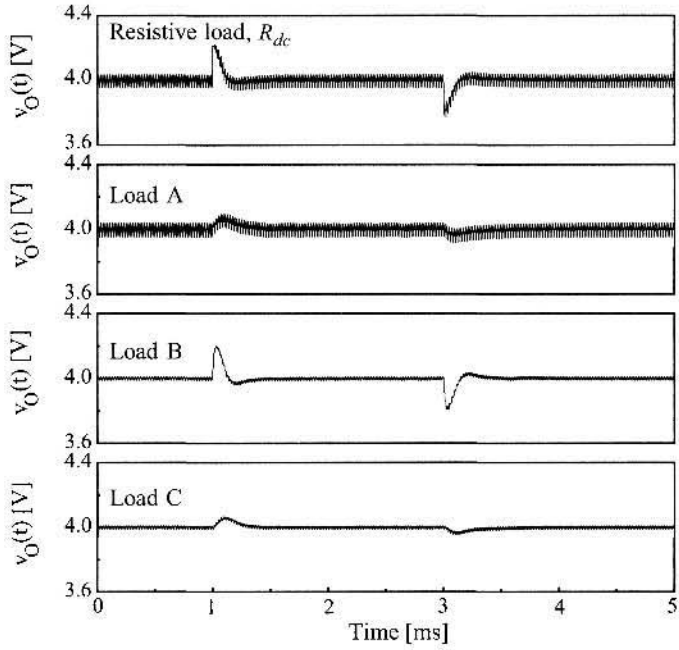


Figure 9.39 Step-load response with different load impedances.

case, the control designed for R_{dc} offers good transient responses for the non-resistive loads.

9.4 SUMMARY

This chapter investigated practical details about modeling, analysis, and design of dc-to-dc converters in real applications. The small-signal modeling, established for the three basic non-isolated converters operating in continuous conduction mode (CCM), is extended to include all isolated/non-isolated dc-to-dc converters operating in both CCM and discontinuous conduction mode (DCM). The small-signal dynamics of dc-to-dc converters in DCM operation are analyzed and compared with those of CCM operation. It was verified that the control design intended for CCM operation guarantees stability in DCM operations and therefore is suited for both CCM and DCM operations.

The input impedance of regulated dc-to-dc converters has unique characteristics — the input impedance behaves as a negative resistance at low frequencies. The negative input resistance is caused by the distinct functional behavior of regulated dc-to-dc converters. A regulated dc-to-dc converter always draws a predetermined power and therefore functions as a constant power load. When the input voltage of a

constant power load increases, the input current must decrease, resulting in a negative incremental input resistance.

The negative input resistance could cause stability problems in practical dc-to-dc operations. In real applications, regulated converters are not directly connected to the voltage source. An input filter stage is usually employed between the voltage source and a regulated dc-to-dc converter, in order to meet mandatory EMI standards. Accordingly, the power stage of the regulated dc-to-dc converter sees the output impedance of the input filter as the source impedance, whereas the power stage itself exhibits a negative input resistance.

A certain source impedance, when coupled with the negative input resistance of the converter power stage, could destablize a formerly stable dc-to-dc converter. The danger of this *source-impedance induced instability* can be minimized by placing the loop gain crossover frequency at higher frequencies than $Q\omega_o$. This design objective is in fact identical to the design strategy developed in Section 8.4.2 for the ideal voltage source. Accordingly, the previous design procedures for an ideal voltage source can be adapted to the converters with finite source impedance.

The load of dc-to-dc converters is typically a combination of passive and active components which show non-resistive impedance characteristics. This chapter demonstrated that dc-to-dc converters designed for the *equivalent resistive load*, $R_{dc} = V_O/I_O$, maintain good performance when feeding various non-resistive loads.

This chapter concluded that the design and analysis techniques covered in this book, even though they appear only to cover the three basic converters in CCM operation with an ideal voltage source and resistive load, actually all apply to real circumstances. The design and analysis method is well suited for isolated/non-isolated dc-to-dc converters operating in both CCM and DCM with non-ideal source and load systems.

REFERENCES

1. V. Vorpérian, "Simplified analysis of PWM converters using the model of the PWM switch: Part I and II," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-26, no. 3, pp. 490-505, May 1990.
2. R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *Proc. IEEE-IAS Annu. Meeting*, 1976, pp. 366-382.
3. R. D. Middlebrook, "Design techniques for preventing input filter oscillation in switch-mode regulators," in *Proc. Powercon 5*, May 1978, pp. A3.1-A3.16.
4. B. Choi, D. Kim, D. Lee, S. Choi, and J. Sun, "Analysis of input filter interactions in switching power converters," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 452-460, Mar. 2007.
5. D. Kim, D. Son, and B. Choi, "Input impedance analysis of PWM Dc-to-Dc converters," in *Proc. IEEE Appl. Power Electron. Conf.*, 2006, pp.1339-1346.
6. B. Choi and B. H. Cho, "Intermediate line filter design to meet both impedance compatibility and EMI specification," *IEEE Trans. Power Electron.*, vol. 10, no. 5, pp. 583-588, Sep. 1995.

7. D. Kim, B. Choi, D. Lee, and J. Sun, "Dynamics of current-mode controlled dc-to-dc converters with input filter stage," in *Proc. IEEE Power Electron. Specialists' Conf.*, 2005, pp. 2648-2656.

PROBLEMS

9.1* Derive the small-signal equations of the DCM PWM switch model expressed in (9.23) and (9.24) in the text. The derivation can be expedited by incorporating (9.22) into (9.21) and taking the partial derivative of the resulting equations.

9.2 Construct the DCM small-signal model for the buck converter and boost converter. Specify the five model parameters $\{r_i\ k_i\ g_f\ k_o\ r_o\}$ in terms of the operational conditions and steady-state circuit variables of the converter.

9.3* Consider the forward converter shown in Fig. P9.3.

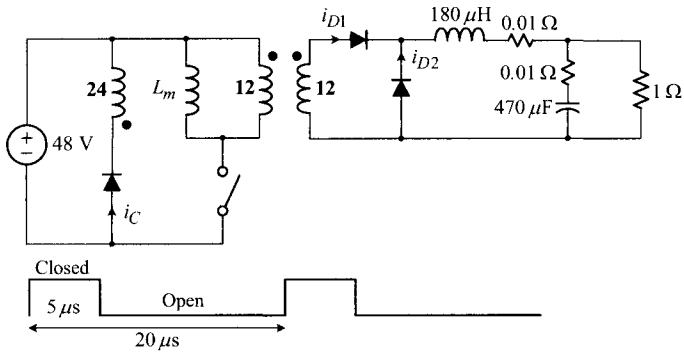


Fig. P9.3

a) Assume $L_m = 480\ \mu$H and answer the following questions.
i) Sketch the steady-state waveforms of $\{i_{D1}\ i_{D2}\ i_C\}$ for the two operational periods. Label the maximum and minimum values of each waveform.
ii) Draw the small-signal model of the power stage. Show all model parameters.
b) Now assume $L_m = \infty$ and repeat **a)**.

9.4 A two-switch forward converter is shown in Fig. P9.4. Answer the questions.
a) Assume $L_m = 72\ \mu$H for the magnetizing inductance of the transformer and sketch the steady-state waveforms of $\{i_{D1}\ i_C\ v_S\ v_Q\}$ for the two operational periods. Label the maximum and minimum values of each waveform.
b) Sketch the small-signal model of the power stage. Show all model parameters.

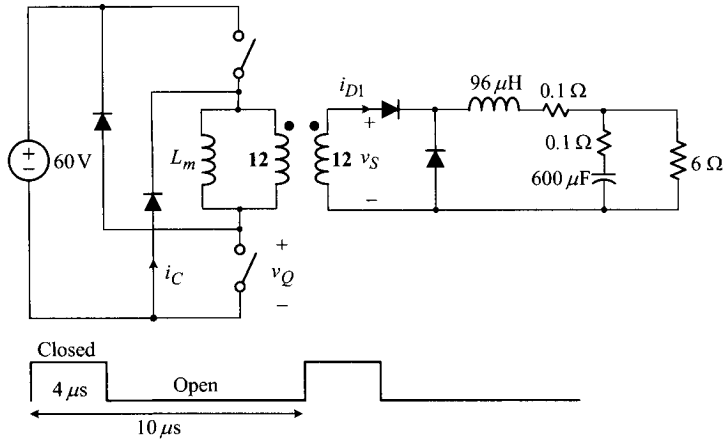


Fig. P9.4

9.5* Figure P9.5 shows a full-bridge PWM converter. Answer the questions.

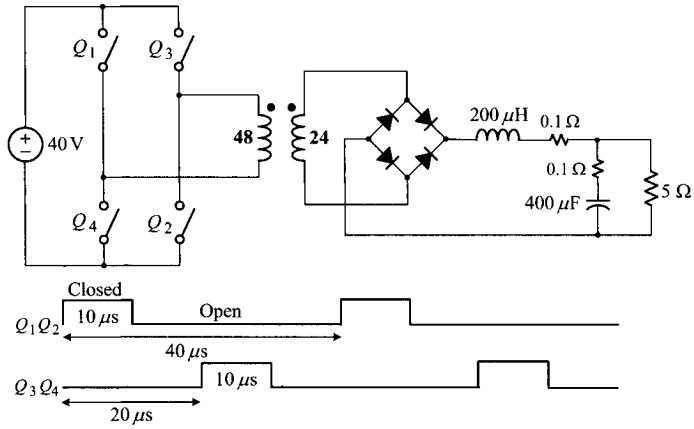


Fig. P9.5

a) Referring to the circuit diagram and the switch drive signals, draw an average model that predicts the time-averaged power stage dynamics. Show all model parameters.

b) Construct the small-signal model of the power stage. Show all model parameters.

9.6* Consider the flyback converter shown in Fig. P9.6 and answer questions.

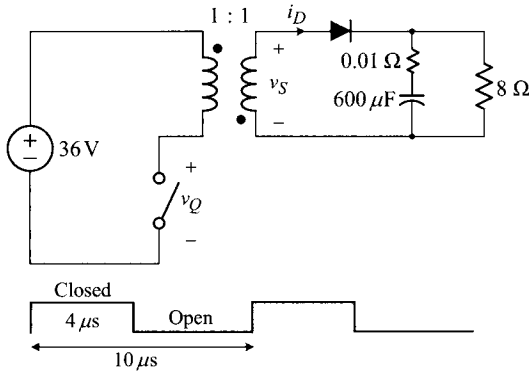


Fig. P9.6

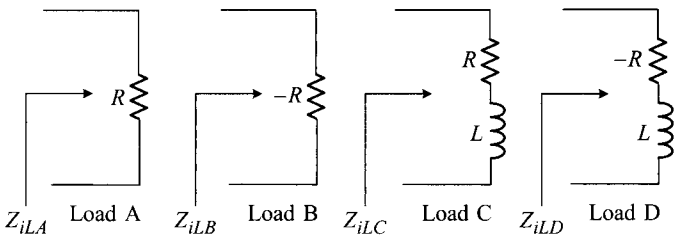
a) Assume L_m = 72 μH for the magnetizing inductance of the transformer and sketch the steady-state waveforms of $\{i_D\ v_S\ v_Q\}$ for the two operational periods. Label the maximum and minimum values of each waveform.

b) Sketch a circuit model that predicts the time-averaged dynamics of the power stage.

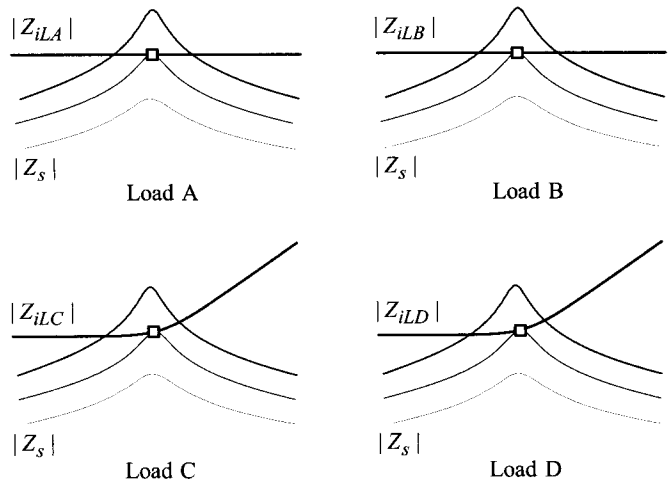
c) Sketch the small-signal model of the power stage. Show all model parameters.

9.7* Four different input impedances, Z_{iLA}, Z_{iLB}, Z_{iLC}, and Z_{iLD}, are defined for the load circuits shown in Fig. P9.7(a). Load B and Load D include a negative resistance. Now assume that each load circuit is combined with various source impedances, resulting in the four impedance plots shown in Fig. P9.7(b). Assume that the phase of the source impedance $\angle Z_s$ varies from +90° to −90°.

For each impedance plot, sketch the corresponding polar plots of the ratios of the source impedance to input impedance, $Z_s(s)/Z_{iL}(s)$, to illustrate the possibility of the source-impedance induced instability. Explain the consequential effects of the negative resistance.



(a)



(b)

Fig. P9.7

9.8* As illustrated in Fig. P9.8(a), a reciprocal two-port network meets the condition

$$A_{vF}(s) = A_{iF}(s)$$

where $A_{vF}(s) = v_F(s)/v_S(s)$ is the forward open-circuit voltage transfer function and $A_{iF}(s) = i_S(s)/i_F(s)$ is the backward short-circuit current transfer function. Two reciprocal networks, Filter A and Filter B, are shown in Fig. P9.8(b).

For Filter A and Filter B, verify the relationship $A_{vF}(s) = A_{iF}(s)$ by directly evaluating the transfer functions. The results of this problem will be used in Problems 9.9 and 9.10 which deal with the input filter design.

9.9** Figure P9.9 shows a single-stage filter with a damping branch. This circuit is often employed as an input filter in low- and medium-power dc-to-dc converters. This filter circuit was analyzed in Problem 9.8.

a) Prove that the backward short-circuit current transfer function $A_{iF}(s)$ and the short-circuit output impedance $Z_{oF}(s)$ of the filter are given by

$$A_{iF}(s) \approx \frac{1}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}}$$

$$Z_{oF}(s) \approx \frac{sL_f}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}}$$

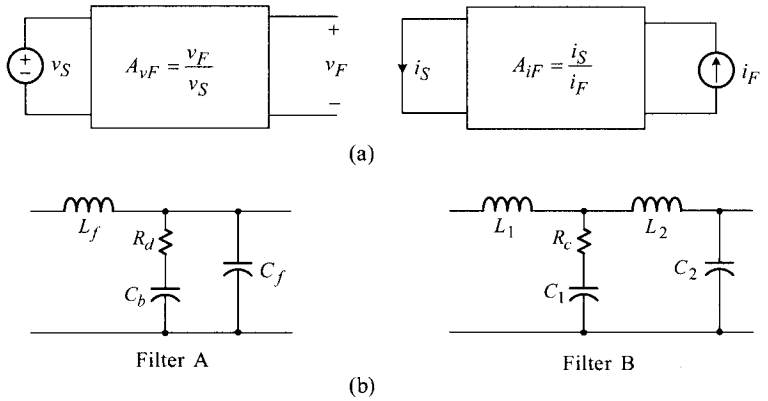


Fig. P9.8

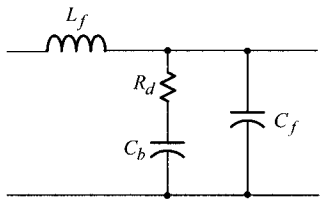


Fig. P9.9

with

$$Q = R_d \sqrt{\frac{C_f}{L_f}} \qquad \text{and} \qquad \omega_o = \frac{1}{\sqrt{L_f C_f}}$$

under the assumptions $C_b \gg C_f$ and $C_b R_d \gg L_f / R_d$.

b) Show that the peak value of the output impedance is given by

$$|Z_{oF}|_{peak} = \sqrt{\frac{L_f}{C_F}} = R_d$$

if the condition $Q = 1$ is met.

c) The input filter design is usually specified by the magnitude of the backward short-circuit current transfer function, evaluated at the switching frequency of the converter. The peak value of the output impedance of the filter is also specified to avoid the source-impedance induced instability for the given input impedance characteristics of the dc-to-dc converter. Design the input filter for the following specifications:

i) $|A_{iF}|_{@100\ \text{kHz}} = -35$ dB ii) $|Z_{oF}|_{peak} = +5$ dB iii) $Q = 1$ iv) $C_b = 10 C_f$.

Verify your design with PSpice® simulations. Also confirm the assumption $C_b R_d \gg L_f/R_d$.

9.10* Figure P9.10 is a two-stage input filter commonly adapted for high-power dc-to-dc converters. This filter was analyzed in Problem 9.8.

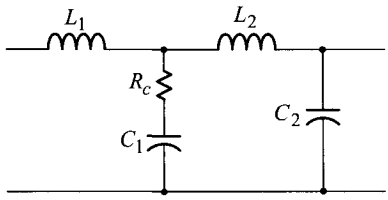


Fig. P9.10

a) Prove that the backward short-circuit current transfer function $A_{iF}(s)$ and the short-circuit output impedance $Z_{oF}(s)$ of the filter are given by

$$A_{iF}(s) \approx \frac{1 + \dfrac{s}{\omega_{z1}}}{\left(1 + \dfrac{s}{Q_1\omega_{o1}} + \dfrac{s^2}{\omega_{o1}^2}\right)\left(1 + \dfrac{s}{Q_2\omega_{o2}} + \dfrac{s^2}{\omega_{o2}^2}\right)}$$

$$Z_{oF}(s) \approx \frac{sL_1\left(1 + \dfrac{s}{\omega_{z1}}\right)\left(1 + \dfrac{s}{\omega_{z2}}\right)}{\left(1 + \dfrac{s}{Q_1\omega_{o1}} + \dfrac{s^2}{\omega_{o1}^2}\right)\left(1 + \dfrac{s}{Q_2\omega_{o2}} + \dfrac{s^2}{\omega_{o2}^2}\right)}$$

with

$$Q_1 = \frac{1}{R_c}\sqrt{\frac{L_1}{C_1}} \qquad \omega_{o1} = \frac{1}{\sqrt{L_1 C_1}}$$

$$Q_2 = \frac{1}{R_c}\sqrt{\frac{L_2}{C_2}} \qquad \omega_{o2} = \frac{1}{\sqrt{L_2 C_2}}$$

$$\omega_{z1} = \frac{1}{C_1 R_c} \qquad \omega_{z2} = \frac{R_c}{L_2}$$

with the assumptions $L_1 \gg L_2$, $C_1 \gg C_2$, $L_1 \gg R_c^2 C_2$, and $C_1 \gg L_2/R_c^2$.

b) Show that the peak value of the output impedance is given by

$$|Z_{oF}|_{peak} = \sqrt{\frac{L_1}{C_1}} = R_c$$

if the condition $Q_1 = Q_2 = 1$ is met.

c) Design the input filter for the following specifications
i) $|A_{iF}|_{@100\text{ kHz}} = -43$ dB ii) $|Z_{oF}|_{peak} = +23$ dB iii) $Q_1 = Q_2 = 1$ iv) $\omega_{o2} = 10\,\omega_{o1}$.
Verify your design with PSpice® simulations. Also, confirm the assumptions $L_1 \gg R_c^2 C_2$ and $C_1 \gg L_2/R_c^2$.

9.11** Figure P9.11 illustrates two different cases of the polar plot for the impedance ratio of $Z_s(s)/Z_{iC}(s)$ where $Z_s(s)$ is the source impedance and $Z_{iC}(s)$ is the input impedance of a dc-to-dc converter.

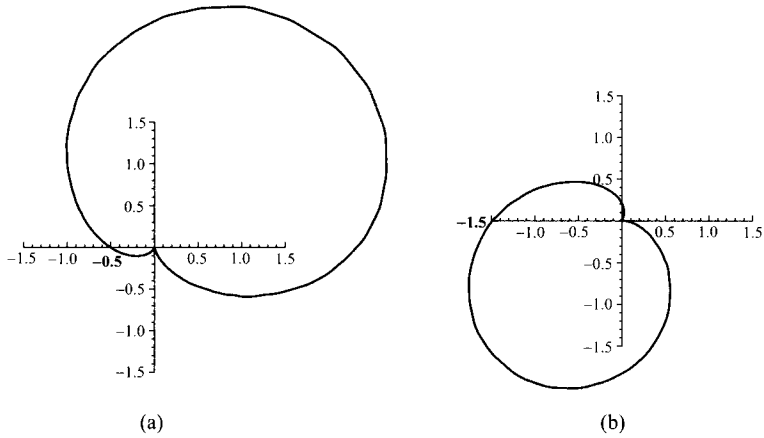


Fig. P9.11

a) For Case (a), determine the stability of the converter. Now assume that the magnitude of the source impedance $|Z_s|$ is varied while its phase characteristics remain the same. The input impedance of the converter also remains unchanged. State the condition that makes the converter marginally stable.
b) Repeat **a)** for Case (b).

9.12* The loop gain $T_m(s)$ of a converter combined with a source impedance $Z_s(s)$ is given by

$$T_m(s) = T_{mC}(s)\frac{1 + \dfrac{Z_s}{Z''_{iC}}}{1 + \dfrac{Z_s}{Z'''_{iC}}}$$

where $T_{mC}(s)$ is the loop gain with an ideal voltage source, and $Z''_{iC}(s)$ and $Z'''_{iC}(s)$ are the input impedance of the converter evaluated with the two specific conditions that were described in Section 9.2.6.

Figure P9.12 shows four different cases of the magnitude plots of the transfer functions associated with the above equation. For each case, sketch the profile

of the $|T_m|$ based on the asymptotic analysis. Show all the prominent features of the loop gain profile.

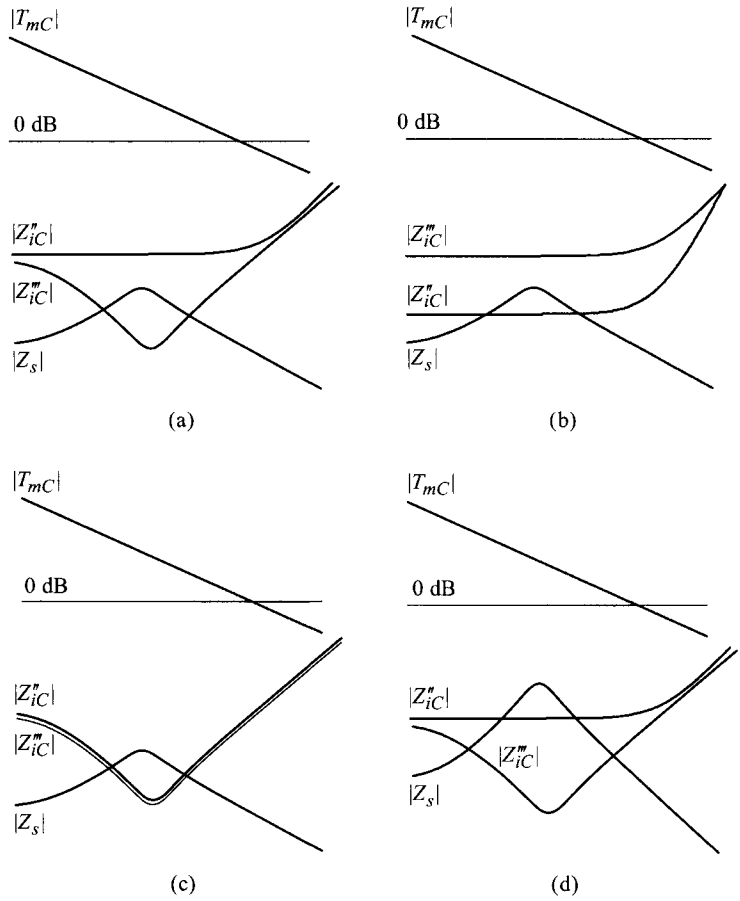


Fig. P9.12

PART III

CURRENT MODE CONTROL

Pulsewidth Modulated Dc-to-Dc Power Conversion. By Byungcho Choi

CHAPTER 10

CURRENT MODE CONTROL — FUNCTIONAL BASICS AND CLASSICAL ANALYSIS

The control scheme studied in Chapters 3 and 8 employs the output voltage as the only feedback signal in the process of generating the pulsewidth modulated (PWM) switch drive signal. This control scheme is called voltage mode control in the sense that the output voltage alone is involved in the PWM process. As introduced in Section 8.4.7, there exists an alternative control scheme for PWM dc-to-dc converters, called current mode control.

Current mode control refers to a class of control schemes that uses the inductor current as an additional functional component in the PWM process. Thus, current mode control uses both the output voltage and inductor current for the closed-loop PWM control. Current mode control is implemented in many different forms by changing the method of current sensing or the way of utilizing the sensed current. Among various current mode control schemes, the most popular is the peak current mode control which employs the peak value of the inductor current as a control variable.

In the previous chapters, we studied voltage mode control. All discussions about the dynamic analysis and control design were presented with regard to voltage-mode controlled PWM converters. However, modern PWM dc-to-dc converters extensively adapt current mode control rather than voltage mode control.

Pulsewidth Modulated Dc-to-Dc Power Conversion. By Byungcho Choi

While the theoretical basics acquired from voltage mode control are equally applicable to current mode control, additional knowledge is necessary for current mode control. As will be shown shortly, the principle of current mode control is rather simple and straightforward. However, its dynamic characteristics are complex and somewhat intriguing. In fact, the dynamic analysis of current mode control had been one challenging and active research topic in the late 1980s through the early 1990s.

This chapter deals with the peak current mode control, covering both functional basics and dynamic characteristics. Motivation, evolution, and implementation of the peak current mode control are first discussed. Then, the dynamic analysis and control design are covered. This chapter also investigates the closed-loop performance of peak current-mode controlled PWM converters. In particular, the design and performance of the peak current mode control, employed to boost and buck/boost converters that have the right-half plane (RHP) zero in their transfer functions, are addressed in detail.

10.1 CURRENT MODE CONTROL BASICS

The current section presents the evolution, benefits, and issues of current mode control. While most contents are directed towards the peak current mode control, other types of current mode control are also introduced.

10.1.1 Evolution to Peak Current Mode Control

The concept of current mode control is illustrated in Fig. 10.1 which compares current mode control and voltage mode control, both adapted to a buck converter. Figure 10.1(a) shows voltage mode control, where the PWM is performed using the ramp signal V_{ramp} and the control voltage v_{con}, derived from the voltage feedback circuit. At the onset of each operational period, the switch is turned-on and later turned-off at the instant V_{ramp} intersects with v_{con}. The output voltage is regulated at the reference voltage, $V_O = V_{ref}$, by the condition $|Z_2(j0)|/|Z_1(j0)| = \infty$ in the voltage feedback circuit. The value of v_{con} is automatically adjusted to yield the required duty ratio for the output voltage regulation, $V_O = DV_S = V_{ref}$.

A time-varying piecewise linear waveform is necessary for PWM operation. In the case of voltage mode control, a ramp signal is generated inside the controller and used for the time-varying waveform. However, for the purpose of PWM, other linear waveforms can be used. In particular, the triangular waveform can be employed for the PWM process. More so, the required triangular waveform is already available in the power stage waveforms. In all PWM converters, the inductor current linearly increases during the on-time period and decreases during the off-time period, thus becoming a triangular waveform.

Figure 10.1(b) illustrates an example of current mode control. The inductor current is sensed via the current sensing network (CSN) and converted into the voltage signal, v_I in Fig. 10.1(b). The sensed voltage signal v_I is then compared against the control signal v_{con}, in order to determine the instant to turn off the switch. Current mode

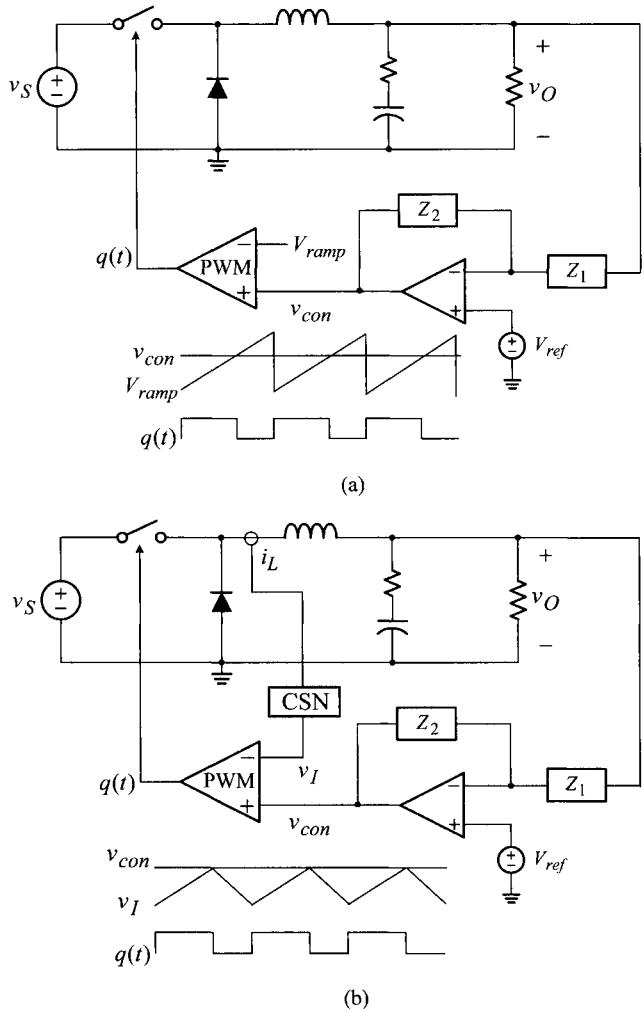


Figure 10.1 Control schemes for PWM converters. (a) Voltage mode control. (b) Current mode control.

control uses the triangular inductor current as a functional replacement of the ramp signal in voltage mode control. The structure and function of the voltage feedback circuit remain the same. The output voltage is regulated at $V_O = V_{ref}$ as long as the condition $|Z_2(j0)|/|Z_1(j0)| = \infty$ is met.

Compensation Ramp

The original motivation of current mode control was to exploit the *free* inductor current waveform in place of the *costly* ramp signal; in the past, the creation of the

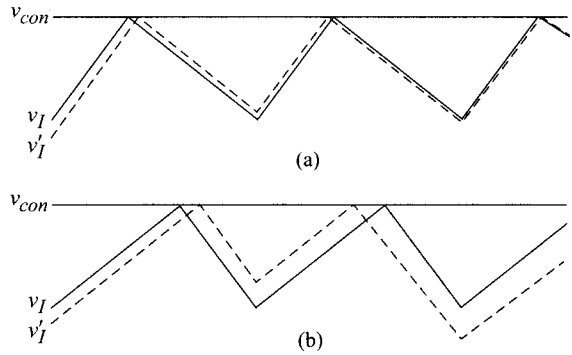


Figure 10.2 Propagation of current feedback signal disturbance. (a) Stable operation with $D < 0.5$. (b) Unstable operation with $D > 0.5$.

ramp signal was not as easy as is the case nowadays. However, it was immediately found that current mode control has one critical problem. This problem is illustrated in Fig. 10.2, which shows the propagation of the disturbed current feedback signal, v_I, for two different cases. Figure 10.2(a) is the case where the duty ratio is less than 0.5. The solid line v_I is the original current feedback signal, while the dashed line v_I' represents the perturbed current feedback signal. As time elapses, the distance between the two feedback signals shrinks and the initial disturbance eventually disappears; in short, the converter is stable.

Figure 10.2(b) is the case where the duty ratio is larger than 0.5. In contrast to the previous case, the initial disturbance successively grows, shortly developing into an erratic behavior. This unstable operation is called the sub-harmonic oscillation, referring to the nonlinear oscillation occurring at half the switching frequency. Thus, when the duty ratio D exceeds 0.5, current mode control becomes unstable and ends up with the sub-harmonic oscillation.

The remedy for the sub-harmonic oscillation is simple. The solution is to reintroduce the ramp signal. This situation is shown in Fig. 10.3(a), where the current feedback signal v_I is summed with V_{ramp} and the resulting signal is compared against v_{con}. Figure 10.3(b) illustrates the propagation of the disturbance in the current feedback signal. Unlike the previous case, the initial disturbance, brought in under the condition $D > 0.5$, gradually lessens until it vanishes. The ramp signal stabilizes the PWM process and the converter thus operates properly for the entire duty ratio range, $0 < D < 1$. The ramp signal employed for this purpose is called the *compensation ramp*.

Although current mode control was first conceived to remove the ramp signal in the PWM process, the compensation ramp is still necessary to avoid the sub-harmonic oscillation. Thus, the initial objective is not achieved. Instead, it was soon revealed that current mode control offers considerable advantages even though it still requires the compensation ramp. The merits of current mode control will be described in the next section.

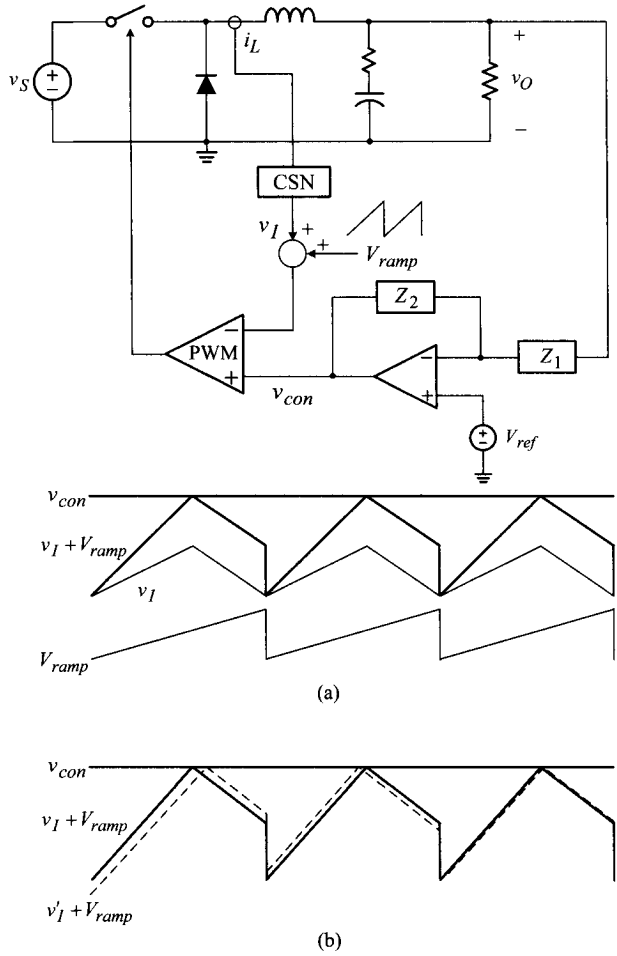


Figure 10.3 Addition of compensation ramp to avoid sub-harmonic oscillation. (a) Control scheme. (b) Propagation of current feedback signal disturbance.

The stabilizing effect of the compensation ramp is explained using the current feedback signal illustrated in Figs. 10.4 and 10.5. Figure 10.4(a) shows the structure and PWM waveforms of current mode control, where the current-to-voltage conversion gain of CSN is assumed unity for simplicity: thus, $v_I = i_L$ for this case. Figure 10.4(a) is rearranged into the equivalent form in Fig. 10.4(b). The PWM waveforms in Fig. 10.4(b) are closely analyzed in Fig. 10.5, which shows the propagation of the perturbed inductor current. In the enlarged illustration in Fig. 10.5, S_n is the slope of the on-time inductor current and S_f is the slope of the off-time inductor current, while S_e is the slope of the compensation ramp. The ΔdT_s denotes the deviation in the on-time period due to the inductor current perturbation. From the graphical

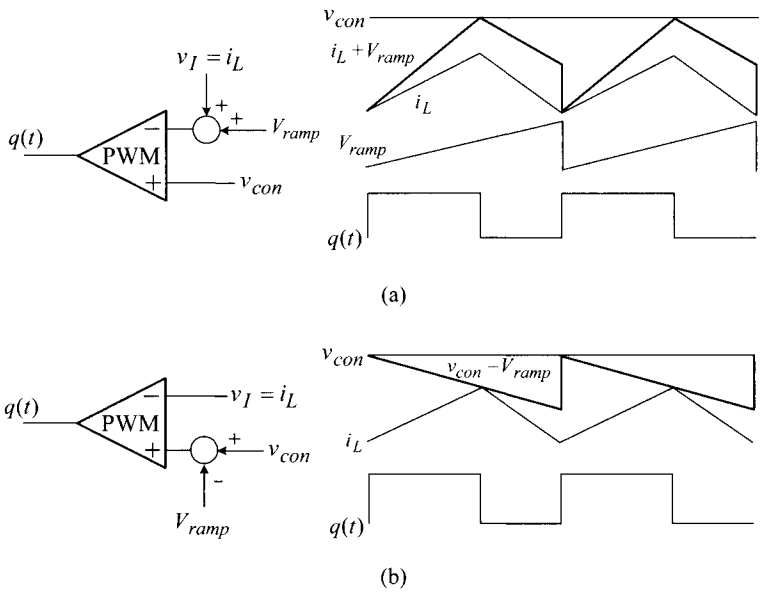


Figure 10.4 Structure and waveforms of current mode control. (a) Current mode control with unity inductor current sensing. (b) Equivalent representation.

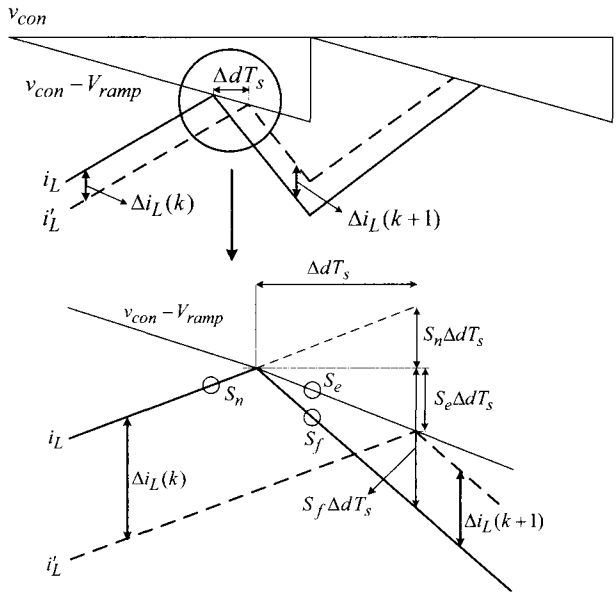


Figure 10.5 PWM waveforms.

construction, the initial distance between the original current i_L and the perturbed current i'_L is given by

$$|i_L(k) - i'_L(k)| = \Delta i_L(k) = S_n \Delta d T_s + S_e \Delta d T_s \tag{10.1}$$

The distance between the two currents after one operational period is given by

$$|i_L(k+1) - i'_L(k+1)| = \Delta i_L(k+1) = S_f \Delta d T_s - S_e \Delta d T_s \tag{10.2}$$

For the successive decrease in the distance between i_L and i'_L in the ensuing operational periods, the condition

$$\frac{\Delta i_L(k+1)}{\Delta i_L(k)} = \frac{S_f - S_e}{S_n + S_e} < 1 \tag{10.3}$$

is required, leading to the condition for the compensation ramp slope

$$S_e > \frac{S_f - S_n}{2} \tag{10.4}$$

for the stabilizing effect. The exact value of the compensation ramp slope should be determined in consideration of the closed-loop performance of the converter. In fact, as will be demonstrated later, the selection of the compensation ramp slope is the most important issue in the design of current mode control. The expression (10.3) also indicates that, when $S_e = 0$ with no compensation ramp, stability is only maintained under the condition $S_n > S_f$, which is true with the duty ratio $D < 0.5$. In other words, the converter is only stable for the duty ratio less than 0.5 at the absence of the compensation ramp.

Peak Current Mode Control

Current mode control can be implemented in many different forms. The most popular among them is the peak current mode control, illustrated in Fig. 10.6. In this control scheme, the switch current is utilized in place of the inductor current. The switch current, which corresponds to the on-time inductor current, is sensed through CSN and blended with the compensation ramp. The peak value of the switch current, or equivalently the peak value of the inductor current, is used to determine the instant to turn off the switch; thus, the control scheme is called the peak current mode control.[†] It should be noted that the switch current sensing is functionally identical to the inductor current sensing because the peak value of the inductor current is employed as the criterion to turn off the switch.

There are several advantages in sensing the switch current rather than the inductor current. The first is the simplicity in CSN. An implementation of CSN for the peak

[†]The inductor current starts declining when the PWM modulator turns off the active switch. Thus, the control scheme ***does not use*** but ***determines*** the peak value of the inductor current. However, the operation of the peak current mode control is broadly interpreted as described above.

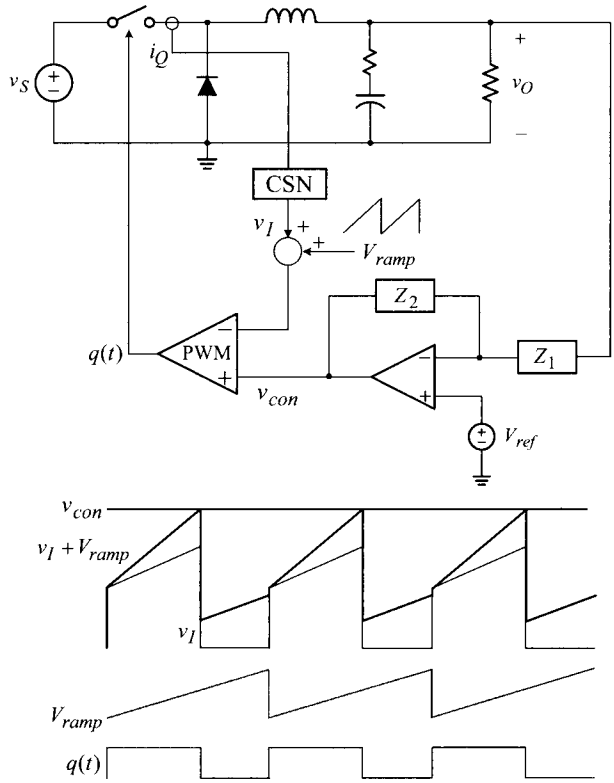


Figure 10.6 Peak current mode control.

current mode control is illustrated in a later example. As the second advantage, the sensed switch current can be used for the over-current protection for semiconductor switches. Due to these advantages, the peak current mode control is widely adapted to modern PWM dc-to-dc converters.

■ EXAMPLE 10.1 Sub-Harmonic Oscillation and Compensation Ramp

This example demonstrates the sub-harmonic oscillation and effects of the compensation ramp. A buck converter employing the peak current mode control is used in this example. The circuit parameters and operational conditions of the buck converter are $L = 40\ \mu$H, $C = 400\ \mu$F, $R_c = 0.01\ \Omega$, $R = 1\ \Omega$, and $f_s = 50$ kHz. The output of the converter is regulated at $V_O = 4$ V, while the input voltage is varied linearly from $V_S = 16$ V to 7 V, and later from $V_S = 7$ V to 16 V. Figure 10.7(a) shows the circuit waveforms where the CSN output alone is used for PWM without the compensation ramp.

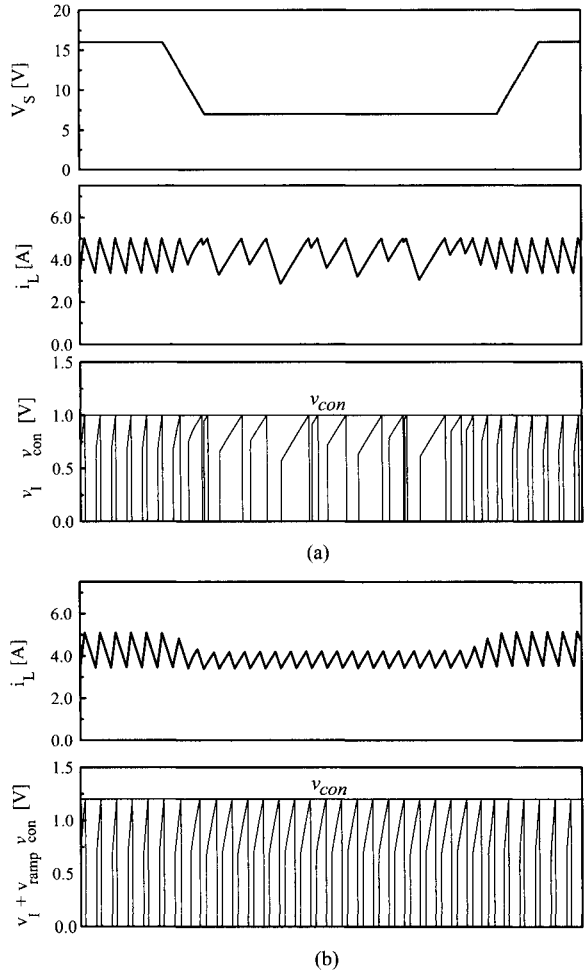


Figure 10.7 Sub-harmonic oscillation and effects of compensation ramp. (a) Sub-harmonic oscillation. (b) Effects of compensation ramp.

When the input voltage is $V_S = 16$ V, thereby yielding the duty ratio $D = 4/16 = 0.25$, the inductor current and PWM waveforms show stable operation. When the input voltage starts declining from $V_S = 16$ V to 7 V, the waveforms depart from the stable pattern and finally develop the sub-harmonic oscillation when the duty ratio is increased to $D = 4/7 \approx 0.57$. Figure 10.7(b) illustrates the waveforms when a compensation ramp is added to the PWM block. The converter shows a stable operation regardless of the change in the input voltage, thereby demonstrating the stabilizing effects of the compensation ramp.

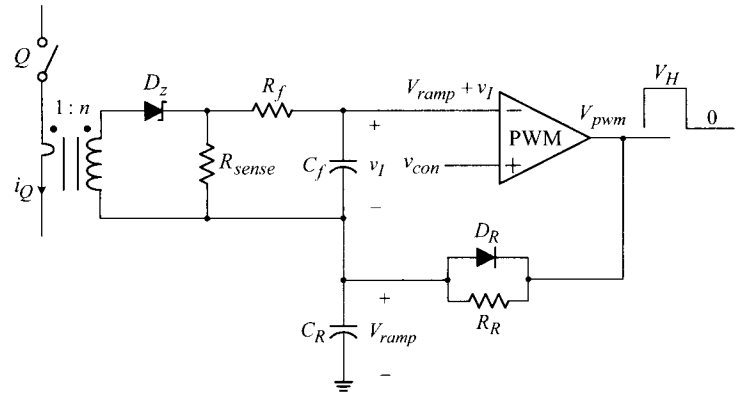


Figure 10.8 Current sensing network with compensation ramp.

■ EXAMPLE 10.2 Current Sensing Network with Compensation Ramp

This example introduces a circuit implementation of CSN with the compensation ramp. The circuit is shown in Fig. 10.8. The switch current i_Q is sensed by a $1 : n$ current transformer and converted into the voltage signal at the sensing resistor R_{sense}. The Zener diode D_z provides a path for the sensed current when the power switch Q is closed, and resets the current transformer when the switch Q is open. A first-order low pass filter is configured using R_f and C_f to remove the switching noise and produce an uncorrupted voltage signal v_I. The ratio of the sensed voltage signal v_I to the switch current i_Q constitutes the current-to-voltage conversion gain of CSN, R_i

$$R_i = \frac{v_I}{i_Q} = \frac{1}{n} R_{sense} \tag{10.5}$$

The compensation ramp is generated using R_R, C_R, and D_R, along with the output of the PWM block, V_{pwm}. At the onset of each operational period, the switch-on signal is issued and V_{pwm} is set at V_H. Then, C_R is charged towards V_H through R_R. When V_{pwm} is reset to zero to turn off the power switch Q, C_R is instantly discharged through D_R. During the charging period, the voltage across C_R is given by

$$V_{ramp}(t) = V_H \left(1 - e^{-\frac{t}{R_R C_R}} \right) \tag{10.6}$$

which can be approximated as a linear ramp signal within the switching period T_s

$$V_{ramp}(t) \approx V_H \left(1 - \left(1 - \frac{t}{R_R C_R} \right) \right)$$

$$= \frac{V_H}{R_R C_R} t \tag{10.7}$$

with the assumption $T_s \ll R_R C_R$. The slope of the ramp signal is given by

$$S_e = \frac{V_H}{R_R C_R} \tag{10.8}$$

and the peak magnitude of the compensation ramp thus becomes

$$V_m = \frac{V_H}{R_R C_R} T_s \tag{10.9}$$

The ramp voltage V_{ramp} is summed with the sensed voltage signal v_I. The resulting signal is fed to the inverting terminal of the PWM comparator whose non-inverting terminal is connected to v_{con}.

10.1.2 Benefits and Issues of Peak Current Mode Control

Peak current mode control still requires the compensation ramp to prevent the sub-harmonic oscillation. Thus, the initial attempt to remove the ramp signal from the PWM process is not fulfilled. Even so, peak current mode control is widely accepted because it offers significant advantages over conventional voltage mode control.

Benefits of Peak Current Mode Control

Advantages of the peak current mode control are mainly recognized in the dynamic performance.

1) Improved dynamic performance: Current mode control improves the dynamic performance of PWM dc-to-dc converters. These benefits are most pronounced in boost and buck/boost converters which have the right-half plane (RHP) zero in their power stage transfer function. In fact, current mode control is indispensable to these converters for stability and performance.

2) Reduced sensitivity of converter dynamics: Current mode control reduces the sensitivity of the converter performance to operational conditions. Current-mode controlled converters exhibit less changes in the dynamic performance at the presence of the source impedance [1, 2] or the switch over between CCM operation and DCM operation [3], when compared with voltage-mode controlled converters.

3) Simple compensation design: Current mode control also simplifies the structure and design of the voltage feedback compensation. In contrast to voltage mode control requiring the three-pole two-zero compensation, current mode control employs a simpler two-pole one-zero circuit for all the three basic PWM converters. Furthermore, the voltage compensation can be standardized so that a single design procedures applies to all PWM dc-to-dc converters.

Issues of Peak Current Mode Control

While current mode control offers the aforementioned advantages, it also complicates the converter dynamics and presents considerable challenges in the small-signal analysis and control design.

1) Dynamic modeling and analysis: Current mode control utilizes an additional feedback from the inductor current on top of the existing output voltage feedback. Thus, in control terminology, current-mode controlled PWM converters are a multi-loop controlled system in which multiple feedback loops are present. The analysis techniques, established in Chapters 7 and 8 for the single-loop voltage mode control, need to be reinforced and extended to deal with the multi-loop controlled system.

2) Sampling effects of current mode control: In peak current mode control, the control action is executed periodically at the instant the inductor current attains its peak value. In other words, the control action is executed by sampling the peak value of the fast-varying inductor current waveform. Due to this feature, the system exhibits the characteristics of sampled-data discrete-time systems. This has been referred to as the *sampling effects* of current mode control. The sampling effects deserve special attention and require pertinent analysis.

10.1.3 Average Current Mode Control and Charge Control

In addition to peak current mode control, two other useful variations of current mode control are the average current mode control and charge control. This section briefly discusses the functional basics of these two control schemes.

Average Current Mode Control

Average current mode control is illustrated in Fig. 10.9. Referring to the block diagram in Fig. 10.9(a) and the control waveforms in Fig. 10.9(b), the operation of the average current mode control is explained as follows. First, the triangular inductor current is sensed through the CSN. The sensed current is converted into a voltage signal v_I and processed through the current feedback circuit, which consists of an op amp along with the current feedback compensation, Z_{I1} and Z_{I2}. If the current feedback compensation meets the condition

$$\frac{|Z_{I2}(j0)|}{|Z_{I1}(j0)|} = \infty \tag{10.10}$$

the sensed voltage signal v_I is forced to follow the control voltage v_{con} as closely as possible. Readers may refer to Section 3.6.1 to validate this statement.

The sensed voltage signal v_I, which is a scaled replica of the triangular inductor current, is also a triangular waveform as shown in Fig. 10.9(b). Accordingly, v_I cannot exactly follow the control voltage v_{con} if v_{con} is a dc or slowly varying waveform. For

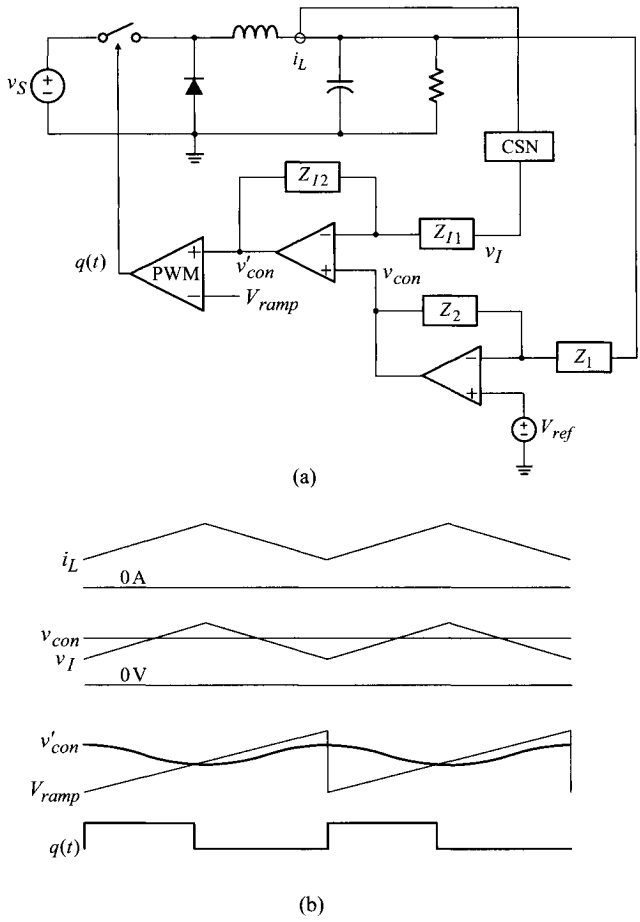


Figure 10.9 Average current mode control. (a) Functional block diagram. (b) Control waveforms.

this case, v_I only tracks v_{con} in the average sense; in other words, the moving average of the scaled inductor current will follow the control voltage v_{con}. On the other hand, the output voltage is regulated at $V_O = V_{ref}$ as long as the voltage feedback circuit satisfies the condition $|Z_2(j0)|/|Z_1(j0)| = \infty$. The output of the current feedback compensation is given by

$$v'_{con}(t) = -\frac{Z_{I2}}{Z_{I1}} v_I(t) + \left(1 + \frac{Z_{I2}}{Z_{I1}}\right) v_{con}(t) \tag{10.11}$$

The composite control signal v'_{con} is compared with the ramp signal to produce the required PWM signal for the output voltage regulation.

The average current mode control forces the moving average of the scaled inductor current to follow the control voltage v_{con}. The potential merit of this feature is not

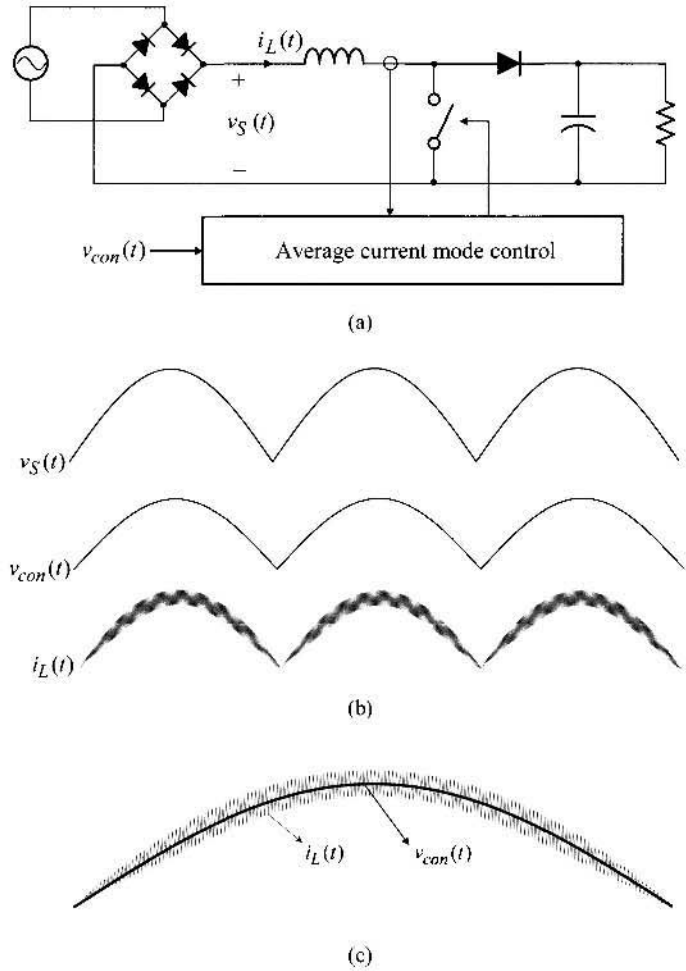


Figure 10.10 PFC ac-to-dc converter and control waveforms. (a) PFC ac-to-dc converter. (b) Major waveforms. (c) Expanded view of $i_L(t)$ and $v_{con}(t)$.

fully revealed in dc-to-dc converters where v_{con} is usually an arbitrary dc waveform. However, there are other applications where the control voltage v_{con} is programmed into a specific waveform. A stand-out example is power factor corrected (PFC) ac-to-dc converters, where v_{con} is given by a low-frequency sinusoidal waveform.

Figure 10.10 is the conceptual illustration of a PFC ac-to-dc converter operating with the average current mode control. The ac-to-dc converter is configured with a bridge rectifier and boost converter. The ac-to-dc converter receives an ac voltage from the utility line. The bridge rectifier performs the full-wave rectification and the resulting voltage waveform is supplied to the boost converter downstream. Accord-

ingly, the input voltage of the boost converter is a rectified line-frequency sinusoid rather than a dc voltage, as illustrated by $v_S(t)$ in Fig. 10.10(b).

Assume that the boost converter is now required to draw its inductor current $i_L(t)$ in a special manner so that the moving average of $i_L(t)$ becomes the same sinusoidal waveform as the converter's input voltage $v_s(t)$. To achieve this goal, the control signal $v_{con}(t)$ is programmed into the line-frequency sinusoid, as shown in Fig. 10.10(b), and the average current mode control is adapted to the boost converter. The resulting inductor current waveform $i_L(t)$ is shown in Fig. 10.10(b). Figure 10.10(c) is an expanded comparison of the $i_L(t)$ and $v_{con}(t)$ waveforms. The moving average of $i_L(t)$ tracks $v_{con}(t)$, as directed by the control law of the average current mode control.

While the detailed discussions about the PFC ac-to-dc converter are beyond the topic of this chapter, it is now seen that the average current mode control is a viable control scheme for PFC ac-to-dc converters. Operations and applications of average current-mode controlled PFC ac-to-dc converters are covered in [4, 5].

Charge Control

Another useful variation of current mode control is the charge control, shown in Fig. 10.11(a). The switch current i_Q is sensed through the CSN and the sensed current is immediately used to charge the capacitor C_I, resulting in the voltage signal v_I shown in Fig. 10.11(b). When v_I intersects with the control voltage v_{con}, the switch-off signal is issued and, at the same time, the capacitor C_I is instantly discharged by closing the parallel switch Q_I.

One obvious advantage of the charge control is the enhanced noise immunity. The switch current i_Q is usually corrupted with the high-frequency ringings and spikes which could cause false triggering. In charge control, the noisy switch current is effectively integrated by charging the capacitor C_I, resulting in a smoothly increasing v_I in Fig. 10.11(b). This practically eliminates the risk of the false triggering even in the presence of substantial high-frequency noises. Further details about the charge control are given in [6].

10.2 CLASSICAL ANALYSIS AND CONTROL DESIGN PROCEDURES

As previously discussed, the peak current mode control implants the discrete-time sampling effects into the converter dynamics. In principle, the sampling effects should be incorporated into the analysis and design of the peak current mode control. This would require discrete-time analyses using z-domain techniques.

Conventionally, the peak current mode control has been analyzed and designed based on the continuous-time s-domain techniques, implicitly assuming that the sampling effects only cause negligible consequences on the converter dynamics. This simplified analysis is referred to as the *classical analysis* in this book. The classical analysis, although it does not include the sampling effects, accurately describes the major dynamics of the peak current mode control and provides legitimate design methodology for most cases. In this chapter, the peak current mode control is

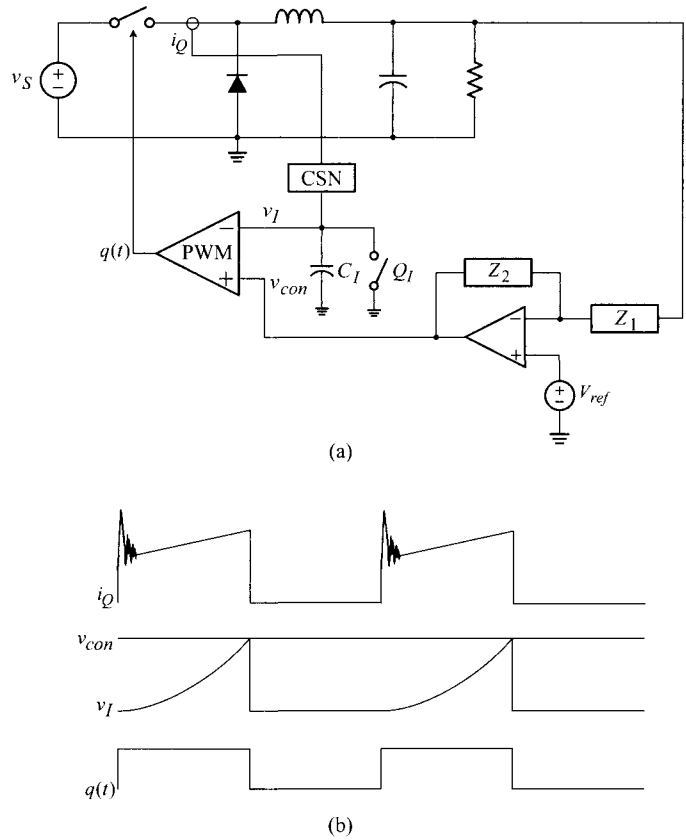


Figure 10.11 Charge control. (a) Functional block diagram. (b) Control waveforms.

investigated via the classical (s-domain) analysis, while postponing the analysis of the sampling effects to the next chapter. The classical analysis will reveal its own value and advantages that would support its long-time prevalence. In particular, the classical analysis provides step-by-step design procedures which offer stability and good dynamic performance for all the three basic PWM converters.

10.2.1 Small-Signal Model for Peak Current Mode Control

Figure 10.12 shows a general circuit diagram of PWM converters employing the peak current mode control. With the connections {a−X p−Y i−Z}, Fig. 10.12 represents the buck converter. Similarly, the connections {i−X a−Y p−Z} lead to the boost converter, while the connections {a−X i−Y p−Z} yield the buck/boost converter.

Figure 10.13 is the small-signal model of the converter, obtained from Fig. 10.12 by replacing the PWM switch, PWM block, and voltage feedback circuit with their respective small-signal models, and by introducing appropriate small-signal excita-

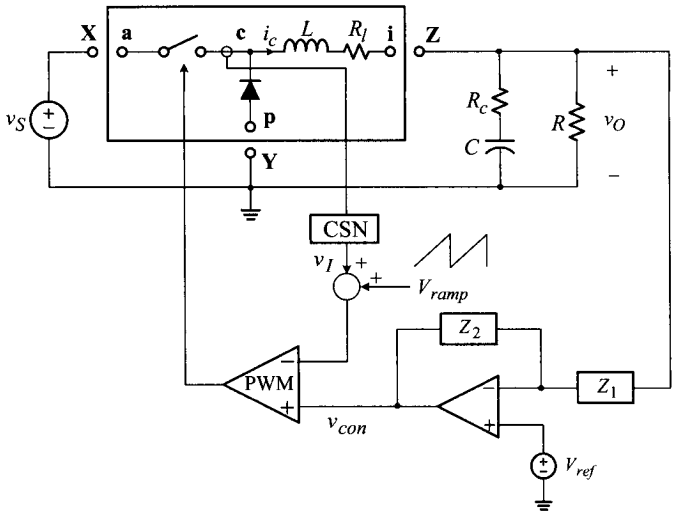


Figure 10.12 General circuit diagram for current-mode controlled PWM converters.

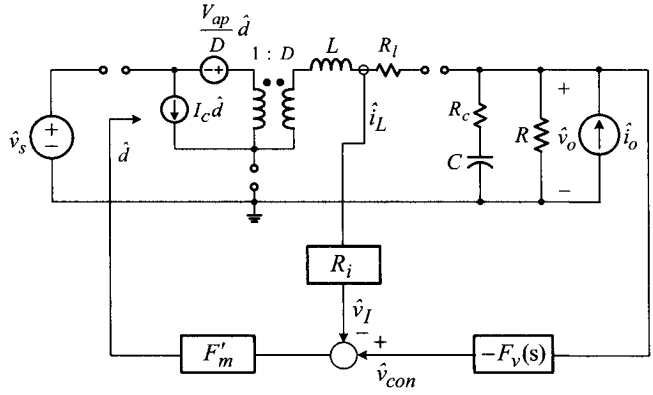


Figure 10.13 Small-signal model for current-mode controlled PWM converters.

tions. In Fig. 10.13, *a feedback path is created from the inductor current $\hat{i}_L$, even though the current is actually sensed from the switch.* This because the control action is executed at the moment the switch current reaches its peak value, as such, the switch current sensing is functionally identical to the inductor current sensing. The feedback path from the inductor current $\hat{i}_L$ accords with this fact. The gain block $F_v(s)$ is the voltage feedback compensation

$$F_v(s) = \frac{Z_2(s)}{Z_1(s)} \tag{10.12}$$

Table 10.1 Expressions for Slopes of PWM Waveforms

	Buck converter	Boost converter	Buck/boost converter
S_n	$\frac{V_S - V_O}{L}R_i$	$\frac{V_S}{L}R_i$	$\frac{V_S}{L}R_i$
S_f	$\frac{V_O}{L}R_i$	$\frac{\lvert V_S - V_O\rvert}{L}R_i$	$\frac{\lvert V_O\rvert}{L}R_i$

and R_i is the CSN gain, given by

$$R_i = \frac{1}{n}R_{sense} \tag{10.13}$$

for the circuit discussed in Example 10.2. The gain block F'_m represents the small-signal gain of the PWM block — the modulator gain of the peak current mode control. The modulator gain of the peak current mode control differs from that of voltage mode control and the notation F'_m is used to emphasize the difference.

Several different expressions for the modulator gain F'_m were proposed in the past. While there are subtle differences in the existing F'_m expressions, they do not cause significant consequences on the analysis and design of the peak current mode control. This book adopts the modulator gain proposed by F. C. Lee [7, 8]

$$F'_m = \frac{2}{(S_n - S_f + 2S_e)T_s} \tag{10.14}$$

where S_n is on-time slope and S_f is off-time slope of the sensed current feedback signal v_I, while S_e is the slope of the compensation ramp. Derivation of the modulator gain is given in Example 10.3. The expressions for S_n and S_f for the three basic converters are summarized in Table 10.1.

Interestingly, the modulator gain in (10.14) correctly predicts the sub-harmonic oscillation, which occurs when the duty ratio D exceeds 0.5 in the absence of the compensation ramp. It can be seen that $S_n > S_f$ with $D < 0.5$, $S_n = S_f$ with $D = 0.5$, and $S_n < S_f$ with $D > 0.5$. When the compensation ramp is not present, or $S_e = 0$, F'_m approaches infinity with $D = 0.5$ and becomes negative with $D > 0.5$. This fact supports the sub-harmonic oscillation occurring with $D \geq 0.5$ and $S_e = 0$.

■ EXAMPLE 10.3 Modulator Gain for Peak Current Mode Control F'_m

This example presents the derivation of the modulator gain given by (10.14). Figure 10.14 shows the modulator waveforms of the peak current mode control, in which the inductor current is assumed to increase cycle-by-cycle so that $i_L(k+1) > i_L(k)$ where $i_L(k)$ is the initial inductor current at the kth switching period. In Fig. 10.14, the current level $\bar{i}_{on}$ is the average value of the inductor

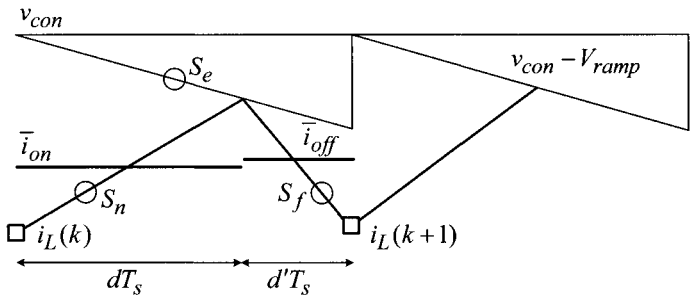


Figure 10.14 Peak current mode control waveforms.

current during the on-time period dT_s and $\bar{i}_{off}$ is that of the off-time period $(1-d)T_s$. The following relationships are derived from Fig. 10.14

$$\bar{i}_{on}(t) = v_{con} - S_e dT_s - \frac{1}{2}S_n dT_s \tag{10.15}$$

$$\bar{i}_{off}(t) = v_{con} - S_e dT_s - \frac{1}{2}S_f(1-d)T_s \tag{10.16}$$

When the inductor current is assumed only to change slowly, $i_L(k) \approx i_L(k+1)$, it becomes $\bar{i}_{on} \approx \bar{i}_{off}$ so that either $\bar{i}_{on}$ or $\bar{i}_{off}$ can be considered as the average inductor current, $\bar{i}_L(t)$. Furthermore, the assumption $i_L(k) \approx i_L(k+1)$ validates the approximation

$$S_n dT_s = S_f(1-d)T_s \tag{10.17}$$

which is rearranged as

$$(S_n + S_f)d = S_f \tag{10.18}$$

By considering $\bar{i}_{off}$ as the approximation of the averaged inductor current $\bar{i}_L(t)$ and using (10.18), the expression (10.16) is modified as

$$\bar{i}_{off}(t) = \bar{i}_L(t) = v_{con} - S_e dT_s - \frac{1}{2}(S_n + S_f)d(1-d)T_s \tag{10.19}$$

Application of the linearization process to (10.19) yields

$$\begin{aligned} I_L + \hat{i}_L = {} & (V_{con} + \hat{v}_{con}) - S_e(D+\hat{d})T_s \\ & -\frac{1}{2}(S_n + S_f)(D+\hat{d})\big(1-(D+\hat{d})\big)T_s \end{aligned} \tag{10.20}$$

By equating the ac terms in (10.20), it becomes

$$\hat{v}_{con} - \hat{i}_L = \left(S_e T_s + \frac{1}{2}(S_n + S_f)T_s(1-2D)\right)\hat{d} \tag{10.21}$$

Using the steady-state expression of (10.18)

$$(S_n + S_f)D = S_f \tag{10.22}$$

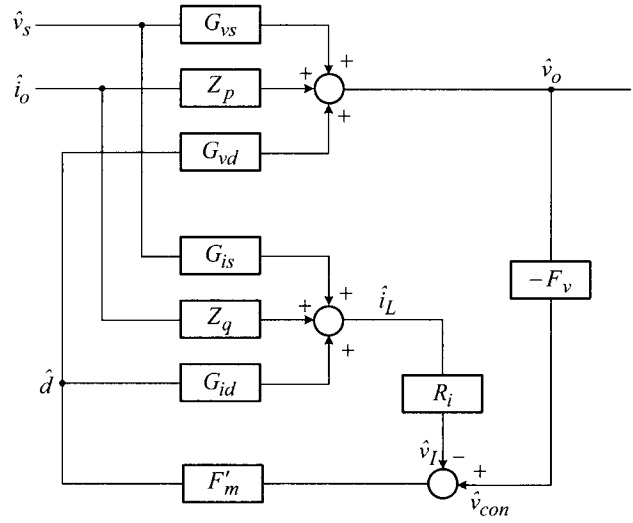


Figure 10.15 Small-signal block diagram representation of current-mode controlled PWM converters.

the expression (10.21) is rearranged as

$$F'_m = \frac{\hat{d}}{\hat{v}_{con} - \hat{i}_L} = \frac{2}{(S_n - S_f + 2S_e)T_s} \tag{10.23}$$

which can be fitted into Fig. 10.13 with the assumption $R_i = 1$.

In this derivation, it was also assumed that the slopes of the inductor current remain unchanged. The cases where this assumption is discarded will be discussed in the next chapter, which covers the sampling effects of current mode control.

Figure 10.15 shows the block diagram representation of the small-signal model. The block diagram is constructed by extending the small-signal model of voltage mode control, shown in Fig. 5.26. The block diagram clearly shows the two individual feedback loops, one originating from the output voltage $\hat{v}_o$ and the other stemming from the inductor current $\hat{i}_L$. The system is thus called a two-loop or multi-loop controlled system.

In addition to the three power stage gain blocks, $G_{vs}(s)$, $Z_p(s)$, and $G_{vd}(s)$, associated with the output voltage feedback, three additional gain blocks, $G_{is}(s)$, $Z_q(s)$, and $G_{id}(s)$, are necessary due to the presence of the inductor current feedback. The expressions for the six gain blocks of the three basic PWM converters are listed in Table 10.2. Now, the small-signal dynamics of current-mode controlled PWM converters are investigated using Fig. 10.15 and Table 10.2.

Table 10.2 Power Stage Transfer Functions of Three Basic Converters

Transfer functions		
$G_{vs}=K_{vs}\dfrac{1+\dfrac{s}{\omega_{esr}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$	$G_{vd}=K_{vd}\dfrac{\left(1-\dfrac{s}{\omega_{rhp}}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$	$G_{is}=K_{is}\dfrac{1+\dfrac{s}{\omega_{is}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$
$G_{id}=K_{id}\dfrac{1+\dfrac{s}{\omega_{id}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$	$Z_p=K_p\dfrac{\left(1+\dfrac{s}{\omega_z}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$	$Z_q=K_q\dfrac{1+\dfrac{s}{\omega_{esr}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}$

Expressions for dc gain and corner frequencies		
Buck converter	Boost converter	Buck/boost converter
$K_{vs}=D$	$1/(1-D)$	$D/(1-D)$
$K_{vd}=V_S$	$V_S/(1-D)^2$	$V_S/(1-D)^2$
$K_{is}=D/R$	$1/\left((1-D)^2R\right)$	$D/\left((1-D)^2R\right)$
$K_{id}=V_S/R$	$2V_S/\left((1-D)^3R\right)$	$V_S(1+D)/\left((1-D)^3R\right)$
$K_p=R_l$	$R_l/(1-D)^2$	$R_l/(1-D)^2$
$K_q=-1$	$-1/(1-D)$	$-1/(1-D)$
$\omega_{esr}=1/(CR_c)$	$1/(CR_c)$	$1/(CR_c)$
$\omega_{rhp}=\infty$	$(1-D)^2R/L$	$(1-D)^2R/(DL)$
$\omega_{is}=1/(CR)$	$1/(CR)$	$1/(CR)$
$\omega_{id}=1/(CR)$	$2/(CR)$	$(1+D)/(CR)$
$\omega_z=R_l/L$	R_l/L	R_l/L
$\omega_o=1/\sqrt{LC}$	$(1-D)/\sqrt{LC}$	$(1-D)/\sqrt{LC}$
$Q=R\sqrt{C/L}$	$(1-D)R\sqrt{C/L}$	$(1-D)R\sqrt{C/L}$

The expressions are approximations whose accuracy improves with the conditions $R \gg R_l$ and $R \gg R_c$.

10.2.2 Loop Gain Analysis

In current-mode controlled PWM converters, there exists two individual feedback loops: namely, one associated with the output voltage feedback and the other involved with the inductor current feedback. Furthermore, several different system loop gains can be defined by breaking the signal path at different locations in the system. These individual feedback loops and system loop gains should be first analyzed in order to characterize the small-signal dynamics of the two-loop controlled systems.

Individual Feedback Loops

From the small-signal block diagram in Fig. 10.15, two individual feedback loops are identified — the current loop and the voltage loop.

Current loop $T_i(s)$: The current loop $T_i(s)$ is the *negative* gain product of the signal path created by the inductor current feedback

$$T_i(s) = -\frac{\hat{i}_L(s)}{\hat{d}(s)}\frac{\hat{v}_I(s)}{\hat{i}_L(s)}\frac{\hat{d}(s)}{\hat{v}_I(s)} = G_{id}(s)\,R_i\,F_m' \tag{10.24}$$

Using the expressions in Table 10.2, the current loop $T_i(s)$ is determined as

$$\begin{aligned} T_i(s) &= \underbrace{K_{id}\frac{1+\dfrac{s}{\omega_{id}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}}_{G_{id}(s)} R_i\,F_m' \\ &= K_i\frac{1+\dfrac{s}{\omega_{id}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}} \end{aligned} \tag{10.25}$$

where

$$K_i = K_{id}\,R_i\,F_m' = K_{id}\,R_i\frac{2}{(S_n - S_f + 2S_e)T_s} \tag{10.26}$$

Figure 10.16 is the asymptotic plot for $|T_i|$. The structure and corner frequencies of $|T_i|$ are fixed by the power stage parameters and only the dc gain K_i can be altered by the CSN gain R_i and compensation ramp slope S_e. Equation (10.26) indicates that the dc gain K_i is inversely proportional to S_e. Thus, when S_e becomes larger, the magnitude of the current loop $|T_i|$ will be decreased, as illustrated in Fig. 10.16. This implies that, when the slope of the compensation ramp is overly increased, the control scheme practically reduces to voltage mode control, even though it has the structure of the peak current mode control.

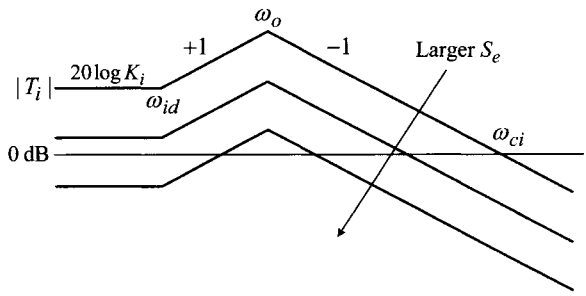


Figure 10.16 Asymptotic plot for $|T_i|$ and effects of compensation ramp slope.

Voltage loop $T_v(s)$: The negative gain product of the signal path associated with the output voltage feedback is referred to as the voltage loop $T_v(s)$

$$T_v(s) = -\frac{\hat{v}_o(s)}{\hat{d}(s)}\frac{\hat{v}_{con}(s)}{\hat{v}_o(s)}\frac{\hat{d}(s)}{\hat{v}_{con}(s)} = G_{vd}(s)\,F_v(s)\,F_m' \tag{10.27}$$

The voltage loop is directly affected by the voltage feedback compensation $F_v(s)$. Thus, the structure and parameters of $F_v(s)$ should be adequately determined in order to obtain desirable $T_v(s)$ characteristics.

Overall Loop Gain and Outer Loop Gain

For single-loop controlled systems, only one system loop gain exists in the system, as is the case with voltage mode control. In contrast, for multi-loop controlled systems, several system loop gains can be identified. Each system loop gain has its own implication and distinct role in the dynamic analysis and control design. For current-mode controlled PWM converters, two particular system loop gains are important and useful. Figure 10.17 illustrates these two system loop gains, which are called the overall loop gain and outer loop gain.

Overall Loop Gain $T_1(s)$: The first system loop gain is defined by breaking the signal path at Point A in Fig. 10.17(a). By applying Mason's gain rule to Fig. 10.17(a), this loop gain is expressed as

$$T_1(s) = -\frac{\hat{v}_y(s)}{\hat{v}_x(s)} = T_i(s) + T_v(s) \tag{10.28}$$

where $T_i(s)$ and $T_v(s)$ are defined in (10.24) and (10.27). This loop gain is called the overall loop gain because it is defined by breaking the signal path inside both the current loop and voltage loop.

Outer Loop Gain $T_2(s)$: The other system loop gain is defined at Point B in Fig. 10.17(b). Application of Mason's gain rule to Fig. 10.17(b) yields

$$T_2(s) = -\frac{\hat{v}_y'(s)}{\hat{v}_x'(s)} = \frac{T_v(s)}{1 + T_i(s)} \tag{10.29}$$

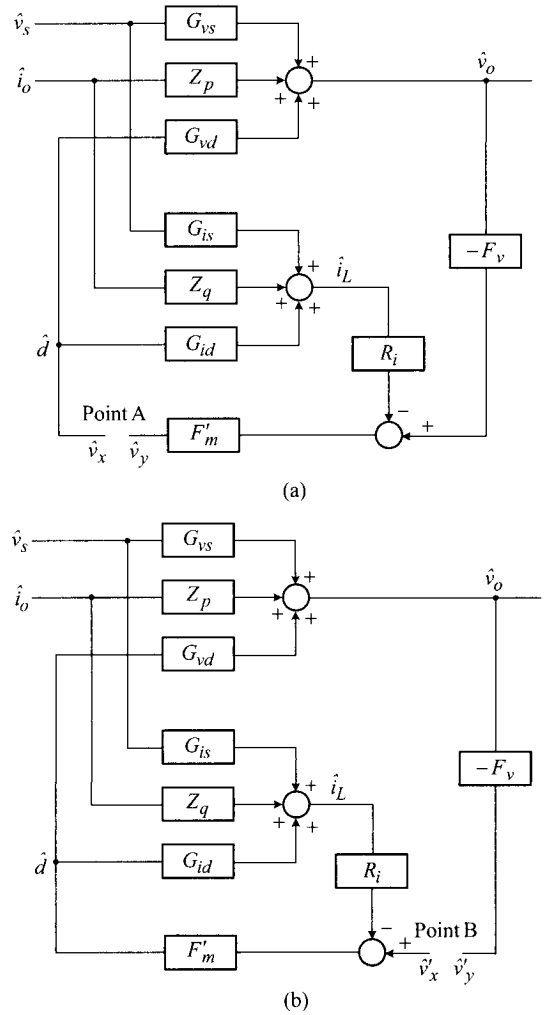


Figure 10.17 System loop gains. (a) Overall loop gain. (b) Outer loop gain.

This loop gain is denoted as the outer loop gain because the loop gain is defined at the outer voltage feedback path.

■ EXAMPLE 10.4 Mason's Gain Rule and System Loop Gains

This example shows the derivation of the system loop gain expressions using Mason's gain rule. Mason's gain rule is a general formula to find the expression

of a specific transfer function at the presence of multiple feedback loops

$$H(s) = \frac{1}{\Delta}\sum_{k=1}^{n} M_k\Delta_k \tag{10.30}$$

where

$H(s)$: transfer function of interest

Δ : 1 – (sum of the gains of all individual loops)
+ (sum of the gain products of all two non-touching loops) – $\cdots$

M_k : gain of the k^{th} forward path

Δ_k : 1 – (sum of the gains of all individual loops not touched by the k^{th} forward path) + (sum of the gain products of all two non-touching loop not touched by the k^{th} forward path) – $\cdots$

To evaluate the overall loop gain $T_1(s)$, Mason's rule is applied to Fig. 10.17(a), yielding $\Delta = 1, M_1 = G_{id}(s)R_iF'_m = T_i(s), \Delta_1=1, M_2 = G_{vd}(s)F_v(s)F'_m = T_v(s)$, and $\Delta_2 = 1$. The overall loop gain is now given by

$$T_1 = \frac{1}{\Delta}(M_1\Delta_1 + M_2\Delta_2) = T_i(s) + T_v(s)$$

Similarly, by applying Mason's rule to Fig. 10.17(b), it becomes that $\Delta = 1 + G_{id}(s)R_iF'_m = 1 + T_i(s)$, $M_1 = G_{vd}(s)F_v(s)F'_m = T_v(s)$, and $\Delta_1 = 1$. Thus, the outer loop gain is resulted as

$$T_2 = \frac{1}{\Delta}M_1\Delta_1 = \frac{T_v(s)}{1 + T_i(s)}$$

10.2.3 Stability Analysis

For voltage mode control, stability analysis was performed using the single loop gain present in the system. In contrast, for current mode control, the overall loop gain and outer loop gain are both necessary and useful in determining the absolute stability and relative stability of the converter.

Absolute Stability

As discussed in Section 7.5, the absolute stability can be assessed using any closed-loop transfer function because all transfer functions have the same denominator. The closed-loop input-to-output transfer function, or audio-susceptibility, is derived by applying Mason's gain rule to the small-signal block diagram of Fig. 10.15.

$$A_u(s) = \frac{\hat{v}_o(s)}{\hat{v}_s(s)} = \frac{G_{vs}(1 + G_{id}R_iF'_m) - G_{is}R_iF'_mG_{vd}}{1 + G_{id}R_iF'_m + G_{vd}F_vF'_m} = \frac{F_p(s)}{1 + T_i(s) + T_v(s)} \tag{10.31}$$

with $F_p(s) = G_{vs}(1 + G_{id}R_iF'_m) - G_{is}R_iF'_mG_{vd}$.

It can be shown that the numerator of the above equation, $F_p(s)$, does not contain any right-half plane (RHP) poles. Thus, the absolute stability is judged by the existence of any RHP roots in the following equation

$$1 + T_i(s) + T_v(s) = 0 \tag{10.32}$$

which is recognized as

$$1 + T_1(s) = 0 \tag{10.33}$$

Equation (10.32) is written in an alternative form

$$1 + \frac{T_v(s)}{1 + T_i(s)} = 0 \tag{10.34}$$

which becomes

$$1 + T_2(s) = 0 \tag{10.35}$$

This analysis implies that the Nyquist criterion can be applied to either $T_1(s)$ or $T_2(s)$, in order to check the existence of any RHP roots in $1 + T_i(s) + T_v(s) = 0$. The result, of course, should be the same regardless of the choice of the loop gain; if one loop gain predicts stability or instability, the other loop gain should indicate the same.

■ EXAMPLE 10.5 Absolute Stability and Polar Plots of $T_1(s)$ and $T_2(s)$

This example demonstrates that the overall loop gain and outer loop gain carry the same information about the absolute stability of the converter. Figure 10.18 shows the polar plots of $T_1(s)$ and $T_2(s)$ of a current-mode controlled boost converter. With a stable operating point, the polar plots of the two loop gains both do not encircle the $(-1, 0)$ point to confirm stability of the converter, as shown in Fig. 10.18(a). Now, the operating point is altered so that the converter becomes marginally stable. As shown in Fig. 10.18(b), both the polar plots identically traverse the $(-1, 0)$ point, thus indicating that the converter is on the verge of instability. Figure 10.18(c) is the polar plots when the operating point is further changed to encounter instability. For this case, the two loop gains encircle the $(-1, 0)$ point as the token of instability. Although the shape and transition pattern are utterly different, the two loop gains exhibit the same information about the absolute stability of the converter.

Relative Stability

Although the overall loop gain and outer loop gain provide the same information about the absolute stability, they are different s-domain transfer functions. Therefore, the frequency responses of the two loop gains are distinct in both the shape and evolution pattern, thereby producing different phase and gain margins. The stability margins thus should be interpreted based on their original definitions. The frequency response

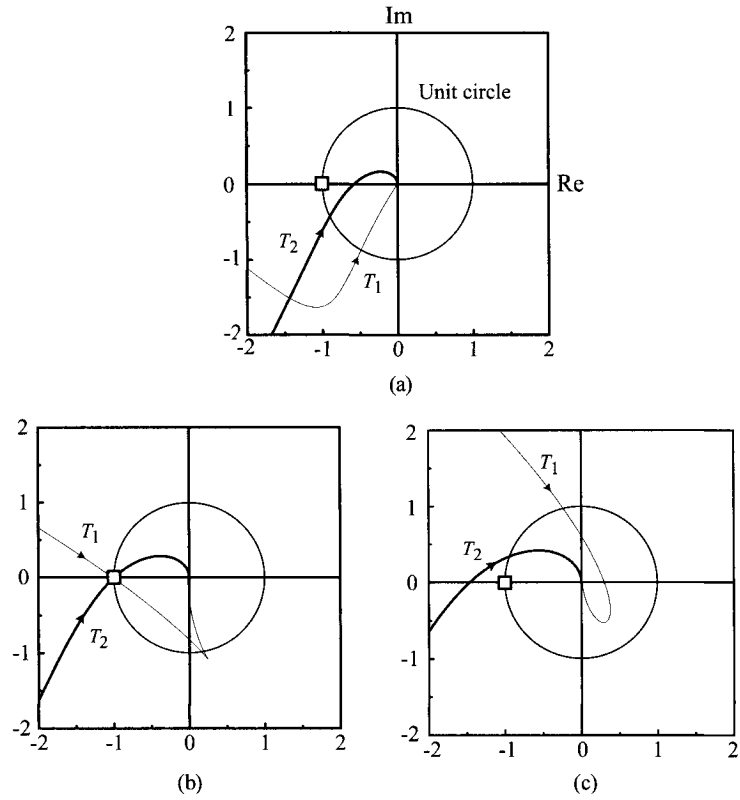


Figure 10.18 Overall loop gain T_1 and outer loop gain T_2. (a) Stable case. (b) Marginally stable case. (c) Unstable case.

of the overall loop gain, $T_1(s) = T_i(s) + T_v(s)$, is expressed as

$$T_1(j\omega) = |T_i(j\omega) + T_v(j\omega)|\angle\big(T_1(j\omega) + T_v(j\omega)\big) \tag{10.36}$$

According to the definitions in Section 7.6, the gain margin is the extra gain that can be added to $|T_i + T_v|$ before the system becomes unstable. For example, if $T_1(s)$ has a 6 dB gain margin, the system remains stable until $|T_v + T_i|$ is doubled: $20 \log 2 \approx 6$ dB. Similarly, the phase margin is the additional delay that can be put in $\angle(T_i + T_v)$ while maintaining stability.

The frequency response of the outer loop gain $T_2(s) = T_v(s)/(1 + T_i(s))$ is given by

$$T_2(j\omega) = \left|\frac{T_v(j\omega)}{1 + T_i(j\omega)}\right| \angle\left(\frac{T_v(j\omega)}{1 + T_i(j\omega)}\right) \tag{10.37}$$

The gain margin and phase margin of T_2 can be interpreted in the same manner. For example, the gain margin is the additional gain increase that can be introduced

to $|T_v/(1 + T_i)|$. However, the stability margins become far more informative and useful when $T_i(s)$ is fixed prior to analyzing $T_2(s)$. For such a case, the stability margins of $T_2(s) = T_v(s)/(1 + T_i(s))$ are, in fact, those of $T_v(s)$. As will be shown in the upcoming control design procedures, $T_i(s)$ is indeed prefixed and $T_v(s)$ is later designed for the optimal $T_2(s)$ characteristics. Accordingly, the phase margin and gain margin of $T_2(s)$ can be used to assist and evaluate the design of the voltage loop $T_v(s)$. Further details about this topic are given later in Section 10.4.2.

10.2.4 Voltage Feedback Compensation

As shown in the previous section, the structure of the current loop $T_i(s)$ is fixed by the power stage transfer functions. On the other hand, the structure of the voltage loop gain $T_v(s)$ can freely be chosen by altering the voltage feedback compensation, $F_v(s)$. Accordingly, $F_v(s)$ needs to be designed for the desired $T_v(s)$ structure.

This section investigates the design of $F_v(s)$ that would offer stability and good closed-loop performance. For simplicity, a buck converter is used in this section. The conclusion of this section will be extended for boost and buck/boost converters in the next section.

Instability with Single Integrator

In order to obtain insight about the $F_v(s)$ design, it is first necessary to investigate the current loop $T_i(s)$ and voltage loop $T_v(s)$.

For the buck converter, the expression for the current loop $T_i(s)$ is given by

$$\begin{aligned} T_i(s) &= G_{id}(s)\, R_i\, F_m' \\ &= \underbrace{\frac{V_S}{R}\, \frac{1 + \dfrac{s}{\omega_{id}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}}}_{G_{id}(s)} R_i F_m' \end{aligned} \tag{10.38}$$

with $\omega_{id} = 1/(CR)$. As previously addressed, the structure of the voltage loop gain is determined by $G_{id}(s)$.

Unlike the $T_i(s)$ case, the expression for the voltage loop $T_v(s)$ is directly affected by the selection of the voltage feedback compensation $F_v(s)$. As the first candidate for $F_v(s)$, a single integrator is considered. With $F_v(s) = K_v/s$, the voltage loop $T_v(s)$ becomes

$$\begin{aligned} T_v(s) &= G_{vd}(s) F_v(s) F_m' \\ &= \underbrace{V_S\, \frac{1 + \dfrac{s}{\omega_{esr}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}}}_{G_{vd}(s)} \underbrace{\frac{K_v}{s}}_{F_v(s)} F_m' \end{aligned} \tag{10.39}$$

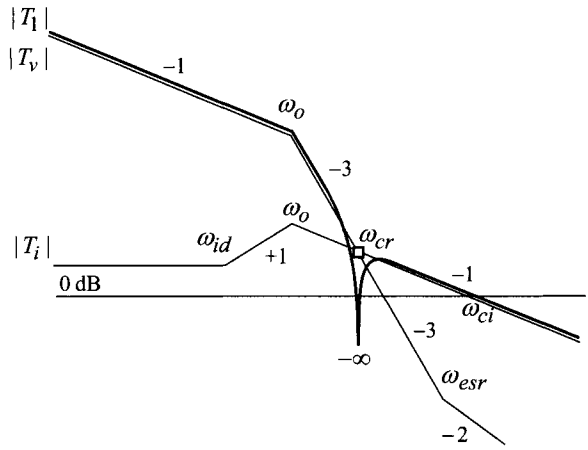


Figure 10.19 Individual feedback loops and overall loop gain with single integrator.

The correctness of the $F_v(s)$ selection can be judged by investigating the overall loop gain $T_1(s) = T_i(s) + T_v(s)$. The magnitude plot of the overall loop gain $|T_1| = |T_i + T_v|$ is depicted in Fig. 10.19, along with the asymptotic plots of $|T_i|$ and $|T_v|$. The asymptotic plot for $|T_1|$ is determined as explained below. Based on the asymptotic analysis, it follows that

$$T_1(s) = T_i(s) + T_v(s)$$

$$\approx \begin{cases} T_i(s) & \text{at frequencies where } |T_i| \gg |T_v| \\ T_v(s) & \text{at frequencies where } |T_i| \ll |T_v| \end{cases} \tag{10.40}$$

Thus, $|T_1|$ follows either $|T_i|$ or $|T_v|$ whichever is larger in magnitude at the given frequencies. However, there is one singular point which could utterly depart from this general trend. At the frequency where $|T_i| = |T_v|$, denoted as ω_{cr} in Fig. 10.19, T_1 is given by the sum of two equal-length vectors, $\vec{T}_1 = \vec{T}_i + \vec{T}_v$. In this case, the magnitude of T_1 is strongly affected by the phase characteristics of $\vec{T}_i$ and $\vec{T}_v$. The slopes of $|T_i|$ and $|T_v|$ indicate that $\angle T_i \approx -90°$ and $\angle T_v \approx -270° = 90°$ at ω_{cr}. Now, the magnitude of T_1 at ω_{cr} becomes infinitely small, because $\vec{T}_i$ and $\vec{T}_v$ are 180° apart and therefore cancel each other. The sudden collapse in magnitude in turn implies an abrupt decrease in phase. Thus, $|T_1|$ prematurely crosses the 0 dB line with the phase far less than −180°; in short, the converter is unstable.

■ EXAMPLE 10.6 Instability with Single Integrator

This example demonstrates the instability of a single integrator. Figure 10.20 shows the Bode plots of $T_i(s)$, $T_v(s)$, and $T_1(s)$ of a buck converter which

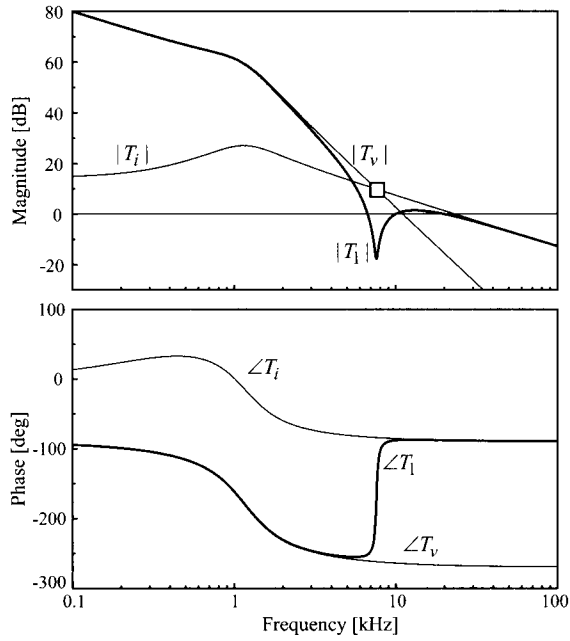


Figure 10.20 Examples of individual feedback loops and overall loop gain.

employs a single integrator. The overall loop gain exhibits the dip in $|T_1|$ and sudden drop in $\angle T_1$ at the frequencies where $|T_i| \approx |T_v|$. The converter is surely unstable with these loop gain characteristics.

Two-Pole One-Zero Compensation

As the second candidate for the voltage feedback compensation, a two-pole one-zero circuit

$$F_v(s) = \frac{K_v\left(1 + \dfrac{s}{\omega_{zc}}\right)}{s\left(1 + \dfrac{s}{\omega_{pc}}\right)} \tag{10.41}$$

is now considered. For this case, the voltage loop $T_v(s)$ becomes

$$\begin{aligned} T_v(s) &= G_{vd}(s)F_v(s)F'_m \\ &= \underbrace{V_S \frac{1 + \dfrac{s}{\omega_{esr}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}}}_{G_{vd}(s)} \underbrace{\frac{K_v\left(1 + \dfrac{s}{\omega_{zc}}\right)}{s\left(1 + \dfrac{s}{\omega_{pc}}\right)}}_{F_v(s)} F'_m \end{aligned} \tag{10.42}$$

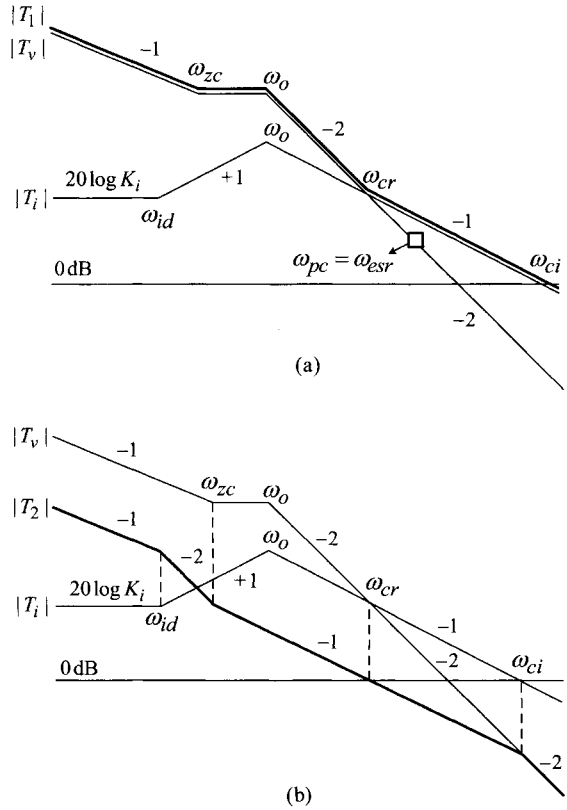


Figure 10.21 System loop gains. (a) Overall loop gain T_1. (b) Outer loop gain T_2.

Figure 10.21(a) shows the asymptotic plots for $|T_i|$, $|T_v|$, and $|T_1|$. The asymptotic plot of $|T_v|$ indicates that the compensation pole ω_{pc} is placed at the esr zero, $\omega_{pc} = \omega_{esr}$, and the compensation zero ω_{zc} is located before the power stage double pole ω_o: $\omega_{zc} < \omega_o$. Justifications for these selections will be given shortly. Due to a 90° phase boost by ω_{zc}, $\angle T_v$ approaches −180° at the frequency where $|T_i| = |T_v|$. The difference between $\angle T_i$ and $\angle T_v$ is 90°, and the magnitude of the overall loop gain now becomes $|T_1| = \sqrt{2}\,|T_i| = \sqrt{2}\,|T_v|$ without showing any eccentric behavior. Thus, the two-pole one-zero circuit is well suited for the voltage feedback compensation. As will be confirmed in the forthcoming discussions, the two-pole one-zero compensation is indeed the optimal structure for $T_v(s)$, which can be adopted to all the three basic PWM converters.

The asymptotic plot of the overall loop gain $|T_1|$ shows the design strategy for the peak current mode control. At low frequencies, the voltage loop should be large in magnitude for a tight output regulation and good closed-loop performance, as is the case with voltage mode control. The compensation zero ω_{zc} should be placed

before the power stage double pole ω_o for the following reason. As demonstrated in Section 8.4.2, the system becomes a conditionally stable system if ω_o comes prior to ω_{zc}, which could encounter stability problems during transition periods in which the output of the feedback controller remains in saturation. To avoid this problem, ω_{zc} should appear before ω_o.

At high frequencies, the current loop should prevail over the voltage loop, $|T_i| \gg |T_v|$ so that $T_1(s) = T_i(s) + T_v(s) \approx T_i(s)$. The current loop $T_i(s)$ is inherently stable with a -20 dB/dec high frequency asymptote and 90° final phase. Thus, the dominance of $T_i(s)$ at high frequencies insures stability for $T_1(s)$. In fact, the crossover frequency and phase margin of $T_i(s)$ become those of the overall loop gain $T_1(s)$ if the $|T_i| \gg |T_v|$ condition is met at high frequencies.

Outer Loop Gain

The outer loop gain defined in (10.29) is now analyzed using the asymptotic method introduced in Section 8.1

$$T_2(s) = \frac{T_v(s)}{1 + T_i(s)} \approx \begin{cases} \dfrac{T_v(s)}{T_i(s)} & \text{at frequencies where } |T_i| \gg 1 \\ T_v(s) & \text{at frequencies where } |T_i| \ll 1 \end{cases} \tag{10.43}$$

Figure 10.21(b) shows the asymptotic plot for $|T_i|$, $|T_v|$, and $|T_2|$. The asymptotic plot for $|T_2|$ is constructed based on (10.43). At the frequencies beyond $|T_i|$ crossover frequency ω_{ci}, $|T_2|$ tracks $|T_v|$. At frequencies lower than ω_{ci}, $|T_2|$ follows the line segments that are created from the asymptote sketch rules given in Table 8.1 in Chapter 8: $|T_2| = |T_v| - |T_i|$.

The outer loop gain $|T_2|$ is very different from the overall loop gain $|T_1|$ in structure, magnitude, and crossover frequency. Features of $|T_2|$ are summarized below.

1) The second-order power stage dynamics do not appear in $|T_2|$. The second-order dynamics, commonly appearing in both $T_i(s)$ and $T_v(s)$, are canceled in $T_2(s) \approx T_v(s)/T_i(s)$ and the loop gain shows the -20 dB/dec slope for a wide frequency range.

2) The magnitude of $|T_2|$ is substantially smaller than the magnitude of $|T_1|$: that is, $|T_2| \approx |T_v/T_i| \ll |T_1| = |T_i + T_v|$.

3) The crossover frequency of $|T_2|$ is much lower than that of $|T_1|$. In fact, $|T_2|$ crossover occurs at the frequency where $|T_v| = |T_i|$; namely, the condition $|T_v| = |T_i|$ indicates $|T_2| = |T_v|/|T_i| = 1 = 0$ dB. This frequency was previously denoted as ω_{cr}.

4) The outer loop gain has a high-frequency pole at the $|T_i|$ crossover frequency, denoted as ω_{ci} in Fig. 10.21(b). For sufficient phase margin, the $|T_2|$ crossover frequency ω_{cr} should appear well before the high-frequency pole ω_{ci}: $\omega_{cr} \ll \omega_{ci}$.

Loop Gain Characteristics

For current mode control, two system loop gains are defined at the different locations in the system. These two loop gains collectively provide useful information about the internal structure of the feedback controller, however, the informational contents of the two loop gains are very different. Thus, the roles of the two loop gains in the dynamic analysis and control design are distinct and unique. This situation is in sharp contrast to the case of voltage mode control, where only one system loop gain exists. For voltage mode control, connections between the loop gain and closed-loop performance are direct and explicit. Thus, the loop gain analysis is straightforward for this case.

For current mode control, the loop gain analysis is rather involved because the connections between the loop gains and closed-loop performance are indirect and implicit. Furthermore, the contributions of the two loop gains to the control design are very different. Details about the dynamic analysis and control design using the two loop gains are given in the next section.

Readers may be tempted to compare the loop gain characteristics of current mode control with those of voltage mode control. In that case, the comparison must be done with care, because a direct comparison between the loop gains of voltage mode control and current mode control does not provide consistent information about the performance of the converter or correctness of the control design. Indeed, the loop gain of voltage mode control usually *seems* superior to the outer loop gain of current mode control. However, this does not imply that voltage mode control outperforms current mode control, but does indicate that the outward message of the two loop gains should be interpreted differently and carefully in consideration of their connections to the closed-loop performance of the respective converter system.

10.2.5 Control Design Procedures

Based on the previous loop gain analysis, step-by-step design procedures for the peak current mode control are established. The design procedures are discussed in a general manner so that the results can be applied for all the three basic PWM converters. As the first step, the current loop $T_i(s)$ is designed to offer good high-frequency characteristics for the overall loop gain $T_1(s)$. The second step is to design the voltage loop $T_v(s)$ for desirable properties of the outer loop gain $T_2(s)$.

Current Loop Design

The general expression for the current loop is given by

$$\begin{aligned} T_i(s) &= G_{id}(s)R_iF'_m \\ &= \underbrace{K_{id}\frac{1+\dfrac{s}{\omega_{id}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}}_{G_{id}(s)} R_iF'_m = K_i\frac{1+\dfrac{s}{\omega_{id}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}} \end{aligned} \tag{10.44}$$

where

$$K_i = K_{id} R_i F'_m \tag{10.45}$$

The current loop $T_i(s)$ should dictate the overall loop $T_1(s)$ at high frequencies. This design objective is simply achieved by placing the 0 dB crossover frequency of $T_i(s)$ at higher frequencies. *The crossover frequency of $T_i(s)$ can be increased up to the frequencies where the validity and accuracy of the small-signal analysis are not severely impaired, typically 15–30% of the switching frequency.* Readers may refer to Example 8.4 in Chapter 8 for the background of this statement. As will be demonstrated in the next chapter, this design strategy also prevents or minimizes the detrimental effects originated from the sampling effects of current mode control.

Once the $T_i(s)$ crossover frequency, denoted as ω_{ci} in Fig. 10.21, is selected, the current loop design proceeds based on the $T_i(s)$ expression in (10.44).

1) Determine the dc gain of the current loop so that the $T_i(s)$ crossover frequency occurs at the desired frequency. It is recommended to place the crossover frequency at 15–30% of the switching frequency. From the asymptotic plot of $|T_i|$ in Fig. 10.21, the following relationship can be seen

$$20\log K_i + 20\log\left(\frac{\omega_o}{\omega_{id}}\right) - 20\log\left(\frac{\omega_{ci}}{\omega_o}\right) = 0 \text{ dB} \tag{10.46}$$

where K_i is the dc gain of the current loop and ω_{ci} is the desired location for the $T_i(s)$ crossover frequency. The preceding equation is converted into the design equation

$$K_i\left(\frac{\omega_o}{\omega_{id}}\right)\left(\frac{\omega_o}{\omega_{ci}}\right) = 1 \quad \Rightarrow \quad K_i = \frac{\omega_{id}\,\omega_{ci}}{\omega_o^2} \tag{10.47}$$

which can be used to determine the required K_i for the preselected ω_{ci}.

2) Determine the CSN gain R_i considering hardware constraints. The product of the peak inductor current $i_{L\,peak}$ and CSN gain R_i should fall in the allowable voltage range for the PWM block: $i_{L\,peak} R_i < V_{max}$ where V_{max} is the maximum allowable input voltage for the PWM block.

3) Determine the modulator gain F'_m using the relationship

$$K_i = K_{id} R_i F'_m \quad \Rightarrow \quad F'_m = \frac{K_i}{K_{id} R_i} \tag{10.48}$$

where K_{id} is given in Table 10.2. Once the modulator gain is fixed, the slope of the compensation ramp S_e is determined from

$$F'_m = \frac{2}{(S_n - S_f + 2S_e)T_s} \quad \Rightarrow \quad S_e = \frac{1}{T_s F'_m} + \frac{S_f - S_n}{2} \tag{10.49}$$

This design procedure places the $T_i(s)$ crossover frequency at the desired frequency. The $T_i(s)$ crossover frequency is the same as the crossover frequency of the overall loop gain $T_1(s) = T_i(s) + T_v(s)$, due to the condition $|T_i| \gg |T_v|$ at high frequencies.

Voltage Loop Design

The general expression for the voltage loop is given by

$$\begin{aligned} T_v(s) &= G_{vd}(s)F_v(s)F'_m \\ &= \underbrace{K_{vd}\frac{\left(1-\dfrac{s}{\omega_{rhp}}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}}_{G_{vd}(s)} F_v(s)F'_m \end{aligned} \tag{10.50}$$

For buck converters, the RHP zero does not exist so $\omega_{rhp} = \infty$ in (10.50). The voltage loop should prevail over the current loop at low frequencies. For this purpose, the two-pole one-zero circuit is employed for the voltage feedback compensation

$$F_v(s) = \frac{K_v\left(1+\dfrac{s}{\omega_{zc}}\right)}{s\left(1+\dfrac{s}{\omega_{pc}}\right)} \tag{10.51}$$

The voltage loop $T_v(s)$ then becomes

$$T_v(s) = \underbrace{K_{vd}\frac{\left(1-\dfrac{s}{\omega_{rhp}}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}}_{G_{vd}(s)} \underbrace{\frac{K_v\left(1+\dfrac{s}{\omega_{zc}}\right)}{s\left(1+\dfrac{s}{\omega_{pc}}\right)}}_{F_v(s)} F'_m \tag{10.52}$$

Referring to the asymptotic plots of the system loop gains in Fig. 10.21, the selection of the compensation parameters is explained below.

1) Place the compensation pole ω_{pc} at the lowest frequency among the RHP zero, esr zero, and half the switching frequency: $\omega_{pc} = \min\{\omega_{rhp}\ \omega_{esr}\ 0.5\,\omega_s\}$. The compensation pole ω_{pc} cancels ω_{rhp} or ω_{esr} whichever comes first, and $T_v(s)$ thus maintains -40 dB/dec roll-off at high frequencies. This design step is necessary to ensure the dominance of the current loop at high frequencies.

2) Place the compensation zero ω_{zc} before the power stage double pole ω_o, in order to provide a 90° phase boost without becoming a conditionally stable system. As will be shown later, the position of ω_{zc} determines the speed of transient responses. For faster response, ω_{zc} should be placed at higher frequencies, yet still not exceed the power stage double pole. As a rule of thumb, it is recommended $\omega_{zc} = (0.6-0.8)\,\omega_o$.

3) Adjust the integrator gain K_v for design trade-off. At this stage, the current loop $T_i(s)$ is fixed and the locations of the compensation pole and zero in

$F_v(s)$ are determined. Now, the integrator gain K_v is the only undecided design parameter. By changing K_v, the magnitude of the outer loop gain, $|T_2| = |T_v|/|1 + T_i|$, can be raised or lowered; in other words, K_v controls the $T_2(s)$ crossover frequency, ω_{cr}. For design purposes, the position of ω_{cr} is first selected and the integrator gain K_v is determined later.

- For buck converters, ω_{cr} can be positioned at high frequencies, approaching the esr zero: $\omega_{cr} = (0.3-1.0)\,\omega_{esr}$.
- For boost and buck/boost converters, ω_{cr} should be selected at sufficiently lower frequencies than the RHP zero: $\omega_{cr} = (0.1-0.3)\,\omega_{rhp}$.

Discussions about the selection of ω_{cr} will be given in Sections 10.3.3 and 10.4.1. Once the $T_2(s)$ crossover frequency, ω_{cr}, is chosen, the integrator gain K_v is determined from the design equation

$$\frac{K_{vd}K_v}{K_{id}R_i\,\omega_{id}}\left(\frac{\omega_{id}}{\omega_{zc}}\right)^2\frac{\omega_{zc}}{\omega_{cr}} = 1 \quad \Rightarrow \quad K_v = \frac{K_{id}\,\omega_{cr}\,R_i\,\omega_{zc}}{\omega_{id}\,K_{vd}} \tag{10.53}$$

Derivation of (10.53) is explained in Example 10.7.

4) Check the phase margin of $T_2(s)$ and tune the integrator gain K_v to secure a $45°-70°$ phase margin.

■ EXAMPLE 10.7 Design Equation for $T_2(s)$

This example shows the derivation of the design equation of $T_2(s)$ given in (10.53). Referring to Fig. 10.21(b), the magnitude of $T_2(s)$ at ω_{id} is given by

$$\begin{aligned} |T_2(j\omega_{id})| &= \left|\frac{T_v(j\omega_{id})}{T_i(j\omega_{id})}\right| \\ &= 20\log\left(\frac{K_{vd}\dfrac{K_v}{\omega_{id}}F'_m}{K_{id}\,R_i\,F'_m}\right) = 20\log\left(\frac{K_{vd}\,K_v}{K_{id}\,R_i\,\omega_{id}}\right) \end{aligned} \tag{10.54}$$

Figure 10.21(b) also indicates that

$$20\log\frac{K_{vd}K_v}{K_{id}R_i\,\omega_{id}} - 40\log\frac{\omega_{zc}}{\omega_{id}} - 20\log\frac{\omega_{cr}}{\omega_{zc}} = 0\ \text{dB} \tag{10.55}$$

which transforms to (10.53) in the linear scale.

Circuit for Two-Pole One-Zero Compensation

Figure 10.22 shows the circuit implementation of the two-pole one-zero compensation. The resistance R_x is used to control the magnitude of the output voltage:

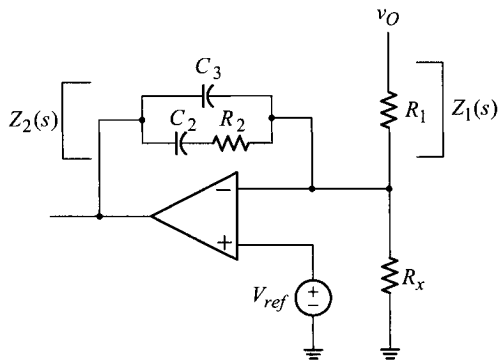


Figure 10.22 Circuit implementation of two-pole one-zero compensation.

$V_O = V_{ref}(1 + R_1/R_x)$. If R_x is not used, the output voltage is regulated at the reference voltage: $V_O = V_{ref}$ with $R_x = \infty$. This resistance is irrelevant to the voltage feedback compensation. Direct circuit analysis shows that

$$F_v(s) = \frac{Z_2(s)}{Z_1(s)} = \frac{K_v\left(1 + \dfrac{s}{\omega_{zc}}\right)}{s\left(1 + \dfrac{s}{\omega_{pc}}\right)} \tag{10.56}$$

$$\begin{aligned} K_v &= \frac{1}{R_1(C_2 + C_3)} \\ \omega_{zc} &= \frac{1}{R_2C_2} \\ \omega_{pc} &= \frac{1}{R_2\left(\dfrac{C_2C_3}{C_2 + C_3}\right)} \end{aligned} \tag{10.57}$$

Once the compensation parameters are selected, the circuit components in Fig. 10.22 are determined using the above equations. Among the four circuit components, one can arbitrarily be chosen and the other components are found using the equations (10.57). The design procedures developed in this section are summarized in Table 10.3 for easy reference.

Table 10.3 Design Procedures for Peak Current Mode Control

Current loop design

$$T_i(s) = \underbrace{K_{id}\frac{1+\dfrac{s}{\omega_{id}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}}_{G_{id}(s)} R_i F'_m = K_i \frac{1+\dfrac{s}{\omega_{id}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}} \quad \text{with } K_i = K_{id} R_i F'_m$$

1) Select $T_i(s)$ crossover frequency: $\omega_{ci} = (0.15 - 0.3)\,\omega_s$.
2) Evaluate the dc gain: $K_i = (\omega_{id}\,\omega_{ci})/\omega_o^2$ with $K_i = K_{id}R_iF'_m$.
3) Select the CSN gain R_i such that $i_{L\,peak}R_i < V_{max}$ where V_{max} is the maximum input voltage for the PWM block.
4) Evaluate the modulator gain: $F'_m = K_i/(K_{id}R_i)$.
5) Evaluate the compensation ramp slope: $S_e = 1/(T_sF'_m) + (S_f - S_n)/2$.

Voltage loop design

$$T_v(s) = \underbrace{K_{vd}\frac{\left(1-\dfrac{s}{\omega_{rhp}}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}}}_{G_{vd}(s)} \underbrace{\frac{K_v\left(1+\dfrac{s}{\omega_{zc}}\right)}{s\left(1+\dfrac{s}{\omega_{pc}}\right)}}_{F_v(s)} F'_m$$

1) Set the compensation pole: $\omega_{pc} = \min\{\omega_{rhp}\ \omega_{esr}\ 0.5\,\omega_s\}$.
2) Select the compensation zero: $\omega_{zc} = (0.6 - 0.8)\,\omega_o$.
3) Set $T_2(s)$ crossover frequency:

   $\omega_{cr} = (0.3 - 1.0)\,\omega_{esr}$ for buck converter, and

   $\omega_{cr} = (0.1 - 0.3)\,\omega_{rhp}$ for boost or buck/boost converter.
4) Evaluate the integrator gain: $K_v = (K_{id}\,\omega_{cr}\,R_i\,\omega_{zc})/(\omega_{id}\,K_{vd})$.
5) Check the $T_2(s)$ phase margin and adjust K_v for a $45° - 70°$ phase margin.
6) Evaluate the circuit components for voltage feedback compensation using (10.57).

For buck converters, ω_{rhp} does not exist so $\omega_{rhp} = \infty$.

■ EXAMPLE 10.8 Buck Converter Design and Performance Evaluation

This example illustrates the control design and closed-loop performance of the peak current mode control adapted to a buck converter. Figure 10.23 shows the circuit diagram of the buck converter. The converter regulates the output voltage at 4 V using the two-pole one-zero compensation. From the power stage circuit parameters, the corner frequencies and dc gains of power stage transfer functions are determined as

$$\omega_o = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{40 \times 10^{-6}\, 470 \times 10^{-6}}} = 2\pi \cdot 1.16 \times 10^3 \text{ rad/s}$$

$$\omega_{esr} = \frac{1}{CR_c} = \frac{1}{470 \times 10^{-6}\, 0.1} = 2\pi \cdot 3.39 \times 10^3 \text{ rad/s}$$

$$K_{vd} = V_s = 16$$

$$\omega_{id} = \frac{1}{CR} = \frac{1}{470 \times 10^{-6}\, 1} = 2\pi \cdot 339 \text{ rad/s}$$

$$K_{id} = \frac{V_S}{R} = \frac{16}{1} = 16$$

The switching frequency is $\omega_s = 2\pi \cdot 50 \times 10^3$ rad/s. The maximum input voltage for the PWM block is assumed as $V_{max} = 5.0$ V and the peak value of the inductor current is calculated as

$$\begin{aligned} i_{L\,peak} &= \frac{V_O}{R} + \frac{1}{2}\frac{V_S - V_O}{L} DT_s \\ &= \frac{4}{1} + \frac{1}{2}\frac{16-4}{40 \times 10^{-6}} 0.25 \cdot 20 \times 10^{-6} = 4.75 \text{ A} \end{aligned}$$

Based on the proposed design procedures, the control design is performed as follows.

Current Loop Design

1) $T_i(s)$ crossover frequency: $\omega_{ci} = 0.2\,\omega_s = 0.2\,(2\pi \cdot 50 \times 10^3) = 2\pi \cdot 10 \times 10^3$ rad/s

2) Dc gain of T_i:

$$K_i = \frac{\omega_{id}\,\omega_{ci}}{\omega_o^2} = \frac{(2\pi \cdot 339)(2\pi \cdot 10 \times 10^3)}{(2\pi \cdot 1.16 \times 10^3)^2} = 2.52$$

3) CSN gain:

$$R_i < \frac{V_{max}}{i_{L\,peak}} = \frac{5.0}{4.75} = 1.05 \quad \Rightarrow R_i = 0.67$$

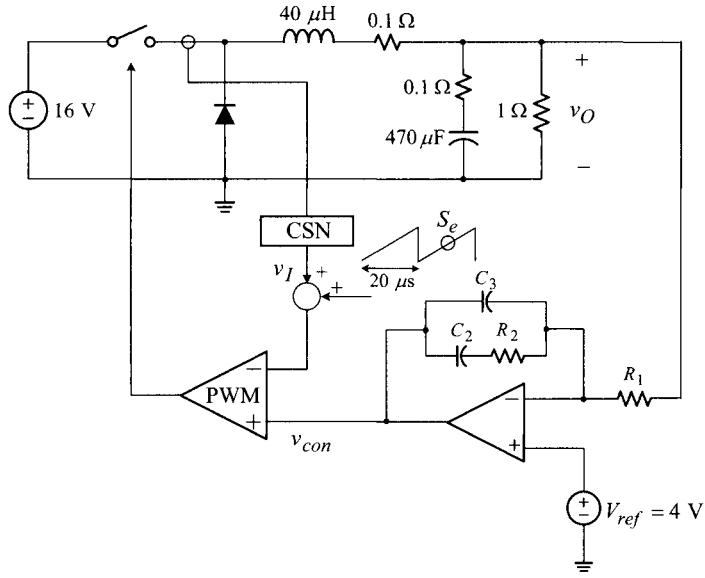


Figure 10.23 Current-mode controlled buck converter: $R_i = 0.67$, $S_e = 1.46 \times 10^5$ V/s, $R_1 = 10$ kΩ, $R_2 = 92.3$ kΩ, $C_2 = 1.86$ nF, and $C_3 = 0.70$ nF.

4) Modulator gain:

$$F'_m = \frac{K_i}{K_{id} R_i} = \frac{2.52}{16 \cdot 0.67} = 0.235$$

5) Compensation ramp:

$$\begin{aligned} S_e &= \frac{1}{T_s F'_m} + \frac{S_f - S_n}{2} \\ &= \frac{1}{20 \times 10^{-6}\, 0.235} + \frac{\dfrac{4}{40 \times 10^{-6}} 0.67 - \dfrac{16 - 4}{40 \times 10^{-6}} 0.67}{2} \\ &= 1.46 \times 10^5 \text{ V/s} \\ V_m &= S_e T_s = (1.46 \times 10^5)(20 \times 10^{-6}) = 2.92 \text{ V} \end{aligned}$$

Voltage Loop Design

1) Compensation pole: $\omega_{pc} = \omega_{esr} = 2\pi \cdot 3.39 \times 10^3$ rad/s

2) Compensation zero: $\omega_{zc} = 0.8\,\omega_o = 0.8\,(2\pi \cdot 1.16 \times 10^3) = 2\pi \cdot 928$ rad/s

3) $T_2(s)$ crossover frequency: $\omega_{cr} = \omega_{esr} = 2\pi \cdot 3.39 \times 10^3$ rad/s

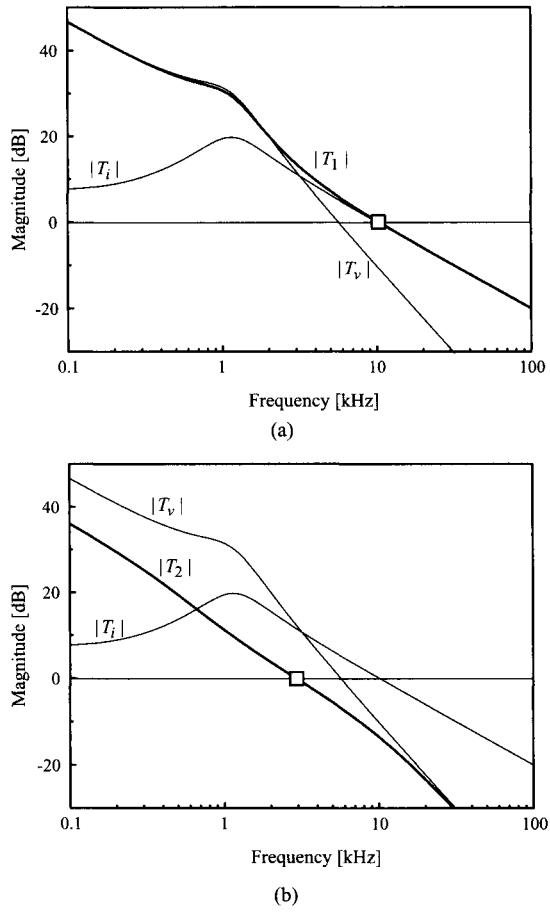


Figure 10.24 Individual feedback loops and system loop gains. (a) Overall loop gain T_1. (b) Outer loop gain T_2.

4) Integrator gain:

$$K_v = \frac{K_{id}\,\omega_{cr}\,R_i\,\omega_{zc}}{\omega_{id}\,K_{vd}} = \frac{16\,(2\pi \cdot 3.39 \times 10^3)\,0.67\,(2\pi \cdot 928)}{(2\pi \cdot 339)16} = 3.91 \times 10^4$$

5) Voltage feedback circuit: $R_1 = 10\ \text{k}\Omega$

$\Rightarrow R_2 = 92.3\ k\Omega$, $C_2 = 1.86$ nF, and $C_3 = 0.70$ nF

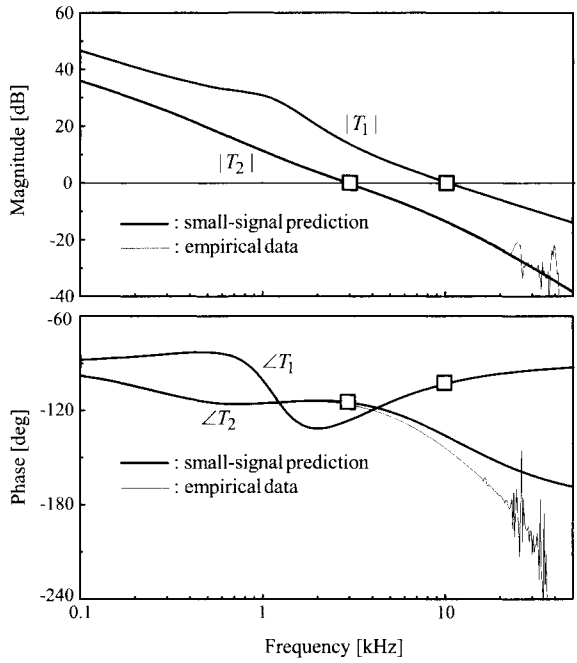


Figure 10.25 Comparison between overall loop gain T_1 and outer loop gain T_2.

The performance of the converter is evaluated using PSpice®simulations. Whenever appropriate and informative, the theoretical predictions are compared with the empirical data obtained from the computational method. Figure 10.24 shows the Bode plots of the individual feedback loops and system loop gains. The Bode plots shows a close resemblance to the asymptotic plots in Fig. 10.21. Figure 10.24(a) confirms that the crossover frequency $T_1(s)$ is located at the exact target frequency, $\omega_{ci} = 2\pi \cdot 10 \times 10^3$ rad/s. On the other hand, the $T_2(s)$ crossover frequency is placed in close proximity to the design aim, $\omega_{cr} = 2\pi \cdot 3.0 \times 10^3$ rad/s.

Figure 10.25 compares the Bode plot of $T_1(s)$ and $T_2(s)$. The theoretical forecasts of the outer loop gain $T_2(s)$ are compared with the empirical data. The predictions and empirical data exhibit a noticeable disparity in the phase characteristics. This difference is due to the sampling effects of current mode control, which are not considered in the classical analysis. Further discussions about this observation will be given in the next chapter. Both the loop gains have a sufficient phase margin; the phase margin of $T_1(s)$ is 78° and that of $T_2(s)$ is 65°. The output impedance and audio-susceptibility characteristics are shown in Fig. 10.26. The time-domain performance of the converter is displayed in Fig. 10.27. Figure 10.27(a) is the transient response of the output voltage due to the step changes of $R = 1\ \Omega \Rightarrow 0.5\ \Omega \Rightarrow 1\ \Omega$ in the load resistance, while

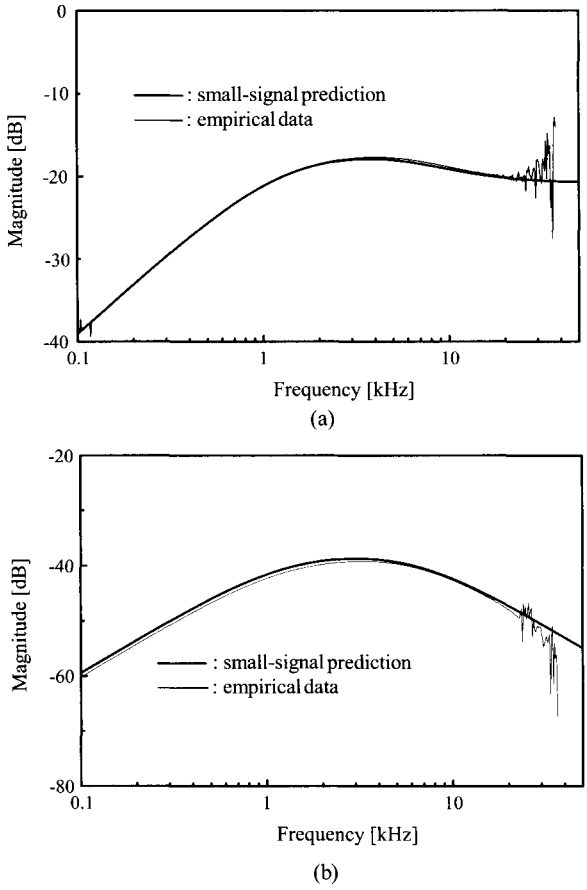


Figure 10.26 Closed-loop performance. (a) Output impedance. (b) Audio-susceptibility.

Fig. 10.27(b) shows the transient response with the V_S = 16 V ⇒ 8 V ⇒ 16 V changes in the input voltage.

10.2.6 Analysis of Converter Dynamics in DCM

As discussed in Chapter 9, the power stage dynamics alter significantly as dc-to-dc converters cross the CCM/DCM boundary. Accordingly, it is informative to investigate the impacts of DCM operation on the converter performance. It will be shown that current mode control could alleviate the sensitivity of the converter performance to the operational mode, compared to voltage mode control.

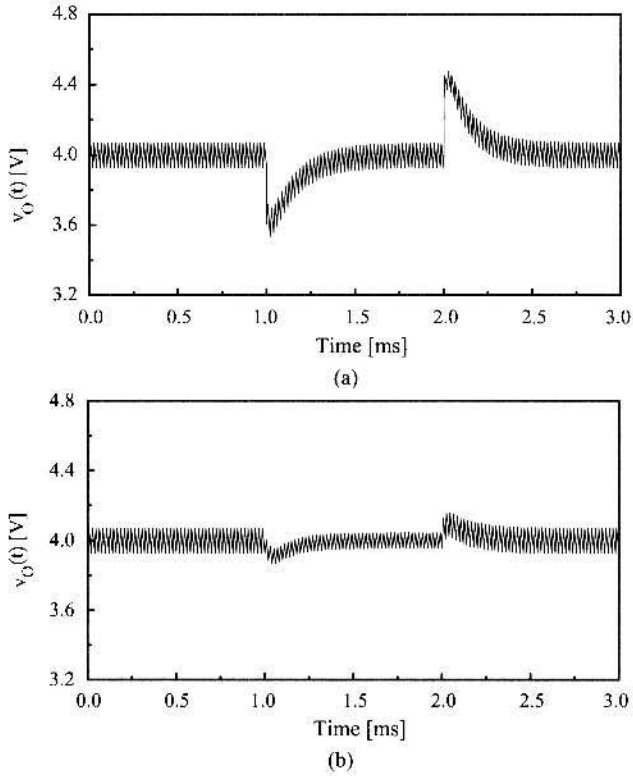


Figure 10.27 Transient response. (a) Step load response. (b) Step input response.

■ EXAMPLE 10.9 Converter Performance in DCM

The performance of the buck converter used in the previous example is evaluated in DCM operations and compared with that of the CCM operation. For the given operational conditions, the critical resistance for the CCM/DCM boundary is determined as $R_{crit} = 2L/(D'T_s) = 5.33\ \Omega$. The DCM power stage model, developed earlier in Section 9.1.2, is combined with the small-signal model of the peak current mode control, resulting in the complete small-signal model in DCM operation. The model predictions are presented in comparison with the empirical data obtained from the computational method. Figure 10.28 first shows the outer loop gain of the converter evaluated with $R = 10\ \Omega$.

Figure 10.29 displays the DCM outer loop gains, evaluated with $R = R_{crit} = 5.33\ \Omega$, $R = 10\ \Omega$, and $R = 20\ \Omega$, along with the CCM loop gain with $R = 1\ \Omega$. The loop gains exhibit relatively small changes in both the crossover frequency and phase margin, compared to the case of the conventional voltage mode control shown in Fig. 9.14. The reduced sensitivity of the loop gain can be explained as follows. The change in the power stage dynamics consistently

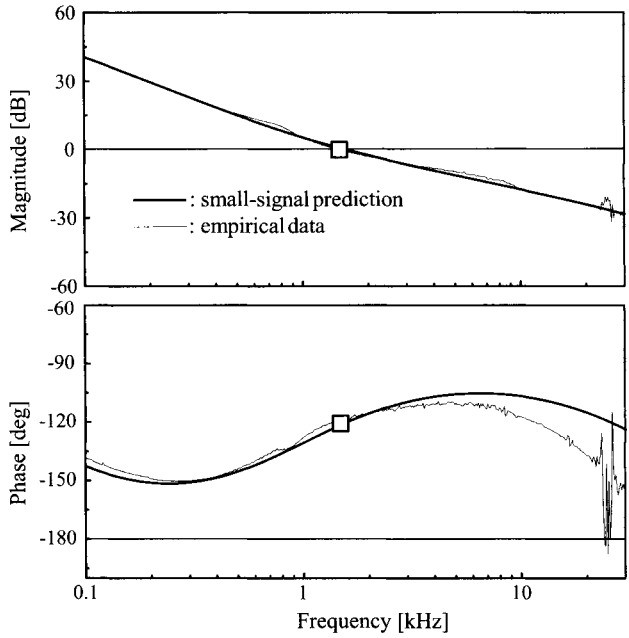


Figure 10.28 Outer loop gain in DCM.

occurs in all the power stage transfer functions. In DCM operations, the split of the power stage double pole and reduction in the mid-band gain will appear in both $G_{vd}(s)$ and $G_{id}(s)$. For frequencies where $|T_i| \gg 1$, the outer loop gain is approximated as $T_2(s) \approx T_v(s)/T_i(s) = G_{vd}(s)F_v(s)F'_m/(G_{id}(s)R_iF'_m)$. Accordingly, the changes occurring in both $G_{vd}(s)$ and $G_{id}(s)$ will be canceled and will not show in $T_2(s)$.

Lastly, Fig. 10.30 compares the transitional output voltage in response to the step changes in the load resistance: $R = 0.8\ \Omega \Rightarrow 1\ \Omega \Rightarrow 0.8\ \Omega$ for CCM case, and $R = 5.3\ \Omega \Rightarrow 20\ \Omega \Rightarrow 5.3\ \Omega$ for DCM case. When compared with the voltage mode control in Fig. 9.16, the changes in the transient response are also reduced.

10.3 CLOSED-LOOP PERFORMANCE OF PEAK CURRENT MODE CONTROL

The previous section investigated the dynamics of the peak current mode control, focusing on the individual feedback loops and system loop gains, along with their use in stability analysis and control design. Based on these analyses, step-by-step control design procedures are established. It was found that the two-pole one-zero compensation offers both stability and good loop gain characteristics.

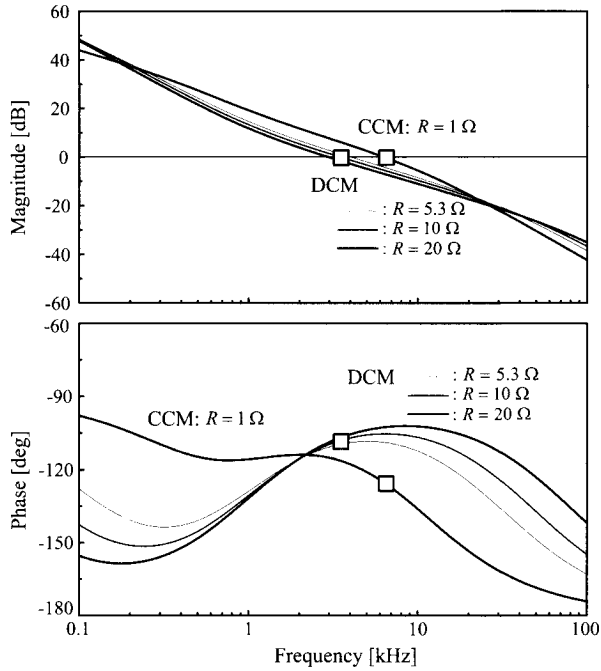


Figure 10.29 Outer loop gain in CCM and DCM operations.

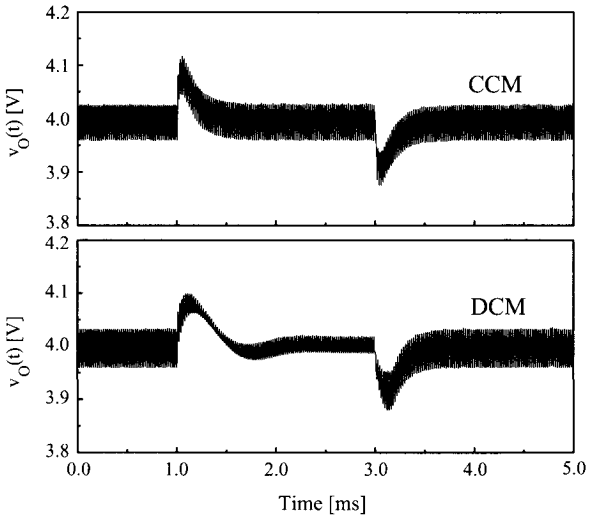


Figure 10.30 Step load response in CCM and DCM operations.

This section now investigates the closed-loop performance of the current-mode controlled PWM converters that employ the two-pole one-zero compensation. The audio-susceptibility and output impedance are analyzed in detail, concentrating on the impacts of the voltage feedback compensation. In particular, the choice of the integrator gain is investigated in conjunction with the position of the crossover frequency of the outer loop gain $T_2(s)$.

This section also analyzes the step load response of current-mode controlled PWM converters. The relationship between the output impedance and step load response is studied, leading to practical methods for predicting the step load response from the output impedance characteristics.

The analysis is presented in a general manner, and, as such, the results are applicable to all the three basic converters. This section first presents buck converter examples. The boost converter examples will be discussed in the next section.

10.3.1 Audio-Susceptibility Analysis

The audio-susceptibility denotes the closed-loop input-to-output transfer function. The general expression of the audio-susceptibility for the three basic PWM converters is derived from Fig. 10.15

$$A_u(s) = \frac{\hat{v}_o(s)}{\hat{v}_s(s)} = \frac{G_{vs}(1 + G_{id}R_iF'_m) - G_{is}R_iF'_mG_{vd}}{1 + G_{id}R_iF'_m + G_{vd}F_vF'_m} \tag{10.58}$$

Using the definitions of the current loop $T_i(s) = G_{id}(s)R_iF'_m$ and voltage loop $T_v(s) = G_{vd}(s)F_v(s)F'_m$, the preceding expression is written as

$$\begin{aligned} A_u(s) &= \frac{G_{vs}(1 + T_i) - G_{is}\dfrac{T_i}{G_{id}}G_{vd}}{1 + T_i + T_v} \\ &= \frac{G_{vs} + T_i\left(G_{vs} - \dfrac{G_{is}G_{vd}}{G_{id}}\right)}{1 + T_i + T_v} \end{aligned} \tag{10.59}$$

Now, the audio-susceptibility is analyzed using the expression (10.59). We first consider buck converters and later deal with boost and buck/boost converters.

Buck Converter

The buck converter is a special case in which the audio-susceptibility analysis is performed in a simple way. For buck converters, it can be shown from Table 10.2 that

$$\frac{G_{vs}(s)}{G_{vd}(s)} = \frac{G_{is}(s)}{G_{id}(s)} = \frac{D}{V_s} \tag{10.60}$$

which implies

$$G_{vs}(s) - \frac{G_{is}(s)G_{vd}(s)}{G_{id}(s)} = 0 \tag{10.61}$$

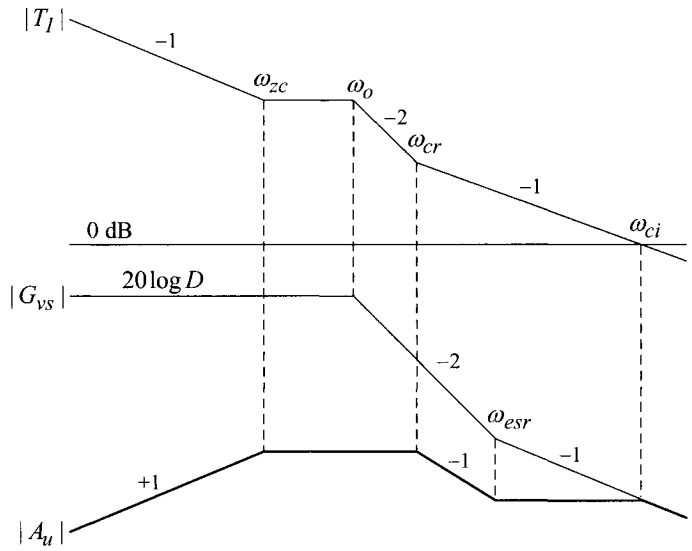


Figure 10.31 Asymptotic analysis of audio-susceptibility.

The audio-susceptibility expression in (10.59) now reduces to

$$A_u(s) = \frac{G_{vs}(s)}{1 + T_i(s) + T_v(s)} = \frac{G_{vs}(s)}{1 + T_1(s)} \tag{10.62}$$

where $T_1(s) = T_i(s) + T_v(s)$ is the overall loop gain. Thus, for buck converters, the audio-susceptibility analysis is identical to that of voltage mode control. The role of the loop gain in voltage mode control is replaced with the overall loop gain $T_1(s)$ in current mode control.

The asymptotic analysis is performed on (10.62), yielding the result shown in Fig. 10.31. The asymptotic plot is constructed using the $G_{vs}(s)$ expression in Table 10.2 and the $|T_1|$ structure shown in Fig. 10.21(a). According to the previous design procedures, the parameters of the voltage feedback compensation are selected as $\omega_{pc} = \omega_{esr}$ and $\omega_{zc} < \omega_o$. The asymptotic plot is converted into an equation for the audio-susceptibility

$$A_u(s) = \frac{D}{V_S F_m' K_v} s \frac{1 + \dfrac{s}{\omega_{esr}}}{\left(1 + \dfrac{s}{\omega_{zc}}\right)\left(1 + \dfrac{s}{\omega_{cr}}\right)\left(1 + \dfrac{s}{\omega_{ci}}\right)} \tag{10.63}$$

based on the analysis technique presented in Table 8.2. The parameter ω_{cr} denotes the frequency where $|T_i| = |T_v|$, which corresponds to the crossover frequency of the outer loop gain $T_2(s)$. Figure 10.31 is a specific example where ω_{cr} is located below the esr zero: $\omega_{cr} < \omega_{esr}$.

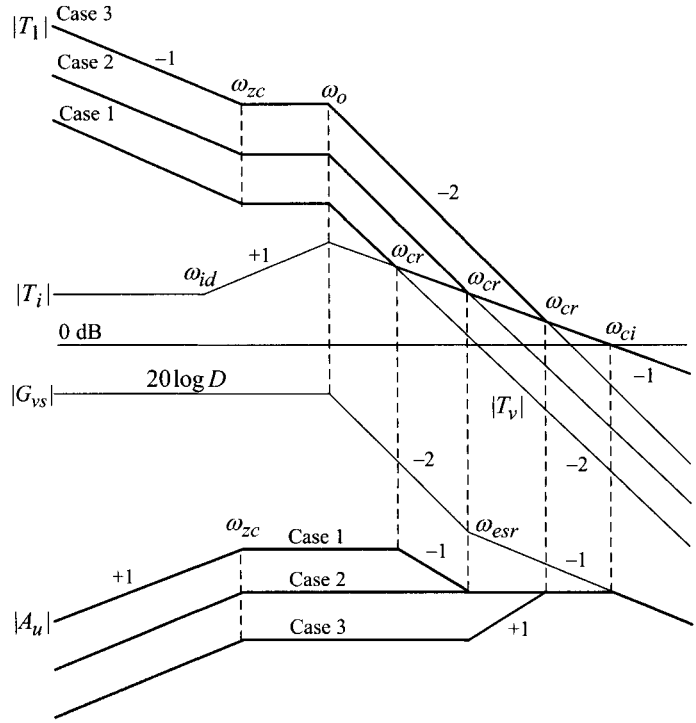


Figure 10.32 Asymptotic analysis of audio-susceptibility.

The audio-susceptibility analysis is generalized in Fig. 10.32 which shows the asymptotic plots for $|G_{vs}|$, $|T_1|$, and $|A_u|$, along with $|T_i|$ and $|T_v|$. In this general analysis, the integrator gain K_v of the voltage feedback compensation is varied to result in the following three cases:

- Case 1: $\omega_{cr} < \omega_{esr}$
- Case 2: $\omega_{cr} = \omega_{esr}$
- Case 3: $\omega_{cr} > \omega_{esr}$

The effect of K_v is clearly seen in Fig. 10.32. The larger K_v shifts ω_{cr} towards higher frequencies and reduces the peak value of $|A_u|$. However, this reduction only happens up to the K_v value that places ω_{cr} at ω_{esr}. Increasing K_v beyond this value does not reduce the audio-susceptibility any further. Instead, it could deteriorate the phase characteristics of $T_1(s)$; the phase margin will be lessened as ω_{cr} approaches the crossover frequency ω_{ci}. For Cases 2 and 3, the peak value of the audio-susceptibility is determined as

$$|A_u|_{peak} = 20 \log\left(\frac{D\,\omega_{zc}}{V_S F'_m K_v}\right) \tag{10.64}$$

For Case 1, the peak value of the audio-susceptibility is given by

$$|A_u|_{peak} = 20\log\left(\frac{D\,\omega_{zc}}{V_S F'_m K_v}\right) + 20\log\left(\frac{\omega_{cr}}{\omega_{esr}}\right) = 20\log\left(\frac{D\,\omega_{zc}}{V_S F'_m K_v}\,\frac{\omega_{cr}}{\omega_{esr}}\right) \tag{10.65}$$

For all three cases, the compensation zero ω_{zc} becomes the first pole in the audio-susceptibility. As demonstrated in Section 8.4.5, this pole determines the settling time of the step input response, $t_s = 3\tau = 3/\omega_{zc}$. Thus, ω_{zc} should be placed as high as possible, without exceeding the power stage double pole ω_o, as explained earlier in the control design procedures. As a general guideline, it was recommended that $\omega_{zc} = (0.6{-}0.8)\,\omega_o$ in the previous section.

■ EXAMPLE 10.10 Buck Converter Example

This example illustrates the accuracy of the previous audio-susceptibility analysis. The integrator gain of the buck converter used in Example 10.8 is now modified to result in the three cases discussed in this section, while other compensation parameters remain the same

- Case 1: $K_v = 1.97 \times 10^4 \quad \Rightarrow \omega_{cr} = 0.5\,\omega_{esr}$
- Case 2: $K_v = 3.91 \times 10^4 \quad \Rightarrow \omega_{cr} = \omega_{esr}$
- Case 3: $K_v = 7.82 \times 10^4 \quad \Rightarrow \omega_{cr} = 2.0\,\omega_{esr}$

Figure 10.33 shows the simulations of various transfer functions of the three cases, which validate the preceding theoretical discussions.

Boost and Buck/Boost Converters

For other topologies, the expression of the audio-susceptibility does not reduce to the simple form of (10.62). For boost and buck/boost converters, the audio-susceptibility analysis proceeds from (10.59). At the frequencies below the $T_i(s)$ crossover frequency, where $|T_i| \gg 1$, the audio-susceptibility expression in (10.59) is approximated as

$$\begin{aligned} A_u(s) &= \frac{G_{vs} + T_i\left(G_{vs} - \dfrac{G_{is}G_{vd}}{G_{id}}\right)}{1 + T_i + T_v} \\ &\approx \frac{G_{vs} + (1 + T_i)\left(G_{vs} - \dfrac{G_{is}G_{vd}}{G_{id}}\right)}{1 + T_i + T_v} \end{aligned} \tag{10.66}$$

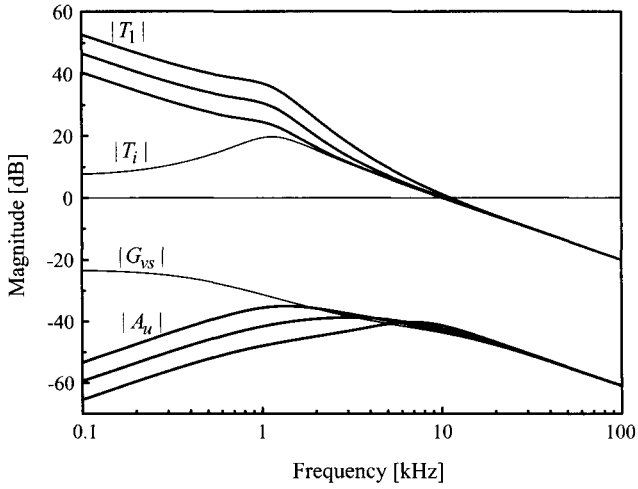


Figure 10.33 Audio-susceptibility of buck converter.

This equation is rearranged as

$$A_u(s) = \frac{G_{vs}}{1+T_i+T_v} + \frac{G_{vs} - \dfrac{G_{is}G_{vd}}{G_{id}}}{1+\dfrac{T_v}{1+T_i}}$$

$$= \frac{G_{vs}}{1+T_1} + \frac{G_{vs} - \dfrac{G_{is}G_{vd}}{G_{id}}}{1+T_2} \tag{10.67}$$

where $T_1(s) = T_i(s) + T_v(s)$ is the overall loop gain and $T_2(s) = T_v(s)/(1 + T_i(s))$ is the outer loop gain. By the definitions of $T_1(s)$ and $T_2(s)$, it follows that

$$|T_1| = |T_i + T_v| \gg |T_2| = \left|\frac{T_v}{1+T_i}\right| \tag{10.68}$$

It also can be shown from Table 10.2 that

$$\left|G_{vs} - \frac{G_{is}G_{vd}}{G_{id}}\right| \gg |G_{vs}| \tag{10.69}$$

The two inequalities of (10.68) and (10.69) further simplify the audio-susceptibility to

$$A_u(s) \approx \frac{G_{vs} - \dfrac{G_{is}G_{vd}}{G_{id}}}{1+T_2(s)} = \frac{A_{ui}(s)}{1+T_2(s)} \tag{10.70}$$

with $A_{ui}(s) = G_{vs} - G_{is}G_{vd}/G_{id}$.

Table 10.4 Expressions for Numerator of $A_u(s)$ and $Z_o(s)$

	$A_{ui}(s) = G_{vs} - \dfrac{G_{is}G_{vd}}{G_{id}}$	$Z_{oi}(s) = Z_p - \dfrac{Z_qG_{vd}}{G_{id}}$
Buck converter	0	$R\dfrac{1 + sCR_c}{1 + sC(R + R_c)}$
Boost converter	$\dfrac{1}{2(1 - D)}\dfrac{1 + sCR_c}{1 + sC(R + R_c)/2}$	$\dfrac{R}{2}\dfrac{1 + sCR_c}{1 + sC(R + R_c)/2}$
Buck/boost converter	$\dfrac{D^2}{(1 + D)(1 - D)}\dfrac{1 + sCR_c}{1 + \dfrac{sC(R + R_c)}{1 + D}}$	$\dfrac{R}{1 + D}\dfrac{1 + sCR_c}{1 + \dfrac{sC(R + R_c)}{1 + D}}$

The asymptotic analysis can now be applied to (10.70) in order to investigate the audio-susceptibility characteristics. In this analysis, the outer loop gain $T_2(s)$ alone appears in the denominator while the overall loop gain $T_1(s)$ is not involved at all. This is in contrast to the buck converter case where $T_1(s)$ is the only loop gain associated with the audio-susceptibility analysis.

Using the power stage transfer functions in Table 10.2, the numerator of (10.70), $A_{ui}(s) = G_{vs} - G_{is}G_{vd}/G_{id}$, can be expressed in a simple form. The results are shown in Table 10.4. Using these expressions, along with knowledge about the outer loop gain $T_2(s)$, the audio-susceptibility is analyzed. Details about this analysis are given in the next section which deals with a boost converter. It should be reminded that this analysis is valid only for the frequencies below the $T_i(s)$ crossover frequency. At higher frequencies where $|T_i| \approx 0$ and $|T_v| \approx 0$, the audio-susceptibility simply follows $G_{vs}(s)$, as can be seen from (10.59).

10.3.2 Output Impedance Analysis

The output impedance is another important performance criterion for closed-loop controlled converters. The output impedance is analyzed in the same manner as that of the audio-susceptibility. The expression for the output impedance is derived from Fig. 10.15

$$Z_o(s) = \frac{Z_p(1 + T_i) - Z_qR_iF'_mG_{vd}}{1 + T_i + T_v} = \frac{Z_p(1 + T_i) - Z_q\dfrac{T_i}{G_{id}}G_{vd}}{1 + T_i + T_v} \tag{10.71}$$

This expression is simplified to

$$Z_o(s) = \frac{Z_p + T_i\left(Z_p - \dfrac{Z_qG_{vd}}{G_{id}}\right)}{1 + T_i + T_v} \approx \frac{Z_p + (1 + T_i)\left(Z_p - \dfrac{Z_qG_{vd}}{G_{id}}\right)}{1 + T_i + T_v} \tag{10.72}$$

in the frequency range below the $T_i(s)$ crossover frequency, and rearranged as

$$Z_o(s) = \frac{Z_p}{1+T_i+T_v} + \frac{Z_p - \dfrac{Z_q G_{vd}}{G_{id}}}{1+\dfrac{T_v}{1+T_i}}$$

$$= \frac{Z_p}{1+T_1} + \frac{Z_p - \dfrac{Z_q G_{vd}}{G_{id}}}{1+T_2} \tag{10.73}$$

Due to the conditions $|T_1| \gg |T_2|$ and $|Z_p - Z_q G_{vd}/G_{id}| \gg |Z_p|$, the output impedance is further simplified to

$$Z_o(s) \approx \frac{Z_p - \dfrac{Z_q G_{vd}}{G_{id}}}{1+T_2(s)} = \frac{Z_{oi}(s)}{1+T_2(s)} \tag{10.74}$$

with $Z_{oi}(s) = Z_p - Z_q G_{vd}/G_{id}$.

The numerator of (10.74), $Z_{oi}(s) = Z_p - Z_q G_{vd}/G_{id}$, is interpreted as the output impedance evaluated under the condition that the current loop is only closed and the voltage loop is broken. This is because the output impedance $Z_o(s)$ reduces to $Z_{oi}(s)$ when $T_2(s) = T_v(s)/(1+T_i(s)) = 0$, which is true when $T_v(s) = 0$. The expressions for $Z_{oi}(s)$ are shown in Table 10.4. For all the three basic converters, the $Z_{oi}(s)$ expression fits into the following format

$$Z_{oi}(s) \approx K_{oi} \frac{1+\dfrac{s}{\omega_{esr}}}{1+\dfrac{s}{\omega_{pi}}} \tag{10.75}$$

where $\omega_{esr} = 1/(CR_c)$ is the esr zero. The expressions for K_{oi} and ω_{pi} are given in Table 10.5. It should be noted that ω_{pi} is practically identical to ω_{id} in the $G_{id}(s)$ expression in Table 10.2. The ω_{id} appears as a pole in $|T_2|$ structure in Fig. 10.21(b).

Table 10.5 Expressions for K_{oi} and ω_{pi}

	K_{oi}	ω_{pi}
Buck converter	R	$\dfrac{1}{C(R+R_c)}$
Boost converter	$\dfrac{R}{2}$	$\dfrac{2}{C(R+R_c)}$
Buck/boost converter	$\dfrac{R}{1+D}$	$\dfrac{1+D}{C(R+R_c)}$

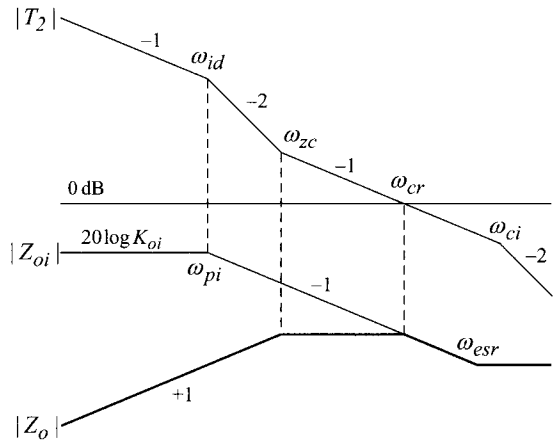


Figure 10.34 Output impedance analysis.

It can be seen from Table 10.5 that the high-frequency asymptote of $|Z_{oi}|$ is the parallel combination of the load resistor and esr of the output capacitor

$$|Z_{oi}(j\infty)| = 20\log\left(K_{oi}\frac{\omega_{pi}}{\omega_{esr}}\right) = 20\log\left(\frac{RR_c}{R+R_c}\right) = 20\log\left(R \parallel R_c\right) \tag{10.76}$$

Now, the output impedance is investigated by performing the asymptotic analysis on (10.74). Figure 10.34 is the result of this analysis. The asymptotic plot is constructed using the expression of $Z_{oi}(s)$ in (10.75) and the structure of $|T_2|$ in Fig. 10.21(b), with the incorporation of the fact $\omega_{pi} = \omega_{id}$. This analysis assumes that the $|T_2|$ crossover occurs before the esr zero: $\omega_{cr} < \omega_{esr}$.

Figure 10.35 shows the output impedance analysis for general cases. The integrator gain K_v in the voltage feedback compensation, which controls the $T_2(s)$ crossover frequency ω_{cr}, is varied to result in the three cases: Case 1 with $\omega_{cr} < \omega_{esr}$, Case 2 with $\omega_{cr} = \omega_{esr}$, and Case 3 with $\omega_{cr} > \omega_{esr}$. For Cases 2 and 3, the peak value of the output impedance is reduced to $20\log(R\|R_c)$, which is the theoretical minimum for the given power stage parameters. For Case 1, the peak value is given by

$$\begin{aligned} |Z_o(j\omega)|_{peak} &= 20\log(R\|R_c) + 20\log\left(\frac{\omega_{esr}}{\omega_{cr}}\right) \\ &= 20\log\left(R \parallel R_c\frac{\omega_{esr}}{\omega_{cr}}\right) \end{aligned} \tag{10.77}$$

For all the three cases, the output impedance has the same first pole at the compensation zero ω_{zc}. As will be shown later, this pole determines the speed of the step load response. For faster response, ω_{zc} should be placed at higher frequency but should not exceed the power stage pole ω_o, in order not to become a conditionally stable system.

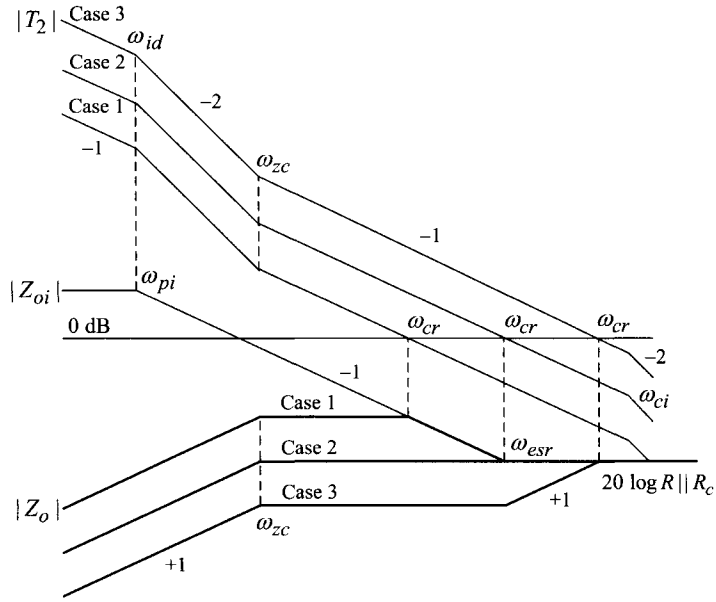


Figure 10.35 Generalization of output impedance analysis.

Figure 10.35 shows that the output impedance can be optimized by placing the $T_2(s)$ crossover frequency at ω_{esr}. Increasing the $T_2(s)$ crossover frequency beyond ω_{esr} does not further reduce the peak value of the output impedance.

The asymptotic plots in Fig. 10.35 assume that the phase margin of $T_2(s)$ is sufficiently large. This assumption precludes the potential peaking in the output impedance at the crossover frequency of $T_2(s)$. Cases where the outer loop gain does not satisfy this assumption are discussed in the next section.

■ EXAMPLE 10.11 Buck Converter Example

The buck converter used in Example 10.10 is revisited in order to substantiate the preceding output impedance analysis. The same compensation parameters as those of Example 10.10 are used to result in the three cases of the output impedance analysis: Case 1 with $\omega_{cr} = 0.5\,\omega_{esr}$, Case 2 with $\omega_{cr} = \omega_{esr}$, and Case 3 with $\omega_{cr} = 2.0\,\omega_{esr}$. Computer simulations for the three cases are shown in Fig. 10.36, which exhibit a close match with the asymptotic analysis of Fig. 10.35.

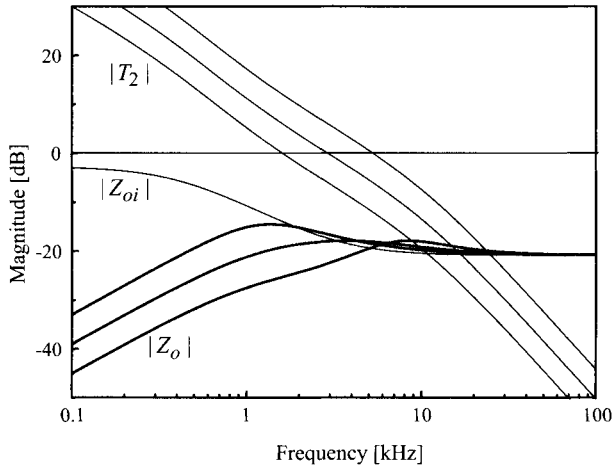


Figure 10.36 Output impedance analysis.

10.3.3 Step Load Response Analysis

The step load response is referred to as the transient waveform of the output voltage due to a step change in the load current. The analysis method for the step load response was discussed in Section 7.3.1. The step load response is investigated using the output impedance and its relationship to the output voltage

$$v_O(t) = \mathcal{L}^{-1}\left(\frac{I_{step}}{s} Z_o(s)\right) \tag{10.78}$$

where $\mathcal{L}^{-1}$ is the inverse Laplace transformation and I_{step} is the magnitude of the step change in the load current.

In this section, the step load response is investigated using the results of the previous output impedance analysis, along with the relationship of (10.78). As shown in Fig. 10.35, the output impedance is classified into three cases depending upon the relative location of the $T_2(s)$ crossover frequency, ω_{cr}, and the esr zero, ω_{esr}. The three illustrative examples in Fig. 10.35 are arranged into Case 1, Case 2, and Case 3 in increasing order of the $T_2(s)$ crossover frequency. However, for smoother flow in the analytical development, the step load response is first discussed for the output impedance of Case 2 with $\omega_{cr} = \omega_{esr}$. The analysis then continues with Case 3 of $\omega_{cr} > \omega_{esr}$, and finally treats Case 1 with $\omega_{cr} < \omega_{esr}$. The analysis now starts with Case 2.

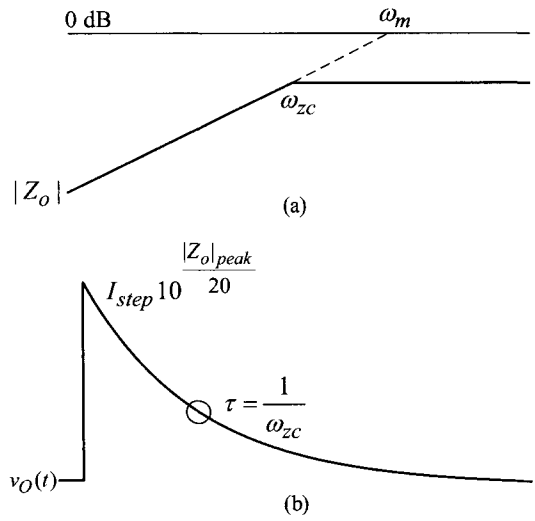


Figure 10.37 Case 2 with $\omega_{cr} = \omega_{esr}$. (a) Output impedance. (b) Step load response.

Case 2: $\omega_{cr} = \omega_{esr}$

This is the case in which the $T_2(s)$ crossover frequency falls at the esr zero. Figure 10.37(a) shows the output impedance of this case. The expression for the output impedance becomes

$$Z_o(s) = \frac{s}{\omega_m} \frac{1}{1 + \frac{s}{\omega_{zc}}} \tag{10.79}$$

where ω_m represents the frequency at which the initial linear segment of $|Z_o|$ crosses the 0 dB line. The peak magnitude of the output impedance is given by

$$|Z_o(j\omega)|_{peak} = |Z_o(j\infty)| = 20\log\left(\frac{\omega_{zc}}{\omega_m}\right) \tag{10.80}$$

The transient response of the output voltage due to the step load change of I_{step} is evaluated as

$$\begin{aligned} v_O(t) &= \mathcal{L}^{-1}\left(\frac{I_{step}}{s} \frac{s}{\omega_m} \frac{1}{1 + \frac{s}{\omega_{zc}}}\right) \\ &= I_{step} \frac{\omega_{zc}}{\omega_m} e^{-\omega_{zc}t} \end{aligned} \tag{10.81}$$

The peak overshoot of the output voltage is found as

$$v_O(t)_{peak} = v_O(0) = I_{step} \frac{\omega_{zc}}{\omega_m} = I_{step} 10^{\frac{|Z_o|_{peak}}{20}} \tag{10.82}$$

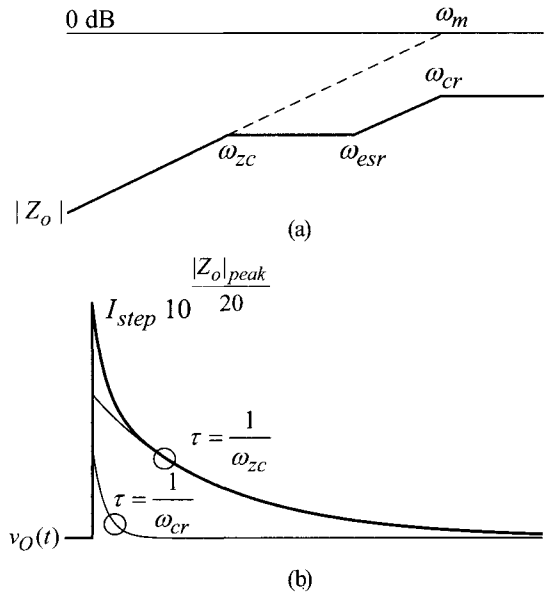


Figure 10.38 Case 3 with $\omega_{cr} > \omega_{esr}$. (a) Output impedance. (b) Step load response.

The output voltage decays from its initial peak with a time constant of $\tau = 1/\omega_{zc}$. Thus, the settling time of v_O is given by $t_s = 3\tau = 3/\omega_{zc}$. The output voltage waveform is shown in Fig. 10.37(b).

Case 3: $\omega_{cr} > \omega_{esr}$

This case corresponds to the situation where the $T_2(s)$ crossover frequency is pushed beyond the esr zero. Figure 10.38(a) shows the output impedance for this case. The output impedance is expressed as

$$Z_o(s) = \frac{s}{\omega_m} \frac{1 + \dfrac{s}{\omega_{esr}}}{\left(1 + \dfrac{s}{\omega_{zc}}\right)\left(1 + \dfrac{s}{\omega_{cr}}\right)} \tag{10.83}$$

with $\omega_{zc} \ll \omega_{esr} \ll \omega_{cr}$. The peak magnitude of the output impedance is given by

$$|Z_o(j\omega)|_{peak} = |Z_o(j\infty)| = 20 \log\left(\frac{\omega_{zc}}{\omega_m} \frac{\omega_{cr}}{\omega_{esr}}\right) \tag{10.84}$$

The transient response of the output voltage due to the step load change of I_{step} is given by

$$\begin{aligned} v_O(t) &= \mathcal{L}^{-1}\left(\frac{I_{step}}{s}\frac{s}{\omega_m}\frac{1+\dfrac{s}{\omega_{esr}}}{\left(1+\dfrac{s}{\omega_{zc}}\right)\left(1+\dfrac{s}{\omega_{cr}}\right)}\right) \\ &= \frac{I_{step}}{\omega_{cr}-\omega_{zc}}\frac{\omega_{zc}\,\omega_{cr}}{\omega_m\omega_{esr}}\left((\omega_{esr}-\omega_{zc})e^{-\omega_{zc}t}+(\omega_{cr}-\omega_{esr})e^{-\omega_{cr}t}\right) \end{aligned} \tag{10.85}$$

where $(\omega_{esr} - \omega_{zc}) > 0$ and $(\omega_{cr} - \omega_{esr}) > 0$. The step load response is the sum of the two exponentially decaying terms. The second term decays much faster than the first term, due to the condition $\omega_{zc} \ll \omega_{cr}$. The peak deviation of the output voltage is expressed as

$$v_O(t)_{peak} = v_O(0) = I_{step}\frac{\omega_{zc}}{\omega_m}\frac{\omega_{cr}}{\omega_{esr}} = I_{step}10^{\dfrac{|Z_o|_{peak}}{20}} \tag{10.86}$$

Figure 10.38(b) shows the output voltage waveform. The output voltage decays from its initial peak with the fast rate of $1/\omega_{cr}$ in the beginning, and with the slow rate of $1/\omega_{zc}$ after the second term diminishes. The peak overshoot of the output voltage is the same as Case 2, but its initial decay is faster due to the condition $\omega_{zc} \ll \omega_{cr}$. Nonetheless, the settling time will be determined by the slow time constant, $t_s = 3/\omega_{zc}$.

Case 1: $\omega_{cr} < \omega_{esr}$

In this case, the $T_2(s)$ crossover frequency falls below the esr zero. Figure 10.39 shows the output impedance and the step load response for this case. The output impedance is expressed as

$$Z_o(s) = \frac{s}{\omega_m}\frac{1+\dfrac{s}{\omega_{esr}}}{\left(1+\dfrac{s}{\omega_{zc}}\right)\left(1+\dfrac{s}{\omega_{cr}}\right)} \tag{10.87}$$

with $\omega_{zc} \ll \omega_{cr} \ll \omega_{esr}$. This expression is the same as (10.83), yet the order of the corner frequencies is different. Unlike the previous two cases, the peak value of the output impedance does not coincide with the high-frequency asymptote. From Fig. 10.39(a), the peak magnitude of the output impedance is given by

$$|Z_o(j\omega)|_{peak} = \left|\frac{s}{\omega_m}\right|_{s=j\omega_{zc}} = 20\log\left(\frac{\omega_{zc}}{\omega_m}\right) \tag{10.88}$$

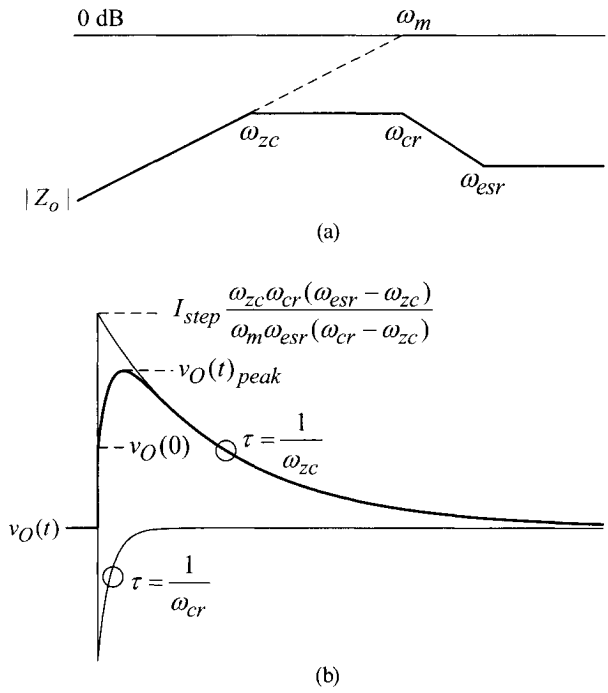


Figure 10.39 Case 1 with $\omega_{cr} < \omega_{esr}$. (a) Output impedance. (b) Step load response.

On the other hand, the high-frequency asymptote is expressed as

$$|Z_o(j\infty)| = 20\log\left(\frac{\omega_{zc}}{\omega_m}\frac{\omega_{cr}}{\omega_{esr}}\right) \tag{10.89}$$

The transient response due to the step load change of I_{step} is evaluated as

$$v_O(t) = \frac{I_{step}}{\omega_{cr}-\omega_{zc}}\frac{\omega_{zc}\,\omega_{cr}}{\omega_m\omega_{esr}}\left((\omega_{esr}-\omega_{zc})e^{-\omega_{zc}t} + (\omega_{cr}-\omega_{esr})e^{-\omega_{cr}t}\right) \tag{10.90}$$

with $(\omega_{esr} - \omega_{zc}) > 0$ and $(\omega_{cr} - \omega_{esr}) < 0$. This description is identical to (10.85), but the sign of the coefficients differs. The step load response is the sum of the two exponentially decaying terms, the same as Case 2. However, the polarities of the two exponential terms are opposite; the first coefficient is positive while the second is negative. The second negative term decays much faster than the first positive term. The waveform for this case is shown in Fig. 10.39(b). The settling time of the output voltage is still governed by the slow time constant, $t_s = 3/\omega_{zc}$.

The initial value of the output voltage is given by

$$v_O(0) = I_{step}\frac{\omega_{zc}}{\omega_m}\frac{\omega_{cr}}{\omega_{esr}} = I_{step}10^{\dfrac{|Z_o(j\infty)|}{20}} \tag{10.91}$$

Unlike the previous cases, the peak deviation of the output voltage, $v_O(t)_{peak}$, cannot be explicitly described in terms of $|Z_o|_{peak}$. Instead, $|Z_o|_{peak}$ can be used to predict the upper bound of $v_O(t)_{peak}$. From the profile of $v_O(t)$ in Fig. 10.39(b), it follows that

$$v_O(0) < v_O(t)_{peak} < I_{step} \frac{\omega_{zc}\,\omega_{cr}(\omega_{esr} - \omega_{zc})}{\omega_m\,\omega_{esr}(\omega_{cr} - \omega_{zc})} \tag{10.92}$$

The last term in (10.92) is the initial value of the slow-decaying first term in (10.90). With the conditions $\omega_{esr} \gg \omega_{zc}$ and $\omega_{cr} \gg \omega_{zc}$, the expression (10.92) is approximated as

$$v_O(0) < v_O(t)_{peak} < I_{step} \frac{\omega_{zc}}{\omega_m} \tag{10.93}$$

Finally, using (10.88) and (10.91), the above inequality is rewritten as

$$I_{step}\, 10^{\frac{|Z_o(j\infty)|}{20}} < v_O(t)_{peak} < I_{step}\, 10^{\frac{|Z_o(j\omega)|_{peak}}{20}} \tag{10.94}$$

The peak deviation of the output voltage can be estimated from (10.94). The high-frequency asymptote of the output impedance, $|Z_o(j\infty)|$, predicts the lower bound of $v_O(t)_{peak}$, while the peak value of the output impedance, $|Z_o(j\omega)|_{peak}$, estimates the upper bound.

■ EXAMPLE 10.12 Buck Converter Example

This example validates the preceding discussions about the step load response. The buck converter in Example 10.11 is used to generate the step load response for the three different cases: Case 1 with $\omega_{cr} = 0.5\,\omega_{esr}$, Case 2 with $\omega_{cr} = \omega_{esr}$, and Case 3 with $\omega_{cr} = 2.0\,\omega_{esr}$. The output impedances for these cases were shown in Fig. 10.36. A series of step changes, $I_O = 4$ A $\Rightarrow$ 8 A $\Rightarrow$ 4 A, is introduced to the load current and the output voltage waveforms are shown in Fig. 10.40. While the profiles of the transient responses are different, the settling time can be considered to be largely the same for all the three cases

$$t_s = \frac{3}{\omega_{zc}} = \frac{3}{2\pi \cdot 928} = 0.51 \text{ ms}$$

For Cases 2 and 3, the peak deviation of the output voltage is given by

$$v_O(t)_{\text{peak}} = I_{step} 10^{\frac{|Z_o|_{peak}}{20}} = 4 \cdot 10^{-20/20} = 0.4 \text{ V}$$

For Case 1, $v_O(t)_{peak}$ is estimated as

$$I_{step}\, 10^{\frac{|Z_o(j\infty)|}{20}} < v_O(t)_{peak} < I_{step}\, 10^{\frac{|Z_o(j\omega)|_{peak}}{20}}$$

$$\Rightarrow 4 \cdot 10^{-20/20} < v_O(t)_{peak} < 4 \cdot 10^{-15/20}$$

$$\Rightarrow 0.40 \text{ V} < v_O(t)_{peak} < 0.71 \text{ V}$$

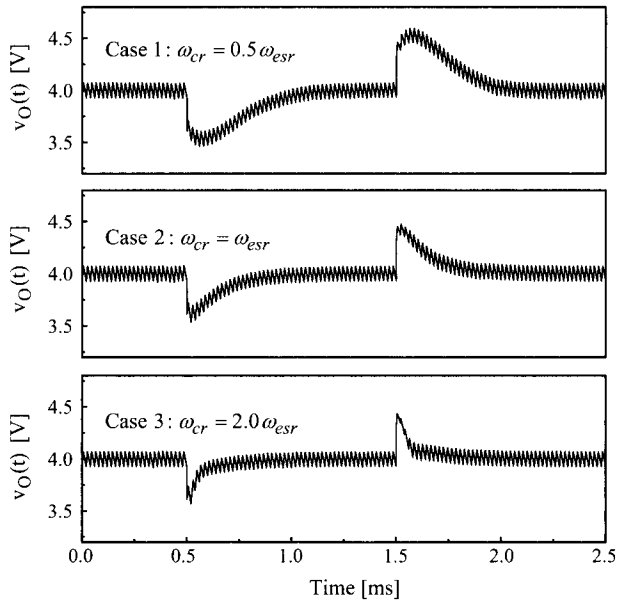


Figure 10.40 Step load response of buck converter.

Compensation Design and Step Load Response

As demonstrated in the previous section, the step load response is mainly determined by the voltage feedback compensation design. In particular, the output voltage deviation can be reduced to the theoretical minimum by placing the $T_2(s)$ crossover frequency at the esr zero. Increasing the $T_2(s)$ crossover beyond the esr zero does not reduce the peak deviation any further. Nonetheless, as shown in Example 10.12, the higher $T_2(s)$ crossover frequency results in a faster transient response at the beginning, thereby reducing the total time necessary for the output voltage to reach a specified percentage of its final value.

The previous analysis assumes that the phase margin of $T_2(s)$ is sufficiently large. In real applications, however, it is not always possible to push the $T_2(s)$ crossover frequency to the esr zero while maintaining a large phase margin. In some cases, pushing the $T_2(s)$ crossover frequency towards higher frequencies causes a reduction in the phase margin. As shown in Section 8.4.4, a small phase margin induces a peaking in the output impedance. If the phase margin is less than 60°, the output impedance exhibits a peaking at the $T_2(s)$ crossover frequency, as a function of the phase margin ϕ_m

$$|Z_o|_{\text{peaking}} = 20\log\left(\frac{1}{\sqrt{2-2\cos\phi_m}}\right) \tag{10.95}$$

The smaller the phase margin, the larger the peaking. The peaking in the output impedance is transformed into a pair of complex poles whose damping ratio is inversely proportional to the phase margin. These complex poles would result in an oscillatory transient response, as discussed in Section 8.4.4.

As shown in Fig. 10.21(b), the outer loop gain has a pole at the $T_i(s)$ crossover frequency, ω_{ci} in Fig. 10.21(b). For an adequate phase margin, the $T_2(s)$ crossover frequency should occur well before the $T_i(s)$ crossover frequency. With a predetermined $T_i(s)$ crossover frequency, commonly located around 15–30% of the switching frequency, the $T_2(s)$ crossover frequency can be increased up to the esr zero while maintaining a sufficient phase margin, only provided that the frequency of the esr zero itself is much lower than the switching frequency. If the esr zero does not meet this requirement, a compromise should be made; namely, the $T_2(s)$ crossover frequency should be increased within the limit that does not reduce the phase margin less than 60°. With such a design trade-off, the $T_2(s)$ crossover frequency would occur below the esr zero, resulting in the output impedance of Case 1. In this instance, the peak deviation of the output voltage is estimated from (10.94).

The settling time of the output voltage is determined by the zero of the voltage feedback compensation. For small settling time, the compensation zero ω_{zc} should be placed as high as possible without exceeding the power stage double pole ω_o. The design procedures recommended that $\omega_{zc} = (0.6 - 0.8)\,\omega_o$.

■ EXAMPLE 10.13 Buck Converter Example

This example illustrates the control design and closed-loop performance of a buck converter whose esr zero is not sufficiently lower than the switching frequency. In the buck converter used in Example 10.11, the esr of the output capacitor is decreased to $R_c = 25$ mΩ, while other power stage parameters remain unchanged. Now, the esr zero is located at $\omega_{esr} = 2\pi \cdot 1.36 \times 10^4$ rad/s = $0.27\,\omega_s$. With this modification, the integrator gain in the voltage feedback compensation is varied between $3.90 \times 10^4 < K_v < 3.13 \times 10^5$ to yield the four different designs listed in Table 10.6. The $T_2(s)$ crossover frequency spans between $0.2\,\omega_{esr} < \omega_{cr} < 1.0\,\omega_{esr}$ with a phase margin of $32° < \phi_m < 64°$.

Table 10.6 Four Different Control Designs

	Integrator gain	T_2 crossover frequency	T_2 phase margin
Design A	$K_v = 3.90 \times 10^4$	$\omega_{cr} = 0.2\,\omega_{esr}$	$\phi_m = 64°$
Design B	$K_v = 7.82 \times 10^4$	$\omega_{cr} = 0.4\,\omega_{esr}$	$\phi_m = 57°$
Design C	$K_v = 1.56 \times 10^5$	$\omega_{cr} = 0.6\,\omega_{esr}$	$\phi_m = 45°$
Design D	$K_v = 3.13 \times 10^5$	$\omega_{cr} = 1.0\,\omega_{esr}$	$\phi_m = 32°$

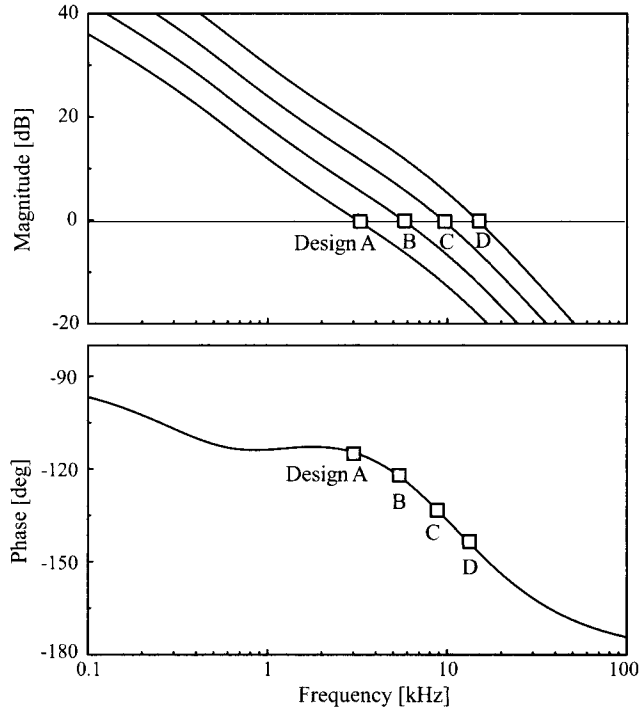


Figure 10.41 Outer loop gain of four different designs.

The outer loop gains of the four designs are shown in Fig. 10.41. As the integrator gain increases, the crossover frequency shifts towards higher frequencies at the expense of the reduction in the phase margin. Figure 10.42 shows the output impedances of the four designs. The output impedance exhibits a peaking at the $T_2(s)$ crossover frequency when the phase margin reduces lower than 60°. Finally, the transient responses due to a series of step load changes, I_O = 4 A ⇒ 8 A ⇒ 4 A, are shown in Fig. 10.43. The output voltage shows an oscillatory behavior for Design C and Design D, where the output impedance reveals a peaking due to the small phase margin. Accordingly, Design A or Design B can be considered acceptable, whose output impedance characteristics belong to Case 1 in the previous analysis.

The control design procedures in Table 10.3 recommended to place the $T_2(s)$ crossover frequency in the range of $\omega_{cr} = (0.3 - 1.0)\,\omega_{esr}$. When the esr zero is sufficiently lower than the switching frequency, ω_{cr} can be placed at ω_{esr}, as is the case with Example 10.8. On the other hand, when ω_{esr} is *not* sufficiently lower than the switching frequency, ω_{cr} should be placed before the esr zero ω_{esr}, for example, $\omega_{cr} = 0.4\,\omega_{esr}$ in Design B in Example 10.13.

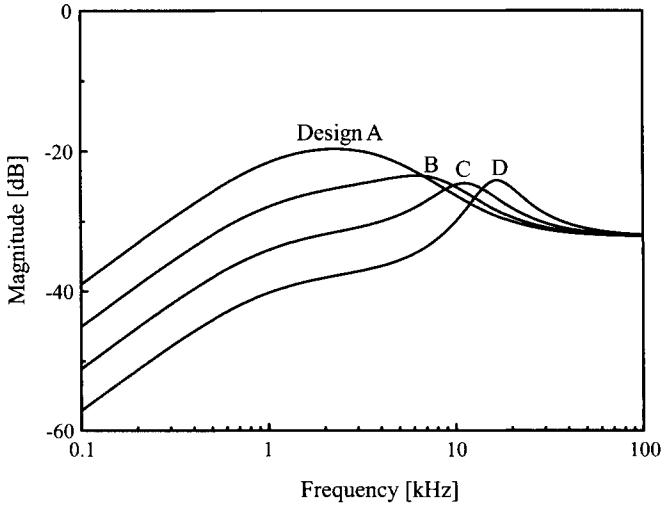


Figure 10.42 Output impedance of four different designs.

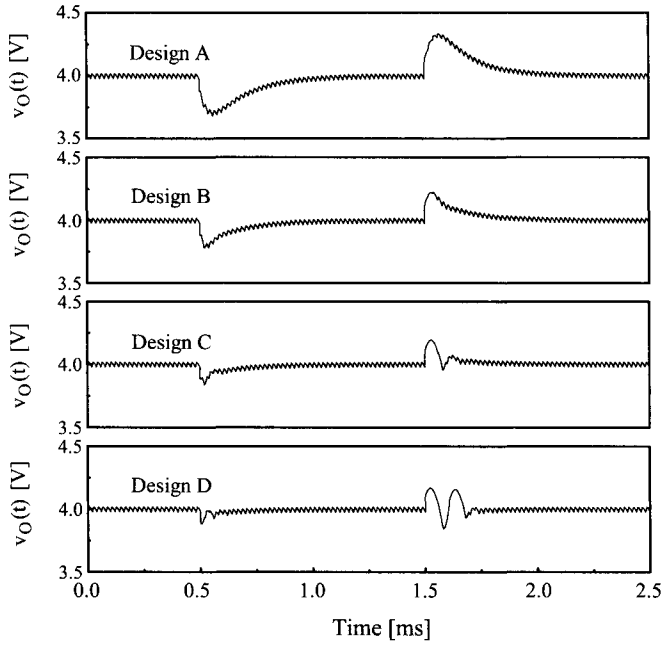


Figure 10.43 Step load response of buck converter with four different designs.

It should be emphasized that the design strategy of $\omega_{cr} = (0.3 - 1.0)\,\omega_{esr}$ only applies to buck converters. For boost and buck/boost converters that have a right-half plane zero (RHP) in their duty ratio-to-output transfer function, other constraints should be considered in determining the $T_2(s)$ crossover frequency. Design considerations for boost and buck/boost converters will be given in Section10.4.

Generalization of Step Load Response

The outcome of the previous step load response analysis can be extended to all dc-to-dc converters in general.

1) The output impedance characteristics for a dc-to-dc converter can be obtained from the small-signal analysis, computational method, or experimental measurement. When the small-signal model of the converter is available, the asymptotic analysis can be employed to obtain the output impedance characteristics. If the small-signal model is not available, either the computational method or the experimental measurement can be used for the acquisition of the output impedance data. The output impedance is displayed in the Bode plot format.

2) The output impedance parameters, required for the step load response analysis, can be extracted from the output impedance plot.

3) The results of the previous section are then adapted to predict the step load response from the output impedance parameters.

The output impedance of practical dc-to-dc converters generally follows the pattern of Case 1 in the previous analysis. For this case, the settling time is given by $t_s = 3/\omega_{zc}$ and peak deviation of the output voltage can be estimated from (10.94). If a more detailed prediction is desired, the expression (10.90) can be used to derive an analytical equation for the output voltage. The resulting equation can be transformed to the output voltage waveform. An example is given below to illustrate the analysis procedures described above.

■ EXAMPLE 10.14 Switched Capacitor Converter Example

This example demonstrates the generality of the step load response analysis. For this purpose, a switched capacitor dc-to-dc converter [10], which performs the dc-to-dc power conversion using only capacitors and switches, is used in this example. Figure 10.44(a) is the output impedance of the switched capacitor converter, which was measured from the experimental converter using an impedance analyzer. The output impedance closely resembles the profile of Case 1, and therefore the corresponding analysis results are applied here.

As shown in Fig. 10.44(a), the major output impedance parameters are measured as $\omega_{zc} = 2\pi \cdot 3 \times 10^3$ rad/s, $|Z_o|_{peak} = -23$ dB, and $|Z_o(j\infty)| = -33$ dB. The output of the converter is regulated at $V_O = 5$ V. Now, a 4 A step decrease

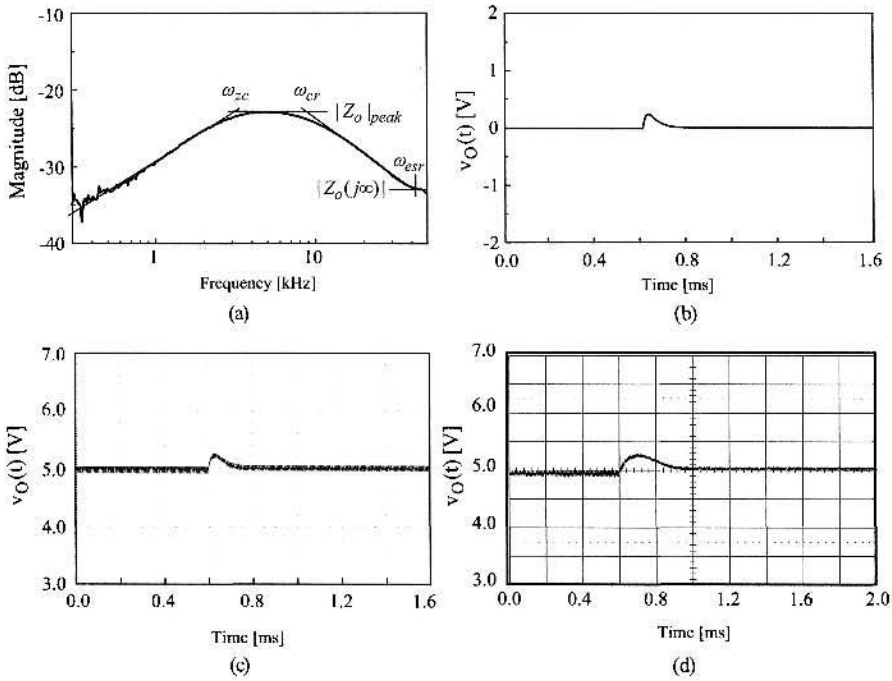


Figure 10.44 Switched capacitor converter example. (a) Output impedance. (b) Prediction of the equation (10.90). (c) Cycle-by-cycle time-domain simulation. (d) Measured step load response.

occurs in the load current, producing a transient response in the output voltage. The settling time of the output voltage is predicted as

$$t_s = \frac{3}{\omega_{zc}} = \frac{3}{2\pi \cdot 3 \times 10^3} = 0.16 \text{ ms}$$

and the peak overshoot is estimated as

$$I_{step} 10^{\frac{|Z_o(j\infty)|}{20}} < v_O(t)_{peak} < I_{step} 10^{\frac{|Z_o(j\omega)|_{peak}}{20}}$$

$$\Rightarrow 4 \cdot 10^{-33/20} < v_O(t)_{peak} < 4 \cdot 10^{-23/20}$$

$$\Rightarrow 0.09 \text{ V} < v_O(t)_{peak} < 0.28 \text{ V}$$

For a more detailed prediction, other output impedance parameters, ω_{cr}, ω_{esr}, and ω_m in Figs. 10.39(a) and 10.44(a), are estimated and the results are

put into (10.90) to obtain an analytical equation for $v_O(t)$. Figure 10.44(b) is the plot of the resulting equation.

The predictions of the step load response analysis are compared with both the exact time-domain simulation and experimental data. Figure 10.44(c) is the step load response generated from an exact cycle-by-cycle time-domain simulation. Finally, Fig. 10.44(d) is the step load response measured from the experimental switched capacitor converter. The close correlation and resemblance among the output impedances and step load responses, obtained from analysis, simulation, and measurement, confirm the generality and accuracy of the step load response analysis.

10.4 CURRENT MODE CONTROL FOR BOOST AND BUCK/BOOST CONVERTERS

Chapter 8 demonstrated that voltage mode control is not suitable for the converters that have the right-half plane (RHP) zero in their power stage transfer function, such as the boost converter, the buck/boost converter, and all other isolated PWM converters derived from these two converters. Accordingly, current mode control can be a candidate for the control scheme of these converters. This section presents the feedback design and dynamic analysis of the peak current mode control adapted to the dc-to-dc converters with the RHP zero. A boost converter is used as an example to address the impact of the RHP zero on the control design and closed-loop performance.

10.4.1 Stability Analysis and Control Design

Figure 10.45 shows the circuit diagram and small-signal model of a boost converter employing the peak current mode control. From the small-signal model in Fig. 10.45(b), the duty ratio-to-output transfer function is derived as

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = K_{vd}\frac{\left(1 - \dfrac{s}{\omega_{rhp}}\right)\left(1 + \dfrac{s}{\omega_{esr}}\right)}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{10.96}$$

and the duty-ratio-to-inductor current transfer function is given by

$$G_{id}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = K_{id}\frac{1 + \dfrac{s}{\omega_{id}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{10.97}$$

The expressions for the dc gain, corner frequencies, and damping factor of the transfer functions are given in Table 10.2. Figure 10.46 shows the asymptotic plot of the duty ratio-to-output transfer function, $G_{vd}(s)$, and voltage loop, $T_v(s) = G_{vd}(s)F_v(s)F'_m$, of

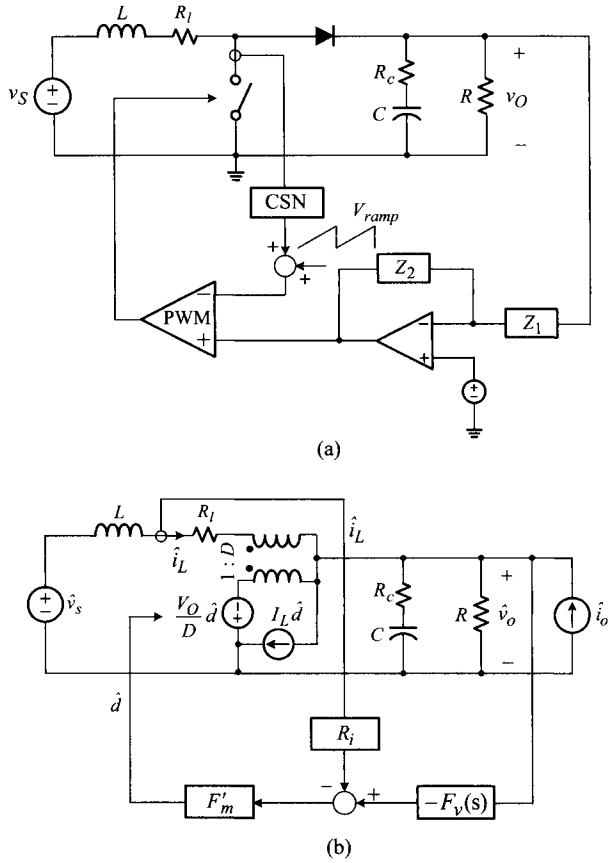


Figure 10.45 Boost converter with peak current mode control. (a) Circuit diagram. (b) Small-signal model.

the boost converter which adopts the two-pole one-zero compensation. This example assumes that the RHP zero comes before the esr zero, $\omega_{rhp} < \omega_{esr}$. According to the control design guidelines, the voltage feedback compensation parameters are selected as $\omega_{pc} = \omega_{rhp}$ and $\omega_{zc} < \omega_o$, resulting in the asymptotic plot shown in Fig. 10.46.

With the compensation pole ω_{pc} located at the RHP zero ω_{rhp}, the phase of the voltage loop drops by $-180°$ over ω_{rhp}. The 90° phase delay caused by ω_{rhp} is augmented by the additional 90° phase drop incurred by ω_{pc}, resulting in a $-180°$ change in $\angle T_v$ while $|T_v|$ stays in a -40 dB/dec slope. These phase characteristics are very unfavorable, mainly staying less than $-180°$ for the frequencies after the power stage double pole, ω_o. In particular, $\angle T_v$ drops to $-270°$ at ω_{rhp}, as illustrated in Fig. 10.46.

Figure 10.47 shows the asymptotic plots for the current loop $|T_i|$, voltage loop $|T_v|$, and overall loop gain $|T_1|$. In order to elucidate the impact of the RHP zero

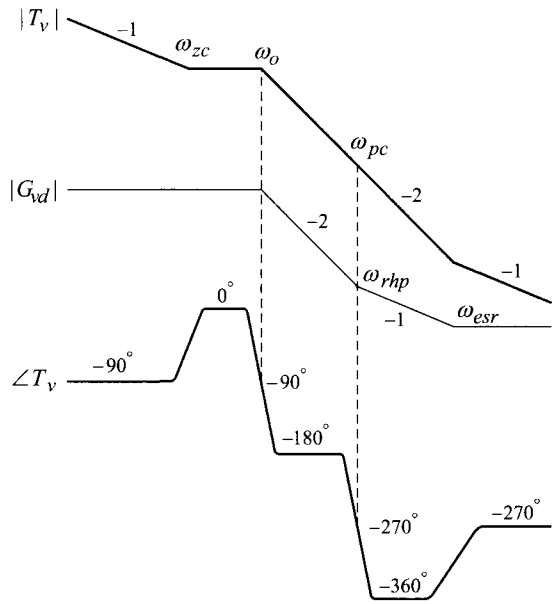


Figure 10.46 Asymptotic plots for duty ratio-to-output transfer function $G_{vd}(s)$ and voltage loop $T_v(s)$.

on stability, it is assumed that $|T_v| = |T_i|$ at ω_{rhp} in Fig. 10.47. In this situation, the overall loop gain at ω_{rhp}, $\vec{T}_1 = \vec{T}_i + \vec{T}_v$, is given by the sum of two equal-length vectors with a 180° phase difference: $\angle T_v = -270° = 90°$ while $\angle T_i = -90°$. Thus, $|T_1|$ dips down to negative infinity and $\angle T_1$ drops rapidly at ω_{rhp}. This implies that the converter is unstable with a negative phase margin.

■ EXAMPLE 10.15 Instability with Condition $|T_v| = |T_i|$ at ω_{rhp}

This example illustrates the preceding discussions about instability. Figure 10.48 shows the Bode plots of $T_v(s)$, $T_i(s)$, and $T_1(s)$ of a boost converter which employs the two-pole one-zero compensation with the condition $|T_i| = |T_v|$ at ω_{rhp}. The overall loop gain reveals the dip in $|T_1|$ and sudden drop in $\angle T_1$ at the frequencies where $|T_v| \approx |T_i|$, thus confirming the converter is unstable.

The previous analysis indicates that, for stability, the frequency at which $|T_v| = |T_i|$ should occur well before the RHP zero. The frequency where $|T_v| = |T_i|$ is the crossover frequency of the outer loop gain $T_2(s)$, previously denoted as ω_{cr}. Accordingly, the $T_2(s)$ crossover frequency ω_{cr} should be placed prior to the RHP zero ω_{rhp}.

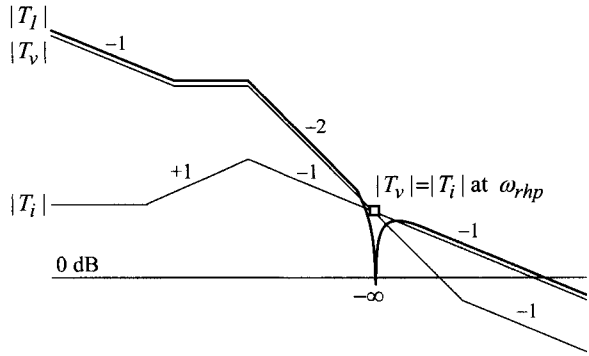


Figure 10.47 Individual feedback loops and overall loop gain with $|T_i| = |T_v|$ at ω_{rhp}.

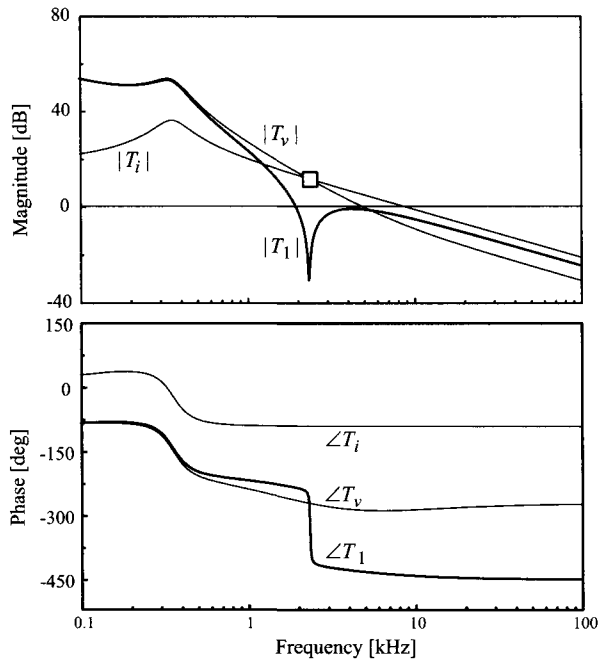


Figure 10.48 Individual feedback loops and overall loop gain with $|T_i| = |T_v|$ at ω_{rhp}.

Figure 10.49 shows the asymptotic plots for $|T_v|$, $|T_i|$, $|T_2|$, and $\angle T_2$ under the assumption that $\omega_{cr} < \omega_{rhp}$. As shown in Fig. 10.49, the phase of $T_2(s)$ at ω_{rhp} becomes $\angle T_2 = \angle T_v - \angle T_i = -270° - (-90°) = -180°$. This also validates the requirement of $\omega_{cr} < \omega_{rhp}$ for an acceptable phase margin at ω_{cr}. In the previous design procedures, it was recommended that $\omega_{cr} = (0.1-0.3)\omega_{rhp}$ for boost and buck/boost converters.

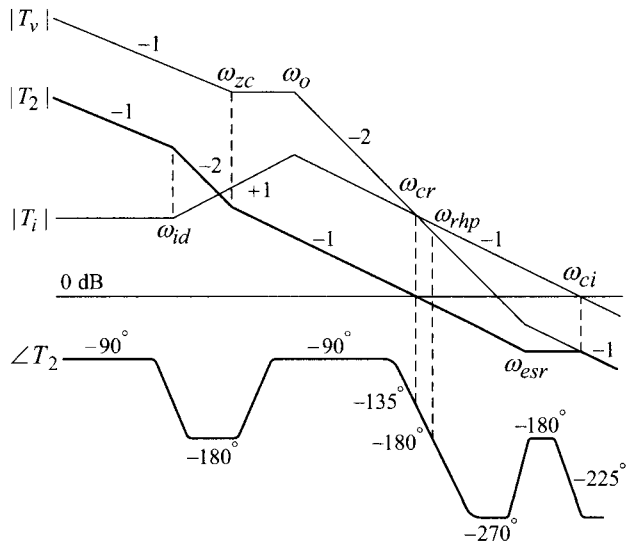


Figure 10.49 Individual feedback loops and outer loop gain with $\omega_{cr} < \omega_{rhp}$.

The control design procedures established in the previous section are still applicable to the dc-to-dc converters with an RHP zero in their power stage transfer function. The same two-pole one-zero compensation is applied for the voltage feedback compensation. As one critical design constraint, the integrator gain should be selected to place the crossover frequency of the outer loop gain $T_2(s)$ in the range of $\omega_{cr} = (0.1-0.3)\,\omega_{rhp}$.

■ EXAMPLE 10.16 Current Mode Control for Boost Converter

This example illustrates the design and performance of the peak current mode control adapted to a boost converter. Figure 10.50 shows the circuit diagram of a boost converter which employs the peak current mode control. The output voltage is regulated at $V_O = V_{ref}(1 + R_1/R_x) = 4\,(1 + 4) = 20$ V with the input voltage $V_S = 12$ V. From the power stage circuit parameters and operating conditions, the corner frequencies and dc gains of the power stage transfer functions are determined as

$$\frac{V_O}{V_S} = \frac{1}{1-D} = \frac{20}{12} \quad \Rightarrow \quad D = 0.4$$

$$\omega_o = \frac{1-D}{\sqrt{LC}} = \frac{1-0.4}{\sqrt{160\times10^{-6}\,470\times10^{-6}}} = 2\pi\cdot 348 \text{ rad/s}$$

$$\omega_{rhp} = \frac{(1-D)^2R}{L} = \frac{(1-0.4)^2 5}{160\times10^{-6}} = 2\pi\cdot 1.79\times10^3 \text{ rad/s}$$

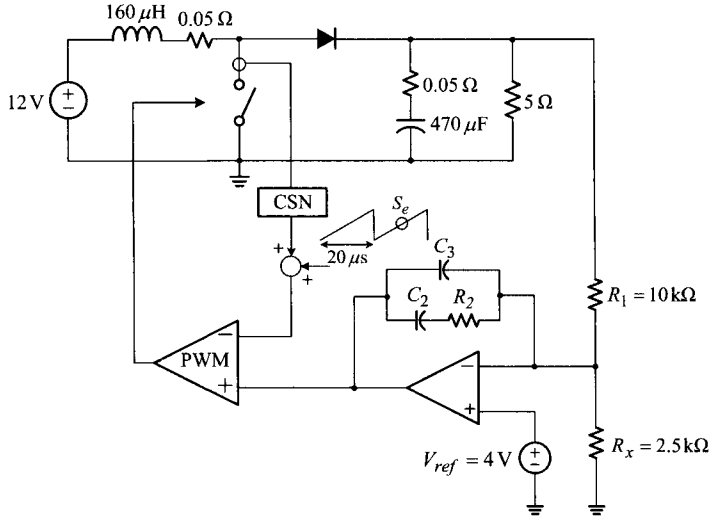


Figure 10.50 Current-mode controlled boost converter: $R_i = 0.67$, $S_e = 7.49 \times 10^4$ V/s, $R_2 = 19.6$ kΩ, $C_2 = 29.2$ nF, and $C_3 = 5.38$ nF.

$$\omega_{esr} = \frac{1}{CR_c} = \frac{1}{470 \times 10^{-6}\, 0.05} = 2\pi \cdot 6.77 \times 10^3 \text{ rad/s}$$

$$K_{vd} = \frac{V_S}{(1-D)^2} = \frac{12}{(1-0.4)^2} = 33.3$$

$$\omega_{id} = \frac{2}{CR} = \frac{2}{470 \times 10^{-6}\, 5} = 2\pi \cdot 135 \text{ rad/s}$$

$$K_{id} = \frac{2V_S}{(1-D)^3 R} = \frac{2 \cdot 12}{(1-0.4)^3\, 5} = 22.2$$

The switching frequency of the converter is $\omega_s = 2\pi \cdot 50 \times 10^3$ rad/s. The maximum input voltage of the PWM block is $V_{max} = 5.0$ V and the peak value of the inductor current is calculated as

$$\begin{aligned} i_{L\,peak} &= \frac{V_O}{(1-D)R} + \frac{1}{2}\frac{V_S}{L}DT_s \\ &= \frac{20}{(1-0.4)5} + \frac{1}{2}\frac{12}{160 \times 10^{-6}} 0.4 \cdot 20 \times 10^{-6} = 6.97 \text{ A} \end{aligned}$$

Now the control design is performed based on the proposed design procedures.

Current Loop Design

1) T_i crossover frequency: $\omega_{ci} = 0.16\,\omega_s = 2\pi \cdot 8 \times 10^3$ rad/s

2) Dc gain of T_i:

$$K_i = \frac{\omega_{id}\,\omega_{ci}}{\omega_o^2} = \frac{(2\pi \cdot 135)(2\pi \cdot 8 \times 10^3)}{(2\pi \cdot 348)^2} = 8.92$$

3) CSN gain:

$$R_i < \frac{V_{max}}{i_{L\,peak}} = \frac{5.0}{6.97} = 0.72 \quad \Rightarrow R_i = 0.67$$

4) Modulator gain:

$$F'_m = \frac{K_i}{K_{id} R_i} = \frac{8.92}{22.2 \cdot 0.67} = 0.60$$

5) Compensation ramp:

$$\begin{aligned} S_e &= \frac{1}{T_s F'_m} + \frac{S_f - S_n}{2} \\ &= \frac{1}{20 \times 10^{-6}\,0.60} + \frac{\dfrac{20-12}{160 \times 10^{-6}}\,0.67 - \dfrac{12}{160 \times 10^{-6}}\,0.67}{2} \\ &= 7.50 \times 10^4 \text{ V/s} \\ V_m &= S_e T_s = (7.50 \times 10^4)(20 \times 10^{-6}) = 1.50 \text{ V} \end{aligned}$$

Voltage Loop Design

1) Compensation pole: $\omega_{pc} = \omega_{rhp} = 2\pi \cdot 1.79 \times 10^3$ rad/s

2) Compensation zero: $\omega_{zc} = 0.8\,\omega_o = 0.8\,(2\pi \cdot 348) = 2\pi \cdot 278$ rad/s

3) T_2 crossover frequency: $\omega_{cr} = 0.28\,\omega_{rhp} = 0.28\,(2\pi \cdot 1.79 \times 10^3)$
$= 2\pi \cdot 501$ rad/s

4) Integrator gain:

$$\begin{aligned} K_v &= \frac{K_{id}\,\omega_{cr}\,R_i\,\omega_{zc}}{\omega_{id}\,K_{vd}} \\ &= \frac{22.2\,(2\pi \cdot 501)\,0.67\,(2\pi \cdot 278)}{(2\pi \cdot 135)\,33.3} \\ &= 2.90 \times 10^3 \end{aligned}$$

5) Voltage feedback circuit: $R_1 = 10$ kΩ
$\Rightarrow R_2 = 19.6$ kΩ, $C_2 = 29.2$ nF, and $C_3 = 5.38$ nF

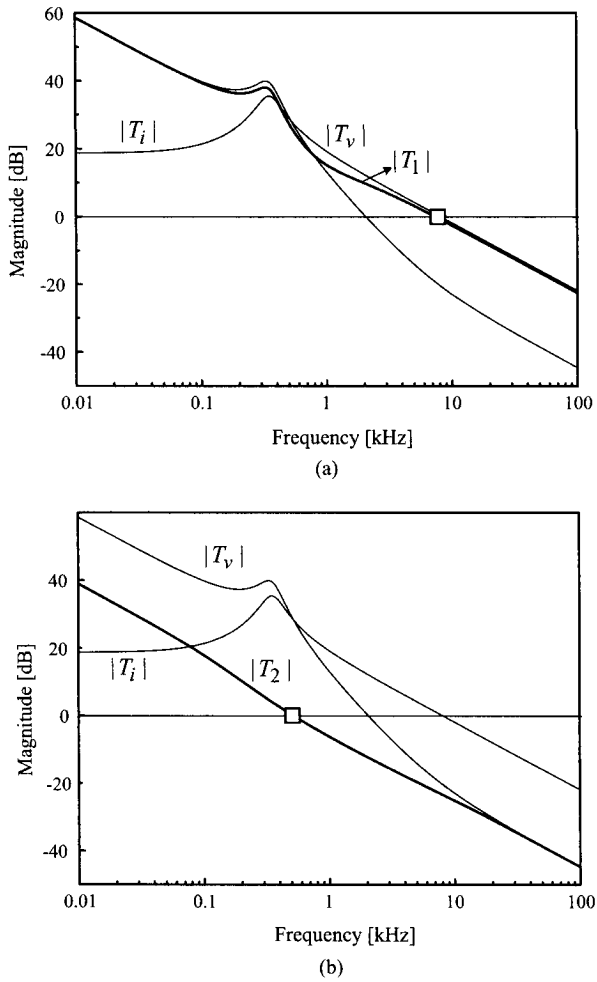


Figure 10.51 Individual feedback loops and system loop gains. (a) Overall loop gain $T_1(s)$. (b) Outer loop gain $T_2(s)$.

Figure 10.51 shows the Bode plots of the individual feedback loops and system loop gains. Figure 10.51(a) reveals that the crossover frequency of $T_1(s)$ is precisely located at the target frequency, $\omega_{ci} = 2\pi \cdot 8.0 \times 10^3$ rad/s. The crossover frequency of $T_2(s)$ is also placed at the exact design goal of $\omega_{cr} = 2\pi \cdot 501$ rad/s. Figure 10.52 compares the Bode plots of $T_1(s)$ and $T_2(s)$. The two loop gains have different phase and gain margins. The overall loop gain T_1 has a 90° phase margin and an ∞ dB gain margin. In contrast, the phase margin of T_2 is only 45° and its gain margin is merely 11 dB.

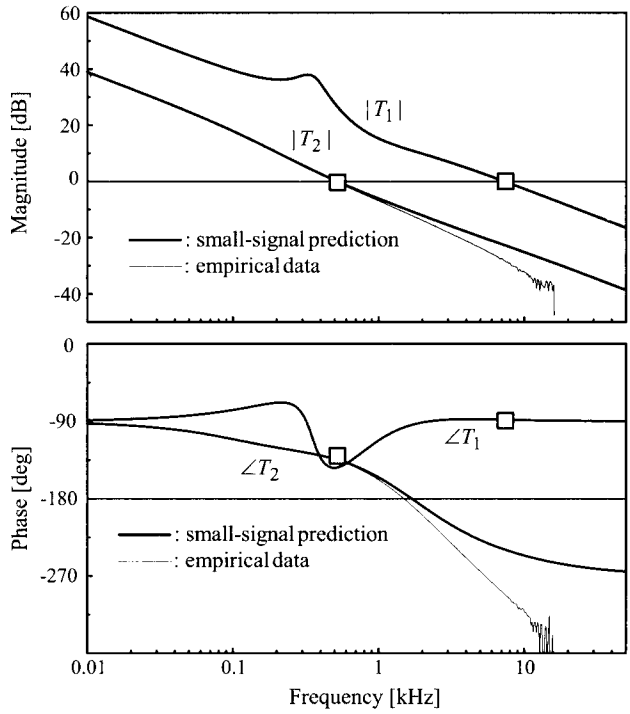


Figure 10.52 Comparison between overall loop gain $T_1(s)$ and outer loop gain $T_2(s)$.

As addressed in Section 10.2.3, the implications of the stability margins of the two loop gains are very different. For the overall loop gain, $T_1(s) = T_i(s) + T_v(s)$, the stability margins are defined for the sum of the two individual feedback loops. The ∞ dB gain margin implies that the converter never becomes unstable, as far as $|T_v|$ and $|T_i|$ are *simultaneously* increased, regardless of the amount of increase. However, this information is not very useful for the control design purpose because we do not increase $|T_v|$ and $|T_i|$ at the same time. Instead, $|T_i|$ is first fixed and $|T_v|$ is later adjusted for a design trade-off.

The stability margin of the outer loop gain $T_2(s) = T_v(s)/(1 + T_i(s))$ is directly related with the voltage feedback compensation. In the control design, most control parameters are routinely determined and, at the final stage, the integrator gain K_v is calibrated for design refinement. The stability margins of $T_2(s)$ provide straightforward and explicit information about this design optimization. For example, the gain margin of 11 dB indicates that the converter becomes unstable when K_v is increased more than the factor of $10^{11/20} = 3.54$. This information is critical when increasing the integrator gain to improve the closed-loop performance.

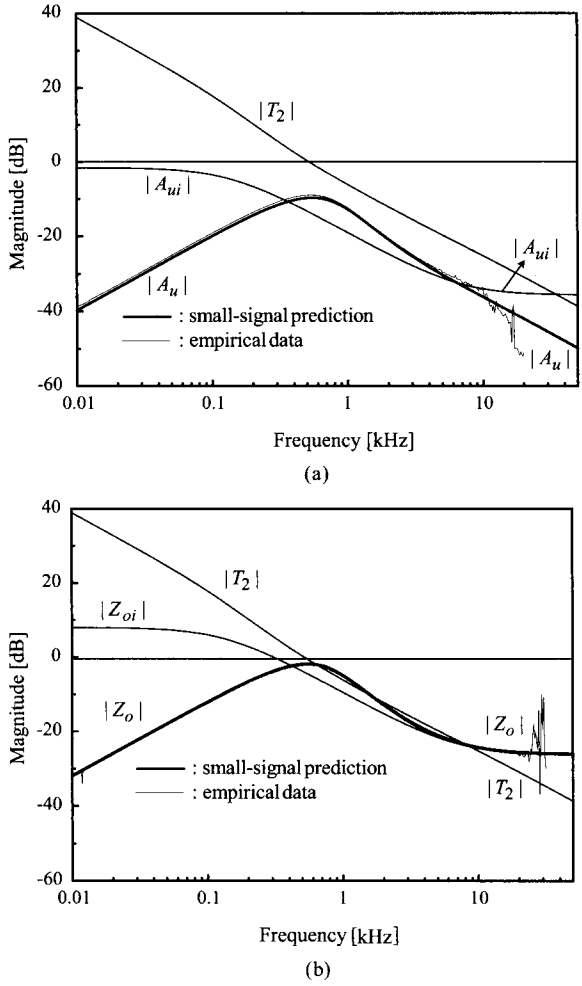


Figure 10.53 Frequency-domain performance. (a) Audio-susceptibility. (b) Output impedance.

The audio-susceptibility and output impedance characteristics are displayed in Fig. 10.53. Referring to Section 10.3.1, the audio-susceptibility is approximately given by

$$A_u(s) = \frac{A_{ui}(s)}{1 + T_2(s)} \approx \frac{\dfrac{1}{2(1-D)} \dfrac{1 + sCR_c}{1 + sC(R + R_c)/2}}{1 + T_2(s)} \tag{10.98}$$

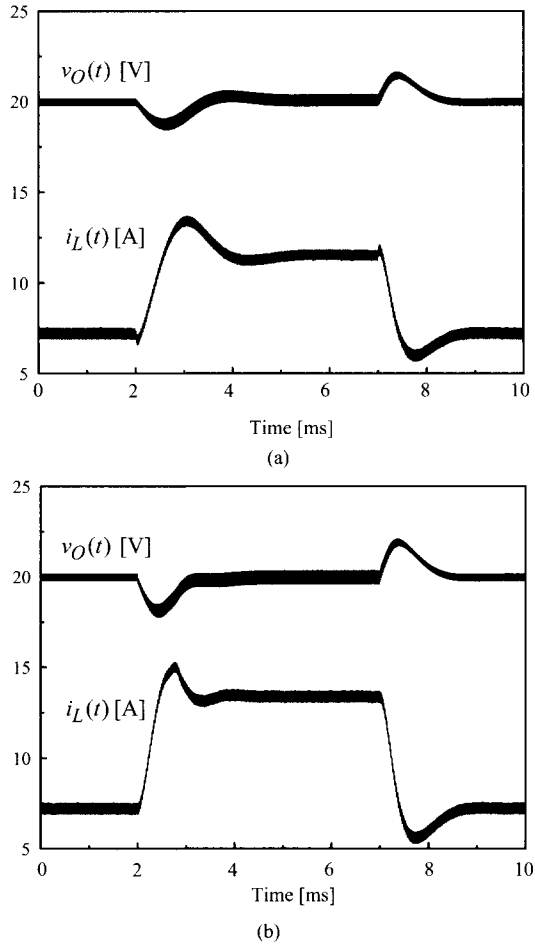


Figure 10.54 Transient response. (a) Step input response. (b) Step load response.

Figure 10.53(a) shows $|A_{ui}|$, $|T_2|$, and $|A_u|$. As addressed in Section 10.3.1, the relationship (10.98) is only valid up to mid frequencies and $|A_u|$ follows $|G_{vs}|$ at high frequencies.

The output impedance is approximated as

$$Z_o(s) = \frac{Z_{oi}(s)}{1 + T_2(s)} \approx \frac{\dfrac{R}{2}\dfrac{1 + sCR_c}{1 + sC(R + R_c)/2}}{1 + T_2(s)} \tag{10.99}$$

Figure 10.53(b) shows $|Z_{oi}|$, $|T_2|$, and $|Z_o|$. The first pole and peak value of the output impedance are predicted from Fig. 10.53(b) as $\omega_{zc} = 2\pi \cdot 400$ rad/s

and $|Z_o|_{peak} = -2$ dB. This information will be used to predict the step load response of the output voltage.

The step input response and step load response are shown in Fig. 10.54. Figure 10.54(a) is the transient response of the output voltage due to the step changes of $V_S = 12\text{ V} \Rightarrow 8\text{ V} \Rightarrow 12\text{ V}$ in the input voltage. Finally, Fig. 10.54(b) shows the output voltage waveform in response to the step changes of $I_O = 4\text{ A} \Rightarrow 7\text{ A} \Rightarrow 4\text{ A}$ in the load current. The settling time of the output voltage is predicted as

$$t_s = \frac{3}{\omega_{zc}} = \frac{3}{2\pi \cdot 400} = 1.19\text{ ms}$$

The upper limit of the output voltage deviation is predicted as

$$v_O(t)_{peak} < I_{step}\, 10^{|Z_o|_{peak}/20} = 3 \cdot 10^{-2/20} = 2.38\text{ V}$$

10.4.2 Loop Gain Analysis

In the previous control design procedures, all the control parameters are systematically selected based on the power stage parameters and operational conditions. However, the integrator gain is often lastly tuned for optimal closed-loop performance. Accordingly, it would be informative to investigate the behavior of the overall loop gain and outer loop gain when the integrator gain varies. This would provide insights about the implication and characteristics of the two loop gains, as well as the overall dynamics of multi-loop controlled converter systems.

■ **EXAMPLE 10.17 Loop Gain Analysis**

For the loop gain analysis purpose, the boost converter used in Example 10.16 is reintroduced. The overall loop gain and outer loop gain of the boost converter with the integrator gain of $K_v = 2890$ were shown in Fig. 10.52. Now, the integrator gain is successively increased from $K_v = 2890$ to 5780, 9900, and 14560. Figure 10.55 shows the overall loop gain $T_1(s)$ with the four different integrator gains. The overall loop gain exhibits rather complex behavior, demonstrating substantial changes in both magnitude and phase. This complex behavior originates from the location of the integrator gain in the loop gain expression

$$T_1(s) = T_i(s) + T_v(s) = T_i(s) + G_{vd}(s)F_m' \underbrace{\frac{K_v}{s}\frac{1+\dfrac{s}{\omega_{zc}}}{1+\dfrac{s}{\omega_{pc}}}}_{F_v(s)}$$

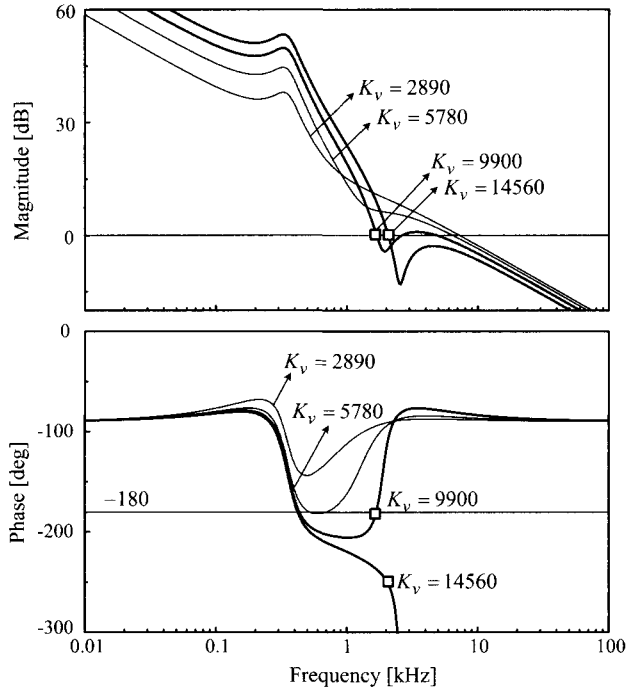


Figure 10.55 Overall loop gains with different integrator gains.

$$= T_i(s) + K_v \left(G_{vd}(s) F'_m \frac{1}{s} \frac{1 + \dfrac{s}{\omega_{zc}}}{1 + \dfrac{s}{\omega_{pc}}} \right) \tag{10.100}$$

The change in K_v affects both the magnitude and phase of the loop gain, because K_v appears as a multiplication factor in the second term only.

Figure 10.56 shows the outer loop gain $T_2(s)$ with the four different integrator gains. In contrast to $T_1(s)$, the outer loop gain shows a linear change in magnitude only, while the phase remains unchanged. This transition pattern can easily be inferred from the $T_2(s)$ expression

$$T_2(s) = \frac{T_v(s)}{1 + T_i(s)} = \frac{G_{vd}(s) F'_m \dfrac{K_v}{s} \dfrac{1 + \dfrac{s}{\omega_{zc}}}{1 + \dfrac{s}{\omega_{pc}}}}{1 + T_i(s)}$$

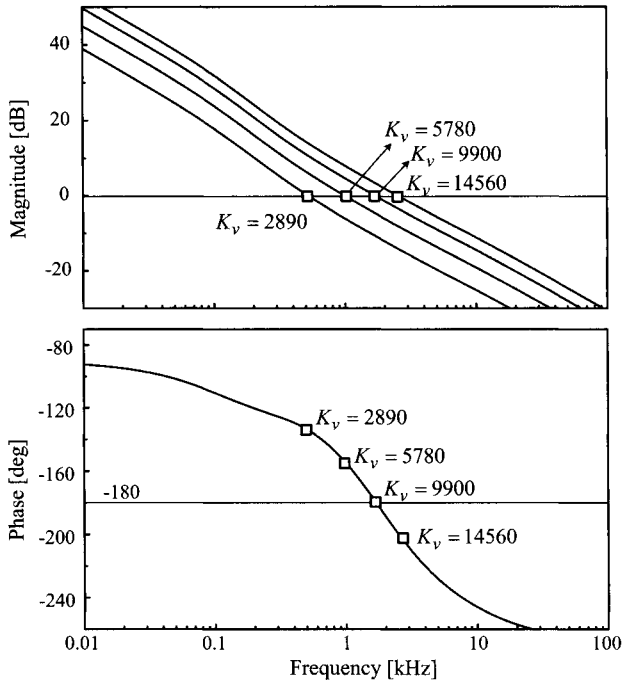


Figure 10.56 Outer loop gains with different integrator gains.

$$= K_v \frac{G_{vd}(s)F'_m \frac{1}{s}\frac{1+\frac{s}{\omega_{zc}}}{1+\frac{s}{\omega_{pc}}}}{1+T_i(s)} \qquad (10.101)$$

Here, the integrator gain K_v is the common multiplication factor in the whole loop gain expression. Thus, K_v linearly increases the magnitude only, without affecting the phase. The original outer loop gain with $K_v = 2890$ exhibits a 11 dB gain margin. Accordingly, the converter is marginally stable with the integrator gain of $K_v = 2890 \cdot 10^{11/20} = 9900$, and becomes unstable for the larger gain, $K_v = 14560$. Figure 10.56 shows an exact match to this analysis.

Although the overall loop gain and outer loop gain show very different stability margins and evolution patterns, they should provide the same information about the absolute stability. As shown in Figs. 10.55 and 10.56, the two loop gains both indicate that the converter is stable with $K_v = 2890$ and 5780, and unstable with $K_v = 14560$.

An important observation is made from the loop gain plots with $K_v = 9900$. The outer loop gain plot in Fig. 10.56 indicates that, when the integrator gain is increased to $K_v = 9900$, the loop gain crosses the 0 dB line at $\omega_{cr} =$

$2\pi \cdot 1.70 \times 10^3$ rad/s with $-180°$ phase angle. This implies

$$T_2(j\omega_{cr}) = \frac{T_v(j\omega_{cr})}{1 + T_i(j\omega_{cr})} = 1\angle -180° = -1 \tag{10.102}$$

with $\omega_{cr} = 2\pi \cdot 1.70 \times 10^3$ rad/s. The above equation is rewritten as

$$1 + \frac{T_v(j\omega_{cr})}{1 + T_i(j\omega_{cr})} = 0 \Rightarrow 1 + T_i(j\omega_{cr}) + T_v(j\omega_{cr}) = 0 \tag{10.103}$$

which also indicates

$$T_1(j\omega_{cr}) = T_i(j\omega_{cr}) + T_v(j\omega_{cr}) = -1 = 1\angle -180° \tag{10.104}$$

Equations (10.102) and (10.104) imply that the overall loop gain and outer loop gain identically predict that the converter is marginally stable with the integrator gain $K_v = 9900$. This information should show up in both the Bode plot and polar plot of the two loop gains.

- The Bode plots of the overall loop gain and outer loop gain both cross the 0 dB line at the frequency $\omega_{cr} = 2\pi \cdot 1.70 \times 10^3$ rad/s with $-180°$ phase angle: $T_1(j\omega_{cr}) = T_2(j\omega_{cr}) = 1\angle -180°$. Figure 10.57 shows the Bode plots

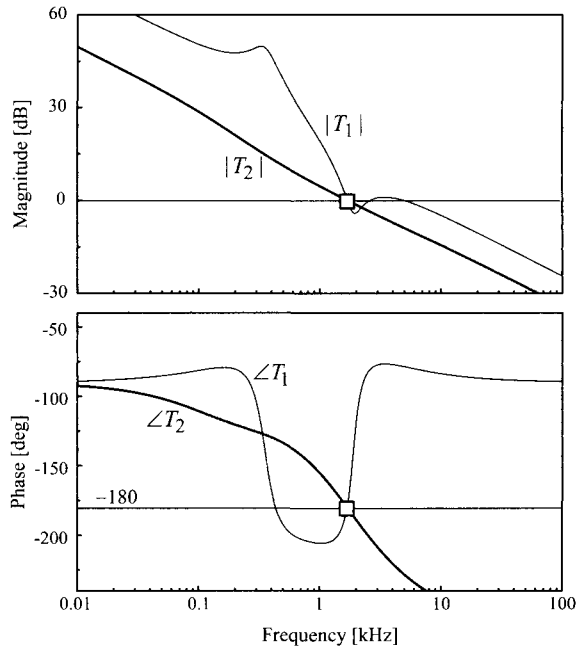


Figure 10.57 System loop gains with $K_v = 9900$.

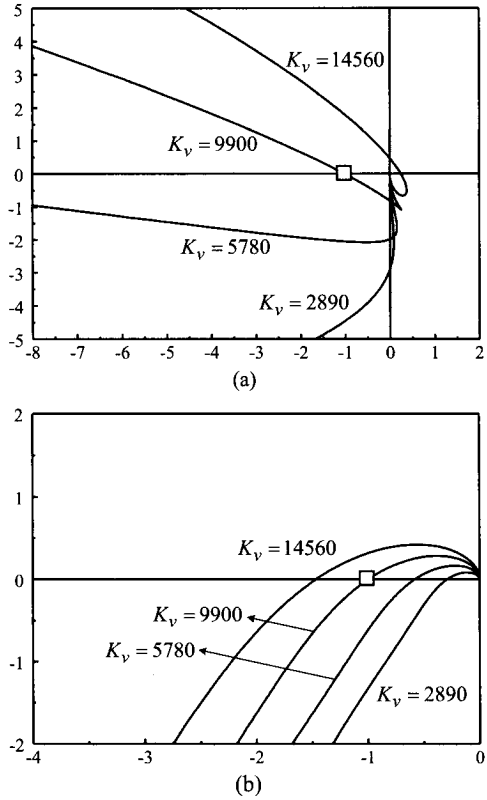


Figure 10.58 Polar plot of loop gains. (a) Overall loop gain. (b) Outer loop gain.

of the two loop gains with $K_v = 9900$. The two loop gains precisely cross the 0 dB line at $\omega_{cr} = 2\pi \cdot 1.70 \times 10^3$ rad/s with a $-180°$ phase angle, thereby confirming that $T_1(j\omega_{cr}) = T_2(j\omega_{cr}) = 1\angle -180°$.

- The polar plots of the two loop gains touch the $(-1, 0)$ point at $\omega_{cr} = 2\pi \cdot 1.70 \times 10^3$ rad/s: $T_1(j\omega_{cr}) = T_2(j\omega_{cr}) = -1$. Figure 10.58 shows the polar plots of the loop gains evaluated with the four different integrator gains. The overall loop gain exhibits a very complex transition pattern, as predicted from (10.100). On the other hand, the polar plot of the outer loop gain expands proportionally as the integrator gain increases. In spite of the very different transition patterns, the polar plots of the two loop gains identically traverse the $(-1, 0)$ point with $K_v = 9900$.

The left-hand side of expression (10.103) also indicates that $\pm\omega_{cr} = \pm 2\pi \cdot 1.70 \times 10^3$ rad/s are the roots of the characteristic equation of the converter.

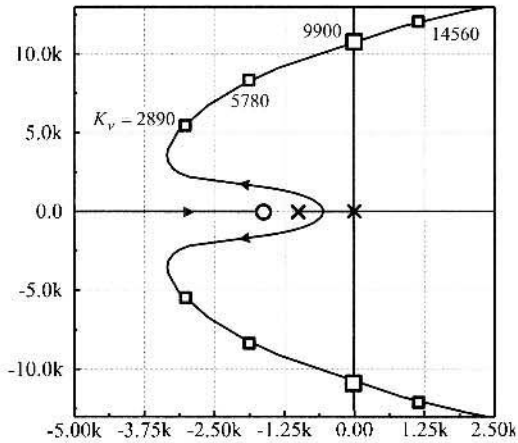


Figure 10.59 Pole trajectory with integrator gain variation.

Thus, a pair of the system poles lie on the imaginary axis when the integrator gain is increased to $K_v = 9900$. Figure 10.59 shows the root locus evaluated with respect to the integrator gain K_v

$$1 + T_2(s) = 1 + K_v \frac{G_{vd}(s)F'_m \dfrac{1}{s} \dfrac{1 + \dfrac{s}{\omega_{zc}}}{1 + \dfrac{s}{\omega_{pc}}}}{1 + T_i(s)} = 0 \tag{10.105}$$

On the root locus plot, the locations of the dominant poles are marked for $K_v = 2890$, 5780, 9900, and $K_v = 14560$. As predicted, a pair of the closed-loop poles indeed cross the imaginary axis with $K_v = 9900$. The crossing points should be $\pm\omega_{cr} = \pm 2\pi \cdot 1.70 \times 10^3$ rad/s $= \pm 1.07 \times 10^4$ rad/s, which are the frequencies that satisfy $1 + T_1(j\omega_{cr}) = 1 + T_2(j\omega_{cr}) = 0$.

10.5 SUMMARY

Current mode control employs an additional feedback from the inductor current on top of the output voltage feedback. Using the two feedback signals, current mode control offers substantial improvements over conventional voltage mode control. Accordingly, modern PWM dc-to-dc converters extensively adapt current mode control. Now, current mode control truly holds the prime position in PWM dc-to-dc power converter control methodologies. This chapter presented a comprehensive analysis and design of current mode control.

Peak current mode control is the most common form of current mode control. The peak current mode control senses the switch current and uses its peak value to execute the PWM function. Since the switch current is the on-time inductor current,

the switch current sensing can be conceptually replaced with the inductor current sensing for the purpose of dynamic analysis and control design. The analysis and design of the peak current mode control are presented using the inductor current sensing.

Current mode control is a multi-loop control scheme in which multiple system loop gains exist in the system. Two particular system loop gains, the overall loop gain and outer loop gain, are identified and utilized for the dynamic analysis. The two loop gains are used, collectively in some cases and individually in other cases, for the analysis and design of current node control. The respective role and implication of the two loop gains are addressed throughout this chapter.

Systematic non-iterative design procedures are formulated for the peak current mode control adapted to all the three basic PWM converters. The current feedback circuit is designed to place the crossover frequency of the overall loop gain at the target frequency. The voltage feedback circuit is constructed using a two-pole one-zero compensation. The compensation parameters are selected for stability and good closed-loop performance. In particular, the integrator gain is determined for the desired location of the crossover frequency of the outer loop gain. Step-by-step design procedures for the three basic PWM converters are given in Table 10.3.

The performance of the peak current mode control adapted to the buck converter and boost converter is analyzed in detail. In particular, the step load response is thoroughly analyzed, leading to a practical method for predicting the transient response of the output voltage from the converter's output impedance characteristics. It was shown that the results of this step load analysis can be extended to all dc-to-dc converters in general. A specific example is given in Example 10.14 where the step load response of a switched capacitor converter is presented.

The use and implication of the overall loop gain and outer loop gain in the stability analysis are demonstrated using a boost converter example. The outward information of the loop gains should be interpreted based on the definition of the corresponding loop gain. Although the two loop gains have utterly different shapes, stability margins, and transition patterns, they provide a coherent message on the internal information about the converter stability. This analysis is covered in Example 10.17.

The analysis presented in this chapter is called the *classical* analysis because the analysis does not include the sampling effects of the peak current mode control and has become less prevalent than the past. A new analysis method that includes the sampling effects has emerged an alternative to the classical analysis. Even so, the classical analysis is still valuable because it duly and *conveniently* describes the major dynamics of current mode control. The next chapter deals with the new analysis to include the sampling effects into the converter dynamics. Whenever appropriate and informative, the results of the new analysis will be compared with those of the current classical analysis.

REFERENCES

1. B. Choi, D. Kim, D. Lee, S. Choi, and J. Sun, "Analysis of input filter interactions in switching power converters," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 452-460, Mar. 2007.
2. D. Kim, B. Choi, D. Lee, and J. Sun, "Dynamics of current-mode controlled dc-to-dc converters with input filter stage," in *Proc. IEEE Power Electron. Specialists' Conf.*, 2005, pp 2648-2656.
3. D. Sable, R. Ridley, and B. Cho, "Comparison of performance of single-loop and current-injection control for PWM converters that operate in both continuous and discontinuous modes of operation," *IEEE Trans. Power Electron.*, vol. 7, no. 1, pp. 136-142, Jan. 1992.
4. L. Dixon, "Average current mode control of switching power supplies," *UNITRODE Power Supply Seminar SEM-700,* 1990.
5. L. Dixon, "Optimizing the design of a high power factor switching regulator," *UNITRODE Power Supply Seminal SEM-700,* 1990.
6. W. Tang, F. C. Lee, R. B. Ridley, and I. Cohen, "Charge control: modeling, analysis, and design," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 396-403, Oct. 1993.
7. F. C. Lee, M. F. Mahmoud, and Y. Yu, *"Design handbook for a standardized control module for dc-to-dc converters,"* vol. I, NASA Contract NAS-3-20102, Apr. 1980.
8. F. C. Lee, Y. Yu, and M. F. Mahmoud, "A unified analysis and design procedure for a standardized control module for dc-dc switching regulators," in *PESC Conf. Rec.*, pp. 284-301, 1979.
9. R. B. Ridley, B. H. Cho, and F. C. Lee, "Analysis and interpretation of loop gains of multi-loop-controlled switching regulator," *IEEE Trans. Power Electron.*, vol. 3, no. 4, pp. 489-498, Oct. 1988. in *PESC Conf. Rec.*, pp. 284-301, 1979.
10. B. Choi and W. Lim, "Control design and closed-loop analysis of a switched-capacitor dc-to-dc converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 37, no. 3, pp. 1099-1107, Jul. 2001.

PROBLEMS

10.1* The current sensing network (CSN) discussed in Example 10.2 is employed in the buck converter operating with the following conditions:

$V_S = 24$ V $\quad V_O = 12$ V $\quad L = 80\,\mu$H $\quad R = 4\,\Omega$

$C = 400\,\mu$F $\quad R_c = 0.01\,\Omega$ $\quad f_s = 50$ kHz

The circuit parameters of the CSN are shown in Fig. P10.1.

a) Sketch the waveforms of the switch current i_Q, sensed voltage signal v_1, and compensation ramp V_{ramp} for the two operational periods. Show the maximum and minimum values of the waveforms.

b) Sketch the composite signal, $V_{ramp} + v_1$, control voltage v_{con}, and PWM output V_{pwm} for the two operational periods, in order to illustrate the waveforms of the peak current mode control.

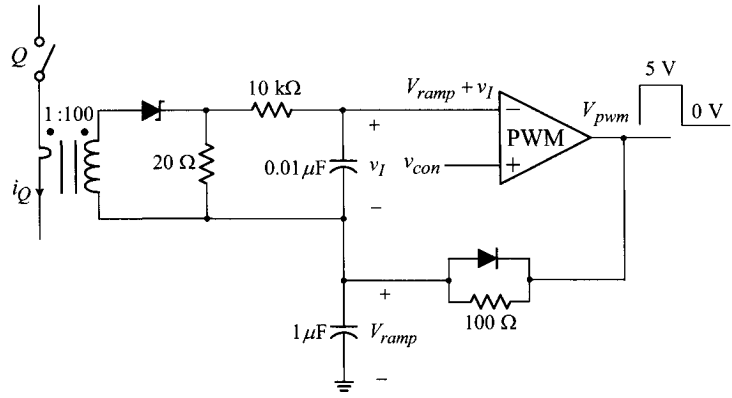


Fig. P10.1

10.2** As discussed in Section 10.2.1, several different expressions for the modulator gain, F'_m, can be formulated, depending on the way of relating the average values of the on-time and/or off-time inductor currents, $\bar{i}_{on}(t)$ and $\bar{i}_{off}(t)$ given below

$$\bar{i}_{on}(t) = v_{con} - S_e dT_s - \frac{1}{2}S_n dT_s$$

$$\bar{i}_{off}(t) = v_{con} - S_e dT_s - \frac{1}{2}S_f(1-d)T_s$$

to the average value of the inductor current, $\bar{i}_L(t)$

a) Show that one modulator gain expression is given by

$$F'_m = \frac{2}{(2S_e + S_n)T_s}$$

by assuming $\bar{i}_L(t) = \bar{i}_{on}(t)$ and linearizing the following equation

$$\bar{i}_L(t) = v_{con} - S_e dT_s - \frac{1}{2}S_n dT_s$$

b) Prove that another modulator gain expression is formulated as

$$F'_m = \frac{2}{(2S_e - S_f)T_s}$$

by linearizing

$$\bar{i}_L(t) = \bar{i}_{off}(t) = v_{con} - S_e dT_s - \frac{1}{2}S_f(1-d)T_s$$

c) Finally, show that the other modulator gain expression is found as

$$F'_m = \frac{1}{S_e T_s}$$

by linearizing the following weighted average of $\bar{i}_{on}(t)$ and $\bar{i}_{off}(t)$

$$\begin{aligned}\bar{i}_L(t) &= d\,\bar{i}_{on}(t) + (1-d)\,\bar{i}_{off}(t) \\ &= v_{con} - S_e dT_s - \frac{1}{2}S_n d^2 T_s - \frac{1}{2}S_f(1-d)^2 T_s\end{aligned}$$

10.3 Derive an exact expression for the duty ratio-to-inductor current transfer function, $G_{id}(s)$, for the buck, boost, and buck/boost converters that contain the parasitics resistance of the reactive components, R_l and R_c in Fig. 10.13. Compare the exact expressions with the approximations given in Table 10.2.

10.4** Figure P10.4 shows the circuit diagram of a current-mode controlled buck converter.

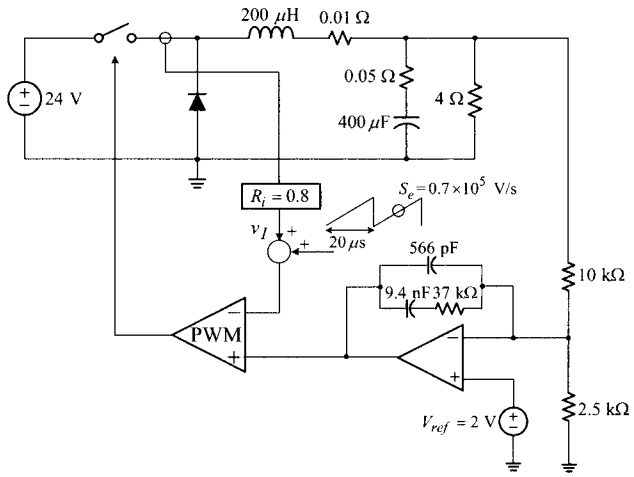


Fig. P10.4

a) Find the expressions for the current loop $T_i(s)$ and voltage loop $T_v(s)$.

b) On semi-log graph paper, sketch the asymptotic plot for $|T_i|$ and $|T_v|$ in order to construct the asymptotic plot for the overall loop gain $|T_1|$ and outer loop gain $|T_2|$. Predict the 0 dB crossover frequency of $T_1(s)$ and $T_2(s)$.

c) Use the results of **b)** to construct the factorized expressions for $T_1(s)$ and $T_2(s)$.

10.5** Shown in Fig. P10.5 is the circuit diagram of a current-mode controlled buck converter.

a) Consider the following power stage parameters and operational conditions for the buck converter:

V_S = 24 V $\quad V_{ref}$ = 2 V $\quad L$ = 80 μH $\quad R_l$ = 0.01 Ω

C = 400 μF $\quad R_c$ = 0.1 Ω $\quad R$ = 2 Ω $\quad R_i$ = 0.5

Determine the slope of the compensation ramp, S_e, to place the 0 dB

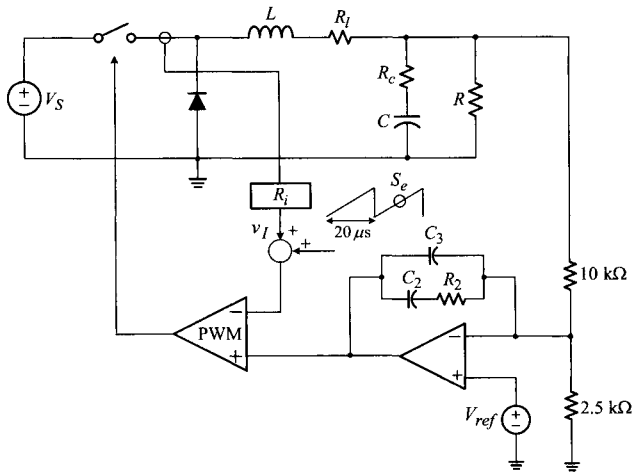


Fig. P10.5

crossover frequency of the current loop at the 20% of the switching frequency, $\omega_{ci} = 0.2\,\omega_s$. Also, determine values for $\{C_2\ R_2\ C_3\}$ to place the 0 dB crossover frequency of the outer loop gain at the esr zero, $\omega_{cr} = \omega_{esr}$. Construct the asymptotic plots for $|T_i|$, $|T_v|$, $|T_1|$, and $|T_2|$ on semi-log graph paper, in order to confirm the compliance with the design requirements.

b) Repeat **a)** for the converter operating with

$V_S = 18$ V $\quad V_{ref} = 1.2$ V $\quad L = 60\,\mu$H $\quad R_l = 0.01\ \Omega$

$C = 600\,\mu$F $\quad R_c = 0.1\ \Omega$ $\quad R = 3\ \Omega$ $\quad R_i = 0.7$

for the design aims of $\omega_{ci} = 0.2\,\omega_s$ and $\omega_{cr} = 0.8\,\omega_{esr}$.

c) Repeat **a)** for the converter operating with

$V_S = 48$ V $\quad V_{ref} = 6$ V $\quad L = 300\,\mu$H $\quad R_l = 0.01\ \Omega$

$C = 600\,\mu$F $\quad R_c = 0.05\ \Omega$ $\quad R = 6\ \Omega$ $\quad R_i = 0.2$

for the design target of $\omega_{ci} = 0.2\,\omega_s$ and $\omega_{cr} = \omega_{esr}$.

10.6** Figure P10.6 shows the four different output impedances of a current-mode controlled PWM converter. For each case, sketch the general profile of the output voltage $v_O(t)$ when a step decrease of $\Delta I_{step} = 5$ A occurs in the load current. Show all the prominent features of $v_O(t)$ including the estimations for the peak overshoot and settling time.

10.7* Shown in Fig. P10.7 are the Bode plots for $|T_i|$, $|T_v|$, $|Z_p|$, and $|G_{vs}|$ of a current-mode controlled buck converter.

a) Construct the asymptotic plot for $|T_1|$, $|T_2|$, $|Z_o|$, and $|A_u|$ on Fig. P10.7.

b) Use the result of **a)** to extract the factorized expressions for $T_1(s)$, $T_2(s)$, $Z_o(s)$, and $A_u(s)$.

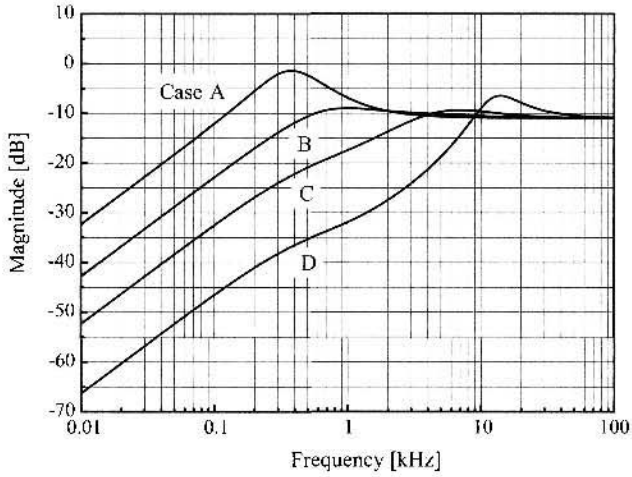


Fig. P10.6

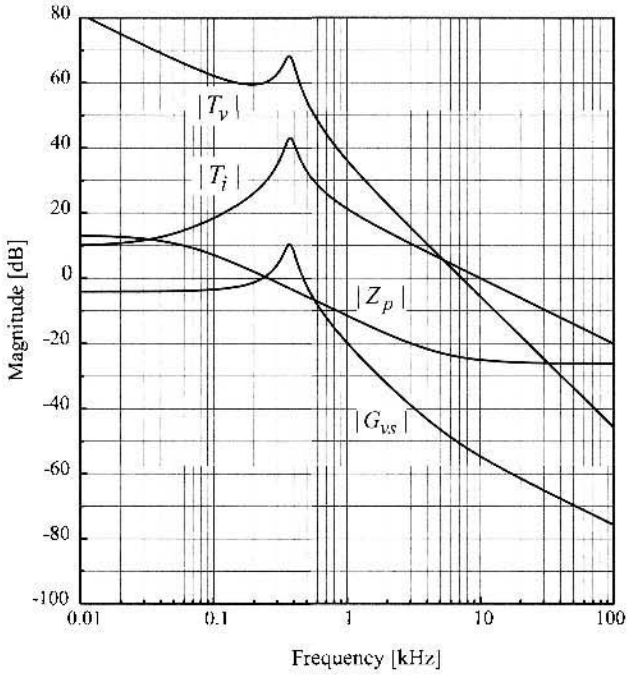


Fig. P10.7

10.8** Perform the asymptotic analysis to evaluate the closed-loop performance of the current-mode controlled buck converter shown in Fig. P10.8.

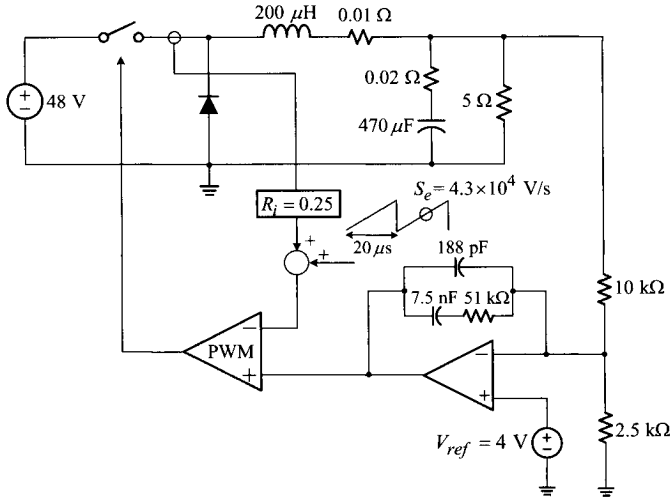


Fig. P10.8

a) Sketch $|T_i|$, $|T_v|$, $|Z_p|$, and $|G_{vs}|$ on semi-log graph paper.

b) Use the results of **a)** to construct the asymptotic plots for $|T_1|$, $|T_2|$, $|Z_o|$, and $|A_u|$.

c) Use the outcomes of **b)** to extract the factorized expressions for $T_1(s)$, $T_2(s)$, $Z_o(s)$, and $A_u(s)$.

10.9* Figure P10.9 shows the circuit diagram of a current-mode controlled boost converter.

a) Find the expressions for the current loop $T_i(s)$ and voltage loop $T_v(s)$.

b) On semi-log graph paper, sketch the asymptotic plots for $|T_i|$ and $|T_v|$ and construct the asymptotic plot for the overall loop gain $|T_1|$ and outer loop gain $|T_2|$. Estimate the 0 dB crossover frequency of the loop gains.

c) Use the results of **b)** to extract the factorized expressions for $T_1(s)$ and $T_2(s)$.

10.10* Shown in Fig. P10.10 is the circuit diagram of a current-mode controlled boost converter.

a) Consider the following circuit parameters and operational conditions for the boost converter:

$V_S = 24$ V $\quad V_{ref} = 9.2$ V $\quad L = 160\,\mu$H $\quad R_l = 0.01\,\Omega$

$C = 400\,\mu$F $\quad R_c = 0.05\,\Omega$ $\quad R = 10\,\Omega$ $\quad R_i = 0.45$

Determine the slope of the compensation ramp, S_e, to place the 0 dB crossover frequency of the current loop at the 20% of the switching frequency, $\omega_{ci} = 0.2\,\omega_s$. Also determine values for $\{C_2\ R_2\ C_3\}$ to place the

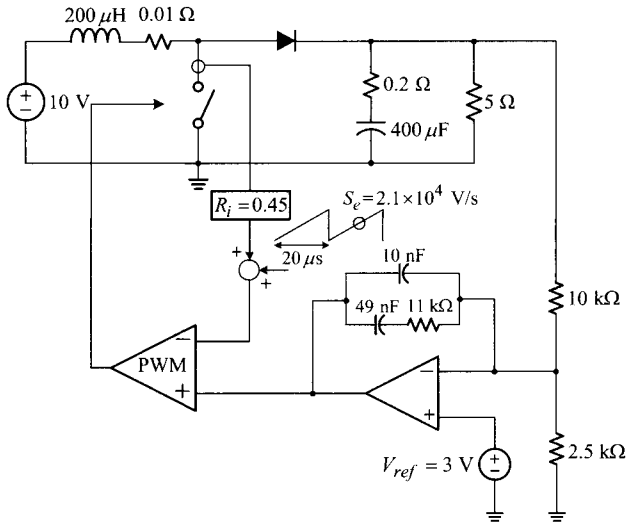


Fig. P10.9

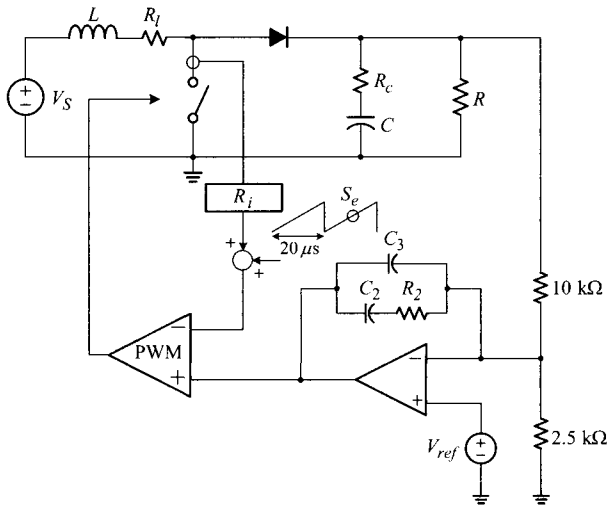


Fig. P10.10

0 dB crossover frequency of the outer loop gain at the 20% of the RHP zero, $\omega_{cr} = 0.2\,\omega_{rhp}$. Construct the asymptotic plots for $|T_i|$, $|T_v|$, $|T_1|$, and $|T_2|$ on semi-log graph paper, in order to confirm the compliance with the design requirements.

b) Repeat **a)** for the converter operating with

$V_S = 30$ V $\quad V_{ref} = 9.6$ V $\quad L = 80\,\mu$H $\quad R_l = 0.01\,\Omega$

$C = 860\,\mu$F $\quad R_c = 0.05\,\Omega$ $\quad R = 10\,\Omega$ $\quad R_i = 0.15$

for the design aims of $\omega_{ci} = 0.2\,\omega_s$ and $\omega_{cr} = 0.15\,\omega_{rhp}$.

c) Repeat **a)** for the converter operating with

$V_S = 12$ V $\quad V_{ref} = 5.6$ V $\quad L = 240\,\mu$H $\quad R_l = 0.01\,\Omega$

$C = 400\,\mu$F $\quad R_c = 0.02\,\Omega$ $\quad R = 2\,\Omega$ $\quad R_i = 0.3$

for the design target of $\omega_{ci} = 0.2\,\omega_s$ and $\omega_{cr} = 0.3\,\omega_{rhp}$.

CHAPTER 11

CURRENT MODE CONTROL — SAMPLING EFFECTS AND NEW CONTROL DESIGN PROCEDURES

Peak current mode control is a sampled-data process because the control action is periodically executed by sampling and holding the error signal produced by the fast-varying inductor current waveform. Due to this feature, current-mode controlled converters exhibit sampled-data system characteristics, which is referred to as the *sampling effects* of current mode control. The dynamics of current-mode controlled converters, at the presence of the sampling effects, can be investigated via sampled-data modeling and z-domain analysis. However, the results would be too complex to expose any easy insights into converter dynamics or design strategy. In fact, several attempts had been made to fully characterize the converter dynamics in terms of z-domain expressions but the outcomes were not widely accepted due to their apparent complexity.

Traditionally, peak current mode control has been analyzed and designed using s-domain techniques, implicitly assuming that the sampling effects simply have negligible consequences. This classical analysis was explored in the previous chapter. It has been proven that the classical analysis duly predicts major dynamics of current mode control and provides correct design procedures for most cases. The classical analysis prevailed until the late 1980s.

Pulsewidth Modulated Dc-to-Dc Power Conversion. By Byungcho Choi

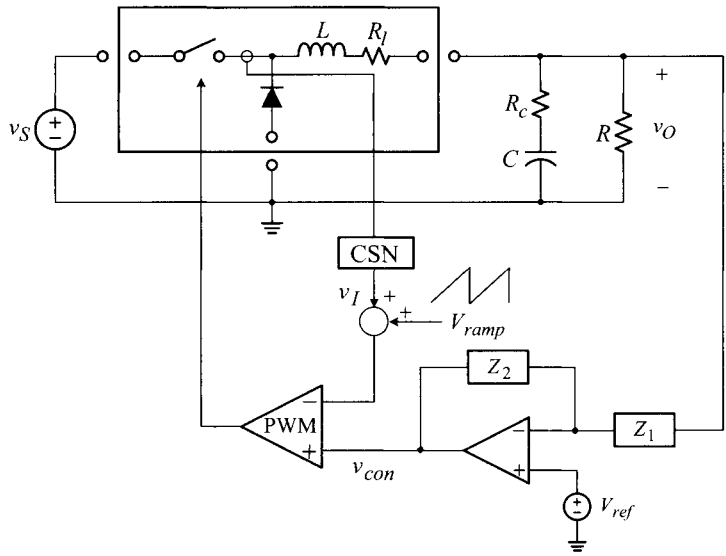


Figure 11.1 Peak current mode control adapted to three basic PWM converters.

In the early 1990s, a new class of dynamic models emerged, which accounts for the sampling effects only using conventional s-domain descriptions. These new models, which are called the *s-domain model for current mode control* in this book, rekindled interest and attention to the sampling effects of current mode control. Using this new s-domain model, several new facets of current mode control are revealed, which supplement and reinforce the outcomes of the earlier classical analysis.

In this chapter, we investigate the sampling effects with the aid of the s-domain model for current mode control. The consequence of the sampling effects on converter dynamics will be studied in detail. Based on the analysis results, new design procedures for current mode control will be developed. The predictions and performance of the new design will be compared and contrasted with those of the classical design, which does not consider the sampling effects. We will explore the correlation between the new design procedures and the classical design procedures. Finally, as a practical application example, the design and evaluation of a flyback converter with an optocoupler-isolated peak current mode control will be discussed.

11.1 SAMPLING EFFECTS OF CURRENT MODE CONTROL

This section presents the origin, nature, and consequence of the sampling effects. It also introduces an s-domain model for current mode control, which will be used in this book to account for the sampling effects.

11.1.1 Origin and Consequence of Sampling Effects

Figure 11.1 shows the peak current mode control adapted to the three basic PWM converters. As discussed in Section 10.2.1, this model could represent each of the three basic converters with the respective connections of the power stage configuration. For peak current mode control, the switch current is sensed with the current sensing network (CSN). As explained in the previous chapter, the switch current sensing is identical to the inductor current sensing, as far as the control mechanism is concerned. For the convenience of graphical illustration and analytical treatment, the peak current mode control is described in terms of the inductor current sensing.

Origin of Sampling Effects

The sampling effects are invoked by the operation of the PWM modulator. The sampling effects of current mode control are investigated using the PWM waveforms shown in Figs. 11.2 and 11.3. Figure 11.2(a) shows the structure and waveforms of the PWM modulator, where the peak current mode control is represented by the inductor current sensing. The CSN gain is assumed unity without loss of generality so $v_I = i_L$ for this case. Figure 11.2(a) is transformed into the equivalent form in Fig. 11.2(b).

The control waveforms in Fig. 11.2(b) are modified into Fig. 11.3, in order to illustrate the evolution of the perturbed inductor current, i'_L, in comparison with the original inductor current i_L. The sampling effects originate from the fact that the control action is periodically executed by sampling and holding the error signal generated by the fast-varying inductor current. The initial perturbation $\hat{\imath}_L(k) = i'_L(k) - i_L(k)$, occurred in the inductor current at the instant of its peak value in the k^{th} period, propagates to ensuing switching periods and generates the continuous error signal, $\hat{\imath}_L(t) = i'_L(t) - i_L(t)$. During the $(k + 1)^{th}$ period, the error signal is sampled at the moment when i'_L intersects with the composite signal, $v_{con} - V_{ramp}$. The sampled error signal $\hat{\imath}_L(k + 1)$ is held constant until the next sampling instant. The PWM modulator samples and holds the error signal in synchronization with the switching period. The $\hat{\imath}^*_L(t)$ at the bottom of Fig. 11.3 is a conceptual representation of the sampled-and-held error signal in the PWM modulator.

Consequence of Sampling Effects

The sampling effects penetrate into the converter dynamics and induce phenomena that the classical analysis is unable to predict. The sampling effects are mainly pronounced at higher frequencies, near or above the half the switching frequency, because the PWM modulator samples and holds the error signal at the rate of the switching frequency.

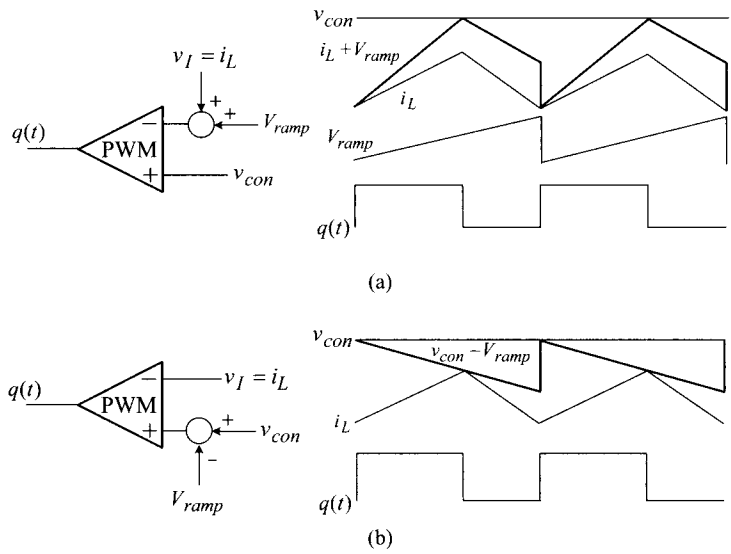


Figure 11.2 Structure and waveforms of peak current mode control. (a) Peak current mode control with unity inductor current sensing. (b) Alternative representation.

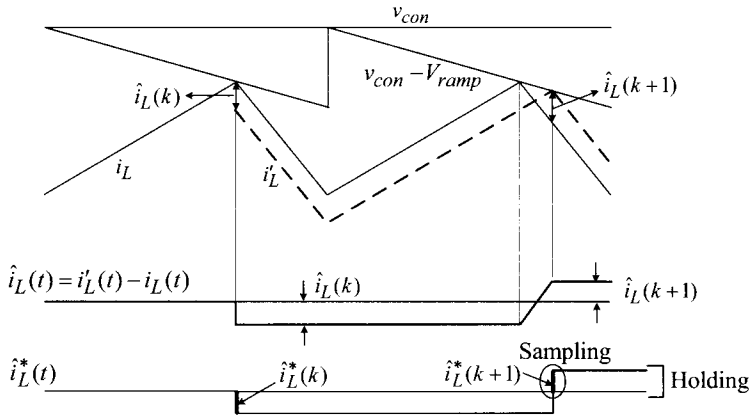


Figure 11.3 Evolution of perturbed inductor current.

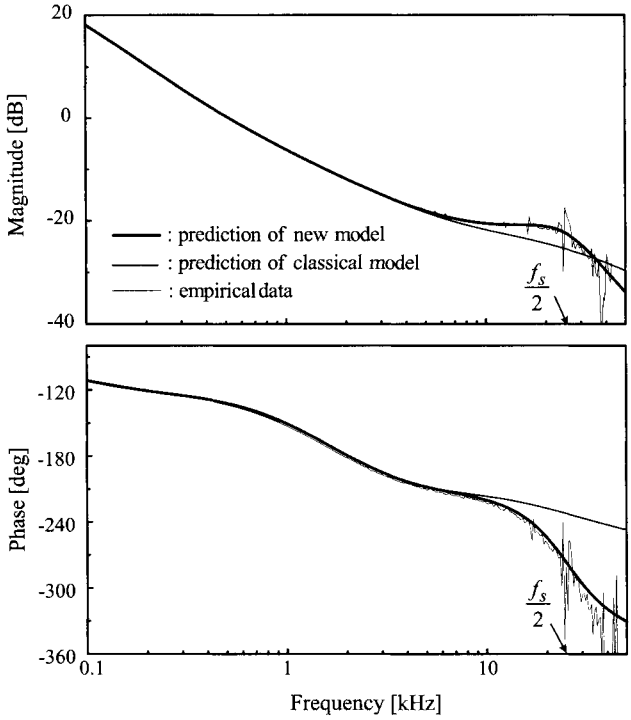


Figure 11.4 Loop gain of boost converter.

■ EXAMPLE 11.1 Consequence of Sampling Effects

This example demonstrates the consequence of the sampling effects on the loop gain characteristics. Figure 11.4 shows the Bode plots of the loop gain of a current-mode controlled boost converter, obtained from two different dynamic models. The thin curve is the prediction of the classical analysis that does not consider the sampling effects. The thick curve is the outcome of the new model that will be developed in this chapter to account for the sampling effects. Along with the model predictions, the empirical loop gain curve obtained using the computational method is also shown in Fig. 11.4. The switching frequency of the converter is f_s = 50 kHz. The loop gain plots do not show any noticeable differences at low frequencies. However, they exhibit notable deviations at high frequencies, particularly in the frequencies around and above half the switching frequency, $f_s/2$ = 25 kHz. Apparently, the new model better correlates with the empirical data in both the magnitude and phase characteristics. The improved accuracy of the new model is a direct consequence of including the sampling effects of current mode control. Detailed discussions about the consequence of the sampling effects will be given in Sections 11.2.3 and 11.3.

11.1.2 Modeling Methodology for Sampling Effects

In current-mode controlled PWM converters, the circuit variables are classified into two categories: the slow-varying variable and fast-varying variable. The output voltage and control voltage are smoothly-filtered slow-varying variables. In contrast, the inductor current is a triangular-shaped fast-varying variable.

The sampling effects are discrete-time phenomena which need to be investigated via sampled-data modeling and z-domain analysis. The sampling effects are initially invoked by the fast-varying inductor current, and therefore the sampled-data modeling needs to be applied to the inductor current feedback circuit. On the other hand, it is unnecessary to apply the sampled-data modeling for the remaining part of the converter circuit, where only the slow-varying circuit variables prevail. For this part, the discrete-time analysis will not yield much different results from those of the classical analysis based on the averaging method. In fact, voltage mode control is also a sampled-data process in the sense that the duty ratio is only updated once in every switching period. Nonetheless, the averaging method offers sufficient accuracy because all the circuit variables involved with the PWM process vary slowly.

One effective modeling methodology for current mode control is to utilize the existing s-domain models as much as possible and to make only necessary modifications or additions to accommodate the sampling effects. In this practice, the sampling effects are first modeled as a discrete-time process and the resulting z-domain model is later transformed into an *equivalent s-domain representation*. The equivalent s-domain representation is then amalgamated with the existing s-domain models for slow-varying circuit variables. The final s-domain model for the entire converter provides both the simplicity of s-domain analysis and the accuracy of sampled-data analysis. The s-domain converter model accepts all the classical analysis techniques and provides the results in s-domain expressions. The analysis results will be accurate up to the Nyquist frequency, i.e., half the switching frequency of the converter, because the model duly accounts for the sample and hold function of the peak current mode control.

11.1.3 Feedforward Gains

In addition to the sampling effects, there exists another mechanism that needs to be considered in analyzing current mode control, but is not included in the classical analysis. In peak current mode control, the changes in the input or output voltage instantly affect the duty ratio. This feature is illustrated in Fig. 11.5 which shows the inductor current and modulator waveforms of the buck converter with two different input voltages. The thin line is the inductor current with the original input voltage. The thick line is the inductor current when the input voltage is decreased while the output voltage remains in regulation. The variation in the input voltage alters the slope of the inductor current and the duty ratio is instantly changed.

In the classical analysis in Example 10.3, the modulator gain of the peak current mode control was derived assuming the slopes of the inductor current remain unchanged. This hypothesis is now discarded to improve the fidelity and accuracy of

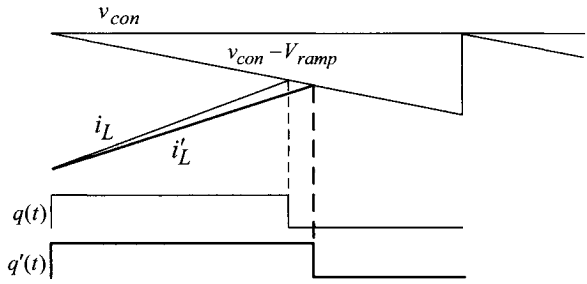


Figure 11.5 PWM waveforms with different input voltages.

the small-signal model. The slopes of the inductor current are affected by both the input voltage and output voltage, and the resulting slope changes immediately alter the duty ratio. This functional dependency is modeled as the feedforward gains from the input and output voltages in the new model.

11.1.4 Complete s-Domain Model for Current Mode Control

The complete s-domain small-signal model for current-mode controlled PWM converters is obtained by adding the necessary gain blocks to the small-signal model introduced in Section 10.2.1. Figure 11.6 shows the resulting small-signal model. In this new small-signal model, four gain blocks are added or modified to represent the sampled-data feature of current mode control, while the voltage feedback compensation $F_v(s)$ and CSN gain R_i remain unchanged.

1) Sampling effects: The s-domain representation of sampling effects can be either merged into the PWM block, resulting in a new s-domain modulator gain $F_m^*(s)$, or included as a separate s-domain gain block, $H_e(s)$, located in the inductor current feedback path.

2) Feedforward gain: The gain block k_f represents the influence of the input voltage and k_r is the feedforward gain from the output voltage.

Once the four additional gain blocks are identified, the complete s-domain model for current mode control is established. With $F_m^*(s) = F'_m$, $H_e(s) = 1$, and $k_f = k_r = 0$, Fig. 11.6 reduces to the model used in the classical analysis in Chapter 10.

11.1.5 Two Prevalent s-Domain Models for Current Mode Control

Two distinct s-domain models for current mode control are being widely used. The first s-domain model was proposed by R. B. Ridley [1]. In Ridley's model, the sampling effects are incorporated as a separate s-domain gain block, $H_e(s)$, while the modulator gain is modeled as a constant. The sampled-data feature of current mode control is initially described as a z-domain transfer function and later transformed

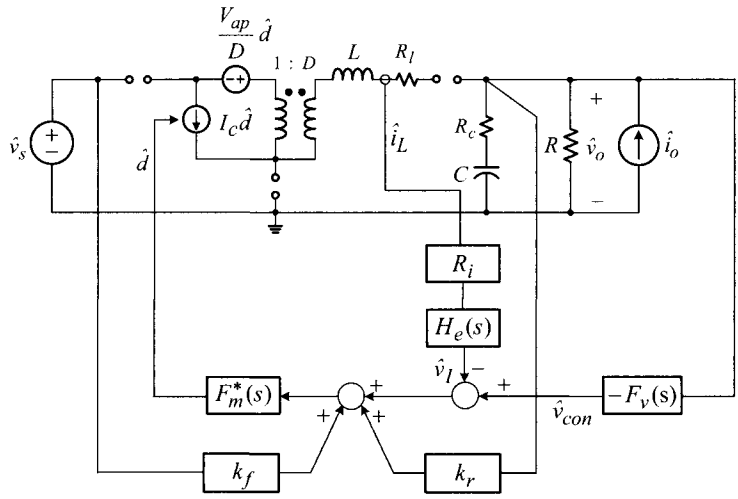


Figure 11.6 Complete s-domain small-signal model for current-mode controlled PWM converters.

into the equivalent s-domain representation, $H_e(s)$. The modulator gain includes the slope of the compensation ramp, yet does not contain any frequency-dependent term. The feedforward gains from the input and output voltages are also included. The expressions for the gain blocks of Ridley's model for the three basic PWM converters are listed in Table 11.1.

Another s-domain model was later proposed by F. D. Tan [2]. In Tan's model, the sampling effects are incorporated into the modulator gain as a frequency-dependent term, while the current feedback loop only contains the CSN gain, namely, $H_e(s) = 1$. This model also contains the feedforward gains from the input and output voltages. The gain blocks for Tan's model are also shown in Table 11.1.

The two s-domain models for current mode control, Ridley's model and Tan's model, have allowed the sampled-data feature of current mode control to be analyzed using only s-domain techniques. However, these two models have subtle differences in their modeling approaches and final results, and therefore have become a subject of comparisons and clarifications. Although the exactness of these two models is still an issue of rigorous assessment, either of them can be selected as a reference model in studying the sampling effects. Each model has its own theoretical developments and provides the correct design procedures for current mode control.

In this book, Ridley's model is chosen as the reference in studying the sampling effects. In the next section, the gain blocks of Ridley's model will be studied. Then, the dynamics of the peak current mode control are analyzed in an attempt to establish new design procedures. Several design examples are given. The predictions and performance of the new design will be compared with those of the classical design developed in Chapter 10. The new control design procedures will be contrasted with

Table 11.1 Two Prevalent s-Domain Models for Current Mode Control

	Ridley's model	Tan's model
$H_e(s)$ for all three converters	$H_e(s) = 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2}$ $Q_z = -\frac{2}{\pi}$ $\omega_n = \frac{\pi}{T_s}$	$H_e(s) = 1$
$F_m^*(s)$ for all three converters	$F_m^*(s) = \frac{1}{(S_n + S_e)T_s}$	$F_m^*(s) = \frac{K_m^*}{1 + \frac{s}{\omega_p}}$ $K_m^* = \frac{2}{(S_n - S_f + 2S_e)T_s}$ $\omega_p = \frac{\omega_s^2}{4K_m^*(S_n + S_f)}$
k_f: buck converter	$-\frac{DT_sR_i}{L}\left(1 - \frac{D}{2}\right)$	$-\frac{D(1-D)T_sR_i}{2L}$
boost converter	$-\frac{T_sR_i}{2L}$	0
buck/boost converter	$-\frac{DT_sR_i}{L}\left(1 - \frac{D}{2}\right)$	$-\frac{D(1-D)T_sR_i}{2L}$
k_r: buck converter	$\frac{T_sR_i}{2L}$	0
boost converter	$\frac{(1-D)^2T_sR_i}{2L}$	$-\frac{D(1-D)T_sR_i}{2L}$
buck/boost converter	$\frac{(1-D)^2T_sR_i}{2L}$	$-\frac{D(1-D)T_sR_i}{2L}$

S_n is the on-time slope and S_f is the off-time slope of the sensed current feedback voltage v_I, while S_e is the slope of the compensation ramp.

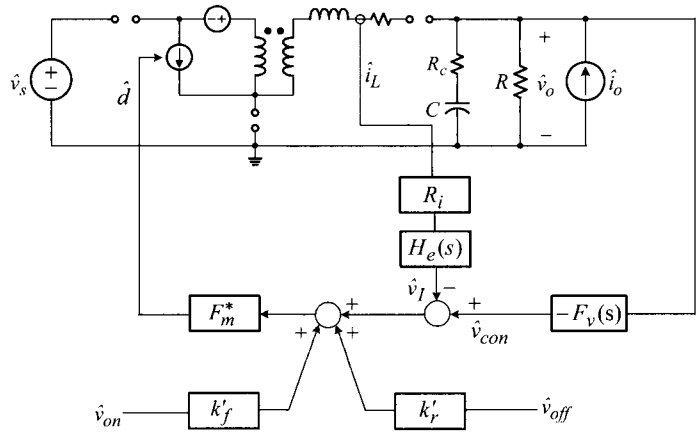


Figure 11.7 Modified small-signal model for current mode control.

the classical design procedures to reveal the connection between the two different design approaches. Lastly, the design and performance of an off-line flyback converter with an optocoupler-based peak current mode control will be discussed.

11.2 EXPRESSIONS FOR S-DOMAIN MODEL FOR CURRENT MODE CONTROL

This section presents analytical details about the Ridley's s-domain model. Expressions for the gain blocks representing the sampled-data feature of current mode control are provided.

11.2.1 Modified Small-Signal Model

In order to facilitate the derivation of the gain blocks, the s-domain model in Fig. 11.6 is modified into an alternative form shown in Fig. 11.7. The modifications incorporated into Fig. 11.7 are as follows.

1) In the modified model, the modulator gain is represented by F_m^* in place of $F_m^*(s)$ because the modulator gain is a constant in Ridley's model.

2) In the original model in Fig. 11.6, the feedforward gains, k_f and k_r, are derived from the input voltage and output voltage of the converter. On the other hand, in the modified model, the feedforward gains are derived from the small-signal sources $\hat{v}_{on}$ and $\hat{v}_{off}$. The small-signal source $\hat{v}_{on}$ represents the voltage that appears across the inductor terminals during the on-time period and $\hat{v}_{off}$ is the (negative) inductor voltage during the off-time period. With these changes, the feedforward gains are renamed as k_f' and k_r'.

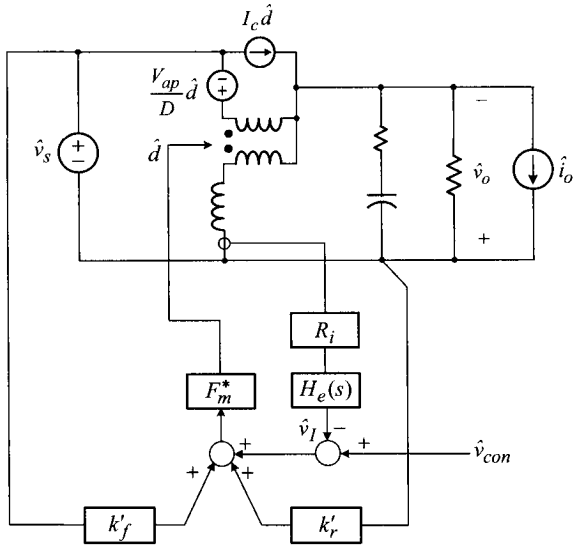


Figure 11.8 Small-signal model of buck/boost converter with current mode control.

The purpose of the above modifications is to simplify the analysis of the feedforward gains. Advantages of the modified model will be explained later in Section 11.2.4.

The modified model in Fig. 11.7 is now adapted to the buck/boost converter. The resulting model is shown in Fig. 11.8. For the buck/boost converter, the modified model is identical to the original model in Fig. 11.6, because $\hat{v}_{on} = \hat{v}_s$ and $\hat{v}_{off} = \hat{v}_o$ for this case. The voltage feedback compensation $F_v(s)$ is not included in Fig. 11.8 because the $F_v(s)$ is predetermined and does not affect the small-signal models of current mode control. The CSN gain R_i is also known in advance.

The four gain blocks, F_m^*, $H_e(s)$, k_f', and k_r', can be derived from Fig. 11.8. Once the four gain blocks are identified, they should be converted into the new expressions that can be put into the original small-signal model of Fig. 11.6. By comparing the two small-signal models of Fig. 11.6 and Fig. 11.7, it is apparent that the expressions for F_m^* and $H_e(s)$ remain the same. However, the feedforward gains, k_f' and k_r', need to be converted to the expressions for k_f and k_r because $\hat{v}_{on} \neq \hat{v}_s$ and $\hat{v}_{off} \neq \hat{v}_o$ in general; the buck/boost converter is a special case where $\hat{v}_{on} = \hat{v}_s$ and $\hat{v}_{off} = \hat{v}_o$ so $k_f = k_f'$ and $k_r = k_r'$. The conversion of the feedforward gains will be discussed later in Section 11.2.4

When the four gain blocks, F_m^*, $H_e(s)$, k_f, and k_r, are inserted into Fig. 11.6, the s-domain small-signal model for the three basic converters can be obtained by appropriately arranging the connections in the power stage circuit configuration. Figure 11.8 itself is the small-signal model of the buck/boost converter with $k_f = k_f'$ and $k_r = k_r'$.

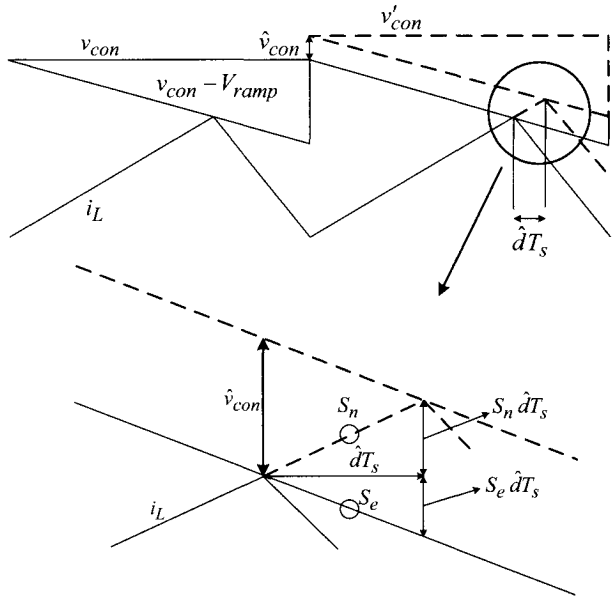


Figure 11.9 Modulator waveforms with perturbed control voltage.

The next section presents the derivation of F_m^*, $H_e(s)$, k_f' and k_r', using Fig. 11.8. In the forthcoming model derivations, the CSN gain is assumed to be unity, $R_i = 1$, unless stated otherwise.

11.2.2 Modulator Gain F_m^*

The modulator gain F_m^* is derived by graphically relating the perturbation in the control voltage, $\hat{v}_{con}$, to the change in duty ratio, $\hat{d}$. Figure 11.9 shows the modulator waveforms where a perturbation is incurred to v_{con} at the onset of the second operational period. The solid line represents the modulator waveforms with the original control voltage, v_{con}, and the dashed line is the waveforms with a perturbed control voltage, v'_{con}. The perturbation in the control voltage, $\hat{v}_{con} = v'_{con} - v_{con}$, causes a change in the on-time period, $\hat{d}T_s$. From the geometry of the modulator waveforms, highlighted in Fig. 11.9 with an expanded view, the following relationship is seen

$$\hat{v}_{con} = S_n \hat{d}T_s + S_e \hat{d}T_s = (S_n + S_e)\hat{d}T_s \tag{11.1}$$

where S_n is the on-time slope of the inductor current and S_e is the slope of the compensation ramp. The above equation is arranged as

$$F_m^* = \frac{\hat{d}}{\hat{v}_{con}} = \frac{1}{(S_n + S_e)T_s} \tag{11.2}$$

to yield the modulator gain.

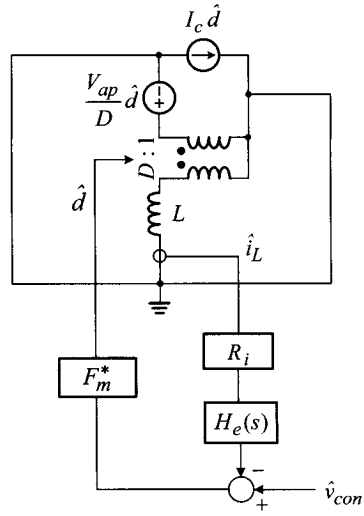


Figure 11.10 Simplified s-domain model for current mode control.

11.2.3 $H_e(s)$: s-Domain Representation of Sampling Effects

The sampling effects of current mode control are modeled as a separate gain block $H_e(s)$ located in the current feedback path. For the purpose of $H_e(s)$ derivation, the input and output voltages are fixed so that $\hat{v}_s = \hat{v}_o = 0$ in Fig. 11.8. Accordingly, Fig. 11.8 is simplified to Fig. 11.10. The expression for $H_e(s)$ is now derived from Fig. 11.10 through the following three steps.

Step One: The expression for the transfer function from the control voltage to inductor current, $H_i(s) = \hat{i}_L(s)/\hat{v}_{con}(s)$, is derived in two different ways, thereby yielding two alternative expressions for the transfer function. The gain block $H_e(s)$ is included in one of the two $H_i(s)$ expressions.

Step Two: By equating the two different $H_i(s)$ expressions, the gain block $H_e(s)$ is derived as $H_e(s) = sT_s/(e^{sT_s} - 1)$.

Step Three: The $H_e(s)$ expression is subsequently approximated to $H_e(s) = sT_s/(e^{sT_s} - 1) \approx 1 + s/(\omega_n Q_z) + s^2/\omega_n^2$ with $Q_z = -2/\pi$ and $\omega_n = \pi/T_s$, based on Taylor series expansion of the complex exponential.

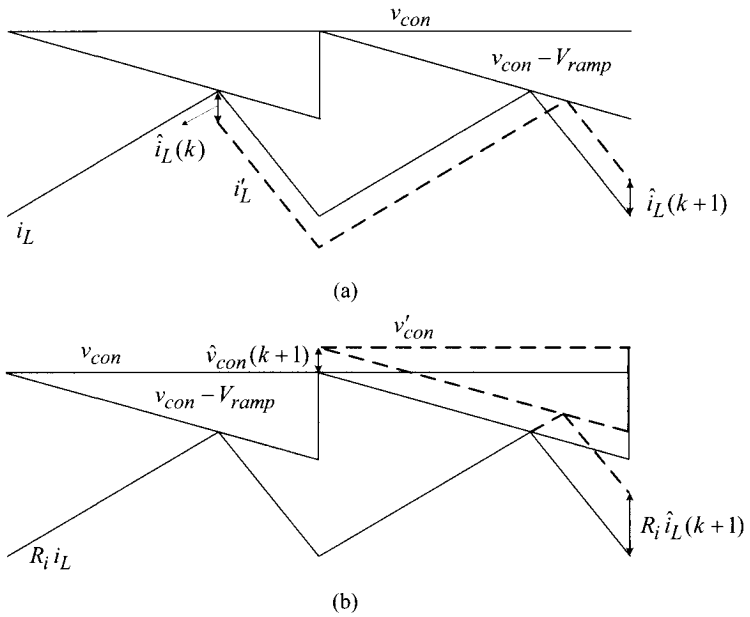


Figure 11.11 Inductor current dynamics. (a) Propagation of inductor current perturbation. (b) Effects of control voltage perturbation.

1) Step One: Two Distinct Expressions for $H_i(s) = \hat{i}_L(s)/\hat{v}_{con}$

Direct application of Mason's gain rule to Fig. 11.10 results in the first expression for the control-to-inductor current transfer function $H_i(s)$

$$H_i(s) = \frac{\hat{i}_L(s)}{\hat{v}_{con}(s)} = \frac{F_m^* \dfrac{\hat{i}_L(s)}{\hat{d}(s)}}{1 + F_m^* \dfrac{\hat{i}_L(s)}{\hat{d}(s)} R_i H_e(s)} \tag{11.3}$$

For the formulation of the second $H_i(s)$ expression, the dynamic behavior of the inductor current is illustrated in Fig. 11.11. Figure 11.11(a) shows the propagation of the inductor current perturbation with the assumption $R_i = 1$, while Fig. 11.11(b) depicts the effects of the control voltage perturbation. The inductor current dynamics under the perturbations in both the inductor current and control voltage are described by a difference equation

$$\hat{i}_L(k+1) = k_1 \hat{i}_L(k) + k_2 \hat{v}_{con}(k+1) \tag{11.4}$$

The first term in the right-hand side of (11.4) represents the propagation of the inductor current perturbation. The inductor current perturbation at $(k+1)^{th}$ period, $\hat{i}_L(k+1)$, is affected by the previous inductor current perturbation, $\hat{i}_L(k)$. This term is the natural

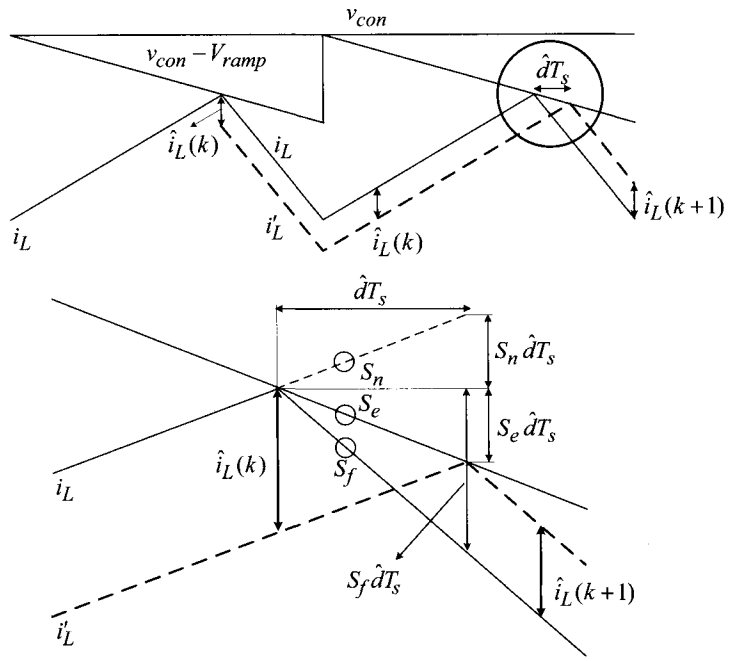


Figure 11.12 Propagation of inductor current perturbation: natural response.

response. The second term describes the impact of the control voltage perturbation on the inductor current. The disturbance in the control voltage at $(k + 1)^{th}$ period, $\hat{v}_{con}(k + 1)$, instantly affects the inductor current, $\hat{i}_L(k + 1)$, without any delay. This second term is the forced response. The two proportionate coefficients in (11.4), k_1 and k_2, are evaluated by analyzing the natural and forced responses.

Natural Response

Figure 11.12 shows the propagation of the inductor current perturbation, $\hat{i}_L(k) = i'_L(k) - i_L(k)$, into the next sampling instant. From the geometry of the PWM waveforms, the following relationships are established

$$-\hat{i}_L(k) = (S_n + S_e)\hat{d}T_s \tag{11.5}$$

and

$$\hat{i}_L(k + 1) = (S_f - S_e)\hat{d}T_s \tag{11.6}$$

From (11.5) and (11.6), it follows that

$$\frac{\hat{i}_L(k + 1)}{\hat{i}_L(k)} = -\frac{S_f - S_e}{S_n + S_e} \tag{11.7}$$

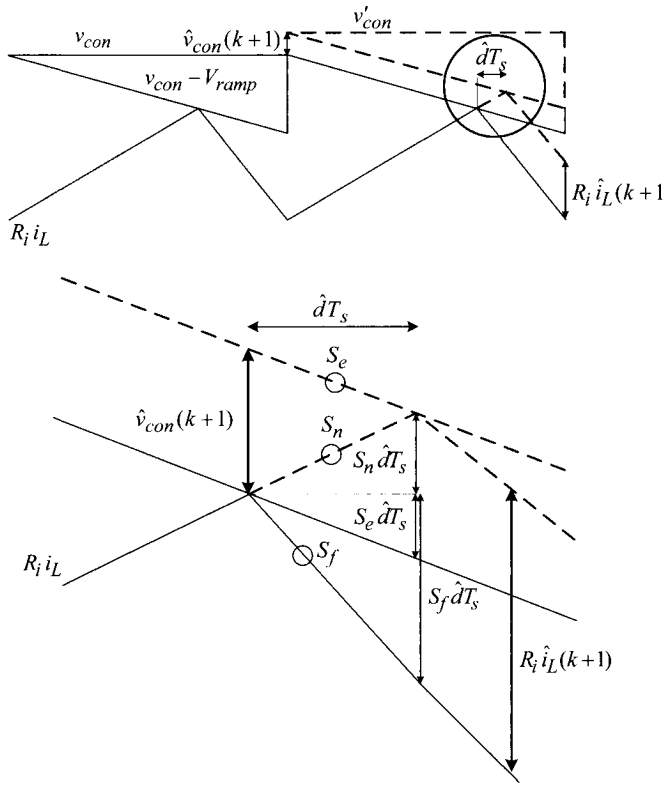


Figure 11.13 Effects of control voltage perturbation: forced response.

which is arranged as

$$\hat{i}_L(k+1) = -\alpha\,\hat{i}_L(k) \tag{11.8}$$

with

$$\alpha = \frac{S_f - S_e}{S_n + S_e} \tag{11.9}$$

Equation (11.8) is the natural response of the inductor current.

Forced Response

Figure 11.13 illustrates the effect of the control voltage perturbation. From the geometry of the modulator waveforms, the following relationships are established

$$\hat{v}_{con}(k+1) = (S_n + S_e)\,\hat{d}T_s \tag{11.10}$$

and

$$R_i\,\hat{i}_L(k+1) = (S_n + S_f)\,\hat{d}T_s \tag{11.11}$$

By eliminating $\hat{d}T_s$ from (11.10) and (11.11), it follows that

$$R_i\,\hat{i}_L(k+1) = \frac{S_n + S_f}{S_n + S_e}\,\hat{v}_{con}(k+1) = \left(1 + \frac{S_f - S_e}{S_n + S_e}\right)\hat{v}_{con}(k+1) \tag{11.12}$$

which is rearranged as

$$\hat{i}_L(k+1) = \frac{1}{R_i}(1+\alpha)\,\hat{v}_{con}(k+1) \tag{11.13}$$

where $\alpha = (S_f - S_e)/(S_n + S_e)$ was defined earlier in (11.9). The above equation is the forced response.

Complete Response

By summing the natural response and forced response, the complete response of the inductor is given by

$$\hat{i}_L(k+1) = k_1\hat{i}_L(k) + k_2\,\hat{v}_{con}(k+1) \tag{11.14}$$

where $k_1 = -\alpha$ and $k_2 = (1+\alpha)/R_i$ with $\alpha = (S_f - S_e)/(S_n + S_e)$. The final expression for the inductor current now becomes

$$\hat{i}_L(k+1) = -\alpha\,\hat{i}_L(k) + \frac{1}{R_i}(1+\alpha)\,\hat{v}_{con}(k+1) \tag{11.15}$$

By taking the z-transformation of (11.15)

$$z\,\hat{i}_L(z) = -\alpha\,\hat{i}_L(z) + \frac{1}{R_i}(1+\alpha)\,z\,\hat{v}_{con}(z) \tag{11.16}$$

the z-domain control voltage-to-inductor current transfer function, $H_i(z)$, is derived as

$$H_i(z) = \frac{\hat{i}_L(z)}{\hat{v}_{con}(z)} = \frac{1}{R_i}(1+\alpha)\frac{z}{z+\alpha} \tag{11.17}$$

The continuous-time representation of $H_i(z)$ is obtained from (11.17) by multiplying $(1 - e^{-sT_s})/(sT_s)$ and replacing z with e^{sT_s} [3]

$$\begin{aligned} H_i(s) &= \frac{1 - e^{-sT_s}}{sT_s} H_i(z = e^{sT_s}) \\ &= \frac{1}{R_i}\frac{1+\alpha}{sT_s}\frac{e^{sT_s} - 1}{e^{sT_s} + \alpha} \end{aligned} \tag{11.18}$$

It is well known that this z-domain-to-s-domain conversion is only valid for the frequencies below the Nyquist frequency, $\omega_n = 0.5\,\omega_s = \pi/T_s$. Equation (11.18) is the second s-domain expression for the control voltage-to-inductor current transfer function. This second $H_i(s)$ expression is developed from the modulator waveforms and therefore does not include the $H_e(s)$ gain block. Recall that the first $H_i(s)$ expression, given by (11.3), contains the $H_e(s)$ block.

2) Step Two: Identification of Gain Block $H_e(s)$

Two independently-driven descriptions for $H_i(s)$, (11.3) and (11.18), are now obtained. By equating these two expressions, the expression for $H_e(s)$ is derived as

$$H_e(s) = \frac{sT_s}{e^{sT_s} - 1} \tag{11.19}$$

Details about this derivation are given in Example 11.2.

■ **EXAMPLE 11.2 Derivation of $H_e(s)$**

This example illustrates the derivation of (11.19). By equating (11.3) and (11.18), it follows that

$$\frac{F_m^* \dfrac{\hat{\imath}_L(s)}{\hat{d}(s)}}{1 + F_m^* \dfrac{\hat{\imath}_L(s)}{\hat{d}(s)} R_i H_e(s)} = \frac{1}{R_i} \frac{1 + \alpha}{sT_s} \frac{e^{sT_s} - 1}{e^{sT_s} + \alpha} \tag{11.20}$$

The objective of this analysis is to find the expression for $H_e(s)$ that satisfies (11.20). First, from the simplified s-domain model in Fig. 11.10, the duty-ratio-to-inductor current transfer function is derived as

$$\frac{\hat{\imath}_L(s)}{\hat{d}(s)} = \frac{V_{ap}}{D} D \frac{1}{sL} \tag{11.21}$$

The expression for V_{ap}, the voltage between the active and passive terminals of the PWM switch, is derived from Fig. 11.14

$$V_{ap} = V_{ai} + V_{ip} \tag{11.22}$$

The voltages V_{ai} and V_{ip} are related to the on-time and off-time slopes of the current feedback signal

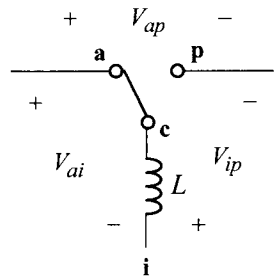


Figure 11.14 PWM switch and terminal voltage definitions.

$$S_n = \frac{V_{ai}}{L} R_i \tag{11.23}$$

$$S_f = \frac{V_{ip}}{L} R_i \tag{11.24}$$

From (11.22) through (11.24), it follows that

$$V_{ap} = \frac{L}{R_i}(S_n + S_f) \tag{11.25}$$

By merging (11.21) and (11.25), it follows that

$$\frac{\hat{\imath}_L(s)}{\hat{d}(s)} = \frac{1}{R_i} \frac{S_n + S_f}{s} \tag{11.26}$$

From (11.26) and $F_m^* = 1/\big((S_n + S_e)T_s\big)$, it becomes that

$$\begin{aligned} F_m^* \frac{\hat{\imath}_L(s)}{\hat{d}(s)} &= \frac{1}{(S_n + S_e)T_s} \frac{1}{R_i} \frac{S_n + S_f}{s} \\ &= \frac{1}{R_i} \frac{1+\alpha}{sT_s} \end{aligned} \tag{11.27}$$

with $\alpha = (S_f - S_e)/(S_n + S_e)$. Using (11.27), the expression (11.20) now becomes

$$\frac{\dfrac{1}{R_i}\dfrac{1+\alpha}{sT_s}}{1 + \dfrac{1}{R_i}\dfrac{1+\alpha}{sT_s} R_i H_e(s)} = \frac{1}{R_i} \frac{1+\alpha}{sT_s} \frac{e^{sT_s} - 1}{e^{sT_s} + \alpha} \tag{11.28}$$

which can be solved for $H_e(s)$ to yield the expression (11.19), as shown in Problem 11.2 at the end of this chapter.

3) Step Three: Approximation of Gain Block $H_e(s)$

As the last derivation step, the s-domain representation of the sampling effects $H_e(s)$ is approximated to

$$H_e(s) = \frac{sT_s}{e^{sT_s} - 1} \approx 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2} \tag{11.29}$$

with

$$Q_z = -\frac{2}{\pi} \tag{11.30}$$

and

$$\omega_n = \frac{\pi}{T_s} \tag{11.31}$$

based on the Taylor series expansion of the complex polynomial. The procedures of this approximation are given in Example 11.3.

■ EXAMPLE 11.3 Approximation of $H_e(s)$

This example illustrates the derivation of (11.29). First, the complex exponential function is approximated as

$$e^{sT_s} = \frac{e^{s\frac{T_s}{2}}}{e^{-s\frac{T_s}{2}}} = \frac{e^{s\frac{\pi}{\omega_s}}}{e^{-s\frac{\pi}{\omega_s}}} \approx \frac{1 + s\frac{\pi}{\omega_s} + \frac{1}{2}\left(s\frac{\pi}{\omega_s}\right)^2}{1 - s\frac{\pi}{\omega_s} + \frac{1}{2}\left(s\frac{\pi}{\omega_s}\right)^2} \tag{11.32}$$

using the identity $e^x = 1 + x + x^2/2! + \cdots$ with $x \ll 1$. This approximation is accurate for frequencies $\omega \ll \omega_s/\pi$. The above expression is further modified to

$$e^{sT_s} \approx \frac{1 + s\frac{\pi}{\omega_s} + \frac{1}{2}\left(s\frac{\pi}{\omega_s}\right)^2}{1 - s\frac{\pi}{\omega_s} + \frac{1}{2}\left(s\frac{\pi}{\omega_s}\right)^2} \approx \frac{1 + \frac{1}{2/\pi}\frac{s}{\omega_s/2} + \left(\frac{s}{\omega_s/2}\right)^2}{1 - \frac{1}{2/\pi}\frac{s}{\omega_s/2} + \left(\frac{s}{\omega_s/2}\right)^2} \tag{11.33}$$

by accepting the approximation of $\pi^2/2 \approx 4.935 \approx 4$. Using (11.33), $H_e(s)$ is written as

$$H_e(s) = \frac{sT_s}{e^{sT_s} - 1} \approx \frac{s\frac{2\pi}{\omega_s}}{\left(\frac{1 + \frac{1}{2/\pi}\frac{s}{\omega_s/2} + \left(\frac{s}{\omega_s/2}\right)^2}{1 - \frac{1}{2/\pi}\frac{s}{\omega_s/2} + \left(\frac{s}{\omega_s/2}\right)^2}\right) - 1}$$

$$= 1 - \frac{1}{2/\pi}\frac{s}{\omega_s/2} + \left(\frac{s}{\omega_s/2}\right)^2 \tag{11.34}$$

which can be put into the expressions (11.29) through (11.31) using $\omega_s = 2\pi/T_s$.

The s-domain representation of the sampling effects is valid only for the frequencies below the Nyquist frequency, due to the z-domain-to-s-domain conversion in (11.18) and assumptions used in (11.32). Figure 11.15 compares the Bode plots of the original expression of $H_e(s)$ and its low-frequency approximation of (11.29).

The s-domain representation of the sampling effects, given by (11.29), is a double zero function with a negative damping factor, $Q_z = -2/\pi \approx -0.637$. The double zero is located at the Nyquist frequency, $\omega_n = \pi/T_s = 0.5\,\omega_s$. Accordingly, $H_e(s)$ exerts negligible effects at low frequencies and only becomes influential at the high frequencies. As shown in Fig. 11.15, $H_e(s)$ does not cause any practical impacts

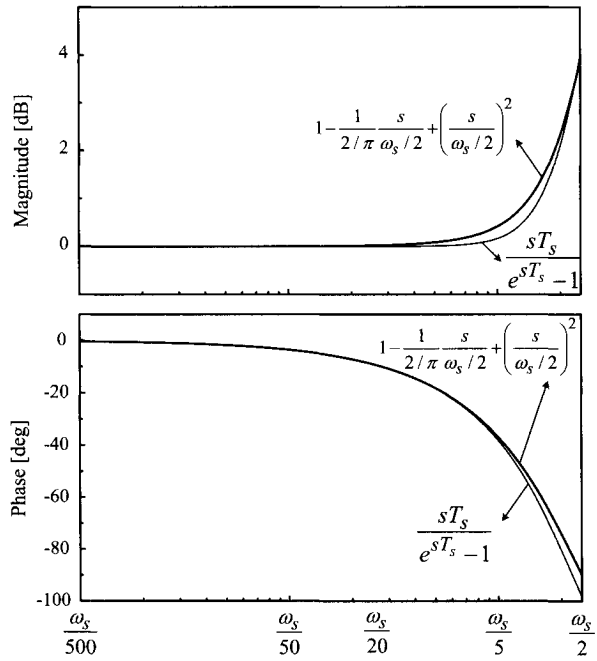


Figure 11.15 Bode plot of the original $H_e(s)$ and its low frequency approximation.

at frequencies below $\omega_s/20$. The maximum impact of $H_e(s)$ occurs at the Nyquist frequency where $|H_e(j\omega)|$ increases about 4 dB and $\angle H_e(j\omega)$ drops by 90°. This observation is consistent with Fig. 11.4 which illustrates the consequence of the sampling effects on the loop gain characteristics. The sampling effects are only pronounced at the frequencies near or above the Nyquist frequency. This fact also supports the prevalence of the classical analysis which ignores the sampling effects. *If the control bandwidth is well below the Nyquist frequency, the sampling effects do not interfere with the control design and closed-loop performance.*

■ EXAMPLE 11.4 Circuit Model for $H_e(s)$

Figure 11.16 shows a simple circuit model for $H_e(s)$. The unique feature of the circuit model is the existence of a negative resistance, which can be accepted by most circuit simulators including PSpice®. The transfer function of the circuit is given by

$$F(s) = -\frac{-\frac{\pi}{2}+\frac{1}{s\frac{2}{\omega_s}}+s\frac{2}{\omega_s}}{\frac{1}{s\frac{2}{\omega_s}}} = -\left(1-\frac{1}{2/\pi}\frac{s}{\omega_s/2}+\left(\frac{s}{\omega_s/2}\right)^2\right) \qquad (11.35)$$

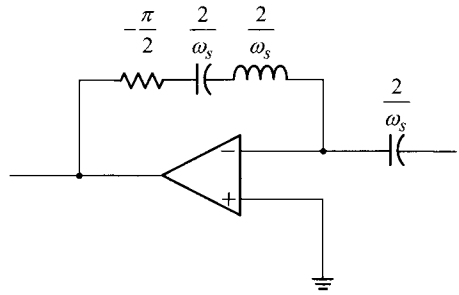


Figure 11.16 Circuit model for $H_e(s) = 1 - \frac{1}{2/\pi}\frac{s}{\omega_s/2} + \left(\frac{s}{\omega_s/2}\right)^2$.

This circuit model can be used to simulate the small-signal dynamics of the converter with the presence of the sampling effects.

11.2.4 Feedforward Gains

Among the four small-signal gain blocks for current mode control, the modulator gain F_m^* and sampling effect $H_e(s)$ are identified. This section now presents derivations of the feedforward gains, k_f' and k_r'. Similar to the case of $H_e(s)$ development, two different expressions for the inductor voltage-to-inductor current transfer function are formulated. By equating these two alternative expressions, the descriptions for the feedforward gains are extracted.

Feedforward Gain k_f'

The feedforward gain is derived from the modulator waveform of the peak current mode control, shown in Fig. 11.17. It can be seen from Fig. 11.17 that

$$R_i\bar{i}_L = v_{con} - S_e dT_s - \frac{1}{2}S_f(1-d)T_s \tag{11.36}$$

where $\bar{i}_L$ denotes the average inductor current. The off-time slope of the sensed inductor current is given by

$$S_f = \frac{v_{off}}{L}R_i \tag{11.37}$$

where v_{off} is the (negative) inductor voltage during the off-time period. The flux-balance condition on the inductor is written as

$$v_{on}dT_s = v_{off}(1-d)T_s \tag{11.38}$$

where v_{on} is the on-time period inductor voltage. The above equation provides the expression for the duty ratio in terms of the inductor voltages

$$d = \frac{v_{off}}{v_{on} + v_{off}} \tag{11.39}$$

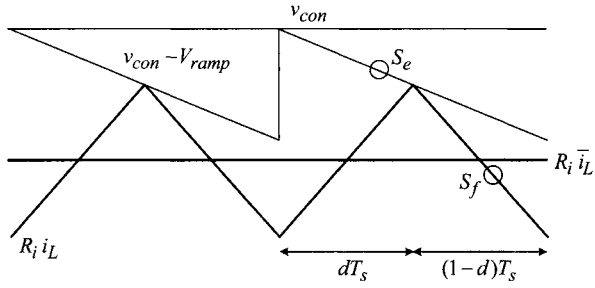


Figure 11.17 Steady-state modulator waveforms.

By incorporating (11.37) and (11.39) into (11.36), and linearizing the resulting equation with respect to $\bar{i}_L$ and $\hat{v}_{on}$, the following equation is obtained

$$G_{on}(s) = \frac{\hat{\bar{i}}_L}{\hat{v}_{on}} = \frac{S_e T_s}{R_i} \frac{D}{V_{ap}} - \frac{T_s}{2L} D^2 \tag{11.40}$$

where $V_{ap} = V_{on} + V_{off}$ is the sum of the respective dc component of the on-time inductor voltage and off-time inductor voltage. Equation (11.40) is the first equation for $G_{on}(s) = \hat{\bar{i}}_L / \hat{v}_{on}$. Derivation of (11.40) is given in Example 11.5.

■ EXAMPLE 11.5 Derivation of $G_{on}(s)$

This example shows the derivation of $G_{on}(s)$ in (11.40). Incorporation of (11.37) and (11.39) into (11.36) yields

$$R_i \bar{i}_L = v_{con} - S_e T_s \frac{v_{off}}{v_{on} + v_{off}} - \frac{1}{2} \frac{v_{off}}{L} R_i T_s \frac{v_{on}}{v_{on} + v_{off}} \tag{11.41}$$

Differentiation of (11.41) with respect to v_{on} results in

$$\begin{aligned} \frac{\partial \bar{i}_L}{\partial v_{on}} &= \frac{1}{R_i} S_e T_s \frac{\partial}{\partial v_{on}} \left(\frac{-v_{off}}{v_{on} + v_{off}} \right) - \frac{1}{2} \frac{v_{off}}{L} T_s \frac{\partial}{\partial v_{on}} \left(\frac{v_{on}}{v_{on} + v_{off}} \right) \\ &= \frac{1}{R_i} S_e T_s \frac{v_{off}}{(v_{on} + v_{off})^2} - \frac{T_s}{2L} \frac{v_{off}^2}{(v_{on} + v_{off})^2} \end{aligned} \tag{11.42}$$

which can be arranged in the form of (11.40) by considering the steady-state circuit variables: $D = V_{off}/(V_{on} + V_{off})$ and $V_{ap} = V_{on} + V_{off}$.

The second expression for $G_{on} = \hat{\bar{i}}_L / \hat{v}_{on}$ is obtained from the simplified small-signal model of the converter, shown in Fig. 11.18. The feedforward gains only describe the low-frequency averaged dynamics of the PWM block. Therefore, the high-frequency modulator dynamics, such as the sampling effects, can be ignored.

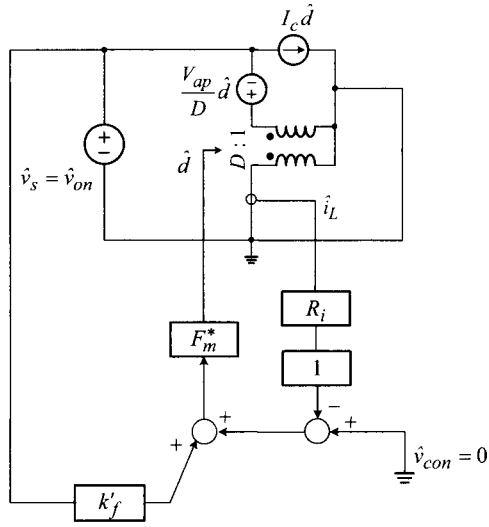


Figure 11.18 Small-signal model for derivation of feedforward gains.

Figure 11.18 is the small-signal model constructed for low-frequency averaged dynamics, based on the following observations.

1) The gain block $H_e(s)$ is approximated by unity: $H_e(s) = 1$.

2) The average value of the inductor voltage is zero, as such, the inductor behaves as a short circuit at low frequencies.

3) The output voltage of the converter is constant: $\hat{v}_o = \hat{v}_{off} = 0$.

4) The control voltage remains constant: $\hat{v}_{con} = 0$

From Fig. 11.18, the following relationship is established

$$(\hat{v}_{on}k_f' - R_i\hat{\tilde{i}}_L)F_m^*\frac{V_{ap}}{D} = -\hat{v}_{on} \tag{11.43}$$

by noting that the transformer windings are shorted. Equation (11.43) is rearranged as

$$G_{on}(s) = \frac{\hat{\tilde{i}}_L}{\hat{v}_{on}} = \frac{1}{R_i}\left(\frac{D}{F_m^*V_{ap}} + k_f'\right) \tag{11.44}$$

to yield the second expression for $G_{on}(s)$. By equating (11.40) and (11.44) with incorporation of $F_m^* = 1/\big((S_n + S_e)T_s\big)$, the feedforward gain is obtained as

$$k_f' = -\frac{DT_sR_i}{L}\left(1 - \frac{D}{2}\right) \tag{11.45}$$

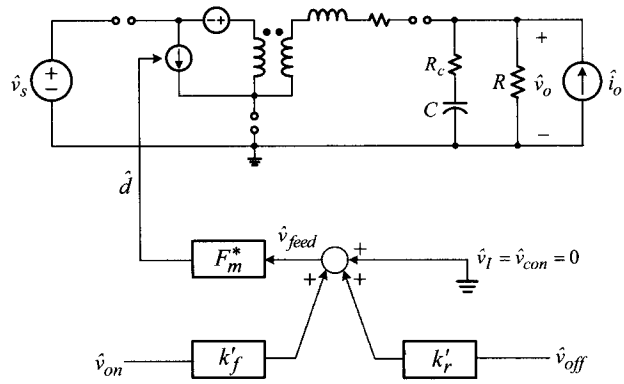


Figure 11.19 Small-signal model for feedforward gain conversion.

Feedforward Gain k_r'

By repeating the same process for the off-time inductor voltage, the feedforward gain k_r' is evaluated as

$$k_r' = \frac{(1-D)^2 T_s R_i}{2L} \tag{11.46}$$

Conversion of Feedforward Gains

As discussed in Section 11.2.1, the feedforward gains, k_f' and k_r' derived in the previous section, should be converted to the original feedforward gains, k_f and k_r defined in Fig. 11.6. Figure 11.19 shows the small-signal model that will be used to find the relationship between $\{k_f' \, k_r'\}$ and $\{k_f \, k_r\}$. This model is derived from Fig. 11.7 with the condition $\hat{v}_I = \hat{v}_{con} = 0$.

In Fig. 11.19, the input signal to the modulator gain block F_m^* is expressed as

$$\hat{v}_{feed} = k_f' \hat{v}_{on} + k_r' \hat{v}_{off} \tag{11.47}$$

The conversion from $\{k_f' \, k_r'\}$ to $\{k_f \, k_r\}$ is now explained using the buck converter. For the buck converter, the following relationships hold

$$\hat{v}_{on} = \hat{v}_s - \hat{v}_o \quad \text{and} \quad \hat{v}_{off} = \hat{v}_o \tag{11.48}$$

Equations (11.47) and (11.48) are combined

$$\hat{v}_{feed} = k_f'(\hat{v}_s - \hat{v}_o) + k_r' \hat{v}_o = k_f' \hat{v}_s + (-k_f' + k_r') \hat{v}_o \tag{11.49}$$

yielding the relationship

$$\hat{v}_{feed} = k_f \hat{v}_s + k_r \hat{v}_o \tag{11.50}$$

with

$$k_f = k_f' \quad \text{and} \quad k_r = -k_f' + k_r' \tag{11.51}$$

Table 11.2 Inductor Voltage Relationships and Feedforward Gains

	Buck converter	Boost converter	Buck/boost converter
v_{on}	$v_S - v_O$	v_S	v_S
v_{off}	v_O	$v_O - v_S$	v_O
k_f	k'_f	$k'_f - k'_r$	k'_f
k_r	$-k'_f + k'_r$	k'_r	k'_r

Expressions (11.51) are the original feedforward gains for the buck converter, shown in Fig. 11.6. The same process is applied to the boost and buck/boost converters. The results of this analysis are shown in Table 11.2. The feedforward gains, k'_f and k'_r derived in (11.45) and (11.46), are now converted into the original gains, k_f and k_r in Fig. 11.6. Table 11.2 is used for this conversion. The final expressions for the feedforward gains of the three basic converters are shown in Table 11.1.

The analysis of the small-signal gain blocks is performed using the modified model of Fig. 11.7 rather than the original model of Fig. 11.6. The advantage of Fig. 11.7 is that k'_f and k'_r are derived only once and the outcomes are adapted to the three basic converters to provide their respective k_f and k_r expressions. If Fig. 11.6 is used for this analysis, the derivation should be repeated three times for the three basic converters.

11.3 NEW CONTROL DESIGN PROCEDURES FOR CURRENT MODE CONTROL

In the previous section, we identified the expressions for the small-signal gain blocks for the peak current mode control. This section presents the analysis of current mode control using these gain blocks. The objective of this analysis is to establish new design procedures that incorporate the sampling effects of current mode control.

11.3.1 New Power Stage Model

Figure 11.20(a) shows the complete small-signal model for current-mode controlled PWM dc-to-dc converters. The analysis will be facilitated by defining a *new* power stage model. The block of the small-signal model, enclosed by the solid line in Fig. 11.20(a), is considered as the new power stage model. The new power stage model is in fact the small-signal model of power stage amalgamated with the gain blocks of the peak current model control. Figure 11.20(a) is converted into the block diagram

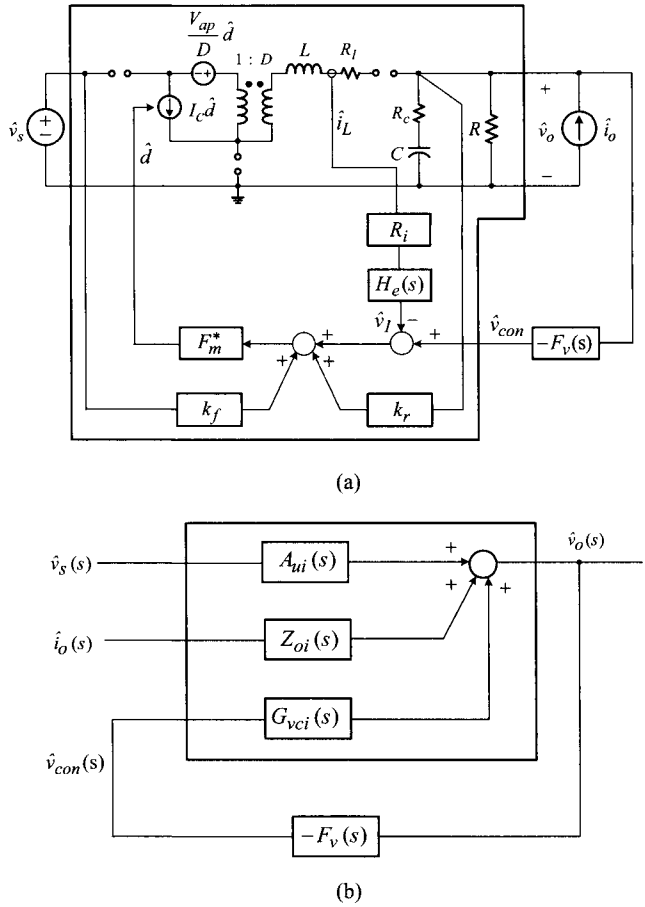


Figure 11.20 Small-signal model for current-mode controlled PWM converters. (a) Circuit model. (b) Block diagram representation.

representation in Fig. 11.20(b) by defining the following composite gain blocks for the new power stage model

$$G_{vci}(s) \equiv \left.\frac{\hat{v}_o(s)}{\hat{v}_{con}(s)}\right|_{\text{current loop closed}} \tag{11.52}$$

$$A_{ui}(s) \equiv \left.\frac{\hat{v}_o(s)}{\hat{v}_s(s)}\right|_{\text{current loop closed}} \tag{11.53}$$

and

$$Z_{oi}(s) \equiv \left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\text{current loop closed}} \tag{11.54}$$

Each transfer function is evaluated under the condition that only the current feedback is activated and the voltage feedback path is broken. Referring to Fig.

11.20(b), the loop gain is defined as

$$T_m(s) = (-)G_{vci}(s)(-)F_v(s) = G_{vci}(s)F_v(s) \tag{11.55}$$

Once $G_{vci}(s)$ is identified, the voltage feedback compensation $F_v(s)$ can be designed for the loop gain offering both stability and good closed-loop performance.

The audio-susceptibility is given by

$$A_u(s) = \frac{A_{ui}(s)}{1 + T_m(s)} \tag{11.56}$$

and the output impedance is determined as

$$Z_o(s) = \frac{Z_{oi}(s)}{1 + T_m(s)} \tag{11.57}$$

The above descriptions can be used to investigate the closed-loop performance using the asymptotic analysis method discussed in Chapter 8. Details about such analyses can be found in [4].

11.3.2 Control-to-Output Transfer Function with Current Loop Closed

The most important gain block in Fig. 11.20(b) is the control-to-output transfer function evaluated with the current loop closed, $G_{vci}(s) = \hat{v}_o(s)/\hat{v}_{con}(s)$. Knowledge of this gain block is essential to the loop gain design.

Derivation of $G_{vci}(s)$

The expression for $G_{vci}(s)$ is derived from the new power stage model with the condition $\hat{v}_s(s) = \hat{i}_o(s) = 0$. Figure 11.21 shows the power stage model modified for

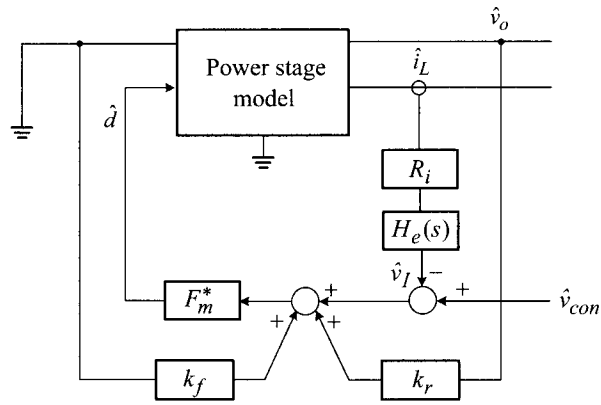


Figure 11.21 Small-signal model for $G_{vci}(s)$ evaluation.

the $G_{vci}(s)$ evaluation. From Mason's gain rule, $G_{vci}(s)$ is described as

$$G_{vci}(s) = \frac{\hat{v}_o(s)}{\hat{v}_{con}(s)} = \frac{F_m^* \dfrac{\hat{v}_o(s)}{\hat{d}(s)}}{1 - k_r F_m^* \dfrac{\hat{v}_o(s)}{\hat{d}(s)} + R_i H_e(s) F_m^* \dfrac{\hat{i}_L(s)}{\hat{d}(s)}} \tag{11.58}$$

Although the above description is rather involved, it can be reduced to a simple expression with some practical assumptions on power stage parameters and operational conditions. As will be illustrated in Example 11.6, $G_{vci}(s)$ is casted into the following third-order approximation

$$G_{vci}(s) \approx K_{vc} \frac{\left(1 - \dfrac{s}{\omega_{rhp}}\right)\left(1 + \dfrac{s}{\omega_{esr}}\right)}{\left(1 + \dfrac{s}{\omega_{pl}}\right)\left(1 + \dfrac{s}{Q_p \omega_n} + \dfrac{s^2}{\omega_n^2}\right)} \tag{11.59}$$

The expressions for Q_p, ω_n, and ω_{esr} are common to all the three basic PWM converters

$$Q_p = \frac{1}{\pi\left(\left(1 + \dfrac{S_e}{S_n}\right)D' - 0.5\right)} \tag{11.60}$$

$$\omega_n = \frac{\pi}{T_s} \tag{11.61}$$

and

$$\omega_{esr} = \frac{1}{CR_c} \tag{11.62}$$

The other three parameters, K_{vc}, ω_{pl}, and ω_{rhp}, vary with the converter topology. Expressions for these parameters for the three basic converters are shown in Table 11.3.

■ EXAMPLE 11.6 Derivation of $G_{vci}(s)$ for Buck Converter

The $G_{vci}(s)$ expression for the buck converter is obtained by evaluating (11.58) with some simplifying assumptions. As the first step, the modulator gain is expressed as

$$F_m^* = \frac{1}{(S_n + S_e)T_s} = \frac{1}{m_c S_n T_s} \tag{11.63}$$

with

$$m_c = 1 + \frac{S_e}{S_n} \tag{11.64}$$

The modulator gain is further modified as

$$F_m^* = \frac{L}{m_c V_S (1 - D) R_i T_s} \tag{11.65}$$

based on the relationship

$$S_n = \frac{V_S - V_O}{L} R_i = \frac{V_S(1-D)}{L} R_i \tag{11.66}$$

Using (11.65) and the expressions of $\hat{v}_o(s)/\hat{d}(s)$, $\hat{i}_L(s)/\hat{d}(s)$, and k_r for the buck converter, given in Table 10.2 and Table 11.1, $G_{vci}(s)$ in (11.58) is evaluated as

$$G_{vci}(s) = \frac{F_m^* \dfrac{\hat{v}_o(s)}{\hat{d}(s)}}{1 - k_r F_m^* \dfrac{\hat{v}_o(s)}{\hat{d}(s)} + R_i H_e(s) F_m^* \dfrac{\hat{i}_L(s)}{\hat{d}(s)}}$$

$$= \frac{\dfrac{L}{m_c V_S D' R_i T_s} V_S \dfrac{1 + sCR_c}{\Delta(s)}}{1 - \dfrac{T_s R_i}{2L} \dfrac{L}{m_c V_S D' R_i T_s} V_S \dfrac{1 + sCR_c}{\Delta(s)} + \dfrac{R_i L}{m_c V_S D' R_i T_s} \dfrac{V_S}{R} \dfrac{1 + sCR}{\Delta(s)} H_e(s)} \tag{11.67}$$

where

$$D' = 1 - D$$

and

$$\Delta(s) = 1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2} \tag{11.68}$$

with $Q = R\sqrt{C/L}$ and $\omega_o = 1/\sqrt{LC}$. The expression (11.67) is rearranged as

$$G_{vci}(s) = \frac{L}{R_i} \frac{1 + sCR_c}{m_c T_s D' \Delta(s) + \dfrac{L}{R}(1 + sCR) H_e(s) - \dfrac{T_s}{2}(1 + sCR_c)} \tag{11.69}$$

Now, using the expression $H_e(s) = 1 + s/(Q_z\omega_n) + s^2/\omega_n^2$ with $Q_z = -2/\pi$ and $\omega_n = \pi/T_s$, the expression (11.69) is written as

$$G_{vci}(s) = \frac{L}{R_i} \frac{1 + sCR_c}{a + bs + cs^2 + ds^3} \tag{11.70}$$

where

$$\begin{aligned}
a &= m_c T_s D' + \frac{L}{R} - \frac{T_s}{2} = T_s(m_c D' - 0.5) + \frac{L}{R} \\
b &= m_c T_s D' \frac{L}{R} + \frac{L}{R}\left(CR - \frac{T_s}{2}\right) - \frac{T_s}{2} CR_c \approx \frac{L}{R} CR - \frac{T_s}{2} CR_c \approx LC \\
c &= m_c T_s D' LC + \frac{L}{R}\left(\frac{T_s^2}{\pi^2} - \frac{CRT_s}{2}\right) \\
&\approx m_c T_s D' LC + \frac{L}{R}\left(-\frac{CRT_s}{2}\right) = m_c T_s D' LC - LC\frac{T_s}{2} \\
d &= \frac{L}{R} CR \frac{T_s^2}{\pi^2} = LC\frac{T_s^2}{\pi^2}
\end{aligned} \tag{11.71}$$

with the assumptions $CR \gg T_s/2$, $CR \gg m_c D' T_s$, $L/R_c \gg T_s/2$, and $CRT_s/2 \gg T_s^2/\pi^2$.

Based on the approximation $a + bs + cs^2 + ds^3 \approx a\left(1 + (b/a)s\right)\left(1 + (c/b)s + (d/b)s^2\right)$ with the conditions $b \gg c$ and $b \gg d$, $G_{vci}(s)$ is factorized as

$$G_{vci}(s) = K_{vc} \frac{\left(1 - \frac{s}{\omega_{rhp}}\right)\left(1 + \frac{s}{\omega_{esr}}\right)}{\left(1 + \frac{s}{\omega_{pl}}\right)\left(1 + \frac{s}{Q_p \omega_n} + \frac{s^2}{\omega_n^2}\right)} \tag{11.72}$$

For the buck converter, ω_{rhp} does not exist so it becomes

$$\omega_{rhp} = \infty$$

The esr zero is given by

$$\omega_{esr} = \frac{1}{CR_c}$$

The other parameters are evaluated as

$$\begin{aligned} K_{vc} = \frac{L}{R_i}\frac{1}{a} &= \frac{L}{R_i}\frac{1}{T_s(m_c D' - 0.5) + \frac{L}{R}} \\ &= \frac{R}{R_i}\frac{1}{1 + \frac{RT_s}{L}(m_c D' - 0.5)} \end{aligned} \tag{11.73}$$

$$\begin{aligned} \omega_{pl} = \frac{a}{b} &= \frac{T_s(m_c D' - 0.5) + \frac{L}{R}}{LC} \\ &= \frac{1}{CR} + \frac{T_s}{LC}(m_c D' - 0.5) \end{aligned} \tag{11.74}$$

$$\omega_n = \sqrt{\frac{b}{d}} = \sqrt{\frac{LC}{LC\frac{T_s^2}{\pi^2}}} = \frac{\pi}{T_s} \tag{11.75}$$

and

$$Q_p \omega_n = \frac{b}{c} = \frac{LC}{m_c T_s D' LC - LC\frac{T_s}{2}} = \frac{1}{(m_c D' - 0.5)T_s} \tag{11.76}$$

yielding the expression

$$Q_p = \frac{1}{\pi(m_c D' - 0.5)} = \frac{1}{\pi\left(\left(1 + \frac{S_e}{S_n}\right)D' - 0.5\right)} \tag{11.77}$$

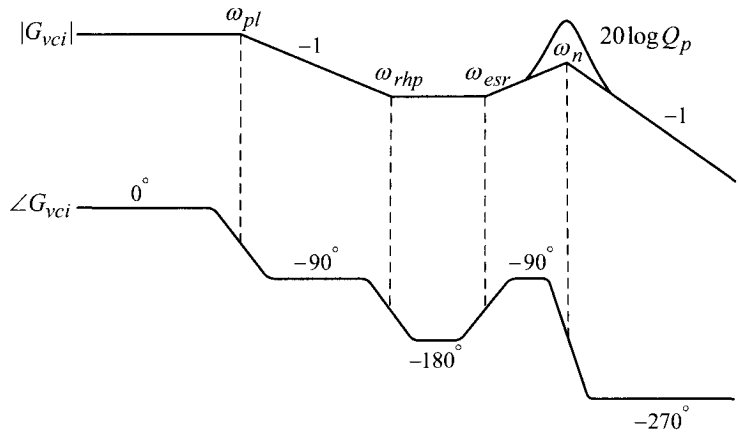


Figure 11.22 Asymptotic plot for $G_{vci}(s)$.

The assumptions used in the previous derivation, $CR \gg T_s/2$, $CR \gg m_c D' T_s$, $L/R_c \gg T_s/2$, and $CRT_s/2 \gg T_s^2/\pi^2$, are easily met in practice. The accuracy of the $G_{vci}(s)$ approximation will be demonstrated in a later example.

For the boost and buck/boost converters, $G_{vci}(s)$ can be derived in the same way and the results are shown in Table 11.3.

Predictions of $G_{vci}(s)$

For the asymptotic plot construction, the G_{vci} expression is repeated below

$$G_{vci}(s) = K_{vc} \frac{\left(1 - \frac{s}{\omega_{rhp}}\right)\left(1 + \frac{s}{\omega_{esr}}\right)}{\left(1 + \frac{s}{\omega_{pl}}\right)\left(1 + \frac{s}{Q_p \omega_n} + \frac{s^2}{\omega_n^2}\right)} \tag{11.78}$$

The noticeable feature of the transfer function is the existence of the quadratic term in the denominator. The quadratic term, which originated from the sampling effects of current mode control, introduces a double pole at half the switching frequency, $\omega_n = \pi/T_s$. The double pole produces a peaking by the amount of $20 \log Q_p$. Figure 11.22 shows the asymptotic plot for $|G_{vci}|$ with conditions $\omega_{pl} \ll \omega_{rhp} \ll \omega_{esr} \ll \omega_n$ and $Q_p > 0.5$.

■ EXAMPLE 11.7 Accuracy of $G_{vci}(s)$ Analysis

This example demonstrates the accuracy of the $G_{vci}(s)$ approximation. Figure 11.23 compares the predictions of (11.78) and the exact small-signal simulations using Fig. 11.20(a). The buck converter used in Example 10.8 is revisited

Table 11.3 Expressions for $G_{vci}(s)$ for Three Basic Converters

Control-to-output transfer function

$$G_{vci}(s) = K_{vc}\frac{\left(1-\frac{s}{\omega_{rhp}}\right)\left(1+\frac{s}{\omega_{esr}}\right)}{\left(1+\frac{s}{\omega_{pl}}\right)\left(1+\frac{s}{Q_p\omega_n}+\frac{s^2}{\omega_n^2}\right)}$$

For all three converters: $Q_p = \dfrac{1}{\pi((1+S_e/S_n)D'-0.5)}$

$$\omega_n = \frac{\pi}{T_s}$$

$$\omega_{esr} = \frac{1}{CR_c}$$

Buck converter

$$K_{vc} = \frac{R}{R_i}\frac{1}{1+\frac{RT_s}{L}(m_cD'-0.5)}$$

$$\omega_{pl} = \frac{1}{CR}+\frac{T_s}{LC}(m_cD'-0.5)$$

$$\omega_{rhp} = \infty$$

Boost converter

$$K_{vc} = \frac{D'R}{2R_i}\frac{1}{1+\frac{D'^3RT_s}{2L}(m_c-0.5)}$$

$$\omega_{pl} = \frac{2}{CR}+\frac{T_sD'^3}{LC}(m_c-0.5)$$

$$\omega_{rhp} = D'^2\frac{R}{L}$$

Buck/boost converter

$$K_{vc} = \frac{D'R}{(1+D)R_i}\frac{1}{1+\frac{D'^3RT_s}{(1+D)L}(m_c-0.5)}$$

$$\omega_{pl} = \frac{1+D}{CR}+\frac{T_sD'^3}{LC}(m_c-0.5)$$

$$\omega_{rhp} = \frac{D'^2}{D}\frac{R}{L}$$

For the buck converter, ω_{rhp} does not exist so $\omega_{rhp} = \infty$ is used.

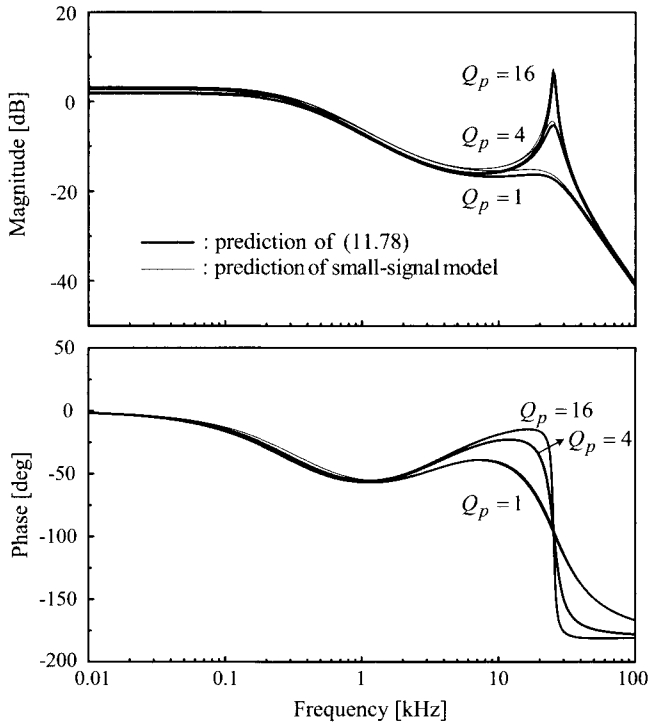


Figure 11.23 Accuracy of $G_{vci}(s)$ approximation with $Q_p = 16, 4$, and 1.

and three different values for Q_p are considered in this analysis: $Q_p = 1$, 4, and 16. The thick curves are the plot of the approximated $G_{vci}(s)$ expression in (11.78). The thin curves are the results of the exact small-signal simulation. Figure 11.24 also shows the $G_{vci}(s)$ prediction of (11.78) for the case of $Q_p = 1.0$, in comparison with the empirical data of the computational method. The close match between the Bode plots and empirical data confirms the accuracy of the $G_{vci}(s)$ approximation.

11.3.3 Control Design Procedures

The most important role of $G_{vci}(s)$ is its use in the control design. Figure 11.25 shows the asymptotic plots for $|G_{vci}|$ and loop gain $|T_m|$. This figure assumes the two-pole one-zero circuit for the voltage feedback compensation

$$F_v(s) = \frac{K_v\left(1 + \dfrac{s}{\omega_{zc}}\right)}{s\left(1 + \dfrac{s}{\omega_{pc}}\right)} \tag{11.79}$$

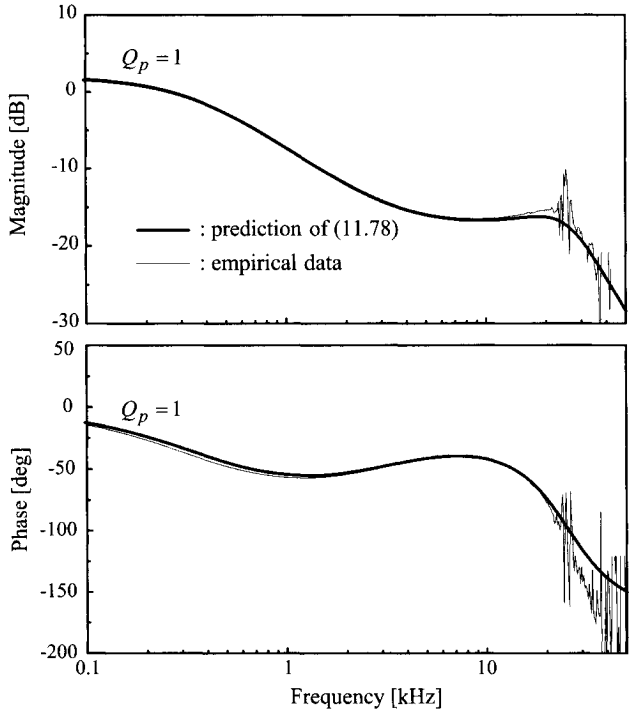


Figure 11.24 Accuracy of G_{vci} (s) approximation with $Q_p = 1$.

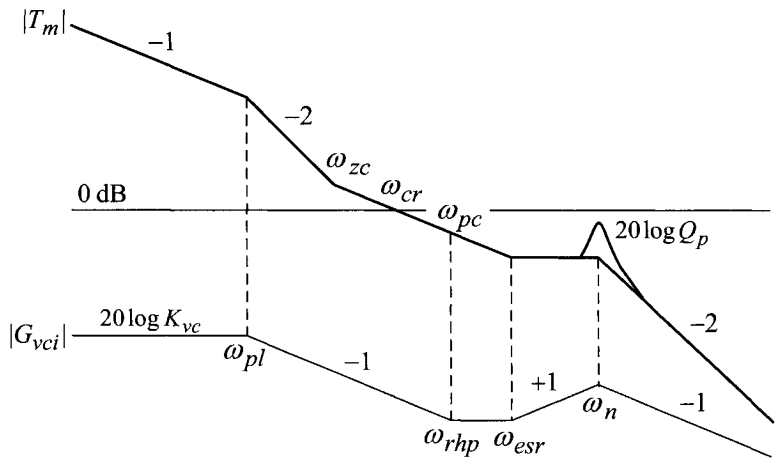


Figure 11.25 Asymptotic plot for $|G_{vci}|$ and $|T_m|$ with two-pole one-zero compensation.

The compensation pole is located at the RHP zero, $\omega_{pc} = \omega_{rhp}$. The compensation zero is placed after the low-frequency pole of G_{vci}, ω_{pl}, but before the loop gain crossover frequency. Details about the compensation parameters will be explained shortly.

The structure and circuit components for the two-pole one-zero compensation were given in Fig. 10.22, along with the equations (10.57) in Section 10.2.5. The profile of the loop gain is very similar to that of the outer loop gain in the previous classical analysis. However, *the loop gain has a double pole at half the switching frequency.* The double pole produces a peaking of 20 log Q_p at $\omega_n = \pi/T_s$. If the peaking is large, the loop gain crosses the 0 dB line at $\omega_n = \pi/T_s$, thereby destablizing the converter.† This becomes the theoretical background for the high-frequency oscillations, often encountered with current mode control. As a simple example, the peaking becomes infinite

$$20\log Q_p = 20\log\left(\frac{1}{\pi((1+S_e/S_n)D' - 0.5)}\right) = \infty \text{ dB} \tag{11.80}$$

when the compensation ramp is absent, $S_e = 0$, and $D' = 0.5$, which are the conditions for the onset of the sub-harmonic oscillation.

The previous discussions naturally conclude that the damping ratio of the double pole, $Q_p = 1/\left(\pi\left((1+S_e/S_n)D' - 0.5\right)\right)$, should be properly controlled to avoid instability due to the excessive peaking. The idea of properly damping the double pole at half the switching frequency leads to an easy and practical design methodology for current mode control.

Current Loop Design

The theme of the current loop design is to control the damping ratio $Q_p = 1/\left(\pi\left((1 + S_e/S_n)D' - 0.5\right)\right)$.

1) Determine the CSN gain R_i such that $i_{L\,peak}R_i < V_{max}$ where V_{max} is the maximum allowable input voltage of the PWM block. The CSN gain R_i affects the on-time slope, S_n, of the current feedback signal.

2) Determine the slope of the compensation ramp, S_e, to provide a damping ratio between $0.3 < Q_p < 1.3$ for the double pole at $\omega_n = \pi/T_s$

$$0.3 < \frac{1}{\pi((1+S_e/S_n)D' - 0.5)} < 1.3 \tag{11.81}$$

This prevents an excessive peaking at half the switching frequency, which could trigger high-frequency oscillations.

†The 0 dB crossing due to the peaking would cause an abrupt decrease in the phase so that the polar plot violates the Nyquist stability criterion.

Voltage Feedback Compensation Design

The voltage feedback compensation is designed to achieve the desirable loop gain characteristics. With the two-pole one-zero compensation, the loop gain is given by

$$\begin{aligned} T_m(s) &= G_{vci}(s)\,F_v(s) \\ &= \underbrace{K_{vc}\frac{\left(1-\dfrac{s}{\omega_{rhp}}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{\left(1+\dfrac{s}{\omega_{pl}}\right)\left(1+\dfrac{s}{Q_p\omega_n}+\dfrac{s^2}{\omega_n^2}\right)}}_{G_{vci}(s)}\ \underbrace{\frac{K_v\left(1+\dfrac{s}{\omega_{zc}}\right)}{s\left(1+\dfrac{s}{\omega_{pc}}\right)}}_{F_v(s)} \end{aligned} \tag{11.82}$$

The design procedures for the voltage feedback compensation are formulated as follows.

1) Place the compensation pole ω_{pc} at the lowest frequency among the RHP zero, esr zero, and half the switching frequency: $\omega_{pc} = \min\{\omega_{rhp}\ \omega_{esr}\ 0.5\,\omega_s\}$.

2) Locate the compensation zero ω_{zc} at the frequencies higher than ω_{pl}, but lower than the power stage double pole ω_o: $\omega_{zc} = (0.6 - 0.8)\omega_o$. Expressions for the power stage double pole ω_o are given in Table 10.2.

3) Select the 0 dB crossover frequency, denoted as ω_{cr} in Fig. 11.25, of the loop gain and determine the integrator gain K_v required for the selected ω_{cr}. The position of ω_{cr} is chosen based on the guidelines established in Chapter 10: $\omega_{cr} = (0.3 - 1.0)\,\omega_{esr}$ for buck converters and $\omega_{cr} = (0.1 - 0.3)\,\omega_{rhp}$ for boost and buck/boost converters. From Fig. 11.25, the following relationship is formulated

$$\left(20\log K_{vc} + 20\log\frac{K_v}{\omega_{pl}}\right) - 40\log\frac{\omega_{zc}}{\omega_{pl}} - 20\log\frac{\omega_{cr}}{\omega_{zc}} = 0\ \text{dB} \tag{11.83}$$

The first term in (11.83) is the magnitude of the loop gain, $|T_m|$, evaluated at ω_{pl}: $|T_m(j\omega_{pl})| = 20\log\left(K_{vc}K_v/\omega_{pl}\right)$. The above equation is converted into the design equation

$$\frac{K_{vc}K_v}{\omega_{pl}}\left(\frac{\omega_{pl}}{\omega_{zc}}\right)^2\frac{\omega_{zc}}{\omega_{cr}} = 1 \tag{11.84}$$

from which the integrator gain is determined as

$$K_v = \frac{\omega_{zc}\,\omega_{cr}}{K_{vc}\,\omega_{pl}} \tag{11.85}$$

The above design procedures are summarized in Table 11.4.

Table 11.4 New Design Procedures for Peak Current Mode Control

Current loop design

$$Q_p = \frac{1}{\pi\left(\left(1 + \frac{S_e}{S_n}\right)D' - 0.5\right)}$$

1) Select the CSN gain R_i such that $i_{L\,peak}R_i < V_{max}$, where V_{max} is the maximum input voltage for the PWM block.
2) Determine Q_p: $0.3 < Q_p < 1.3$
3) Evaluate the compensation ramp slope:

$$S_e = S_n\left(\frac{\frac{1}{\pi Q_p} + 0.5}{D'} - 1\right)$$

Voltage loop design

$$T_m(s) = \underbrace{K_{vc}\frac{\left(1 - \frac{s}{\omega_{rhp}}\right)\left(1 + \frac{s}{\omega_{esr}}\right)}{\left(1 + \frac{s}{\omega_{pl}}\right)\left(1 + \frac{s}{Q_p\omega_n} + \frac{s^2}{\omega_n^2}\right)}}_{G_{vcr}(s)} \underbrace{\frac{K_v\left(1 + \frac{s}{\omega_{zc}}\right)}{s\left(1 + \frac{s}{\omega_{pc}}\right)}}_{F_v(s)}$$

1) Set the compensation pole: $\omega_{pc} = \min\{\omega_{rhp}\ \omega_{esr}\ \omega_s/2\}$.
2) Select the compensation zero: $\omega_{zc} = (0.6 - 0.8)\,\omega_o$. Expressions for ω_o are given in Table 10.2.
3) Set the loop gain crossover frequency ω_{cr}:

   $\omega_{cr} = (0.3 - 1.0)\,\omega_{esr}$ for buck converter

   $\omega_{cr} = (0.1 - 0.3)\,\omega_{rhp}$ for boost and buck/boost converters.

4) Evaluate the integrator gain:

$$K_v = \frac{\omega_{zc}\ \omega_{cr}}{K_{vc}\ \omega_{pl}}$$

5) Check the phase margin and adjust K_v to secure a 45°–70° phase margin.
6) Evaluate the circuit components for voltage feedback compensation using (10.57) in Chapter 10.

For buck converters, ω_{rhp} does not exist so $\omega_{rhp} = \infty$ is used.

■ EXAMPLE 11.8 Buck Converter Design Example

This example illustrates the adaptation of the new design procedures developed in this section. The peak current mode control, employed to the buck converter in Example 10.8, is redesigned in this example. The corner frequencies and operational conditions of the buck converter are $\omega_o = 2\pi \cdot 1.16 \times 10^3$ rad/s, $\omega_{esr} = 2\pi \cdot 3.39 \times 10^3$ rad/s, and $D = 0.25$. The switching frequency is $\omega_s = 2\pi \cdot 50 \times 10^3$ rad/s. The maximum input voltage for the PWM block is assumed as $V_{max} = 5.0$ V and the peak value of the inductor current is calculated as $i_{L\,peak} = 4.75$ A. Based on the new design procedures, the control design is performed below.

Current Loop Design

1) CSN gain:

$$R_i < \frac{V_{max}}{i_{L\,max}} = \frac{5.0}{4.75} = 1.05 \quad \Rightarrow R_i = 0.67$$

2) Damping ratio of double pole:

$$Q_p = \frac{1}{\pi\left(\left(1 + \frac{S_e}{S_n}\right)D' - 0.5\right)} = 1 \quad \text{with}$$

$$S_n = \frac{V_S - V_O}{L} R_i = \frac{10 - 4}{40 \times 10^{-6}} 0.67 = 1.01 \times 10^5 \text{ V/s}$$

$$\Rightarrow \quad S_e = S_n \left(\frac{\frac{1}{\pi Q_p} + 0.5}{D'} - 1 \right)$$

$$= 1.01 \times 10^5 \left(\frac{\frac{1}{\pi\, 1} + 0.5}{0.75} - 1 \right) = 9.2 \times 10^3 \text{ V/s}$$

$$\Rightarrow \quad V_m = S_e T_s = (9.2 \times 10^3)(20 \times 10^{-6}) = 0.18 \text{ V}$$

$$m_c = 1 + \frac{S_e}{S_n} = 1 + \frac{9.2 \times 10^3}{1.01 \times 10^5} = 1.09$$

The slope of the compensation ramp, $S_e = 9.2 \times 10^3$ V/s, is noticeably smaller than that of the conventional design in Example 10.8, $S_e = 1.46 \times 10^5$ V/s. Detailed comparisons between the current design and the earlier design in Example 10.8 will be given later.

Voltage Loop Design

The voltage loop design is performed as follows.

1) Compensation pole: $\omega_{pc} = \omega_{esr} = 2\pi \cdot 3.39 \times 10^3$ rad/s

2) Compensation zero: $\omega_{zc} = 0.8\,\omega_o = 2\pi \cdot 928$ rad/s

3) Loop gain crossover frequency: $\omega_{cr} = \omega_{esr} = 2\pi \cdot 3.39 \times 10^3$ rad/s

4) Integrator gain:

$$K_v = \frac{\omega_{zc}\,\omega_{cr}}{K_{vc}\,\omega_{pl}} \qquad \text{with}$$

$$K_{vc} = \frac{R}{R_i}\frac{1}{1 + \dfrac{RT_s}{L}(m_c D' - 0.5)}$$

$$= \frac{1}{0.67}\frac{1}{1 + \dfrac{1 \cdot 20 \times 10^{-6}}{40 \times 10^{-6}}(1.09 \cdot 0.75 - 0.5)} = 1.29$$

$$\omega_{pl} = \frac{1}{CR} + \frac{T_s}{LC}(m_c D' - 0.5)$$

$$= \frac{1}{470 \times 10^{-6}\,1} + \frac{20 \times 10^{-6}}{40 \times 10^{-6}\,470 \times 10^{-6}}$$

$$\cdot (1.09 \cdot 0.75 - 0.5) = 2\pi \cdot 392 \text{ rad/s}$$

$$\text{Thus,} \quad K_v = \frac{(2\pi \cdot 928)(2\pi \cdot 3.39 \times 10^3)}{(1.29)(2\pi \cdot 392)} = 3.91 \times 10^4$$

5) Voltage feedback circuit: $R_1 = 10\ \text{k}\Omega$

$\Rightarrow R_2 = 92.3\ \text{k}\Omega$, $C_2 = 1.86$ nF, and $C_3 = 0.70$ nF

The design results are the same as those of the classical design in Example 10.8, except for the reduced compensation ramp slope. The theoretical background for this sameness will be discussed in the next section.

Performance of Current Mode Control

The performance of the buck converter with the newly-designed peak current mode control is now evaluated to show the validity of the design procedures and accuracy of the new model. Figure 11.26 shows the loop gain of the converter. The prediction of the new model is compared with the empirical data of the computational method, along with the prediction of the classical model which does not include the sampling effects but has the *same control parameters as those of the new model – that is, the control parameters of the new design.*

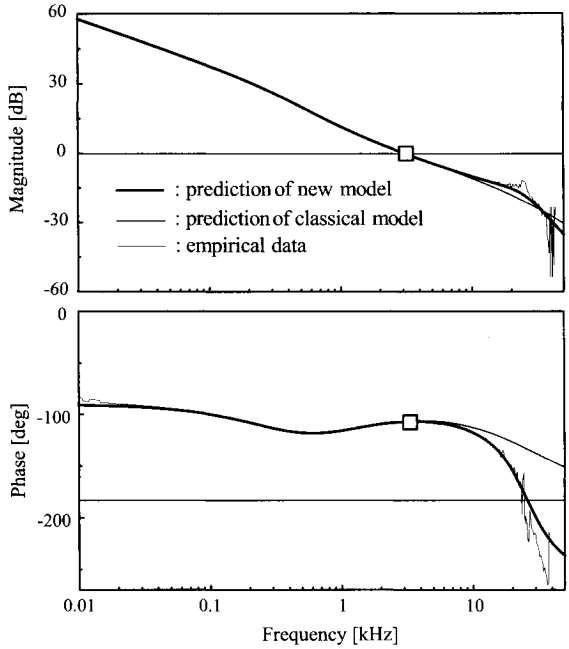


Figure 11.26 Loop gain of buck converter: predictions of new and classical models.

The existence of the double pole at half the switching frequency, which was theoretically predicted by the new model, is well supported by the empirical data. The new model accurately correlates with the empirical data and thus demonstrates notable improvement over the classical model. More specifically, the new model correctly predicts the double pole at half the switching frequency, which is well damped by the design goal of $Q_p = 1$.

The loop gain crossover frequency is located at the exact target frequency of $\omega_{cr} = 2\pi \cdot 3.39 \times 10^3$ rad/s with sufficient phase margin. Figure 11.27(a) shows the output impedance characteristics of the converter. The predictions of the new model and classical model both show a good match with the empirical data. Figure 11.27(b) depicts the audio-susceptibility of the converter. The audio-susceptibility curves show the impacts of the feedforward gains in the new model. The new model shows improved audio-susceptibility characteristics compared to the classical model which assumes the *zero* feedforward gain.

Comparison between New Design and Classical Design

The performance of the new design is compared with that of the previous classical design which was done in Example 10.8 without considering the sampling effects. For this comparative study, the new model developed in this chapter is used for the theoretical predictions of the two designs. The

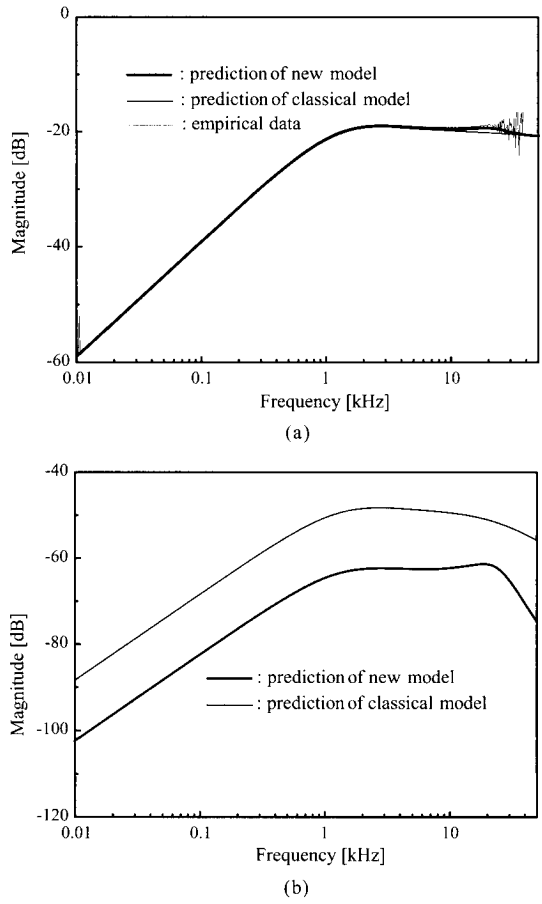


Figure 11.27 Frequency-domain performance of buck converter. (a) Output impedance. (b) Audio-susceptibility.

theoretical predictions are compared with the empirical data. Figure 11.28 compares the loop gain of the two designs. Although the new design and classical design both predict stability with a sufficient phase margin, they show discernible disparities at high frequencies.

As will be demonstrated in the next section, the classical design is in fact an *exact match* to the new design that is executed with the target of $Q_p = 0.4$. Accordingly, the classical design corresponds to the new design with $Q_p = 0.4$, while the current design was performed with the design goal of $Q_p = 1.0$. The difference in Q_p is well reflected in the loop gain characteristics. The classical design shows more gradual changes in high-frequency phase characteristics with a small damping ratio of $Q_p = 0.4$, while the new design exhibits a gain boost at high frequencies with $Q_p = 1$.

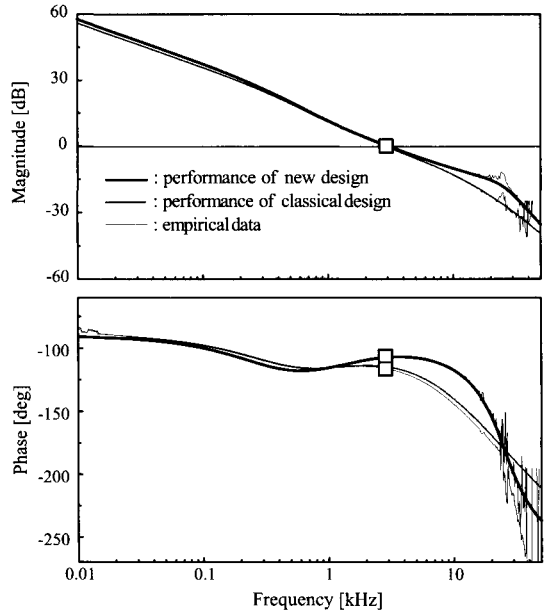


Figure 11.28 Loop gain of buck converter: comparison of new and classical designs.

Figure 11.29 shows the output impedance and audio-susceptibility of the two designs. As shown in Fig. 11.29(a), the two designs do not show any noticeable difference in the output impedance characteristics. However, the new design offers improved audio-susceptibility characteristics. This improvement is due to the reduction in the compensation ramp slope. The compensation ramp slope of the new design, $S_e = 9.2 \times 10^3$ V/s, is much smaller than that of the classical design, $S_e = 1.46 \times 10^5$ V/s. Referring to Section 10.2.2, the smaller ramp slope increases the magnitude of the current loop. The enhanced current loop in turn provides more attenuation for the audio-susceptibility. However, this improvement only occurs in the buck converter. It was shown in Section 10.3.1 that, in the case of the buck converter, the audio-susceptibility is governed by the overall loop gain which is directly affected by the current loop. In contrast, for boost and buck/boost converters, the audio-susceptibility is dictated by the outer loop gain which is not largely influenced by the current loop.

Figure 11.30 compares the time-domain performance. For this analysis, the same time-domain model is used for both the new design and classical design. The only difference is the slope of the compensation ramp. Figure 11.30(a) is the transient response of the output voltage due to the $I_O = 4$ A $\Rightarrow$ 8 A $\Rightarrow$ 4 A changes in the load current, while Fig. 11.30(b) shows the transient waveform of the output voltage in response to the $V_S = 16$ V $\Rightarrow$ 8 V $\Rightarrow$ 16 V changes in the input voltage. The step load responses are identical in both designs, as predicted from the output impedance analysis. On the other hand, the new

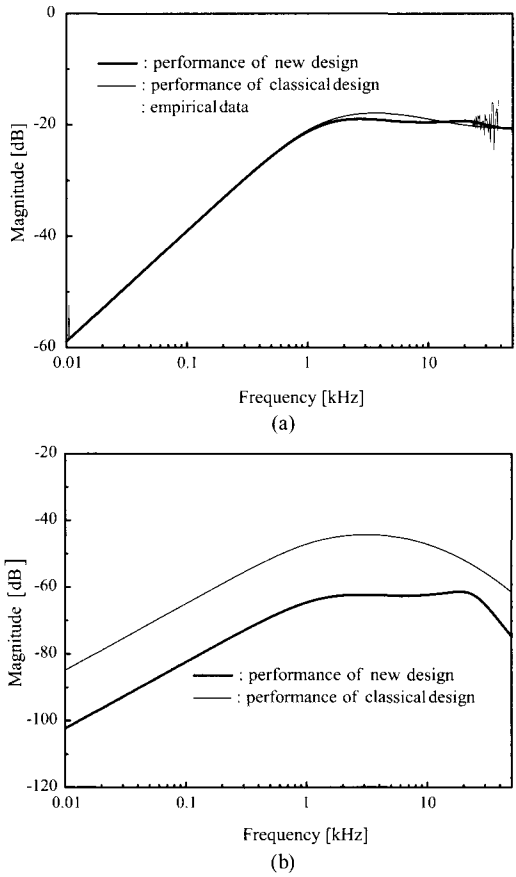


Figure 11.29 Frequency-domain performance of buck converter. (a) Output impedance. (b) Audio-susceptibility.

design shows an improved step input response. This result is consistent with the audio-susceptibility analysis and demonstrates the benefits of the enhanced current loop magnitude.

■ EXAMPLE 11.9 Boost Converter Design Example

The new design procedures are now applied to the boost converter that was used in Example 10.16. The small-signal parameters and operational conditions are $\omega_o = 2\pi \cdot 348$ rad/s, $\omega_{rhp} = 2\pi \cdot 1.79 \times 10^3$ rad/s, $\omega_{esr} = 2\pi \cdot 6.77 \times 10^3$ rad/s, and $D = 0.4$. The switching frequency is $\omega_s = 2\pi \cdot 50 \times 10^3$ rad/s and the maximum input voltage of PWM block is $V_{max} = 5.0$ V. The peak value of

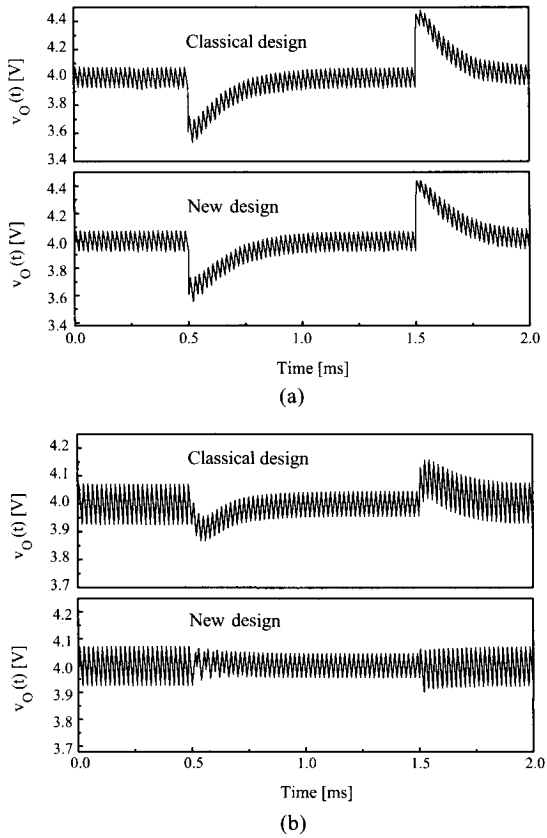


Figure 11.30 Time-domain performance of buck converter. (a) Step load response. (b) Step input response.

the inductor current is $i_{L\,peak} = 6.97$ A. The new design procedures are now adapted to these conditions.

Current Loop Design

1) CSN gain:

$$R_i < \frac{V_{max}}{i_{L\,peak}} = \frac{5.0}{6.97} = 0.72 \quad \Rightarrow R_i = 0.67$$

2) Damping ratio of double pole:

$$Q_p = \frac{1}{\pi\left(\left(1 + \frac{S_e}{S_n}\right)D' - 0.5\right)} = 1 \quad \text{with}$$

$$S_n = \frac{V_S}{L}R_i = \frac{12}{160\times10^{-6}}0.67 = 5.03\times10^4 \text{ V/s}$$

$$\Rightarrow S_e = S_n\left(\frac{\frac{1}{\pi Q_p}+0.5}{D'}-1\right)$$

$$= 5.03\times10^4\left(\frac{\frac{1}{\pi\,1}+0.5}{0.6}-1\right) = 1.83\times10^4 \text{ V/s}$$

$$\Rightarrow V_m = S_eT_s = 1.83\times10^4\,20\times10^{-6} = 0.37 \text{ V}$$

$$m_c = 1+\frac{S_e}{S_n} = 1+\frac{1.83\times10^4}{5.03\times10^4} = 1.36$$

Voltage Loop Design

1) Compensation pole: $\omega_{pc} = \omega_{rhp} = 2\pi\cdot 1.79\times10^3$ rad/s

2) Compensation zero: $\omega_{zc} = 0.8\,\omega_o = 2\pi\cdot 278$ rad/s

3) Loop gain crossover frequency: $\omega_{cr} = 0.28\,\omega_{rhp} = 2\pi\cdot 501$ rad/s

4) Integrator gain:

$$K_v = \frac{\omega_{zc}\,\omega_{cr}}{K_{vc}\,\omega_{pl}} \qquad \text{with}$$

$$K_{vc} = \frac{D'R}{2R_i}\frac{1}{1+\frac{D'^3RT_s}{2L}(m_c-0.5)}$$

$$= \frac{0.6\cdot5}{2\cdot0.67}\frac{1}{1+\frac{0.6^3\,5\cdot20\times10^{-6}}{2\cdot160\times10^{-6}}(1.36-0.5)} = 2.12$$

$$\omega_{pl} = \frac{2}{CR}+\frac{T_sD'^3}{LC}(m_c-0.5)$$

$$= \frac{2}{470\times10^{-6}\,5}+\frac{20\times10^{-6}\,0.6^3}{(160\times10^{-6})(470\times10^{-6})}$$

$$\cdot(1.36-0.5) = 2\pi\cdot143 \text{ rad/s}$$

$$\text{Thus,}\quad K_v = \frac{(2\pi\cdot278)(2\pi\cdot501)}{2.12\,(2\pi\cdot143)} = 2.88\times10^3$$

5) Voltage feedback circuit: $R_1 = 10\text{ k}\Omega$

$\Rightarrow R_2 = 19.6\text{ k}\Omega$, $C_2 = 29.2$ nF, and $C_3 = 5.38$ nF

The design results are identical to those of the classical design in Example 10.16, except for the reduced compensation ramp slope. The compensation

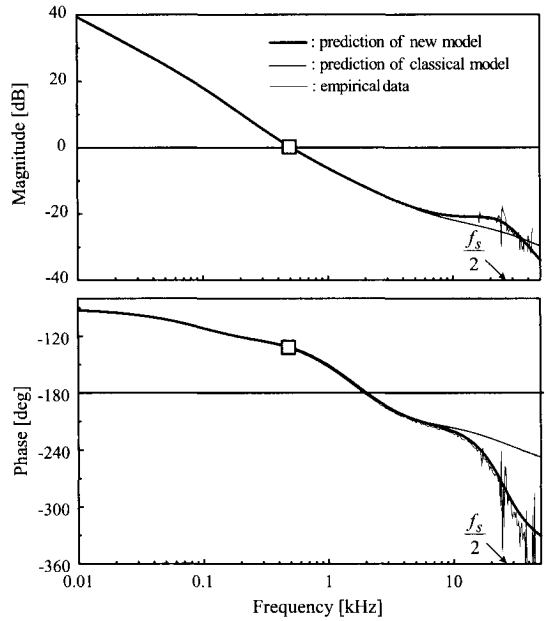


Figure 11.31 Loop gain of boost converter: prediction of new and classical models.

ramp slope of the new design is $S_e = 1.83 \times 10^4$ V/s, while that of the classical design is $S_e = 7.50 \times 10^4$ V/s.

Performance of Current Mode Control

The loop gain of the boost converter is shown in Fig. 11.31. The loop gain is displayed using the new model and the classical model, together with the empirical data. The loop gain exhibits an exact match to the design target of $\omega_{cr} = 2\pi \cdot 501$ rad/s with sufficient phase margin. The new model also shows good correlations to the empirical result and demonstrates improved model accuracy over the classical model. The double pole at half the switching frequency is evident in the new model prediction and empirical result. Figure 11.32 shows the output impedance and audio-susceptibility of the boost converter. Here, both the classical model and new model show good correspondence to the empirical data.

Comparison between New Design and Classical Design

In Fig. 11.33, the loop gain characteristics of the new design are compared with those of the classical design which was done in Example 10.16 without considering the sampling effects. The new model incorporating the sampling effects is used to access loop gain characteristics of the two designs. Both

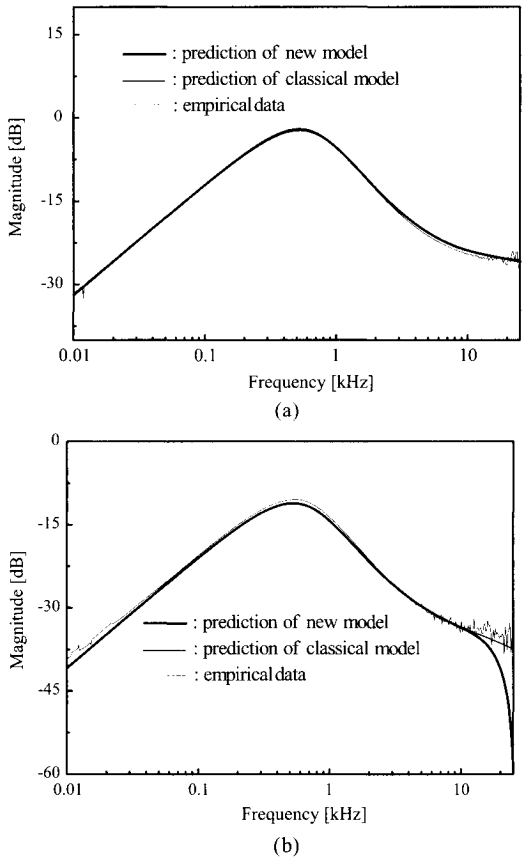


Figure 11.32 Frequency-domain performance of boost converter. (a) Output impedance. (b) Audio-susceptibility.

designs show good loop gain characteristics and also exhibit close agreement with the empirical data. It can be shown that the classical design is an exact match to the new design with $Q_p = 0.32$. On the other hand, the current design is done with the goal of $Q_p = 1.0$. This apparent difference in Q_p values is well shown in the loop gain characteristics.

11.3.4 Correlation between New and Classical Design Procedures

The control design procedures developed in this chapter are different from those of Chapter 10. The new design procedures explicitly incorporate the sampling effects of the peak current mode control. In contrast, the classical design does not consider the sampling effects at all. Nonetheless, the two design procedures showed remarkable similarity, as illustrated in Examples 11.8 and 11.9. Theoretical

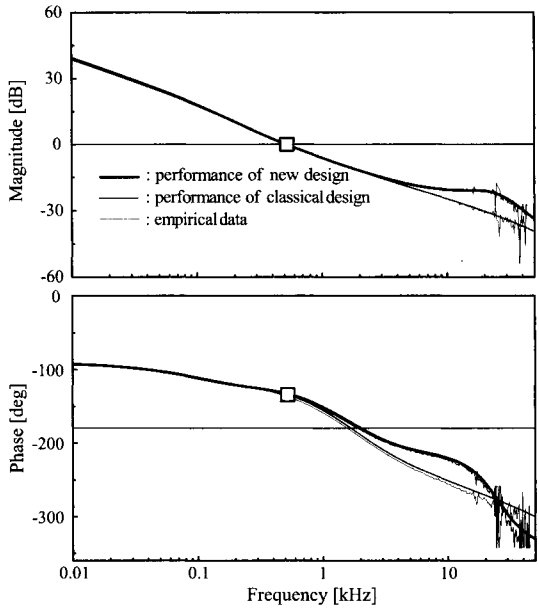


Figure 11.33 Loop gain of boost converter: comparison of new and classical designs.

backgrounds behind this similarity are explored in this section. The current loop designs are first investigated and the voltage loop designs are subsequently compared.

Current Loop Design

The goal of the new current loop design is to provide a predetermined value for Q_p. On the other hand, the classical design targets to place the crossover frequency of the current loop at the desired frequency. Although the objectives of the two designs are distinct, the means of obtaining their goal is the same. Once the power stage and CSN parameters are determined, the only remaining design freedom is the slope of the compensation ramp.

The new design attempts to provide a desired Q_p value by adjusting the compensation ramp slope S_e in the following expression

$$Q_p = \frac{1}{\pi\left(\left(1 + \frac{S_e}{S_n}\right)D' - 0.5\right)} \tag{11.86}$$

The classical design aims to adjust the ratio of the current-loop crossover frequency to the switching frequency, ω_{ci}/ω_s, by controlling S_e in the following equation

$$\frac{\omega_{ci}}{\omega_s} = \frac{K_{id}R_i\dfrac{\omega_o^2}{\omega_{id}}\dfrac{2}{(S_n - S_f + 2S_e)T_s}}{\dfrac{2\pi}{T_s}} \tag{11.87}$$

The above design equation is obtained from (10.47) and (10.48) in Chapter 10. An explicit correlation between the new and classical designs can be established using (11.86) and (11.87), as illustrated in the following example.

■ EXAMPLE 11.10 Buck and Boost Converter Examples

The buck converter in Example 11.8 is used as the first example to illustrate the connection between Q_p in the new design and ω_{ci}/ω_s in the classical design. Figure 11.34(a) is the Q_p–ω_{ci}/ω_s curve, obtained by relating (11.86) and (11.87) with the given power stage parameters and operational conditions. First, the required S_e value for a specific Q_p is calculated using (11.86). The ratio of ω_{ci}/ω_s is then evaluated from (11.87) using the calculated S_e value. By repeating this process, the continuous Q_p–ω_{ci}/ω_s curve is obtained. The curve is evaluated for $0.3 < Q_p < 1.3$. Figure 11.34(a) reveals a linear relationship between Q_p and ω_{ci}/ω_s. For one example, the goal of $Q_p = 0.5$ in the new design requires the S_e value that offers the condition $\omega_{ci}/\omega_s = 0.25$ in the classical design. As another example, the design aim of $Q_p = 1$ in the new design translates to the condition $\omega_{ci}/\omega_s = 0.5$ in the classical design: that is, placing the current loop crossover frequency at half the switching frequency. Furthermore, selecting the damping ratio between $0.3 < Q_p < 1.3$ in the new design is equivalent to placing the constraint $0.15 < \omega_{ci}/\omega_s < 0.65$ in the classical design.

Figure 11.34(b) shows the Q_p–ω_{ci}/ω_s curve for the boost converter used in Example 11.9. Interestingly, the curve is identical to that of Fig. 11.34(a). The sameness in Fig. 11.34(a) and Fig. 11.34(b) is actually the expected and logical consequential effect of a general relationship that links Q_p and ω_{ci}/ω_s. The exact description of this relationship is given below.

As demonstrated in the previous example, a direct correlation exists between the new and classical designs. In fact, it can be proved that the following relationship holds true

$$\frac{\omega_{ci}}{\omega_s} = \frac{Q_p}{2} \tag{11.88}$$

for all the three basic dc-to-dc converters, regardless of the operational conditions and power stage parameters. The sameness between Figs. 11.34(a) and 11.34(b) is now self-evident from (11.88). The verification of (11.88) is given in Example 11.11.

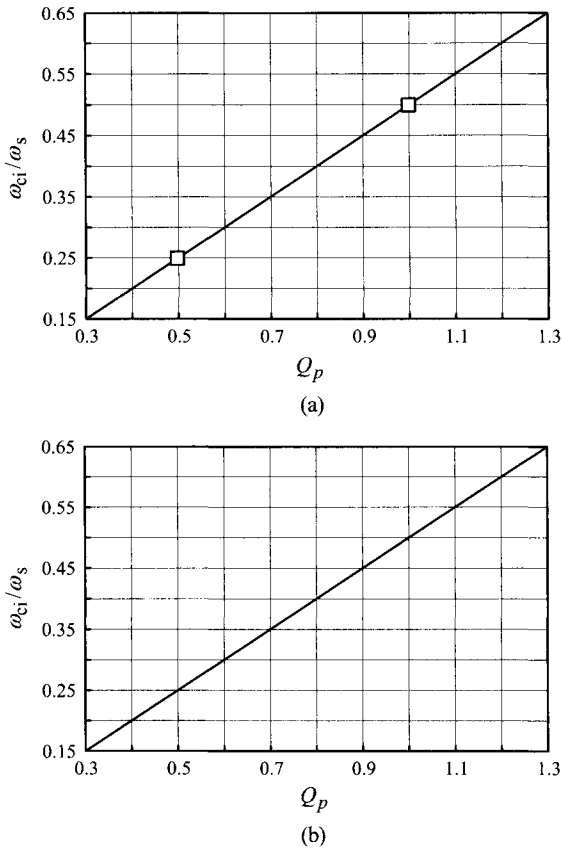


Figure 11.34 Relationship between Q_p and ω_{ci}/ω_s. (a) Buck converter in Example 11.8. (b) Boost converter in Example 11.9.

■ EXAMPLE 11.11 Derivation of $\omega_{ci}/\omega_s = Q_p/2$ for Buck Converter

This example shows the validity of (11.88) using the buck converter. First, the following two identities are derived for the buck converter

$$K_{id}R_i\frac{\omega_o^2}{\omega_{id}} = \frac{V_S}{R}R_i\frac{\frac{1}{LC}}{\frac{1}{CR}} = \frac{V_S}{L}R_i \tag{11.89}$$

and

$$\frac{2}{(S_n - S_f + 2S_e)T_s} = \frac{2}{\left(S_n(2m_c - 1) - S_f\right)T_s}$$

$$= \frac{2}{\left(\frac{V_S - V_O}{L} R_i(2m_c - 1) - \frac{V_O}{L} R_i\right) T_s}$$

$$= \frac{L}{2R_i V_S} \frac{2}{(m_c D' - 0.5) T_s} \tag{11.90}$$

with

$$m_c = 1 + \frac{S_e}{S_n}$$

Using (11.89) and (11.90), the equation (11.87) is written as

$$\frac{\omega_{ci}}{\omega_s} = \frac{K_{id} R_i \frac{\omega_o^2}{\omega_{id}} \frac{2}{(S_n - S_f + 2S_e) T_s}}{\frac{2\pi}{T_s}}$$

$$= \frac{\left(\frac{V_S}{L} R_i\right)\left(\frac{L}{2R_i V_S} \frac{2}{(m_c D' - 0.5) T_s}\right)}{\frac{2\pi}{T_s}}$$

$$= \frac{1}{2\pi(m_c D' - 0.5)} = \frac{1}{2\pi\left(\left(1 + \frac{S_e}{S_n}\right) D' - 0.5\right)} 1 = \frac{Q_p}{2} \tag{11.91}$$

The same procedures can be applied to the boost and buck/boost converters to show that the relationship $\omega_{ci}/\omega_s = Q_p/2$ is always valid for all the three basic PWM converters.

Voltage Loop Design

The objective of the voltage loop design is to select the three parameters, ω_{pc}, ω_{zc}, and K_v, for the two-pole one-zero compensation. The selection of ω_{pc} and ω_{zc} is same in both the new design and the classical design. The only difference exists in the selection of K_v.

In the new design, the integrator gain K_v in (11.85) is selected from

$$K_v = \frac{1}{K_{vc}\, \omega_{pl}} \omega_{zc}\, \omega_{cr} \tag{11.92}$$

where ω_{cr} is the desired crossover frequency of the loop gain $T_m(s)$. In the classical design, K_v in (10.53) is determined from

$$K_v = \frac{1}{\frac{K_{vd}}{K_{id} R_i} \omega_{id}} \omega_{zc}\, \omega_{cr} \tag{11.93}$$

where ω_{cr} is the desired crossover frequency of the outer loop gain $T_2(s)$. For most designs, the following relationship holds true for the three basic PWM converters

$$K_{vc}\,\omega_{pl} \approx \frac{K_{vd}}{K_{id}R_i}\omega_{id} \tag{11.94}$$

as will be shown in Example 11.12. Accordingly, if the same ω_{cr} is selected in the two designs, the required K_v is practically identical. Now, all the three parameters, ω_{pc}, ω_{zc}, and K_v, are the same in the two design approaches.

■ EXAMPLE 11.12 Buck Converter Example

This example shows the validity of (11.94). For the buck converter, it follows that

$$K_{vc} = \frac{R}{R_i}\frac{1}{1+\dfrac{RT_s}{L}(m_cD'-0.5)} \approx \frac{R}{R_i} \tag{11.95}$$

with the condition $1 \gg RT_s(m_cD'-0.5)/L$. In addition, it becomes that

$$\omega_{pl} = \frac{1}{CR} + \frac{T_s}{LC}(m_cD'-0.5) \approx \frac{1}{CR} \tag{11.96}$$

with the assumption $1/(CR) \gg T_s(m_cD'-0.5)/(LC)$. On the other hand, from the power stage transfer functions, it can be shown that

$$\frac{K_{vd}}{K_{id}R_i} = \frac{R}{R_i} \tag{11.97}$$

and

$$\omega_{id} = \frac{1}{CR} \tag{11.98}$$

From the expressions (11.95) through (11.98), the relationship (11.94) is inferred

$$K_{vc}\omega_{pl} = \frac{R}{R_i}\frac{1}{CR} \approx \frac{K_{vd}}{K_{id}R_i}\omega_{id} \tag{11.99}$$

This approximation is very accurate because the conditions $1 \gg RT_s(m_cD'-0.5)/L$ and $1/(CR) \gg T_s(m_cD'-0.5)/(LC)$ are well satisfied for most designs. The validity of (11.94) was demonstrated in Examples 11.8 and 11.9.

Final Remarks

The analysis of the sampling effects has led to the new design procedures for the peak current mode control. This alternative design controls the damping ratio in the control-to-output transfer function so that the sampling effects neither cause stability problems nor interfere with the closed-loop performance. The rationale of the new design is utterly different from that of the previous classical design which does not

consider the sampling effects at all. Nonetheless, the results of the two designs markedly resemble each other.

The voltage loop designs in the two approaches yield identical results, given that the loop gain crossover frequency of the new design is the same as the crossover frequency of the outer loop gain in the classical design.

The current loop designs are intimately connected by the relationship, $\omega_{ci}/\omega_s = Q_p/2$. If this information is incorporated in the current loop design, the results of the two designs should be the same. More importantly, *if the conservative design constraint,* $0.15 < \omega_{ci}/\omega_s < 0.3$, *is imposed on the classical design as recommended in Chapter 10, the performance of the converter is not adversely affected by the sampling effect of current mode control.* This is because the design constraint of $0.15 < \omega_{ci}/\omega_s < 0.3$ is the same as the requirement of $0.3 < Q_p < 0.6$, which avoids the detrimental consequence of the sampling effects. Now, the conservative design guideline of $0.15 < \omega_{ci}/\omega_s < 0.3$ is relaxed to a less restrictive condition of $0.15 < \omega_{ci}/\omega_s < 0.65$ with the knowledge of the sampling effects of current mode control.

In conclusion, either the classical design or the new design can be adapted for the three basic PWM converters, as long as the design constraint $0.15 < \omega_{ci}/\omega_s < 0.65$ is used in the classical design, or the equivalent condition $0.3 < Q_p < 1.3$ is incorporated in the new design. For this case, both the new and classical design offer stability and good closed-loop performance. Furthermore, there is an exact one-to-one correspondence, matched by the condition $\omega_{ci}/\omega_s = Q_p/2$, between the two designs. For example, the classical design with $\omega_{ci}/\omega_s = 0.5$ can be interpreted as the new design with $Q_p = 1$ because they are in fact the same design.

11.4 OFF-LINE FLYBACK CONVERTER WITH OPTOCOUPLER-ISOLATED CURRENT MODE CONTROL

This section deals with the design and analysis of the optocoupler-isolated peak current mode control. A flyback converter, which functions as a rear-end dc-to-dc converter in an off-line power supply, is used to illustrate all the details involved with practical applications of the peak current mode control.

11.4.1 Off-Line Power Supplies

Off-line power supplies refer to the power converters that receive an ac voltage from the utility line and provide a dc voltage to the load. Figure 11.35 is the functional diagram of a typical off-line power supply. The system consists of an ac-to-dc rectifier, filter capacitor C_F, and dc-to-dc converter. The front-end ac-to-dc rectifier converts the ac utility voltage into an intermediate dc voltage. The rear-end dc-to-dc converter then alters the intermediate voltage into the voltage level required by the load.

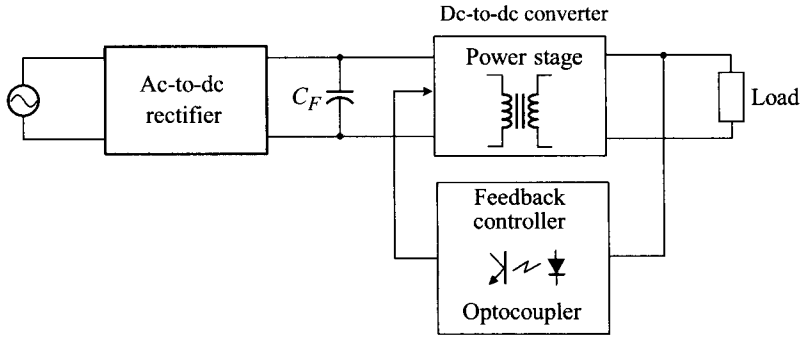


Figure 11.35 Structure of off-line power supplies.

The ac-to-dc rectifier comes in a wide variety in structure and function, ranging from simple line-frequency rectifiers to sophisticated power factor corrected (PFC) ac-to-dc converters. An introduction to a PFC ac-to-dc converter was given in Section 10.1.3. A large filter capacitor C_F is connected at the output of the ac-to-dc rectifier to stabilize the intermediate dc voltage.

The rear-end dc-to-dc converter is required by law to provide galvanic isolation for practical reasons such as safety. The isolation should be provided in both the power stage and feedback controller. For the power stage isolation, one of the transformer-isolated topologies is employed. For the feedback isolation, the controller typically employs an optocoupler which couples the infrared diode and photo-transistor in order to transmit the control signal with isolation. This optocoupler-isolated feedback control is widely adapted to cost-sensitive applications such as off-line power supplies for consumer electronics.

11.4.2 Current Mode Control for Flyback Converter with Optocoupler-Isolated Feedback

The flyback converter is widely used for off-line power supplies because it provides the power stage isolation with minimal component count. The off-line flyback converter usually adapts the peak current mode control using the optocoupler-isolated feedback technique.

Figure 11.36 shows the conceptual circuit diagram of an off-line power supply configured using a flyback converter with an optocoupler-isolated feedback control. A simple bridge rectifier converts the ac line voltage to a dc voltage for the flyback converter downstream. An EMI filter is placed in front of the bridge rectifier and a large filter capacitor C_F is employed at the output of the rectifier. The flyback converter employs the peak current mode control implemented with an optocoupler-isolated feedback controller.

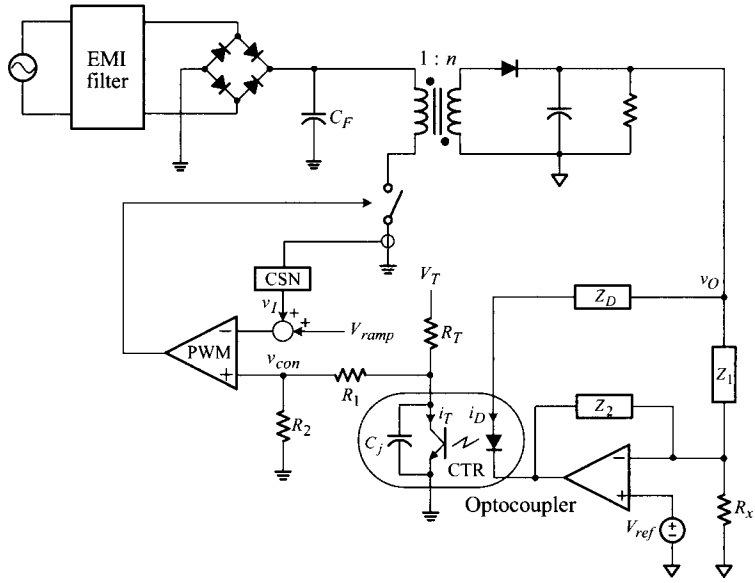


Figure 11.36 Optocoupler-isolated current-mode controlled flyback converter.

Optocoupler-Isolated Feedback Circuit

The flyback converter adopts the standard optocoupler-isolated feedback circuit, illustrated in Fig. 11.36. The resistor R_x is employed to adjust the output voltage V_O with a fixed reference voltage V_{ref}: $V_O = V_{ref}(1 + Z_1(j0)/R_x)$. The infrared diode in the optocoupler is powered by the output voltage v_O through the current limiting circuit, represented by its impedance $Z_D(s)$ in Fig. 11.36. The dc voltage V_T and resistance R_T allow the photo-transistor in the optocoupler to deliver the current i_T in proportion to the infrared diode current i_D. The two gain blocks, $Z_1(s)$ and $Z_2(s)$, represent the impedances of the passive circuit components in the voltage feedback circuit.

The electrical characteristics of the optocoupler are specified by two parameters. The first is the ratio of the photo-transistor current i_T to the infrared diode current i_D. This ratio is referred to as the current transfer ratio, CTR $\equiv i_T/i_D$. The other parameter is the parasitic capacitance between the collector and emitter terminals of the photo-transistor, denoted as C_j. Because these parameters could vary widely with the operational conditions of the optocoupler, their actual values at the given operating point need to be experimentally measured. A simple method to measure the CTR and C_j of an optocoupler is described in Example 11.13.

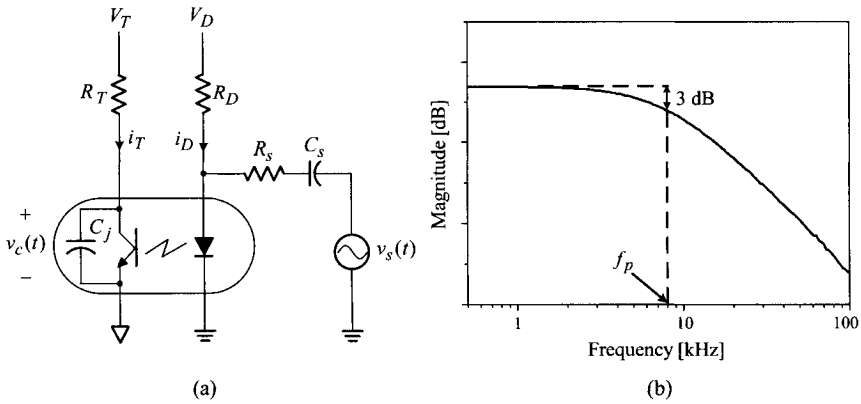


Figure 11.37 Measurement of optocoupler parameters. (a) Measurement circuit. (b) Measurement result.

■ EXAMPLE 11.13 Measurement of Optocoupler Parameters

Figure 11.37(a) shows a simple circuit to measure the current transfer ratio CTR and parasitic capacitor C_j of an optocoupler. The circuit parameters, R_T, V_T, R_D, and V_D, are selected to result in the actual operational conditions of the optocoupler in the converter. Under this condition, the ratio i_T to i_D is measured to yield the current transfer ratio, CTR = i_T/i_D. In this experiment, the small-signal source $v_s(t)$ is not activated.

Next, the small-signal source $v_s(t)$ is activated and the frequency response of $|v_c(j\omega)|/|v_s(j\omega)|$ is recorded using an impedance analyzer. Figure 11.37(b) shows an example of such measurements. The frequency response exhibits the first-order low-pass filter characteristics, whose corner frequency is given by

$$f_p = \frac{1}{2\pi C_j R_T} \tag{11.100}$$

under the condition $C_s(R_s \parallel R_D) \ll C_j R_T$. This equation can be used to determine the value of C_j with a predetermined R_T.

Peak Current Mode Control

The peak current mode control is adapted to the optocoupler-isolated feedback circuit, as shown in Fig. 11.36. The switch current is sensed with the current sensing network (CSN) and combined with the compensation ramp V_{ramp}. The resulting signal is compared with the output of the optocoupler-isolated feedback circuit, v_{con}, in order to generate the PWM output. The techniques for the analysis and design of the conventional peak current mode control can be readily extended to Fig. 11.36 with minor modifications, as will be illustrated in later sections.

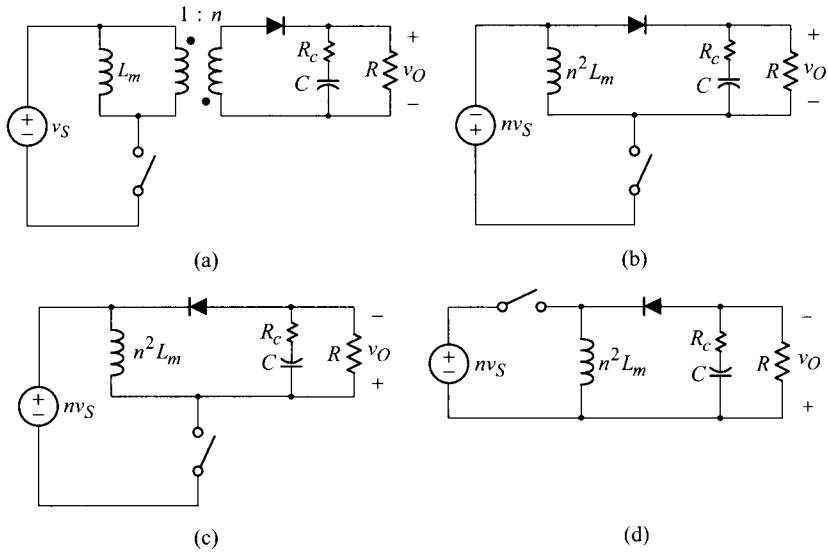


Figure 11.38 Simplification of power stage circuit. (a) Flyback converter. (b) Reflection of input voltage and magnetizing inductance. (c) Modified circuit. (d) Equivalent buck/boost converter.

Small-Signal Model

As discussed in Chapter 9, the flyback converter can be transformed into an equivalent buck/boost converter. Figure 11.38 shows the steps of the circuit transformation described in Section 9.1.3.

Figure 11.39 shows the small-signal model of the flyback converter, obtained by merging the small-signal model of the equivalent buck/boost converter and s-domain model for current mode control. In the small-signal model, the CSN gain is given by

$$R_i' = nR_i \tag{11.101}$$

where R_i is the CSN gain of the original flyback circuit and n is the turns ratio of the transformer. This modification is necessary because the current feedback signal is extracted from the secondary side in the small-signal model, while the current feedback is actually employed to the primary side in the original flyback circuit. The gain block $F_v(s)$ represents the transfer function of the optocoupler feedback circuit.

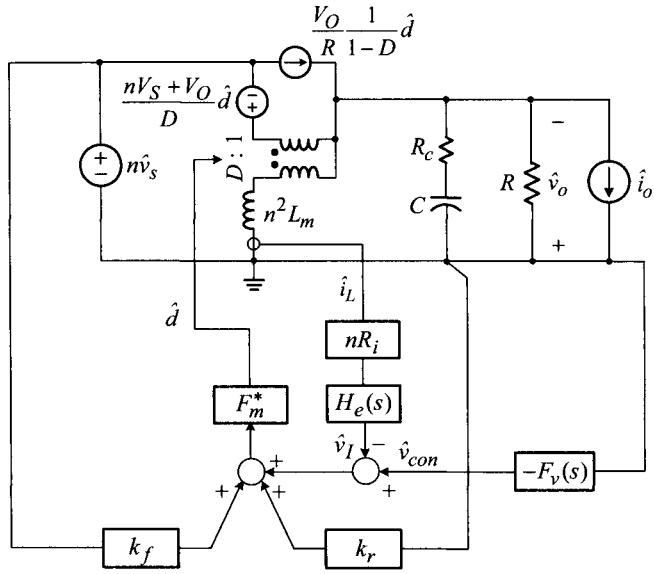


Figure 11.39 Small-signal model of flyback converter.

Optocoupler-Isolated Feedback Circuit

The optocoupler feedback circuit in Fig. 11.36 is redrawn in Fig. 11.40(a). This circuit can be configured into the two-pole one-zero circuit

$$F_v(s) = \frac{K_v\left(1+\dfrac{s}{\omega_{zc}}\right)}{s\left(1+\dfrac{s}{\omega_{pc}}\right)} \tag{11.102}$$

or three-pole two-zero circuit

$$F_v'(s) = \frac{K_v\left(1+\dfrac{s}{\omega_{zc}}\right)\left(1+\dfrac{s}{\omega_{zc}'}\right)}{s\left(1+\dfrac{s}{\omega_{pc}}\right)\left(1+\dfrac{s}{\omega_{pc}'}\right)} \tag{11.103}$$

by appropriately selecting the impedances, $Z_D(s)$, $Z_1(s)$, and $Z_2(s)$. Figure 11.40(b) shows the circuit implementation of the two-pole one-zero circuit, while Fig. 11.40(c) depicts the three-pole two-zero circuit. The expressions for the dc gain and corner frequencies of the two transfer functions are shown in Table 11.5. Derivations of the equations (11.102) and (11.103) are given in Example 11.14.

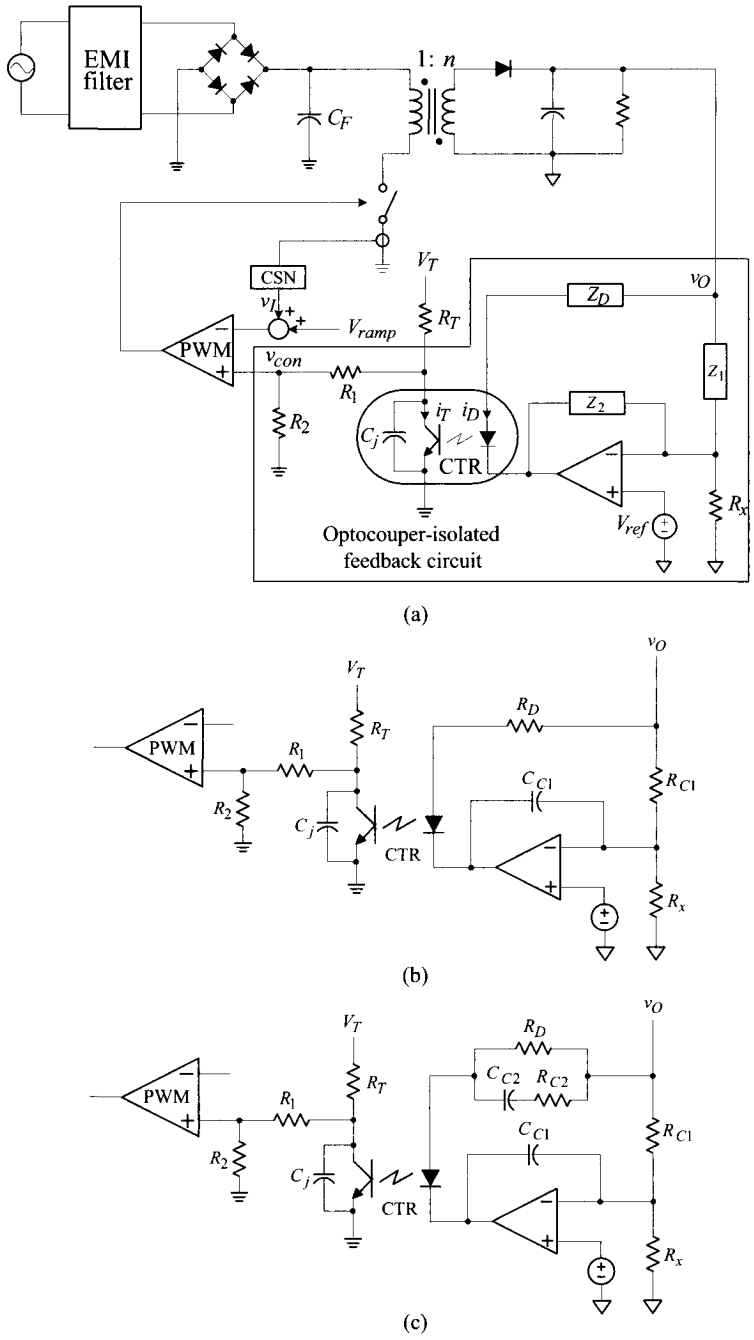


Figure 11.40 Optocoupler-isolated feedback circuit. (a) Voltage feedback circuit. (b) Two-pole one-zero circuit. (c) Three-pole two-zero circuit.

■ EXAMPLE 11.14 Analysis of Optocoupler-Isolated Feedback Circuit

This example shows the derivation of the transfer function of the optocoupler-isolated feedback circuit. Referring to Fig. 11.40(a), the voltage feedback compensation is given by

$$F_v(s) = -\frac{\hat{v}_{con}(s)}{\hat{v}_o(s)} = -\frac{\hat{i}_D(s)}{\hat{v}_o(s)}\frac{\hat{i}_T(s)}{\hat{i}_D(s)}\frac{\hat{v}_{con}(s)}{\hat{i}_T(s)} \tag{11.104}$$

The first term in the right-hand side of (11.104) is evaluated as follows. By recognizing that the inverting terminal of the error amplifier is the virtual ground for the ac signal, the relationship between $\hat{v}_o$ and $\hat{i}_D$ is given by

$$\hat{i}_D(s) = \frac{\hat{v}_o(s) - \left(-\dfrac{Z_2(s)}{Z_1(s)}\right)\hat{v}_o(s)}{Z_D(s)} \tag{11.105}$$

which is rearranged as

$$\frac{\hat{i}_D(s)}{\hat{v}_o(s)} = \frac{1}{Z_D(s)}\left(1 + \frac{Z_2(s)}{Z_1(s)}\right) \tag{11.106}$$

The second term in (11.104) is the current transfer ratio CTR of the optocoupler.

By considering the photo-transistor as a small-signal current source $\hat{i}_T$ in Fig. 11.40(a), the following relationship is formulated

$$\hat{v}_{con}(s) = -\left(\frac{1}{sC_j} \parallel R_T \parallel (R_1 + R_2)\right)\left(\frac{R_2}{R_1 + R_2}\right)\hat{i}_T(s) \tag{11.107}$$

yielding the description

$$\frac{\hat{v}_{con}(s)}{\hat{i}_T(s)} = -\frac{R_T \parallel (R_1 + R_2)}{1 + sC_j\left(R_T \parallel (R_1 + R_2)\right)}\left(\frac{R_2}{R_1 + R_2}\right) \tag{11.108}$$

By combining (11.106) and (11.108), the transfer function of the feedback circuit is given by

$$\begin{aligned} F_v(s) &= \frac{R_2}{R_1 + R_2}\frac{R_T \parallel (R_1 + R_2)}{Z_D(s)}\text{CTR} \\ &\quad \cdot\left(1 + \frac{Z_2(s)}{Z_1(s)}\right)\frac{1}{1 + sC_j\left(R_T \parallel (R_1 + R_2)\right)} \end{aligned} \tag{11.109}$$

The above transfer function can be converted into either the two-pole one-zero or three-pole two-zero circuit. The circuit in Fig. 11.40(b) becomes the two-pole one-zero compensation with the selection of $Z_D(s) = R_D$, $Z_1(s) = R_{C1}$, and $Z_2(s) = 1/(sC_{C1})$. The resulting transfer function is denoted as $F_v(s)$ in Table 11.5. On the other hand, in the circuit in Fig. 11.40(c), where $Z_D(s) = R_D \parallel$

Table 11.5 Expressions for Dc Gain and Corner Frequencies of Optocoupler-Isolated Feedback Circuit Transfer Functions

Transfer function	
$F_v(s) = \dfrac{K_v\left(1+\dfrac{s}{\omega_{zc}}\right)}{s\left(1+\dfrac{s}{\omega_{pc}}\right)}$	$F_v'(s) = \dfrac{K_v\left(1+\dfrac{s}{\omega_{zc}}\right)\left(1+\dfrac{s}{\omega_{zc}'}\right)}{s\left(1+\dfrac{s}{\omega_{pc}}\right)\left(1+\dfrac{s}{\omega_{pc}'}\right)}$
$K_v = \dfrac{R_2}{R_1+R_2}\dfrac{R_T \parallel (R_1+R_2)}{R_D}\text{CTR}\dfrac{1}{C_{C1}R_{C1}}$	
$\omega_{pc} = \dfrac{1}{C_j\left(R_T \parallel (R_1+R_2)\right)}$	$\omega_{pc}' = \dfrac{1}{C_{C2}R_{C2}}$
$\omega_{zc} = \dfrac{1}{C_{C1}R_{C1}}$	$\omega_{zc}' = \dfrac{1}{C_{C2}(R_{C2}+R_D)}$

$\left(R_{C2}+1/(sC_{C2})\right)$, $Z_1(s) = R_{C1}$, and $Z_2(s) = 1/(sC_{C1})$, a pole-zero pair is added to the previous two-pole one-zero compensation, thus yielding the three-pole two-zero compensation. This transfer function is described as $F_v'(s)$ in Table 11.5.

Control Design Procedures

The control design procedures established in the previous section are now applied to the small-signal model of Fig. 11.39. Detailed design steps are illustrated in the following example.

■ EXAMPLE 11.15 Current Mode Control for Off-Line Flyback Converter

Figure 11.41 shows the circuit diagram of a flyback converter which employs the peak current mode control using the optocoupler-isolated feedback. The feedback controller is implemented using a PWM chip, optocoupler, and op amp, along with other passive components. A simple resistive sensing is used for a low-cost CSN implementation. The switching frequency of the flyback converter is $\omega_s = 2\pi \cdot 65 \times 10^3$ rad/s and the turns ratio of the transformer is $n = 6/62 = 0.097$. From the information given in Fig. 11.41, the small-signal

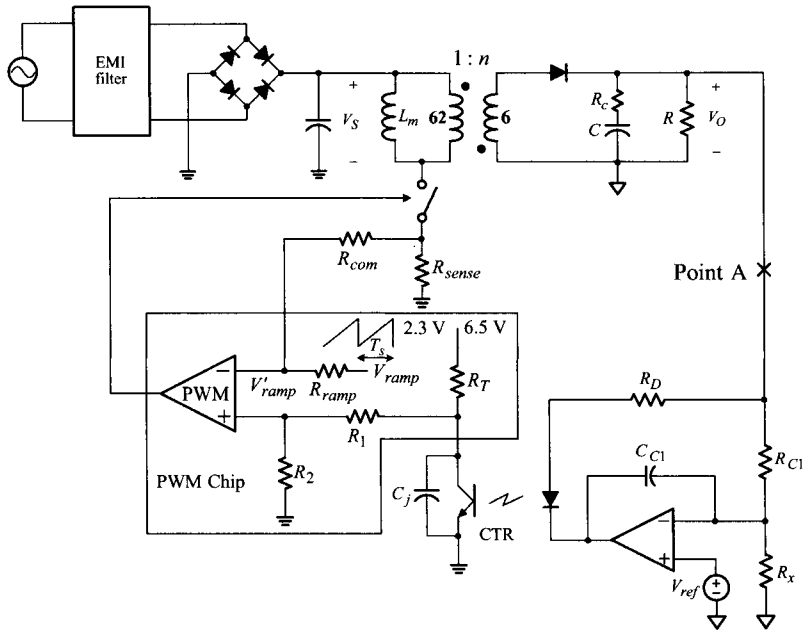


Figure 11.41 Off-line flyback converter with optocoupler-isolated peak current mode control: $V_S = 220\sqrt{2}$ V, $V_O = 10$ V, $L_m = 1.5$ mH, $n = 6/62 = 0.097$, $C = 910$ μF, $R_c = 0.04$ Ω, $R = 2$ Ω, $R_D = 393$ Ω, $R_{C1} = 2$ kΩ, $C_{C1} = 0.1$ μF, $V_{ref} = 2.5$ V, $R_x = 667$ Ω, CTR = 0.236, $C_j = 2.3$ nF, $R_T = 20$ kΩ, $R_1 = 55$ kΩ, $R_2 = 25$ kΩ, $R_{com} = 6.4$ kΩ, $R_{sense} = 0.67$ Ω, $R_{ramp} = 18$ kΩ, $V_{ramp} = 2.3$ V, $T_s = (65 \times 10^3)^{-1}$ s, and PWM chip: NCP1230 from On Semiconductor®.

parameters and operational conditions are determined as follows

$$\frac{V_O}{V_S} = \frac{D}{1-D}n$$

$$\Rightarrow \quad \frac{10}{220\sqrt{2}} = \frac{D}{1-D}0.097 \quad \Rightarrow \quad D = 0.25$$

$$\omega_o = \frac{1-D}{\sqrt{n^2 L_m C}}$$

$$= \frac{1-0.25}{\sqrt{0.097^2\, 1.5 \times 10^{-3}\, 910 \times 10^{-6}}} = 2\pi \cdot 1.05 \times 10^3 \text{ rad/s}$$

$$\omega_{rhp} = \frac{(1-D)^2}{D}\frac{R}{n^2 L_m}$$

$$= \frac{(1-0.25)^2}{0.25}\frac{2}{0.097^2\, 1.5 \times 10^{-3}} = 2\pi \cdot 5.07 \times 10^4 \text{ rad/s}$$

$$\omega_{esr} = \frac{1}{CR_c} = \frac{1}{910 \times 10^{-6}\, 0.04} = 2\pi \cdot 4.37 \times 10^3 \text{ rad/s}$$

The maximum value of the switch current is evaluated as

$$\begin{aligned} i_{Q\,max} &= n\frac{V_O}{R}\frac{1}{1-D} + \frac{1}{2}\frac{V_S}{L_m}DT_s \\ &= 0.097\frac{10}{2}\frac{1}{1-0.25} + \frac{1}{2}\frac{220\sqrt{2}}{1.5\times10^{-3}}0.25\frac{1}{65\times10^3} \\ &= 1.05\text{ A} \end{aligned}$$

The maximum input voltage for the PWM block is given as $V_{max} = 1.0$ V. The four resistances inside the PWM chip are prefixed: $R_{ramp} = 18$ kΩ, $R_T = 20$ kΩ, $R_1 = 55$ kΩ, and $R_2 = 25$ kΩ. In addition, the PWM chip provides a ramp signal whose magnitude is fixed at $V_{ramp} = 2.3$ V. The ramp signal is divided by the three resistors, R_{ramp}, R_{com}, and R_{sense}, and the resulting signal is applied to the PWM block as the compensation ramp V'_{ramp}.

Current Loop Design

The current loop design involves the selection of resistances for R_{com} and R_{sense} in compliance with the design specification, while using the predetermined resistances $R_{ramp} = 18$ kΩ and $V_{ramp} = 2.3$ V.

1) CSN gain:

$$R_i < \frac{V_{max}}{i_{Q\,max}} = \frac{1.0}{1.05} = 0.95 \quad \Rightarrow R_i = 0.50$$

2) Damping ratio of double pole:

$$Q_p = \frac{1}{\pi\left(\left(1+\dfrac{S_e}{S_n}\right)D' - 0.5\right)} = 0.6$$

$$S_n = \frac{nV_S}{n^2L_m}nR_i = \frac{0.097\cdot220\sqrt{2}}{0.097^2\,1.5\times10^{-3}}0.097\cdot0.5 = 1.04\times10^5\text{ V/s}$$

$$\Rightarrow\quad S_e = S_n\left(\frac{\dfrac{1}{\pi\,Q_p}+0.5}{D'} - 1\right)$$

$$= 1.04\times10^5\left(\frac{\dfrac{1}{\pi\,0.6}+0.5}{0.75} - 1\right) = 3.89\times10^4\text{ V/s}$$

$$\Rightarrow\quad V'_{ramp} = S_eT_s = 3.89\times10^4\frac{1}{65\times10^3} = 0.60\text{ V}$$

$$m_c = 1 + \frac{S_e}{S_n} = 1 + \frac{3.89\times10^4}{1.04\times10^5} = 1.37$$

where V'_{ramp} denotes the magnitude of the actual compensation ramp applied to the input of the PWM block.

3) Selection of R_{com} and R_{sense} with the assumptions of $R_{sense} \ll R_{ramp}$ and $R_{sense} \ll R_{com}$:

$$\begin{aligned} V'_{ramp} &= V_{ramp}\frac{R_{com}+R_{sense}}{R_{ramp}+R_{com}+R_{sense}} \approx V_{ramp}\frac{R_{com}}{R_{ramp}+R_{com}} \\ &\Rightarrow 0.6 = 2.3\frac{R_{com}}{18\times 10^3 + R_{com}} \\ &\Rightarrow R_{com} = 6.4\ \text{k}\Omega \\ R_i &= \frac{R_{sense}}{R_{ramp}+R_{com}+R_{sense}}R_{ramp} \\ &\approx \frac{R_{sense}}{R_{ramp}+R_{com}}R_{ramp} \\ &\Rightarrow 0.5 = \frac{R_{sense}}{18\times 10^3 + 6.4\times 10^3}18\times 10^3 \\ &\Rightarrow R_{sense} = 0.68\ \Omega \end{aligned}$$

Control-to-Output Transfer Function with Current Loop Closed

Referring to Table 11.3, the control-to-output transfer function of the flyback converter with the current loop closed is given by

$$G_{vci}(s) = K_{vc}\frac{\left(1-\frac{s}{\omega_{rhp}}\right)\left(1+\frac{s}{\omega_{esr}}\right)}{\left(1+\frac{s}{\omega_{pl}}\right)\left(1+\frac{s}{Q_p\omega_n}+\frac{s^2}{\omega_n^2}\right)} \tag{11.110}$$

where

$$\begin{aligned} \omega_n &= \frac{\omega_s}{2} = 2\pi\cdot 32.5\times 10^3\ \text{rad/s} \\ K_{vc} &= \frac{D'R}{(1+D)nR_i}\frac{1}{1+\frac{D'^3RT_s}{(1+D)n^2L_m}(m_c-0.5)} \\ &= \frac{0.75\cdot 2}{(1+0.25)0.097\cdot 0.5} \\ &\quad\cdot\frac{1}{1+\frac{0.75^3\,2\,(65\times 10^3)^{-1}}{(1+0.25)0.097^2\,1.5\times 10^{-3}}(1.37-0.5)} \end{aligned}$$

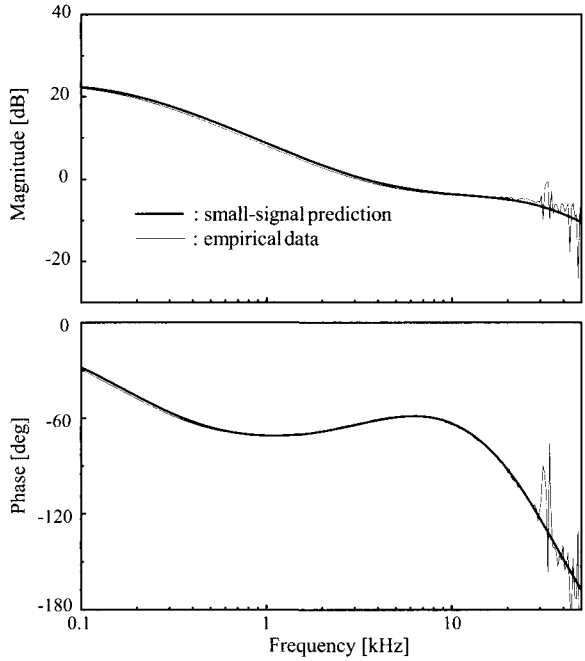


Figure 11.42 Control-to-output transfer function with current loop closed.

$$= 15.1$$

$$\omega_{pl} = \frac{1+D}{CR} + \frac{T_s D'^3}{n^2 L_m C}(m_c - 0.5)$$

$$= \frac{1+0.25}{910 \times 10^{-6}\, 2} + \frac{(65 \times 10^3)^{-1}\, 0.75^3}{0.097^2\, 1.5 \times 10^{-3}\, 910 \times 10^{-6}}(1.37 - 0.5)$$

$$= 2\pi \cdot 179 \text{ rad/s}$$

Figure 11.42 shows the control-to-output transfer function evaluated with only the current loop closed. The theoretical prediction is shown in parallel with empirical data obtained using the computational method.

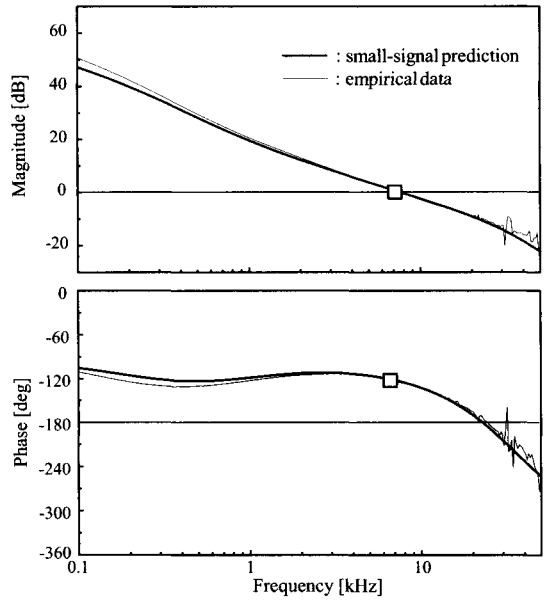


Figure 11.43 Loop gain characteristics of flyback converter.

Voltage Loop Design

The voltage feedback circuit constitutes the two-pole one-zero compensation shown in Fig. 11.40(a)

$$F_v(s) = \frac{K_v\left(1 + \dfrac{s}{\omega_{zc}}\right)}{s\left(1 + \dfrac{s}{\omega_{pc}}\right)} \tag{11.111}$$

where

$$\omega_{pc} = \frac{1}{C_j\,(R_T \parallel (R_1 + R_2))} \tag{11.112}$$

$$\omega_{zc} = \frac{1}{C_{C1}R_{C1}} \tag{11.113}$$

$$K_v = \frac{R_2}{R_1 + R_2}\,\frac{R_T \parallel (R_1 + R_2)}{R_D}\,\mathrm{CTR}\,\frac{1}{C_{C1}R_{C1}} \tag{11.114}$$

1) Compensation pole: $\omega_{pc} = \min\{\omega_{rhp}\ \omega_{esr}\ 0.5\,\omega_s\} = \omega_{esr} = 2\pi \cdot 4.37 \times 10^3$ rad/s. By evaluating (11.112) with the given resistive parameters, the desired capacitance is determined as $C_j = 2.3$ nF. The collector-emitter parasitic capacitance of the optocoupler was measured as 1.2 nF. Thus, an

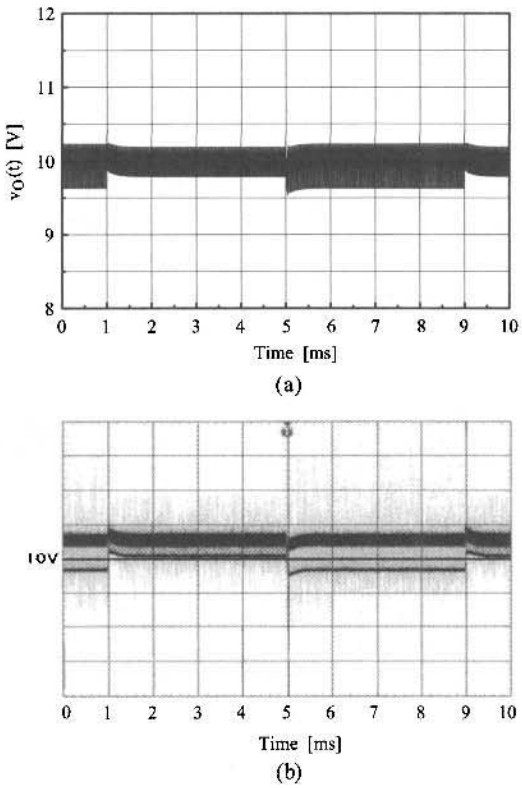


Figure 11.44 Step load response of flyback converter. (a) Simulated response. (b) Measured transient response.

external capacitance $C_{ext} = 1.1$ nF is added across the collector and emitter terminals in order to obtain the required capacitance 2.3 nF.

2) Compensation zero: $\omega_{zc} = 0.76\,\omega_o = 2\pi \cdot 800$ rad/s. One circuit parameter is initially selected as $R_{C1} = 2\,\text{k}\Omega$. Then, $C_{C1} = 0.1\,\mu$F is determined from (11.113). Finally, $R_x = 667\ \Omega$ is selected to produce the desired output voltage $V_O = 10$ V with $V_{ref} = 2.5$ V: $V_O = V_{ref}(1 + R_{c1}/R_x) \Rightarrow 10 = 2.5\,(1 + 2 \times 10^3/667)$.

3) T_2 crossover frequency: $\omega_{cr} = 0.16\,\omega_{rhp} = 2\pi \cdot 8.12 \times 10^3$ rad/s

4) Integrator gain: $K_v = \dfrac{\omega_{zc}\,\omega_{cr}}{K_{vc}\,\omega_{pl}} = \dfrac{(2\pi \cdot 800)\,(2\pi \cdot 8.12 \times 10^3)}{15.1\,(2\pi \cdot 179)} = 1.51 \times 10^4$

The current transfer ratio of the optocoupler is measured as CTR = 0.236. Accordingly, the last compensation component is determined as $R_D = 393\,\Omega$ from (11.114).

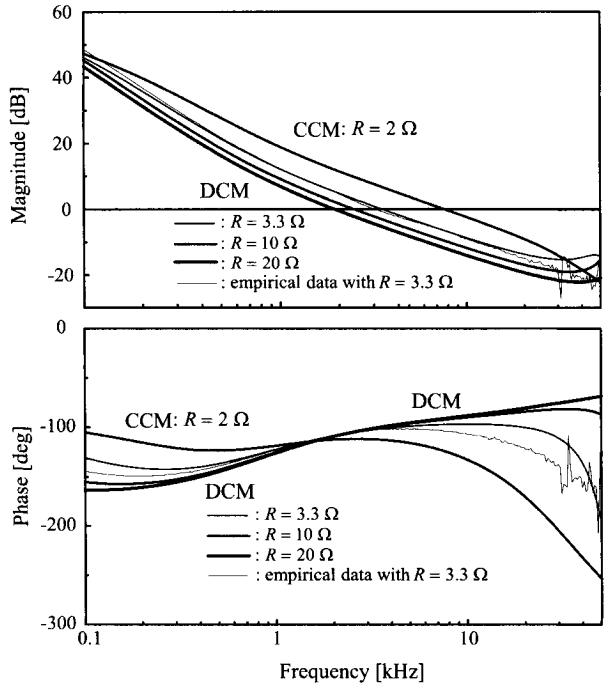


Figure 11.45 Loop gain characteristics of flyback converter in CCM and DCM operations.

Performance of Current Mode Control

Figure 11.43 compares the theoretical and empirical loop gains. The loop gain should be evaluated at Point A in Fig. 11.41. Point A is the only place that provides the correct loop gain information. The loop gain closely meets the design target of $\omega_{cr} = 2\pi \cdot 8.12 \times 10^3$ rad/s with sufficient phase margin.

Although the loop gain magnitude does not show any sign of the peaking at the Nyquist frequency due to the design goal of $Q_p = 0.6$, the phase characteristics advocate the existence of the double pole. Figure 11.44 compares the simulated and measured step load responses due to the step changes between $R = 1\ \Omega$ and $R = 2\ \Omega$.

Performance in DCM Operation

When the load resistance is increased beyond the critical value

$$R_{crit} = \frac{2n^2 L_M}{(1-D)^2 T_s} = \frac{2 \cdot 0.097^2\ 1.5 \times 10^{-3}}{(1-0.25)^2\ (65 \times 10^3)^{-1}} = 3.3\ \Omega$$

the flyback converter enters DCM operation. Figure 11.45 shows the loop gain characteristics of the converter in DCM operations, in comparison with those

of the CCM operation. The DCM loop gains with $R = 3.3\ \Omega$, $10\ \Omega$, and $20\ \Omega$ are compared with the CCM loop gain with $R = 2\ \Omega$. Although the mid-band gain and 0 dB crossover frequency are reduced, the loop gain curves confirm that the converter maintains stability in DCM operations with sufficient phase margin.

11.5 SUMMARY

The sampling effects of current mode control originate from the fact that the control action is periodically executed by sampling and holding the error signal produced by the fast-varying inductor current. In other words, the PWM modulator samples and holds the error signal at the rate of the switching frequency. The sampling effects, ignored in the preceding classical analysis, need to be duly addressed to accurately describe the high-frequency dynamics of current mode control. This chapter presented comprehensive analyses of the sampling effects using Ridley's s-domain model for current mode control.

The analysis of the sampling effects culminates with the derivation of the control-to-output transfer function evaluated with the current loop closed

$$G_{vci}(s) = K_{vc} \frac{\left(1 - \frac{s}{\omega_{rhp}}\right)\left(1 + \frac{s}{\omega_{esr}}\right)}{\left(1 + \frac{s}{\omega_{pl}}\right)\left(1 + \frac{s}{Q_p\omega_n} + \frac{s^2}{\omega_n^2}\right)}$$

The most distinctive feature of the transfer function is the presence of the quadratic term in the denominator. As an ultimate upshot of the sampling effects, the quadratic term introduces a double pole at half the switching frequency. This term is common to all the three basic PWM converters and constitutes the foundation for the control design for all the PWM converters.

The transfer function produces the peaking of $20 \log Q_p$ at half the switching frequency $\omega_n = \pi/T_s$. This peaking could cause the loop gain to violate the Nyquist stability criterion, thereby destabilizing the converter. To prevent such a consequence, the damping factor of the quadratic term needs to be controlled between $0.3 < Q_p < 1.3$. The idea of *adequately damping the double pole at half the switching frequency* leads to a simple and practical design methodology for current mode control. These new design procedures are illustrated in Section 11.3.3.

The goal of the new design procedures is to provide a predetermined value for Q_p. On the other hand, the classical design in Chapter 10 targets to place the crossover frequency of the current loop ω_{ci} at the desired frequency, thereby achieving a prefixed value for the ratio of the current loop crossover frequency to the switching frequency, ω_{ci}/ω_s. These two apparently different design goals are intimately linked by the equation

$$\frac{\omega_{ci}}{\omega_s} = \frac{Q_p}{2}$$

Therefore, there exists an exact one-to-one match between the new design and classical design. For example, selecting $Q_p = 1$ in the new design is identical to placing the current loop crossover frequency at half the switching frequency in the classical design. This rather surprising fact was also verified in [2] using an entirely different approach.

The quadratic term in the control-to-output transfer function – emerging as the ultimate outcome of the sampling effects – can also be exploited to investigate high-frequency converter dynamics. For example, the 20 log Q_p peaking at half the switching frequency can be used to account for sub-harmonic oscillations which could occur even with a duty ratio less than 0.5. Furthermore, the control-to-output transfer function can be used to investigate the converter dynamics when the converter is connected to general load systems other than a pure resistor [5].

This chapter presented several analysis and design examples of the peak current mode control adapted various of PWM converters, including the off-line flyback converter with an optocoupler-isolated feedback control. The outcomes of these examples can be readily adapted to all types of isolated or non-isolated PWM dc-to-dc converters for real applications.

REFERENCES

1. R. B. Ridley, "A new, continuous-time model for current-mode control," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp.271- 280, Apr. 1991.
2. F. D. Tan and R. D. Middlebrook, "A unified model for current-programmed converters," *IEEE Trans. Power Electron.*, vol. 10, no. 4, pp. 397-408, Jul. 1995.
3. G. F. Franklin, J. D. Power, and M. Workman, *Digital Control of Dynamic Systems*, 3rd Ed., Addison-Wesley Longman, Inc., 1998, Chapter 6.
4. R. B. Ridley, *A new small-signal model for current mode control*, Ph. D. Dissertation, Virginia Polytechnic Institute and State University, Blacksburg, VA, Nov. 1990.
5. B. Choi, B. H. Cho, and S. Hong, "Dynamics and control of dc-to-dc converters driving other converters downstream," *IEEE Trans. Circuits Syst. I*, vol. 46, pp. 1240-1248, Oct. 1999.

PROBLEMS

11.1** In Example 10.3 in Chapter 10, the modulator gain of the peak current mode control was derived from the expression

$$\bar{i}_L(t) = v_{con} - S_e dT_s - \frac{1}{2}(S_n + S_f)d(1-d)T_s$$

with the assumption that the slopes of the inductor current remain unchanged. Now, discard this assumption and introduce the perturbation to both S_n and S_f, in order to derive the feedforward gains from the input voltage/output voltage

to duty ratio. Show that the feedforword gains are given by

$$\text{Buck converter:} \quad k_f = -\frac{D(1-D)T_s R_i}{2L} \qquad k_r = 0$$

$$\text{Boost converter:} \quad k_f = 0 \qquad k_r = -\frac{D(1-D)T_s R_i}{2L}$$

$$\text{Buck/boost converter:} \quad k_f = -\frac{D(1-D)T_s R_i}{2L}$$

$$k_r = -\frac{D(1-D)T_s R_i}{2L}$$

The above expressions differ from those of Ridley's model, but they coincide with the feedforward gains of Tan's model, as can be confirmed in Table 11.1.

11.2 Solve the expression (11.28)

$$\frac{\dfrac{1}{R_i}\dfrac{1+\alpha}{sT_s}}{1+\dfrac{1}{R_i}\dfrac{1+\alpha}{sT_s}R_i H_e(s)} = \frac{1}{R_i}\frac{1+\alpha}{sT_s}\frac{e^{sT_s}-1}{e^{sT_s}+\alpha} \quad \text{with} \quad \alpha = \frac{S_f - S_e}{S_n + S_e}$$

in order to derive the expression for $H_e(s)$ given in (11.19)

$$H_e(s) = \frac{sT_s}{e^{sT_s}-1}$$

11.3* Modify the procedures given in Example 11.5 to derive the expression for the feedforward gain from the output voltage, given in (11.46)

$$k_r' = \frac{(1-D)^2 T_s R_i}{2L}$$

11.4* The procedures for casting the control-to-output transfer function into the third-order expression

$$G_{vci}(s) = K_{vc}\frac{\left(1-\dfrac{s}{\omega_{rhp}}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{\left(1+\dfrac{s}{\omega_{pl}}\right)\left(1+\dfrac{s}{Q_p\omega_n}+\dfrac{s^2}{\omega_n^2}\right)}$$

are illustrated in Example 11.6.

a) Follow the procedures of Example 11.6 to derive the control-to-output transfer function of the boost converter given in Table 11.3

$$K_{vc} = \frac{D'R}{2R_i}\frac{1}{1+\dfrac{D'^3 RT_s}{2L}(m_c - 0.5)}$$

$$\omega_{pl} = \frac{2}{CR} + \frac{T_s D'^3}{LC}(m_c - 0.5)$$

$$\omega_{rhp} = D'^2 \frac{R}{L}$$

Specify the restrictions for the power stage parameters and operational conditions, which will improve the accuracy of the approximations.

b) Repeat **a)** for the buck/boost converter

$$K_{vc} = \frac{D'R}{(1+D)R_i} \frac{1}{1 + \frac{D'^3 R T_s}{(1+D)L}(m_c - 0.5)}$$

$$\omega_{pl} = \frac{1+D}{CR} + \frac{T_s D'^3}{LC}(m_c - 0.5)$$

$$\omega_{rhp} = \frac{D'^2}{D}\frac{R}{L}$$

11.5** Adaption of the new design procedures to a buck converter was illustrated in Example 11.8. Redesign the feedback controller for $Q_p = 0.4$, while keeping other design criteria unchanged. Compare the results of your design with those of Example 10.8.

11.6* Redesign the boost converter used in Example 11.9 with $Q_p = 0.32$, while keeping other design criteria the same. Compare the outcomes of your design with those of Example 10.16.

11.7* Example 11.11 proved the relationship

$$\frac{\omega_{ci}}{\omega_s} = \frac{Q_p}{2}$$

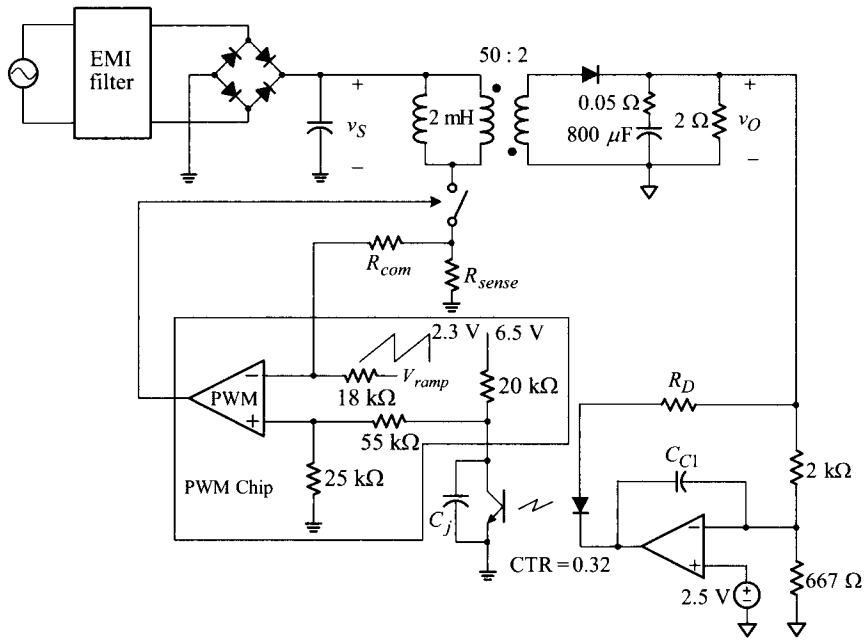
for the buck converter. Show that the above relationship also holds true for the boost and buck/boost converters.

11.8 Example 11.12 illustrated the relationship

$$K_{vc}\,\omega_{pl} \approx \frac{K_{vd}}{K_{id} R_i}\,\omega_{id}$$

for the buck converter. Verify that this relationship is also valid for the boost and buck/boost converters. Specify the conditions that enhance the accuracy of the approximation.

11.9* Figure P11.9 shows the off-line flyback converter with an optocoupler-isolated peak current mode control. The switching frequency of the converter is $\omega_s = 2\pi \cdot 65 \times 10^3$ rad/s. Perform the control design to meet the specifications of $Q_p = 0.8$ and $\omega_{cr} = 0.1\omega_{rhp}$, while adapting the other design guidelines practiced in Example 11.15. Specify values for $\{R_{sense}\ R_{com}\ C_{C1}\ R_D\ C_j\}$.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v_S
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2 mH
0.05 Ω
800 μF
2 Ω
+
v_O
–
R_{com}
R_{sense}
2.3 V
6.5 V
V_{ramp}
18 kΩ
20 kΩ
55 kΩ
25 kΩ
PWM
PWM Chip
R_D
C_{C1}
2 kΩ
C_j
CTR = 0.32
2.5 V
667 Ω

Fig. P11.9

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