Power Electronic Packaging

Yong Liu

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Design, Assembly Process, Reliability and Modeling

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Preface

Since Fairchild introduced the first commercially viable integrated circuit in Silicon Valley in 1957, the semiconductor industry has made impressive progress, particularly in communications, health, automotive, computing, consumer, security, and industrial electronics. This progress has followed Moore's Law, which predicts IC miniaturization down to nano dimensions and system-on-chip integration. At the same time, there are technologies based on or derived from silicon that do not scale according to Moore's Law such as RF, power electronics, sensors, MEMS, and lighting. These technologies are called "More than Moore."

Along with technology development trends characterized by Moore's Law and "More than Moore," business trends are characterized by cost reduction, shorter product life cycles, and outsourcing. The combination of these technology and business trends leads to increased design complexity, decreased design margins, increased probability of failures, decreased product development and qualification time, and challenges in assembly manufacturing. The quality and reliability of the assembly manufacturing process is critical in assuring a successful product. It is important to recognize that concurrent engineering of the semiconductor content and its high performance power package is becoming increasingly dependent on the rigorous use of proven multi-physics/FEA tools and techniques. The correct use of modeling tools can shorten power package design cycles but the challenge is insuring that the modeling tools and methodologies can support next generation products. Models for power packaging designs, materials, reliability and assembly manufacturing processes include electromigration simulation; diffusion along the interface of two metal materials; contamination at the interface between the lead frame, multiple chips, and epoxy mold compound (EMC); thermal resistance definition in multiple die power system in package (SiP) or the power module; 3D copper stud bumping and wire bonding simulation.

In the semiconductor industry, we all understand the importance of design, material selection, assembly manufacturing, reliability, and testing in minimizing power packaging failures. Wire bonding and stud bumping processes can induce silicon cratering, bond pad peel off, and cracking of the interlayer dielectric (ILD)

under the bond pad. Thin power die (below 50 μm) can crack when picked up from the tape. Molding can induce failures such as delamination due to voids in the interface between the lead frame and EMC. Lead frame forming, punch/singulation and trim may result in die and package cracking due to the impact. Tiny defects induced in an initial assembly process can impact quality in later assembly processes becoming a potential product quality and reliability concern. For example, during wafer sorting, cratering/marks can be induced on the bond pad. Later during wire bonding, when the wire is bonded to the cratered/marked bond pad, the adhesion strength at the interface between the wire bond and the bond pad can be compromised.

Power electronics packaging is rapidly advancing due to the increased market demand in almost all areas of power applications such as portable, consumer, home, computing, and automotive electronics. Due to its intrinsic structural nature, the performance requirements for power products are extremely high, especially due to their thermal and electrical environments. The materials and structural layout of power electronics makes the design rules and development of power packaging quite different from the development of regular IC packaging. The development of power packages depends heavily on power device integration. Current power devices have two major integration modes: Monolithic integration and hybrid integration. Monolithic integration includes power integrated circuits, high voltage integrated circuits (HVIC), and intelligent discrete power devices, combined with functional integration and the integration of passive elements. Hybrid integration includes the standard power module and the intelligent power module (IPM). This book presents a state-of-the-art and in-depth overview of power electronic packaging design, assembly processes, material characterization, reliability, and modeling. Recent advances in power electronic packaging are presented based on the development of power device integration. The book also covers how advances in both semiconductor content and advanced power package design and materials have co-enabled significant advances in power device capability during recent years. Extrapolating the same trends in representative areas for the remainder of the decade serves to highlight where further improvement in materials and techniques can drive continued enhancements in thermal management, usability, efficiency, reliability, and overall cost of power semiconductor solutions.

This book is arranged into 12 chapters. The first chapter introduces the challenges of power electronics packaging development, which include the impact of die shrinkage; power system on chip (SoC) vs. system in packaging (SiP); power package foot print pitch; and new power packaging materials. Chapter 2 describes electrical isolation design for power packaging, including design rules for isolation, estimation of clearance and creepage distances, power package design layout considerations, and application categories and standards. Chapter 3 discusses discrete power MOSFET package design and analysis. This chapter covers the trends for epoxy molding compound use; trends for current carrying capability; low Rds(on) and multiple direction heat transfer; typical discrete power package design and constructions; power VDMOSFET wafer level chip scale package (WLCSP) with Cu stud bumping; and trends of discrete power WLCSP. Chapter 4 regards

power IC packaging design, which includes power IC technology evolution; trends of high power density at the die level; smaller package foot prints and typical package design and analysis. Chapter 5 addresses the development of power module/SiP/Stack/3D/Embedded die package design and considerations, including the side by side die placement power system in packaging and module for low and high power applications; power stack die SiP; wafer level power stack die packaging with through silicon via (TSV); stack/embedded power module and integrating the power package with active and passive chips. Chapter 6 reviews thermal management, design, analysis and cooling for power packaging, including thermal resistance and measurement methods; selection of thermal test boards; thermal prediction, management and design including from device to board and multiple die thermal analysis; cooling design for power packaging. Chapter 7 discusses the material characterization for power packaging including the polyimide coating behavior on MOSFET die; die attach delamination characterization; EMC characterization; the mechanical and thermal behavior of ceramic and direct bond copper (DBC) substrates; solder material characterization; lead frame material testing and MOSFET material behavior in copper wire bonding. Chapter 8 presents typical assembly processes for power packaging, which include wafer handling; die pick up; die attach; wire bonding; molding; and trim/singulation. Chapter 9 introduces typical power packaging reliability testing which includes thermal and power cycling; passivation crack analysis; wafer probing; drop test and moisture related reliability analysis. Chapter 10 discusses power packaging modeling including the role of modeling; challenges of modeling tools; modeling requirements; modeling methodologies and modeling trends. Chapter 11 introduces codesign automation simulation for power packaging that includes thermal modeling and test correlation; wafer level power package parameter thermal simulation and thermal–mechanical, hygroscopic and vapor pressure codesign automation. Lastly, Chapter 12 presents power package electrical and multiple physics simulation. It consists of four sections: electrical simulation for resistance, inductance and capacitance (RLC); current capability; power unclamped inductive load (UIL) test or unclamped inductive switching (UIS) test and simulation, and electromigration simulation. Each chapter has a summary for the related design and methodology. The author hopes this book provides good reference material for researchers, design engineers, managers, university professors, and students who work on power electronics.

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Chapter 1
Challenges of Power Electronic Packaging

Over the last 2 decades, power semiconductor technology has made impressive progress, particularly in increasing the high power density of monolithic, system module, and hybrid designs [1, 2], which are the driving forces toward a power system module, power system in package (SiP), and 3D power package with heterogeneous functional integration.

The development of power packages depends on the development of power device integration. Current power devices have two major integration modes: Monolithic integration and hybrid integration—Monolithic integration includes power integrated circuits, high voltage integrated circuits (HVIC), and intelligent discrete power devices, combined with functional integration and the integration of passive elements. Hybrid integration includes the standard power module and the intelligent power module (IPM).

Figure 1.1 shows the various power applications in different integration modes with different operation frequencies [1]. The complete power system integration may be monolithic or hybrid according to the power range desired. Today the trend of monolithic integration is moving toward 3D heterogeneous integration and hybrid integration is moving toward high switching frequency with reduced or eliminated bulky magnetics and capacitances as well as soft switching technologies for high efficiency and low harmonics [3]. Silicon carbide (SiC) and other wide bandgap (WBG) semiconductor devices will ultimately be important elements for hybrid integration due to advance system dynamic characteristics, overload capability, device ruggedness, and thermal and electrical performance [4–8].

This chapter introduces power package trends based on power device developments. A review of recent advances in power electronic packaging with both monolithic and hybrid power integrations is presented. This chapter will cover in more detail how advances in both semiconductor content and advanced package design and the materials have coenabled the significant advances in power device capability during recent years. Extrapolating the same trends in representative areas to the remainder of the decade serves to highlight where further improvement in

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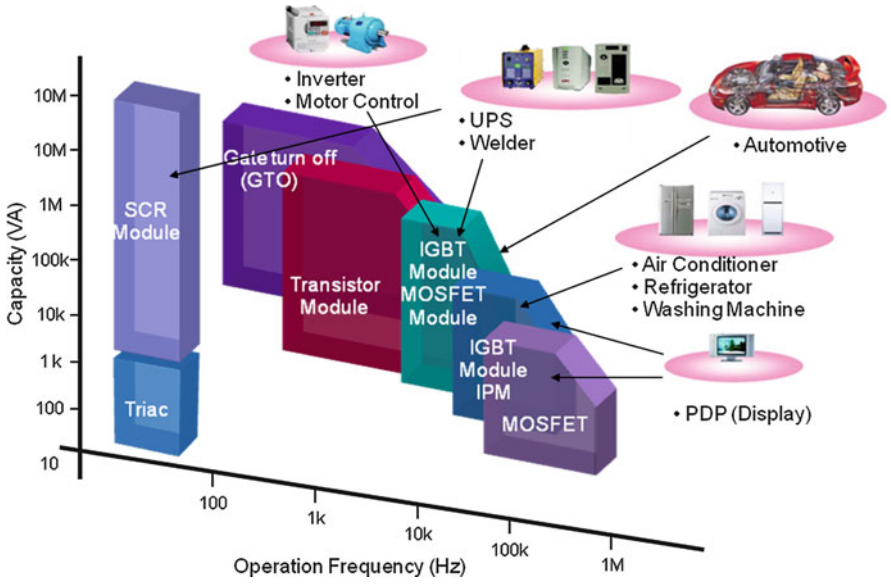


Fig. 1.1 Various power applications

materials and techniques can drive continued enhancements in usability, efficiency, reliability, and overall cost of power semiconductor solutions. Challenges of power semiconductor packaging in both next-generation design and assembly process are presented and discussed.

In addition to the forward looking trends it is important to recognize that the methods for concurrent engineering of these solutions (both the semiconductor content and high performance package capability) are becoming increasingly dependent on rigorous use of proven multi-physics/FEA tools and techniques for both new power package development and its assembly process. The challenges for modeling of power semiconductor package in new package and assembly process are investigated and discussed. Examples of new power semiconductor packaging in thermal management and assembly process are presented.

1.1 Challenges of Power Semiconductor Packaging

Today, providing energy-efficient solutions for various products is becoming increasingly important in our world due to limited energy resources and climate change. Especially significant is the fast growth of consumer electronics in both communications and entertainment, industrial power conversion, automotive, and standard power electronics products. Consumer demand for increased mobility with

advanced features and for high efficiency energy solutions has paved the way for a variety of new products [9] and has driven advances in power electronics technology toward the high power density design of monolithic devices, discrete components, 3D heterogeneous and multiple-chip module, or power SiP [10]. As compared to the development in general IC package [11–19], the power package is far behind due to the extremely harsh operating environment. New modeling methodologies and tools are becoming necessary to support new power package development. This chapter describes the challenges for today and the next few years in power package development that should be addressed by our industry.

1.1.1 Impact of Power Die Shrinkage

The development of power semiconductor device has begun to aim at 130 nm technology, while today 180 and 250 nm technologies are beginning to drive significant die size shrinkage as compared to regular 350 or 500 nm power technology. As the metal interconnect system inside the die continues to become thinner, current density has significantly increased. The electromigration (EM) issues will grow and new interconnect alternatives will be considered. Current techniques such as the cu-stud (should this be Cu pillar or Au stud) bumping, copper wire bonding, and aluminum wedge bonding will meet the challenges of cratering and related wire bonding reliability. Development of fine copper wire (less than 1 mil) bonding technology becomes necessary due to smaller wire bond pitch. As the die shrinks, the pitch of power wafer level chip scale packages (CSP) will move from current 0.5 toward 0.4 mm. The heat dissipation will become a very critical and significant challenge. Finding a high efficiency heat dissipation solution is necessary.

1.1.2 Power System on Chip vs. System in Package

The monolithic integration of power devices allows state of art smart power ICs with technologies such as integration of bipolar, complementary metal oxide semiconductor (CMOS) and double diffused metal oxide semiconductor (DMOS)-BCDMOS, intelligent discrete power device, and the function integration in both lateral DMOS (LDMOS) and vertical DMOS (VDMOS) for power control and protection as well as other functions. This is called power semiconductor system on chip (SOC), which is the integration of several heterogeneous technologies—analog, digital, MOSFETs, etc. into a single silicon chip. However, such power SOC technology often is too expensive and complex. This leads to a wealth of opportunities for SiP, in which multiple chips with different functions are placed in one package or module [20] which has similar function of SOC but with a lower cost.

SiP has evolved as an alternative approach to SOC for electronics integration because this technology provides advantages over SOC in many market segments. In particular, SiP provides more integration flexibility, faster time-to-market, lower research and development (R&D) or nonrecurring engineering (NRE) cost, and lower product cost than SOC for many applications. This is particularly a great advantage for SiP or the power module for high power applications such as automotive, solar energy, wind energy, railway and other industrial applications, in which the SOC seems only not possible. SiP is not a replacement for high level, single chip, silicon integration but should be viewed as complementary to SOC in the applications that SOC can contribute. For some very high volume applications SOC will be the preferred approach. Some complex SiP products will contain SOC components.

As the die shrinks, SOC can add more functions, and SiP can include more chips. In SOC, the thermal density will become very high. Determining how to insulate different functions in one chip and how to effectively dissipate the heat through the package will be a challenge [21]. Although the cost of SiP is low, there are challenges due to the assembly of multiple chips. The internal parasitic effects of SiP, such as parasitic inductance [22], are higher than that of SOC. The impact of heat from the power components on the electrical performance of IC drivers will be a concern. To build an advanced SiP which has good thermal and electrical performance with low cost is the greatest challenge of power SiP, especially for high power hybrid application power module, the excellent efficiency, good thermal and electrical performances are critical for the product design and reliability.

1.1.3 Power Package Foot Print Pitch vs. PCB Pad Pitch

As power die size shrinks, the package footprints shrink as well, and maintaining the thermal transfer capacity at the package level is difficult since the function/unit area of die is increasing with advanced BCDMOS processes. While the overall package footprint pad pitch is decreasing area, the customer's printed circuit board (PCB) pitch will remain relatively larger. For example, the trend of peripheral pad pitch for a power IC chip will be reduced from about 400–500 to 200–300 μm, while the pitch from customer board will be from 800 to 500 μm. Bridging the power IC pitch to board pitch without impacting thermal performance is the challenge for the power package engineers. We need to build the interposer to reroute the WLCSP that can fill the interconnect gap between the fine print pitch and the larger PCB pitch. This interposer must have excellent electrical performance with lower $R_{ds(on)}$, smaller parasitic inductance and good heat transfer capabilities. More importantly, the product should have robust reliability with lower cost. WLCSP directly attached to the leadframe or direct bond copper on ceramic (DBC), with overmolding, is an effective packaging approach to connect the fine pitch on power chip to the larger pitch on PCB. This method is a trend that has very good thermal and electrical performances for fine pitch power device.

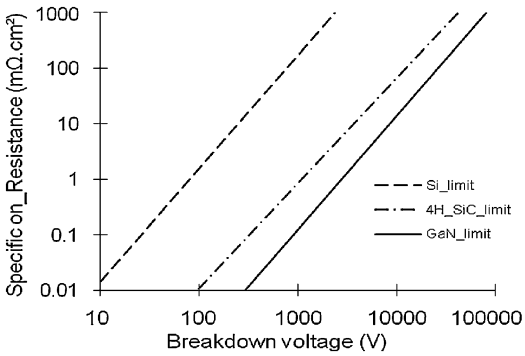


Fig. 1.2 The comparison of Si, SiC and GaN

1.1.4 New Materials for Power Device

Due to the limit of silicon power device at high voltage level (600–700 V), the technological advancement has pushed the development of new materials for power devices, such as SiC, gallium nitride (GaN), and other WBG semiconductor materials. SiC is one of the most promising semiconductor materials that will be used to replace silicon in future power electronics. There are three great advantages of SiC [4, 7] as shown in Fig. 1.2: (1) The higher breakdown electric field strength of SiC allows a much thinner drift region and thus a much smaller specific on-resistance of SiC devices than their silicon devices. (2) The low on-resistance of SiC devices allows the use of majority-carrier devices like MOSFET and Schottky diodes rather than minority-carrier devices such as insulated gate bipolar transistor (IGBT) and PiN diodes. This results in a much reduced switching loss due to the absence of the charge storage effect. Lower switching losses will further allow higher switching frequency and subsequently smaller and less expensive passive components such as filter inductors and capacitors. (3) The larger bandgap results in a lower intrinsic carrier concentration and higher operating junction temperature.

In general, SiC devices could operate at a junction temperature as high as 500–550°C, as compared to a typical 150–200°C maximum junction temperature of silicon devices. The increased operating temperature can reduce the weight, volume, cost, and complexity of thermal management. Furthermore, the very high thermal conductivity of SiC reduces the thermal resistance of the device die. Significant progress has been made in research and development of SiC and other WBG device technologies in the past decade [4]. Various types of SiC switching devices and diodes have been developed and reported. The 600–1,700-V SiC Schottky diodes are commercially available, which can replace Si freewheeling diodes in renewable energy (solar and wind), industrial motor drives, and hybrid/full electric vehicle (HEV/EV) inverters. SiC Schottky diodes have demonstrated superior performance to that of similar silicon PN diodes, especially with respect to their switching characteristics because they have negligible reverse recovery losses.

SiC JFETs, MOSFETs, and bipolar transistors with exceptionally resistance were reported, which can potentially be used as the active power switches replacing Si-IGBTs. It is a great challenge to produce a high-quality interface between SiC and a suitable gate dielectric material for SiC MOSFET structures. JFETs and bipolars avoid the gate reliability and poor channel mobility issues of MOSFETs, while bipolars offer normally-off operation with high noise margin for single supply input drives. The high defect density and cost of SiC has delayed widespread commercialization. The cost of SiC diodes historically ranged from 5 to 10 times that of silicon devices with the same voltage and current ratings, but is declining as materials improve and volume increases.

Gallium Nitride devices have a theoretical limit for a vertical device even lower than SiC. Realizing that performance is not yet possible due to the lack of a reasonable cost single crystal GaN substrate, GaN devices today are lateral, and so have limitations of high surface electric fields, susceptibility to voltage transients, on-state instability due to charge accumulation in the off-state, and usually normally-on operation. Normally-off devices are emerging, using hybrid GaN/silicon cascode arrangements or special gate structures that add to the device on-state resistance. Power terminals must be interdigitated and routed on the surface and space reserved for power wire bonds or other interconnects, which limits active area utilization. Nevertheless, GaN devices do show promise for future medium voltage and current applications.

Much progress is happening to fully exploit these benefits of new semiconductor materials to achieve system-level improvement in the weight, size, efficiency, performance, and even possibly the overall cost of the power electronic products.

1.1.5 New Materials for Power Package

Development of new package materials to support power package heat transfer and good electrical performance is critical and a challenge. An example is to develop new thermosetting molding compound material with reasonable content of nano-silica fillers to rapidly dissipate heat from the power die while keeping the adhesion strength high. At present, both Pb-free solder alloys and green epoxy mold compound material (EMC) are used and accepted by most companies. However, thermal stability is a key issue [9], especially in the automotive environment, where current epoxy mold compound materials have difficulties meeting the requirement of exceeding 180°C continuous operation. The new green EMC will have to withstand such temperature from the power chip. Pb-free solder alloy must have high melting temperatures for power package. Currently the solder material for power package is PbSnAg based alloy which normally has the melting temperature 300°C with low cost. The challenge today we have is can we develop an equivalent Pb-free solder alloy for power device that has the melting temperature about 300°C with similar low cost? Also, the Green EMC should not burn during high temperature operation in the power device.

As the chip shrinks, there are related trends in power packages. The first is for low power ICs, where the volume of EMC is decreasing with the introduction of package technologies such as WL-CSP, power BGA, and flip-chip BGA, which are gaining wider application. The second is in high power applications which currently use VDMOS devices and IGBTs. We see a trend for increasing usage of SiC, GaN, and other WBG semiconductor materials [3, 7] due to higher breakdown electric field strength, larger bandgap, low on-resistance, and very high thermal conductivity. For the latter trend, the EMC usage is not decreasing. Therefore, the challenge is to develop robust materials and methods that can easily transfer the heat from SiC to ambient. Two such technologies are DBC and insulated metal substrate with polymer insulation to dissipate the heat to heat sink [23–25]. The other is the built copper material based substrate at bottom and copper clips at package top for excellent heat transfer. For high power application, the built-in microchannel-based new SiC material die and substrate will be a promising trend in the future that can effectively help the heat dissipation in power packages [26].

1.2 Summary

The development of power packages is closely related to the development of power devices. For discrete power devices, the trends in power packaging are toward the EMC free and high current carrying capability for the low voltage application. However, the EMC today in discrete power package is still useful as a component "encapsulant" or as a premolded substrate component in a modified form. The trends of power IC are high power density at die level and small foot print. The major thermal transfer path is based on the board level. Therefore, how to design the power package so that its small footprint can match the PCB is a challenge for the power package designer. High power hybrid integration is mostly based on power SiP and module with multiple die. SiP has a lot of advantages and flexibilities for power device while power SOC with a single chip is still an excellent solution if the cost is acceptable by customers. SiC and other new WBG semiconductor devices will help the system with good thermal and electrical performance. The green thermal-setting EMC and Pb-free materials will be the challenges for high power devices; therefore, the built-in microchannel in SiC die and the DBC substrate will be a trend in the future for high power application.

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Chapter 2
Power Package Electrical Isolation Design

Power Electronics packaging consists of power semiconductor devices, power integrated circuits, sensors, and protection circuits for a wide range of power electronics applications [1–3], such as inverters for motor drives and converters for power processing equipment. Integration in power electronics is a rather complex process due to incompatibility of materials and processing methods used in fabrication, and due to the high electrical density levels and electrical isolation requirements these components must handle. Packaging involves the solution of electrical, mechanical, and thermal problems. Electrical isolation is one of the important factors to be considered in the power packaging design, as it relates directly to the product reliability and safety. Based on the standard of International Electrotechnical Commission (IEC) and the US Standard (UL), such as the standard IEC60950-1 [4] and UL60950-1[5], designers shall take into account not only the normal operating conditions of the equipment but also likely fault conditions, consequential faults, foreseeable misuse, and external influences such as temperature, altitude, pollution, moisture, overvoltages in a system that use the power packaging products. This chapter discusses the power package electrical isolation design considerations.

2.1 Background

Figure 2.1 is an example of a complex, high-power automotive-solenoid driver system showing the control block and power die [3]. One of the major issues that must be overcome, when combining power and control in a single package, is that the back side of the power device is normally the drain or collector of the power switch. As a result, the control die must be electrically isolated from the die-attach area on which the power die is mounted. Since the power die is typically a vertical-conducting device, a good low-resistance, high melting temperature-solder die

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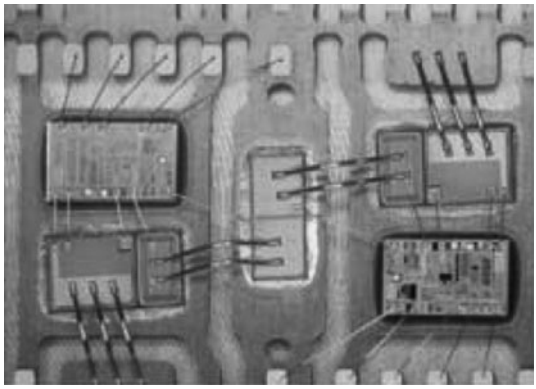


Fig. 2.1 An example of automotive power packaging

attach is normally used. There are several ways to approach the electrical isolation required between the power and control devices. One method for the electrical isolation is to separate the die-attach areas and the others are to use the nonconducting epoxy, polyimide, and the silicon back-side laminate on control die as the isolation.

Each isolation technique has its advantages and disadvantages regarding cost, reliability and manufacturability. Some packages, such as the molded leadless package (MLP) or quad flat no lead (QFN) devices (as shown in Fig. 2.1), can easily accommodate multiple die-attach areas. But traditional power packaging, such as the TO220 or TO252 (which have a thick header or tab), are not easily divided into two separated electrical areas. Use of a nonconducting epoxy die-attach is one of the easiest isolation solutions to implement, but this approach has been shown to be susceptible to reliability issues related to pin holes in the epoxy die attach. Polyimide tape is being used successfully, but the die-attach area must be larger than the attached-die area, to account for the alignment tolerance of the die to the polyimide tape. Thus, it takes up more area then the back-side laminate solution mentioned. For the back-side laminate solution, a film is attached to the entire back side of the control-die wafer, and then the die is sawn from the wafer. In this way, each die has the polyimide film attached to the back of the die, and the need for additional area to account for the alignment variability when attaching the die is eliminated. This can be particularly beneficial when the control die is being attached on top of the power die, allowing a smaller power die to still accommodate the die-on-die assembly requirements.

The electrical isolation requirement does not only apply to the power packaging for the multiple die layout, but also apply for the layout of interconnects and output pins of the packaging, especially for the median and high power application. For example, for a higher accuracy data acquisition system, it is a challenge for the designers to measure small signal variations when high common mode voltages (wanted or unwanted) are present. These high voltages exist due to the different

potential in the two grounds or any sudden transient over voltages due to lightning strikes or power surges from motors or switching devices. These voltages do not only impact on the accuracy of the measurement but also damage the test systems and cause hazards to people operating the tester. Isolations are needed to physically and electrically separate two systems to protect against sudden voltage surges between two circuits or systems. They are used to provide a higher common mode voltage range; common mode voltage is the voltage that appears simultaneously between both measurement signal leads and a common ground. For example, when measuring the voltage across a specific cell in a series connected string of battery cells a high common voltage range is important. Isolations are also needed to break up ground loops, which are the unwanted currents between two points that share a common path in an electrical system. This is widely used in instrumentation probing systems that measure differential voltages. In addition, isolations can serve as a level shifter to solve incompatibility of voltage levels between systems or circuits.

2.2 Design Rule for Isolation

2.2.1 Protection with Insulation

US National Standard UL60950-1 defines five types of insulation (1) *Functional insulation* is that which is only necessary for circuit operation. It is assumed to provide no safety protection. (2) *Basic insulation* provides basic protection against electric shock with a single level; however, this category does not have a minimum thickness specification for solid insulation and is assumed to be subject to pin holes. Safety is provided by a second level of protection such as supplementary insulation or protective earth. (3) *Supplementary insulation* is normally used in conjunction with Basic insulation to provide a second level of protection in the event that the Basic level fails. A single layer of insulating material must have a minimum thickness of 0.4 mm to be considered Supplementary insulation. (4) *Double insulation* is a two-level system, usually consisting of basic insulation plus supplementary insulation. (5) *Reinforced insulation* is a single-insulation system equivalent to Double insulation. It also requires a minimum thickness of 0.4 mm for use in a single layer.

Electric circuits rely upon insulation for operator protection, but designing for safety requires the premise that anything can fail. Therefore, safety standards demand a redundant system with at least two levels of protection under the assumption that any single level may experience a failure, but the chance of two simultaneous failures in the same spot is so improbable as to represent an acceptable risk. It should be noted that while two random failures need not be considered, the possibility of a second failure as a consequence of a first failure is something that the designer must evaluate if the two together would result in a total breakdown.

With the insulation levels defined, specific requirements for the insulating medium must be considered. This medium can be either a solid material (such as plastic molding compound) or air (as in the space between components), and the requirements for both are affected by the voltage stress across the medium. Typically, a power supply is evaluated to determine the highest voltage levels possible at all points in the circuitry and under all operating conditions. The highest measured voltage between any two points then defines the working voltage for those two points. The working voltage between a primary circuit and a secondary circuit, or between the primary and ground, is taken as the upper limit of the rated voltage range for the supply. The working voltage normally stands for the highest root mean square (rms) value of the ac or dc voltage that may occur locally across any insulation at rated supply voltage transients.

2.2.2 Solid and Air Insulation

The choice and application of solid insulating material must consider, in addition to working voltage, the needs for electrical, thermal, and mechanical strength, as well as the operating environment. Only nonhygroscopic and flame resistant materials may be used. With particular respect to wiring insulation, it should be noted that some material compounds may contain plasticizers, intended to make them more flexible but with a side effect of increased flammability. Semiconductor devices and other components that are molded in solid insulating material typically are independently qualified and inspected in the manufacturing process. Solid insulation material in sheet form must also conform to the following thickness requirements (1) If a single sheet of insulation is provided, the minimum thickness is 0.4 mm. (2) With two sheets together, there is no thickness requirement but each sheet must meet the required electric strength value. (3) With three or more sheets, there is also no minimum thickness but every combination of two sheets must have adequate electric strength. (4) There is no thickness requirement for Functional or Basic insulation. The use of air as an insulation medium introduces concerns both about the "quality" of the air and the spacing between electrically conducting components. The potential for conduction through air is affected by temperature, pressure, humidity, and pollution, with "pollution" being defined according to the operating environment by the following categories: Pollution Degree 1—Components and assemblies which are sealed to exclude dust and moisture, example is the dry and clean rooms. Pollution Degree 2—General office or home environment, which normally only allows the nonconductive pollution. Pollution Degree 3—Equipment where the internal environment is subject to conductive pollution or possible moisture condensation, products used in heavy industrial, farming areas, and mechanical workshop that are typically exposed to pollution such as dust. Pollution Degree 4—Pollution generates persistent conductivity caused, for instance, by conductive dust or by rain or snow.

Table 2.1 Partial clearance distance (mm) selected from [4] IEC 61950-1 ed.2.0. Copyright 2005 IEC Geneva, Switzerland, www.iec.ch

Working voltage		AC mains < 150 V (transient to 1,500 V), pollution levels 1 and 2			AC mains < 300 V (transient to 2,500 V), pollution levels 1 and 2		
Peak dc (V)	rms (V)	F (mm)	B/S (mm)	R (mm)	F (mm)	B/S (mm)	R (mm)
71	50	0.4	1.0	2.0	1.0	2.0	4.0
210	150	0.5	1.0	2.0	1.4	2.0	4.0
420	300	1.5	2.0	4.0	1.5	2.0	4.0
840	600	3.0	3.2	6.4	3.0	3.2	6.4

Table 2.2 Partial creepage distance (mm) selected from [4] IEC 61950-1 ed.2.0. Copyright 2005 IEC Geneva, Switzerland, www.iec.ch

Working voltage	Pollution level 1 material group III			Pollution level 2 material group III			Pollution level 3 material group III		
dc or rms (V)	F (mm)	B/S (mm)	R (mm)	F (mm)	B/S (mm)	R (mm)	F (mm)	B/S (mm)	R (mm)
<50	0.4	0.7	1.4	1.2	1.2	2.4	1.9	1.9	3.8
<150	0.6	0.9	1.8	1.6	1.6	3.2	2.5	2.5	5.0
<300	1.6	1.9	3.8	3.2	3.2	6.4	5.0	5.0	5.0
<600	3.2	3.2	5.0	6.3	6.3	12.6	10	10	10

2.2.3 Design Rule of Clearance and Creepage

In the discussion that follows, the Tables 2.1 and 2.2 presented show partial quantitative values for design rule of spacing requirements, in millimeters, which are listed as a function of the voltage, material, and environment. An additional distinction is the category of insulation system of which these spaces are a part, i.e., Functional, Basic/Supplementary, or Reinforced. In other words, if the spacing between components is not needed for safety, the "F" column may be used; if only one level of safety insulation is needed because a second level is provided elsewhere, the "B/S" column is applicable; and for the equivalent of a complete two level safety insulation, the "R" column should be used. The spacing distance between components that are required to withstand a given working voltage is specified in terms of Clearance and Creepage, as shown in Fig. 2.2.

2.2.3.1 Clearance Distance

Clearance is defined as the shortest distance through air between two conductive parts, as shown in Fig. 2.3. Breakdown along a Clearance path is a fast phenomenon where damage can be caused by a very short duration impulse. Therefore, it is the maximum peak voltage, including transients, that is used to determine the required Clearance spacing according to charts given in the standard. A sample of one of

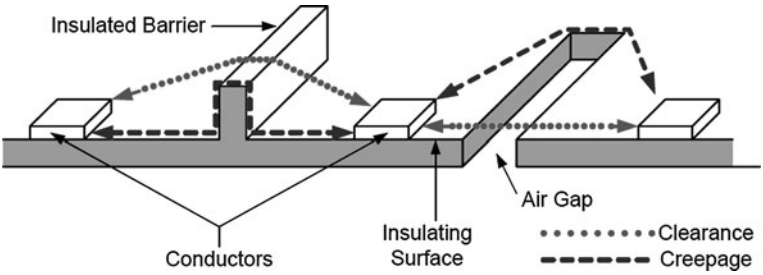


Fig. 2.2 The clearance and creepage in a system

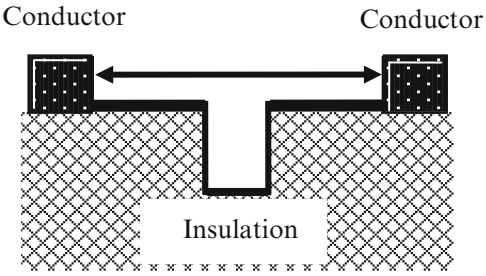


Fig. 2.3 The definition of clearance

these design rules is shown in Table 2.1 [4] where the spacing in millimeters required for different levels of insulation is given as a function of working voltage. Additional variables of ac mains voltage and the quality of the air within the space are indicated in this illustration but are applied more quantitatively in additional charts given in the complete standard.

2.2.3.2 Creepage Distance

Creepage is defined as the shortest distance between two conductive parts along the surface of any insulating material common to both parts as shown in Fig. 2.4. While the path is in the air, it is heavily influenced by the surface condition of the insulating material. Breakdown of the Creepage distance is a slow phenomenon, determined by dc or rms voltage levels rather than peak events. Inadequate Creepage spacing may last for days, weeks, or months before it fails. A sample of a table of Creepage requirements for design rule is given as Table 2.2 [4] with different pollution levels and material group III, where the spaces are given as a function of the steady-state working voltage with additional variables of insulation type, material composition, and content of the air.

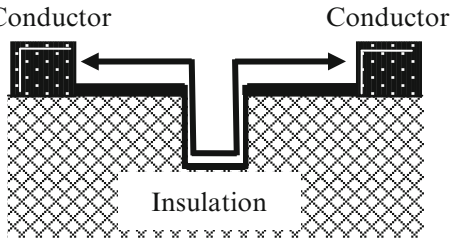


Fig. 2.4 The definition of creepage

Table 2.3 Design rule *X* [4] (IEC 61950-1 ed.2.0. Copyright 2005 IEC Geneva, Switzerland, www.iec.ch)

Pollution degree	Design rule *X* (mm)
1	0.25
2	1.0
3	1.5

2.2.3.3 The Measurement of Clearances and Creepage Distances

The methods of measuing clearance and creepage distances which are specified in IEC/UL60950-1 in the following figures are used in interpreting the design rule of the clearance and creepage for power package. In Table 2.3, *X* is the design rule. Where the distance in design is less than *X*, the depth of the gap or groove is disregarded when measuring a creepage distance.

Figure 2.5 shows six cases of the clearance/creepage distances with the design variable less or larger than the design rule *X* (mm) in Table 2.3. In Fig. 2.5, the solid line stands for clearance distance and the dot line stands for the creepage. Figure 2.5 (1) shows that the path under consideration includes a parallel or converging-sided groove of any depth with width less than *X* mm, the design rule is to measure the clearance and creepage distances across the groove. Figure 2.5(2) that the path under consideration includes a parallel or converging-sided groove of any depth with width equal or more than *X* mm, the design rule for clearance is the "line of sight" to measure the clearance distances across the groove, while the creepage distance path follows the contour of the groove. Figure 2.5(3) shows that the path under consideration includes a V-shaped groove with internal angle of less than 80° and a width greater than *X* mm. The clearance is the "line of sight" distance across the V-shaped groove. The creepage distance is the path follows the contour of the groove but "short circuits" the bottom of the groove by a link *X* mm long. Figure 2.5 (4) shows the path is a rib-like shape. The design rule requires that the clearance is the shortest direct air path over the top of the rib and the creepage distance path follows the contour of the rib. Figure 2.5(5) shows the creepage path as the gap between the head of screw and wall of recess is too narrow to be taken into account. This induces the short cut of the creepage distance. Figure 2.5(6) shows the creepage path as the gap between head of screw and wall of recess is wide.

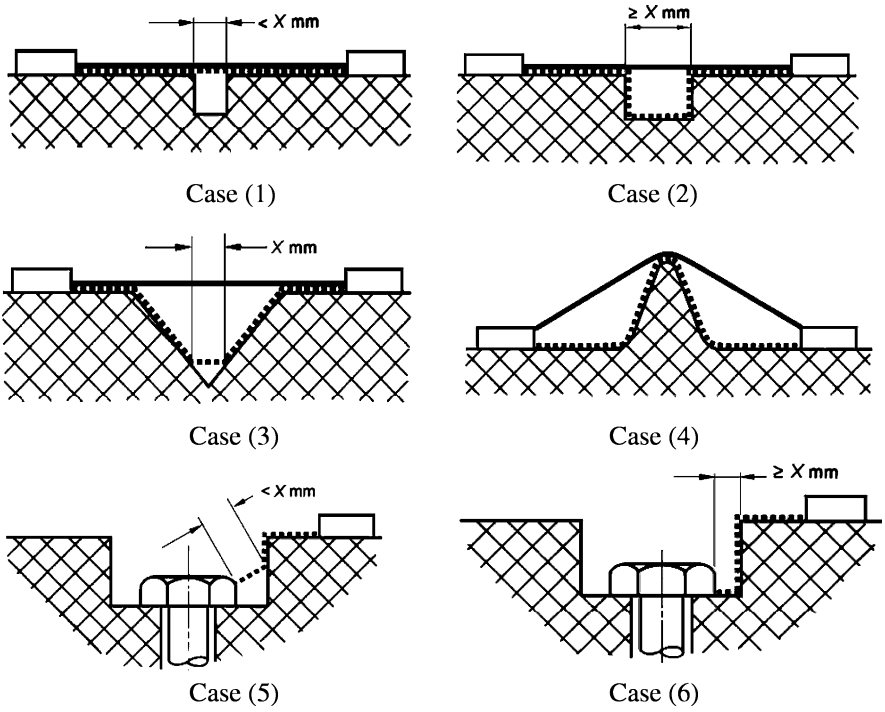


Fig. 2.5 The clearance and creepage distances in different cases when the design variable less or larger than *X* (mm) (IEC 61950-1 ed.2.0. Copyright 2005 IEC Geneva, Switzerland www.iec.ch)

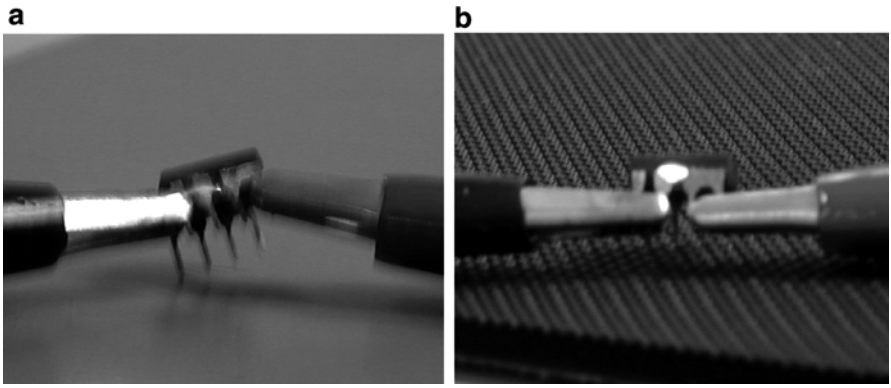


Fig. 2.6 The dielectric breakdown modes of clearance and creepage. (**a**) Clearance, (**b**) creepage

The dielectric breakdown modes are different between clearance and the creepage. The dielectric breakdown of clearance is through air between the leads while the dielectric breakdown of creepage happens on the surface of insulation material such as epoxy mold compound in power packaging. Figure 2.6 shows the two dielectric breakdown modes.

2.3 Estimation of the Clearance and Creepage Distances

2.3.1 Required Major Functions

There are four major functions that can be used to judge the clearance and creepage distances. These functions are pollution degree, comparative tracking index (CTI) value, insulation type, and the working voltage. In Sect. 2.2, the concepts and defintions of pollution degree, insulation type, and the working voltage are introduced, while the CTI value is defined the measurement of the breakdown voltage on surface tracking that a materials exhibits under specific test conditions. Figure 2.7 shows the schmetic diagram of the CTI test. The breakdown voltage is measured by 50 drops 0.1% ammonium chlorde on a 3-mm thick insulating material. Based on the measured result, the insulating materials may be divided into different groups, which normally are three groups: Material Group I, II, and III (see IEC60664-1 [6]). Some standard like UL 746 [7] perfers to divide the CTI results with performance level categories (PLC), which normally have categories: level 0–6. Table 2.4 lists the material groups and the PLC levels with related CTI values based on IEC60664-1 and UL746 standards. If the CTI value of a metrail is not known, apply the material group III for it.

As an example, let's examine the effect of humidity and corrosive chemicals on the breakdown voltage of a 8 lead DIP package. The distance between leads is 1.01 mm as shown in Fig. 2.8. Two group test samples are investigated. One is in the normal operation environment and the other is the samples after autoclave (ACLV) with 96 h.

The test result is shown in Table 2.5. From the Table 2.5, it can be seen that the sample with normal operation, its average breakdown voltage is 3.46 kV with

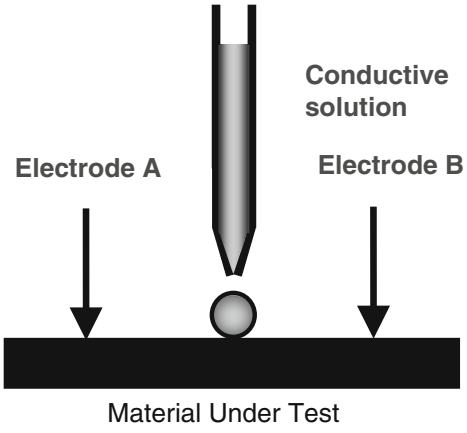


Fig. 2.7 The schemetic CTI test diagram

Table 2.4 Insulating material group and PLC levels

Performance level categories (PLC) UL746	Insulating material group IEC60664-1	CTI (V)
0	I	600 and above
1	II	400–599
2	III_a	250–399
3		175–249
4	III_b	100–175
5		Less than 100

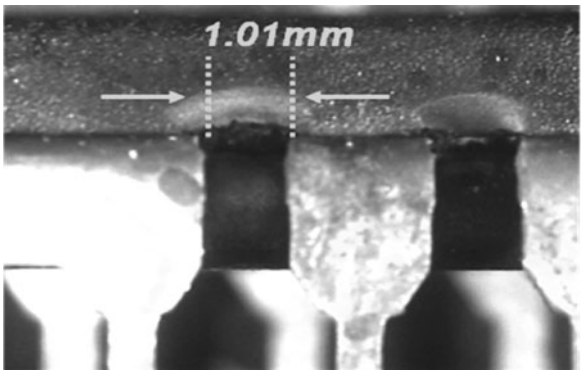


Fig. 2.8 The leads layout of the 8 lead DIP with 1.01 mm distance between leads

Table 2.5 The comparison of the dielectric breakdown voltage CTI value

Breakdown voltage	Minimum (kV)	Maximum (kV)	Average (kV)	Remark
Normal	3.02	3.97	3.46	Clearance
ACLV	1.27	3.75	2.76	Creepage

1.01 mm clearance distance. While the sample after 96 hours ACLV, its average breakdown voltage is 2.76 kV even with creepage distance (greater than 1.01 mm). Therefore, the sample after ACLV has reduced the breakdown voltage about 700 V. This is because the sample after 96 hours ACLV, it has been in a humid and corrosive environment. The humid and corrosive conditions will reduce the breakdown voltage which will be easy to damage the power device.

Figure 2.9 shows two PCB FR4s, one is coated with solder resist and the other does not coat with solder resist. The dielectric breakdown voltages are measured for the two cases in Fig. 2.9. In each case, the clearance and creepage distances

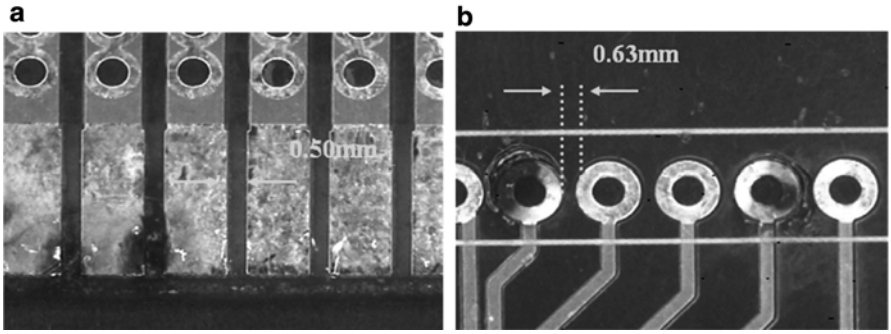


Fig. 2.9 The PCB FR4 with and without the solder resist. (**a**) FR4 coated with solder resist, (**b**) FR4 not coated with solder resist

Table 2.6 The breakdown voltage CTI for the FR4 with and without the solder resist

Test cases	Clearance/creepage distance (mm)	Minimum breakdown voltage (kV)	Maximum breakdown voltage (kV)	Average breakdown voltage (kV)
FR4 without solder resist	0.63	1.37	2.20	1.75
FR4 with solder resist	0.50	2.20	2.65	2.46

are selected the same distance. The results are listed in Table 2.6. From the Table 2.6, it shows that the FR4 with solder resist has larger breakdown voltage (CTI value) than the FR4 without the solder resist which has even larger clearance/creepage distance.

2.3.2 Determine the Clearance and Creepage for Power Package

The package TO-220 for high voltage application like TV is investigated. The working voltage (rms) is 400 V, and the peak working voltage is 1,100 V. The pollutiion degree is 2 for office and home environment. The insulation type is the basic insulation. The material group is III_a or III_b. Based on the standard IEC60950-1 [4] (refer to Tables 2.7 and 2.8), the required minimum creepage distance between the leads of the TO-220 is 4.0 mm, and the required minimum clearance distance between the leads of the TO-220 is 4.2 mm. Therefore, when we design the leadframe for the TO-220 in TV application, the minimum distance between the leads should be 4.2 mm for a reliable product.

Table 2.7 The creepage distance (IEC60950-1, Section 2.10.4, Table 2L) in millimeters (IEC 61950-1 ed.2.0. Copyright 2005 IEC Geneva, Switzerland, www.iec.ch)

WORKING VOLTAGE V r.m.s.or d.c.	FUNCTIONAL.BASIC and SUPPLEMENTARY INSULATION						
	Pollution Degree 1	Pollution degree 2			Pollution Degree 3		
	Material Group	Material Group			Material Group		
	I, II,IIIa or IIIb	I	II	IIIa or IIIb	I	II	IIIa or IIIb
50	See(1)	0.6	0.9	1.2	1.5	1.7	1.9
100		0.7	1.0	1.4	1.8	2.0	2.2
125		0.8	1.1	1.5	1.9	2.1	2.4
150		0.8	1.1	1.6	2.0	2.2	2.5
200		1.0	1.4	2.0	2.5	2.8	3.2
250		1.3	1.8	2.5	3.2	3.6	4.0
300		1.6	2.2	3.2	4.0	4.5	5.0
400		2.0	2.8	4.0	5.0	5.6	6.3
600		3.2	4.5	6.0	8.0	9.6	10.0
800		4.0	5.6	8.0	10.0	11.0	12.5
1000		5.0	7.1	10.0	12.5	14.0	16.0

1) No minimum CREEPAGE DISTANCE is specified for insulation in Pollution Degree 1. However, the minimum CLEARANGE, as previously determined in 2.10.3 or annex G, still applies.
2) Linear interpolation is permitted between the nearest two points, the calculated spacing Being rounded to the next higher 0.1mm increment

Table 2.8 The clearance distance (IEC60950-1, Section 2.10.3, Table 2H) in millimeters (IEC 61950-1 ed.2.0. Copyright 2005 IEC Geneva, Switzerland, www.iec.ch)

WORKING VOLTAGE up to and including		MAINS TRANSIENT VOLTAGE 1 500 v (Nominal AC MAINS SUPPLY voltage ≤150 v)						MAINS TRANSIENT VOLTAGE 2 500 v (Nominal AC MAINS SUPPLY voltage >150 V≤300 v)						MAINS TRANSIENT VOLTAGE 4000 V (Nominal AC MAINS SUPPLY voltage >300 v≤600 v)		
Voltage Peak or d.c.	Voltage r.m.s. (Sinu-soidal)	Pollution Degree 1 and 2			Pollution Degree 3			Pollution Degree 1 and 2			Pollution Degree 3			Pollution Degree 1,2, and 3		
V	V	F	B/S	R	F	B/S	R	F	B/S	R	F	B/S	R	F	B/S	R
71	50	0.4	1.0 (0.5)	2.0 (1.0)	0.8	1.3 (0.8)	2.6 (1.6)	1.0	2.0 (1.5)	4.0 (3.0)	1.3	2.0 (1.5)	4.0 (3.0)	2.0	3.2 (3.0)	6.4 (6.0)
210	150	0.5	1.0 (0.5)	2.0 (1.0)	0.8	1.3 (0.8)	2.6 (1.6)	1.4	2.0 (1.5)	4.0 (3.0)	1.5	2.0 (1.5)	4.0 (3.0)	2.0	3.2 (3.0)	6.4 (6.0)
420	300	F 1.5 B/S 2.0(1.5) R4.0(3.0)												2.5	3.2 (3.0)	6.4 (6.0)
840	600	F3.0 B/S3.2(3.0 R6.4(6.0)														
1400	1000	F/B/S4.2/R6.4														
2800	2000	F/B/S/R 8.4														
7000	5000	F/B/S/R 17.5														
9800	7000	F/B/S/R 25														
14 000	10 000	F/B/S/R 37														
28 000	20 000	F/B/S/R 80														
42 000	30 000	F/B/S/R 130														

2.4 Packaging Design Layout Consideration

The power package design layout may impact the creepage distance and breakdown voltage of the device. Good package design can sugnificantly increase the creepage and breakdown voltage without changing the dimention and outline of the package. Figure 2.10 shows that there are two designs for TO-220 package. One is the regular TO-220 package and one is TO-220 package for the high voltage application. In the design layout of TO-220 for high voltage application, there are two design grooves as shown in the arrow indication in Fig. 2.10. The comparison of the clearance and the creepage distances are listed in Table 2.9. The design of TO-220 for high voltage application with grooves has significantly increased the creepage distance while it keeps the same clearance as the regular TO-220 package.

Figure 2.11 shows the design consideration for the layout of a Fairchild smart power module (SPM®) to check the effect of the inserting grooves and how the dielectric voltage changes with and without the grooves. The size of the groove is 0.5 mm width and 0.8 mm depth in one layout. The other design layout does not have groove. The dielectric breakdown voltages are measured in the two design layouts with and without the grooves.

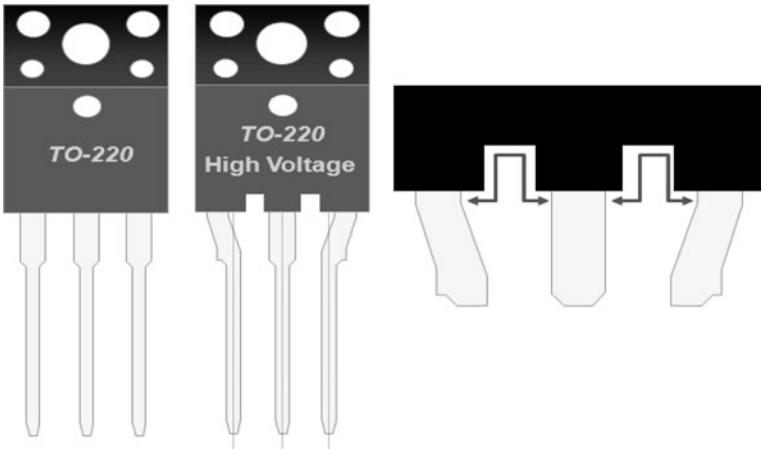


Fig. 2.10 The design layout for high voltage TO-220 package with groove

Table 2.9 The comparison of creepage and clearance distances

Design layout	Creepage distance (mm)	Clearance distance (mm)
TO-220	1.07	1.07
TO-220 HV	5.09	1.07

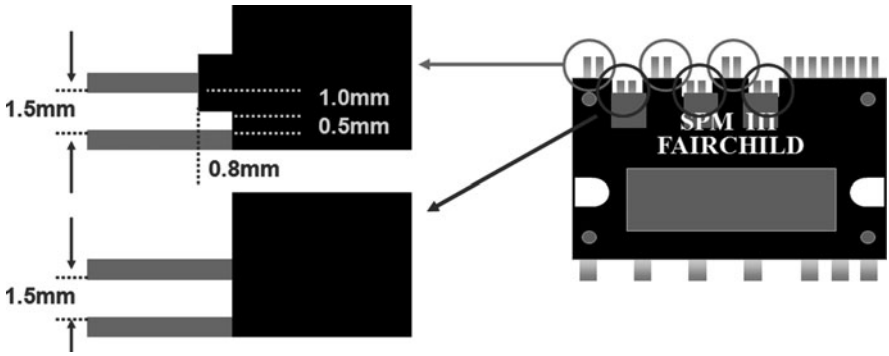


Fig. 2.11 The design layout between pins for a Fairchild SPM package

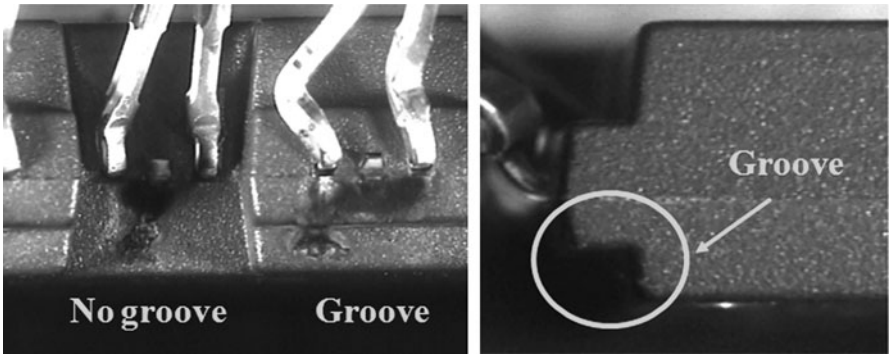


Fig. 2.12 The comparison of designs with and without grooves after the breakdown voltage

Table 2.10 The breakdown voltage measurement for the the two design layouts

Design layout	Minimum breakdown voltage (kV)	Maximum breakdown voltage (kV)	Average breakdown voltage (kV)
With groove	4.32	5.99	5.36
No groove	3.46	5.07	4.20

Figure 2.12 shows the SEM photos of the SPM package with and without the groove after the breakdown voltage. The result of design without consideration of the groove is clearly worse than the case with groove from the surface of the EMC. Table 2.10 gives the measurement result of the breakdown voltage for the SPM package with and without the groove design. The average voltage of the breakdown voltage with the groove design has increased 1.16 kV as compared with the design without consideration of the goove.

Besides the design and layout considerations, materials and mechanical design are two important factors that should not be neglected. Pick components and materials which have prior safety certification. With certified components, the safety engineer looks only to see that they have been applied correctly and physical testing is done only as a complete system. Without certified components, additional component-level testing or excessively conservative design techniques could be required. As an example, the Y capacitor in an input EMI noise filter would be accepted as a certified device, but otherwise might require two capacitors in series to allow a safety test to short one of them, plus the additional testing of the capacitors themselves. For mechanical design, the safety engineer looks for rigid construction with all components securely attached and no sharp edges or corners. All areas containing hazardous voltages have been protected from access by the user, including through any openings in the enclosure. Openings in the enclosure are examined to ensure that there is no user access to hazardous voltage, sharp edges, hot components, fan blades, or any other item that might cause injury.

2.5 Safety Standards and Categories of Application [8–18]

The first international standard for safety, IEC950, was prepared by the International Electrotechnical Commission (IEC) primarily for information technology industry. Later, the IEC had generated a harmonized standard, IEC60950 (third edition), to cover products from the most industries. Upon its release in 1999, it was quickly adopted by most countries and is today the primary standard for safety for most users of power supplies (IEC60950-1 first edition, 2003 and second edition, 2005). In addition to IEC, designations of this standard can be found as EN (European Union), UL (United States), and CSA (Canada). In the USA, the plan is to withdraw approvals to all earlier standards by July, 2006. The US Standard, as of this writing, is UL60950-1, first edition, published in 2003, second edition published in 2007. While UL60950-1 is the most widely applied standard for power supplies, it is also intended for use with information technology, business, and telecom equipment. Other standards exist for other industries, such as IEC 60065 for audio and video, IEC 60335-1 and 2 for household and similar electrical appliances, like air conditioner, refrigerator, vacuum cleaner etc, IEC 60664-1 for equipment within low voltage systems, IEC 60598-1 and 2 for general requirements and tests, IEC 60601 for medical, IEC 61010 for laboratory supplies, and others. The first version of standard, IEC 61204-7, which is intended for use with power supplies sold into multiple industries, was proposed by IEC in 2006. One of the first tasks for power electronic package designers in any new design should be to identify the standards, including recent revisions, which applies to the intended end use. As an example, Table 2.11 lists the basic categories of home applications and the related IEC standards. Figure 2.13 shows the list of other standards that may be used for the power electronic packaging design.

Table 2.11 The basic categories of home applications and related IEC standards

Item	Products of home application	IEC standards
1	Cooking range	IEC-60335-2-6
2	Hair dryer	IEC-60335-2-23
3	Iron	IEC-60335-2-3
4	Microwave oven	IEC-60335-2-25
5	Room air conditioner	IEC-60335-2-40
6	Rice cooker	IEC-60335-2-15
7	Refrigerator	IEC-60335-2-24
8	Vacuum cleaner	IEC-60335-2-2
9	Kettle	IEC-60335-2-15
10	Washing machine	IEC-60335-2-7
11	Home computer system	IEC-60950
12	Coffee maker, slow cooker	IEC-60335-2-15
13	Table, standing lamp	IEC-60598-2-4
14	Toaster, grill, roaster	IEC-60335-2-9
15	Decorative lighting fixture	IEC-60598-2-20
16	TV set, monitor	IEC-60950

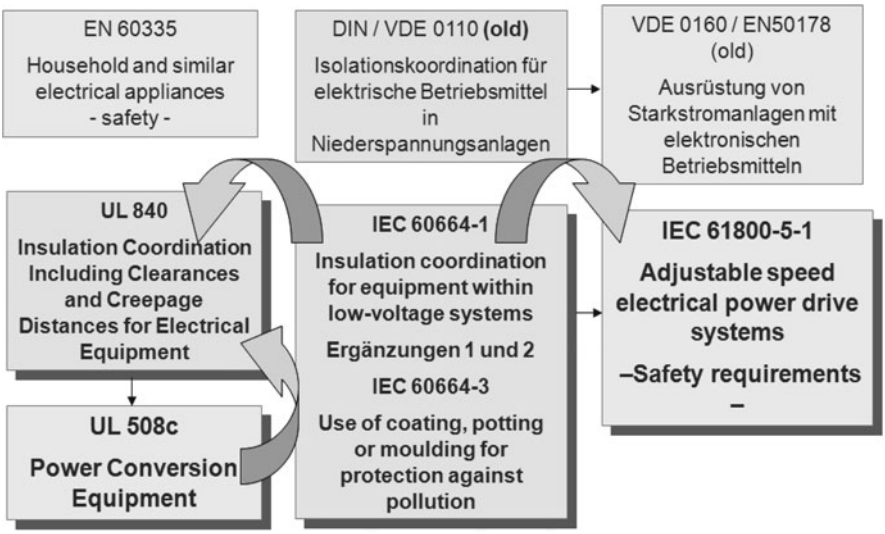


Fig. 2.13 The diagram of other standards for power electronic packaging design

2.6 Summary

This chapter introduces the isolation design for the power electronic packaging. There are many decisions in the design process where a knowledge of safety requirements and the application of their principles can go a long way toward easing the time and cost of the safety certification process. Particularly if a failure in safety testing requires a redesign effort late in the program. Anticipating the testing which may be required and designing accordingly certainly pays off at the end of the day. While definitely not all inclusive, a summary of some of the design considerations for power packaging is given below: (1) The spacing between the power devices and pins is essential in the design of power packaging that needs to meet the requirements of the IEC or UL product safety standards. (2) Increasing the creepage distance in package layout can help to present the arcing and the current leakage across the package surface caused by high voltage or by humidity. (3) In design of the power packaging for isolation, four major functions need to be considered and identified: Pollution degree, CTI value of insulated material, insulating type, and the working voltage. Besides the above isolation design and layout considerations, material selection and mechanical design are two important factors that should not be neglected. It is always necessary to pick components and materials which have prior safety certification and to avoid the sharp edges or corners in mechanical design.

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Chapter 3
Discrete Power MOSFET Package Design and Analysis

In the world of semiconductor packaging, most of the attention is focused on high pin count, stack die/3D/TSV, and mixed-signal ICs integration. But the real workhorses in most system are the power devices that fuel those flashy central processing unit (CPU)s and digital signal process (DSP) ICs for power management and conversion [1, 2]. Discrete power device is one of these applications. Typical discrete products include various Diodes, Bipolars, metal-oxide-semiconductor field effect transistor (MOSFET)s, and insulated gate bipolar transistor (IGBT)s. One development in discrete power package is the trend of more leads for a large die. Example is the leads of the TO-220 package; they have been increased from 3 to 5 or 7 leads and above. The multiple direction heat transfer and lower electrical resistance of drain and source $R_{ds(on)}$ are also the development needs. Since power levels and power density requirements continue to increase for many types of end equipment such as personal computers, servers, network, and telecom systems, it demands higher performance from the components that make up the power management system. This chapter introduces the trends of discrete power package design, material usage, and the analysis of the discrete power package performance.

3.1 An Example of a TO Power Package: Design, Assembly, and Mount Process

TO power product is a very typical discrete power package which is still widely used today. Figure 3.1 shows a power TO-220 package design. Its construction consists of power MOSFET or IGBT die, solder paste for die attach, leadframe and pad, bond wires, and epoxy mold compound (EMC). The drain of the power MOSFET or IGBT connects to a drain lead which is the middle lead and the exposed dap. The source of

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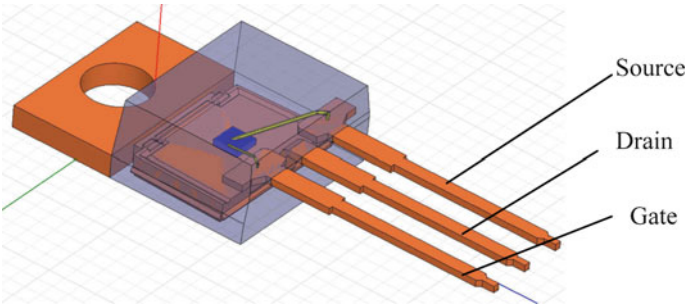


Fig. 3.1 The design of a typical power discrete package TO220

the power MOSFET/IGBT connects to the source lead through a larger diameter metal (such as Al) bond wire. The gate of the MOSFET/IGBT connects to the gate lead with a smaller diameter bond wire. The basic assembly process for a discrete power device includes (1) the power wafer dice, (2) die pick up and die attaches to the dap of the leadframe, (3) wire bonding the source of the power die to the source leads and gate of the power die to the gate lead, (4) molding, and (5) trim/form and singulation [3].

After completing the TO packaging assembly, the discrete power product may be shipped to the customers for use. Normally, the designs often require custom mounting process which basically includes leads forming and the heat sink mounting. Improper handling of lead forming of the devices and the heat sink mounting can result in immediate or latent failure from cracked epoxy, epoxy delamination, die fractures, and bond-wire shearing [4].

Figure 3.2 shows the power discrete package TO220 in lead forming. It discloses the basic guidelines of the lead forming process: (a) Clamp all leads firmly and uniformly between the bend and the mold compound, ensuring that the clamp does not come in contact with the mold compound. The clamping area should be greater than the force required to bend leads to desired form. Leads are normally deformed about 0.03–0.05 mm during clamping. (b) The bending location should be beyound the seating plane area of the leads. (c) The bending radius (R) should always be greater than the thickness (T) of the lead terminal. (d) The leads should never be bent more than 90°. (e) Lead forming should avoid dambar cut area, see Fig. 3.3. The benting radius should be formed outside that area.

Figure 3.4 shows that the leads should not be bent laterally. This will result in the high stress at the interface between leads and mold compound. Figures 3.5 and 3.6 show that the stress disctribution comparison of the normal lead forming and the abnormal lead forming processes. As it can be seen that from these two figures, when the clamps come in contact with the mold compound and the clamping force is not strong enough to grip lead tightly, high stress is induced at leads and

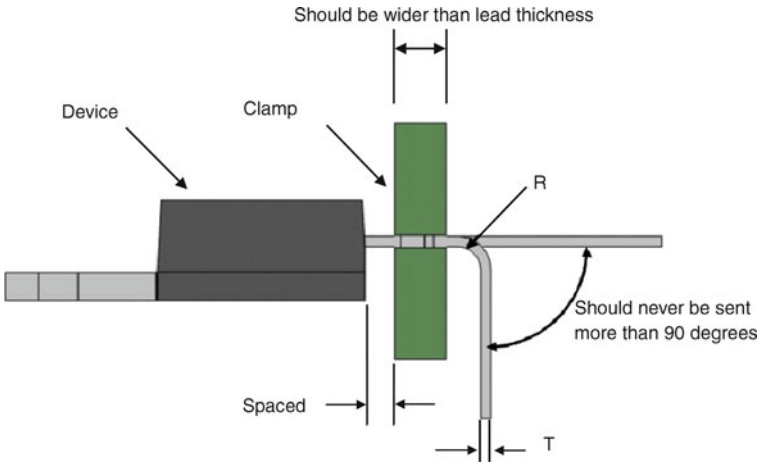


Fig. 3.2 The TO packaging in lead forming of the mounting process

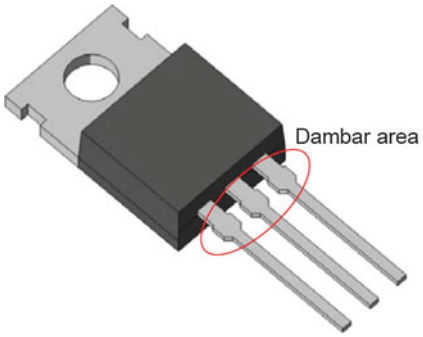


Fig. 3.3 The dambar area of a power discrete packaging

the mold compound while normal clamping does not create much stress in molding compound and adjacent lead.

The use of heat sink is often required to maintain thermal stability within an application. Figure 3.7 shows th discrete power package that mounted on the heat sink and the print circuit board (PCB). The guidelines for mounting the heat sink basically include the following: (a) The surface of the heatsink should be smooth, flat, and clear of dust; (b) The mounting hole in the heat sink should be free of burrs and have no cratering occuring around the hole; (c) Proper application of thermal grease should be applied to fill in any irregularities and decrease the thermal resistance; (d) When the device is mounted on the heatsink and is in a position on PCB,

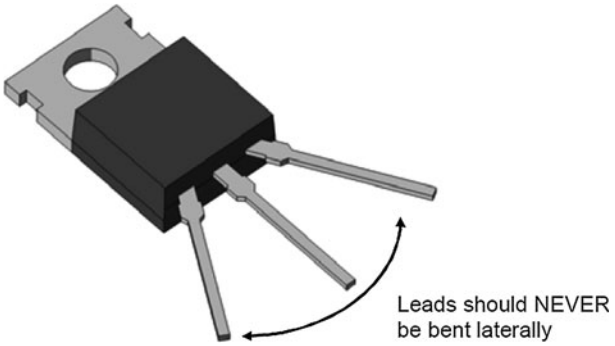


Fig. 3.4 Lateral bending leads

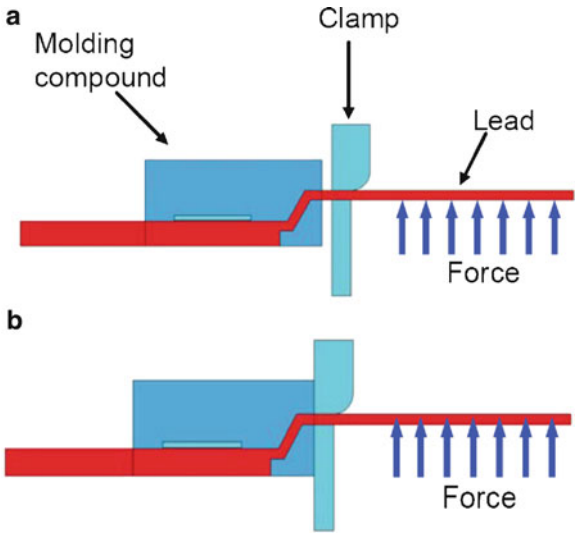


Fig. 3.5 Normal lead forming process vs. abnormal process. (**a**) Lead forming process. (**b**) Abnormal process

there should no additional deformation or stress in any direction. Figure 3.8a shows the corrected mounting position while Fig. 3.8b gives incorrect mounting that may induce high stress in mold compound. (e) The heat sink should be rigidly mounted to the PCB so that the weight of both the device/heatsink is not supported by the leads; (f) The power discrete package should be mounted to heatsink prior to soldering leads to the PCB. Lead forming, if needed, should be done prior to mounting.

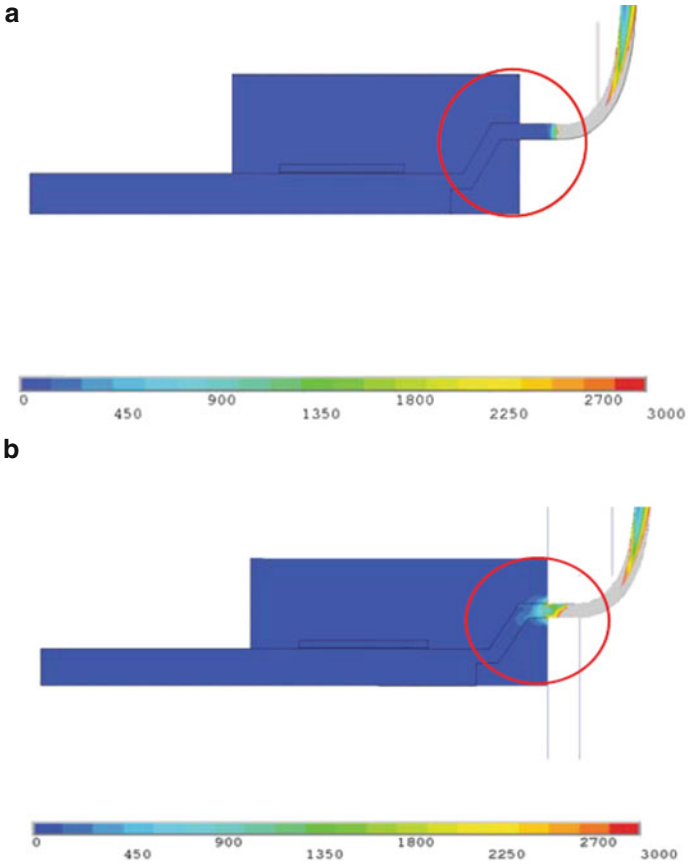


Fig. 3.6 The stress distribution comparison of normal vs. abnormal lead forming processes. (**a**) Von Mises stress in normal lead forming process. (**b**) Von Mises stress in abnormal lead forming process

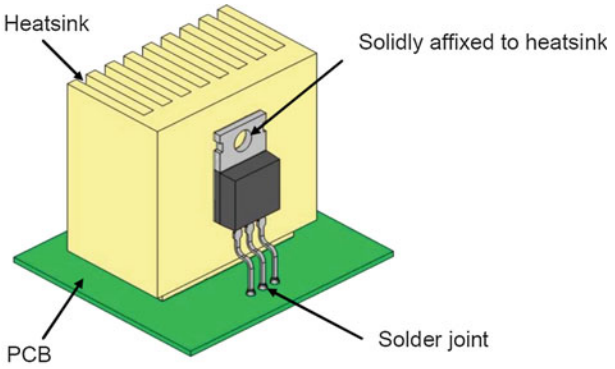


Fig. 3.7 Mounting the discrete power package TO220 on heatsink and PCB

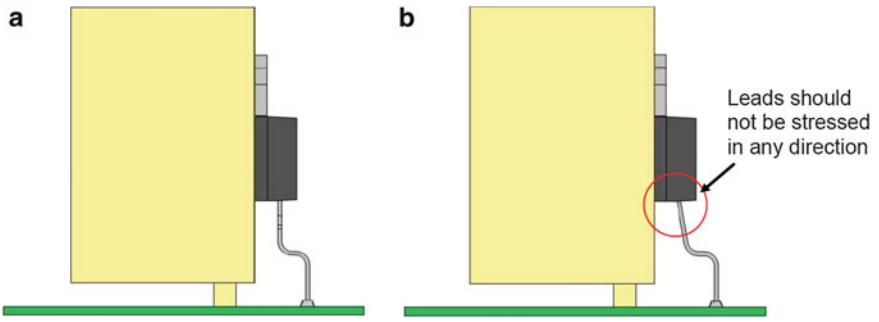


Fig. 3.8 Comparison of the correct and incorrect mounting methods. (**a**) Correct mounting. (**b**) Incorrect mounting

3.2 The Trend of Using Epoxy Mold Compound [1]

Since the discrete product started, most of the power discrete products are molded packages. Typical molded discrete power packages include the three terminal packages, such as small outline transistor (SOT) family; TO family including DAP (TO-252), D2PAK (TO-263); dual-in-line packages, such as small outline (SO) family including thin small outline package (TSOP) family and the thin shrink small outline package (TSSOP) family; and the quad-in-line package such as the quad flat no lead (QFN) family, power quad flat-pack, no leads (PQFN) family with exposed die-pad for heat sink; and the molded leadless package (MLP) families. Figure 3.9 shows an eight leads SO power package. The eight leads SO package includes a leadframe with a die attach pad that connects four leads and the drain of the power MOSFET die. The source of the power semiconductor die connects to the three source leads through bond wires. One gate wire connects the MOSFET gate and the gate lead. The whole package is encapsulated with EMC material. The EMC is a major encapsulated material for the discrete power package. This is because that the EMC can provide substantial protection and mechanical integrity to placed components across a wide generational range of pick and place equipment. However, one drawback of EMC is that its thermal performance is not good as the metal. Therefore, when larger current density request and smaller size become necessary such as in the portable application, the EMC technology is not enough to satisfy these requirements. To meet such requirement in recent years there appears MOSFET ball grid array (BGA) and wafer level chip scale package (WL-CSP) for discrete power device. Figure 3.10 shows the development evolution of the discrete power device. In Fig. 3.10, the Fig. 3.10a is one of the earliest packages for power device TO-263 which is still widely used today for the discrete device. Figure 3.10b, c are the eight leads SO power package with and without the bond wires. In the case of SO-8 without the bond wires, the package uses the metal clip which improves the electrical and thermal performances. Figure 3.10d shows the Fairchild MOSFET BGA, which directly attaches the drain of power MOSFET on the folded

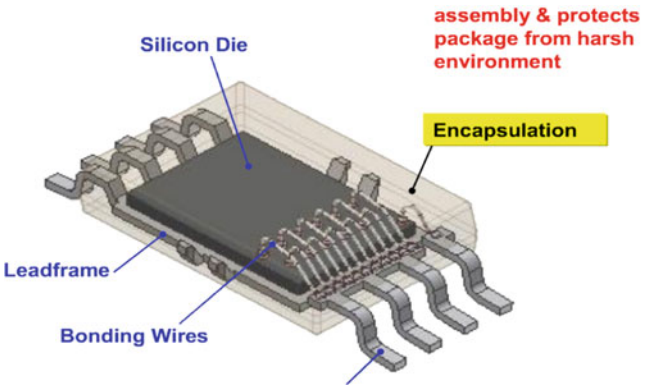


Fig. 3.9 A typical power package SO-8

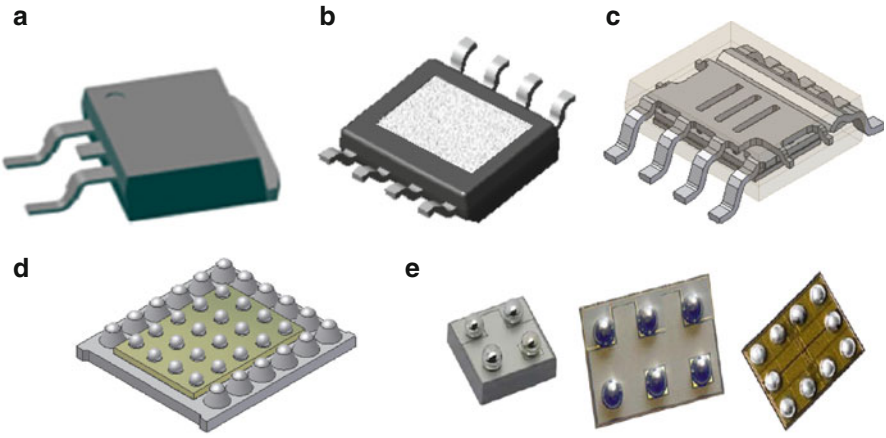


Fig. 3.10 The development evolution of the discrete power package. (**a**) TO-263 package. (**b**) SO-8 package with bond wire. (**c**) SO-8 package with metal clip. (**d**) MOSFET BGA. (**e**) Power MOSFET WL-CSP

leadframe without the epoxy molding compound. The drain of the MOSFET can then be found through the pins of leadframe which locate at the front side of the MOSFET due to the folded leadframe design. Figure 3.10e shows the typical discrete power WLCSP in various products. From the Fig. 3.10, it can be seen that the designs of Fig. 3.10d, e have very good electrical performance due to shrink die size and smaller package size.

Table 3.1 shows some typical development trends of the discrete MOSFET package. It gives the representative power transistor package constituent volumetric percentages. As the package develops from Fairchild early DPAK (TO252) through SO-8 to MOSFET BGA and MOSFET WL-CSP, the molding compound decreases

Table 3.1 Typical discrete power package constituent volumetric percentages

Package type	Total volume (mm^3)	Approximate % EMC	Approximate % silicon	Approximate % lead frame	Approximate% interconnect
TO-252 (wire)	90	75	4	20	1
SO-8 (wire)	28	83	6	10	1
SO-8 (clip)	28	70	6	20	2
MOSFET BGA	20	0	40	50	10
WL-CSP	20	0	82	0	18

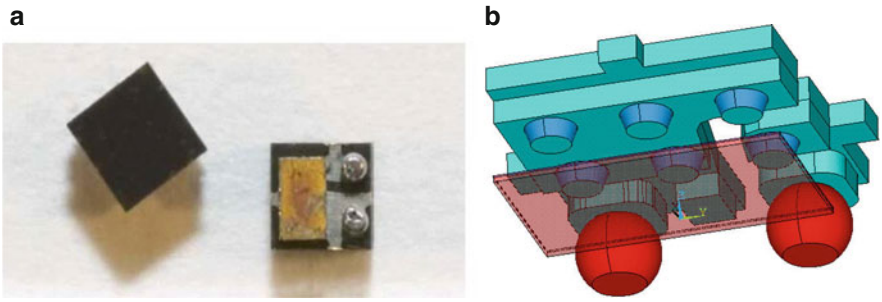


Fig. 3.11 An example of EMC as the substrate. (**a**) The prototype of the MAXFET. (**b**) The internal structure of the MAXFET

as a percentage of volume, until it reaches zero with the MOSFET BGA and WL-CSP packages. At the same time, the silicon and interconnect metal increases as a percentage of volume. At DPAK level, leadframe is about 20% and silicon is about 4%, while EMC is about 75%. At MOSFET BGA level, the leadframe is about 50% and the silicon is about 40%. There is no EMC in the MOSFET BGA.

However, the advantage of EMC is that it can enhance handling and mechanical robustness, as it had in the past. The function of EMC which can provide substantial protection and mechanical integrity to place components across a wide generational range of pick and place equipment is still widely used. So the EMC today in discrete power packages is still useful as a component "encapsulant" or as a premolded substrate component in a modified form. Figure 3.11 shows the use of EMC in nonencapsulant applications. This is a Fairchild prototype premolded lead frame, 1.5 × 1.5 mm MAXFET package. A power MOSFET flip chip is bumped on a premolded leadframe which take the source and gate of the power MOSFET to the same side of its drain through the two solder balls. In terms of disadvantages, EMC can trap moisture under nonideal environmental conditions, which will induce delamination or containment issues.

Figure 3.12 shows a multiple die application of the EMC for a power package 8 × 8 MLP DrMOS with 56 pins plus two drains of the two MOSFETs, which includes a high side MOSFET die, a low side MOSFET die, and an IC controller. The leadframe includes three pads and a 56 leads. The two MOSFET die and one IC

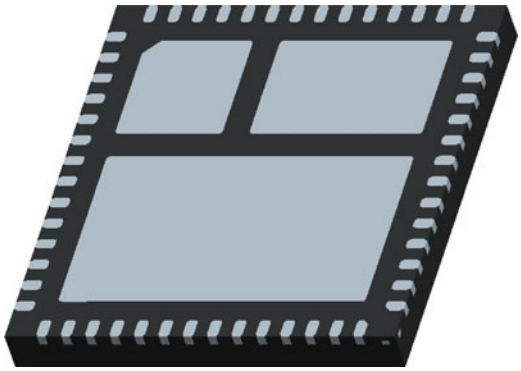


Fig. 3.12 Multiple die DrMOS using EMC

die are attached to the three pads with solder paste for MOSFET and epoxy die attach for IC die side by side. Wire bonding process is applied to all the three dies. The bond wires connects the low side MOSFET drain to high side MOSFET source, as well as the connection of the gate with IC controller and the output pins. All these parts are molded through the panel molding process. The final products are singulated by sawing. The MLP DrMOS product is widely used in lower voltage application for portable products.

3.3 Trends of Current Carrying Capability, Low $R_{ds(on)}$, and Multiple Direction Heat Transfer

One trend of the discrete power package is to increase the current carrying capability per unit area; this is partly due to the customer's request for high current capability and partly due to the die shrinkage. Figure 3.13 shows low voltage discrete package development with different package size in recent years. Figure 3.14 shows the trends of current carrying capability of low power MOSFET package development in the industry, the data was selected from the released products of Vishay, IR, and Fairchild Semiconductor [1]. From Fig. 3.14, we can see as the current carrying capability increases significantly as the low power discrete product develops in recent years. Therefore, this requires the power semiconductor industry to develop the excellent heat dissipation product with such high current density.

To better manage the thermal performance with the trend to higher current carrying capabilities, there are two approaches: one is to intensify the thermal management requirements from the PCB level. Another approach is heat

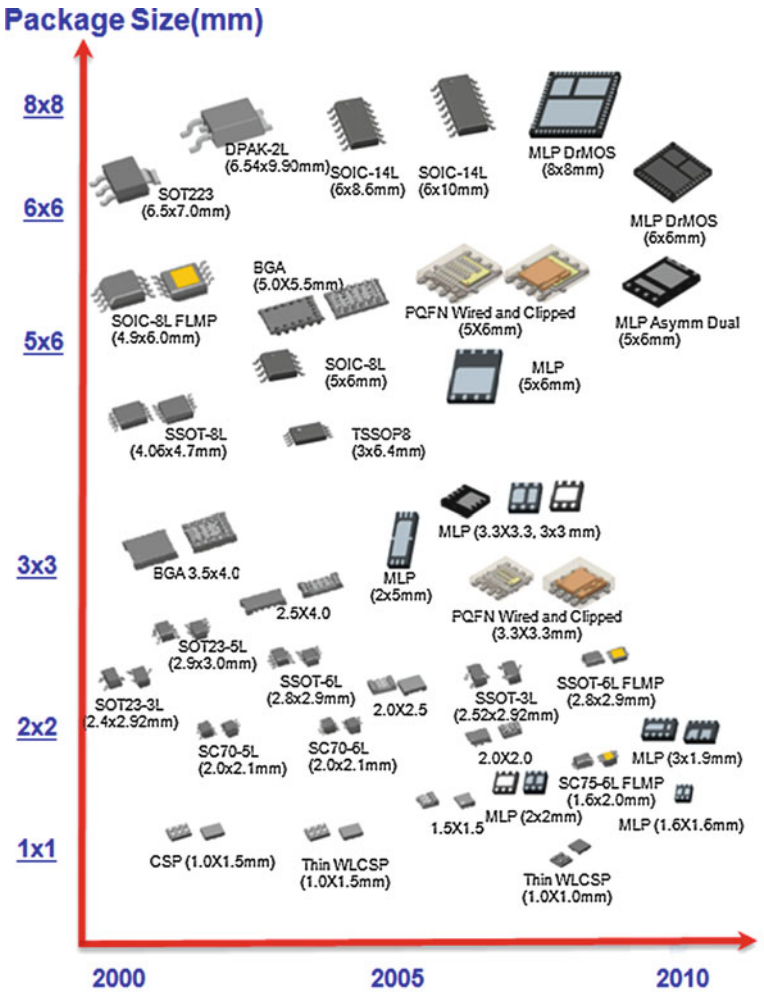


Fig. 3.13 The discrete low power package development

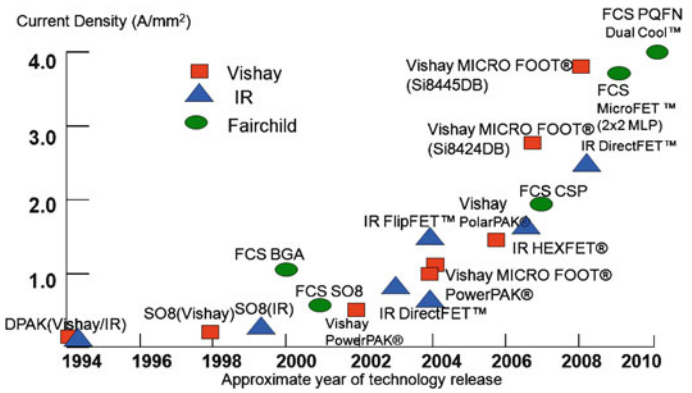


Fig. 3.14 Trends of current carrying density of the low power package development



Fig. 3.15 Multiple direction heat transfer packages

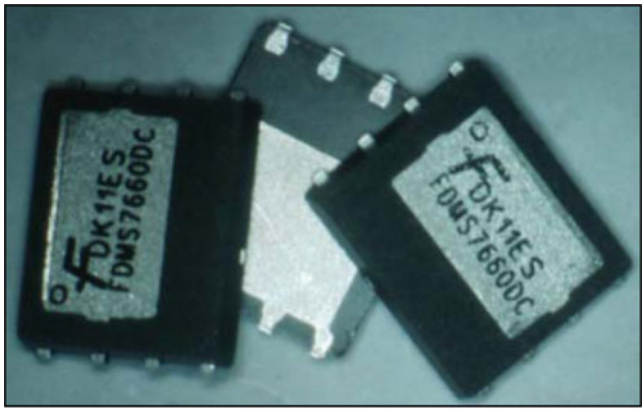
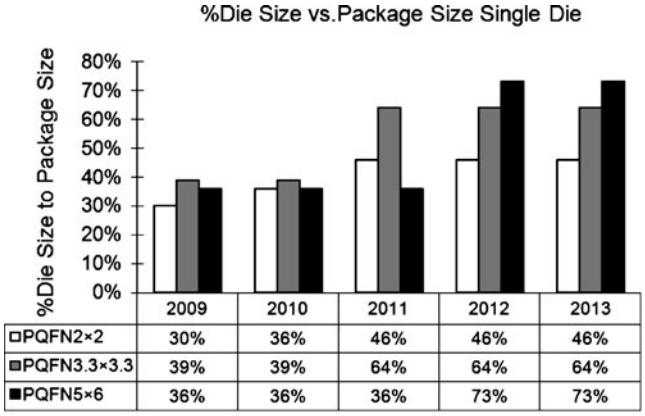


Fig. 3.16 Fairchild PQFN 5 × 6 with dual sided cooling function

dissipation in multiple directions at the package level, which is advantageous for discrete power packages. Figure 3.15 shows the examples of multiple direction heat transfer of Fairchild MOSFET BGA and Vishay POLARPAK™.

Figure 3.16 shows another example for a double side cooling method of Fairchild PQFN 5 × 6 Dual Cool™ package of the low power application in which the drain and source surfaces are exposed with metals directly. Such configuration has both excellent thermal and electrical performances which also makes the trend of ratio of die size and package size become larger and the lower $R_{ds(on)}$. Figure 3.17 shows such trends of PQFN package with larger ratio of die size over the package size. Figure 3.18 shows the thermal resistance which has been significantly reduced after using the Dual Cool™ technology in PQFN package.



	2009	2010	2011	2012	2013
PQFN2×2	30%	36%	46%	46%	46%
PQFN3.3×3.3	39%	39%	64%	64%	64%
PQFN5×6	36%	36%	36%	73%	73%

Fig. 3.17 The trend of the die size over package size for PQFN package

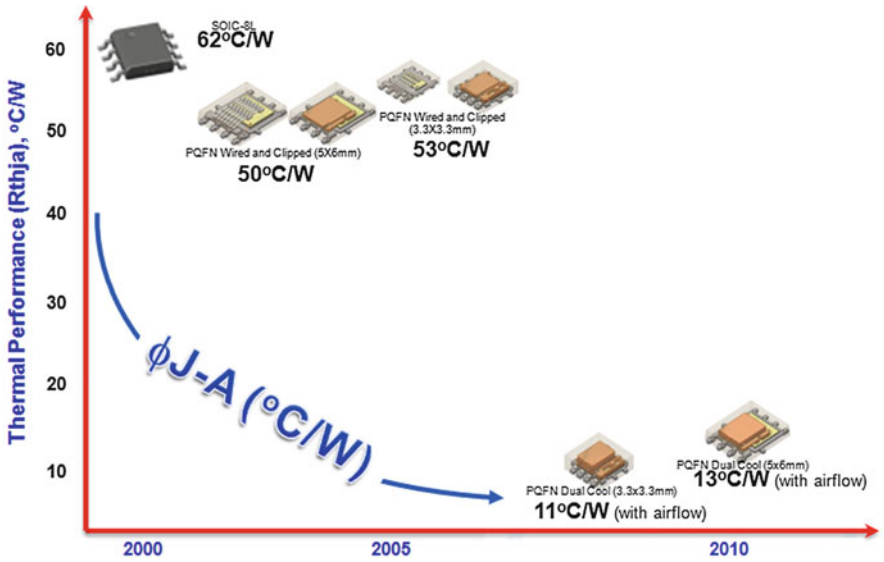
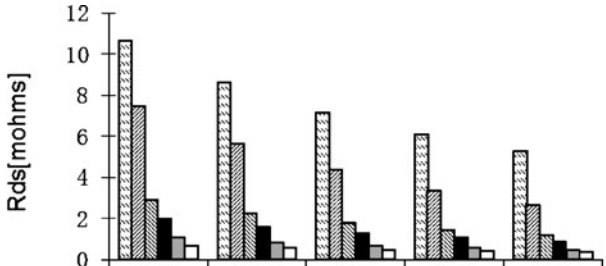


Fig. 3.18 The thermal resistance vs. the package development

To get lower $R_{ds(on)}$ and to improve the thermal performance, there is a shift from wire bonding to technologies such as clips. A metal strap and metal clip structure with solder paste to connect the die were developed. Figure 3.19 gives the comparison and the development trend of the $R_{ds(on)}$ of the power package wire bond MLP, clip bond PQFN and Power clip package. In Fig. 3.19, MLP 2 × 2 is wire bonding based lead less molded package while the Power Clip 2 × 2 is the same size package



	2009	2010	2011	2012	2013
MLP2×2	10.64	8.63	7.15	6.06	5.25
PowerClip2×2	7.42	5.64	4.33	3.36	2.65
PQFN3×3	2.86	2.23	1.76	1.41	1.16
PowerClip3×3	1.97	1.57	1.27	1.06	0.89
PQFN5×6	1.06	0.84	0.67	0.55	0.47
PowerClip5×6	0.65	0.54	0.45	0.39	0.35

Fig. 3.19 The $R_{ds(on)}$ comparison of typical power packages MLP, power clip and PQFN

with the clip structure to replace the bond wire. It can be seen from the Fig. 3.19 that the Power Clip package with clip structure has much smaller $R_{ds(on)}$ than the MLP package with bond wires. Furthermore from the Fig. 3.19, it can also be seen that PQFN 5 × 6 and Power Clip 5 × 6 have the excellent electrical performances with the lowest $R_{ds(on)}$.

3.4 Typical Discrete Power Package Designs and Constructions

In this section, three typical discrete power package designs and constructions are introduced. One is the SO-8 bond wireless power package with clip to replace the bond wire; the second one is the flip leaded molded package in which the drain of the MOSFET locates at the same surface of the leads; the third one is the MOSFET BGA.

3.4.1 The SO-8 Wireless Power Package

Figure 3.20 shows the SO-8 wireless design construction chart, which includes seven parts. The first one is the drain metal clip which basically is made of Cu alloy with Ni plated. The design of the drain clip is to connect to the leadframe by V grooved pad. The second part is the solder paste materials between the Die and clip attach materials. Part three is the MOSFET die with source and gate array. The fourth part is the solder bumps on the source and gate array. The fifth part is the gate

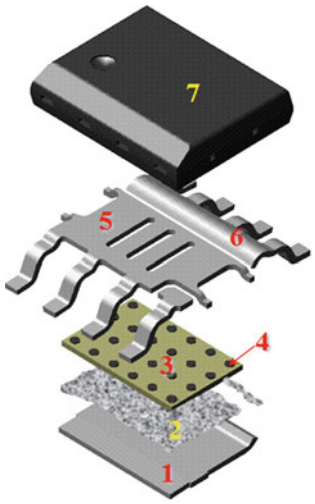


Fig. 3.20 The design construction of package SO-8

and source pad frame with three source leads and one gate lead. The design is coplanar source and gate pads. The sixth part is the V-grooved drain pad frame with four leads, in which the design is coplanar with source pad and is fused to the four drain leads. The V-grooved drain pads, source and gate pads are within one matrix leadframe. The last part 7 is the EMC to package the parts 1–6 by molding process.

The typical assembly process of the power packaging SO-8 wireless has five major steps (see Fig. 3.21): (a) The solder paste is dispensed on leadframe; the flip chip die is picked up and is attached on the leadframe with the solder paste, and the reflow process is applued to bond the MOSFET die; (b) Solder paste is dispensed on the back surface of the MOSFET die and the drain clip is attached on the solder paste of the back surface of the MOSFET; (c) The molding process is applied following by debar and dejunct process; (d) Then is the strip plating process; (e) Marking is applied on the surface of the EMC and then trim/form/singulate the SO-8 package from the leadframe. After that, the final electrical test is carried out following by tape and reel process.

3.4.2 The Flip Chip Leaded Molded Package

The design concept of the Flip Chip Leaded Molded Package (FLMP) is to use the flip chip MOSFET die bumping on the leadframe, then mold the leadframe and the flip chip. Figure 3.22 shows its construction on a PCB. The FLMP includes a MOSFET flip chip die, solder bumps and solder paste, leadframe, and the EMC. The MOSFET die is placed in such a way that its drain surface is exposed in the same plane as the leads. Figure 3.23 shows the major assembly process steps of the FLMP.

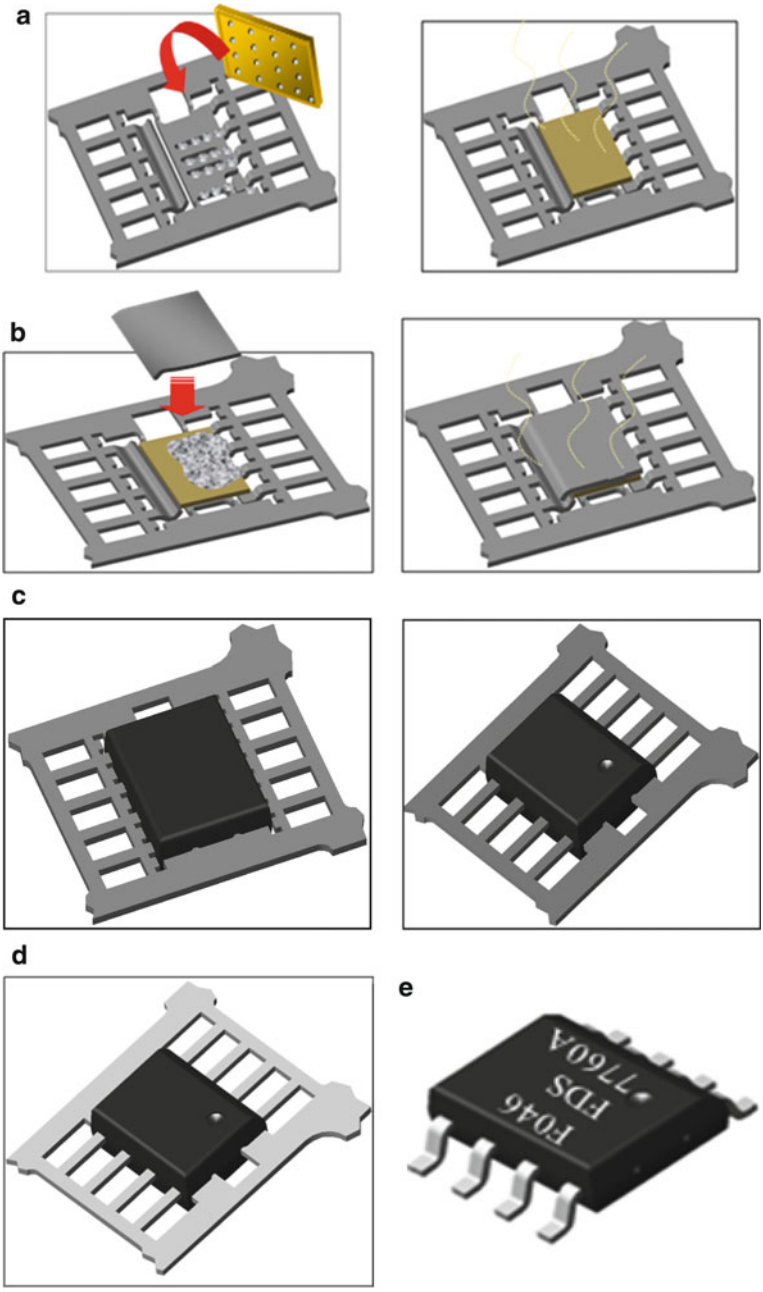


Fig. 3.21 Typical assembly process for SO-8 wireless. (**a**) Solder paste dispensing, flip chip attach and reflow. (**b**) Solder paste dispensing and drain clip attach. (**c**) Molding,debar and dejunct. (**d**) Strip plating. (**e**) Mark, trim/form and singulation

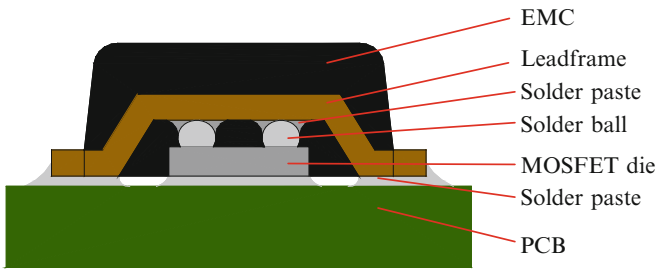


Fig. 3.22 The design constructure of the FLMP

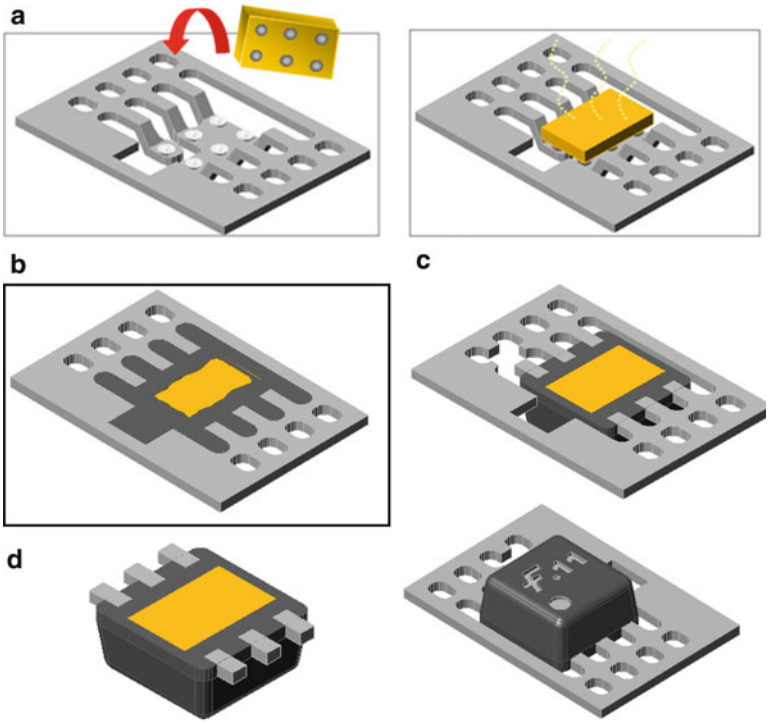


Fig. 3.23 The major FLMP assembly process. (**a**) Flip chip attach and reflow. (**b**) Film assisted molding. (**c**) Gate lead cut, strip test, and the laser mark. (**d**) Trim/singulation

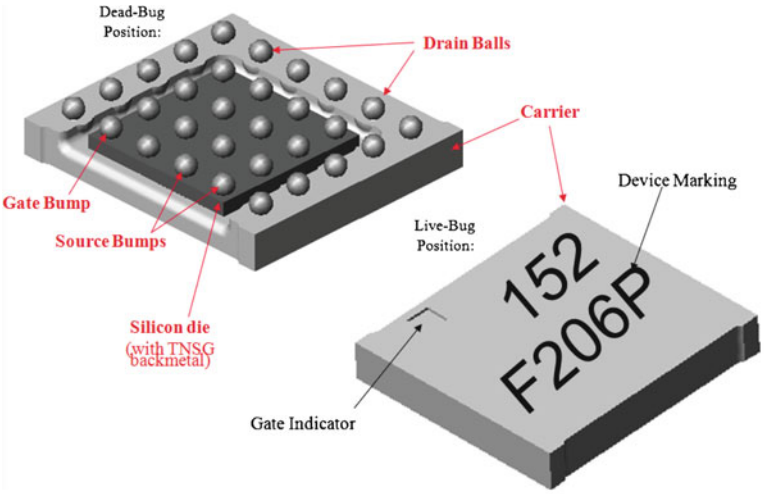


Fig. 3.24 The MOSFET BGA construction

The major assembly process of FLMP has four major steps: (a) The solder paste is dispensed on leadframe, the flip chip MOSFET die is attached on the leadframe, and the reflow process is applued to bond the MOSFET die; (b) The molding process is applied with film assisted method to remove the tolerance of the MOSFET drain surface and the leads; (c) Cut the gate lead, strip test, and laser mark; (d) Trim/form/singulate the FLMP package from the leadframe. Then comes the final electrical sort, tape and reel process.

3.4.3 The MOSFET BGA

The design construction of MOSFET BGA includes the MOSFET die with bumps, leadframe carrier, solder balls and paste as shown in Fig. 3.24.

The typical assembly process for MOSFET BGA is shown in Fig. 3.25. The first assembly step is to make the fluxing on the leadframe. Then attach the solder ball on it and reflow (Fig. 3.25a). The second step is to dispense the solder paste on the leadframe die attach pad and attach the MOSFET die (Fig. 3.25b). The third step is to have the strip test followed by the laser marking. The last step is to singulate the MOSFET BGA from leadframe by punch and to make the tape and reel (Fig. 3.25).

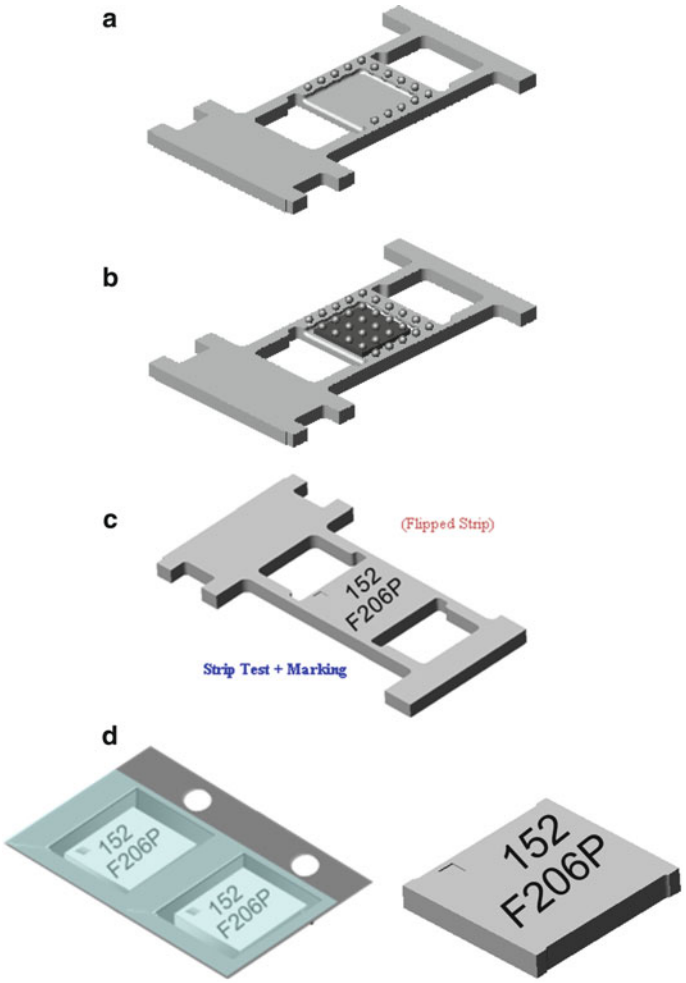


Fig. 3.25 Assembly process for MOSFET BGA. (**a**) Fluxing, Solder ball attach and reflow. (**b**) MOSFET die attach and second time reflow. (**c**) Strip test and marking. (**d**) Singulation, tape and reel

3.5 Power VDMOSFET WL-CSP with Cu Stud Bumping

3.5.1 The Cu Stud Bumping Construction on a Power WL-CSP

Power WLCSP may have different bumping options. There are two major bumping technologies (see Fig. 3.26): One is the regular UBM based bump method which normally selects high Pb solder material with high melting temperature to keep the bump height under reflow. The other is the Cu stud bump method which may use the Pb free solder material with lower melting temperature due to the height of Cu stud

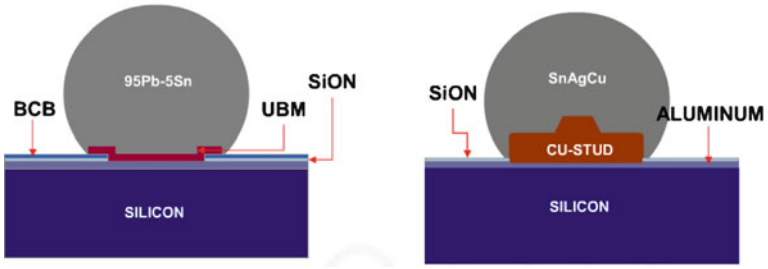


Fig. 3.26 Power WLCSP bumping options: UBM vs. Cu stud

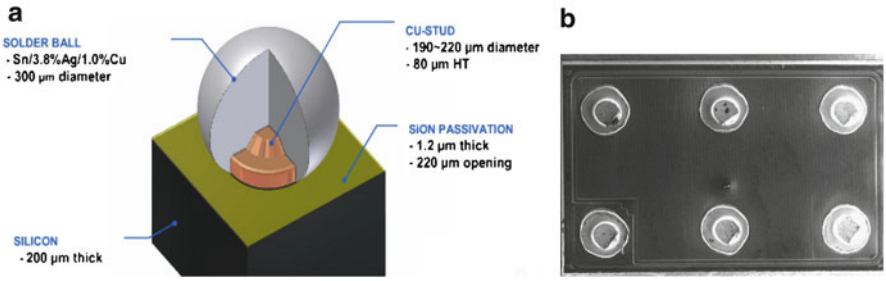


Fig. 3.27 WL-CSP Cu stud bumping package. (**a**) The construction of a Cu stud bumping. (**b**) The Cu stud layout on the source and gate

bumping. The UBM based solder bumping is much more expense than the Cu stud bumping process. In addition, the Cu stud bumping may use the SAC Pb free solder materials due to the Cu stud which satisfies the requirement of the customers and is the trend of power WLCSP with Pb-free solder. Figure 3.27 shows the construction of the copper stud bumping structure on the metal of the power chip. It includes the solder ball, Cu stud, SiON passivation, metal Aluminum, and the silicon substrate.

3.5.2 Investigation of BPSG Design Profile Under the Al Layer and FAB Size on Cu Stud Bumping Process

It has been seen that one of the advantages of Cu stud bumping is the lower cost. However, due to the Cu stud bumping process and the harder material properties of Cu, it might induce the potential cratering on the silicon as well as the crack on the the device layer, such as the borophosphosilicate glass (BPSG) layer (see the Fig. 3.28).

In Cu stud bumping process, the wire bonder forms a free air ball (FAB) on the tip of a wire protruding from the capillary. The capillary then descends to the work surface and bonds the ball. Instead of moving on to form a wire loop, as in a typical wire bond process, the capillary rises and shears off the wire above the ball before

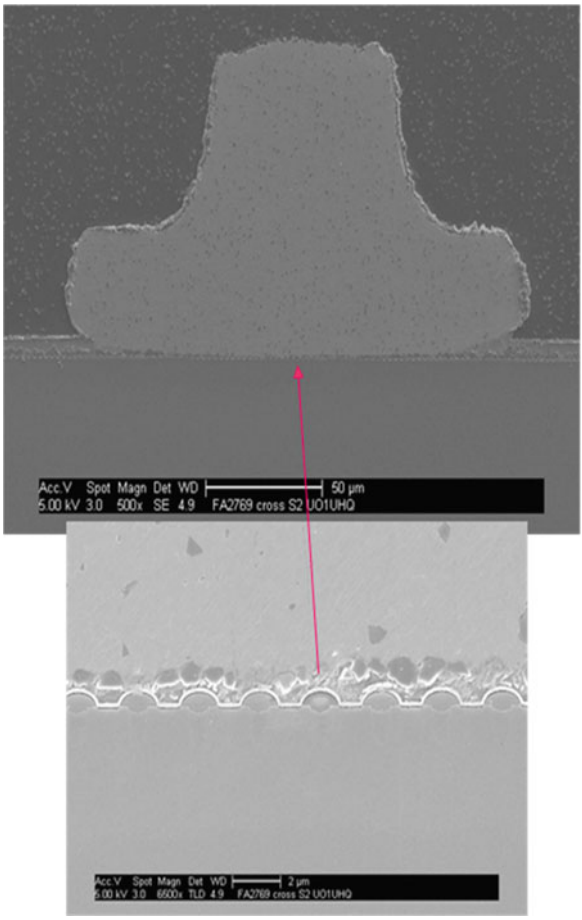


Fig. 3.28 The BPSG device under the Cu stud bumping

forming a new ball. The process is repeated for as many bumps required on the device. The Cu stud bumping process consists of two distinct steps: one is the cu wire bonding process [5] and the other is the shearing process as shown in Fig. 3.29. Stud bumping is significantly faster than wire bonding, because all of the looping motions of normal wire bonding are not needed. Incorporating wire bond technology as a part of the flip-chip cu stud bumping process is attractive because existing facilities and infra-structures can be used without the high capital costs required by more expensive sputter/plating facilities inevitable in the conventional flip chip process. This technology has several advantages: a UBM process is not necessary, bumping cost is low and fine-pitch and chip-level bumping is possible [6, 7].

During the Cu stud bumping process, wafer cratering may be induced. Cratering means the copper stud comes off and creates a local deformed area in the silicon or interlayer dielectric under the bond pad [8]. The numerical analysis of the Cu stud

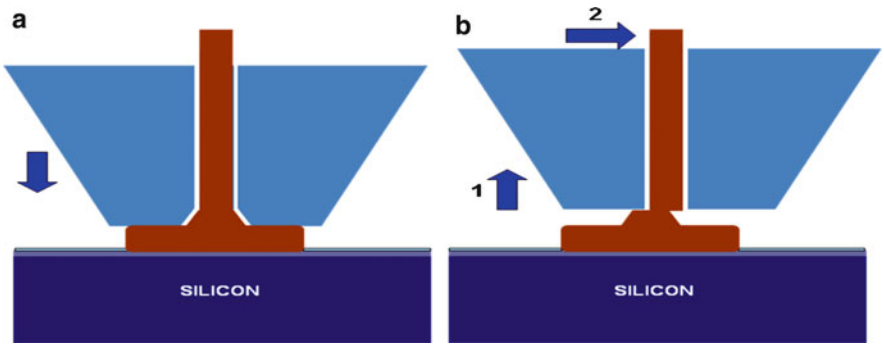


Fig. 3.29 The Cu stud bumping process. (**a**) Capillary moving down for wire bonding. (**b**) Capillary lifting and shearing

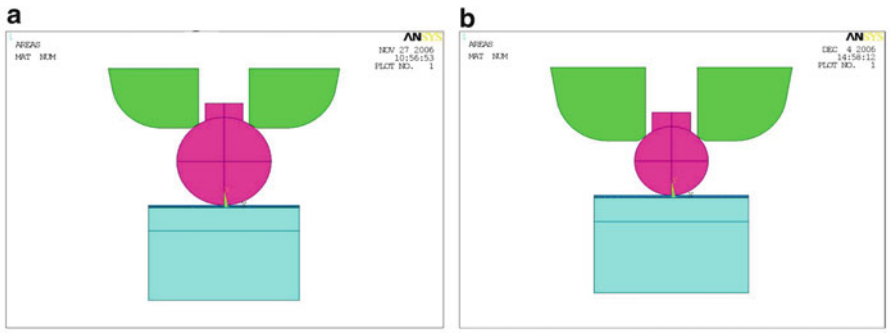


Fig. 3.30 A 2D FEA model including silicon, Cu wire and capillary with different FAB size: (**a**) 190 μm (**b**) 145 μm

bonding and shearing process is conducted by using the commercial finite element code ANSYS®. The impact of three BPSG profiles: dome shape, square shape and M shape, and two FAB diameters: 190 and 145 μm are studied. Experimental results of the bond crater test are discussed for the wafers with these three different BPSG profiles.

3.5.2.1 Bumping Model

A 2D FEA bumping model is shown in Fig. 3.30, which includes power die, Cu wire and capillary. The power device includes silicon layer, BPSG layer, TiW layer, and Al metal layer (see the local structure under the Al metal of Fig. 3.31). During the Cu stud bumping process, an ultrasonic power is applied to the capillary to form the ball bond.

The 2D FEA models with two different FAB sizes 190 and 145 μm are illustrated in Fig. 3.30. The silicon structure with three different BPSG profiles dome shape, square shape and M shape are shown in Fig. 3.32, together with the actual BPSG SEM pictures.

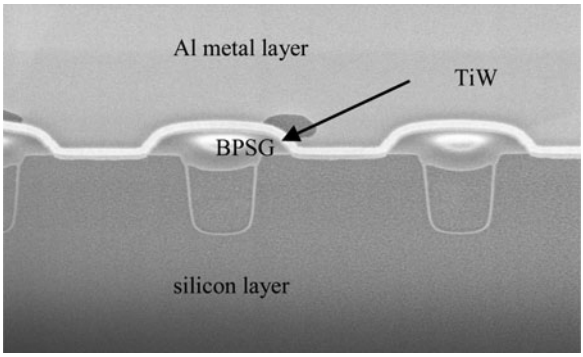


Fig. 3.31 local structure under the Al metal

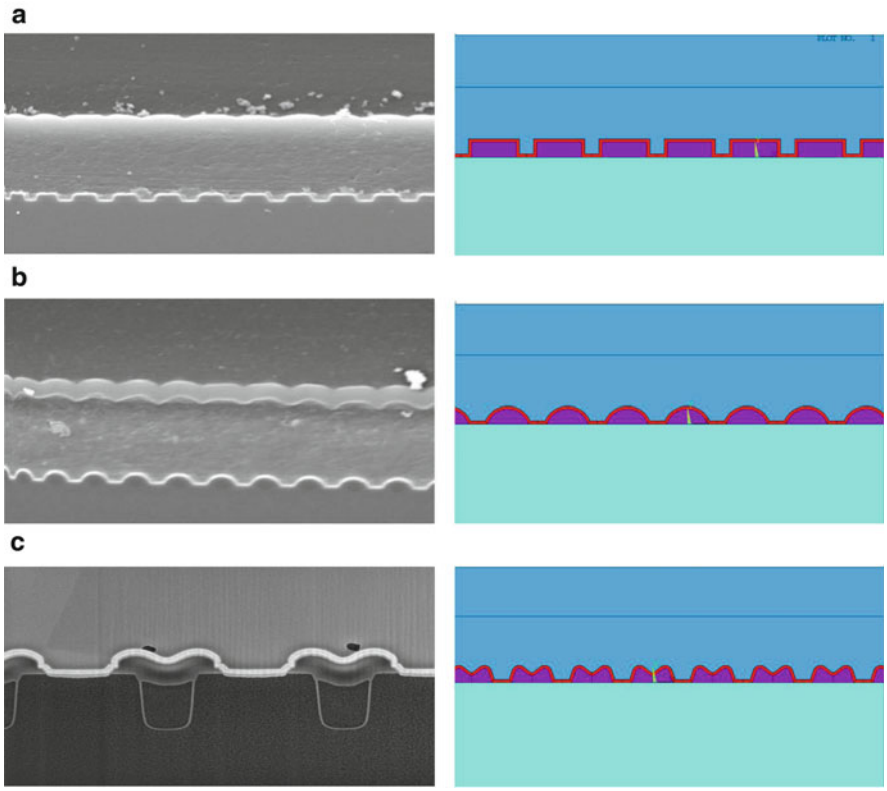


Fig. 3.32 Wafer structure with different BPSG profiles: (**a**) square shape (**b**) dome shape (**c**) M shape

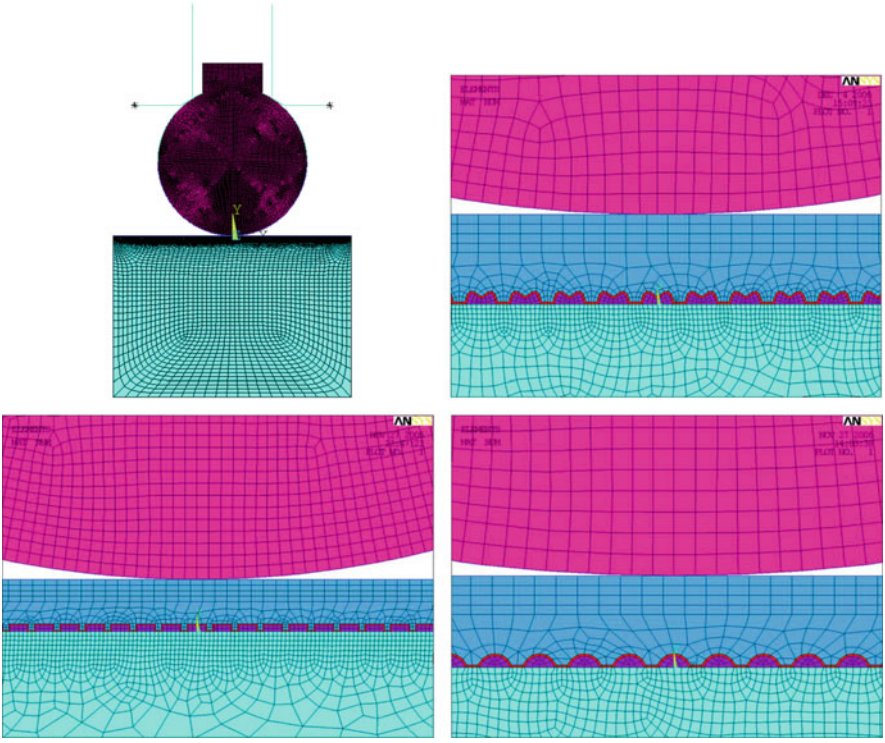


Fig. 3.33 FEA mesh of the bonding model with different BPSG

The Cu stud bumping process consists of bonding and shearing. In the following sections, the simulation procedure and results discussion are described separately.

3.5.2.2 Bonding Process Simulation

In the bonding process, the capillary vibrates laterally due to the ultrasonic power; at the same time, it presses the FAB downward to form the ball bond. To simplify the simulation process, ultrasonic effect is neglected, and the bond force is substituted by an equivalent downward displacement. Two contact pairs are defined. One is between the capillary and FAB, the other is between the FAB and Al metal layer of wafer. The friction coefficient between capillary and FAB is assumed to be 0.4 and that between FAB and Al metal is assumed to be 0.8. The mesh of the FEA model is illustrated in Fig. 3.33.

1. Effect of FAB size for dome shape BPSG profile.
   The deformation contour of the model after bonding process is shown in Fig. 3.34, with two different FAB sizes 190 and 145 μm. The simulation results show that the deformation of 190 μm FAB is larger to obtain the proper final ball bond shape.

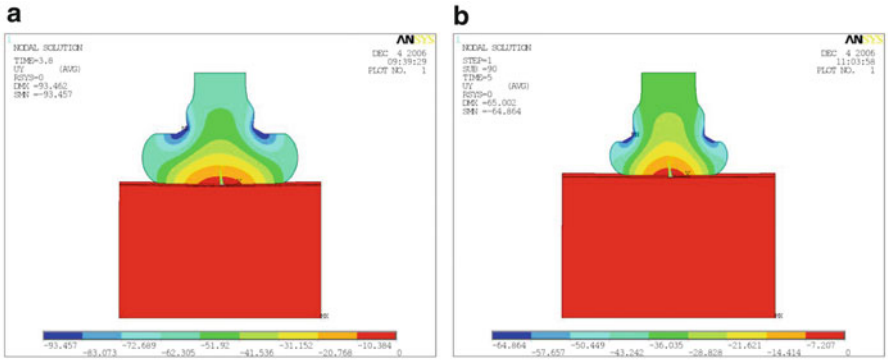


Fig. 3.34 Deformation of the model after bonding process with different FAB size: (**a**) 190 μm (**b**) 145 μm

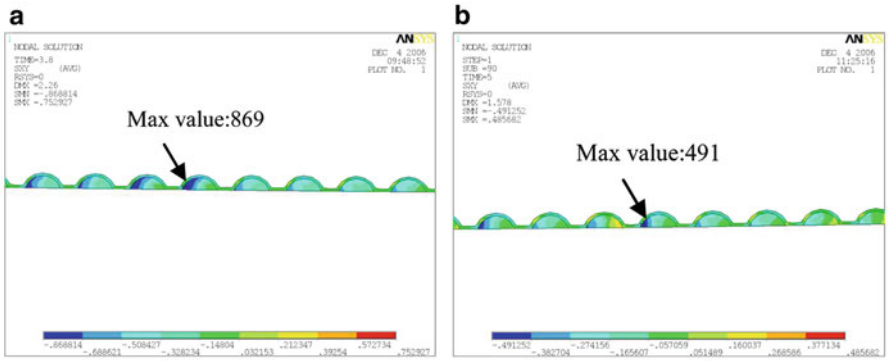


Fig. 3.35 Shear stress distribution in BPSG/TiW layer with different FAB size: (**a**) 190 μm (**b**) 145 μm

Shear stress distribution of BPSG/TiW layer is shown in Fig. 3.35. It can be seen that smaller FAB size induces less stress in BPSG/TiW layer, thus producing less destruction of these layers during bonding process.

2. Effect of BPSG profile with 145 μm FAB.
   The shear stress distribution of BPSG/TiW layer are illustrated in Fig. 3.36 for square and M shape BPSG profile. By comparing with Fig. 3.35b for dome shape BPSG profile, it can be seen that the M shape BPSG induces the largest stress in BPSG/TiW layer after the bonding process.

3.5.2.3 Shearing Process Simulation

During Cu stud bumping process, first the ball bond is formed in the bonding process as described in Sect. 3.5.2.2, then the capillary rises and shears off the wire above the

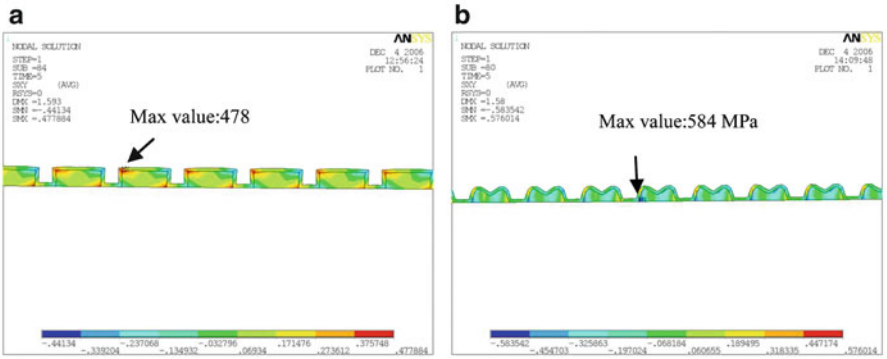


Fig. 3.36 Shear stress distribution of the BPSG/TiW layer for different BPSG profiles: (**a**) square shape (**b**) M shape

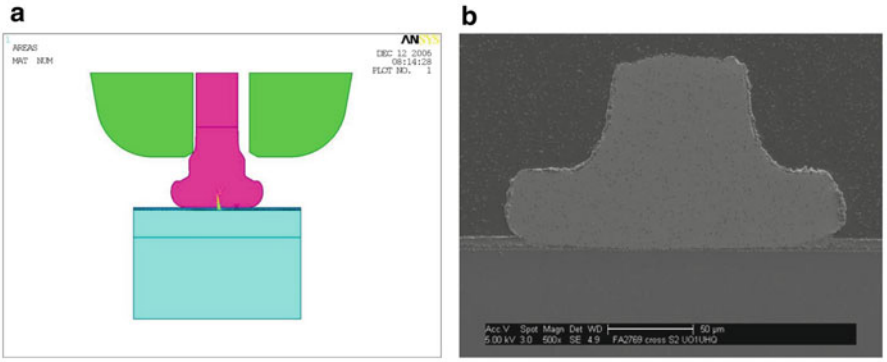


Fig. 3.37 (**a**) FEA model for shearing process. (**b**) Real SEM picture of finished Cu Stud

ball bond, which is regarded as shearing process. The FEA model for shearing process is shown in Fig. 3.37. The shearing height is based on the picture of the actual finished Cu stud shown in Fig. 3.37b. A horizontal displacement 75 μm is applied to the capillary as the shearing load. It is assumed that the ball bond is connected to the Al metal layer ideally, no separation occurred during the shearing simulation.

1. Effect of FAB size for dome shape BPSG profile.
   The shear stress contours of the BPSG/TiW layer with two smashed FAB sizes under shearing process are illustrated in Fig. 3.38. It can be seen that smaller FAB size with diameter 145 μm induces significantly large stress during the shearing process.
2. Effect of BPSG profile with 145 μm FAB.
   The shear stresses in BPSG/TiW layer and BPSG layer are illustrated in Fig. 3.39 for square and M shape BPSG profiles. By comparing with Fig. 3.38b for the dome shape BPSG profile, it can be found that the shear stress in the dome shape BPSG/TiW layer is the lowest.

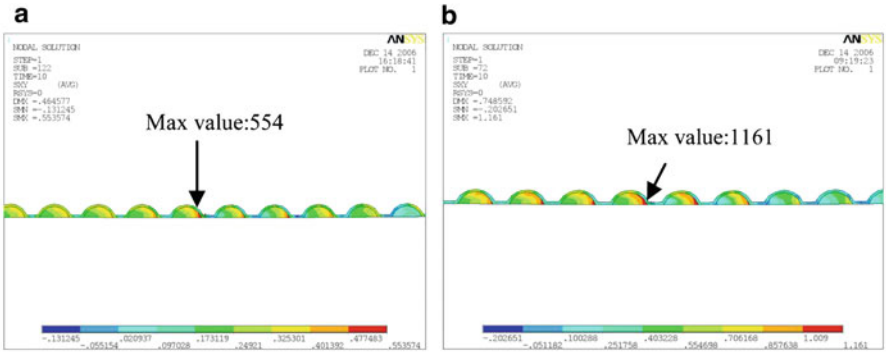


Fig. 3.38 Shear stress distribution in BPSG/TiW layer with different FAB size: (**a**) 190 μm (**b**) 145 μm

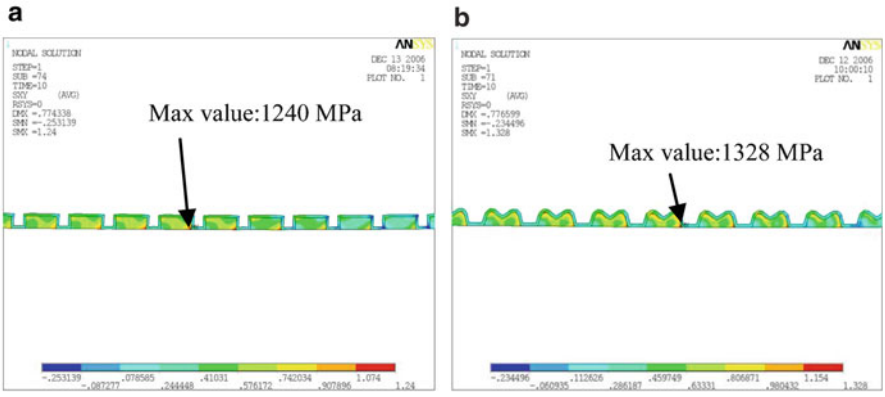


Fig. 3.39 Shear stress distribution in BPSG/TiW layer for different BPSG profiles: (**a**) square shape (**b**) M shape

3.5.2.4 Experimental Results and Discussion

Experiment is conducted to investigate the BPSG profile impact to the cratering on silicon.

The experiment results are listed in Table 3.2. Crater check is conducted after Cu stud bumping and solder ball reflow for the three settings of the BPSG. No bond cratering occurred for all the cases with different BPSG profiles and setting in Table 3.2. This indicates that with the process used, the BPSG profile might not be sensitive to silicon cratering in the Cu stud process. This result seems consistent with the FEA simulation results, which show that the stresses on the silicon dice with different BPSG shapes do not have significant difference in Cu stud bumping, while the stress on silicon with M shape BPSG is the largest. However, the reliability tests for the same settings of the BPSG profile has shown the fails in solder ball shear test and in 72 HTSL test, see Table 3.3. This indicates that the M shape BPSG is not strong enough in its reliability test even if it can pass the bond crack check after the Cu stud bumping.

Table 3.2 Experimental results for bond crater check

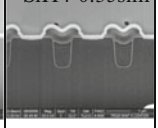
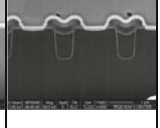
BPSG profile / test	SiH4-0.15slm	SiH4-0.24slm	SiH4-0.35slm
			
Bond crater test (after Cu stud bumping)	0/128	0/128	0/128
Bond crater test (after solder ball reflow)	0/128	0/128	0/128

Table 3.3 Reliability test result

BPSG profile / test	SiH4-0.15slm	SiH4-0.24slm	SiH4-0.35slm
			
Cu stud bump shear test	pass	pass	pass
Solder bump shear test	pass	pass	fail
72 hours HTSL	0/248	0/244	1/247

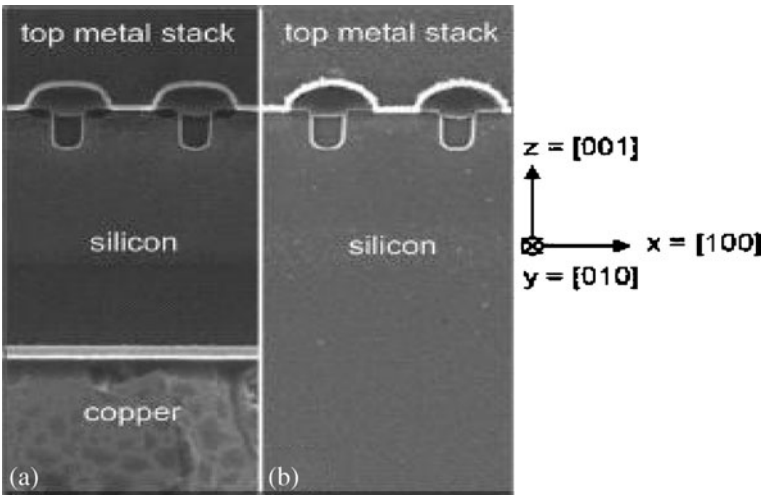


Fig. 3.40 (**a**) Fairchild UMOSFET (**b**) regular MOSFET (© 2009 IEEE [9])

3.6 The Trends of Discrete Power VDMOSFET WL-CSP

3.6.1 Ultrathin Silicon Substrate and Thick Back Metal

To get lower $R_{ds(on)}$ and to improve the thermal performance, the wafer level MOSFET with vertical metal-oxide can be built on a silicon substrate thinned to 7 μm and plated with 50 μm copper as its drain, see ref. [9] Fairchild wafer level UMOSFET. This can extremely reduce the $R_{ds(on)}$ resistance and improves the thermal performance. Figure 3.40 shows the ultrathin device structure of the UMOSFET and its comparison with regular MOSFET.

3.6.2 Move the MOSFET Drain to Front Side

For the wafer level discrete MOSFET, another trend which obtains the attention in the industry is to move the drain of the MOSFET to the front side of the die so that the drain, source and gate are at the same side. This would be helpful for the surface mounting application in various PCBs.

Figure 3.41 shows one of the lateral layouts of the front side drain for a MOSFET WL-CSP. Since the drain is in lateral placement, the back metal does not need to contact the front side drain directly, so its application limits to lower power and lower voltage area. For VDMOS WL-CSP, the trend is to develop the directly connection to the front side by TSV in trench area. The advantage of the direct connection the back drain to front side is its good electrical performance with lower

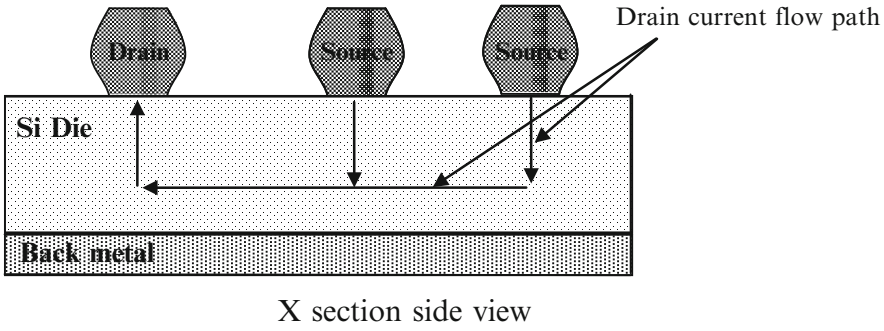


Fig. 3.41 Move the drain to the front side the MOSFET

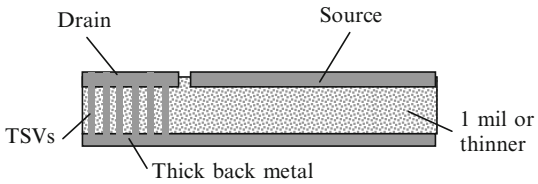


Fig. 3.42 Direct contact back drain discrete power WL-CSP

$R_{ds(on)}$. Because this is a vertical DMOS, the application area may be relatively wider in power range as compared to the structure in Fig. 3.41. Figure 3.42 shows such concepts in discrete power WL-CSP.

3.7 Summary

This chapter starts with an example of discrete TO power package from its design construction, assembly process to the mount process in which the leads forming and the heat sink mounting are discussed in details. Then the trends of using EMC in discrete power device are introduced, which shows two directions: one is the decrease of the using the EMC such as the new generation of SO-8 package with clip and bottom, MOSFET BGA, and power discrete WL-CSP without EMC. The other direction is that the EMC is still not only useful in power discrete package today, but also developing new applications such as the premolded substrate and the wafer level molding for redistribution layout (RDL). Then this chapter discusses the trends of the discrete power package with current carrying capability, low $R_{ds(on)}$, and multiple direction heat transfer designs. As the increasing of current density and the shrinkage of the package for low $R_{ds(on)}$ electrical performance, the ratio of die and package size will significantly increased and the multiple direction heat

dissipation design is a way to improve the thermal performance. After that, three typical discrete power package designs and constructions are presented and discussed. The first design is the SO-8 bond wireless power package with clip to replace the bond wire; the second one is the flip leaded molded package in which the drain of the MOSFET is exposed and locates at the same surface of the leads; the third one is the MOSFET BGA. Following that, a low cost VDMOSFET WL-CSP with Cu stud bumping is introduced with Cu stud bumping design construction and bumping process. Modeling and the experimental tests with different stud bumping parameters and the structures under the top bond metal are conducted and discussed. Finally, the trends of the power discrete power VDMOSFET are discussed.

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Chapter 4
Power IC Package Design and Analysis

The development of the power IC package is a dynamic technology. Power IC Applications that were unattainable only a few years ago are today commonplace thanks in part to advances in electronic package design. From portable applications such as in mobile telecommunications and consumer electronics to aerospace and automotive applications, each imposes its own individual demands on the electronic package. To meet such a diverse range of application requirements, IC package range encompasses over 30 different types, most of which are subdivided into a number of outline versions. The power IC packages offers a high thermal dissipation, enabling power IC usage in some of the most demanding application areas which integrate analog, logic, and power MOSFETs [1, 2].

4.1 The Evolution of the Power IC Technology

In early and middle of 1980s, the power IC technology was developed from vertical diffusion metal-oxide semiconductor (VDMOS) discrete technology and the bipolar IC's technology to the mixed power technology which integrated Bipolar, complementary metal–oxide–semiconductor (COMS) and double-diffused metal–oxide–semiconductor (DMOS) with bipolar based technology (BCD). At that time, the CMOS technology used 2.5 μm, electrically erasable programmable read-only memory (EEPROM) technology used 1.2 μm and the FLASH technology used 0.6 μm. Since 2000, the mixed power technologies have been evolved with CMOS (implantation) based technology. There are three major functions: (1) main stream CMOS compatible with 0.35, 0.18, 0.13 μm and below, (2) module approach for integrating more functions, and (3) capability for many small systems integrated on a single chip (SOC). Figure 4.1 shows the evolution of the power IC technology. Figure 4.2 shows the power IC main strain CMOS implantation based technology and the process module flexibility [3], in which the technology has been designed to be highly module so that mask steps can be added or omitted according to the components required for the ICs design. About 96 power analog components may be

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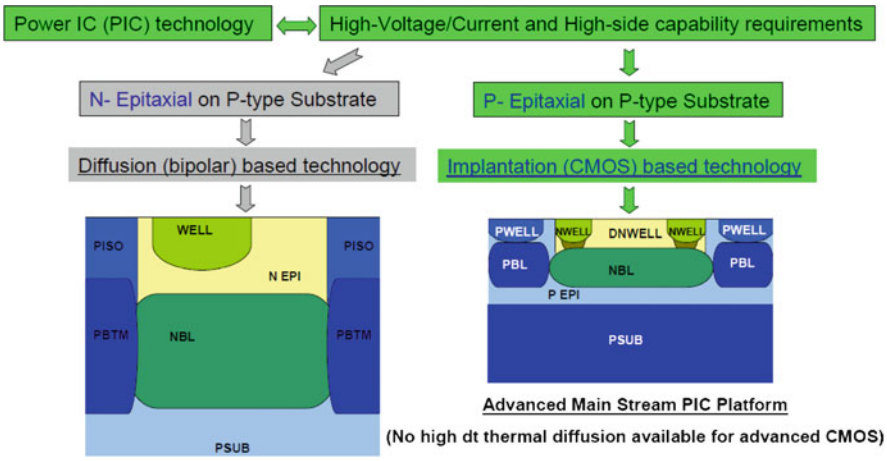


Fig. 4.1 Power IC technology development

integrated into the module. A module route creation system allows more cost-effective process flow for various application needs. The process can be either simplified or differentiated or specialized according to the application requirements. Therefore, it is possible for the modularity power IC technology to generate a large variety of very different power analog ICs for target applications.

It can be seen from Figs. 4.1 and 4.2 that challenges using the advanced main stream CMOS platform are the following: the trend of increment of power density in wafer level that induces the increased Latch-up sensitivity for CMOS, the cross-talking concerns between DMOS to high density logic CMOS and analog blocks, the increased noise (electrical and thermal) isolation between DMOS to high density logic CMOS and analog blocks. Furthermore from Fig. 4.2, we can see that the power IC platform is built with thin p-epitaxial on p type substrate which is the same concept as advanced main stream logic CMOS platform for reduced CMOS latch-up concern. Small isolation tub lateral diffusion due to thin epitaxial for reduced intradevice and interdevice spaces that maximizes power analog and signal path analog shrink. For example, the space is only 2.7 μm between 40 V isolation tub (min. breakdown to sub. 50 V) to another 40, 20 V (min. BV to sub. 35 V), or 5 V (min. BV to sub. 15 V) isolation tub. Devices module in the system can be added or omitted according to the components required for IC design. It is possible for the BCD module technology to generate a large variety of very different ICs, with the best trade-off between functions, performance and cost. This is actually today's concept for smart power IC integration which combines the logic, analog, and power functions. One advantage of the integration power IC is the low power IC parasitic concern. This is because the features of the main stream CMOS based BCD technology have very low minority carrier lifetime (very thin p-epitaxial on p type substrate) plus customized isolation scheme (retarded) E-field in the platform to effectively suppress power stage cross-talking to logic and

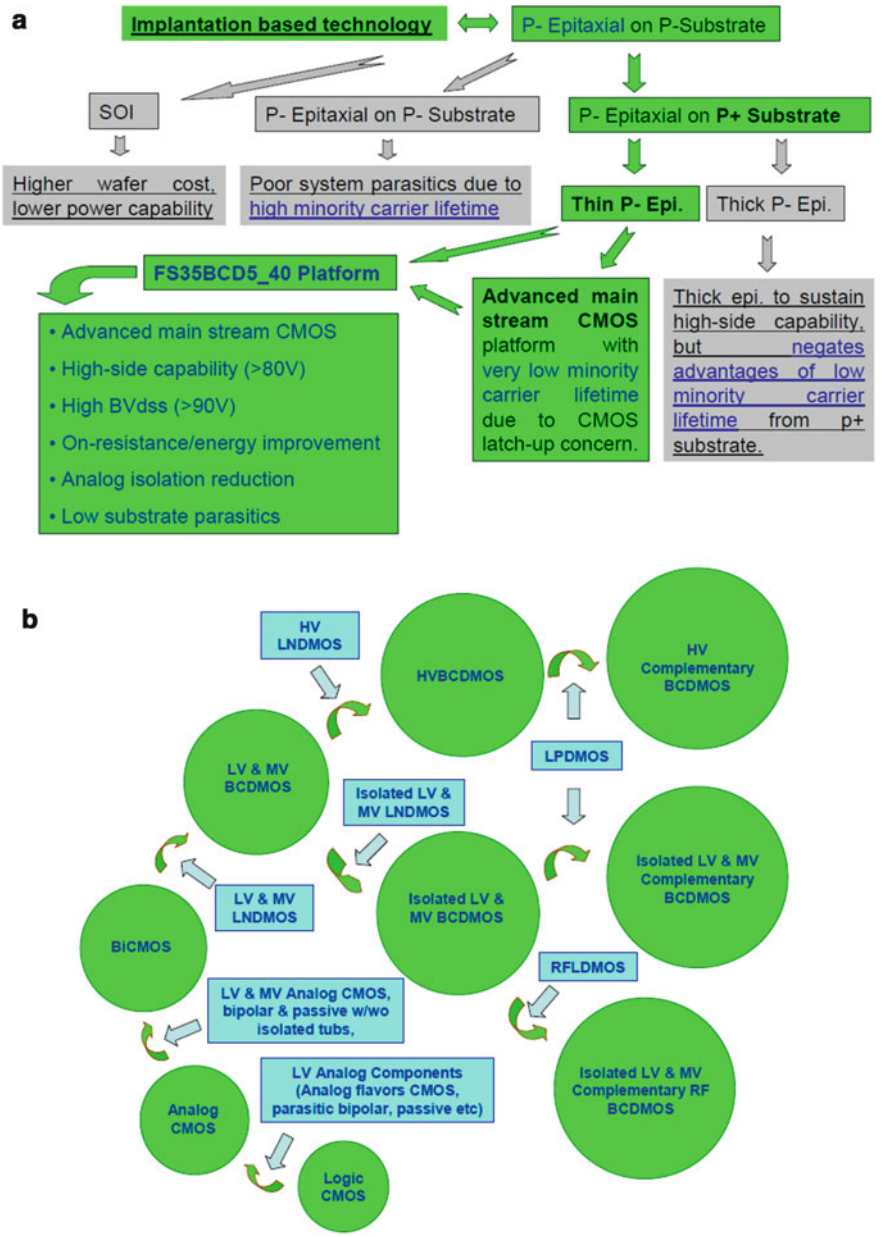


Fig. 4.2 Power IC main strain CMOS implantation based technology. (**a**) Implantation based technology and Fairchild FS35BCD platform, (**b**) process module flexibility (© 2009 IEEE [3])

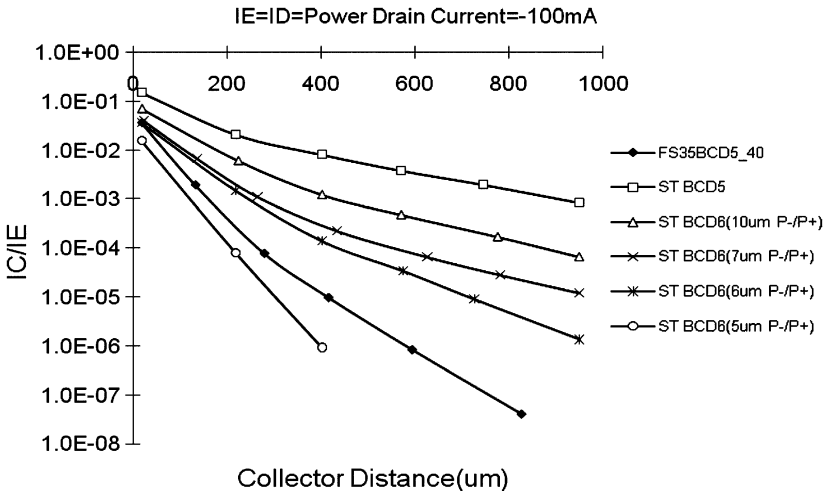


Fig. 4.3 Significant suppression of parasitic NPN (Ic/Ie ~ 0.005 at a distance of 100 μm) by the thin epitaxial on p type substrate (© 2009 IEEE [3])

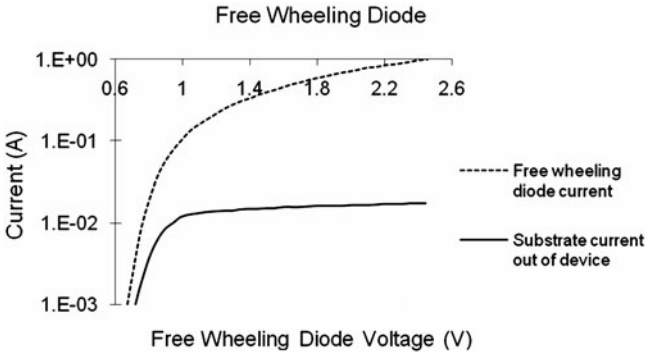


Fig. 4.4 Significant suppression of parasitic PNP (Ic/Ie $<$ 0.02) by a customized retarded E-field built in a isolation scheme (© 2009 IEEE [3])

analog blocks, especially for inductive loads at high current during "dead times." Figures 4.3 and 4.4 show the low parasitics concern of the parasitic npn substrate minority carriers (electrons) suppression by the thin epitaxial on p type substrate and the parasitic pnp substrate majority carriers (holes) suppression by a customized retarded E-field built in a isolation scheme [3].

From the device level, the optimized high voltage retrograde doping profiles for high side capabilities can support 5–40 V rating modular processes with 60 and 80 V rating extensions. Novel isolated architectures (isolated LV/HV MOSFET devices and LV/HV isolation tubs) allows the integration of isolated pockets to realize high voltage functions up to 40/80 V and also for noise isolation, and

eliminated substrate carriers injection. Dual gate oxide architectures are adopted to maintain full compatibility with logic CMOS and the thicker gate oxide is added according to high voltage gate application needed. Multiple thin Al/Cu metal layers for high density interconnections plus an extra thick aluminum power metal with bond pad overlap active (BPOA) for additional high current routing layer can enhance the power capability of devices.

4.2 Higher Power Density at the Die Level

For the voltage range at 5–100 V, there are a wider range of inductive loads handled with a monolithic solution and higher level of functional integration in monolithic solution. One direction of the fast growing electronic system market is requiring multimedia capability, portability, and connectivity. The major function of the multimedia capability is the video capability, in which the color displays driving architecture requires high voltages. The portability will increase the battery life time and reduce the power consumption. The connectivity stands for the high frequency capability in wireless and RF application. This increases the demands on power dissipation with low Ron power devices, high density and integrated power, which means that the power density increases greatly and hence power dissipation is confined to less available spreading which makes the localized temperature increase faster. Because of this, the p type substrate is used to reduce the specific resistance of substrate for both electrical and thermal problems. The power dissipation can be further reduced blocking as much as possible by heavily adopting the doped p type substrate and by using highly conductive die attach material from the chip to the pad of the package, the same as in regular discrete power devices. The thick metal with bond pad over active circuit design can easily integrate wafer level chip scale packaging (WLCSP) in which the high density features offers a great contribution in die size reduction for power ICs. This indicates that the power IC integration today has made the high power density at the die level. It can drive complicated loads with the BCD technology that adopts process architectures very similar to the main stream CMOS technology and with a powerful packaging which can effectively take the heat from the chip and keep the excellent electrical performance. Figure 4.5 shows the devices for the possible basic target functional block/module in a high density power IC die.

The target functional blocks of power IC are defined to condition and to convert analog inputs, to transfer the digital output into analog signals that drive actuators. These basic power IC blocks can generate the power IC system on chips (SOCs), which include the following: (1) regulated internal supply with bipolar/diodes, LV/HV CMOS, capacitors, resistors, and isolation tubs, (2) voltage references with isolated LV CMOS and isolated bipolar with analog flavors, resistors, caps, and fuses with isolated tubs, (3) operational amplifiers with LV/HV with and without isolated CMOS with analog flavors, capacitors, resistor, low R_{dson} output

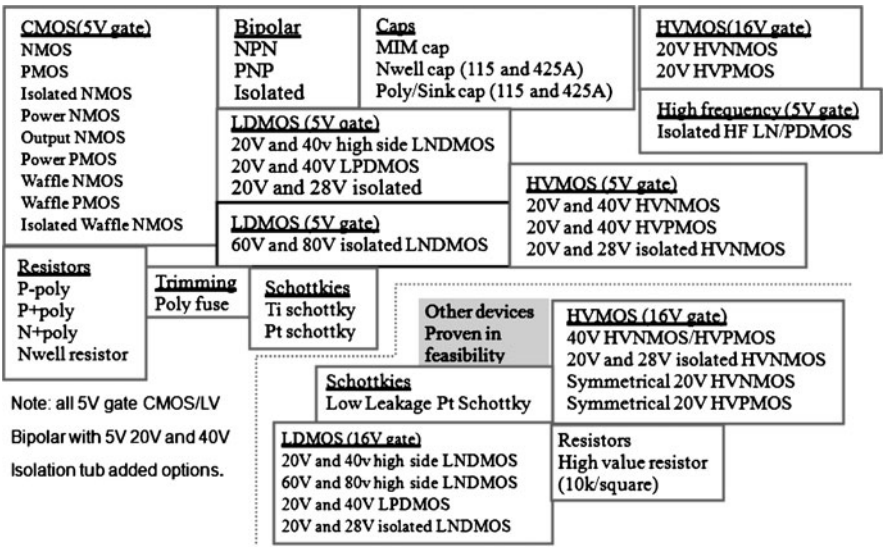


Fig. 4.5 Devices set for target functional blocks

transistors, and isolated tubs, (4) current sensing with scalable LV/HV CMOS, power FET and matched mirror device, and caps, (5) digital control with main stream CMOS code, caps, and isolated CMOS, (6) drivers with square electrical SOA LDMOS, isolated power CMOS/LDMOS for noise isolation, low switching losses or HV level shifts in H-drivers, and LV/HV CMOS, (7) power FET (power CMOS and LDMOS) with matched mirror device, isolated power CMOS/LDMOS when driving inductive loads at high current, the state-of-the-art low R_{dson} LD MOS devices, customized isolated schemes.

Because the multiple functions are built on a chip together with the trend of die shrinkage, the power density is very high at the die level. The heat transfer for the power IC is a challenge for the high power density design. The packaging layout and design will extremely help and benefit the heat dissipation of the high density power IC die. For a long time, the power IC uses the matured packages, such as the TSSOP, QSOP, SSOP, SOIC, MDIP, SC etc. As the power IC technology develops, the power density increases and the die size shrinks. Packages such as MLP, thin MLP, premolded and MicroPak MLP, WLCSP, QFN, dual row MLP are widely used today for the power IC products. To fit the high power density such as the smart power IC system on chip with multiple functions which integrate logic, analog, and power technologies, the next-generation packages such as ultrathin MLP package (uMLP), molded flip chip scale package (MCSP), flip chip BGA, chip-on-lead MLP, flip chip MLP, micromodule and microarray MLP will be developed.

Figure 4.6 shows the possible application regions and mapping various packages for power IC products. The compact end use products require ever thinner solutions, moving the bar from 0.75 to 0.55 to 0.4 mm and less. For WLCSP, this

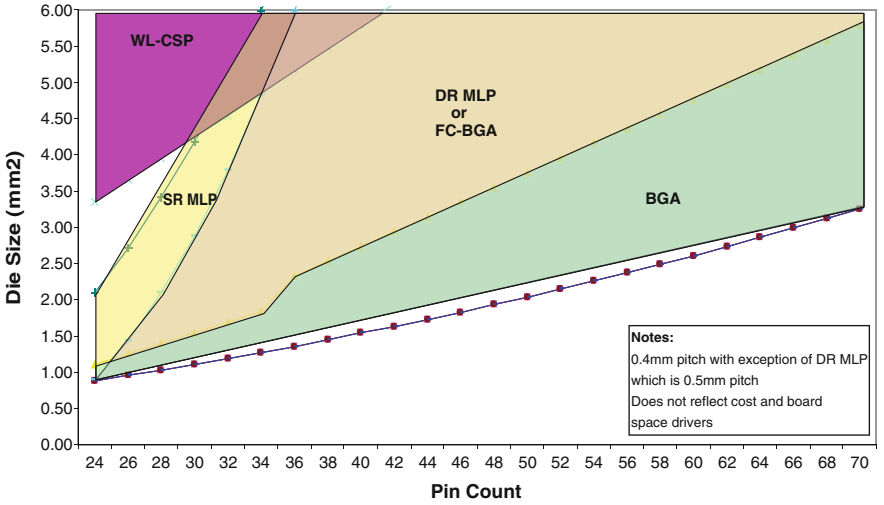


Fig. 4.6 The possible application mapping/region of the power IC packages [2]

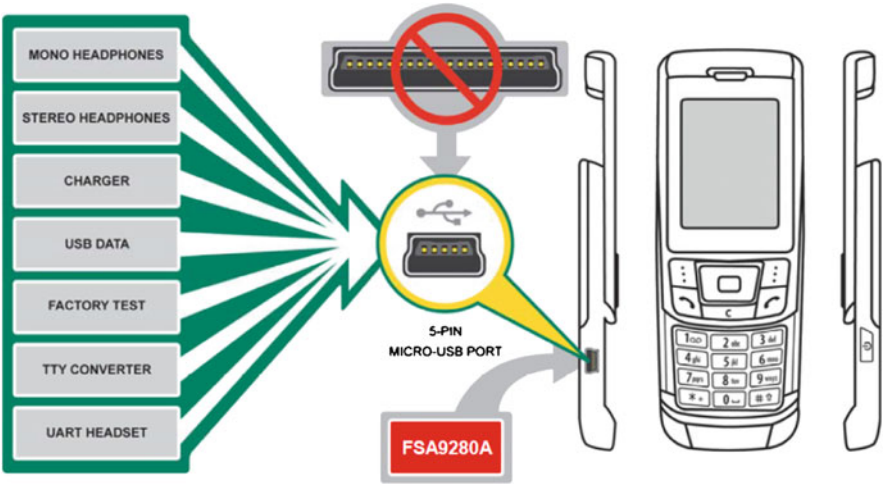


Fig. 4.7 Fairchild power IC product FSA9280A in multimedia switch USB

forces the use of thinner silicon and smaller solder balls. This can drive a move away from the conventional solder ball approach to a bumped die approach.

Figure 4.7 shows an application of a Fairchild power IC product FSA9280A in multimedia switch for mobile phones and portable media players [4]. Figure 4.8 shows the circuitry of the power IC product. The FSA9280A is a high-performance multimedia switch featuring automatic switching and accessory detection for

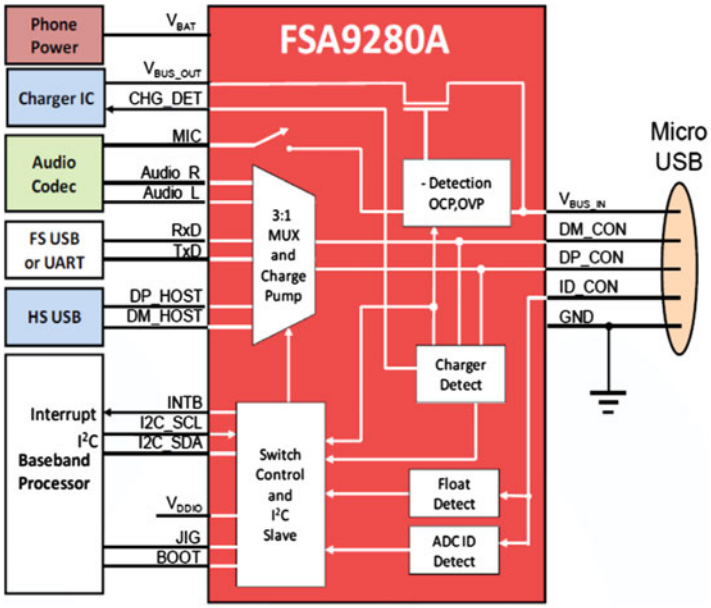


Fig. 4.8 The circuitry of the FSA9280A

the USB port which allows the sharing of a common USB port to pass audio, USB data/charging, as well as factory programmability. In addition, it integrates detection of accessories, such as headphones, headsets (MIC/button), car chargers, USB chargers, and UART data cable with the ability to use a common USB connector. The FSA9280A includes an integrated 28 V overvoltage and 1.5 A overcurrent protected FET. To better dissipate the heat, the package selected for this product is uMLP with 20 leads. This package has a large metal die attach pad which allows the good heat dissipation. Figure 4.9 shows the foot print layout of the 20L uMLP. Figure 4.10 gives the package design construction of the 20L uMLP. Figure 4.11 shows the wire bonding diagram of the package. The package design construction includes the leads, die attach pad, die attach epoxy, power IC die (FSA9280A), bond wires, and epoxy mold compound. The total package thickness is 0.55 mm, and its size is 3×4 mm^2 with the pitch 0.5 mm.

Figure 4.12 shows the thermal modeling result of the temperature distributions for the power product FSA9280A with 20L uMLP package mounted on a 1s0p JEDEC board with 1.0 W power dissipation, the max temperature on die is 196°C. Table 4.1 lists the thermal comparison of junction temperature and thermal resistance with different power dissipations and different die attach thermal conductivities under different JEDEC board layouts for the product FSA9280A. The maximum thermal resistance of junction to ambient (θ_{Ja}) is about 178°C/W with 1s0p JEDEC board. The result shows that the different power dissipation will not significantly impact the thermal resistance of junction to ambient, while the thermal conductivity of the die attach material has some marginal effect on the

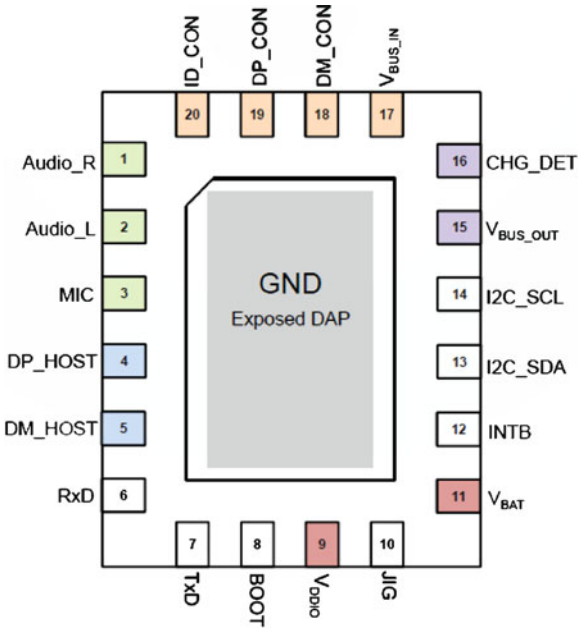


Fig. 4.9 The foot print of the uMLP 20L package for FSA9280A

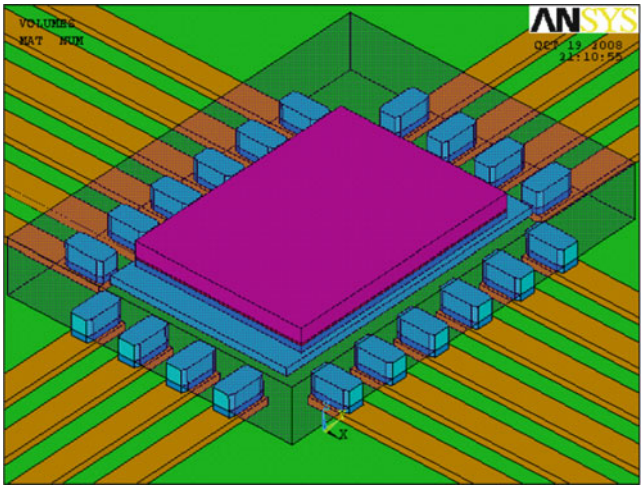


Fig. 4.10 The construction of uMLP20 package

thermal resistance (only 7.24°C/W difference). The layout of PCB has significant impact on the thermal resistance. From the Table 4.1, it can be seen that the thermal resistance of the 20L uMLP with 2s2p board is about 62°C/W less than the case with 1s0p board. For high power density product at die level, 2s2p board is an effective method to dissipate the heat.

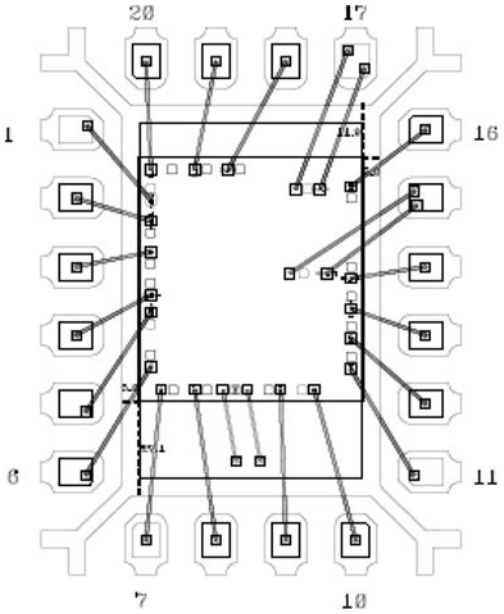


Fig. 4.11 The wire bonding diagram of 20L uMLP with FSA9280A die

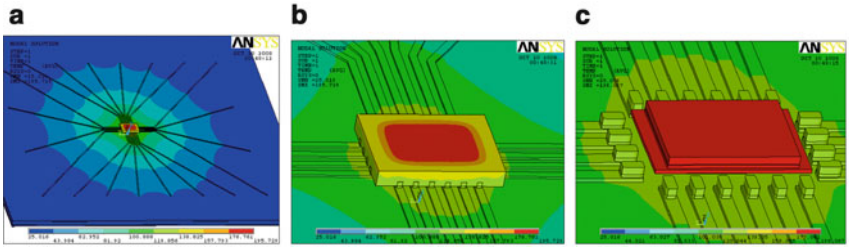


Fig. 4.12 The temperature distribution of the power product FSA9280A with 20L uMLP package mounted on a 1s0p JEDE PCB (with 1.0 W power dissipation). (**a**) Board level temperature distribution, (**b**) local temperature, (**c**) maximum temperature on die (196°C)

One typical and simple power IC application is the wafer level integrated system power conversion solution which combines two power switches (the high side and lower side) together with an IC driver [5]. Figure 4.13 shows an example of such a wafer level power system on chip. There are also integrated advanced digital control functions for motion which includes "sensorless" positioning and fault detection at the low end and "adaptive" motion control at the high end. For the voltage range at 100–700 V, next generation of integrated LDMOS structures reach the limits of Si for breakdown voltage (BVdss) as a function of geometry, which allows a corresponding increase in HV monolithic power conversion capability (AC-DC) and results in an incremental raising of the limit at which multiple die are requested in the actual products.

Table 4.1 The thermal comparison with different power dissipations and different die attach conductivities under different JEDEC boards for 20L uMLP with FSA9280A die

		Die attach with thermal conductivity 11 W/mK		Die attach with thermal conductivity 0.23 W/mK		
JEDEC board type (no vias)	Power dissipation (W)	Junction temperature (°C)	θ_{Ja} (°C/W)	Junction temperature (°C)	θ_{Ja} (°C/W)	$\Delta\theta_{Ja}$ of different die attaches (°C/W)
1s0p	1	196.067	171.067	203.302	178.302	7.23
	0.1	42.107	171.07	42.83	178.3	
1s2p	1	136.461	111.461	143.696	118.696	7.24
	0.1	36.146	111.46	36.87	118.7	
2s2p	1	134.07	109.07	141.306	116.306	7.24
	0.1	35.907	109.07	36.631	116.31	

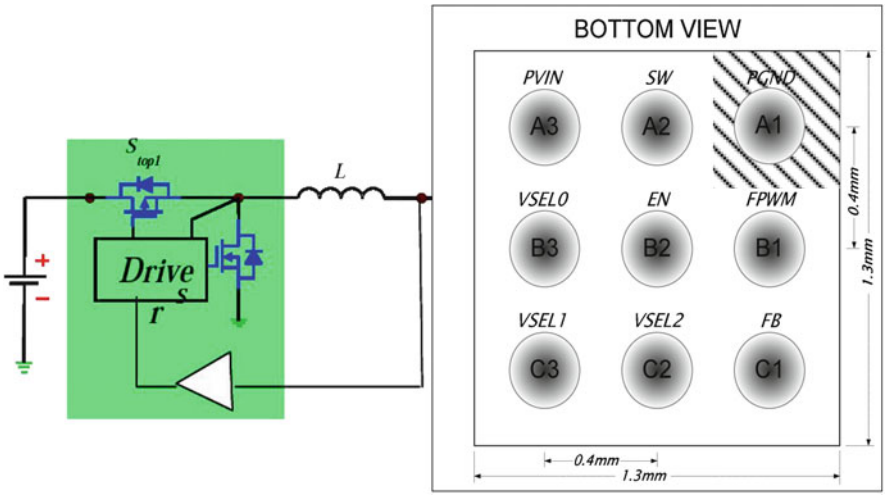


Fig. 4.13 Wafer level integrated power solution

4.3 Smaller Package Footprints

As the power IC die shrinks, the package footprints become small. This results in the high power density and high heat generation in a power IC die. How to effectively dissipate the heat from the power IC die becomes a challenge. Integrating the heat sink or heat transfer coupling apparatus into a molded package remains a key feature for shrinking footprints. Figure 4.14 shows the smaller footprint molded package with exposed metals for integrating heat sink or directly attach Board/system [1].

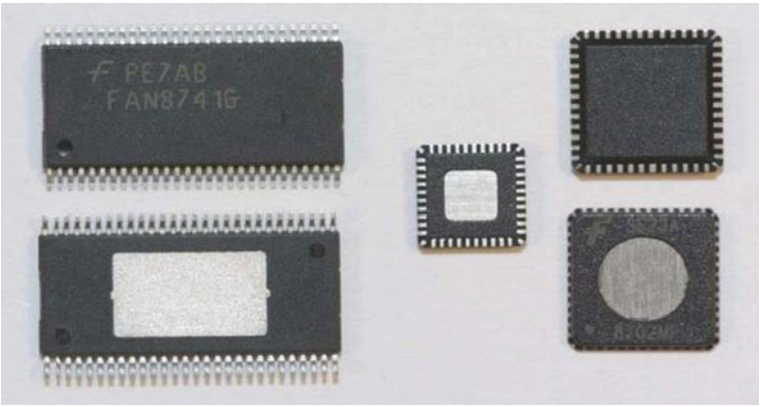


Fig. 4.14 Molded packages with exposed metals

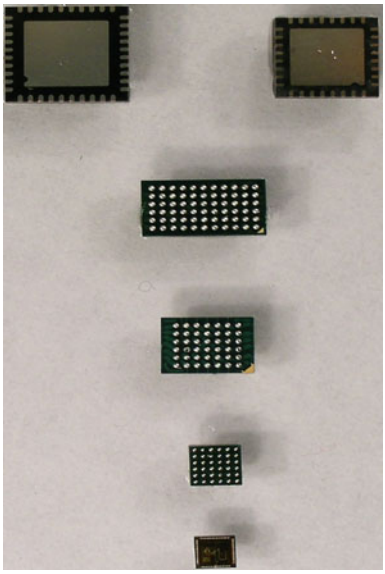


Fig. 4.15 Evolution of the power IC packages [2]

The high power density is the drive to small form factor of power IC package, eventually leads the power IC package from QFN/MLP, BGA to move to small pitch WL-CSP. Figure 4.15 shows such evolution trends of power IC packages. These array packages are also following similar trends in pitch reduction.

Table 4.2 lists the trends of smaller power IC package and footprints in today and future needs. It shows the package development and roadmap in thickness and foot pitch.

Table 4.2 Trends of smaller power IC package and footprints [2]

	Package thickness	Mounting	Testability	Environmental	Pitch
Today	1.0 mm (BGA and MLP) 0.45 mm (WL-CSP)	MLP and WL-CSP packages are mountable on flex and thin PCB. BGA is not	Multiple insertions Package related yield issues	ROHS but not Green	0.5 mm with 0.4 mm in development
Future needs	0.8 mm needed now with roadmap to 0.6 mm and beyond	BGA package is not mountable on flex and ultrathin PCB	Package needs to allow reduced test insertions and high throughput	Must be Green compliant ("Green" definition evolves)	0.4 mm now with roadmap to 0.3 mm

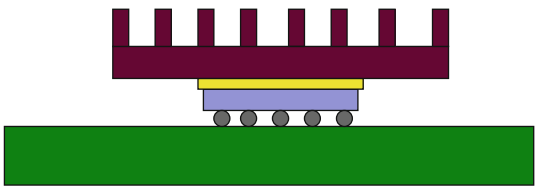


Fig. 4.16 Example of WL-CSP which is hard to mount the heat sink on its back side

As power IC die size and thickness shrink, the package footprints shrink as well, and maintaining the thermal transfer capacity at the package level is difficult since the function/unit area of die is increasing with advanced BCDMOS processes. While the overall package footprint trend is decreasing, the thermal dissipation capabilities rely more on the PCB as part of the system. Therefore insuring mechanical integrity of WL-CSP in the form of bare flipped die in conjunction with board level assembly of a heat sink is difficult, see Fig. 4.16.

Figure 4.17 shows a construction of a molded flip chip package (MCSP) which includes a fine pitch flip chip die which is bonded to the substrate with gold to gold interconnection (GGI), a PCB substrate with copper trace as the redistribution layer (RDL) and vias, the mold cap with epoxy mold compound to encapsulate the flip chip and the PCB substrate, and the solder bumps for connecting the MCSP to outside world. This is a typical application of a power IC shrink die with small pitch to connect to a PCB substrate with larger pitch for pin out. Its heat dissipation capability majorly relies on the PCB substrate to transfer to the board. Figure 4.18 shows the design layout of the MCSP with 16 pins and the 3D top view as well as the internal view. The smallest pitch in die is about 0.2 mm. The pitch of solder balls on substrate is 0.5 mm. The following thermal simulation gives the example of how the heat dissipation of the power IC flip chip die replies on the board layout and

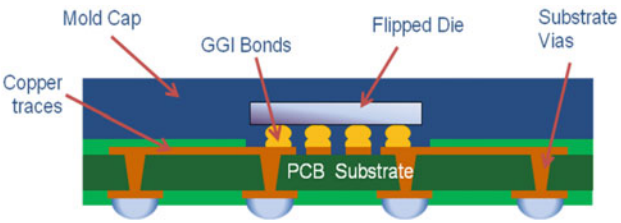


Fig. 4.17 Construction of MCSP with fine pitch flip die and PCB as the RDL and heat dissipation

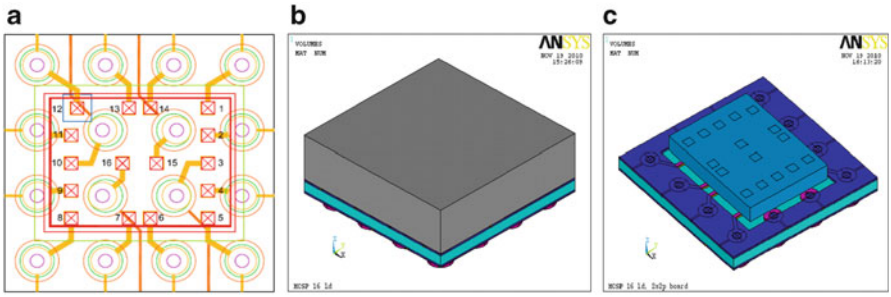


Fig. 4.18 The model of a 16 pin MCSP. (**a**) The layout of die and trace RDL, (**b**) *top* view, (**c**) the flip chip attached on the substrate

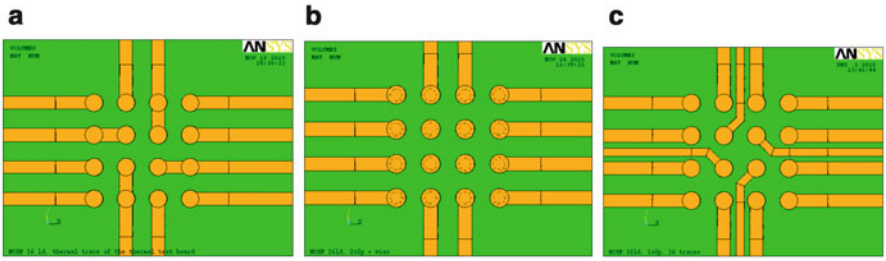


Fig. 4.19 The PCB layout with different trace designs based on JEDEC standard 51-9. (**a**) Trace (1), (**b**) Trace (2), (**c**) Trace (3)

trace design. Figure 4.19 shows the three different trace designs for the boards based on JEDEC standard 51-9.

Figure 4.20 shows the thermal simulation result for the 16 lead MCSP which is mounted on a 1s0p JEDEC board. The Fig. 4.20a shows the temperature distribution of the MCSP and the JEDEC board; Figure 4.20b shows the temperature of the local area of flip chip and the substrate on the JEDEC board in which the maximum junction temperature is 259.1°C; Figure 4.20c shows the temperature distribution on the MCSP only. Table 4.3 gives the thermal resistance (junction to ambient, θ_{Ja}, junction to the package top Ψ_{Jt}, and junction to the board Ψ_{Jb}) comparison of different trace designs and different JEDEC boards. From the Table 4.3 it can be

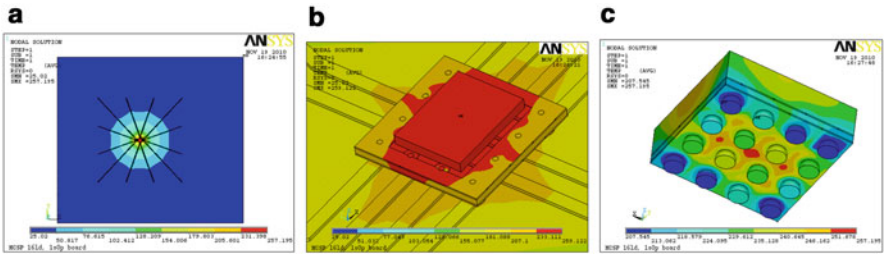


Fig. 4.20 The temperature distribution for the MCSP mounted on a 1s0p JEDEC board with trace design (1) and 1 W power dissipation (the maximum temperature is about 259.1°C). (**a**) MCSP on board with trace, (**b**) the junction temperature on flip chip, (**c**) the temperature of MCSP

Table 4.3 The thermal resistances of different PCB layouts and trace designs with 1 W power dissipation

Trace design	Thermal board	Junction temperature T_j (°C)	Package top max temp T_t (°C)	Test board max temp T_b (°C)	θ_{Ja} (W/°C)	Ψ_{Jt} (W/°C)	Ψ_{Jb} (W/°C)
(1)	1s0p	259.1	257.2	237.6	234.1	1.9	21.5
	2s2p + vias	92.9	91.7	62.8	67.9	1.2	30.1
(2)	1s0p	269.2	266.9	260.9	244.2	2.3	8.3
	2s2p + vias	93.4	92.2	64.6	68.4	1.2	28.8
(3)	1s0p	238.7	236.8	218.5	213.7	1.9	20.2
	2s2p + vias	92.4	91.1	62.8	67.4	1.3	29.6

seen that the board layout and trace design can significant impact the thermal resistances. Trace design (3) has the smallest the thermal resistance of junction to ambient which may effectively dissipate the heat from the flip chip die.

4.4 Typical Package Design and Analysis for Power IC

As we know today most common packages that may be used for power IC and signal path controller are lead frame based packaging such as MLP (or QFN) and Dual row MLP, substrate based packaging, such as the MicroPak™ package with premolded substrate or laminate substrate, and the WLCSP. This section introduces the basic design and construction of the MLP package first, followed by the substrate based MicroPak MLP as well as the WLCSP for IntelliMAX™ power IC product.

4.4.1 MLP Design and Construction

Figure 4.21 shows the construction of a typical MLP package. The package consists of lead frame with exposed die attach pad, epoxy die attach material, power IC die,

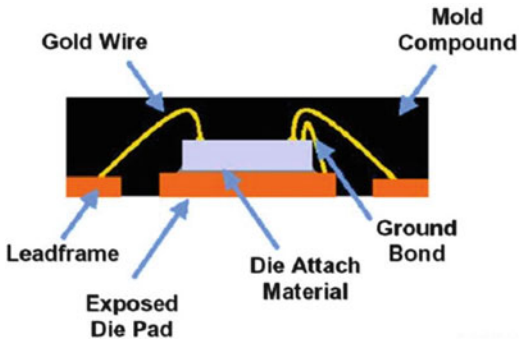


Fig. 4.21 The construction of a typical MLP package

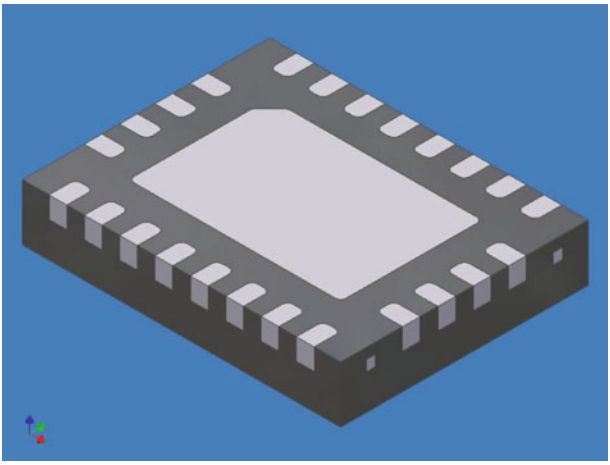


Fig. 4.22 The 3D view of a 24L MLP package

bond wire (typically gold or copper wire) and mold compound. Since the power IC die is attached on the metal pad directly, it can effectively dissipate the heat from the high density power die.

Figure 4.22 shows the 3D review of a typical 24 leads MLP package. Figures 4.23 and 4.24 show the lead frame design for the MLP package with tie bar that connects to the die attach pad and the strip design for a whole panel lead frame. The basic assembly process step for a MLP package includes die sorting and pickup, die attaching with epoxy resin material, wire bonding process, molding with epoxy molding compound over the whole panel, postmold cure, laser mark, plating and singulation normally by saw, electrical testing, tape and reel.

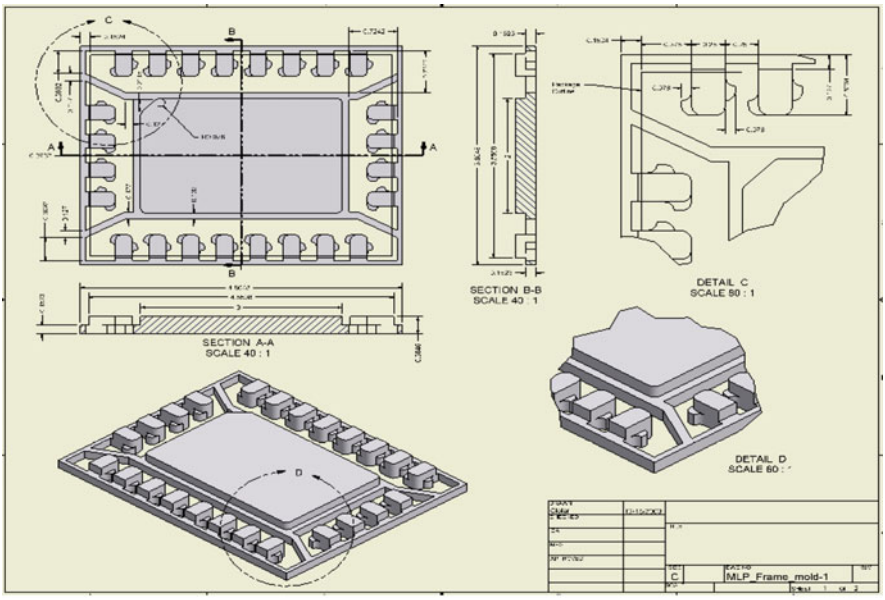


Fig. 4.23 The lead frame design of MLP

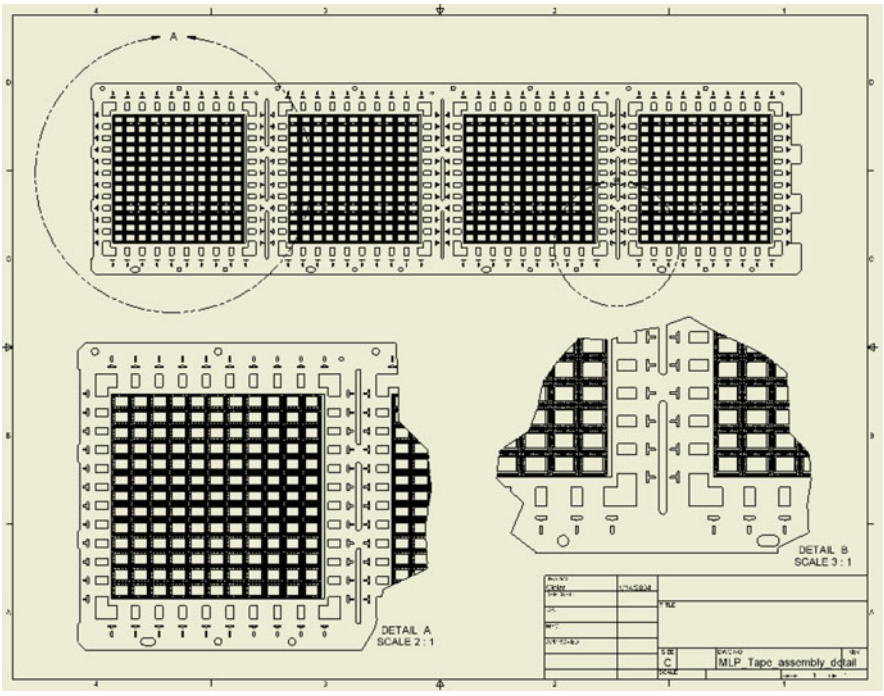


Fig. 4.24 Lead frame panel design

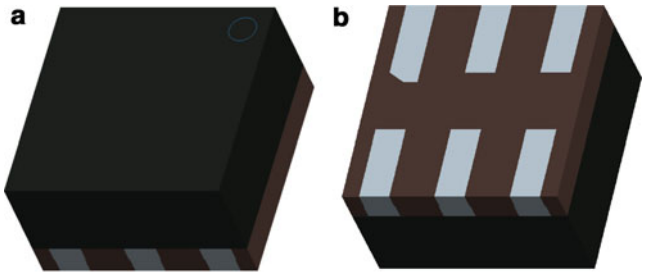


Fig. 4.25 The six leads package MicroPak MLP. (**a**) *Top* view, (**b**) *bottom* view

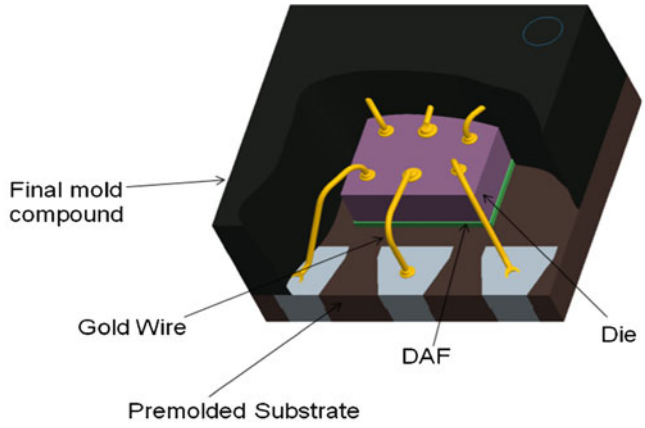


Fig. 4.26 The construction of the six lead MicroPak with premolded substrate

4.4.2 Design and Thermal Analysis of Premolded MicroPak MLP

To save the cost for a low voltage power IC application, a premolded lead frame substrate based MLP is developed for MicroPak packaging. This design usually has potential benefits for low power die and is very small size package about $1.0 \times 1.45\ mm^2$, and its thickness is about 0.5 mm. Figure 4.25 has shown such a package concept. Figure 4.26 shows the design construction of the premolded MicroPak MLP. It consists of a premolded substrate with leads, die attach film (DAF), die, the bond wire, and the final molding compound. The difference between the premolded MicroPak MLP and the regular MLP is the premolded MicroPak MLP design removes the die attach pad due to the small size and low power dissipation in die. Most of the heat is dissipated through the metal leads and the mold compound.

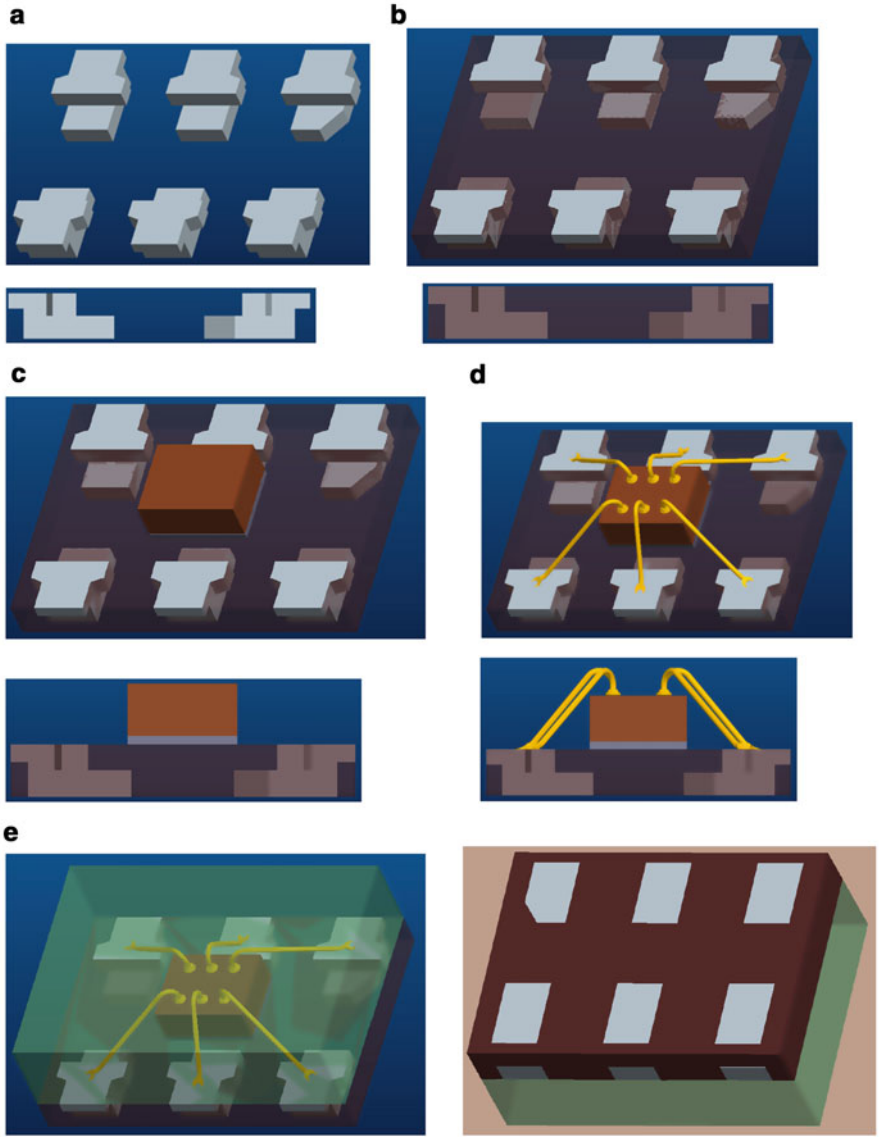


Fig. 4.27 The assembly process of the premolded MicroPak MLP. (**a**) Lead frame design. (**b**) Premolded lead frame. (**c**) Die attach with DAF. (**d**) Wire bonding. (**e**) Final overmolding and singulation. The *left* is *top* view and *right* is *bottom* view

Figure 4.27 shows the major assembly process steps for the premold MicroPak MLP, which includes (1) lead frame design without the die attach dap, (2) molding of the lead frame to form the premolded substrate, (3) attaching the die on the premolded substrate with DAF, (4) wire bonding, (5) final overmolding of the panel

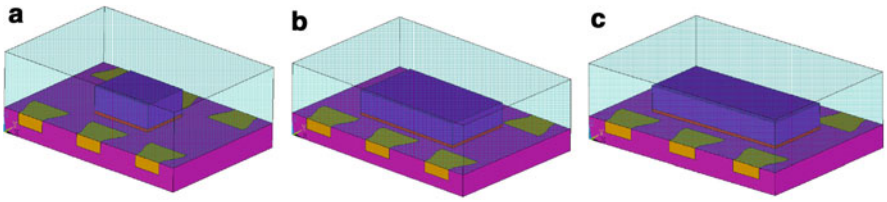


Fig. 4.28 MicroPak MLP with three different die sizes. (**a**) Die size: 350 × 450 μm^2, (**b**) die size: 460 × 780 μm^2, (**c**) die size: 410 × 960 μm^2

Table 4.4 The thermal resistance of junction to ambient with different die size for the six leads MicroPak MLP

		Thermal resistance θ_{Ja} (°C/W)
JEDEC board	Die size of MicroPakMLP	FR4: 0.4 W/mK
1s2p	0.96 × 0.41 × 0.1524	323.2
1s0p		471.9
1s2p	0.78 × 0.46 × 0.1524	336.1
1s0p		484.9
1s2p	0.45 × 0.35 × 0.1524	511.2
1s0p		660.5

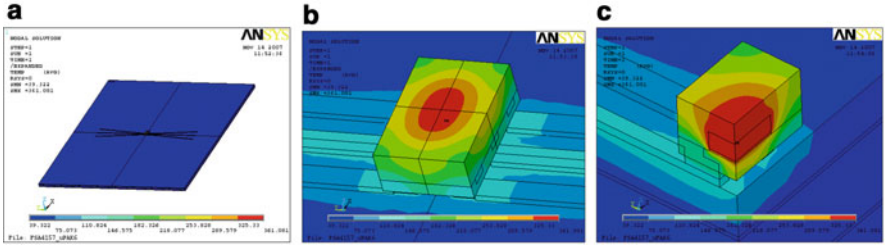


Fig. 4.29 The temperature distribution of the six leads MicroPak MLP with 1s2p JEDEC board (no vias), the maximum temperature is 361°C with 1 W power dissipation on die. (**a**) PCB and trace, (**b**) full model, (**c**) quarter model

strip of the premold substrate with power IC die and singulating the final molded panel package with saw. Figure 4.28 shows three different die sizes of a typical MicroPak MLP with its outline dimension 1 × 1.45 × 0.55 mm^3. Figure 4.28 shows the temperature distribution of a six leads MicroPak MLP which mountes on a JEDEC 2s1p board without vias. The maximum junction temperature is 360°C with 1 W power dissipation on die. Table 4.4 shows the comparison of thermal resistance of junction to the ambient with three die sizes and two JEDEC boards 1s0p and 1s2p. The results tell us that the larger die can effectivly dissipate the heat from the die level to the board. The board layout has also significantly impact on the thermal resistance of junction to the ambient. Higher effective board such as 1s2p definitely helps to take the heat out of the power IC chip (Fig. 4.29).

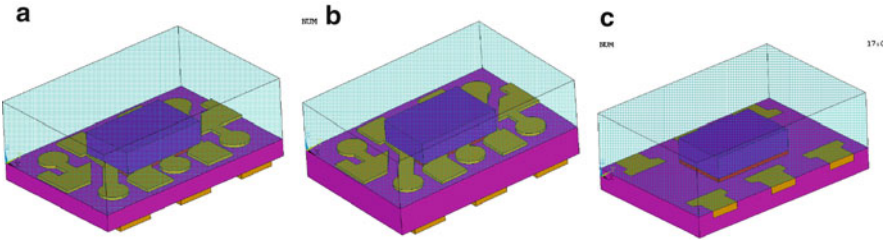


Fig. 4.30 MicroPak package with BT, ceramic, and premolded substrates, its outline dimension is $1 \times 1.5 \times 0.55$ mm^3 (**a**) BT substrate (0.12 mm), (**b**) ceramic substrate (0.2 mm), (**c**) premold substrate (0.15 mm)

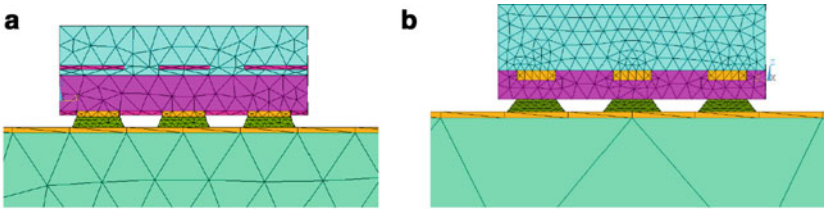


Fig. 4.31 The finite ekement models mounted on a TMCL board for the Micrpak package with BT, ceramic, and premolded substrates. (**a**) MicroPak with BT or Ceramic substrate, (**b**) MicroPak with premold substrate

4.4.3 Package Substrate Design for Reliability

The substrate design and material selection are very important to keep the robust reliability of package. This section takes the substrate design of the Fairchild MicroPak as the example. The substrate design could be selected with ceramics, BT material, and premolded lead frame substrate. Ceramic substrates have excellent thermal conductivity, but its manufacture and solder joint reliability could be challenges because of the ceramic material. BT is a substrate which is popular in the industry and the premold lead frame substrate for MicroPak MLP is the low cost and easy to manufacture. This section tries to compare the three substrate design and their impact on the thermal cycling solder joint reliability. Figure 4.30 shows the designs of a MicroPak package with three substratses. Figure 4.31 shows the finite element models of the MicroPak mounted on a thermal cycling board with BT, ceramic, and premolded substrates.

Figure 4.32 shows that the plastic energy density of solder joint with ceramic is much higher than the premolded substrate due to the largest stiffness of the ceramic material while the BT substrate got the smallest. Table 4.5 compares the solder joint lives of the MicroPak package with ceramic, BT, and premolded substrates. The results show that the solder joint life with BT substrate is the longest; follows by premolded substrate, the shortest case is the MicroPak package

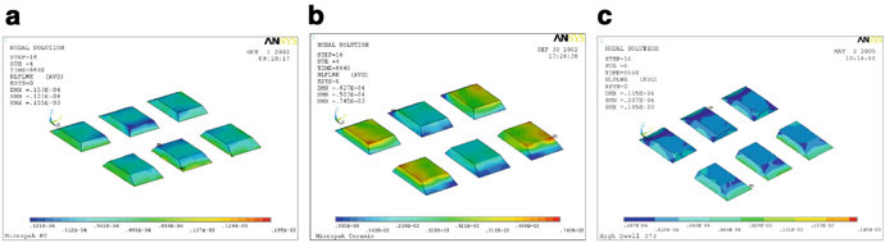


Fig. 4.32 The plastic energy densities at solder joints for the three substrates. (**a**) BT max 0.15 MPa, (**b**) ceramic max 0.745 MPa, (**c**) premold max 0.185 MPa

Table 4.5 The solder joint life compariosn with different substrate design for MicroPak package under TMCL (0–100°C)

Substrate type	First fail	Characteristic life
Ceramic	1,615	2,626
BT	20,348	33,092
Premold	17,486	28,439

with ceramic substrate, which is about 10 times short than the MicroPak MLP with premolded substrate. Therefore, in design of the MicroPak package, to select the ceramic substrate will have excellent thermal dissipation performance but will induce the larger solder joint plastic density energy and the shortest solder joint life. MicroPak package design with BT and premolded substrates have the robust solder joint reliability and with low cost.

4.4.4 Challenges in Wire Bonding Process for Package with Laminate Substrate

It is known that, wire bonding is a complicated, multiple physical transient dynamic process and is completed within a very short time. There are challenges of the wire bonding process on a laminate substrate, since the modulus of the laminate material is much lower than the silicon and metal. The dynamic impact of wire bonding to both devices and the dynamic substrate is critical and significant for the quality and reliability of the product. This section will evaluate the wire bonding process on a laminate substrate by use of both modeling and experimentation [6]. Different values of out of plane modulus of laminate material are studied to understand their impact on the wire bonding quality. Different wire bonding forces are studied and discussed for the effects of the bonding process on laminate substrate structures with partial supports.

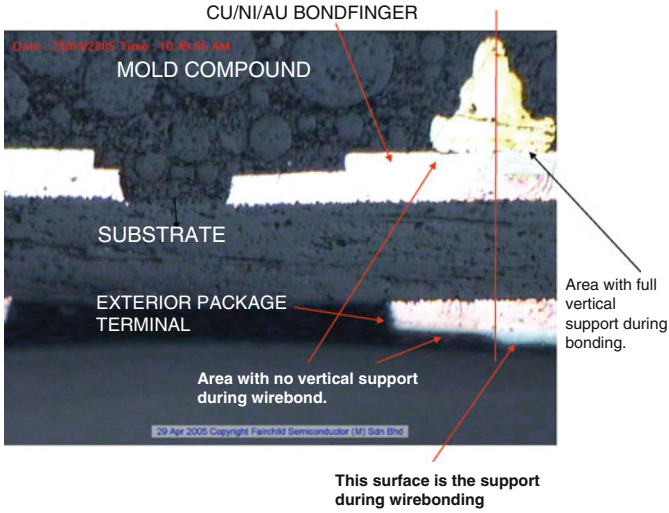


Fig. 4.33 Bond pad structure and laminate of a BSOB system with partial support at bottom

The basic bond pad structure of the laminate substrate, shown in Fig. 4.33, is created using Cu, Ni and Au layers plated onto the laminate material. The wire bonding area is located near the via, which is also very close to the edge of the die. Furthermore, due to the substrate design the bottom is only partially supported. This increases the difficulty of the wire bonding.

The results of different wire bonding forces are showed in Figs. 4.34–4.37. These results are obtained with a fixed ultrasonic frequency 128 KHz.

Figure 4.34 provides the von Mises stress and shear stress distribution on the contact layer of ball and bond pad. Figure 4.35 indicates the friction stress distribution on the ball and bond pad surface. 45% stress imbalance is found between left and right sides. Figure 4.36 illustrates the bond tilt profile. Due to the imbalance of stresses, it is very likely to induce the partial bonding seen on the right hand side (see Fig. 4.34).

In order to examine the stress balance and the bond pad tilt during the wire bonding process, different wire bonding forces are applied to the model. Figure 4.37 gives the stress imbalance on bond pad varies with wire bonding force. In the ideal case the imbalance is 0%, then the two sides of the bondpad get the same stress level. From Fig. 4.37, it can be seen that for von Mises stress as the wire bonding force increases, its imbalance is reduced. When the wire bonding force is higher than 1,000 mN, the stress on right hand side of bond pad became bigger. However, if the wire bond force is too big, the wire bonding will be overloaded which will reduce bonding quality. As we have seen from the Fig. 4.37 the left side has been overstressed, resulting in the stress balance becoming negative when the wire bonding force exceeds 1,000 mN. Therefore if we control the wire bonding force so that it cannot overstress the bond pad, we can reduce the stress balance as much as possible.

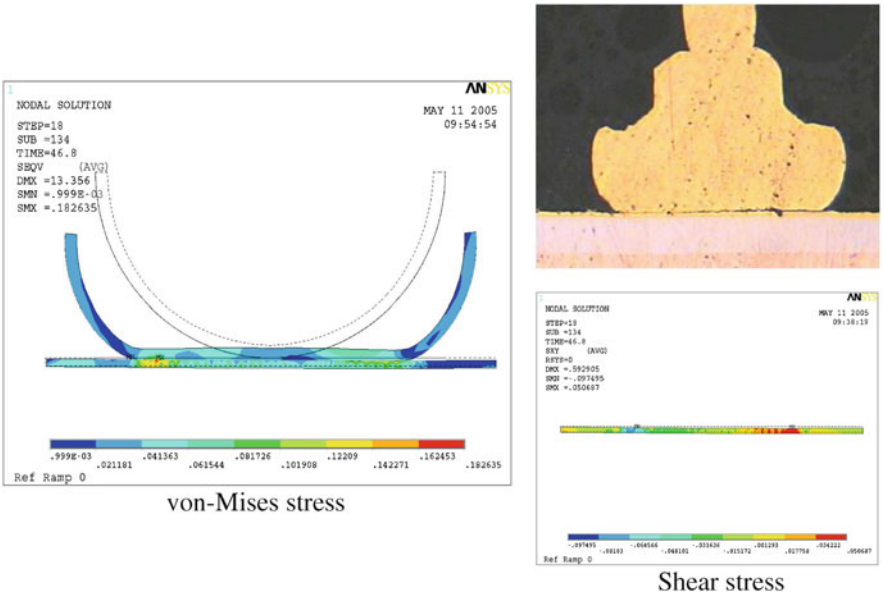


Fig. 4.34 von Mises stress and shear stress at the interface layers under partial left support. Bonding force: 650 mN

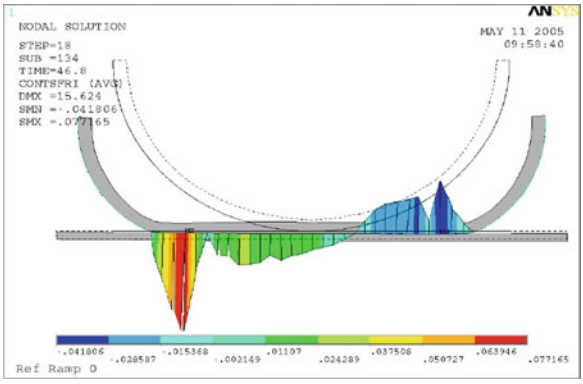


Fig. 4.35 Friction stress distribution. *Left side* is about 45% greater than *right side* with bonding force 650 mN

The laminate material in the MicroPak package is considered to be an orthotropic elastic material. The out of plane modulus is very important to the bondpad tilt. Figure 4.38 shows that as the out of plane modulus of the laminate increases, the bond pad tilt decreases. This indicates that higher out of plane modulus of laminate is helpful to optimize the wire bonding process on laminate substrate.

Figure 4.39 has shown that the capillary print mark on bond pad with two different wire bonding forces. It clearly shows that with smaller wire bonding

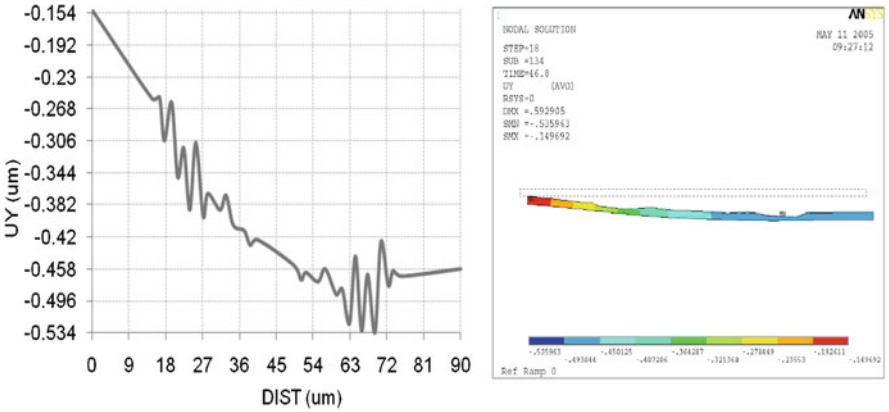


Fig. 4.36 Bond pad tilt during wire bonding under partial left side support. Bonding force: 650 mN

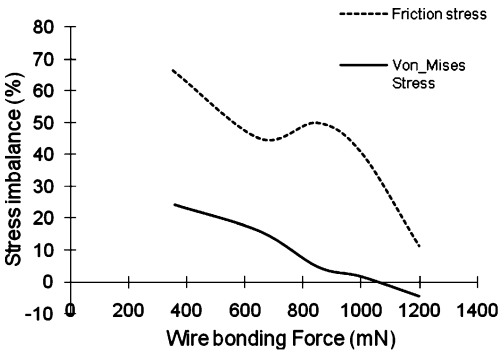


Fig. 4.37 Stress imbalance ($Stress_{left} - Stress_{right}$)/$Stress_{left}$ on bond pad vs. wire bonding force

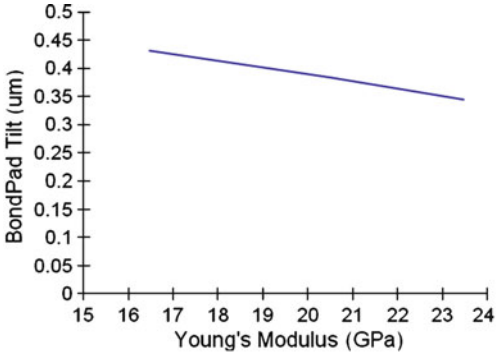


Fig. 4.38 Bondpad tilt vs. out of plane modulus of laminate

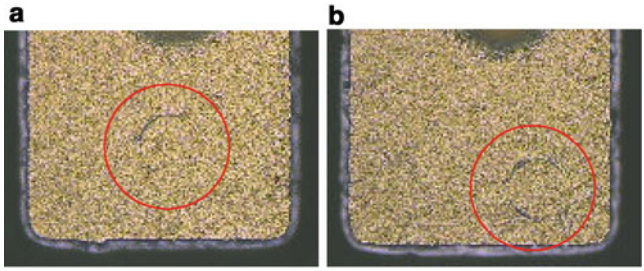


Fig. 4.39 Bonding capillary images at 25 and 85 g force showing imbalance compensation effect. (**a**) *Less half* capillary mark with 25 g force. (**b**) *Full circle* capillary mark with 85 g force

force 25 g, the print mark on bond pad is less than half circle due to imbalance force. However, when the wire bonding force is increased to 85 g, the capillary print mark seems to be a full circle. This agrees with our modeling results regarding the stress imbalance ratio vs. wire bonding force (see Fig. 4.37).

Therefore for designing a package with laminate substrate for a power IC application, from the above study it can obtain:

1. For the wire bonding above laminate with partial support, increasing the wire bonding force will increase the bond pad tilt, but it will reduce the stress imbalance and get better ball shear response. However, too high a wire bonding force will induce overstress on the bonding interface which will decrease the ball shear performance.
2. For laminate material under bondpad with partial support, the greater the out of plane modulus, the smaller the bond pad tilt. So selecting the higher out of plane modulus laminate material in design a package with laminate substrate is a good way to generate better wire bonding quality and reliabily.

4.4.5 Wafre Level Chip Scale Package for Power IC

One of the major application of power IC technology is the portable devices such as the mobile phones, PDAs, digital cameras, MP3 players and portable bar code readers. Fairchild's IntelliMAX™ family [7] of integrated load switches supports the latest generations of mobile and consumer electronic devices. The IntelliMAX family combines conventional MOSFET performance with a unique combination of protection, control and fault monitoring features to enhance power management design. This level of integration helps designers achieve efficiency and reliability while minimizing board space requirements. Wafter level chip scale package is particular suitable for the portable device due to its small size and the excellent electrical performance. Figure 4.40 shows two typical wafer level chip scale packages (WL-CSP) that are used for Fairchild IntelliMAX.

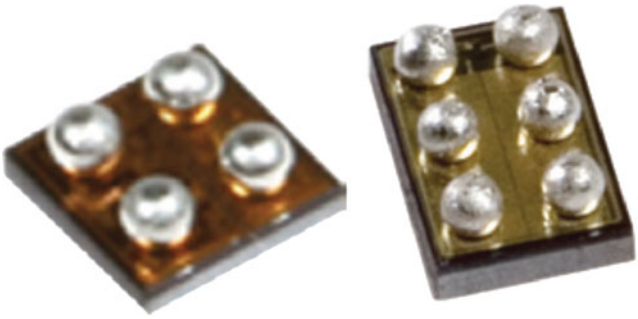


Fig. 4.40 Wafer level chip scale package for IntelliMAX

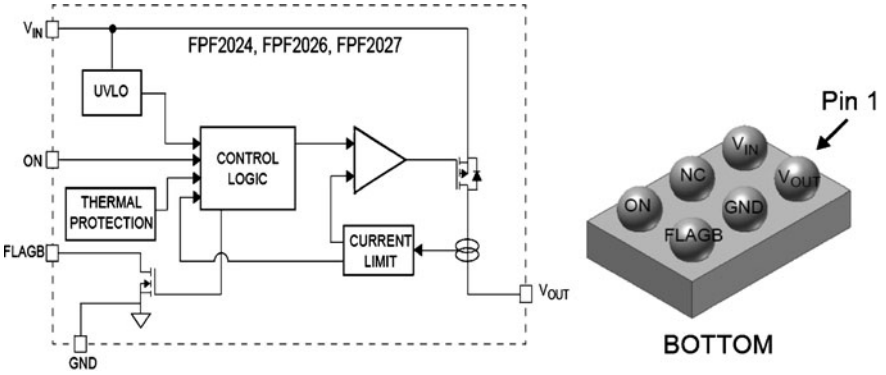


Fig. 4.41 The circuit of IntelliMAX that integrates the control logic and MOSFET with thermal protection and current limit

Figure 4.41 shows the circuit diagram of Fairchild IntelliMAX that integrates the control logic and MOSFET with a six pin WLCSP for the power IC device in which one pin is not used. This product has three major functions: (1) overcurrent limit protection (OCP), (2) thermal shutdown protection (TSP), and (3) undervoltage lock out (UVLO). The OCP prevents excessive current and triggers one of the three fault conditions: Automatic Restart which automatically shuts down and attempt to restart at the defined "auto restart time" interval until the fault is cleared; Shutdown: the part will automatically shut down and requires a power cycle on the "ON" pin to clear the fault. Constant Current: the part will limit the current to the fixed or user-defined value. The TSP protects the part from damage due to thermal events in which the threshold is 140°C, with 10°C hysteresis. The UVLO turns the switch off if the input voltage drops below a threshold which ensures stable operation of the device. Figure 4.42 shows the circuit diagram of another Fairchild IntelliMAX that integrates the control logic and MOSFET with a four pin WLCSP for the power IC device. This four pin power IC WLCSP has two major functions: (1) electrostatic discharge (ESD) protection and (2) turn on slew rate control which

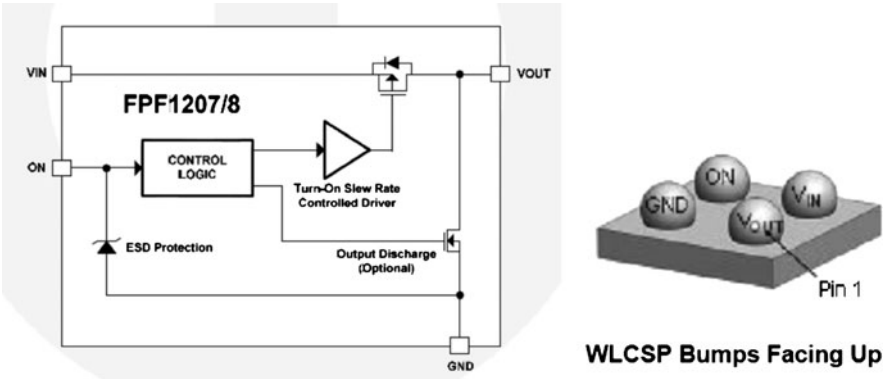


Fig. 4.42 The circuit of IntelliMAX that integrates the control logic and MOSFET with ESD protection and output discharges functions

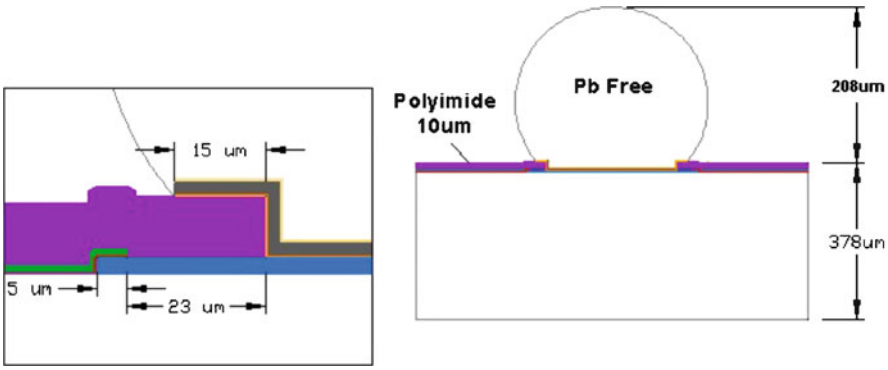


Fig. 4.43 The WLCSP bumping design with typical industry standard

turns the switch on over a defined period of time, which limits the current through the device and into the load. When balanced with the load capacitance, this feature helps to prevent current spikes on the load and minimize voltage sags on the input. This WLCSP also has the output discharge optional function which turns on when the main switch is turned off, offering quick and safe discharge of the load capacitance.

Figure 4.43 shows the WLCSP bumping design layout with typical industry standard metal stack for pad Al0.5Cu and underbumping metal (UBM) Au/Ni with Cu and Ti plating under the Ni layer. Between the UBM and the metal pad, there is a layer of polyimide. Figure 4.44 shows the WLCSP design layout with microbumping in 80 μm height. The design uses the metal stack with Al0.5Cu pad and Ni/Cu UBM with To plating under the Cu layer. The polyimide layer is placed between the UBM and metal pad. The two designs may be used for the both the six pin WLCSP and four pin WLCSP for power IC technology such as the IntelliMAX in Fairchild.

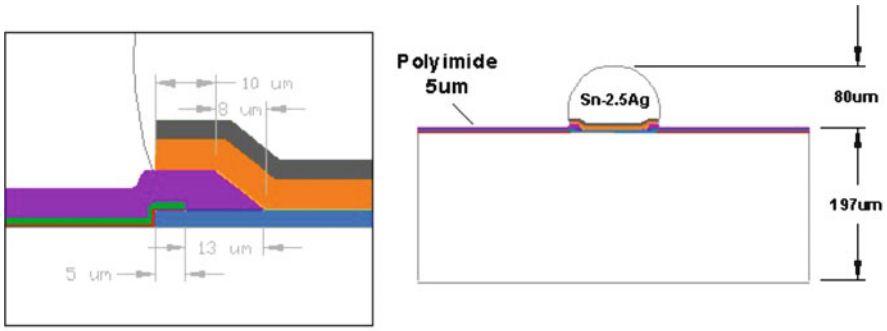


Fig. 4.44 The WLCSP bumping design with a 80 μm height

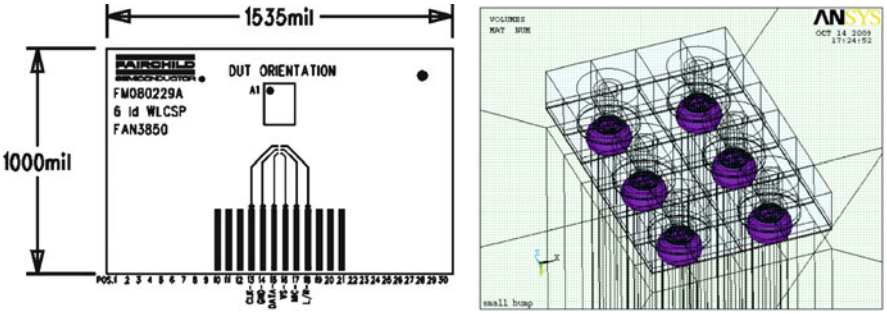


Fig. 4.45 Thermal cycling board and the six pin WLCSP model

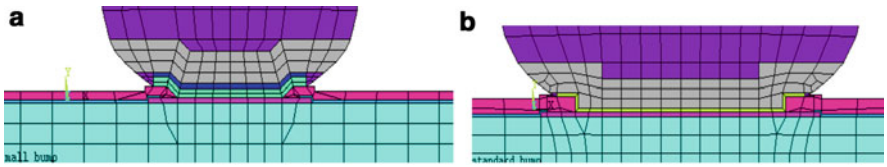


Fig. 4.46 The two models for the microbumping and standard bumping configurations. (**a**) Microbumping model. (**b**) Standard bumping model

From the design view point, solder joint plays a key role in the product reliability. This section compares the stress and the solder joint life for the microbumping and the standard bumping from the design concepts with six pin WLCSP in the thermal cycling (TMCL). The TMCL range in a cycle is −40 to 125°C/30 min. Figure 4.45 gives the test board layout and the model of the six pin WLCSP. Figure 4.46 shows the two models for the configurations of microbumping and the standard bumping, both bumpings use the Pb-free solder material 95.5Sn4.0Ag0.5Cu (SAC405).

Figure 4.47 shows the von Mises stress comparison of the microbumping and the standard bumping at −40°C in the TMCL. The max stress stress appears at the

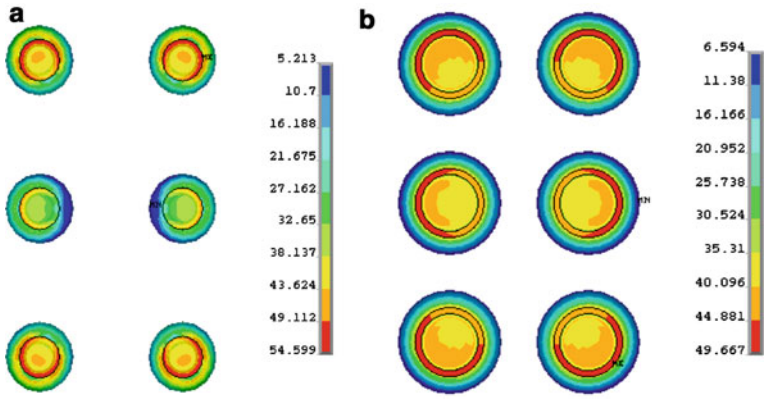


Fig. 4.47 The von Mises stresses of microbump and standard bump at −40°C in TMCL. (**a**) Microbump, max: 54.6 MPa, (**b**) standard bump, max: 49.7MPa

Table 4.6 The stress comparison of the microbumping and standard bumping in a six pin WLCSP

	PAD (Al-0.5Cu)		Polyimide (PI)		Solder (SAC405)	
Item	Microbump	Standard bump	Microbump	Standad bump	Microbump	Standard bump
Von Mises stress (MPa)	199.4	199.5	103.6	101.2	54.6	49.7
Von Mises plastic strain (%)	0.77	0.45	–	–	2.1	1
Max shear stress (MPa)	100.3	74.1	34.1	33.8	30	28.3
Max shear plastic strain (%)	1.1	0.29	–	–	3.4	1.8
Plastic energy density (MPa)	2.6	1.1	–	–	3.6	1.4

corner joints of die side and the von Mises stress of microbumping is greater than the standard bumping about 10%. Table 4.6 lists the maximum stress comparison of the metal pad Al0.5Cu, polyimide (PI) and the solder bumpings. In the metal pad, the maximum von Mises stresses of both the microbump and standard bump are equivalent, but the maximum von Mises plastic strain, plastic energy density, maximum shear stress, and strain of metal pad in the standard bump are significant small than the metal pad in the microbump case. All the stresses and strains and the plastic energy density in standard solder bump are small than the microbumping. The von Mises stress and shear stress in polyimide in standard bump are slightly less than the microbumping.

Table 4.7 shows the solder joint life comparison of the microbump and the standard bump. It can be seen from the Table 4.7 that the standard bump has

Table 4.7 The solder joint life comparison of microbump and the standard bump

TMCL life	Microbump	Standard bump
First failure	612	1,924 (52.6% longer)
Character cycle	995	3,129 (68.2% longer)



Fig. 4.48 The WL-CSP for the power IC integration (© 2009 IEEE [3])

much longer solder joint life than the microbump in bith first failure (52.6%) and the character life (68.2%). This is due to the plastic energy density in microbump is much greater than the standard bump. Therefore from the design view point based on the solder joint reliability in thermal cycling analysis, the standard bumping WLCSP is better than the microbumping. However, as the die shrinks, the microbumping technology for the power IC technology is approaching the requirement for next generation product, more studies and investigations for the power IC with micrbumping to get the robust design will definitely come out soon.

For the application of the power IC in a multiple function smart module platform with power analog and logic integration, different voltage rating isolated tubs can be added to high value resistors, capacitors, diodes, scaleable HV/LV CMOS, bipolar, and matched mirror devices that allows the integration of isolated analog pockets to realize high voltage level shift functions, precision voltage reference, current sensor accuracy, noise isolation, and eliminated substrate carriers injection. Trimmed components are also available in the PIC platform to make power analog product design highly accurate to provide a competitive advantage. The metal system in the platform can support multiple thin Al/Cu metal layers (4LM) for high density interconnections plus an extra thick power metal with BPOA for additional high current routing layer and enhanced energy capability. The thick power metal with BPOA is easily compatible with WLCSP in which the high-density features of this modular power IC platform can offer power analog technology with a great contribution in die size reduction (Fig. 4.48).

4.5 Summary

This chapter first introduced the development and evolution of the power IC technology, the power IC technology was developed from VDMOS discrete technology and the bipolar IC's technology to the mixed power technology which integrated bipolar, CMOS and DMOS with bipolar (diffusion) based technology. The mixed power technologies have been evolved with CMOS (implantation) based technology today. Then, this chapter introduces the trends of high power density at die level for power IC and its application in a portable product with a ultrathin MLP package; After that, the trends of smaller package footprints are discussed. The high power density is the drive to small form factor of power IC package, eventually leading the power IC package from QFN/MLP, BGA to move to small pitch WL-CSP. As the power IC die shrinks, the package footprints become small. This results in the high power density and high heat generation in a power IC die. Maintaining the thermal transfer capacity at the package level is difficult since the function/unit area of die is increasing with advanced BCDMOS processes. While the overall package footprint trend is decreasing, the thermal dissipation capabilities rely more on the PCB as part of the system. An example of MCSP package shows the effciiency of the role of the PCB for dissipating the heat to PCB through the substrate. At last, this chapter discusses the typical package constructions, design, assembly, modeling, and analysis for power IC technology which include MLP, MicroPak MLP, and wafer level chip scale package.

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Chapter 5
Power Module/SiP/3D/Stack/Embedded Packaging Design and Considerations

Over the last 2 decades, power semiconductor technology has made impressive progress by increasing the power density of monolithic and system modules [1–4]. This is the primary driving force behind power system in package (SiP), stack die, and 3D power packages with heterogeneous functional integration. For low-power ultraportable applications such as mobile phones and the iPad® tablet, the most critical requirement for the point of load (POL) buck converter is its size. There are several ways to build the buck converter power module. The typical approach is to design the product with die side by side placement in a single level module using a QFN or other standard package, but this method cannot get the benefit of smaller package size. Another way is to build the buck converter with stack die or 3D concept, which may significantly reduce the package size to satisfy the power management for portable application. For high power with hybrid integration, side by side die placement power module is the primary design method for motion control such as automotive, railway, wind energy and so on.

5.1 Side by Side Placement Power System in Package/Module

5.1.1 Lower Power Driver MOSFET System in Package

In this section, the lower power application with a side by side die placement system in package Fairchild 40L 6×6 DrMOS (Fig. 5.1) is considered.

5.1.1.1 The Design Layout of the Package

The 6×6 DrMOS package is based on Molded Leadless Packaging (MLP) technology. There are two MOSFET die (low side (LS) and high side (HS)) and one IC

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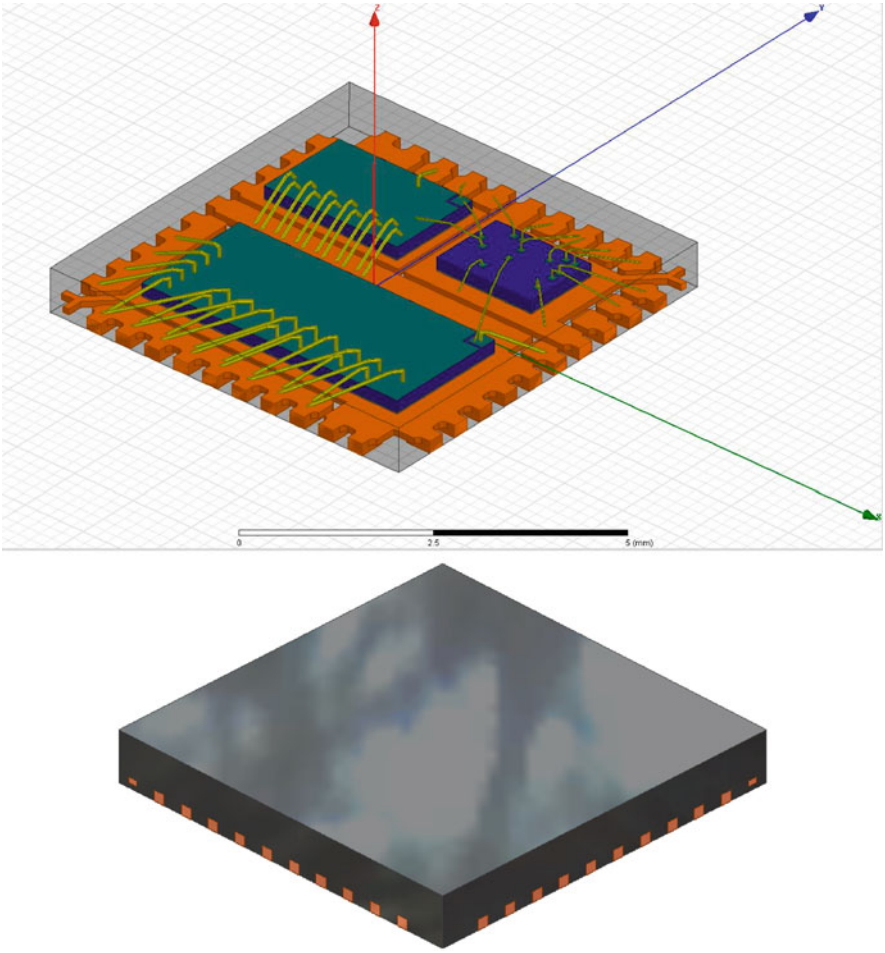


Fig. 5.1 A Fairchild DrMOS system in package

controller. The source of HS die is electrically connected to the drain of the LS die through bond wires. The source of LS die is connected to output pins by bond wires. All three die are side by side placed on three metal pads, then wire bonding the IC controller to the two MOSFETs and the output pins and then mold all the die and the metal frame to form the MLP system in package, see Fig. 5.1 the power module with built in molded clips. The layout of the die, metal pads, pin out, and the bond wires is shown in Fig. 5.2. This technology has been increasingly used in packaging for power related products due to its low package height, excellent thermal performance with large thermal pads in the center of the package which solder directly to the printed wiring board (PWB) and allow modularity in package design; single and multidie packages are within the capability of MLP technology.

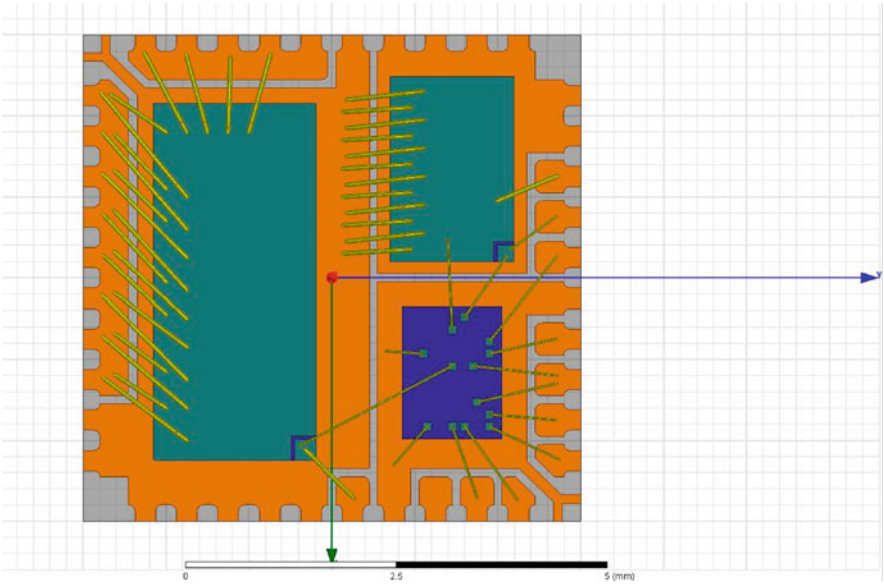


Fig. 5.2 The layout of the die, metal pads, bond wire, and pin out

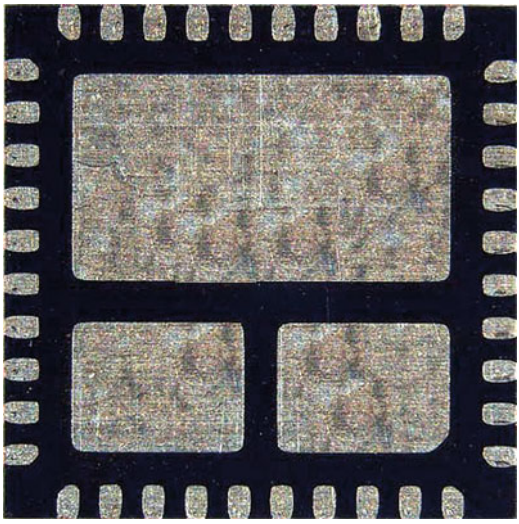


Fig. 5.3 Bottom view of the 6×6 DrMOS

The 6×6 DrMOS has three large die attach pads, allowing direct soldering to the PWB for best thermal and electrical performance.

Figure 5.3 shows the bottom side view of the 6×6 DrMOS system in package, which shows the three exposed pads. These three pads are related to the LS and

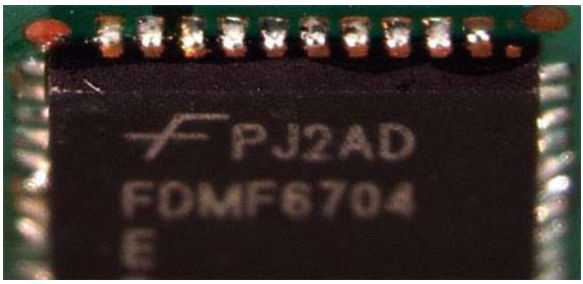


Fig. 5.4 Solder wetted to lead-frame copper exposed by singulation on lead ends

HS MOSFETs and the driver IC controller. The 6×6 DrMOS is designed to be used in high current synchronous buck DC–DC circuits, saving board space and component count by integrating several functions into one package. Since the solder joint and the pas design are important factors for the assembly reliability, below I list the considerations of the DrMOS in a reliable board level assembly [5].

(a) Board mounting
The pad must be designed to the proper dimensions to allow for tolerances in PWB fabrication and pick and place, and also to allow for proper solder fillet formation where applicable. MLP packages, when the preplated lead frame is sawn, show bare copper on the end of the exposed side leads. This is normal, and is addressed by IPC JEDEC J-STD-001C "Bottom Only Termination." However, it has been found that optimized PWB pad design and a robust solder process will typically yield solder fillets to the ends of the lead due to the cleaning action of the flux in the solder paste. Figure 5.4 shows the solder wetted to lead ends.

(b) PWB design considerations
Any land pad pattern must take into account the various tolerances involved in production of the PWB and the assembly operations required for soldering the DrMOS to the PWZB. These factors have already been taken into consideration on the recommended footprint given on the datasheet of the product. It is recommended that the customer follow this footprint to assure best assembly and ultimately reliability performance, as well as from a thermal performance.

(c) PAD finish
The most frequently encountered pad finish for consumer electronics with tin lead solders was hot air solder leveled, HASL. With lead free, other finishes are preferred. Immersion silver, immersion nickel gold, and organic surface protectant (OSP) are the board finishes of choice. Each finish has useful properties, and each has its challenges. It is beyond the scope of this section to discuss each system's merits. Not any one finish will be right for all applications, but currently the most commonly seen in large scale consumer electronics is OSP. A high quality OSP such as Enthone® Entek® Plus HT is recommended. Figure 5.5 gives the PWB pad with OSP pad finish.

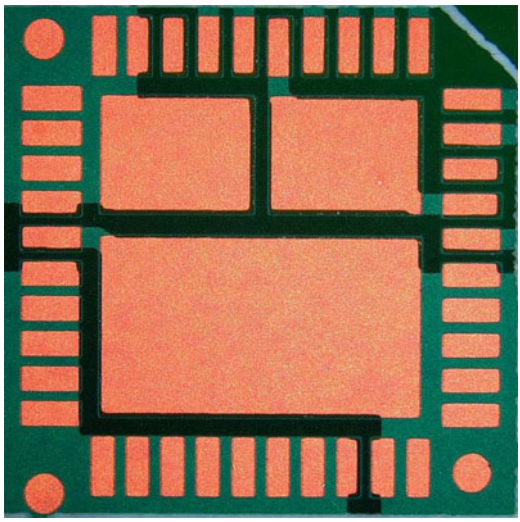


Fig. 5.5 Printed wiring board (PWB) pad with OSP pad finish

(d) PWB material
It is recommended that green FR4 is used in PWB construction. Lower quality FR4 can cause numerous problems with the reflow temperatures seen when using lead free solder. IPC-4101B "Specification for Base Materials for Rigid and Multilayer Printed Boards" contains further information on choosing the correct PWB material for the intended application.

(e) Using vias with 6×6 DrMOS
Often the designer will wish to place vias inside of the center pads. While this is acceptable, the user should realize that vias often create voiding, and carefully study the process design with X-ray inspection of voiding to assure the design is yielding the expected performance. There are several types of via. Blind vias are not recommended due to the fact they often trap gases generated during reflow and yield high percentages of voiding. Solder mask can also be placed over the top of the via to prevent solder from wicking down the via. It has been shown in previous studies that this will also create a higher incidence of voiding than an open through-hole or filled via. If through hole vias are used, a drill size of 0.3 mm with 1 oz copper plating yields good performance. The test board used four vias with favorable results. With through-hole vias, solder wicking through the hole, or solder protrusion, must be considered. Opening the solder mask just enough to keep from plugging the via is recommended. By not creating a pad for solder to wet to on the reverse side of the via will help prevent protrusion. In high reliability applications, filled vias are the preferred due to lower incidences of voiding during reflow and eliminating the stress riser created by a void at the edges of the via barrel.

(f) Stencil design
It is estimated that 60% of all assembly errors are due to paste printing. For a robust manufacturing process, it is therefore the most critical phase of assembly.

Due to the importance of the stencil design, many stencil types were tried to determine the optimal stencil design for the recommended footprint pad, on a typical application board with OSP surface finish, thermal vias, on FR4. It was found through statistical analysis the optimum solder paste coverage for the center drain and IC pads was 50–70% coverage using a 4 mil thick stencil. To allow gases to escape during reflow it is recommended that the paste be deposited in a grid allowing "channels" for gases to vent. Various other stencil apertures can be used, such as circles, but were not studied here. The paste is printed on the outer pins with a slightly reduced ratio to the PWB pad. IPC-7525 "Stencil Design Guidelines" gives a formula for calculating the area ratio for paste release prediction:

$$\text{Area ratio} = \text{Area of pad}/\text{area of aperture walls} = LW/(2LWT), \quad (5.1)$$

where L is the length, W the width, and T the thickness of the stencil. When using this equation, an Area ratio >0.66 should yield acceptable paste release. The recommended stencil apertures with for 50, 60, and 70% can be found in Fig. 5.6.

(g) Solder paste
The 6×6 DrMOS is a RoHS compliant and lead free package. The lead finish is NiPdAu. Any standard lead free no clean solder paste commonly used in the industry should work with this package. The IPC Solder Products Value Council has recommended that the lead free alloy, 96.5Sn/3.0Au/0.5Cu (SAC305), commonly known as SAC305, which is the lead free solder paste alloy family SAC of choice for the electronics industry." Figure 5.7 gives the printed solder paste pattern.

(h) Reflow profile
The optimum reflow profile used for every product and oven is different. Even the same brand and model oven in a different facility may require a different profile. The proper ramp and soak rates are determined by the solder paste vendor for their products. Obtaining this information from the paste vendor is highly recommended. If one is using a KIC® profiler, downloading the latest paste library from KIC® will yield ramp rate and soak times at temperature for most commonly used solder pastes. The Fairchild 6×6 DrMOS is rated for 260°C peak temperature reflow. Figure 5.8 is a reflow profile example. This profile is provided for reference only. Different PWBs, ovens and pastes might change this profile dramatically.

(i) Voiding
Voiding is a very controversial topic in the industry currently. The move to lead free solders, due to various governmental regulations, has created intense study in the area of solders, solder joints, and reliability effects. There are varying viewpoints on the effect of vias and allowable quantity. There are several types of voids; however, we divide them into two classes: macrovoids and microvoids. Macrovoids could also be called process voids. Macrovoids are the large sized voids commonly seen on X-ray during inspection. These voids

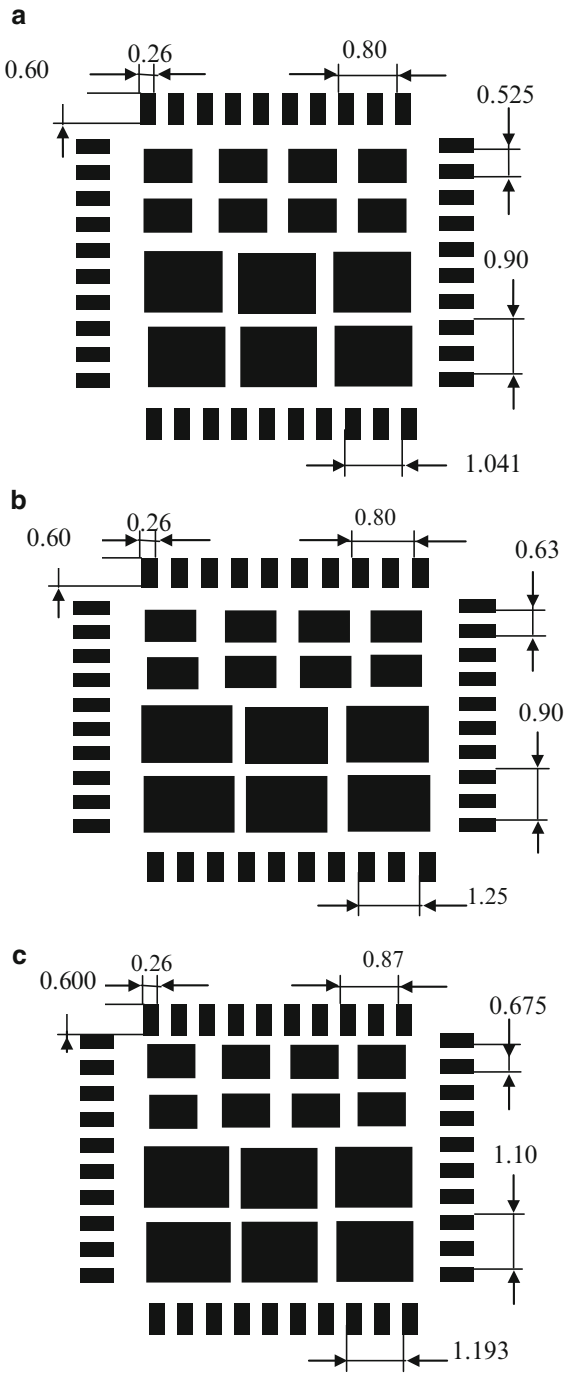


Fig. 5.6 The recommended stencil design for 6×6 DrMOS with different solder paste coverage. (**a**) 50% Solder paste coverage, (**b**) 60% solder paste coverage, (**c**) 70% solder paste coverage

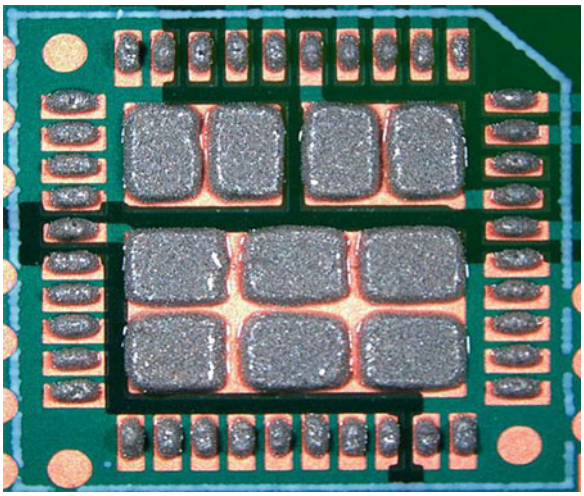


Fig. 5.7 Printed solder paste pattern

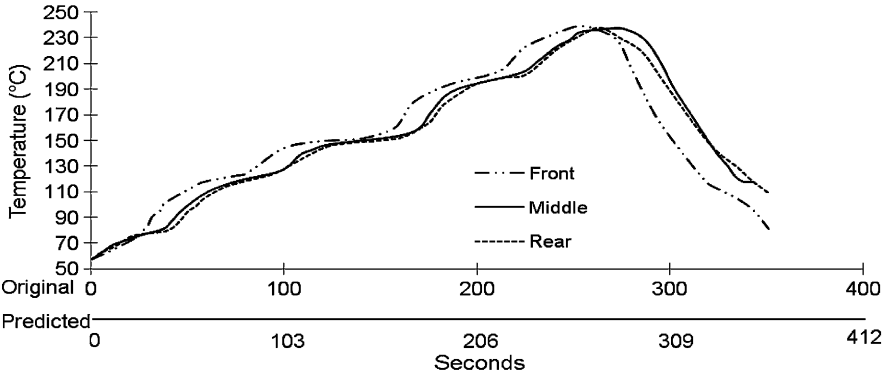


Fig. 5.8 An example of reflow profile for 6×6 DrMOS

are due to process design/control issues, or PWB design issues. All of the parameters discussed in this application note will effect macrovoiding. Most standards that currently exist, such as IPC-610D specifically address void criteria for BGA, and limit it to 25%. This standard is for macrovoiding. There is currently no IPC standard for voiding under large soldered areas as seen on the 6×6 DrMOS. Fairchild has done several studies of the amount of voiding in various types of components with large thermal pads, and the effect on reliability. It was found that components with 25% voiding or less had acceptable reliability performance in package qualification temperature cycling. Fairchild gives the customer the guideline of 25% voiding for 6×6 DrMOS packages. There are also several forms of microvoiding, namely,

planar microvoids and Kirkendall voids. The mechanism of void creation is different for each; however, both are practically undetectable by X-ray inspection. Both types are also currently the subject of several in-depth studies; however, none have confirmed theories of creation. Planar microvoids, or "champagne voids" occur at the PWB land to solder joint interface. There are several theories on the mechanism that creates planar microvoids, but there is not a confirmed root cause. Planar microvoids are a risk for reliability failures. Kirkendall voids are created at the interface of two dissimilar metals at higher temperatures, and in the case of solder attachments, at the pad to joint intermetallic layer. They are not due to the reflow process; Kirkendall voids are created by electromigration in assemblies that spend large amounts of time above 100°C. There is currently conflicting evidence whether Kirkendall voids are a reliability risk or not.

(j) Rework
Due to the high temperatures associated with lead free reflow, it is recommended that this component not be reused if rework becomes necessary. The 6×6 DrMOS should be removed from the PWB with hot air. After removal, the 6×6 DrMOS should be discarded. The solder remnants should be removed from the pad with a solder vacuum or solder wick, the pads cleaned and new paste printed with a ministencil. Localized hot air can then be applied to reflow the solder and make the joint. Due to the thermal performance of this component, and the typical high performance PWB it will be mounted on, quite a bit of heat energy will be necessary. Heating of the PWB may be helpful for the rework process.

(k) Board level reliability
As mentioned previously, per JDC-STD-001D a solder fillet is not required on the side of the lead for this package. But it has been found through modeling and temperature cycling that a solder fillet on the lead end can improve reliability. An improvement of 20% can be expected with this fillet. It was also found that if the fillet only wets half way up the side of the lead, this reliability enhancement is still attained. Through process control these fillets are often created. As part of the standard reliability testing this package was temperature cycled from −10 to 100°C. There could be no failures in the sample set at 1,000 cycles to pass the test.

5.1.1.2 Design Optimization of the DrMOS Package

To reduce cost and improve time to market, electrical and thermal virtual prototyping are applied to investigate the electrical and thermal performance of the power package [6, 7]. The 3D finite element models for the design optimization are generated for conducting the design of experimental (DoE) numerical simulations.

(a) Electrical Simulation

In this section, the impact of bond wire diameter, bond wire number, and die size of the LS and HS MOSFETs on the DrMOS package design in Fig. 5.9 is investigated. Totally eight DoE legs are designed [7]. For models 1–3, the bond wire diameters of the LS and HS MOSFETs are 1, 2, and 3 mil, respectively. The ratio of bond wire numbers for LS and HS MOSFETs is kept as 20:10. For models 4 and 5, the bond wire diameters are 3 mil, and the ratio of bond wire numbers for LS and HS MOSFETs is 6:3 and 10:5, respectively. Clip bonds are used for LS and HS MOSFETs connection in model 6. For model 7, the die size for both LS and HS MOSFETs increases 20%, and the ratio of bond wire numbers for LS and HS MOSFETs is 10:5 with the bond wire diameter 3 mil. Model 8 has the same bond wire condition as model 7, except that the die size for both LS and HS MOSFETs decreases 20%.

The current density distributions of the eight DoE legs are illustrated in Fig. 5.9. The current density is a measure of the density of flow of a conserved electric charge, and it is defined as the electric current per unit area of cross section. High current densities have undesirable consequences. Most electrical conductors have a finite, positive resistance, making them dissipate power in the form of heat. The current density must be kept sufficiently low to prevent the conductor from melting or burning up, or the insulating material failing. From the simulation results, it can be seen that model 6 with the clip bond for both MOSFETs has the lowest current density among all the cases.

The extracted resistances and inductances (the ground (GND) and VDD parasitic and R_{DSon}) of all the DoE legs are illustrated in Fig. 5.10. Model 6 with the clip bond produces the lowest resistance of LS and HS R_{DSon}, as well as the lowest inductance of LS and HS MOSFETs. The bond wire diameter change from 1 to 3 mil has very little impact on the inductance values of both the LS and HS MOSFETs. However, the resistance of both LS and HS R_{DSon} decreases with the increase of the bond wire diameter (as shown in Fig. 5.11). The impact of bond wire numbers for the LS and HS MOSFETs is shown in Fig. 5.12. It can be seen that both the inductance and resistance values decrease with more bond wires. However, the inductance and resistance tend to be saturated with the increase of bond wire diameter and bond wire numbers. Comparing with the bond wire diameter and bond wire numbers, the die size has relatively small impact on the extracted *R*/*L* values, especially for the LS MOSFET (as shown in Fig. 5.13).

The efficiency of a component is defined as useful power output divided by the total electrical power consumed. Conduction losses in switching power supplies are induced by the parasitic resistance from packaging (wire bonds, lead frame, solder, solder balls, etc.), in addition to the on resistance of the MOSFETs. For the buck converter circuit of the SiP package as shown in Fig. 5.14a, the conduction efficiency (without considering other power losses, such as inductor conduction loss) is defined as

$$\eta = \frac{P_{\mathrm{o}}}{P_{\mathrm{o}} + P_{\mathrm{C\text{-}HS}} + P_{\mathrm{C\text{-}LS}}} \tag{5.2}$$

where P_{o} is the output power, $P_{\mathrm{C\text{-}HS}}$ and $P_{\mathrm{C\text{-}LS}}$ are the consumed power by the HS and LS MOSFETs, respectively.

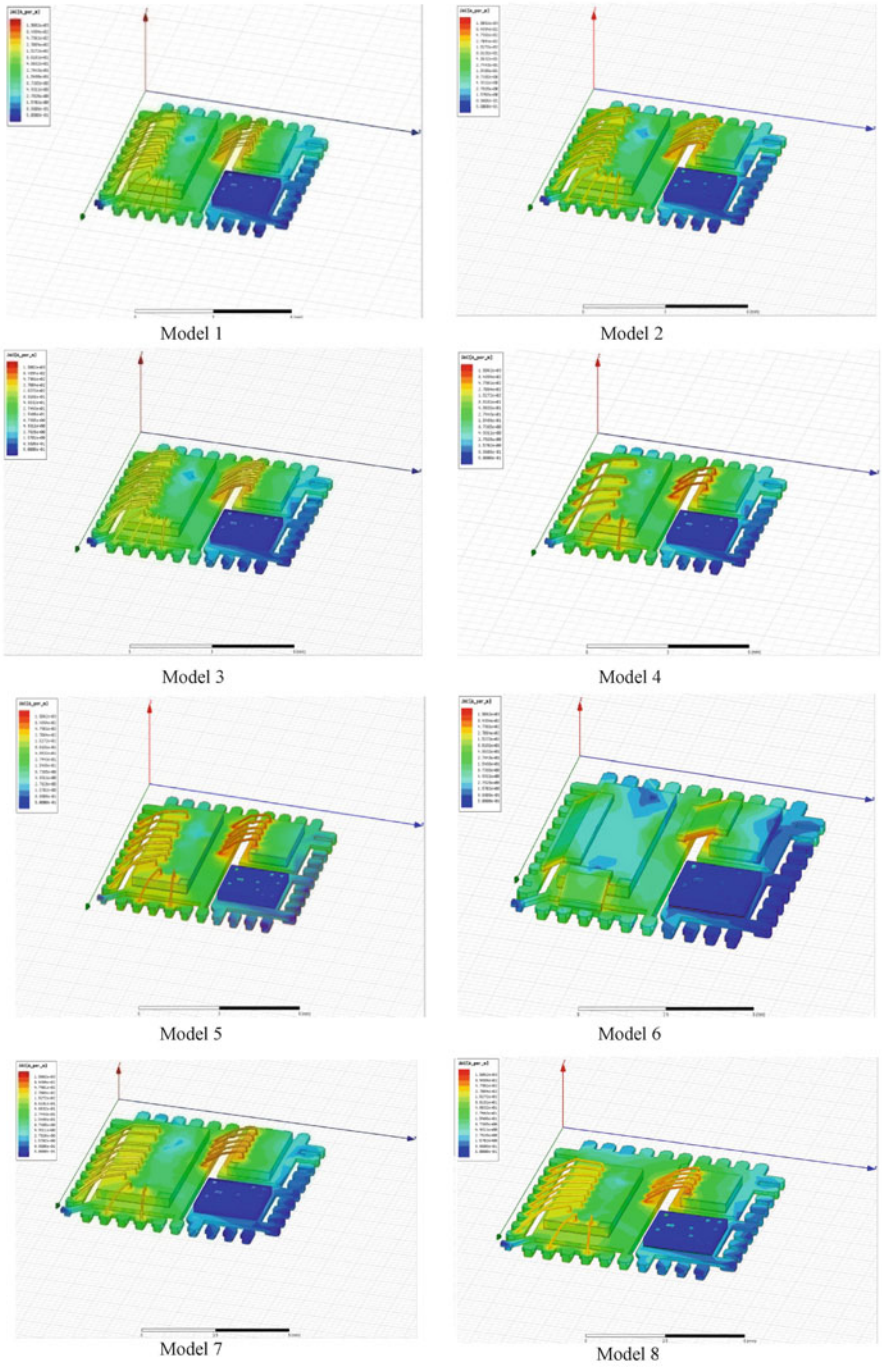


Fig. 5.9 The current density distributions of eight design of experimental (DoE) legs

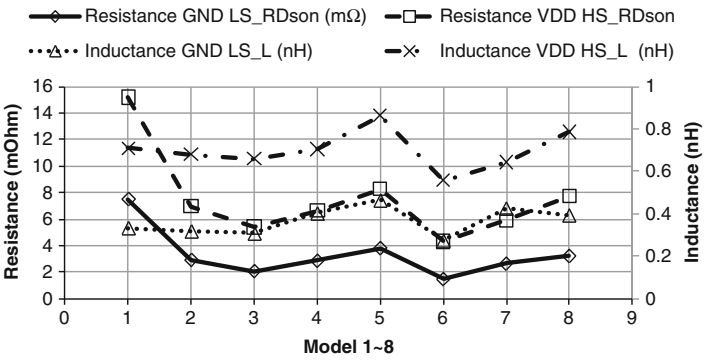


Fig. 5.10 The comparison of *R*/*L* values for all the eight DoE legs

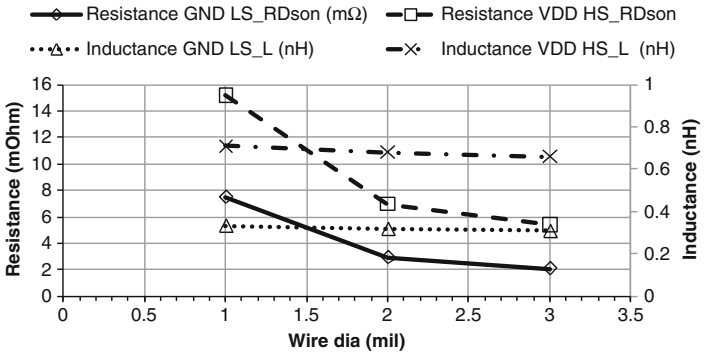


Fig. 5.11 Impact of wire diameter on the *R*/*L* values

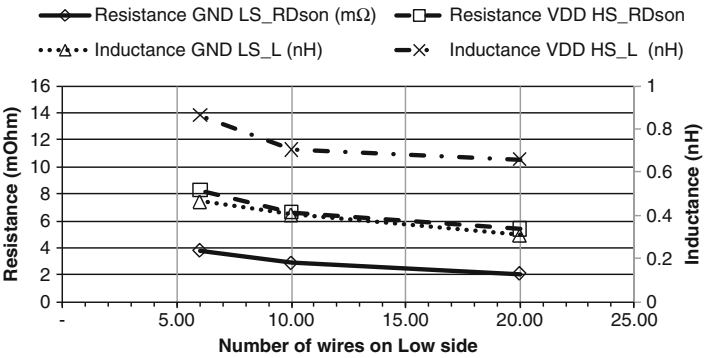


Fig. 5.12 Impact of bond wire numbers on the *R*/*L* values

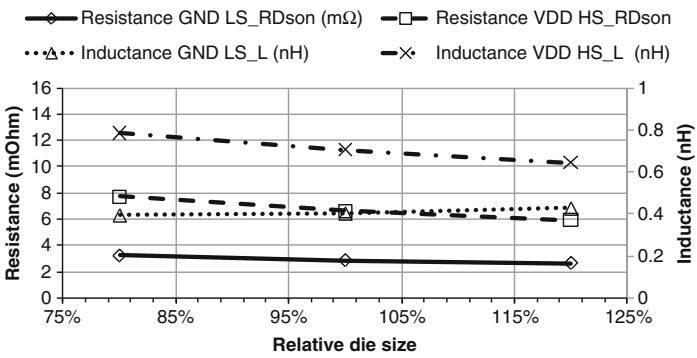


Fig. 5.13 Impact of die size on the *R*/*L* values

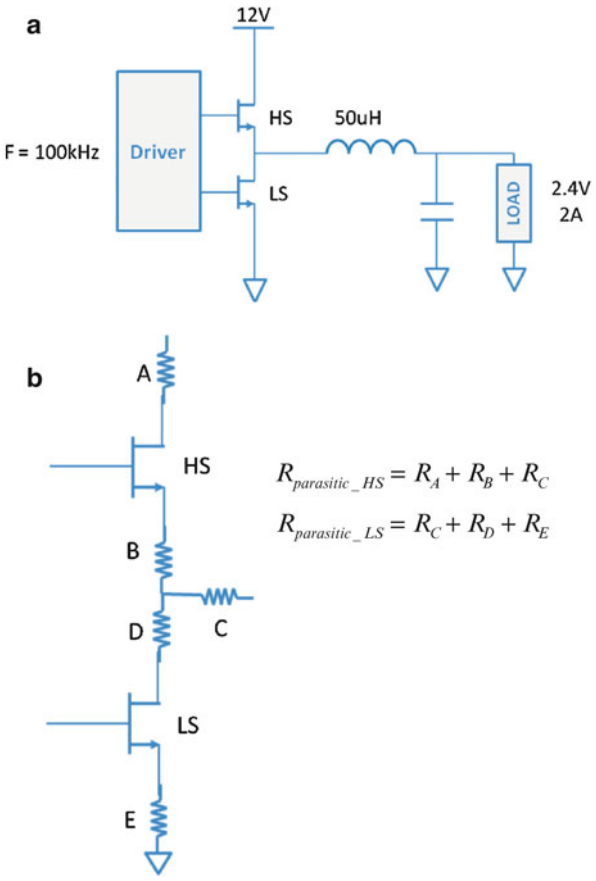


Fig. 5.14 The schematic diagram a buck converter. (**a**) Schematic of the buck converter circuit. (**b**) Parasitic resistance of the packaging

$$P_{\mathrm{o}} = I_{\mathrm{out}} \cdot V_{\mathrm{out}}$$

$$P_{\text{C-HS}} = \left(R_{\text{DSon-HS}} + R_{\text{parasitic-HS}}\right) \cdot \frac{2}{3} \cdot I_{\mathrm{out}} \cdot I_{\mathrm{pk}} \cdot \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} \tag{5.3}$$

$$P_{\text{C-LS}} = \left(R_{\text{DSon-LS}} + R_{\text{parasitic-LS}}\right) \cdot \frac{2}{3} \cdot I_{\mathrm{out}} \cdot I_{\mathrm{pk}} \left(1 - \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}\right)$$

where I_{out} (variable) and V_{out} (=2.4 V) are output current and voltage, $R_{\text{DSon-HS}}$ and $R_{\text{DSon-LS}}$ are the on resistances between drain and source in HS and LS die, $R_{\text{parasitic-HS}}$ and $R_{\text{parasitic-LS}}$ stand for parasitic resistance of HS and LS MOSFETs, respectively as shown in Fig. 5.14b, V_{in} (=12 V) is the input voltage, and I_{pk} is defined in the following equation.

$$I_{\mathrm{pk}} = \frac{\Delta I}{I_{\mathrm{out}}} + I_{\mathrm{out}} \tag{5.4}$$

where ΔI in the following format

$$\Delta I = \Delta T \left(\frac{V_{\mathrm{in}} - V_{\mathrm{out}}}{L}\right) \tag{5.5}$$

where L is the inductance (50 μH) as shown in Fig. 5.14a, ΔT in the following format, with f_{sw} (=100 kHz) as the switching frequency

$$\Delta T = \frac{V_{\mathrm{out}}}{f_{\mathrm{sw}} V_{\mathrm{in}}} \tag{5.6}$$

The conduction efficiencies of all the eight DoE models are calculated according to (5.2), with different output current (0.2–6 A) studied. The efficiency comparison of all eight DoE models is illustrated in Fig. 5.15, in which similar trends have been observed. The efficiency increases when the output current increases from 0.2 A. It reaches the maximum value when the output current is 1 A, and then decreases when the output current becomes higher. Among all the cases, model 6 design with clip bond has the highest efficiency.

(b) Thermal Analysis

Thermal simulations of θ_{JA} for all the DoE models are conducted by using the finite element analysis (FEA) software ANSYS®. The standard JEDEC thermal boards of

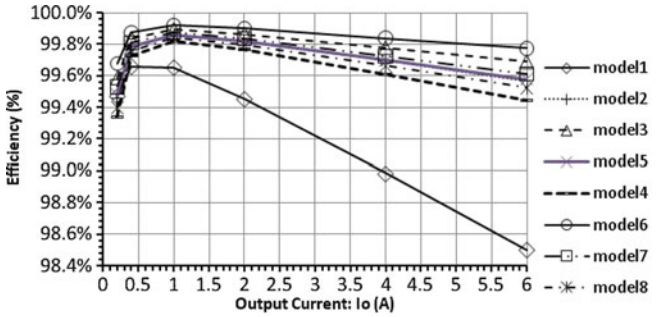


Fig. 5.15 Efficiency of all eight DoE models with respect to different output current

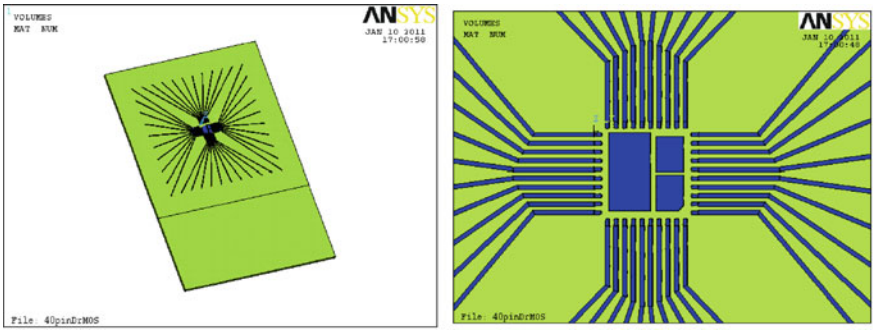


Fig. 5.16 Finite element analysis (FEA) model for the JEDEC thermal board with 1s0p layout

1s0p, 1s2p, and 1s2p with thermal vias, are applied to all the DoE simulation legs [7–9]. The 1s0p thermal board has only a top trace layer in the component mounting and trace fan-out region (see Fig. 5.16). The 1s2p thermal board is formed by embedding two 35 μm copper planes in the printed circuit board (PCB). For packages that need direct thermal contact with the thermal test board, thermal vias can be designed in the PCB. Thermal vias are only allowed on multilayer test boards, spaced with a 1.2 × 1.2 mm grid.

In the thermal model, the HS MOSFET is defined as die 1, the LS MOSFET as die 2, and the IC as die 3. If the power is applied to die 1, the temperature distribution of the whole model can be obtained. The thermal resistance θ_{JA11} can be calculated based on the following equation

$$\theta_{JA11} = (T_{1j} - T_a)/P_d \tag{5.7}$$

where T_{1j} is the junction temperature of die 1, T_a is the ambient temperature, P_d is the power applied. θ_{JA22} and θ_{JA33} can be obtained in the similar way.

The temperature distribution for model 1 with three types of thermal boards is illustrated in Fig. 5.17, in which 1 W power is applied on die 1. The left figure

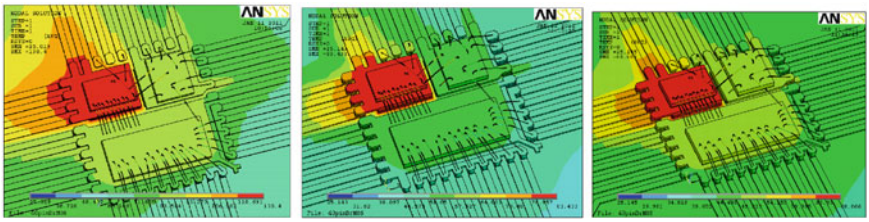


Fig. 5.17 Temperature distribution for model 1 with three types of thermal boards by applying 1 W power on die 1

corresponds to the simulation results of 1s0p thermal board, the middle one to the 1s2p thermal board, and the right one to the 1s2p thermal board with ten thermal vias. The junction temperature of die 1 decreased almost 50% using the 1s2p thermal board with ten thermal vias comparing to the 1s0p thermal board.

The thermal resistance θ_{JA} comparison of all the DoE legs with three types of thermal boards is shown in Fig. 5.18. Model 6 with clip bond has the lowest thermal resistance for all dies and for all thermal boards. The thermal resistance decreases with the increase of the bond wire diameter, and models with more bond wires produce lower thermal resistance. The impact of die size on the thermal resistance is not significant. However, the thermal test board plays an important role. The θ_{JA} decreases more than 50% for 1s2p thermal board with ten thermal vias, comparing with that for 1s0p thermal board. For the eight DoE models, only the bond wires and die size of the two MOSFETs change, and the bond wires and die size of the IC die keep the same. This explains why the thermal resistance θ_{JA33} has very little variation for the eight models. From Fig. 5.18, it can be seen that the thermal resistance θ_{JA22} is the lowest as compared to θ_{JA11} and θ_{JA33}.

5.1.2 Hybrid Power System in Package Module

In this section, the hybrid die side by side placement for power system in package module is introduced. This type of power module is mainly used in motion control for energy saving and quiet-running. The terms "energy-saving" and "quiet-running" are becoming very important in the world of variable speed motor drives. For low-power motor control, there are increasing demands for compactness, built-in control, and lower overall-cost. An important consideration, in justifying the use of inverters in these applications, is to optimize the total cost–performance ratio of the overall drive system. In other words, the systems have to be less noisy, more efficient, smaller and lighter, more advanced in function, and more accurate in control with a very low cost. In order to meet these needs, Fairchild has developed a series of compact, high-functionality, and high efficiency power semiconductor device called motion-smart power module (SPM®) in Mini-DIP package [8]. This Motion-SPM™ package based inverters are now considered an excellent

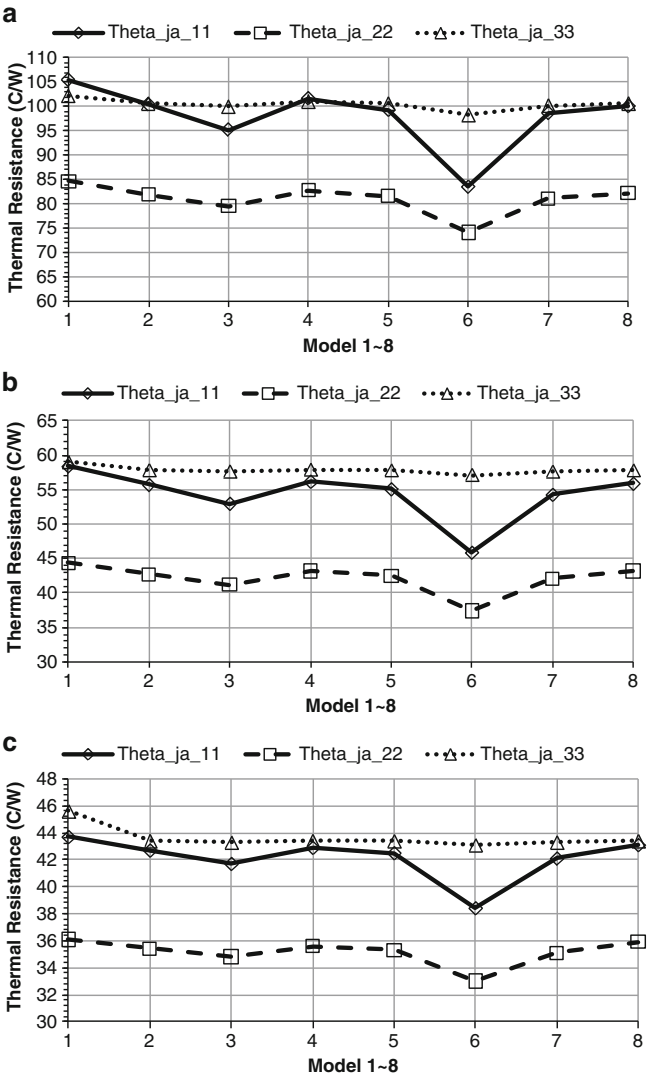


Fig. 5.18 The thermal resistance comparison for all the DoE models with different JEDEC boards. (**a**) Thermal resistance comparison for all eight DoE models with 1s0p thermal board. (**b**) Thermal resistance comparison for all eight DoE models with 1s2p thermal board. (**c**) Thermal resistance comparison for all eight DoE models with 1s2p board with ten thermal vias

alternative to conventional discrete-based inverters for low-power motor drives, specifically for appliances such as washing machines, air-conditioners, refrigerators, water pumps, etc. This Motion-SPM package combines optimized circuit protection and drive matched to the insulated gate bipolar transistor's (IGBT's) switching characteristics. System reliability is further enhanced by the

integrated undervoltage protection function and short circuit protection function. The high speed built-in HV IC provides an opto-coupler-less IGBT gate driving capability that further reduces the overall size of the inverter system design. Additionally, the incorporated HV IC allows the use of a single-supply drive topology without negative bias. The section is to show the detailed power module and circuit design of Motion-SPM product in Mini-DIP package and its applications. It provides design examples which enable motor drive design engineers to create efficient optimized designs with shortened design cycles.

5.1.2.1 Design Concept of the SPM Module

The key design objective of Motion-SPM product in Mini-DIP package is to create a low power module with improved reliability. This is achieved by applying existing IC and LSI transfer mold packaging technology. The structure of Motion-SPM package is relatively simple: power chips and IC chips are directly die bonded on the copper lead frame, and the bare ceramic material is attached to the frame, and then molded into epoxy resin. In comparison, the typical IPM is made of power chips bonded on a metal or ceramic substrate with the ICs and the passive components assembled on a PCB. This is then assembled into a plastic or epoxy resin case and filled up with silicon gel. The Motion-SPM product in Mini-DIP package greatly minimizes the number of parts and material types, optimizing the assembly process and overall cost. This is the first design advantage.

The second important design advantage of Motion-SPM product in Mini-DIP package is the realization of a product with smaller size and higher power rating. Of the low power modules released to date, the Motion-SPM product in Mini-DIP package has the highest power density with 3–30 A rated products built into a single package outline.

The third design advantage is the design flexibility enabling use in a wide range of applications. This Motion-SPM package series has two major flexibility features. First is the 3-N terminal structure with the negative rail IGBT emitters terminated separately. With this structure, shunt resistance can be placed in series with each 3-N terminal to easily sense individual inverter phase currents. Second is the HS IGBT switching dv/dt control. This is made possible by the insertion of an appropriate impedance network in the HS IGBT gate drive circuits. By properly designing the impedance network, the HS switching speed can be adjusted so that critical electromagnetic interference (EMI) problems may be easily dealt with. The detailed features and integrated functions are listed as follows:

- 600 V/3–30 A ratings in one package (with identical mechanical layouts)
- Low-loss efficient IGBTs and fast recovery diodes (FRDs) optimized for motor drive applications
- High reliability due to fully tested coordination of HV IC and IGBTs
- 3-Phase IGBT Inverter Bridge including control ICs for gate drive and protection

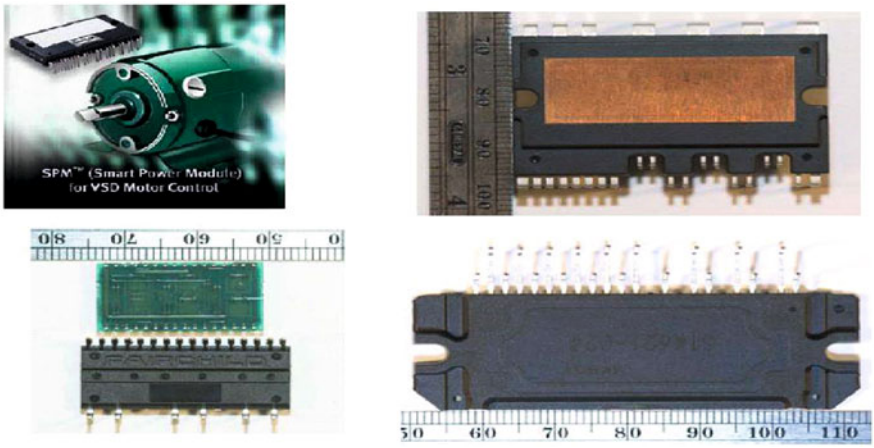


Fig. 5.19 Motion-SPM package

  - HS features: Control circuit under voltage (UV) protection (without fault signal output)
  - LS features: UV and short-circuit (SC) protection through external shunt resistor (with fault signal output)

- Single-grounded power supply and opto-coupler-less interface due to built-in HV IC
- Active-high input signal logic resolves the startup and shutdown sequence constraint between the VCC control supply and control input providing fail-safe operation with direct connection between the Motion-SPM package and a 3.3 V CPU or DSP. Additional external sequence logic is not needed
- Divided negative DC-link terminals for inverter applications requiring individual phase current sensing
- Isolation voltage rating of 2,500 V rms for 1 min
- Very low leakage current due to ceramic or direct bonding copper (DBC) substrate

Figure 5.19 shows the Motion-SPM package and its application in motor.

(a) Power devices—IGBT and FRD

The improved performance of Motion-SPM product in Mini-DIP package is primarily the result of the technological advancement of the power devices—IGBT and FRD in the 3-phase inverter circuit. The fundamental design goal is to reduce the die size and increase the current density of these power devices. Through optimized PT planar IGBT design, they maintain a SOA (Safe Operating Area) suitable for motor control application while dramatically reducing the on-state conduction and turn-off switching losses. They also implement smooth switching performance without sacrificing other characteristics. The FRDs are fast diodes that have a low forward voltage drop along with soft recovery characteristics.

(b) Control IC—LV IC, HV IC
The HV IC and LV IC driver ICs are designed to have only the minimum necessary functionality required for low power inverter drives. The HV IC has a built-in high voltage level shift function that enables the ground referenced PWM signal to be sent directly to the Motion-SPM package's assigned HS IGBT gate circuit. This level shift function enables opto-coupler-less interface, making it possible to design a very simple system. In addition a built-in undervoltage lockout (UVLO) protection function interrupts IGBT operation under control supply undervoltage conditions. Because the bootstrap charge-pump circuit interconnects to the LS VCC bias external to the Motion-SPM package, the HS gate drive power can be obtained from a single 15 V control supply referenced to control ground. It is not necessary to have three isolated voltage sources for the HS IGBT gate drive as is required in inverter systems that use conventional power modules. Recent progress in the HV IC technology includes chip downsizing through the introduction of wafer fine process technology. Input control logic change from the conventional low active to high active permits direct interface to 3.3 V microcontrollers or DSPs. This provides low circuit current, increased noise immunity, and good performance stability against temperature variation.

(c) SPM module layout
Since heat dissipation is an important factor which limits the power module's current capability, the heat dissipation characteristics of a package are critical in determining the performance of Motion-SPM package. A trade-off exists between heat dissipation characteristics and isolation characteristics. The key to a good package technology lies in the implementation of outstanding heat dissipation characteristics without compromising the isolation rating. In Motion-SPM product in Mini-DIP package, a technology was developed in which bare ceramic with good heat dissipation characteristics is attached directly to the lead frame. For expansion to a targeted power rating of 20 and 30 A in this same physical package size, DBC technology was applied. This made it possible to achieve optimum trade-off characteristics while maintaining cost-effectiveness. Figure 5.20 shows the cross sections of the Mini-DIP package. As seen in Fig. 5.20a, the lead frame structure was bent to secure the required electrical spacing. In Fig. 5.20b, the lead frame and the DBC substrate are directly soldered into this Motion-SPM product in Mini-DIP package lead frame.

The layout of side by side die placement for the IGBTs, FRDs, LV IC, and HV ICs inside the SPM module is shown in Fig. 5.21, in which the drains of six IGBTs and six FRDs are connected through lead frame on ceramics or DBC, the sources of the six IGBTs and six FRDs are connected through Al bonding wires. While the gates of IGBTs are connected to the leads which are connected to the LV IC and three HV ICs, the sources of FRDs are connected to the output pin leads.

The Motion-SPM product in Mini-DIP package is designed to satisfy the basic UL/IEC creepage and clearance spacing safety regulations required in inverter systems. In Mini-DIP, 3 mm creepage and 4 mm clearance are secured in all areas where high voltage is applied. In addition, the Cu frame pattern and

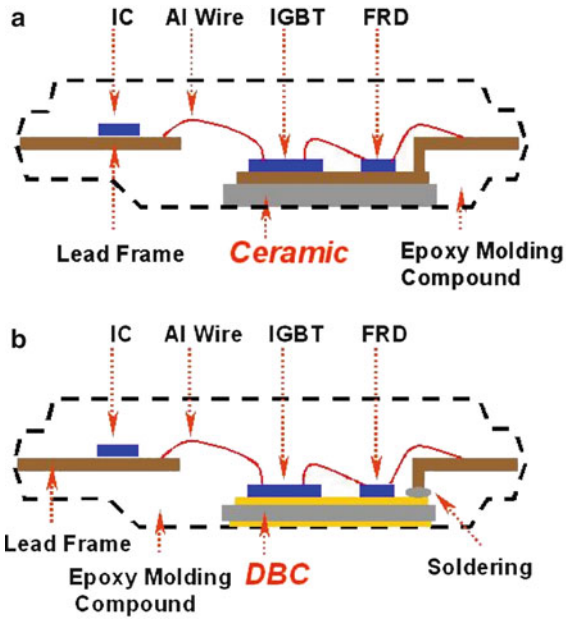


Fig. 5.20 Cross section of typical Motion-SPM module. (**a**) SPM package with ceramic substrate. (**b**) SPM package with direct bonding copper (DBC) substrate

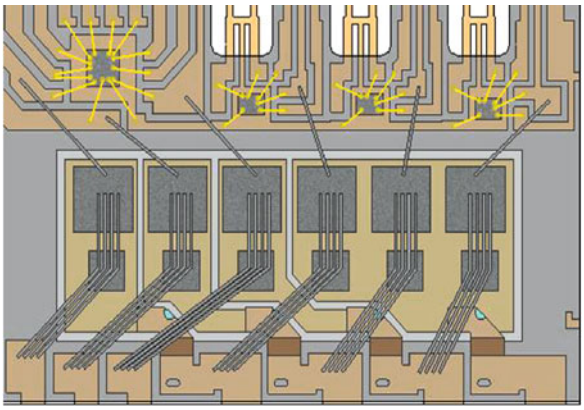


Fig. 5.21 The side by side die layout of IGBTs, FRDs, LV IC, and HV ICs inside the module

wire connection have been optimized with the aid of computer simulation for less parasitic inductance, which is favorable to the suppression of voltage surge at high frequency switching operation. HVIC is sensitive to noise since it is not a complete galvanic isolation structure but is implemented as a level shift latch logic using high voltage LDMOS that passes signals from upper side gate and lower side gate. Consequently, it was designed with sufficient immunity against

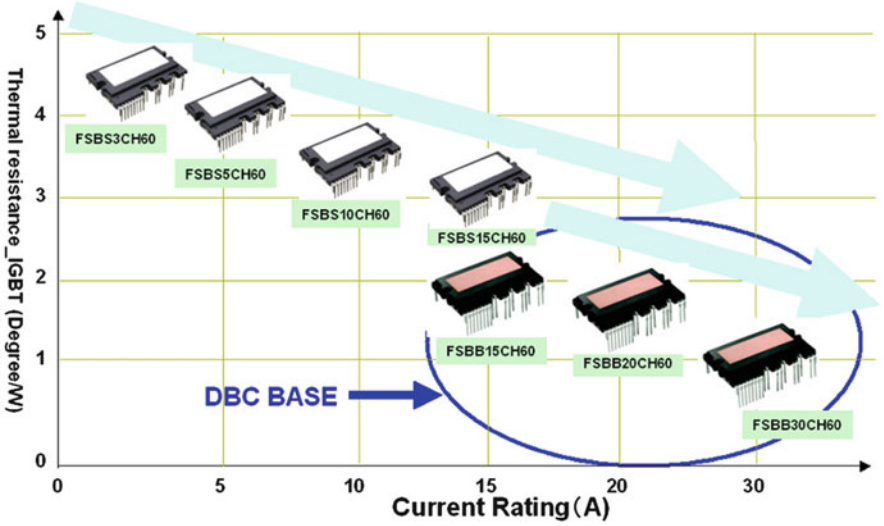


Fig. 5.22 Junction-to-case thermal resistance according to current rating of Motion-SPM product in mini-DIP package line-up

such possible malfunctions as latch-on, latch-up, and latch-off caused by IGBT switching noise and system outside noise. Fairchild's Motion-SPM design has also taken into consideration the possibility of HS malfunction caused by short PWM pulse. Since the low voltage part and the high voltage part are configured onto the same silicon in the HV IC, it cannot operate normally when the electric potential in the high voltage part becomes lower than the ground of the low voltage part. Accordingly, sufficient margin was given to take into account the negative voltage level that could cause such abnormal operation. Soft turn-off function was added to secure basic IGBT SOA under short circuit conditions. Motion-SPM product in Mini-DIP package was designed to have 3–30 A rated products built into a single package outline. Figure 5.22 shows the junction to case thermal resistance at each current range of this Motion-SPM. As seen in the figure, in the 15, 20, and 30 A range, intelligent 3-phase IGBT module with high power density (size vs. power) was implemented. Accordingly, in the low power range, inverter system designers are able to cover almost the entire range of 0.1–2.2 kW rating in a single power circuit design using this Motion-SPM package series. Since circuitry and tools can become more standardized, product development and testing process are simplified. This has significantly reduced development time and cost. Through control board standardization, overall manufacturing cost will be substantially reduced as users are able to simplify materials purchasing and maintain manufacturing consistency.

For the thin IGBT die attach process, one challenge is the die crack during molding process, Fig. 5.23 gives a die attach model with a single die, the bottom tensile stress vs. the void diameters with three different IGBT die thicknesses.

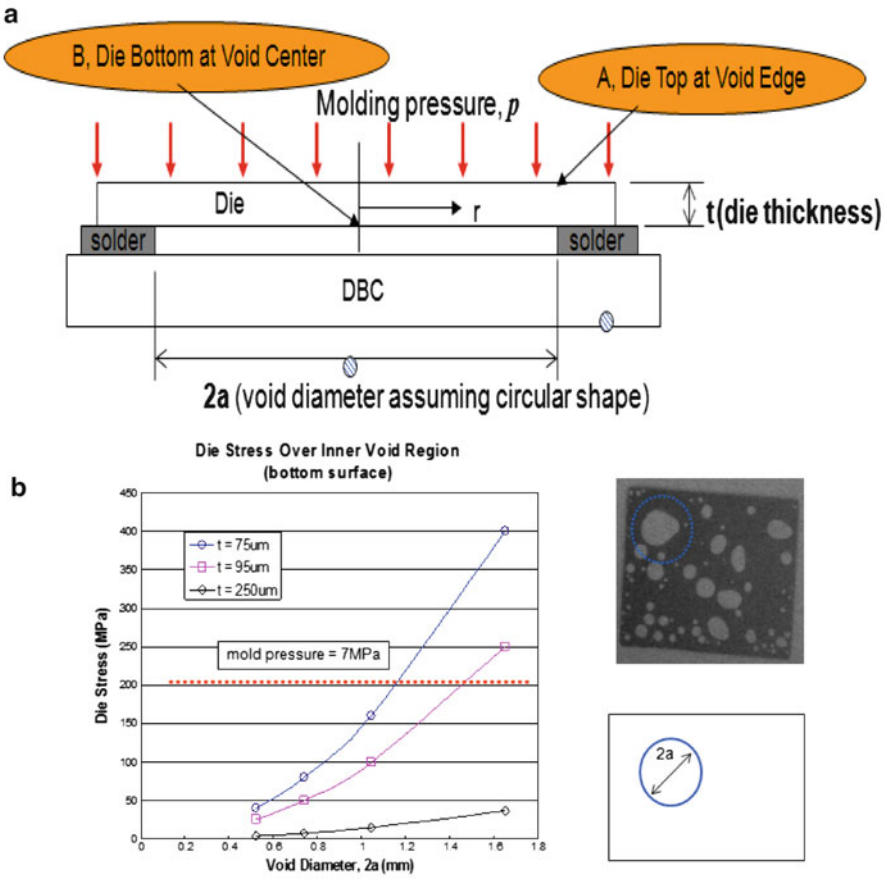


Fig. 5.23 The impact of the void on the stress of die bottom surface. (**a**) The die attach model with a single void. (**b**) The stress curves vs. void diameter

It can be seen from Fig. 5.23 that the die tensile stress at the bottom surface increases as the void diameter increases. When the void diameter exceeds 1.1 mm, the die with 75 μm thickness has reached its tensile strength. When the void diameter is larger than 1.4 mm, the die with 95 μm thickness has reached its tensile strength. However, for the thicker die with 250 μm, there is no much impact for the void size.

Figure 5.24 gives the outline of a typical Motion-SPM module design and Fig. 5.25 shows the input/output pins, and the dummy pins with description in larger fonts followed with arrows pointing to the dummy pins in the figure.

Figure 5.26 illustrates the internal block diagram of the Motion-SPM product in Mini-DIP package. It should be noted that the Motion-SPM package consists of a 3-phase IGBT inverter circuit power block and four drive ICs for control functions. The major features and integrated functions of the

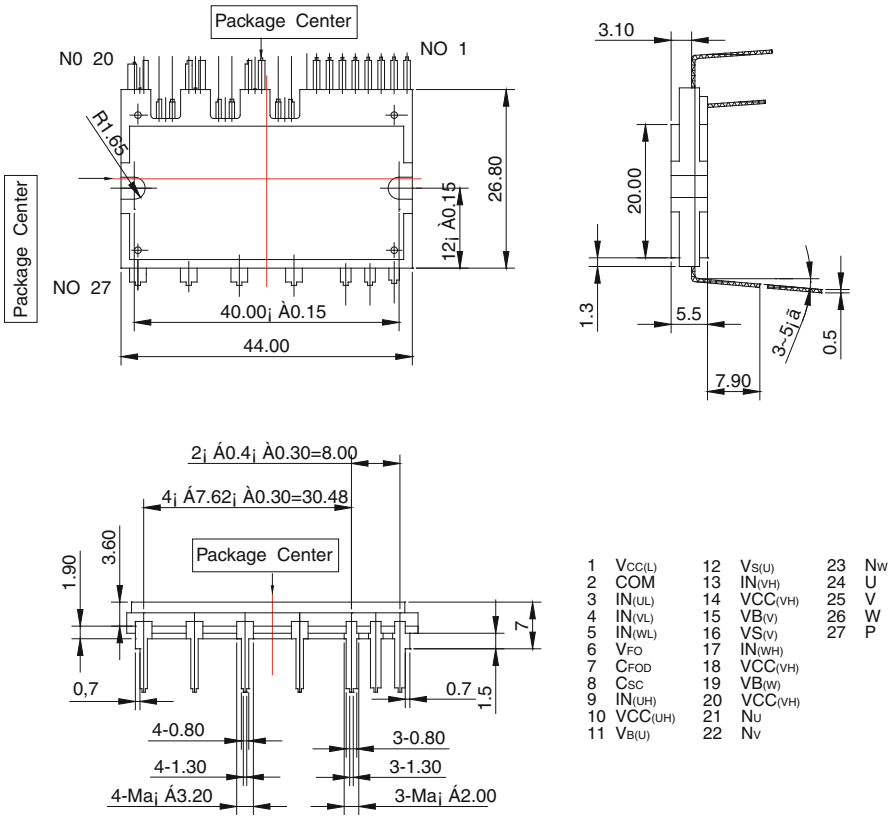


Fig. 5.24 The outline of a typical Motion-SPM module

above 27 pin Motion-SPM module and the benefits acquired by using it are described as follows.

Major features

- 600 V/3–30 A rating in one physical package size (mechanical layouts are identical).
- Low-loss efficient IGBTs and FRDs optimized for motor drive applications.
- Compact and low-cost transfer mold package allows inverter design miniaturization.
- High reliability due to fully tested coordination of HV IC and IGBTs.
- 3-Phase IGBT Inverter Bridge including control ICs for gate driving and protection—HS: Control circuit under voltage (UV) protection (without fault signal output)—LS: UV and Short-Circuit (SC) protection by means of external shunt resistor (with fault signal output).
- Single-grounded power supply and opto-coupler-less interface due to built-in HV IC.

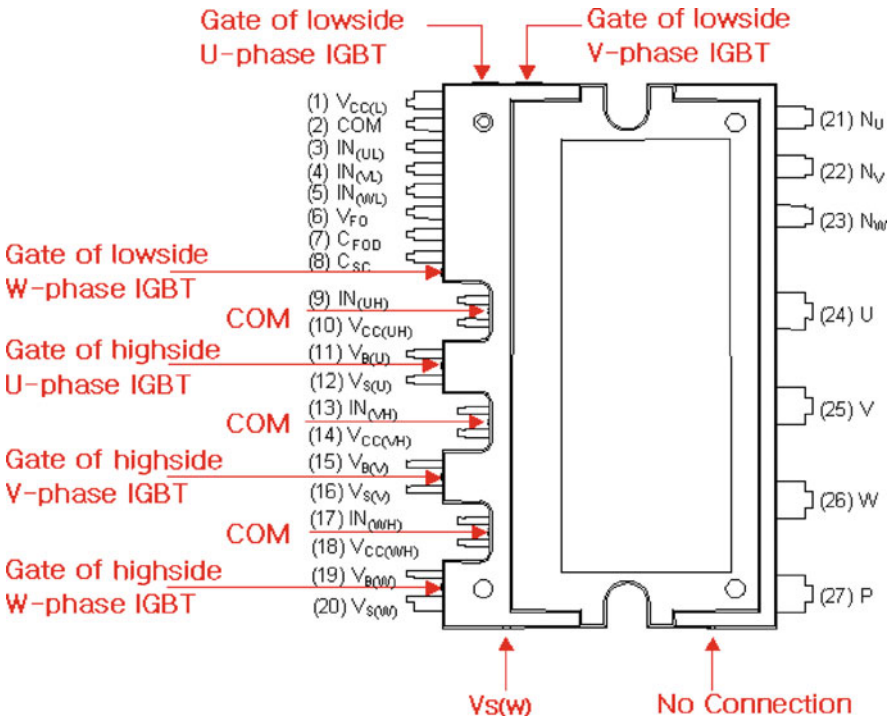


Fig. 5.25 The input/output pins and description of dummy pins in larger fonts followed with arrows

- IGBT switching characteristics matched to system requirement.
- Low leakage current and high isolation voltage due to ceramic and DBC-based substrate.
- Divided 3-N Power Terminals provide easy and cost-effective phase current sensing.
- Active-high input signal logic, resolves the startup and shutdown sequence constraint between the control supply and control input, this provides fail-safe operation with direct connection between the Motion-SPM package and a 3.3 V CPU or DSP. Additional external sequence logic is not needed.

Integrated functions

- Inverter HS IGBTs: Gate drive circuit, High-voltage isolated high-speed level shifting, Control supply under voltage (UV) protection.
- Inverter LS IGBTs: Gate drive circuit, Short-circuit protection with soft shutdown control, Control supply circuit undervoltage protection.
- Fault signaling (VFO): Corresponding to a SC fault (LS IGBTs) or a UV fault (LS supply).
- Input interface: 3.3, 5 V CMOS/LSTTL compatible, Schmitt trigger input, Active high.

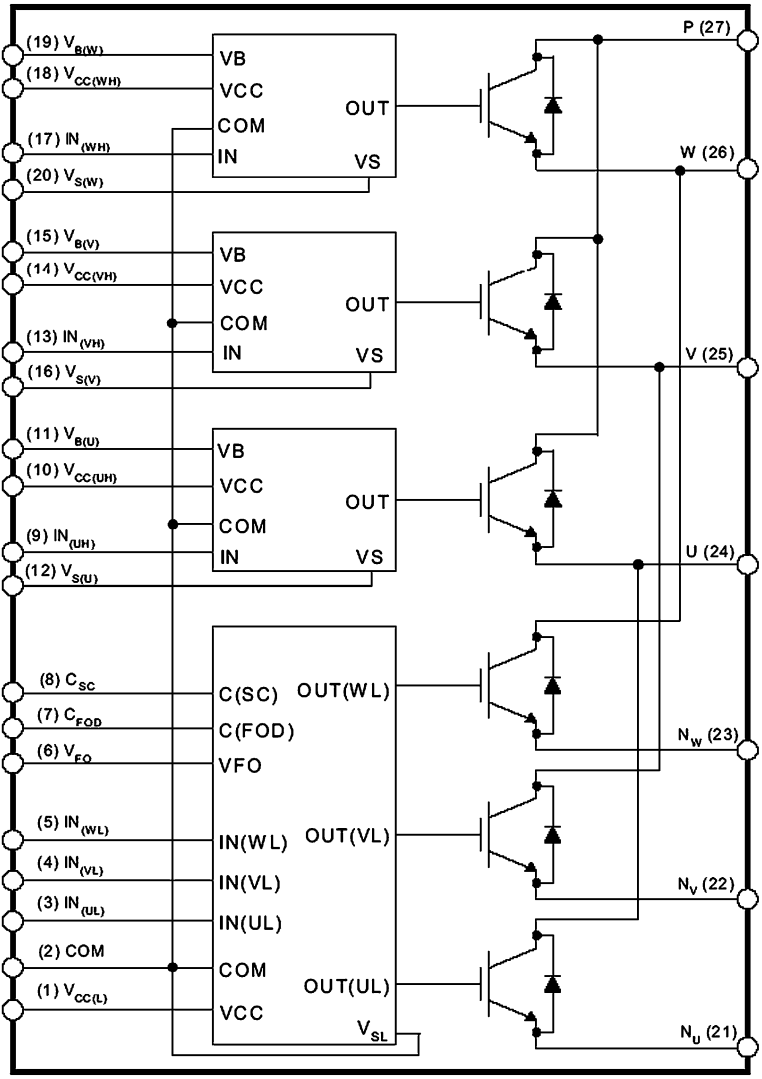


Fig. 5.26 Internal block diagram of the Motion-SPM product in mini-DIP package

(d) Heat sink mounting

There are two important factors in the heat sink mounting process that can significantly impact the quality of the SPM module for the heat transfer performance. One is the silicon grease and the other is the screw tightening torque. Apply silicon grease between the SPM and the heat sink to reduce the contact thermal resistance. Be sure to apply the coating thinly and evenly with a uniform layer of silicon grease (100–200 μm thickness) for the Motion-SPM module. Do not exceed the specified fastening torque. Overtightening

Table 5.1 Heat sink mounting torque rating

Item	Mounting condition	Minimum value	Typical value	Maximum value	Unit
Mounting torque	Recommended 0.59	0.49	0.59	0.69	Nm
Ceramic/DBC flatness	See Fig. 5.27	0	–	+120	μm
Heat sink flatness		−100		+50	μm
Weight			15.65		g

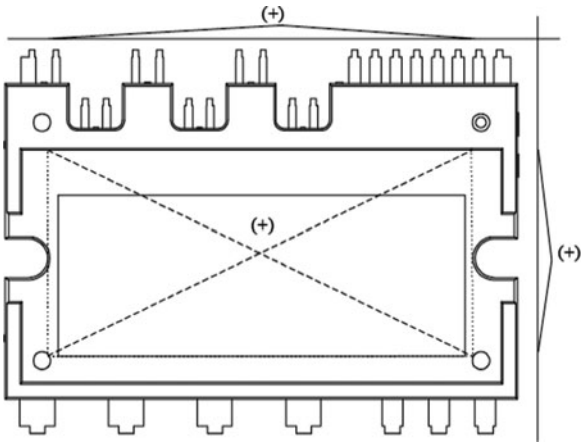


Fig. 5.27 Flatness effect in the heat sink mounting process

the screws may cause ceramic cracks, bolts, and AL heat-fin destruction. Tightening the screws beyond a certain torque can cause saturation of the contact thermal resistance. The tightening torques in Table 5.1 is recommended for obtaining the proper contact thermal resistance and avoiding the application of excessive stress to the device. Avoid stress due to tightening on one side only. Figure 5.27 shows the flatness information of the motion-SPM module in the mounting process. Uneven mounting can cause the SPM modules' ceramic substrate to crack.

5.1.2.2 Thermal-Mechanical Stress Analysis

It is important to understanding the impact of the design parameters on thermal-mechanical behaviors of the SPM [9, 10]. Below gives the simulation results for stress analysis with different solder materials and die attach thickness, as well as the effect of lead frame warpage on the IGBT die.

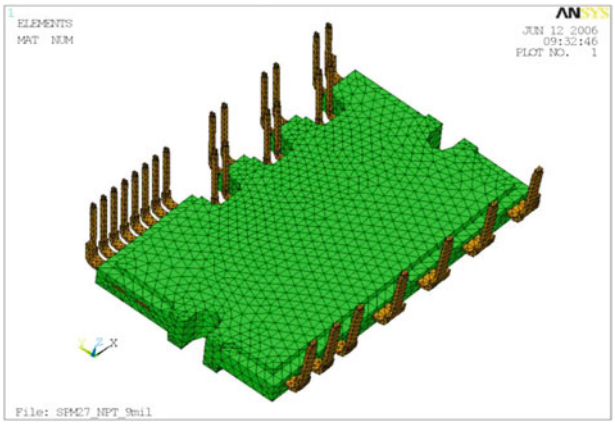


Fig. 5.28 The model of a typical Motion-SPM package

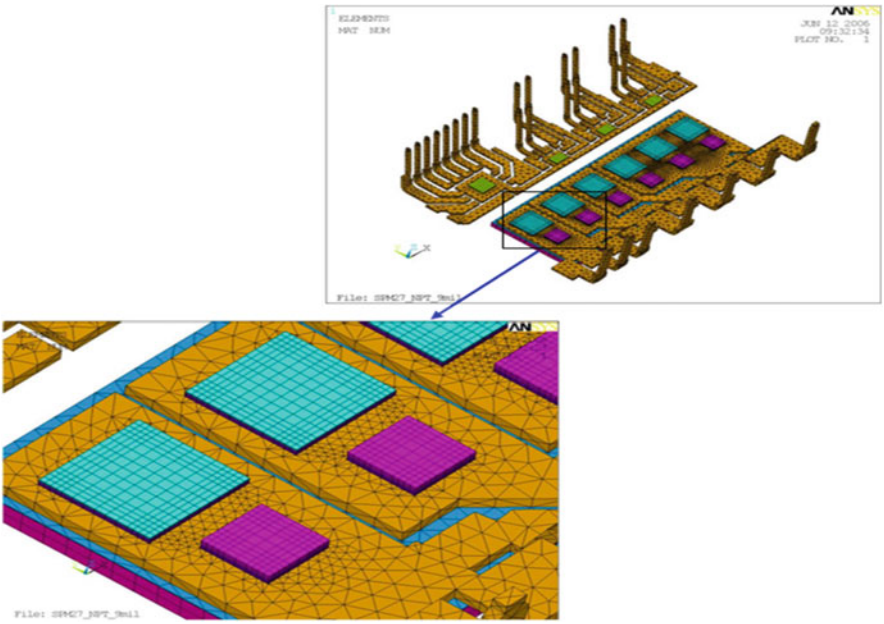


Fig. 5.29 The IGBT and FRD die attached on lead frame and the local mesh of the SPM module

1. The stress analysis in temperature cycle with different die attach thickness and solder materials
   Figure 5.28 shows the model of a typical Motion-SPM module, which is used to check the stresses in IGBT and FRD die with different solder materials and different die attach thicknesses. The temperature cycle applied this section is −40 to 125°C. Figure 5.29 shows the detail information of the mesh for

Table 5.2 The DoE scheme for the simulation

IGBT type	Die attach thickness (for IGBT and FRD dies) (mil)	Solder wire material
NPT	1	Pb88Sn10Ag2
NPT	1	Pb92.5Sn5Ag2.5
NPT	1	Pb97.5Sn1Ag1.5
NPT	3	Pb88Sn10Ag2
NPT	3	Pb92.5Sn5Ag2.5
NPT	3	Pb97.5Sn1Ag1.5
NPT	5	Pb88Sn10Ag2
NPT	5	Pb92.5Sn5Ag2.5
NPT	5	Pb97.5Sn1Ag1.5
NPT	7	Pb88Sn10Ag2
NPT	7	Pb92.5Sn5Ag2.5
NPT	7	Pb97.5Sn1Ag1.5
NPT	9	Pb88Sn10Ag2
NPT	9	Pb92.5Sn5Ag2.5
NPT	9	Pb97.5Sn1Ag1.5

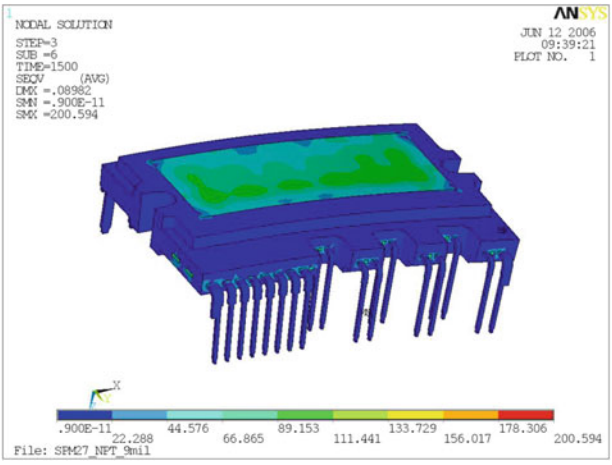


Fig. 5.30 The deformation and stress of a typical Motion-SPM module at −40°C of the temperature cycle

IGBT and FRD attached on lead frame, which are inside of the SPM module. Table 5.2 lists the simulation for DoE scheme for different die attach thickness and different die attach solder materials.

Figure 5.30 shows the overall von Mises stress and deformation of a typical Motion-SPM module at −40°C. Figure 5.31 shows the compressive third principal stresses of IGBT and FRD die at −40°C. Note that the maximum stress appears at the both die corners. Figure 5.32 gives the effective plastic strain of

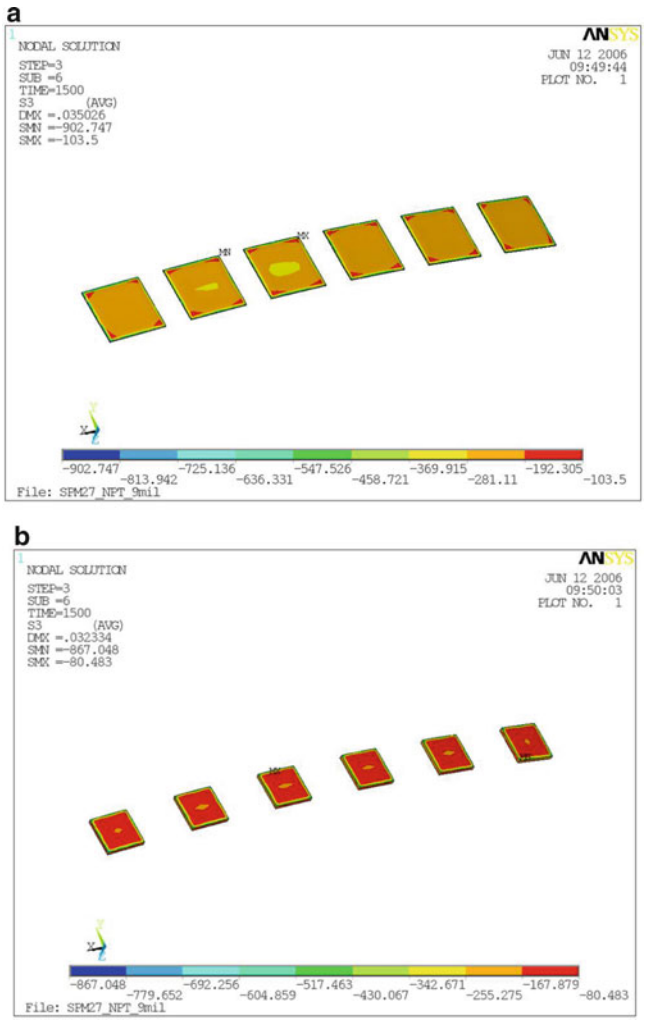


Fig. 5.31 The compressive stresses for IGBT and FRD at −40°C of the temperature cycle. (**a**) The compressive stress S3 of IGBT die. (**b**) The compressive stress S3 of the FRD die

the die attach solder material at −40°C; the maximum plastic strain under the FRD die is larger than the strain under the IGBT die.

Figure 5.33 gives the third principal (compressive) stress curves of the IBGT as the function of the die attach thickness with three different solder materials. It can be seen that as the die attach thickness increases, the stresses increase at beginning, and after the die attach thickness exceeds 3 mil, the stresses decrease. Figure 5.34 shows the compressive stress curves of FRD as the function of the die attach thickness with three different solder materials. As the die attach thickness increase, the stresses of FRD with the three solder materials decrease.

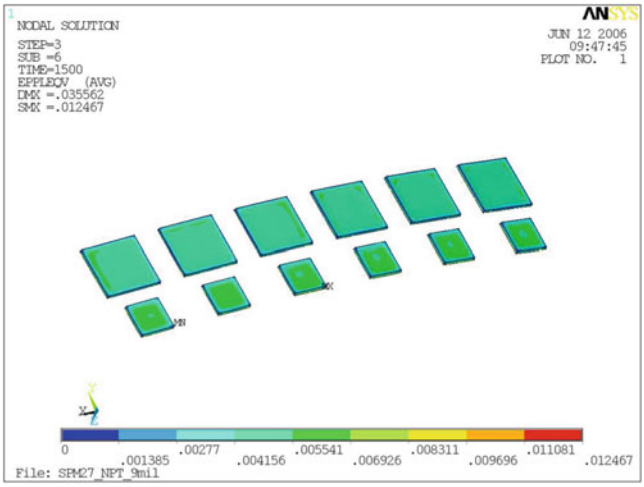


Fig. 5.32 The effective plastic strain at the die attach solder material (maximum appeared at corners)

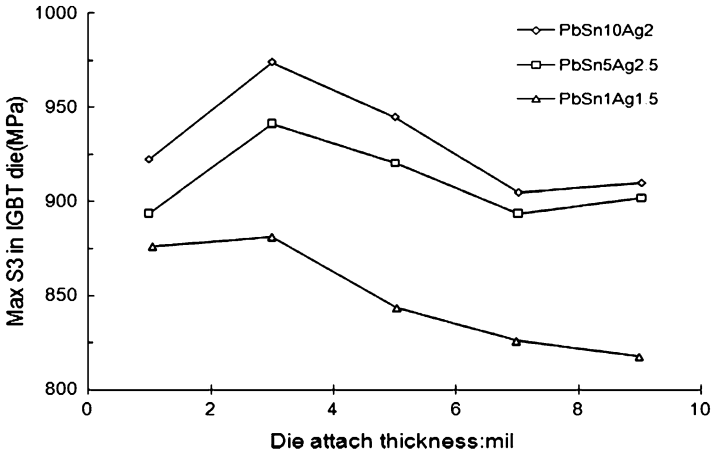


Fig. 5.33 The compressive stress of IGBT vs. die attach thickness with three solder materials

Figure 5.35 gives the effective plastic strains of the three solder materials vs. the die attach thickness. It shows that there is an optimized point at die attach thickness 5 mil, the maximum plastic strains are the lowest for the three solder materials. In all Figs. 5.33–5.35, the solder material PbSn1Ag1.5 gives the lowest compressive stress in IGBT, FRD and the lowest plastic strain in three die attach solder materials.

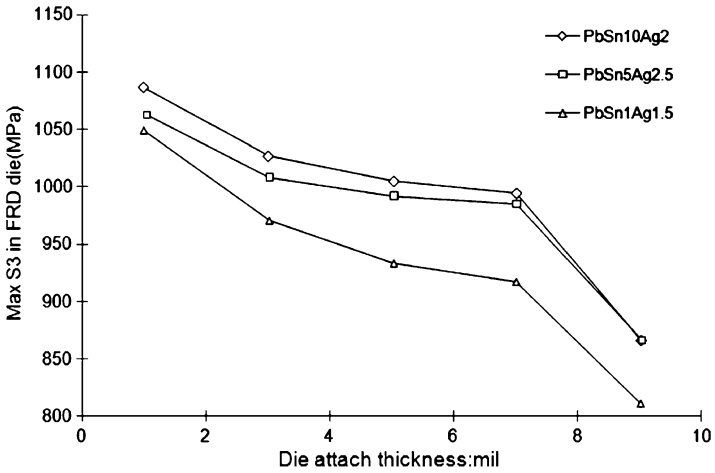


Fig. 5.34 The compressive stress of FRD vs. die attach thickness with three solder materials



Fig. 5.35 The maximum effective plastic strain in die attach solder vs. die attach thickness

2. The effect of warpage of lead frame dap on the IGBT die stress
   This section gives the impact of the warpage in the lead frame dap on the IGBT die stress. Figure 5.36a gives the picture of the clamp process in assembly for a convex warpage. There are two compressive pins. Due to the warpage of the dap, for a convex warpage the left pin stands for the #1 compressive pin and the right pin is for the #2 compressive pin which will contact the deformed lead frame

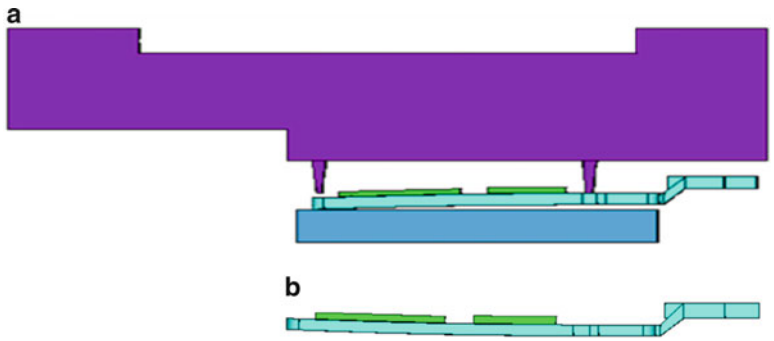


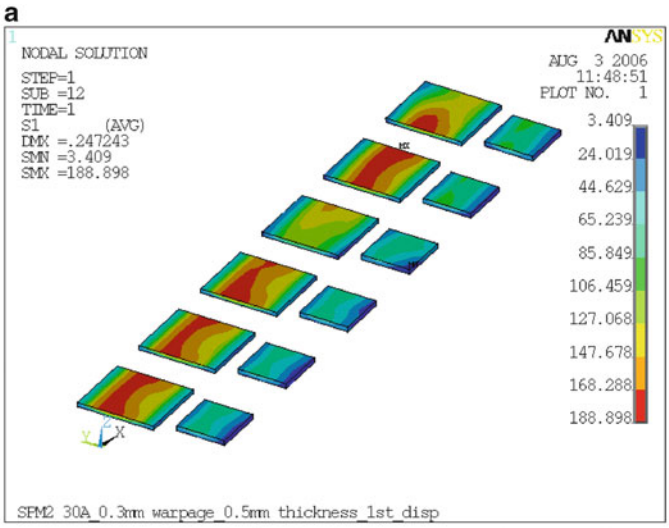
Fig. 5.36 The convex warpage of the lead frame dap (maximum: 0.3 mm). (**a**) The convex warpage of the lead frame dap. (**b**) The concave warpage of the lead frame dap

Table 5.3 The comparison of IGBT die tensile stress with convex and concave warpages, DAP thickness: 0.7 mm

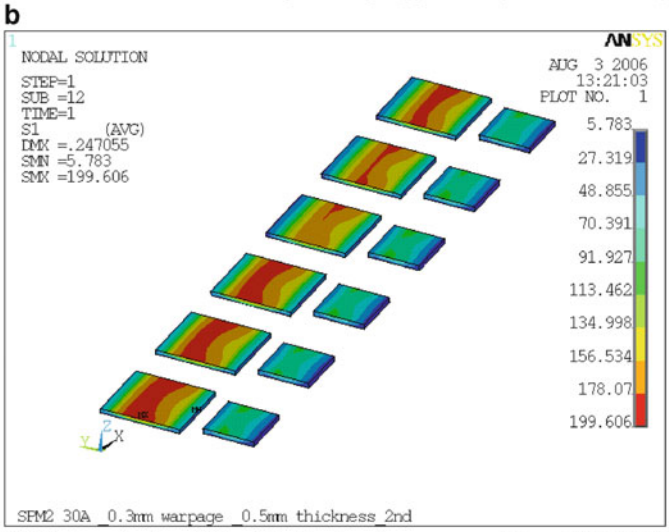
	Motion-SPM module	
	IGBT stress (MPa)	
DAP warpage (mm)	#1 Pin	#2 Pin
0.3 Concave warpage	229.1	233.3 (with #1 pin)
0.3 Convex warpage	30.8 (with #2 pin)	25.3

first. However, for a dap with the concave warpage, the #1 compressive pin will contact the dap first, follows by #2 compressive pin (see Fig. 5.36b). Table 5.3 lists the tensile stress comparison of IGBT die, it can be seen that the concave can induce much larger stress than convex warpage of the lead frame dap.

Figure 5.37 gives the IGBT die tensile stresses under the #1 and #2 pin clamping process due to the dap concave warpage 0.3 mm with 20 μm die attach thickness. The #2 pin has induced larger stress as compared to the #1 pin, since in this case, both #1 and #2 pins are applied. Table 5.4 list the comparison of the IGBT tensile stress with two different lead frame dap thickness. It may be seen that the thicker lead frame dap has induced the larger tensile stress at IGBT die. Table 5.5 shows the tensile stress comparison of IGBT die under concave warpage with different die attach thicknesses. From Table 5.5, we know that thicker die attach thickness helps to reduce the tensile stress in IGBT die during the clamping assembly process. Figure 5.38 shows the IGBT die tensile stress comparison with different DAP concave warpages for the 0.7 mm lead frame for 30 A SPM module, 0.5 mm for 15 A SPM module with 20 μm die attach thickness. It can be seen that the larger dap concave warpage has increased the IGBT die stress significantly.



IGBT stress due to the # 1 pin clamping pressure (max: 188.9 MPa)



IGBT stress due to add the # 2 pin clamping pressure (Max: 199.6 MPa)

Fig. 5.37 The first principal stress (tensile stress) of the IGBT due to the dap warpage 0.3 mm, DAP thickness 0.5 mm. (**a**) IGBT stress due to the #1 pin clamping pressure (maximum: 188.9 MPa). (**b**) IGBT stress due to the #2 pin clamping pressure (maximum: 199.6 MPa)

Table 5.4 The tensile stress comparison with two lead frame dap thickness for the concave warpage 0.3 mm

Die DAP thickness (mm)	Motion-SPM module IGBT stress (MPa)	
	#1 Pin	#1 and #2 Pins
0.7	229.1	233.3
0.5	188.9	199.6

Table 5.5 The tensile stress comparison with different die attach thickness for the concave warpage 0.3 mm

Die attach thickness (μm)	Motion-SPM module IGBT stress (MPa)	
	#1 Pin	#1 and #2 Pins
10	241.4	247.8
20	229.1	233.3
40	217.1	220.8

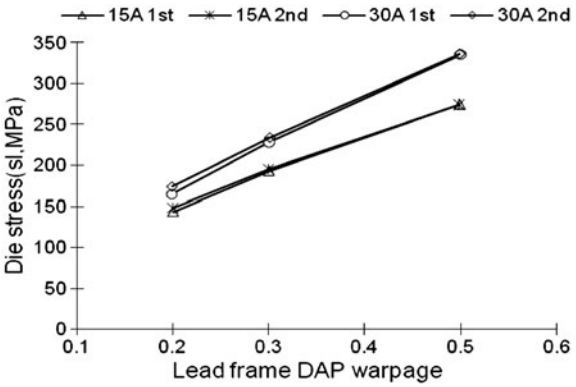


Fig. 5.38 The tensile stress comparison of IGBT die with different dap warpage (lead frame: 0.7 mm for 30 A, 0.5 mm for 15 A, die attach thickness 20 μm)

5.2 Power Stack Die System in Package

This section presents a power stack die package design for a POL buck converter. The buck converter system in package (SiP) consists of a LS MOSFET and a HS MOSFET together with an IC controller. Its structure includes a premolded lead frame with an IC controller. The two MOSFETs (both LS and HS) are stacked on the premolded lead frame (LF) and IC controller. Solder balls are placed on the lead frame's exposed lands, and together with the two drains of MOSFETs, to form the

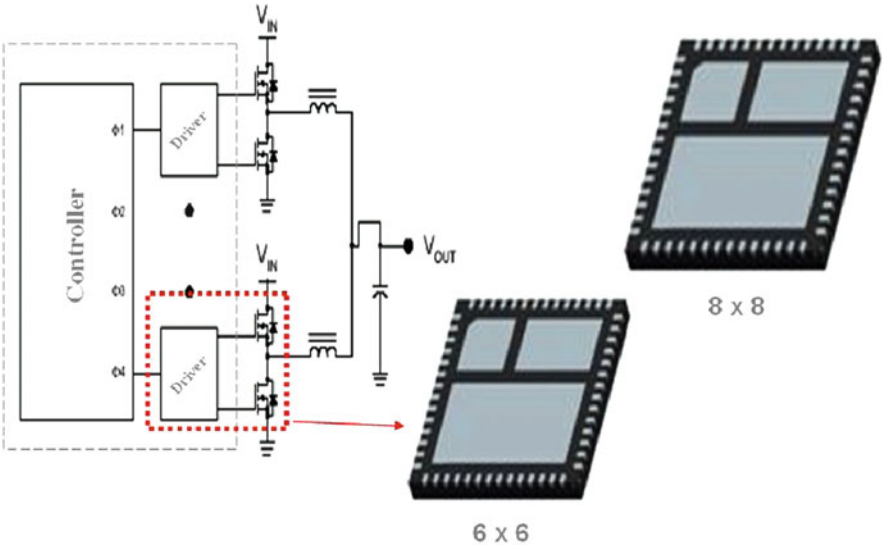


Fig. 5.39 A typical side by side SiP of DrMOS module

stacked die power package. The thermal cycling simulations for the solder balls to connect the PCB and solder joints of the two MOSFET die to the lead frame pads are studied. The failure mechanism and reliability analysis of the power package in TMCL test are discussed.

5.2.1 The Design Concept of the Power Stack Die SiP

In many power conversion and power management applications, the optimized semiconductor solution is a combination of lateral and vertical conduction devices. This makes a monolithic silicon solution combining the power switching (VDMOS/IGBT) and control functions (BCDMOS/CMOS IC) impractical. Therefore, the Power SiP becomes necessary [3, 4].

In power applications, the advantages of "SiP" includes reducing board level design complexity, smaller space for power delivery and control functions, and improved electrical performance through reduced parasitic effects in high-performance switching applications. One application of the power SiP is to expand ease of POL power regulation and management. Figure 5.39 shows a typical Fairchild driver MOSFET's SiP with three die for a POL switch integration with an IC controller, a HS MOSFET die and a LS MOSFET die, in which the three die are copackaged in a conventional QFP. Figure 5.40 shows the profile of power efficiency (%) vs. current load of such SiP in Fig. 5.39. It can be seen from the profile that the average efficiency of the SiP is about 2–4% higher than the individual MOSFET DPAK [1].

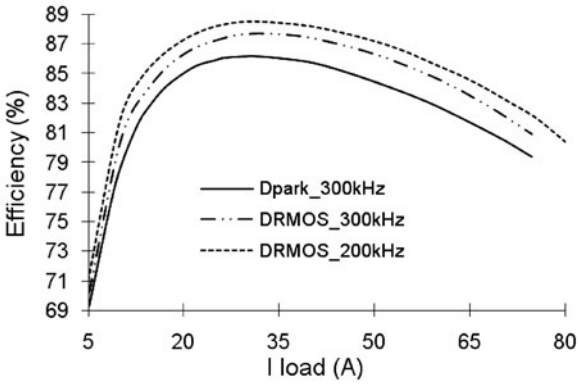


Fig. 5.40 Power efficiency (%) vs. current load (*I*) for single DPAK and DrMOS

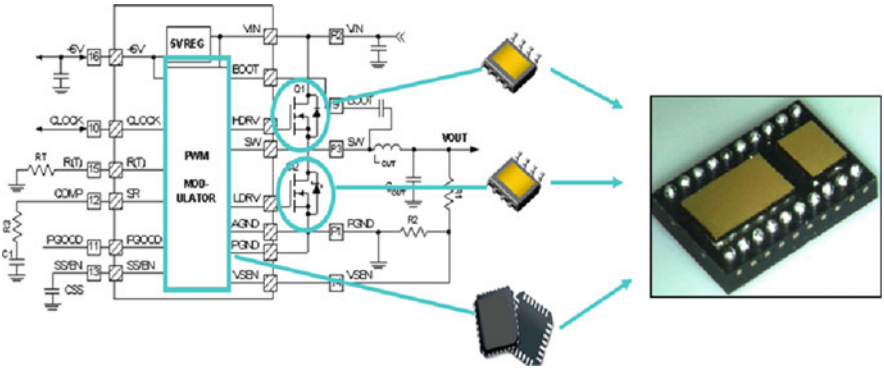


Fig. 5.41 The design concept of stack die power module

However, the above SiP with side-by-side placed die has certain drawbacks: its size is not as small as desired, and the electrical performance also needs further improvement. Reference [11] discussed the SiP of a voltage regulator with component side by side placement and the stacked SiP and found that the stacked SiP has 55% lower parasitic inductance than conventional SiP. This is particularly important for portable applications, and for small size industry applications.

The trend of the stacked power package is from simply enhancing one function to systematic function and multiple functions while reducing the board level complexity and space.

Stacked die package is quite common for analog, RF, digital, and memory products [4], but not so common for products in power electronics.

Figure 5.41 shows the design concept of a POL stack die buck converter. The circuit requires one LS MOSFET, one HS MOSFET and an IC controller. In regular

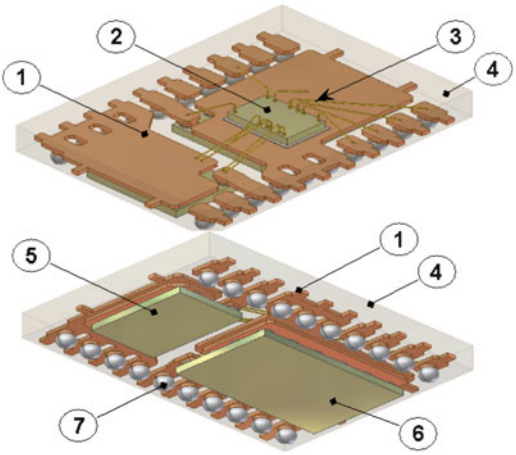


Fig. 5.42 Construction of the stack die power package

application, it needs three different packages for LS, HS, and IC as shown in Fig. 5.41. However, if we integrate the three die together with stack die, it not only can save the size and space of the application but also can improve the electrical performance such as the higher efficiency and lower parasitic inductance and resistance.

Figure 5.42 shows the construction layout of the stack die power package. It consists of seven components including: (1) lead frame, (2) IC controller chip, (3) Bond wire, (4) Mold compound, (5) HS MOSFET chip, (6) LS MOSFET chip, and (7) Solder ball.

Figure 5.43 shows the prototype and the cross section of the package which stacked the discrete power die on a premolded lead frame which includes the molded IC controller. From Figs. 5.42 and 5.43 it can be seen that the two bottom drains feature solderable surfaces which are mounted and soldered on the PCB as are the two rows solder bumps for the electrical pin outs. The two direct attaching MOSFET drains effectively dissipate the heat from the MOSFET die to PCB. Since the controller IC is molded into the package and the two MOSFET die are attached to exposed pads on the package's bottom, the size of the stacked die power module becomes significant smaller than the SiP in which three die are placed side by side. In addition, since the HS and LS MOSFETs are attached to two isolated exposed pads, the mold compound between the two pads acts to restrict thermal flow between them. The advantages of this power SiP layout are the smaller package size due to the stacked die technology and the high efficiency heat dissipation due to the direct attaching PCB of the two power MOSFET drains.

Figure 5.44 shows the major assembly process steps of the power stacked die package. The process includes the following: (1) the IC die attach on the lead frame; (2) wire bonding of IC controller to the controller pins of the lead frame; (3) to form the premolded structure that covered the IC controller and exposed the connection areas for the pin out and for stacking the two MOSFETs die; (4) solder paste printing

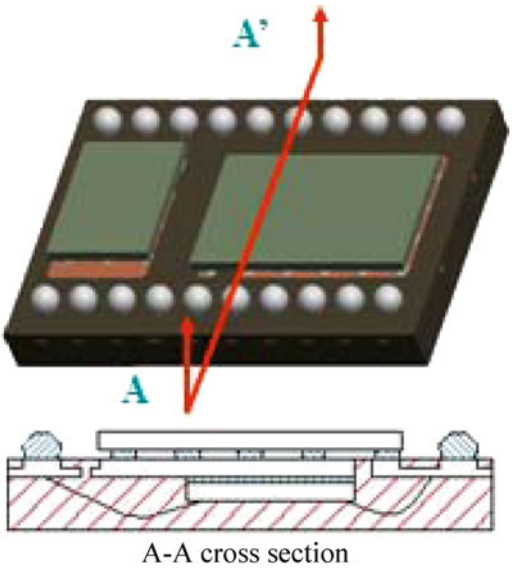


Fig. 5.43 The prototype and cross section of the stack die package

on the exposed lead frame for two MOSFET drains and gates, as well as for the bump pins out; (5) two MOSFETs die solder attached to the premolded and exposed lead frame; (6) solder ball mounting on the pads of the two rows of the bump pads.

5.2.2 TMCL Solder Joint Reliability Analysis

One of the major reliability tests for the new concept product is the thermal cycling to check the failure mode and the solder joint reliability. The stacked power SiP (showed in Fig. 5.43) investigated by the author has two levels of the solder joint interconnect. One is the board level solder joint connect in which the solder bumps and solder paste of MOSFET drain are attached to the PCB. The other is the package level solder joint interconnects in which the two MOSFET sources and gates are attached to the exposed pads of premolded lead frame.

To investigate the thermal-mechanical stress, failure modes and the solder joint life during thermal cycling, a 3D finite element model for the stacked die power module is built as shown in Fig. 5.45. Figure 5.45a gives the model of power SiP mounted on PCB; Fig. 5.45b shows the detail mesh of the SiP; Fig. 5.45c lists the model and meshes of the two levels solder joint interconnects. Two solder materials are applied to the system. One is the Pb-free solder 95.5Sn3.8Ag0.7Cu (SAC387) and the other is the 95Sn5Sb.

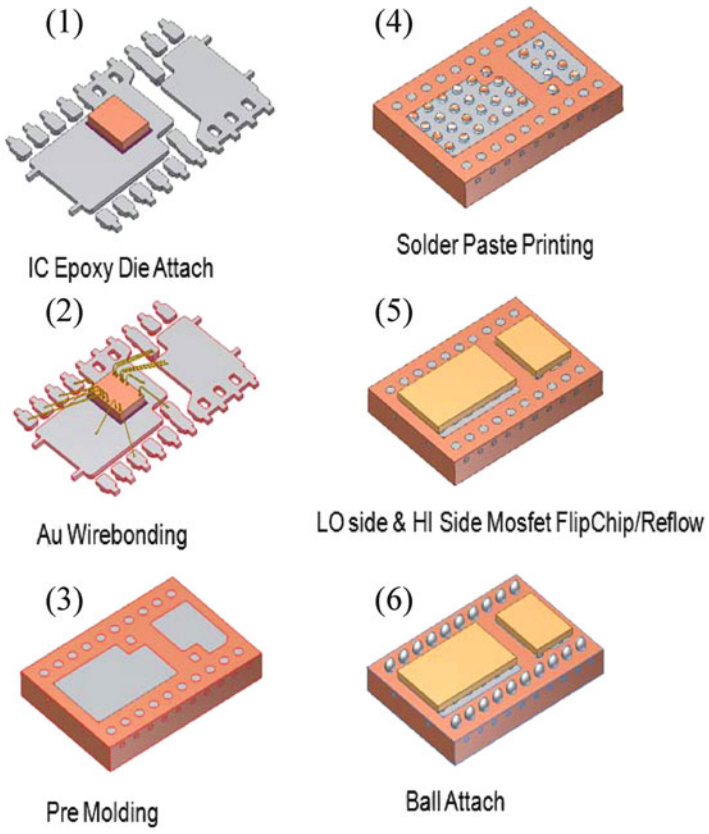


Fig. 5.44 Assembly process of the power stacked die package [12]

The nonlinear material properties of SAC387 are listed in Table 5.6. Its Young's modulus is 48.5 GPa at room temperature, and its coefficient of thermal expansion (CTE) is 21.9 ppm. The solder paste 95Sn/5Sb is a bilinear material. Its Young's modulus is 41.6 GPa at room temperature, its CTE is 25 ppm, its yield stress is 41 MPa, and the tangent module is 410 MPa at room temperature. Its yield stress and tangent modulus are 25 and 250 MPa, respectively, at 100°C.

The solder joints character life prediction formula for the stack die power package system is based on the element volume averaged energy method [12]

$$N_0 = K_1 \Delta W_{\text{ave}}^{K_2}$$

$$\frac{da}{dN} = K_3 \Delta W_{\text{ave}}^{K_4} \quad \text{where} \quad \Delta W_{\text{ave}} = \frac{\sum \Delta W \cdot V}{\sum V} \tag{5.8}$$

$$\alpha_w = N_0 + N$$

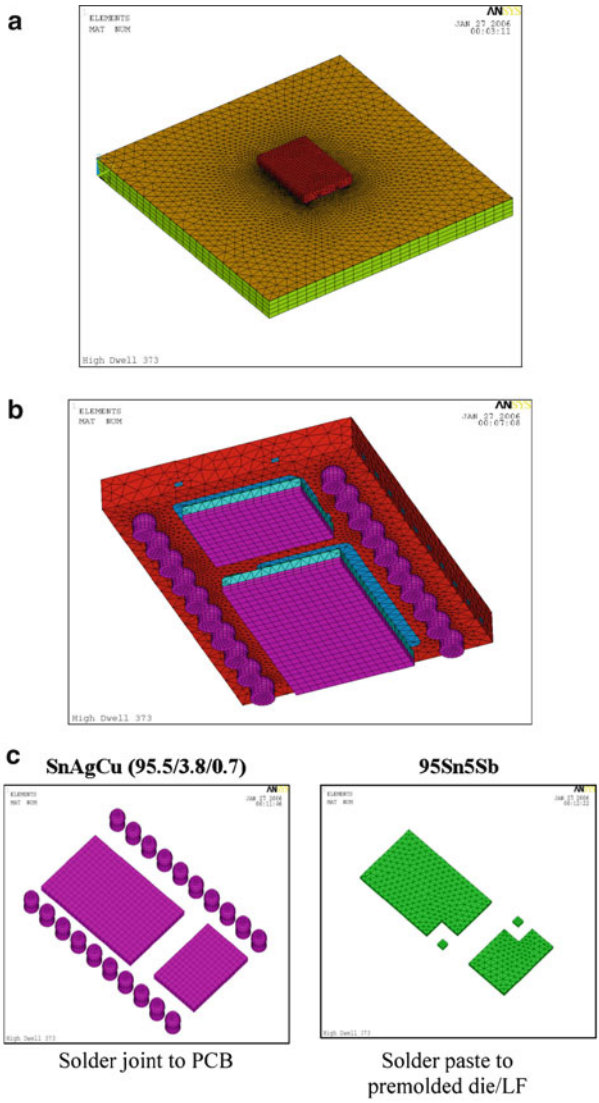


Fig. 5.45 The FEA model and mesh [12]. (**a**) The stack die power module amounted on printed circuit board (PCB). (**b**) The FEA mesh for package. (**c**) The two level solder joints

The α_w is the character thermal cycling life; the coefficients K_1, K_2, K_3, and K_4 are selected as 56,300, −1.62, 3.34e − 7, and 1.04, respectively, based on the element geometry and thickness.

The first failure life N may also be predicted by the 3-parameter Weibull distribution,

Table 5.6 ANAND model parameters for SAC387 [12]

Description	Symbol	SAC387
Preexponential factor	A (1/s)	107.65
Activation energy	Q/R (K)	7,619
Stress multiplier	ξ	59.36
Strain rate sensitivity of stress	m	4.03
Coefficient for deformation resistance saturation value	$\hat{s}$ (MPa)	86.28
Strain rate sensitivity of saturation value	n	0.0046
Hardening coefficient	h_0 (MPa)	9,002
Strain rate sensitivity of hardening coefficient	a	1.3
Initial value of s	s_0 (MPa)	22.64

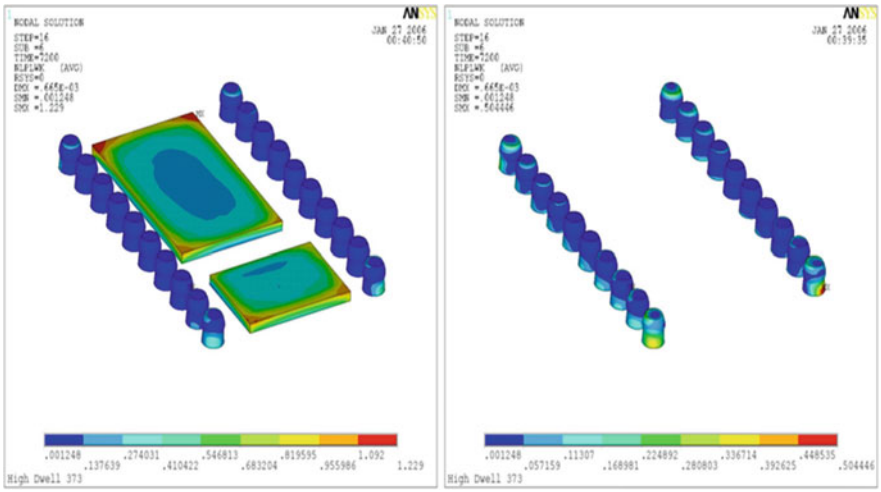


Fig. 5.46 Plastic energy density distribution of the board level solder joint (maximum: 1.2 MPa)

$$N = N_{\mathrm{ff}} + (\alpha_w - N_{\mathrm{ff}})(-\ln(1-F))^{(1/\beta_w)} \tag{5.9}$$

where $N_{\mathrm{ff}} = \alpha_w/2$, $F = 0.7/(S_{\mathrm{s}} + 0.4)$, β_w is the shape parameter, the typical value is 2.6. The S_{s} is the sample size and typical number is 32.

The temperature cycle is from the range of 0 to 100°C within 30 min/cycle. The thermal cycling simulation for the power SiP package is completed through finite element software ANSYS®. Figures 5.46–5.49 [12] show the board level solder joint stress and plastic energy density distribution. From these figures it can be seen that the weakest solder joints are located at the corner positions. Although the center solder paste corner has shown the maximum plastic energy density, the size of center paste is larger enough to resist the failure compared to the corner solder bumps.

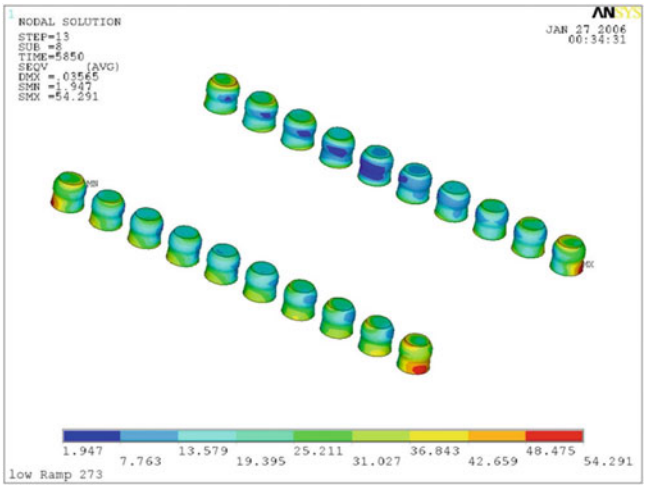


Fig. 5.47 Maximum von Mises stress of the board level solder joint in corner location at 0°C (maximum stress: 54.3 MPa)

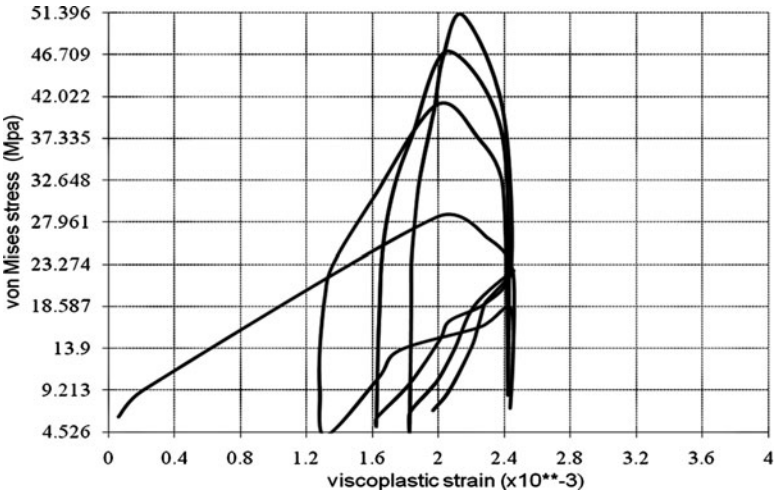


Fig. 5.48 The maximum cycling von Mises stress vs. strain

Figures 5.48 and 5.49 show the cycling curves of von Mises and shear stress vs. strain, indicating the maximum cycling stress and strain range for the board level solder joints.

Figures 5.50 and 5.51 [12] describes the plastic energy density distribution and the von Mises stress distribution of the package level solder joints. Compared to board level solder joint stress, the package level solder maximum stress appears at

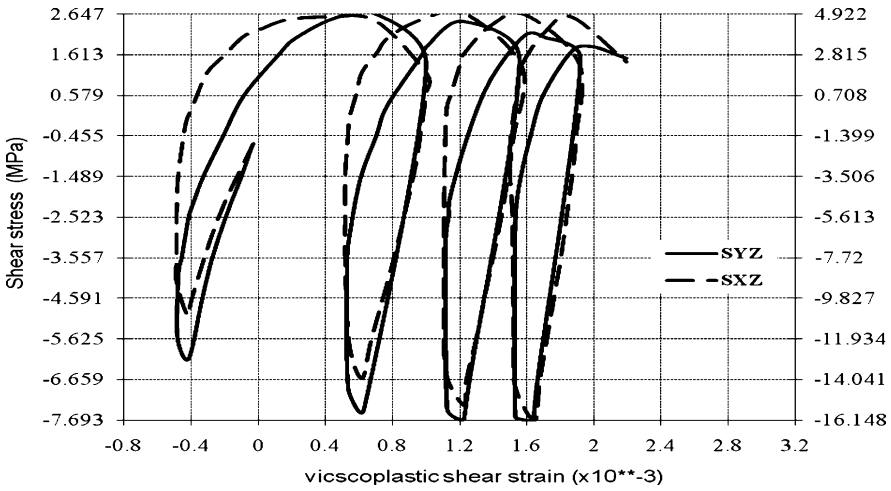


Fig. 5.49 The cycling of maximum shear stress vs. shear strain

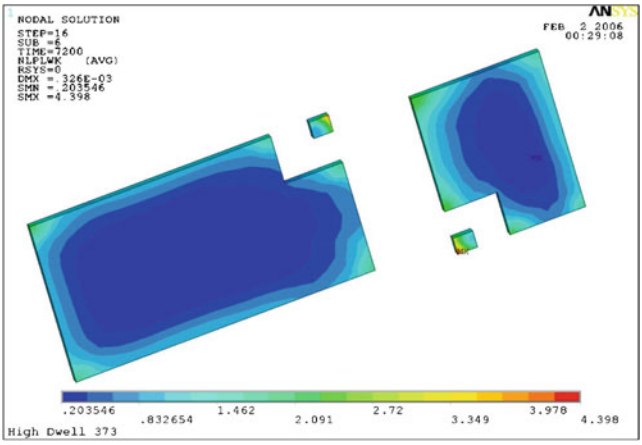


Fig. 5.50 Plastic energy density of the package level solder paste (maximum: 4.4 MPa)

the gate solder joint. Its maximum plastic energy density is about 3.7 times greater than the board level solder joint and its maximum von Mises stress is about 1.44 times greater than the board level solder joint.

Figures 5.52 and 5.53 [12] show the cycling curves of the von Mises stress and shear stress vs. strain which listed the stress and strain range on the package level at the gate.

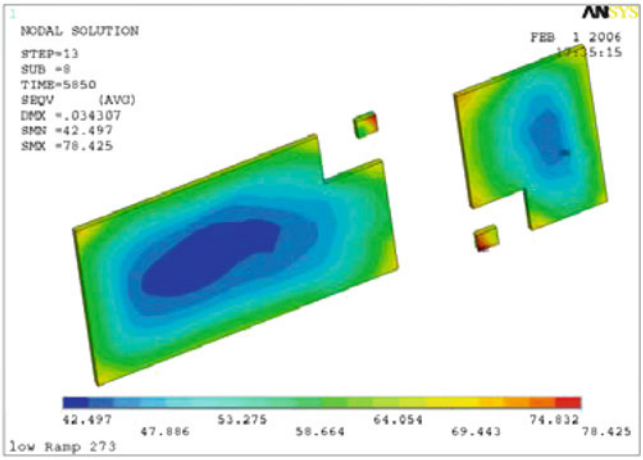


Fig. 5.51 von Mises stress distribution of the package level solder paste at 0°C (maximum: 78.4 MPa)

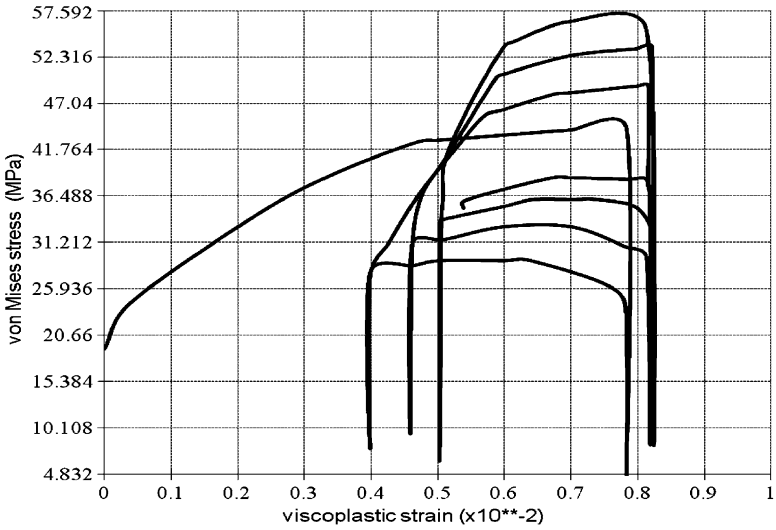


Fig. 5.52 The cycling maximum von Mises stress vs. strain of the package level solder paste (it is actually located at gate joint)

Table 5.7 lists the TMCL life prediction for both the board and package levels, it can be seen that the board level TMCL life is much longer than the package level (about 46 times greater).

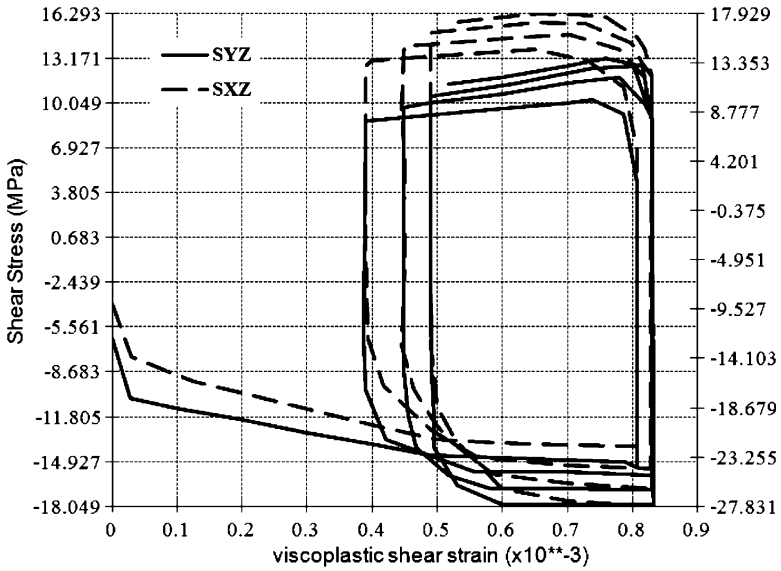


Fig. 5.53 The cycling maximum shear stress vs. shear strain of the package level solder paste

Table 5.7 TMCL life prediction [12]

Solder joint type	Character life	First failure
Board level	15,219	9,357
Package level	419	258

5.2.3 Failure Analysis of the Power Module

The failure analysis is conducted after a TMCL test. The test has gone through over 1,000 cycles. The results showed that the board level solder joint experienced no failure while the package level solder joints have been seen cracks at the gate solder joints after 100 cycles (see Figs. 5.54 and 5.55; [12]) and both gate and source cracks after 500 cycles. Especially the gate joint solder of lower side MOSFET has been fully broken (Fig. 5.56).

The Failure analysis is consist with the modeling trend that has shown the package level solder joints has larger stress and therefore has short TMCL life. When the TMCL test was checked after 100 cycles cracks appeared on gate and after 500 cycles cracks on both gate joints and other joints in the package level were observed.

There is some difference between the FEA model and the TMCL test. In the model, the package level solder joint is assumed as the uniform solder layer, while in TMCL the two MOSFET die used the copper stud bump die to attach on the solder pasted exposed lead frame. The simulation does not include the copper stud

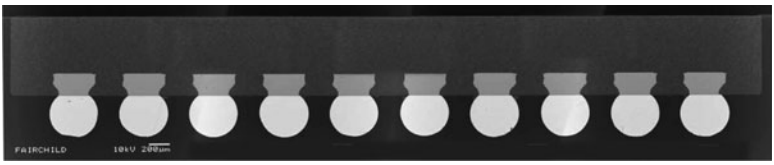


Fig. 5.54 No crack found for the board level solder joint after 1,000 cycles

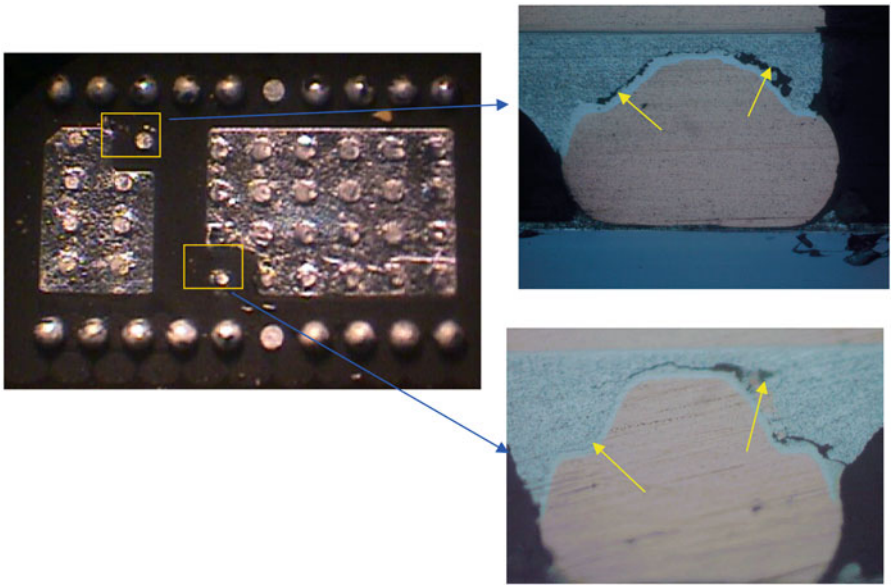


Fig. 5.55 Cracks have been seen in the gate solder joints in package level after 100 cycles

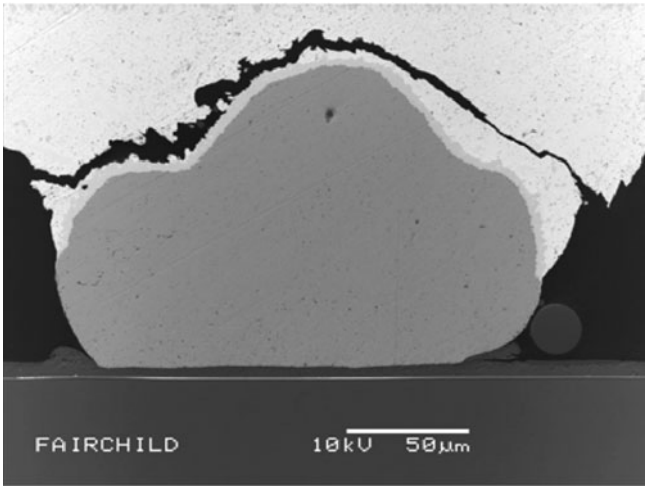


Fig. 5.56 The crack at LS Mosfet gate solder in the package level joint after 500 cycles [12]

bumping in the modeling, which might induce some difference between the modeling and the test results. However, the trends of the package level gate solder joint in the two MOSFET die will fail first are the same for both the modeling and the test. One of the root causes for the crack at the package level in the test could be the CTE mismatch between copper (16 ppm) and the solder paste (25 ppm). If the bumps use the solder material or the designer chose a solder paste with similar CTE of copper, it would be much better. However, the both modeling test data have shown that solder joint life in MOSFET package level is very small. This is possibly due to the thickness of the solder joint in both test and modeling being very thin (within 1 mil); however, if the solder joint height is made higher (example is larger than 4 mil), the TMCL life will get significant improvement.

5.2.4 Discussion

This section introduces a stacked die design concept of the buck converter SiP, simulation, and reliability analysis. This new SiP package has smaller size for the portable application that integrates three die into one system as compared to the similar product with die side by side placement buck converter. The package has the advantage of high efficiency heat dissipation due to the two drains of MOSFETs directly attaching on PCB. The simulation and TMCL test has shown that the board level solder joints have excellent reliability behavior while the package level solder joint reliability needs to be improved either through selection of similar CTE mismatch solder materials or to increase the solder joint height of the MOSFET die at the package level.

5.3 Wafer Level Power Stack Die 3D Package with TSV

This section relates to the wafer level power stack die concept with through silicon via (TSV), and more particularly to wafer level stack die synchronous buck converters.

Synchronous buck converters, primarily used in stepdown power supply circuits, typically include two switching field effect transistors (FETs) and a series inductor to permit digital, rather than analog, control of the FETs which either supply current into the inductor or draw current back from the inductor, as shown in Fig. 5.57. Compared to analog power supplies, the synchronous buck converter with FET switching transistors are small and use very little overhead current. Thus, they are often used for mobile electronic devices. Since space is an important consideration in such devices, the size of synchronous buck converters is important in the marketplace. The wafer level stack die 3D package with TSV technology is an effective approach to realize the smaller package size and at the same time to keep the smaller thickness (Fig. 5.58).

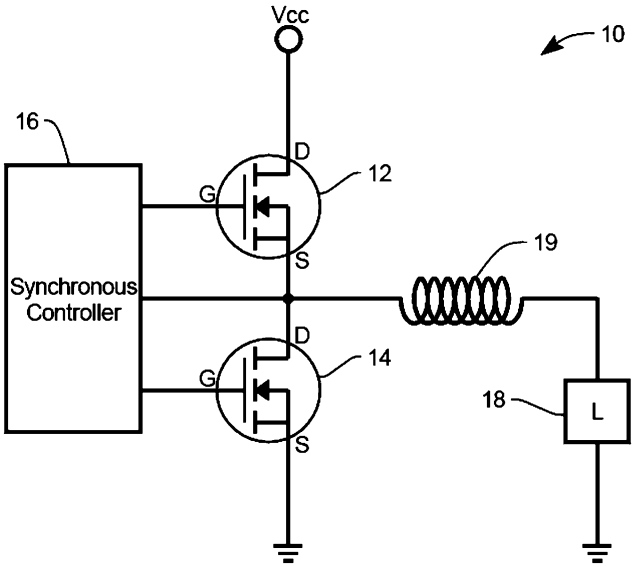


Fig. 5.57 A circuitry of synchronous buck converter

Due to large mismatch in coefficients of thermal expansion between the copper via and the silicon with TSVs, significant thermal stresses will be induced at the interfaces of copper/dielectric layer (usually SiO_2) and dielectric layer/silicon when TSV structure is subjected to subsequent assembly temperature loadings, which would influence the reliability and the electrical performance of interconnects. Thus section discusses the design concept of the wafer level power stack die package with TSV, thermal loading, and the impact of thermal-mechanical stress on the design variable of the package during the assembly process.

5.3.1 The Design Concept of the Wafer Level Power Stack Die Package

The design concept comprises, in one form thereof, a wafer level buck converter with stack die 3D package including a HS MOSFET die having source, drain, and gate bonding pads on a front side of the HS die, a LS MOSFET die with a plurality of TSVs extending from a back side to a front side of the LS die, the LS die having source, drain, and gate bonding pads located on the front side, the drain bonding pad electrically connected to the back side of the LS die. The HS die and the LS die are bonded together such that the source bonding pad with Cu stud bumps of the HS die is electrically connected to the drain of the back side LS die through anisotropic conductive film (ACF), and each of the drain and gate bonding pads of HS die are electrically connected to separate TSVs in the LS die. Figure 5.58a shows such

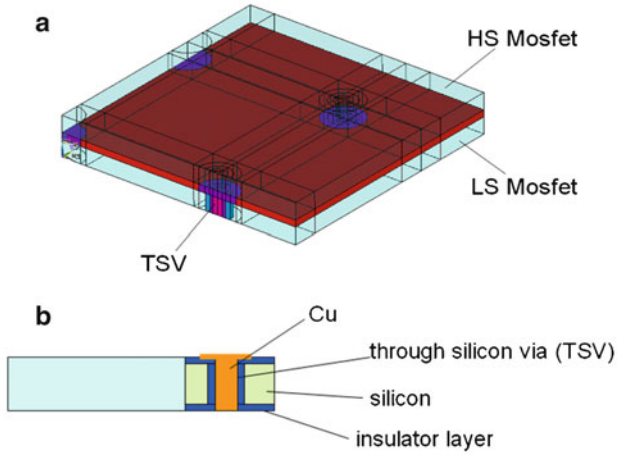


Fig. 5.58 The concept of wafer level buck converter with stack die 3D through silicon via (TSV) technology. (**a**) The concept of wafer level buck converter in a quarter model. (**b**) TSV at LS die

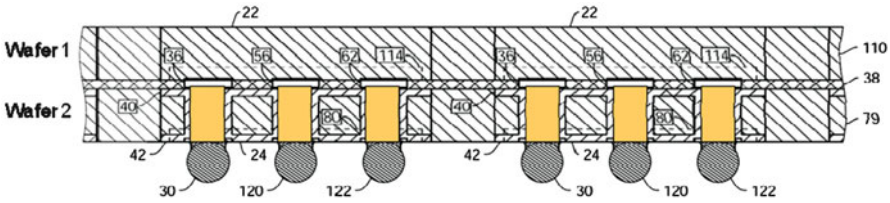


Fig. 5.59 The cross section of the wafer level buck converter with two stacked wafers before singulation (wafer1 for HS and wafer2 for LS)

concept in a quarter model, in which the TSV is filled with conductive polymer and Fig. 5.58b gives the Copper TSV structure layout. Figure 5.59 shows the cross section of the wafer level buck converters with HS wafer (wafer1) stacked on LS wafer (wafer2) before the singulation.

5.3.2 Thermal Analysis

The thermal analysis for the wafer level power stack die package through simulation is introduced in this section. The package is mounted on a JEDEC 1s0p board with $76.2 \times 114.3 \times 1.6$ mm^3 and with PCB vias. Assume natural convention is applied in the simulation. Figure 5.60 gives the quarter model of the stack die package and the system with PCB. The package size is $1.5 \times 1.5 \times 0.12$ mm^2. Figure 5.61a gives the temperature distribution of the system including both stacked die and PCB with an input power 0.1 W on HS MOSFET die. Figure 5.61b shows

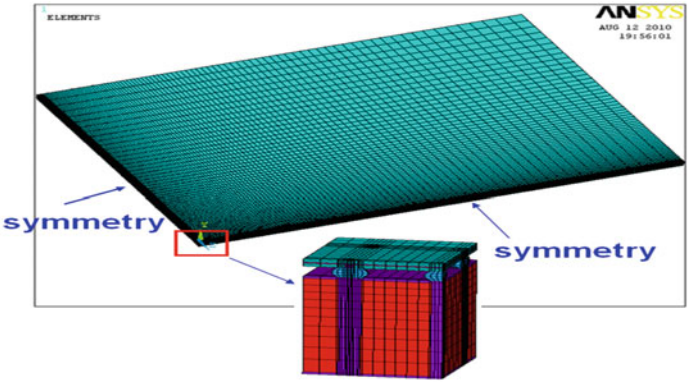


Fig. 5.60 The quarter model of the wafer level buck converter on JEDEC 1s0p PCB with vias

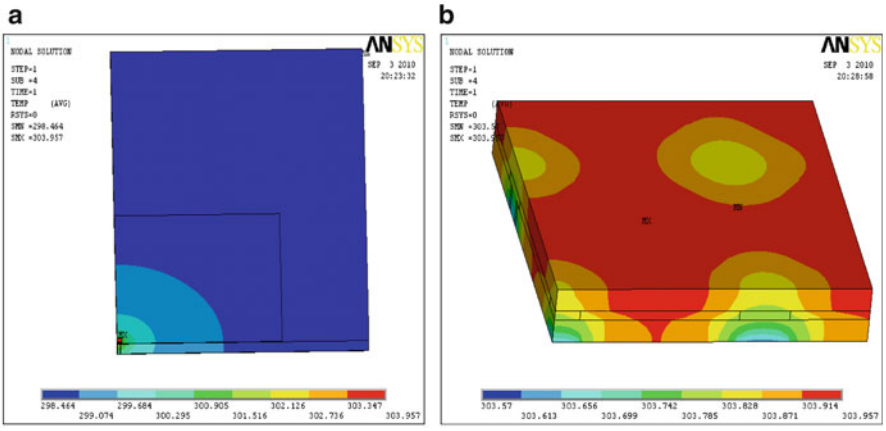


Fig. 5.61 The temperature distribution when the power (0.1 W) applied to the HS die, maximum temperature: 304 K. (**a**) The temperature of both PCB and die. (**b**) The temperature distribution on the stack die package

Table 5.8 Thermal resistance of junction to ambient vs. the die size under natural convention and the input power is 0.1 W

Die size (mm^2)	$R\theta_{JA11}$ (°C/W)	$R\theta_{JA12}$ (°C/W)	$R\theta_{JA21}$ (°C/W)	$R\theta_{JA22}$ (°C/W)
1.2 × 1.2	60.85	60.5	60.28	60.57
1.3 × 1.3	60.29	59.99	59.79	60.05
1.4 × 1.4	59.89	59.64	59.46	59.69
1.5 × 1.5	59.57	59.35	59.2	59.4

the temperature distribution of the stacked die package. Table 5.8 lists the thermal resistance $R\theta_{JA}$ junction to the ambient varies with the different die sizes, in which the table includes the coupling thermal effects. $R\theta_{JA11}$ is the thermal resistance of HS die due to the power is applied on the HS die; $R\theta_{JA12}$ is the thermal resistance of

Table 5.9 Thermal resistance of junction to ambient vs. the TSV diameter under natural convention and the input power is 0.1 W

TSV diameter (μm)	$R\theta_{JA11}$ (°C/W)	$R\theta_{JA12}$ (°C/W)	$R\theta_{JA21}$ (°C/W)	$R\theta_{JA22}$ (°C/W)
20	59.49	59.26	59.11	59.31
40	59.56	59.34	59.19	59.39
50	59.57	59.35	59.2	59.40
60	59.58	59.36	59.21	59.41

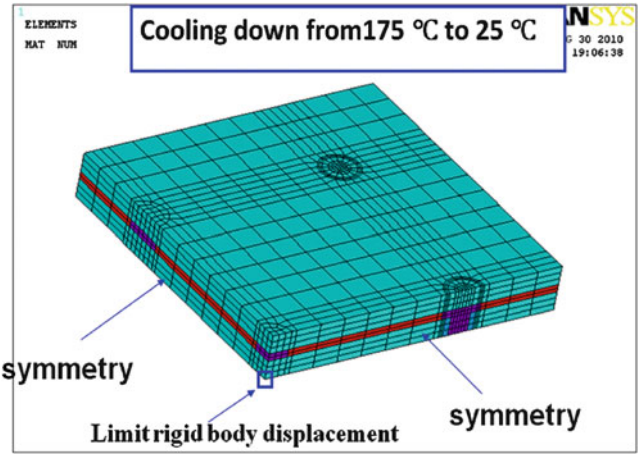


Fig. 5.62 The quarter model of the stack die power package

LS die due to the power is applied on the HS die; $R\theta_{JA21}$ is the thermal resistance of HS die due to the power is applied on the LS die; $R\theta_{JA22}$ is the thermal resistance of LS die due to the power is applied on the LS die; From Table 5.8, it can be seen that the thermal resistance of the stack die power package decreases slightly as the die size increases. Table 5.9 lists the thermal resistance of the wafer level power package under the impact of different diameter of TSV. The result does not show significantly changes. From both the Tables 5.8 and 5.9, it can be seen that the wafer level stack die power package has excellent thermal performance with low thermal resistance.

5.3.3 Stress Analysis in Assembly Process

There are two major assembly processes in the stack die power package. One is the cooling stress after thermally compressing and stacking HS with metal (copper or gold) stud bumping on the lower side through ACF. The other is the reflow process to mount the wafer level stack die power package on the PCB. This section gives the stress analysis in the two assembly processes with key design parameter variables.

Table 5.10 Material properties

Material	Copper	Silicon	SiO_2	Parylene	Epoxy	ACF
Young's modulus (GPa)	127.7	131.0	60.1	3.2	3.0	3.56 at 223 K 2.76 at 298 K 1.52 at 423 K 1.44 at 523 K
Poisson ratio	0.34	0.28	0.16	0.4	0.4	0.35
CTE (ppm/K)	17.1	2.8	0.6	35	65	74 at 223 K 75 at 268 K 100 at 278 K 109 at 283 K 119 at 288 K 143 at 298 K 144 at 473 K

5.3.3.1 Residual Stress After Stacking High Side Die on Low Side Die

Stacking the HS die to LS die is completed through thermally compressing and curing of ACF. Assume that the curing temperature of ACF is at 175°C, in which the stress is free. After stacking HS die on LS die, the system will cool down from to room temperature (Fig. 5.62).

Finite element method has been used for insight into the state of stresses and reliability of TSV by some authors. A "physics-of-failure" based approach, using experimental methods for material characterization and test as well as finite element simulations, was used to characterize thermo-mechanical stresses of TSV by Ramm et al. [13]. The study on the effect of via size on thermal mismatch and possible cracking due to loading force during the stacking process was carried out by Tanaka et al. [14]. The state of stresses and the accumulated effect of the local thermal mismatch in individual TSVs, resulting in global mismatch between the interposer and chip, was analyzed by Selvanayagam et al. [15]. Table 5.10 gives the material mechanical properties. It can be seen that the larger CTE mismatch between SiO_2 and the Copper of the TSV. The conventional dielectric layer SiO_2 will induce larger stress mismatch at the interfaces of copper/SiO_2 as well as the interface of silicon/SiO_2. As a solution, a modified TSV was proposed. The thin SiO_2 dielectric layer is replaced by a thick polymer isolation layer Parylene, which has significantly reduced the thermal-mismatch stress (see the work by Chen et al. [16]). In this section, the material Parylene is introduced as the isolation layer of TSV in the stack die power package. Conformal copper plating is used to realize the connection and the remaining hole in the copper via is filled with epoxy polymer material.

Figure 5.63 shows the tensile stress (the first principal stress S1) and the compressive stress (the third principal stress S3) of the wafer level power packaging after the HS MOSFET die thermally stacking on the LS MOSFET die. The maximum tensile stress appears at the interface between Copper TSV and its isolation. The maximum compressive stress appears at the copper stud bumping which is right above the TSV copper. Figure 5.64 shows the compressive stresses

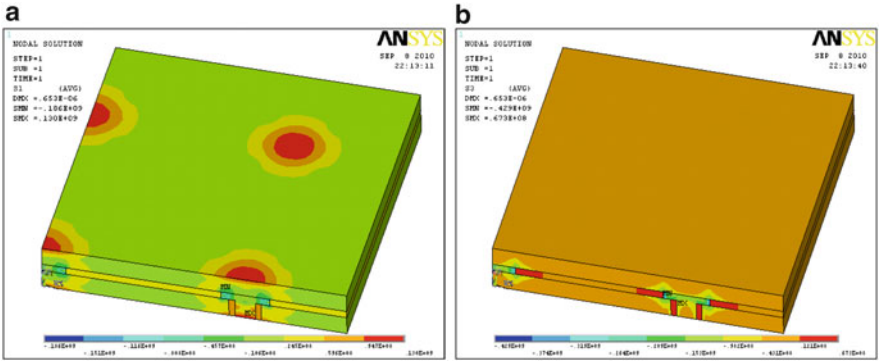


Fig. 5.63 The principal stress of the stack die power package at 25°C after the stacking process. (**a**) The first principal stress S1 (tensile) maximum: 130 MPa. (**b**) The third principal stress S3 (compressive) maximum: 429 MPa

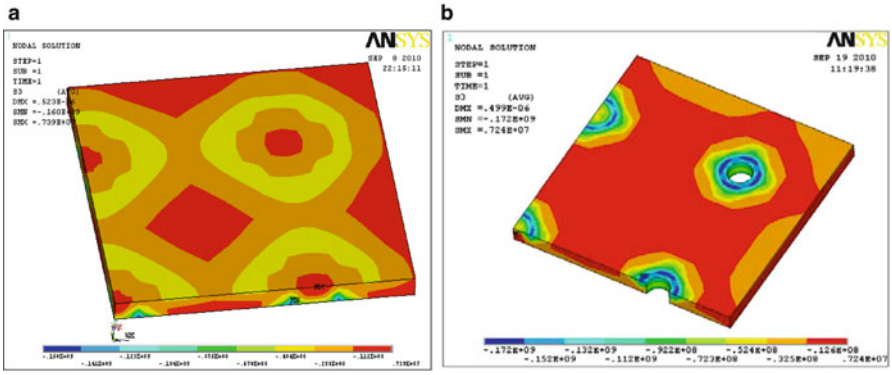


Fig. 5.64 The compressive stress at HS and LS die after the stacking process. (**a**) Compressive stress S3 on HS die (maximum: 160 MPa). (**b**) Compressive stress S3 on LS die (maximum: 172 MPa)

(the third principal stress S3) for the HS die and LS die. Both maximum stress happen at the TSV areas. Those compressive stresses are much lower than silicon compressive strength. Figure 5.65 shows the stress distributions for Copper stud bumpings, TSV copper, TSV isolation layer, and the ACF layer. It can be seen from the Fig. 5.65 that the Copper stud bumping withstands the highest von Mises stress at the TSV location after the HS die stacking on the LS die. In the TSV Copper, there also appears the larger stress at the junction with Copper stud bumping. The maximum tensile stress of the TSV isolation layer appears at the interface with TSV Copper near the junction with Copper stud bumping. The maximum von Mises stress of ACF layer appears at the corner TSV location at the interface with the Copper Stud. Therefore, the maximum stress of the wafer level stack die power

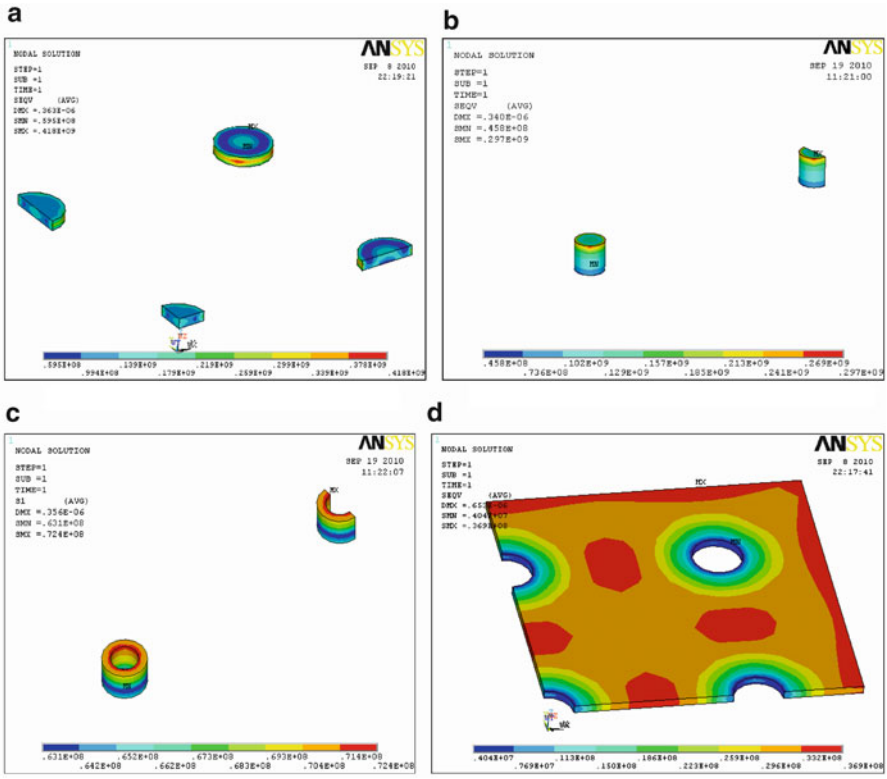


Fig. 5.65 The stress distribution of the copper stud bump, TSV/isolation, and the anisotropic conductive film (ACF) layer after the stacking die process. (**a**) von Mises stress of the copper stud bump (maximum: 418 MPa). (**b**) von Mises stress of the copper TSV (maximum: 297 MPa). (**c**) The tensile stress of the isolation layer (maximum: 72.4 MPa). (**d**) von Mises stress of the ACF layer (maximum: 36.9 MPa)

package is related to the TSV design, location and its materials. Figure 5.66 has shown that the compressive stress S3 of HS die and LS die, von Mises stresses of TSV copper, Copper stud bumping, ACF layer and the tensile stress S1 of the isolation layer vary as the design parameter of TSV diameter after stacking the HS die on the LS die. The TSV diameter has significantly impact on stress of the HS and LS die, Copper stud bumping, TSV copper. As the TSV diameter increases, it can significantly reduce the von Mises stress inside TSV Copper, while there are no significant changes in ACF layer and the TSV isolation layer. However, increasing the TSV diameter may induce the higher von Mises stress in Copper stud bumping, compressive stress S3 in HS and LS die.

Figure 5.67 shows the compressive stress S3 of HS die and LS die, von Mises stresses of TSV copper, Copper stud bumping, the tensile stress S1 of the isolation, and the von Mises stress of ACF layer vs. the thickness of ACF layer after stacking the HS MOSFET die on the LS MOSFET die. As the ACF layer thickness increases,

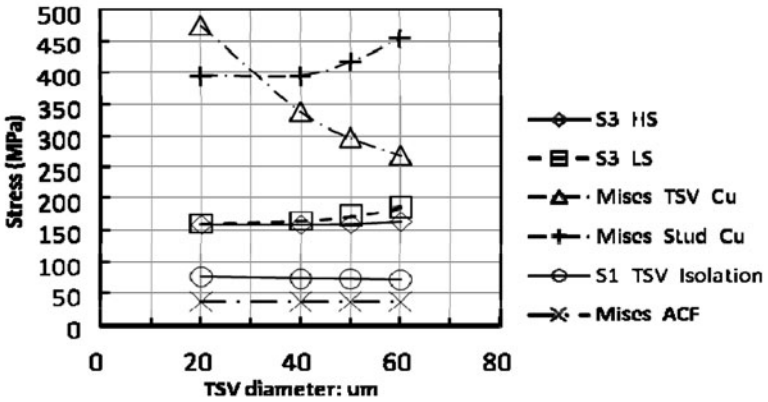


Fig. 5.66 The stresses of HS, LS, Cu stud, TSV Cu, ACF, and isolation layer vs. TSV diameter

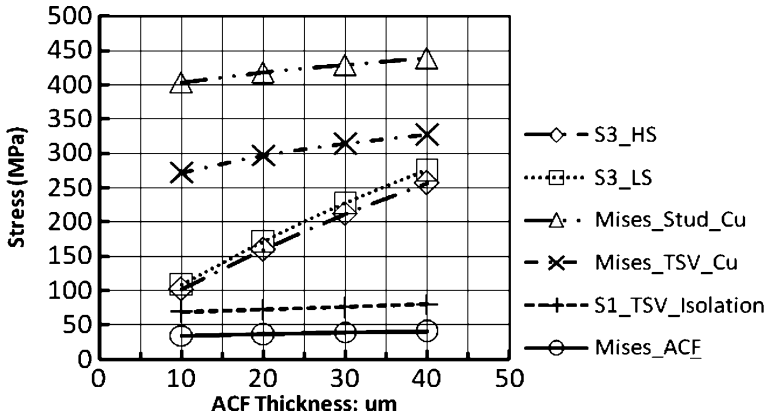


Fig. 5.67 The stresses HS, LS, Cu stud, TSV Cu, isolation layer and ACF layer vs. ACF thickness

all the stresses increase, which includes the von Mises stress of ACF layer. Especially, it can significantly increase the third principal stresses in HS and LS die, as well as the von Mises stress of Copper stud and TSV Copper. This indicate that for the thick ACF with Copper stud bumping, it will induce greater stress in the stacking process.

Figure 5.68 shows the compressive stress S3 of HS die and LS die, von Mises stresses of TSV copper, Copper stud bumping, the tensile stress S1 of the isolation, and the von Mises stress of ACF layer vs. the thickness of HS die. As the HS die thickness increases, the compressive stress S3 of HS die decreases and becomes stable after the HS die thickness exceeds 80 μm. All the rest stresses in LS die and TSV increase. The stresses in TSV isolation and ACF layer do not show significant

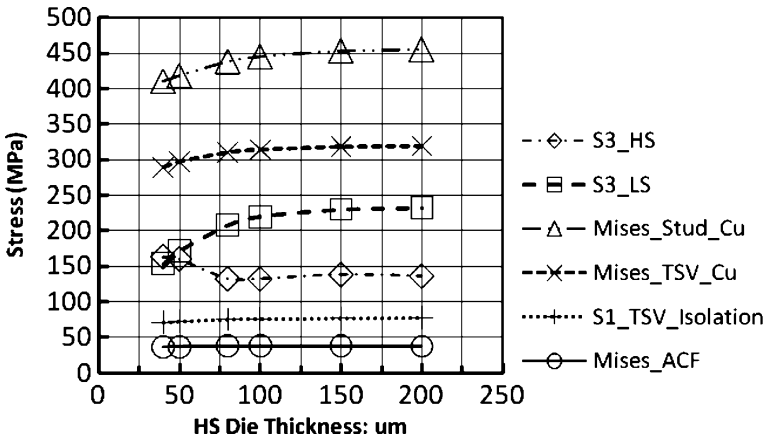


Fig. 5.68 The stresses HS, LS, Cu stud, TSV Cu, isolation layer and ACF layer vs. HS die thickness

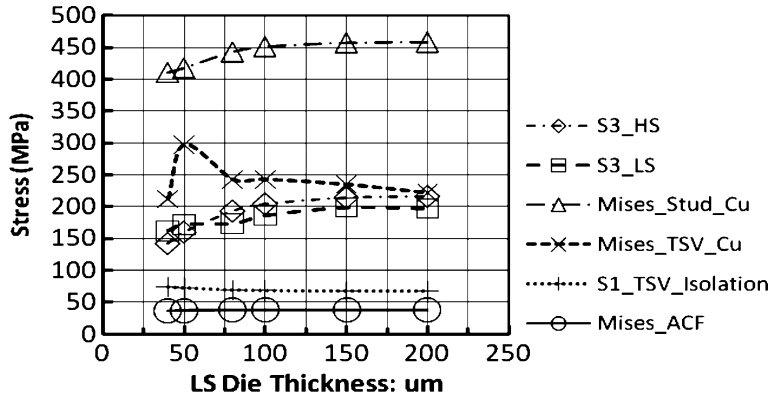


Fig. 5.69 The stresses HS, LS, Cu stud, TSV Cu, isolation layer and ACF layer vs. LS die thickness

changes, while the stress in TSV isolation layer seems to have slight increment. Figure 5.69 has shown that the compressive stress S3 of HS die and LS die, von Mises stresses of TSV copper, Copper stud bumping, the tensile stress S1 of the isolation, and the von Mises stress of ACF layer vs. the thickness of LS die. As the LS die thickness increases, the compressive stress S3 of both HS and LS die, as well as von Mises stress of Copper stud increase and becomes stable after the LS die thickness is larger than 150 μm. The von Mises stress of TSV copper sharply increases at beginning, then immediately decreases as the LS die thickness increases. The tensile stress S1 of the TSV isolation decreases slightly and becomes stable after the LS die thickness exceeds 100 μm. The von Mises stress of ACF layer is almost no change.

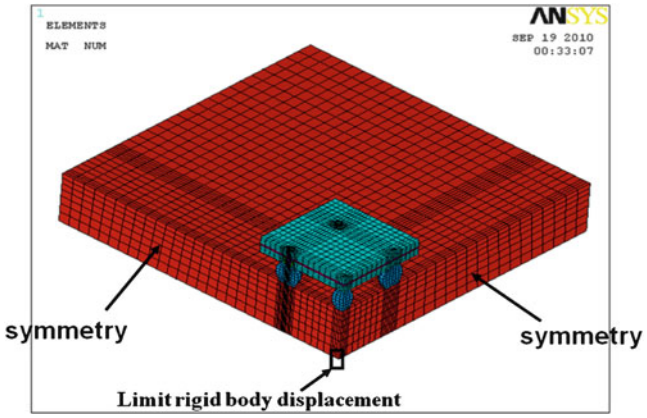


Fig. 5.70 The quarter model of the wafer level power stack die package mounted on a PCB

Table 5.11 The material properties of solder and PCB

Material	Solder ball	PCB
Young's modulus (GPa)	75.8–0.152*T*	EX: 25.4
		EY: 11
		EZ: 25.4
Poisson ratio	0.35	XY: 0.39
		YZ: 0.39
		XZ: 0.11
CTE (ppm/K)	24.5	XZ: 16
		Y: 84

5.3.3.2 Reflow Stress Analysis

Reflow process is used for mounting the wafer level stack die power package on a PCB. At this process, the solder joints in the wafer level stacking die power package are connected to the PCB through 260°C, which will induce high stresses inside the package as well as the solder joints. At the same time, the changes of material properties due to such high temperature are also the challenges in the reflow process (Fig. 5.70). Tables 5.11 and 5.12 list the solder 95.7Sn3.8Ag0.5Cu (SAC385) and PCB material properties. In Table 5.12, the viscoplastic behavior of the solder at high temperature is described by ANAND material model. All the properties of other materials are listed in Table 5.10.

In reflow process, most of the system are subjected to tensile stress. Therefore, the tensile stresses of the HS die and LSD die are checked. Figure 5.71 shows the first principal stresses (tensile) of HS die and LS die. The maximum stress appears at the TSV area. The tensile stress of LS die is larger than the HS die. Both tensile stresses of HS and LS die are within the range of the tensile strength of silicon.

Table 5.12 The viscoplastic property of solder at reflow

Description	Symbol	Units	SnAgCu385
Initial value of s	s_0	MPa	16.31
Activation energy	Q/R	K	13,982
Preexponential factor	A	1/s	49,601
Stress multiplier	ξ	–	13
Strain rate sensitivity of stress	m	–	0.36
Hardening coefficient	h_0	MPa	8.0e − 5
Coefficient for deformation resistance saturation value	$\hat{s}$	MPa	34.71
Strain rate sensitivity of saturation value	n	–	0.02
Strain rate sensitivity of hardening coefficient	a	–	2.18

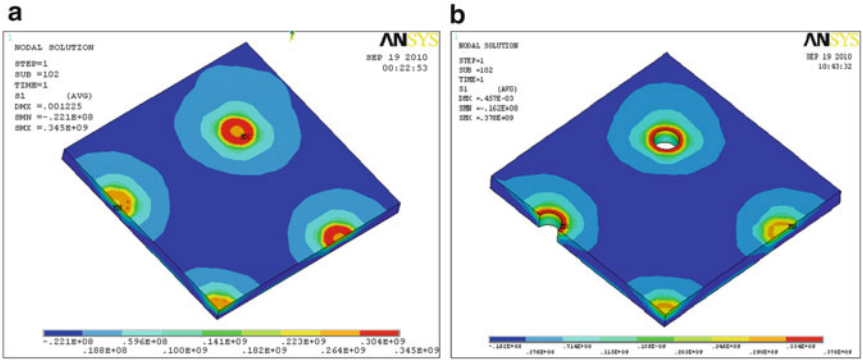


Fig. 5.71 The tensile stress S1 of HS and LS die at reflow. (**a**) The tensile stress S1 of the HS die at reflow (maximum: 345 MPa). (**b**) The tensile stress S1 of the LS die at reflow (maximum: 378 MPa)

Figure 5.72 shows the von Mises stress of the copper stud bumping and the ACF layer at reflow. The maximum stress (939 MPa) of Copper stud bumping appears at the corner bump of which the TSV is underneath. The Copper stud bumping stress is the highest inside the wafer level stacking die power package, while the von Mises stress of the ACF layer is the very low at reflow. Figure 5.73 gives the von Mises stress of the Copper TSV and the compressive stress S3 of isolation layer at reflow. The maximum stress of Copper TSV appears at the corner of die and at the interface that connects to the solder bumping, while the maximum compressive stress (S3) of the isolation layer appears at the interface of the Copper stud bumping. Figure 5.74 shows that the von Mises stress and the plastic energy density of the solder joints at the reflow. Both the maximum von Mises stress and maximum plastic energy density happen at the corner joint. Figure 5.75 lists the stress distribution of TSV filled with Epoxy. The design concept of TSV filled with epoxy is to reduce the stress in the TSV and the power stacking die package. Figure 5.75a shows the von Mises stress of the TSV epoxy core; Fig. 5.75b

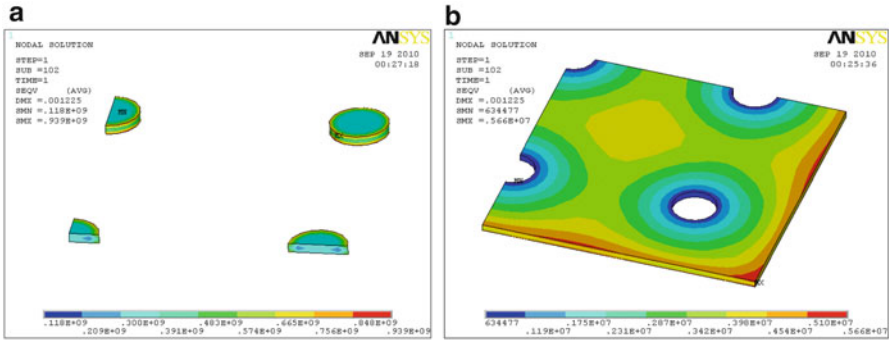


Fig. 5.72 The von Mises stress of Cu stud and the ACF layer at reflow. (**a**) The von Mises stress of Cu stud (maximum: 939 MPa). (**b**) The von Mises stress of ACF layer (maximum: 5.66 MPa)

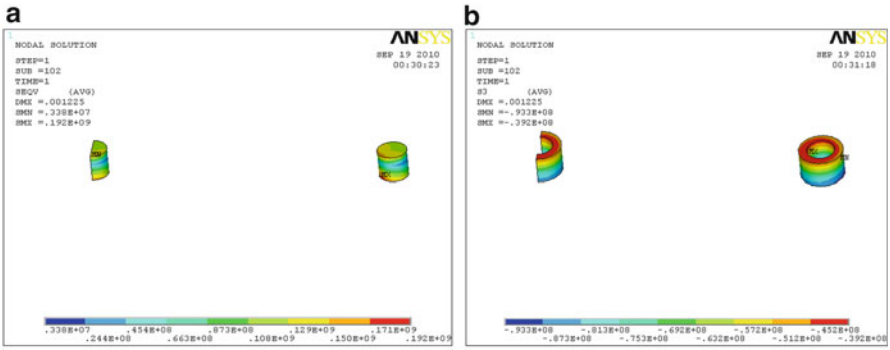


Fig. 5.73 The reflow stresses of TSV in Copper and isolation layer. (**a**) The von Mises stress of TSV Cu (maximum: 192 MPa). (**b**) The compressive stress S3 of isolation layer (maximum: 93.3 MPa)

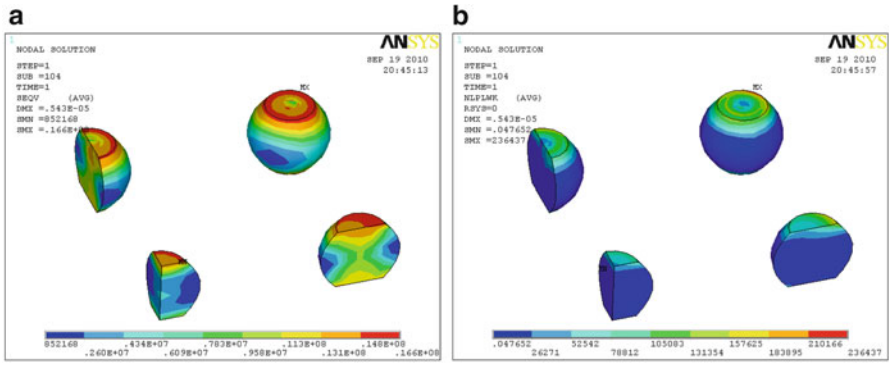


Fig. 5.74 The von Mises stress and plastic energy of solder balls at reflow. (**a**) The von Mises stress of solder bump (maximum: 16.6 MPa). (**b**) The plastic energy density of solder bump (maximum: 0.236 MPa)

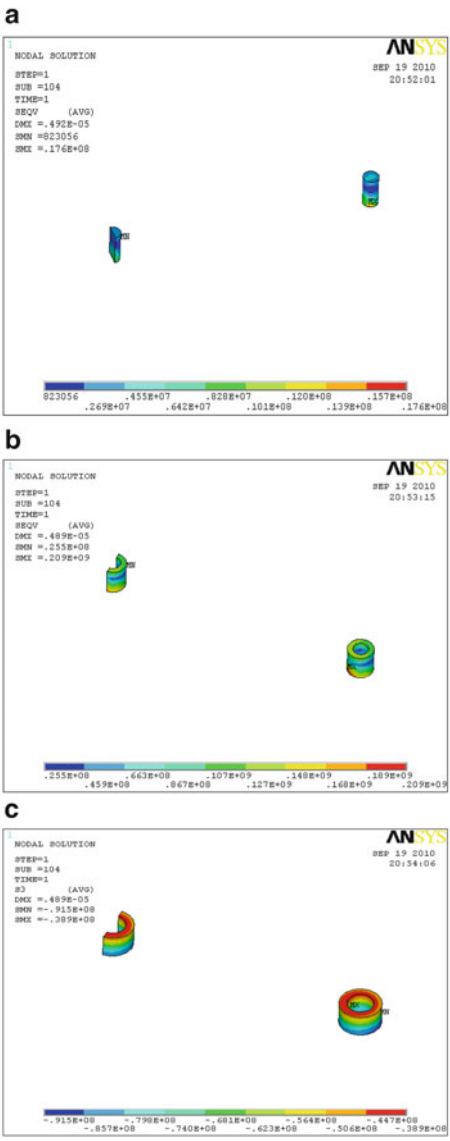


Fig. 5.75 The stress distribution of TSV filled with epoxy at reflow. (**a**) The von Mises stress of epoxy core in TSV (maximum: 17.6 MPa). (**b**) The von Mises stress of TSV copper (maximum: 209 MPa). (**c**) The compressive stress S3 of isolation layer (maximum: 91.5 MPa)

shows the von Mises stress of TSV Copper; Fig. 5.75c shows the compressive stress of the TSV isolation layer. As compared to the full copper TSV case (Fig. 5.73) and the TSV cooper with filled Epoxy core, the von Mises stress of TSV Copper slightly increases and the compressive stress S3 of the isolation layer is slightly decreases.

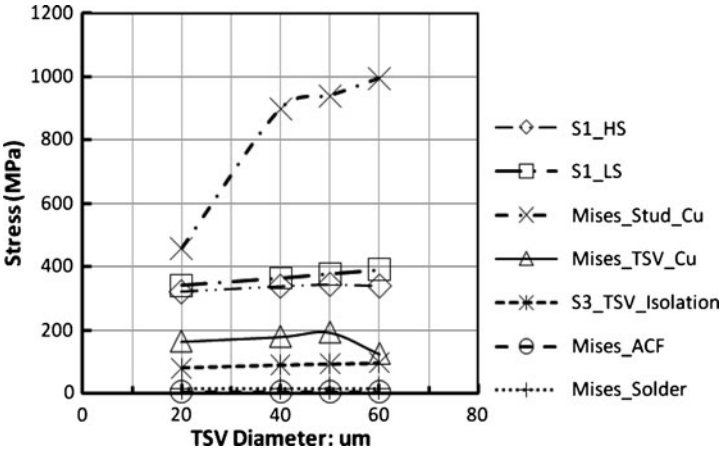


Fig. 5.76 The stresses of HS, LS, Cu stud, TSV Cu, ACF, isolation layer and solder vs. TSV diameter at reflow

Figure 5.76 has shown that the tensile stress S1 of HS die and LS die, von Mises stresses of TSV copper, Copper stud bumping, ACF layer, the compressive stress S3 of the isolation layer, and the von Mises stress of solder ball vary as the design parameter of TSV diameter at reflow. The TSV diameter has a significant impact on von Mises stress of the Copper stud bumping and TSV copper, tensile stress S1 of HS and LS die. As the TSV diameter increases, the von Mises stress of the Copper stud bumping has significantly increased, while the von Mises stress of TSV Copper increases slightly first, after the TSV diameter is larger 50 μm, it shows the decrement. The compressive stress S3 of the TSV isolation increases as well. However, there are no significant stress changes in ACF layer and the solder ball. Figure 5.77 shows the tensile stress S1 of HS die and LS die, von Mises stresses of TSV copper, Copper stud bumping, ACF layer, the compressive stress S3 of the isolation layer, and the von Mises stress of solder ball vs. the ACF thickness at reflow. As the ACF thickness increases, the tensile stresses S1 of both HS and LS die increase significantly (LS die stress increases fast), while the von Mises stress of Copper stud bump has significantly reduced. The von Mises stress of TSV copper decreases in a wave-like function. The compressive stress S3 of the TSV isolation layer increases slightly. There are no significant changes in the von Mises stresses of ACF layer and the solder ball.

Figure 5.78 shows that the tensile stress S1 of HS die and LS die, von Mises stresses of TSV copper, Copper stud bumping, ACF layer, the compressive stress S3 of the isolation layer, and the von Mises stress of solder ball vs. the HS die thickness at reflow. As the HS die thickness increases, the tensile stress S1 of LS die and the von Mises stress of TSV Copper increase slightly and become stable after HS die thickness exceeds 100 μm, while the tensile stress S1 of the HS die decreases and becomes stable after the HS die thickness is larger than 100 μm. All the rest stresses do not have significantly changes. Figure 5.79 shows the tensile stress S1 of HS die and LS die, von Mises stresses of TSV copper, Copper stud bumping, ACF layer, the compressive

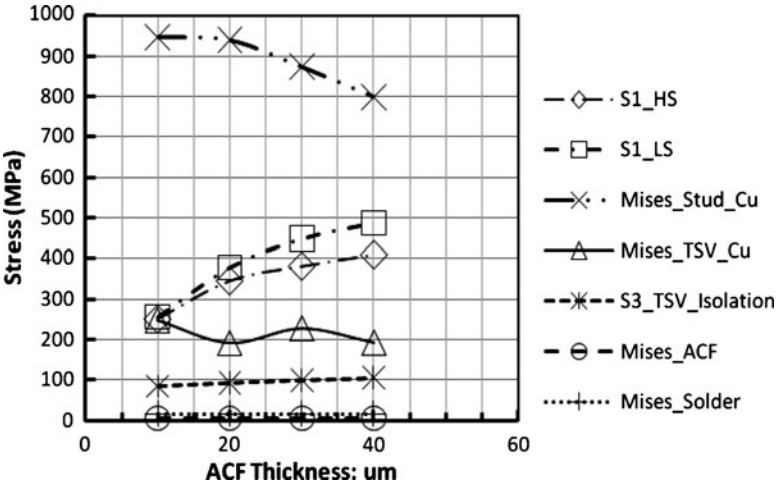


Fig. 5.77 The stresses of HS, LS, Cu stud, TSV Cu, ACF, isolation layer and solder vs. ACF thickness at reflow

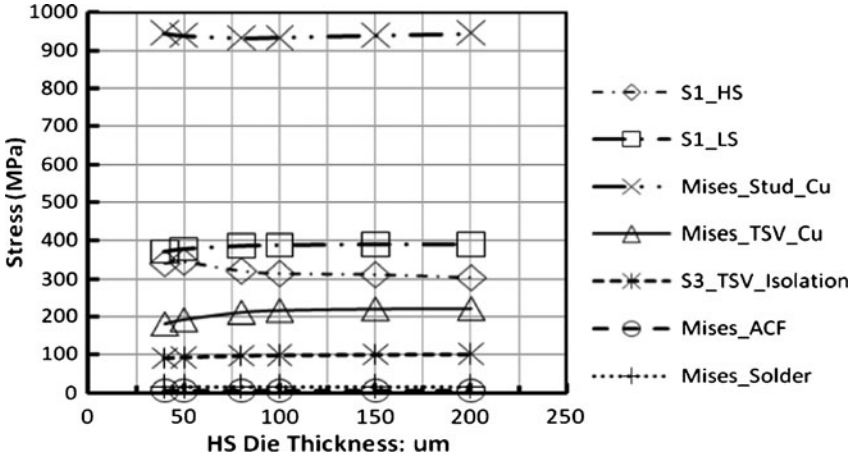


Fig. 5.78 The stresses of HS, LS, Cu stud, TSV Cu, ACF, isolation layer and solder vs. HS die thickness at reflow

stress S3 of the isolation layer, and the von Mises stress of solder ball vs. the LS die thickness at reflow. As the LS die thickness increases, the von Mises stresses of Copper stud bump and TSV copper increase. The tensile stresses S1 of HS and LS die have slightly increased, while the rest of the stresses of TSV isolation layer, ACF layer and solder ball are almost kept the same. Therefore through the stress analysis at reflow process, we understand that the stresses of ACF layer, solder ball, and the TSV

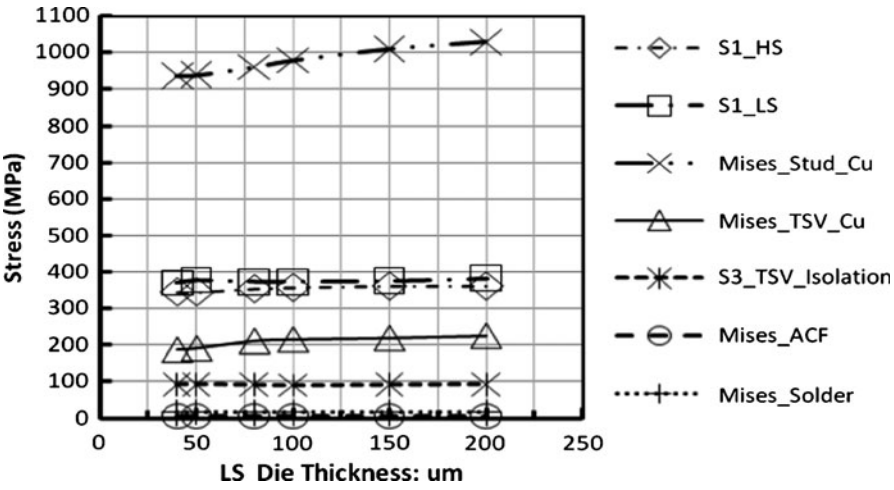


Fig. 5.79 The stresses of HS, LS, Cu stud, TSV Cu, ACF, isolation layer and solder vs. LS die thickness at reflow

Table 5.13 The comparison of stresses of TSV copper and TSV filled with epoxy

Compared items	Copper TSV (MPa)	Copper TSV filled with epoxy core (MPa)
Tensile stress S1 of HS	345	344
Tensile stress S1 of LS	378	377
von Mises stress of ACF	5.66	5.62
von Mises stress of Cu stud	939	940
von Mises stress of solder ball	16.5	16.6
von Mises stress of TSV (copper)	192	209
Compressive stress S3 of the TSV isolation	93.3	91.5

isolation layer are not sensitive to the design variable of the wafer level stack die power package. Table 5.13 lists the comparison of the stresses in Copper TSV and in Copper TSV filled with epoxy. The result shows there is no significantly difference for both cases, although the von Mises stress of Copper TSV filled with epoxy has a little higher stress (8% higher) than the Copper TSV.

5.4 Stack and Embedded Die Power Module

The introduction of embedded active components and integrated passives may be the most significant development in the electronics industry since the introduction of microvia technology [17, 18]. This section presents the design concept for

stack and embedded die power module. The power MOSFETs or IGBTs can be embedded inside the PCB, then add the stack die on the embedded die substrate. This layout allows the small size power module with optimization stack die height and allows the excellent thermal and electrical performance.

It is well known that as the development of the advanced power package, embedding of semiconductor MOSFET or IGBT chips into substrates has the advantages of achieving high degree of miniaturization, good electrical performance, and possible low cost. An embedding concept, so-called "Chip in Polymer" technology, was introduced early by Fraunhofer IZM and TU Berlin [19]. It is based on the embedding of thin chips into build-up layers by using PCB technology. At wafer level an extra Cu layer is added to the chip *I*/*O* pads to achieve laser-drilling selectivity and to realize good chip contact after via metallization. The wafer is thinned to the desired thickness and singulated. Then the chips are placed and bonded on a PCB substrate core and afterwards the chips are embedded in a polymer layer by vacuum lamination of Resin Coated Copper foil (RCC). Laser drilling is utilized to form the microvias from the outer layer to the chip and to the core substrate. Electrical contacts to the chips are realized by the metallized microvias. This embedded die technology is attractive because it provides the potentials of low cost and miniaturization.

5.4.1 The Design Concept of the Stack and Embedded Die Power Package

The design concept is to build the embedded HS MOSFET and LS MOSFET with an IC controller as the substrate. The drain of LS MOSFET connects to the source of HS MOSFET. Then, additional die and passives are stacked on the substrate of the embedded MOSFETs and IC die to form the stack die and embedded die power module. Figure 5.80 shows such a concept of the package. The power MOSFETs (HS and LS) and the IC controller are embedded in a prepreg material, which l is used as the core, which is a glass fabric filled composite impregnated with a resin and cured to an intermediate B-stage, e.g., like PCB material FR4. The prepreg material has punched out holes at a size somewhat larger than the die so that the prepreg can fit around the MOSFET die and the IC die. A RCC foil is used as lamination layer above the FR4, prepreg and all die. Then after the photo etching for the redistribution routing layout (RDL), stack a capacitor on the RDL that includes the source of the LS and drain of HS. Finally, overmold the capacitor and the embedded MOSFETs and the IC die to form the power module (see Fig. 5.80). The output pin layout is landed on the bottom surface which is easy for the surface mounting process on PCB through solder paste.

The assembly process flow steps for such stack die and embedded die power package can be described as follows: It starts with a Cu foil with a solder resist pattern, and MOSFET/IGBT/IC die that have a bond pad. Solder paste is stencil

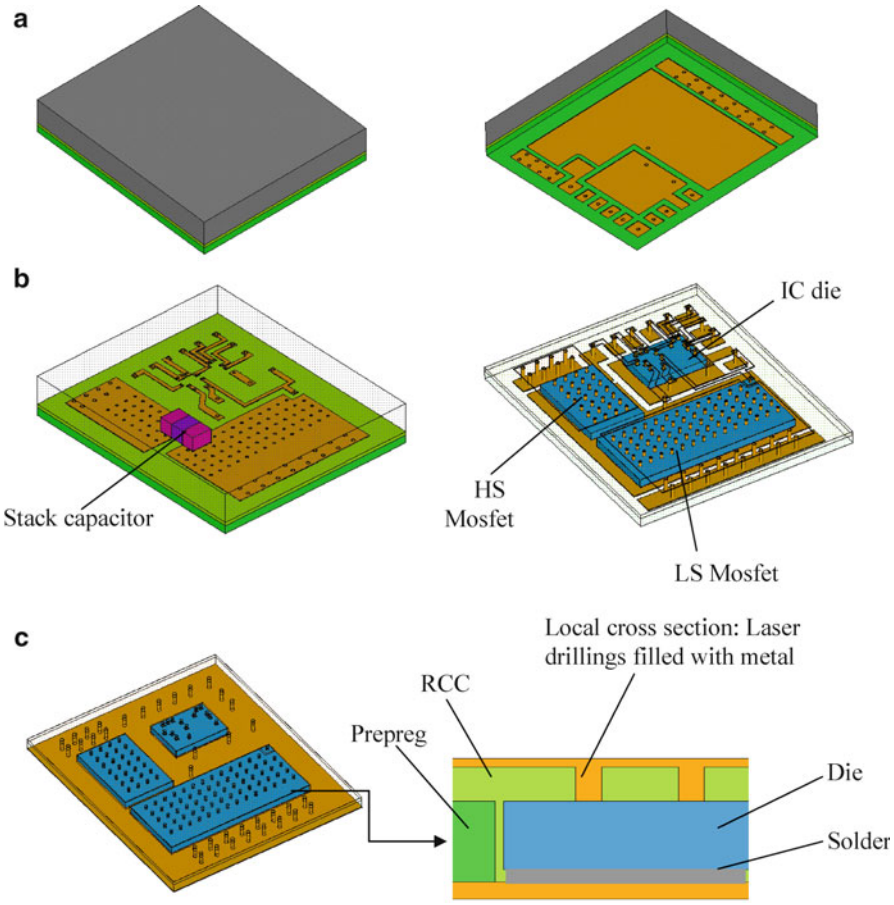


Fig. 5.80 The concept of the stack and embedded die power module. (**a**) The outer appearance of the embedded 3D power module. (**b**) The internal layout of the stack die embedded 3D power module. (**c**) Leaser drilling, plating after placing the RCC foil in the embedded Mosfet substrate

printed onto the Cu-foil and then MOSFET/IGBT/IC die are attached on it using a die bonder. The prepreg, with holes corresponding to the die and with the same thickness, is aligned onto the foil assembly. Then a RCC foil is added. This stack is laminated under vacuum. Optimization of the lamination conditions (pressure and temperature) is necessary to prevent die crack. Microvias are then drilled through leaser and electroplated. These microvias make contact to both the MOSFET die and the bottom copper foil. After the microvia filling the top and bottom copper layers are structured by photo etching to form the top RDL and the bottom land pin out. Then stack additional die or passives on the etched RDL metals. Overmold the stack die and passives on the embedded die substrate. Finally, sawing process is applied to separate the packages.

Table 5.14 The geometry of the stack and embedded die power module

Package type	Package dimension (mm^3)	Die dimension (mm^3)	Die attach thickness (mm)	Cu trace thickness (mm)
Stack and embedded die	6 × 7 × 1.2	LS: 4.4 × 1.96 × 0.2	0.025	0.025
		HS: 1.63 × 1.2 × 0.21	0.035	
		IC: 1.5 × 2.3 × 0.2	0.025	
		Capacitor: 1.2 × 0.6 × 0.4	0.025	

Table 5.15 The material thermal properties for the embedded die power module

Material	Capacitor (equivalent)	Silicon	EMC	Solder paste	Copper	Prepreg/resin
Thermal conductivity (W/mK)	58	146	1.0	33	392	0.4

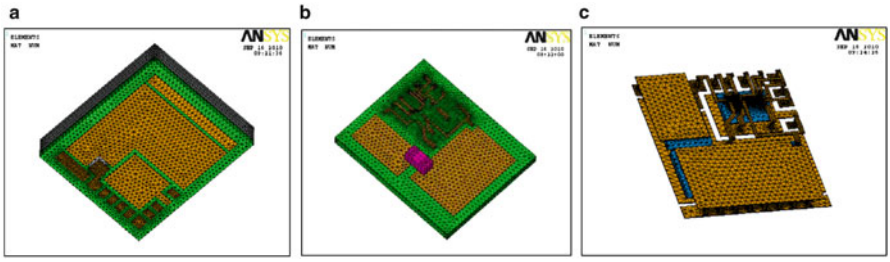


Fig. 5.81 The thermal model and mesh. (**a**) The full model. (**b**) Model exposed capacitor. (**c**) The internal structure

5.4.2 Thermal Performance Evaluation

The thermal simulation is applied to check the thermal performance of the stack and embedded die power package design. Table 5.14 gives the package design geometry data and Table 5.15 gives the material thermal properties data for heat dissipation analysis.

Figure 5.81 shows the thermal models with mesh. For the thermal analysis of a power module, most people are interested in the thermal resistance of junction to the case ($R\theta_{jc}$). This means that we put the power package in contact with heat sink or with water-cooled cold plate to force the most of the heat to flow to the heat sink or the cold plate through the package bottom surface at room temperature and at the same time, insulate the power module from air convention. Therefore, the temperature of bottom surface of the power package may be assumed the room temperature (25°C). Since this is the multiple die power package, we apply the input power on each of the active die and not to apply the power to the passive. There is thermal coupling effect between the die. When the power is applied on

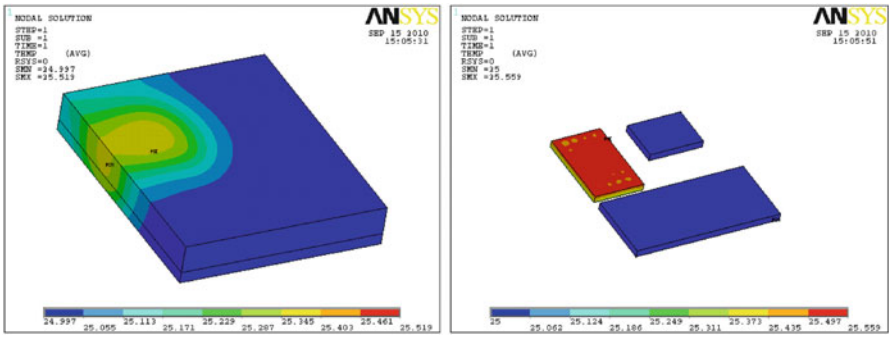


Fig. 5.82 The temperature distribution of the power module when the input power (1 W) is applied on HS die (maximum temperature on HS die is 25.56°C; maximum temperature on LS die is 25.033°C; maximum temperature on IC die is 25.004°C)

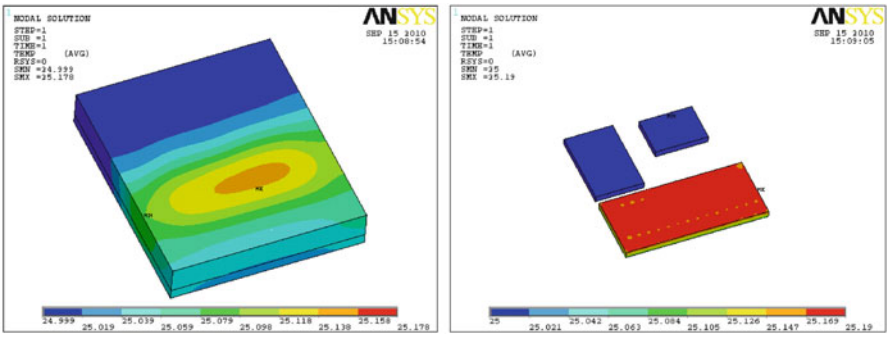


Fig. 5.83 The temperature distribution of the power module when the input power (1 W) is applied on LS die (maximum temperature on LS die is 25.19°C; maximum temperature on HS die is 25.013°C; maximum temperature on IC die is 25.001°C)

each die, the coupling thermal resistance will impact other die. Figures 5.82–5.84 show that the temperature distributions on the power module and on each die when the power is applied to HS, LS, and IC die. The thermal resistance of junction to the case ($R\theta_{jc}$) is listed in Table 5.16. From the Table 5.16, it can be seen that the design of the stack and embedded die power module has excellent thermal performance. The thermal coupling effect of the design is very small as well.

5.4.3 The Stress Assessment After the Molding Process

One major process of the stack and embedded die power module is the molding process after the completing the embedded MOSFET die. Normally the molding temperature is applied at about 175°C to allow the curing of EMC material at about 60–80 s. Then the molded package or penal strip will be ejected or taken out for cooling down

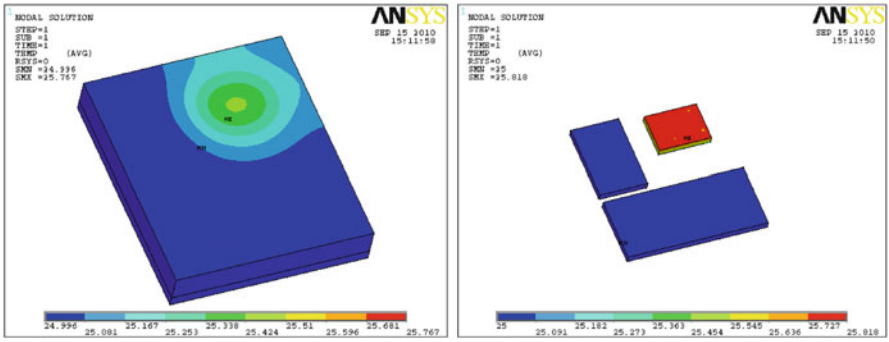


Fig. 5.84 The temperature distribution of the power module when the input power (1 W) is applied on IC die (maximum temperature on IC die is 25.82°C; maximum temperature on LS die is 25.005°C; maximum temperature on IC die is 25.002°C)

Table 5.16 The thermal resistance of junction to the case for the stack and embedded die power module

Thermal resistance	1 W applied on HS die	1 W applied on LS die	1 W applied on IC die
$R\theta_{jc}$ of HS die (°C/W)	0.56	0.013	0.002
$R\theta_{jc}$ of LS die (°C/W)	0.033	0.19	0.005
$R\theta_{jc}$ of IC die (°C/W)	0.004	0.001	0.82

Table 5.17 The thermal-mechanical properties of the embedded power module

Material	Capacitor (equivalent)	Copper	Silicon	Solder	EMC	Prepreg/FR4
Young's modulus (GPa)	198	127.7	131.0	26.4 at 328 K 25.8 at 343 K 25.0 at 373 K 24.1 at 413 K	26.5	EX: 25 EY: 25 EZ: 11
Poisson ratio	0.28	0.34	0.28	0.37	0.3	XY: 0.11 XZ: 0.39 YZ: 0.39
CTE (ppm/K)	10	17.1	2.8	21.9	8 ($T < 120$°C) 32 ($T > 120$°C)	X: 16 Y: 16 Z: 60

to room temperature before sent it to postcuring process. The cooling process from 175 to 25°C will induce the residual stress which will be potential to induce the failure of the power module. This section gives the stress assessment of the stack and embedded die power module after the molding process.

The model mesh is same as the Fig. 5.81 and the only difference is the element type. The elements of Fig. 5.81 are used for the thermal simulation, while in this section the elements for stress analysis are selected. Table 5.17 lists the material thermal-mechanical properties of the power module. Table 5.18 shows the viscoplastic property of the solder material Sn3.38Ag0.84Cu. Figure 5.85 gives

Table 5.18 The viscoplastic property of solder Sn3.38Ag0.84Cu

Description	Symbol	Units	Sn3.38Ag0.84Cu
Initial value of s	s_0	MPa	1.3
Activation energy	Q/R	K	9,000
Preexponential factor	A	1/s	500
Stress multiplier	ξ	–	7.1
Strain rate sensitivity of stress	m	–	0.3
Hardening coefficient	h_0	MPa	5,900
Coefficient for deformation resistance saturation value	$\hat{s}$	MPa	39.4
Strain rate sensitivity of saturation value	n	–	0.03
Strain rate sensitivity of hardening coefficient	a	–	1.4

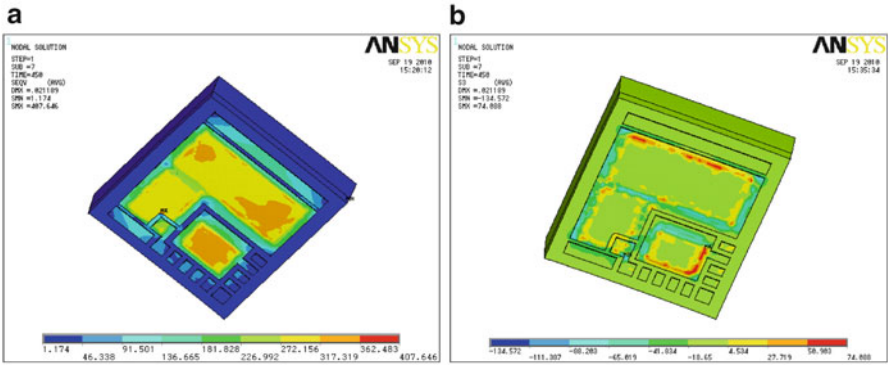


Fig. 5.85 von Mises and compressive stress distribution of the power module when cooling down to the room temperature. (**a**) von Mises stress distribution (maximum: 408 MPa). (**b**) The compressive stress S3 (maximum: 135 MPa)

the von Mises stress and compressive stress (the third principal stress S3) distribution of the embedded power module cooling down room temperature, the maximum stress appear at the embedded die substrate with the interfaces between the die and the embedded material prepreg/FR4 and resin. When the power module cools down from molding curing temperature to room temperature, the package is mostly under the compressive stress. Figure 5.86 checks both the von Mises stress and the compressive stress of the epoxy mold compound. Both maximum von Mises stress (79 MPa) and the compressive stress S3 (maximum: 119 MPa) appear at the interface of capacitor area. Figure 5.87 gives the von Mises stress and compressive stress S3 of the MOSFET die and IC die. It has shown that maximum von Mises stress (358 MPa) appears at the corner of IC die, while the maximum stress of the compressive S3 (484 MPa) appear at the corner of the LS which is the largest die in the power module. Figure 5.88 shows the von Mises stress and the compressive stress of solder paste. The largest von Mises stress (20 MPa) of the solder paste at room temperature appears at the corner of interface with LS MOSFET die while the maximum compressive stress S3 (162 MPa) appears at the corner of interface of with the IC die. Figure 5.89 has shown the von Mises stress, the compressive stress S3, and the tensile stress S1 distributions of the prepreg or FR4 core after the

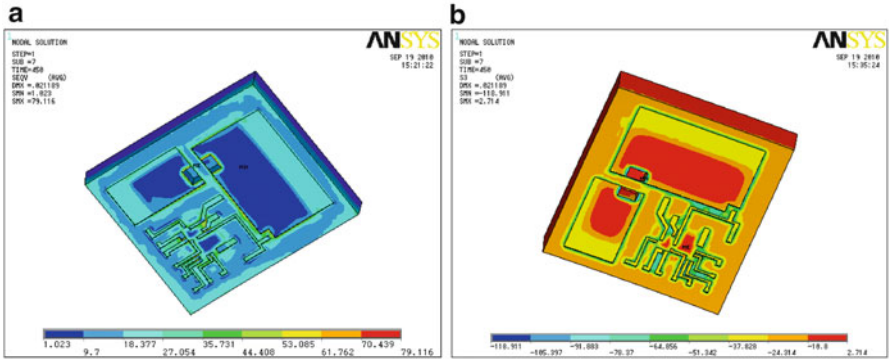


Fig. 5.86 von Mises and compressive stress distribution in EMC when cooling down to the room temperature. (**a**) von Mises stress distribution (maximum: 79 MPa). (**b**) The compressive stress S3 (maximum: 119 MPa)

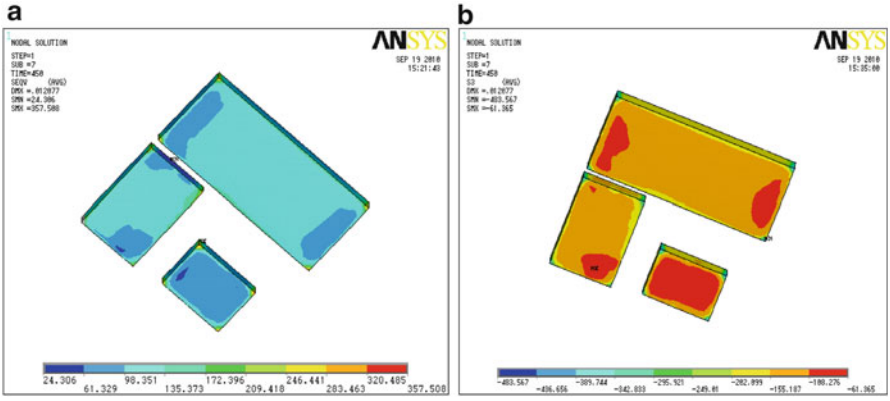


Fig. 5.87 von Mises and compressive stress distribution in die when cooling down to the room temperature. (**a**) von Mises stress of die (maximum: 358 MPa). (**b**) The compressive stress S3 of die (maximum: 484 MPa)

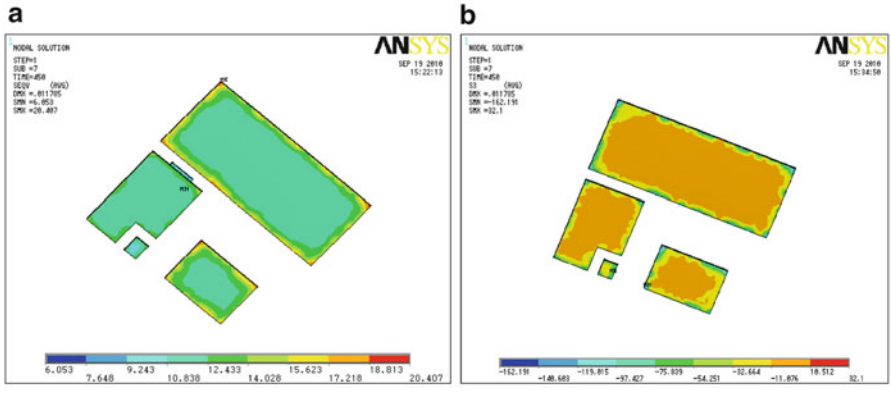


Fig. 5.88 von Mises and compressive stress distribution in solder paste when cooling down to the room temperature. (**a**) von Mises stress of solder paste (maximum: 20 MPa). (**b**) The compressive stress S3 of solder paste (maximum: 162 MPa)

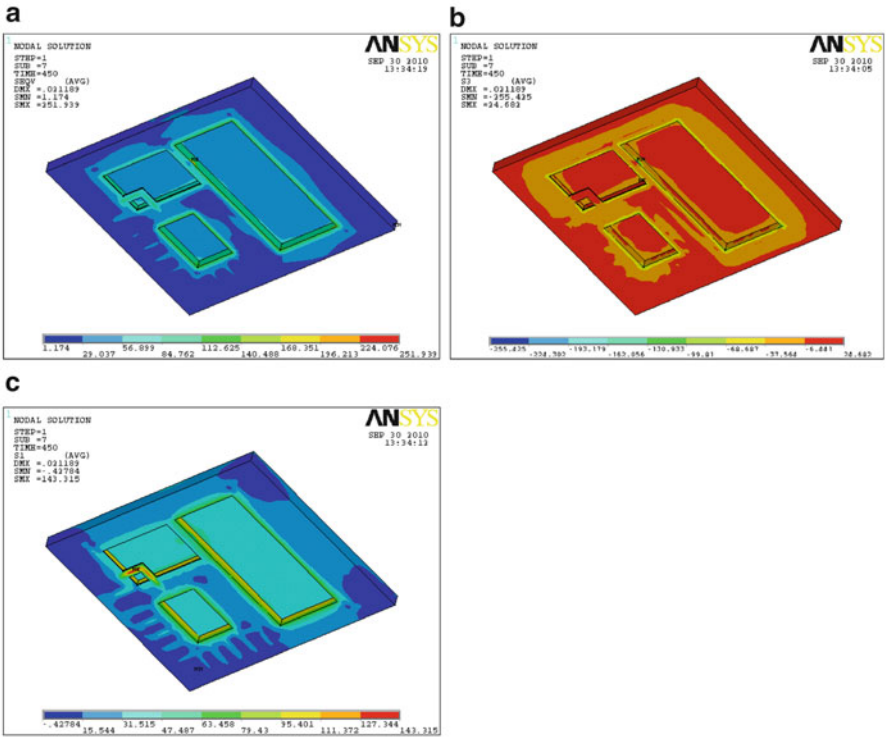


Fig. 5.89 von Mises compressive S3 and tensile S1 stress distribution in prepreg/FR4 core when cooling down to the room temperature. (**a**) The von Mises stress of prepreg (maximum: 252 MPa). (**b**) The compressive stress S3 of the prepreg (maximum: 255 MPa). (**c**) The tensile stress S1 of the prepreg (maximum: 143 MPa)

molding and curing from 175°C to the room temperature. The largest von Mises stress (252 MPa) and the maximum compressive stress S3 (255 MPa) of the prepreg/FR4 core appear at the interface with LS MOSFET die, while the highest tensile stress S1 appears at the interface of gate/solder paste area of the HS MOSFET die. In assessment of these stresses level of current design, the silicon stresses in the multiphase die are quite safe as compared to the silicon compressive strength. The stresses in the corner and interface of the EMC and solder paste need to pay attention to their development. In most case under compressive stress at room temperature would benefit to prevent the delamination and its growth.

5.4.4 The Preconditioning Stress Analysis

In the design of the stack and embedded die power module, one key design consideration is the stress analysis in the preconditioning test, which impacts the reliability and quality of the product with the delamination issue. This section

Table 5.19 The moisture properties of EMC and substrate core

Material		EMC	Substrate core prepreg FR4
Diffusivity (mm^2/s)	85°C	2.19e − 6	2.13e − 6
	260°C	8.0e − 5	3.14e − 5
C_{sat} (mg/mm^3)		3.69e − 3	0.0075
CME (mm^3/mg)		0.3	0.4

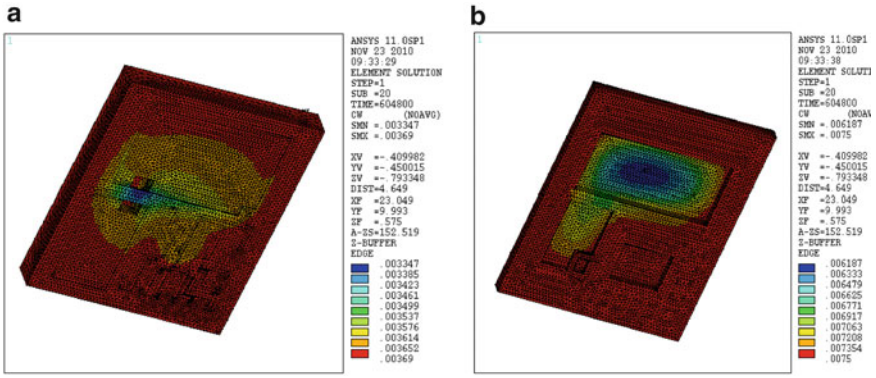


Fig. 5.90 The moisture distribution of the EMC and the substrate core at MSL1. (**a**) Moisture in EMC. (**b**) Moisture in substrate

introduces the stress analysis for the preconditioning. The first part presents the simulation results of the moisture distribution in moisture sensitivity level one test (MSL1) with 85°C/85 RH for 168 h moisture soak. Then, the simulation result will show the moisture and vapor pressure distribution for the sample with moisture in the reflow in 260°C. Based on the moisture and vapor distribution, the regions for calculating the stress can then be determined. The second part discusses the stress analysis in preconditioning and autoclave (ACLV).

5.4.4.1 The Moisture and Vapor Pressure Distribution

To simplify the problem, the epoxy resin in RCC layer is not considered, only the prepreg/FR4 substrate and the epoxy mold compound are investigated. The moisture properties of the two materials are listed in Table 5.19, in which the C_{sat} is the saturated moisture and CME is the coefficient of moisture expansion.

Figure 5.90 shows the moisture disctribution of the EMC and the substrate core of the stack and embedded die power module. It can be seen from the Fig. 5.90 that the moisture diffusion is almost soaked in most area of the EMC and substrate core after 168 h in 85°C/85 RH. At the back side of the LS MOSFET die there is about 80% moisture soak and the back side of capacitor there is about 90% moisture soak as compared to other areas.

Figure 5.91 shows the moisture distribution of the EMC and substrate core at reflow after MSL1. The results have shown that in reflow the moisture of the exposed

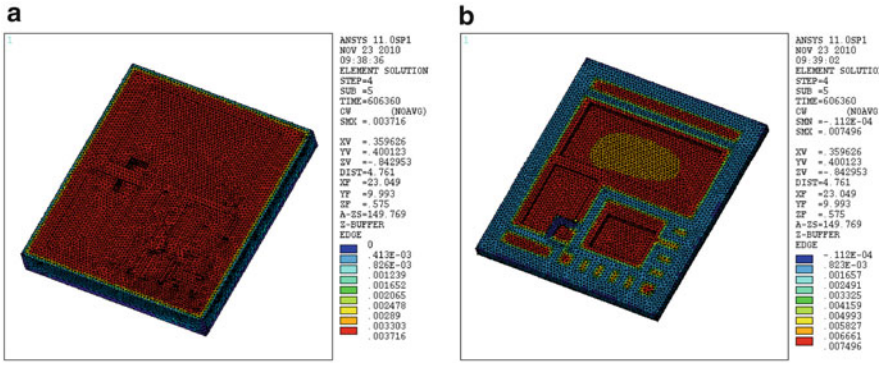


Fig. 5.91 The moisture distribution of EMC and the substrate core at reflow. (**a**) Moisture in EMC. (**b**) Moisture in substrate

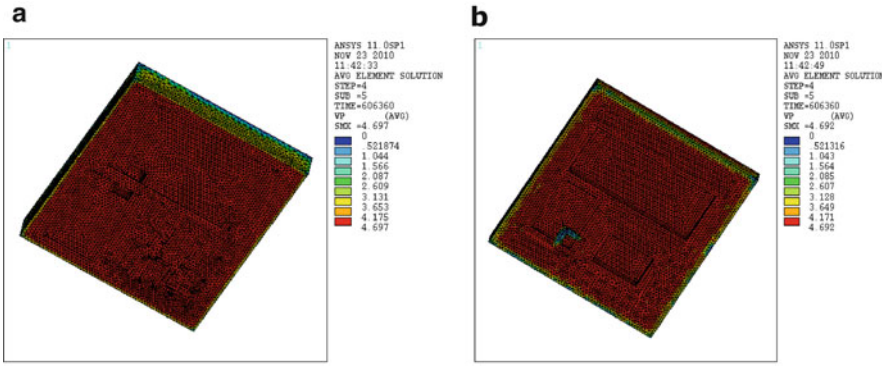


Fig. 5.92 Vapor pressure distribution of EMC and the substrate core at reflow. (**a**) Vapor pressure at EMC (maximum: 4.697 MPa). (**b**) Vapor pressure at substrate (maximum: 4.692 MPa)

surfaces in EMC and substrate core has been baked out. However on the other hand, most of the moisture is driven into the center area of the package, which possibly will induce higher hygroscopic stress and vapor pressure in reflow. Figure 5.92 shows the vapor pressure distribution of the EMC and substrate core at reflow. It has shown clearly that the most inner areas have been filled with saturated vapor pressures with 4.69 MPa at reflow. The saturated vapor pressure is the potential factor to induce the crack growth in reflow if there is a initial defect.

5.4.4.2 The Stress Analysis in Precondition

The stress level at reflow is important for the stack and embedded die power module. Based on the Figs. 5.91 and 5.92, it can divided the EMC and substrate core into two regions, region 1 is the area that the moisture at the out surfaces of the EMC and

Table 5.20 The equivalent coefficient of thermal expansion (CTE) coefficients for EMC and substrate core at reflow

Materials		CTE (ppm/°C)	Equivalent CTE (hygroscopic)	Equivalent CTE (vapor pressure)	Integrated CTE (ppm/°C)
EMC	Region 1	32	8.0	13.1	53.1
	Region 2	32	3.2	6.7	41.9
Substrate core	Region 1	16/60	21.4	10.3/6.7	47.7/88.1
	Region 2	16/60	8.6	5.3/3.4	29.8/72

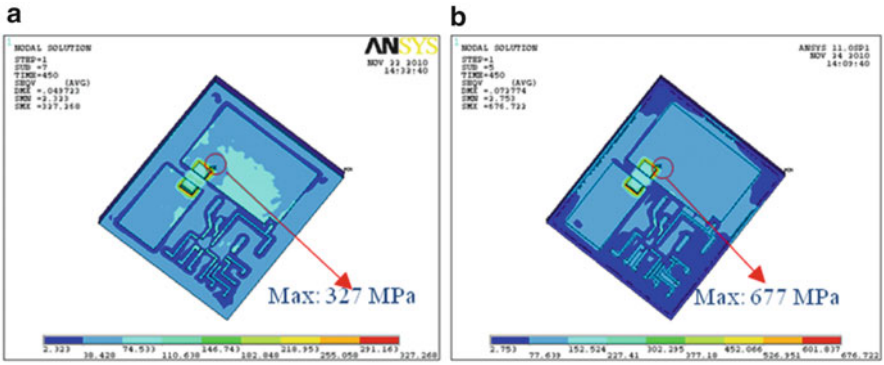


Fig. 5.93 The von Mises stress distribution of EMC in dry and wet case at reflow. (**a**) EMC dry case. (**b**) EMC with moisture

the substrate has been baked out and region 2 is the areas that have been fully filled with moisture and saturated vapor pressure. Since the region 1 is very small as compared to the region 2, therefore we can consider the region 1 with average moistre and vapor pressure. Based on the work of ref. [20], the equivalent CTE coefficients for hygroscopic and vapor pressures are obtained in the Table 5.20.

Figure 5.93 gives the von Mises stress comparison of the EMC with dry and wet case at reflow. The wet case is the case after moisture soak at 85°C/85 RH with 168 h. The results show that the maximum stress appears at the corner of the top surface of the capacitor. As we can see that the maximm stress of wet case is two times greater than the dry case. Figure 5.94 shows the von Mises stress comparison of the substrate core with dry and wet case at reflow. The results show that the maximum stress appears at the corner of the active side surface of the LS die. As it can be seen again that the maximm von Mises stress of substrate core in wet case is two times greater than that of the dry case.

Table 5.21 lists the maximum von Mises stress and the first principal stress comparison of EMC and substrate core at precondition, in which the impacts of pure CTE (dry case) stress, the hygroscopic stress and stress induced by vapor pressure are presented. For the reference, the stress comparison of EMC and substrate core at ACLV is also listed. From the Table 5.21, it can be seen that the influence of the pure CTE, moisture expansion and the vapor pressure. At the reflow, the CTE

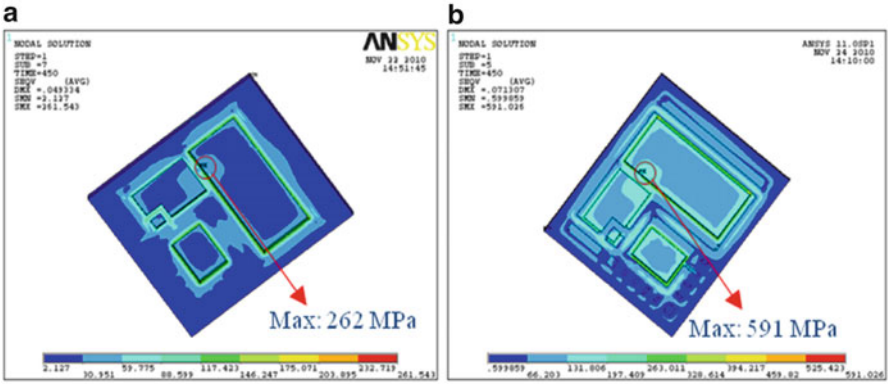


Fig. 5.94 The von Mises stress of the substrate core in dry and wet case at reflow. (**a**) Substrate core in dry case. (**b**) Substrate core in wet case

Table 5.21 The maximum stress comparison at precondition and the autoclave (ACLV) condition

Items		CTE mismatch	Hygroscopic stress	Vapor pressure	Integrated stress
Reflow	von Mises stress in EMC (MPa)	327	78	80	677
	S1 in EMC (MPa)	208	114	92	405
	von Mises stress in substrate (MPa)	262	244	138	591
	S1 in substrate (MPa)	262	264	182	527
ACLV	von Mises stress in EMC (MPa)	11.2	145	6	163
	S1 in EMC (MPa)	7.3	87	7	97
	von Mises stress in substrate (MPa)	8.6	210	3	218
	S1 in substrate (MPa)	8.5	165	4	171

mismatch stress, hygroscopic stress and vapor pressure induced stress are roughly at the same value scale level. While the CTE mismatch stress is the largest stress in EMC, the CTE mismatch and hygroscopic stresses are equivalent value in substrate core. However, the fact that shows the integrated total stress in wet case is almost double greater than the pure CTE mismatch stress case. This indicates that in reflow although the dry case can pass the reliability test, the stress in wet case would be hard to pass it. In ACLV test, the hygroscopic stress dominates the failure. The hygroscopic stresses in EMC and substrate core are ten time above greater than the CTE mismatch stress and the stress induced by vapor pressure. Therefore in the design of the stack and embedded die powre module, we understand that at precondition condition, the CTE mismatch stress, hygroscopic stress and vapor pressure induced stress make the contributions to the delamination failure while in ACLV test, the hygroscopic stress play an dominated role in the delamination.

5.5 Summary

This chapter induces the power system in package and power module packaging design considerations and analysis. First, the design concept of side by side die placed power SiP and power module is presented with a typical 6×6 MLP for a SiP mounting on a PCB are discussed, which includes board mounting, PCB design, PAD finish, stencil design, soldering and reflow, voiding problem. The design optimization of the DrMOS SiP packaging is applied through finite element electrical and thermal analysis with eight DoE legs. Both the electrical and thermal DoE analysis show that the metal clip bond design has the lowest the electrical resistance and parasitic inductance, highest conduction efficiency, as well as the lowset the thermal resistance. Then the design of a hybrid power module Fairchild SPM® module with a group side by side IGBT, FRD, HV and LV die is introduced. The thermal mechanical stress analysis in assembly process (including voiding effect) and heat sink mounting process is discussed. After that the design concept of a power stack die SiP is presented for a low voltage buck converter. This package uses the premolded lead frame and IC die as the substrate, two MOSFET flip chips are then mounted on it. The failure mechanism and reliability analysis of the power SiP package in TMCL test are discussed. The failure mechanism and reliability analysis of the power package in TMCL test are discussed. Then the design concept of 3D wafer level power stack die packaging is introduced for a synchronous buck converter with TSV to connect the high MOSFET side and LS MOSFET die. The design parameter DoE studies for thermal and stress in two major assembly processes with FEA for the 3D wafer level stack die power SiP are presented. Then the design concept of the stack and embedded die power module is introduced. The thermal performance of the embedded power module is assessed. The stresses of the embedded power module after molding curing, ACLV and in the preconditioning are investigated. The results indicate that the hygroscopic stress in ACLV dominates the embedded power module failure while in reflow, the CTE mismatch, hygroscopic and the vapor pressure plays equally roles in the stress contributions.

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Chapter 6
Thermal Management, Design, and Cooling for Power Electronics

The operation of a semiconductor device is sensitive to junction temperature [1]. When the junction temperature exceeds the functional limit, the device does not operate in a normal way. It is also well known that the failure rates of semiconductor devices increase exponentially as the junction temperature rises. It is very crucial that the package designer and set application engineer understand the definition, characteristics, and application of the thermal resistance of the electronic packaging for proper device operation. Power dissipation during the operation of the semiconductor device induces an increase in the junction temperature. This depends on the amount of power dissipation and the thermal resistance between the junction and the package surface (referred to as "case" hereafter), an ambient and some other specified reference point. This chapter introduces the thermal management, design, and cooling methods for power electronic packaging.

6.1 Thermal Resistance and Measurement Methods

6.1.1 Thermal Resistance Concept

The relation among these thermal properties such as thermal resistance, power dissipation, and the junction temperature $R\theta_{jx}$ is defined in the following (6.1) [1].

$$R\theta_{jx} = \Delta T/P = (T_j - T_x)/P \tag{6.1}$$

where

P: Power dissipation per device
T_j: Junction temperature
T_x: Reference temperature
Unit: °C/W

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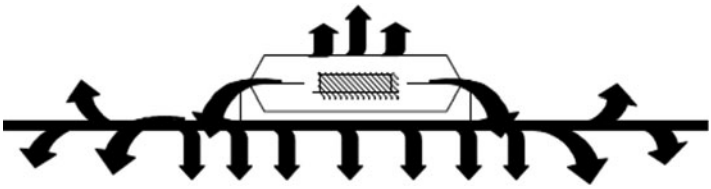


Fig. 6.1 Heat paths to ambient air

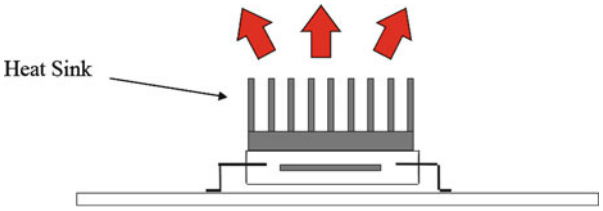


Fig. 6.2 Heat path through heat sink

The thermal resistance indicates the temperature drop between the junction and a specific reference point per unit of power consumption. It is a simplified parameter characterizing the thermal performance of a package (Fig. 6.1). The selection of the reference point is arbitrary, and typical points and their abbreviations are summarized as follows:

(a) Junction to ambient temperature ($R\theta_{JA}$):

$$R\theta_{JA} = \frac{T_j - T_A}{P} \tag{6.2}$$

There are three major paths to air: one is the junction through package top to air; another is the junction through package bottom to either air or bottom; another one is the junction through package leads to board. In most cases, primary path is leads to board (Fig. 6.2).

(b) Junction to the component case ($R\theta_{jc}$):

$$R\theta_{jc} = \frac{T_j - T_c}{P} \tag{6.3}$$

$R\theta_{jc}$ applies only to situations in which all or nearly all of heat is flowing out of top or bottom of package through heat sink. Low $R\theta_{jc}$ means that heat will flow easily into external heat sink (Fig. 6.3).

(c) Junction to the component lead ($R\Psi_{jl}$):

$$R\Psi_{jl} = \frac{T_j - T_l}{P} \tag{6.4}$$

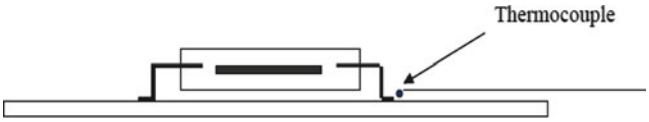


Fig. 6.3 Heat path through the package lead

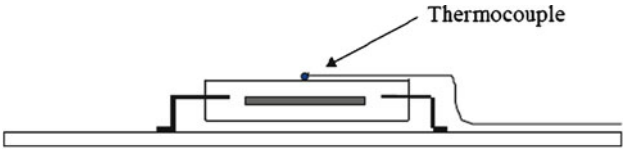


Fig. 6.4 Heat path through the package top surface

$R\Psi_{jl}$ is not a true thermal resistance. In the formula (6.4), the total power is used because it is what is known. In standard environment, most but not all of the power flows to the board through leads (Fig. 6.4).

(d) Junction to component top surface ($R\Psi_{jt}$):

$$R\Psi_{jt} = \frac{T_j - T_t}{P} \tag{6.5}$$

This is used to estimate the junction temperature from a measurement of top of package in actual applications. $R\Psi_{jt}$ is not a thermal resistance. The total power is used in the formula (6.5) because it is what is known. It is not the power dissipation between the junction and the top of the package. Normally, only a small amount of power exits the package top.

(e) Other well-defined reference sites

Usually, here (c)–(e) are called thermal parameters rather than thermal resistances. From the above definitions, $R\theta_{JA}$ (the junction to ambient thermal resistance) and $R\theta_{jc}$ (the junction to case thermal resistance) are generally the most commonly used definitions in power packaging.

6.1.2 Temperature Sensitive Parameter (TSP) Method for Junction Calibration

The only unknown parameter is the junction temperature in the thermal resistance test, since the case or ambient temperature and power consumption are measured directly during the test. The direct measurement of the junction temperature is not possible, except in some packages, which have dies that are exposed to the air. But the P–N junction of a device reveals a specific forward voltage drop at a given

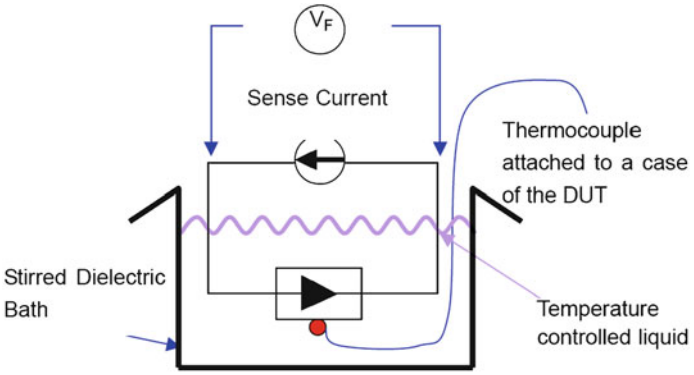


Fig. 6.5 Schematic diagram of a calibration bath for TSP measurement

temperature and a current. This forward voltage drop of a junction is called TSP (Temperature Sensitive Parameter) and is also known as the "diode-forward-voltage-drop" method from the original applications using power diodes or bipolar power transistors. This test method is called ETM (Electrical Test Method), since the junction temperature is measured indirectly by an electrical relationship. Currently, ETM is the most popular technique for junction temperature measurement.

The relationship between the forward-voltage-drop and the junction temperature is an intrinsic electro-thermal property of the semiconductor junction. The relationship is characterized by a nearly linear relationship between the forward-biased-voltage-drop and the junction temperature when a constant forward-biased current (also called Sense Current, hereafter) is applied. Figure 6.5 is a schematic illustration describing a measurement test setup of this voltage drop vs. the junction temperature relationship for a diode junction.

In this test, the device under test (DUT) is heated up to a thermally equilibrated temperature in a hot bath, and a sense current is applied to the device to measure the forward-biased-voltage-drop at this temperature. The amount of the sense current is small enough to not heat the DUT, such as 1, 10 mA, depending on the DUT's operating characteristics. By repeating the same tests at various temperatures, Fig. 6.6 can be obtained.

The relationship shown in Fig. 6.6 can be expressed in various mathematical equations, and a typical linear equation formula is given by equation (6.6) through a curve fitting.

$$T_j = m \cdot V_f + T_o \tag{6.6}$$

Here, the slope "m" (°C/V) and the temperature ordinate-intercept "T_o" are used to quantify this straight-line relationship. The reciprocal of the slope is often referred to as "K factor" in unit of mV/°C. In this case, V_f is the "TSP" for the diode junction, and the slope of the temperature–voltage calibration line is always negative, i.e., the forward conduction voltage decreases with increasing junction temperature. Table 6.1 shows TSP candidates for the various devices.

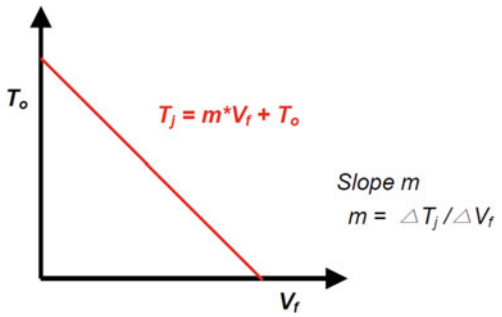


Fig. 6.6 Typical example of a TSP plot

Table 6.1 TSP candidates for the various devices

DVC	Temperature sensitive parameter
Diode, rectifier, SCR, TRIAC	Diode *V*
Integrated circuit, thermal test die	Die sensing diode *V*
Integrated circuit, functional die	Substrate isolation diode sensed and powered or sense diode voltage and functional powering
Bipolar transistor, NPN	Base-to-emitter or base-to-collector diode *V*
Bipolar transistor, PNP	Emitter-to-base or collector-to-base diode *V*
MOSFET (N channel)	Source-to-drain diode *V* or gate turn-on *V*
MOSFET (P channel)	Drain-to-source diode *V* or gate turn-on *V*
Darlington transistor	Base-to-emitter diode *V* or saturation *V*
IGBT	Saturation *V* or gate turn-on *V*

6.1.3 Thermal Resistance Measurement Procedure

Once the device is calibrated, the thermal resistance measurement test is conducted. Figure 6.7 describes a schematic of the thermal resistance measurement test circuit. This is composed of two subcircuits, i.e., the heating and the sensing circuit. The heating circuit is operated to heat up the DUT up to T_{jmax}, given in the datasheet, by adjusting the power, while the sensing circuit is designed to measure the TSP with the sense current used in the device calibration. During the thermal resistance measurement test, an electrical switch is changed automatically for the operation of the heating circuit or the sensing circuit.

Figure 6.8 shows a typical example of the power pulse train with a specific heating and sensing interval.

A power of known current and voltage is applied to the device according to the heating time interval, i.e., 80 ms in Fig. 6.8. During a sensing time interval, 100 μs in Fig. 6.8, the sense current is applied to the device to measure the TSP, i.e., the junction temperature. The sense current must be the same as the one used in the device calibration. While monitoring the TSP, the applied power is adjusted so as to

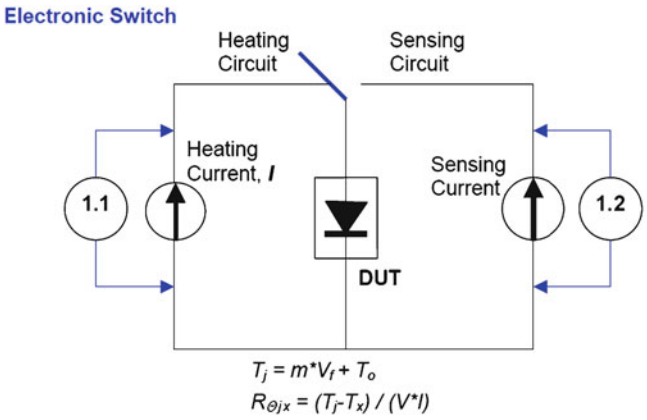


Fig. 6.7 Schematic of the thermal resistance measurement circuit

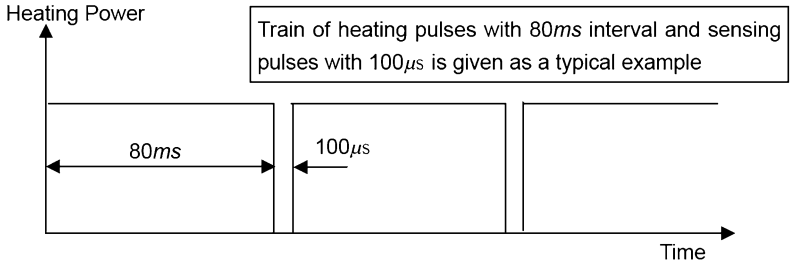


Fig. 6.8 Example of a power pulse train for a thermal resistance measurement test

insure a sufficient rise in T_j, or the temperature difference between the junction and the reference site to guarantee a sufficient measurement resolution.

The TSP sensing time interval must be adjusted so as not to allow the cooling of the junction prior to reapplying power, but long enough to measure the TSP in a stable manner, while avoiding the parasitic effect of the circuit. The heating and sensing pulse train shown in Fig. 6.8 has a duty cycle of 99.9%, which is considered to be continuous power for all practical purposes.

When T_j attains a convergent value, then the junction temperature T_j, the reference temperature T_x, and also the applied power P can be recorded simultaneously. By using these values and formula (6.1), the thermal resistance can be obtained directly.

When the reference temperature T_x is measured at the package case, then T_x is referred to as T_c. The thermal resistance is written as $R\theta_{jc}$, and called junction-to-case thermal resistance. This indicates a package's power dissipation capability from the junction to the case. This is usually used for packages mounted on infinite or temperature-controlled heat sinks.

When the reference temperature T_x is an ambient temperature, then T_x is referred to as T_a. The thermal resistance is written as $R\theta_{JA}$, and called junction-to-ambient

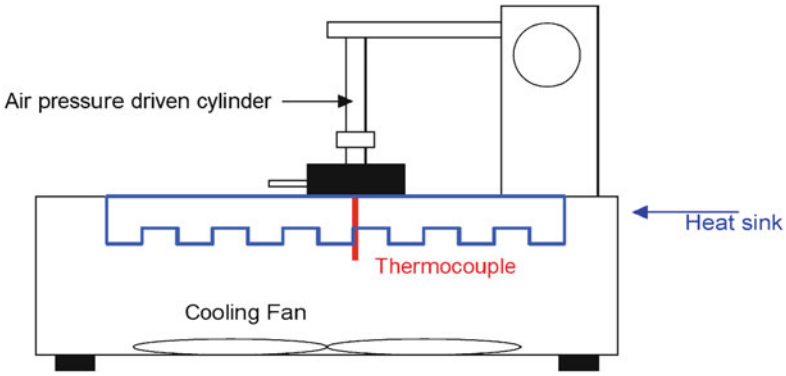


Fig. 6.9 Schematic of the junction-to-case thermal resistance measurement test

thermal resistance. This indicates a package's power dissipation capability from the junction to the ambient. This is usually used for packages mounted on PCBs without a heat sink. The detail test environments for $R\theta_{JA}$ and $R\theta_{jc}$ are described in the following section.

6.1.4 Thermal Resistance Measurement Environments

6.1.4.1 Junction-to-Case Thermal Resistance

Figure 6.9 shows a schematic of the junction-to-case thermal resistance also known as the $R\theta_{jc}$ measurement test. The major components are a heat sink, thermocouple, cooling fan, and a pressure-driven cylinder. The package is placed on the heat sink, and fixed by the cylinder. The size of the heat sink and the airflow capacity of the cooling fan must be large enough so as to maintain a constant temperature over the heat sink during the test. It is essential to apply thermal grease between the package and the heat sink, and sufficient clamping cylinder pressure to minimize the contact thermal resistance. A thermocouple is inserted through the heat sink and is pressed against the underside of the package nearest the device to record the package case temperature. The thermocouple needs to make good thermal contact with its reference location.

6.1.4.2 Junction-to-Ambient Thermal Resistance

Natural Convection Environments

Figure 6.10 shows a schematic of the junction-to-ambient thermal resistance test, also known as the θ_{JA} measurement test under natural convection conditions. The

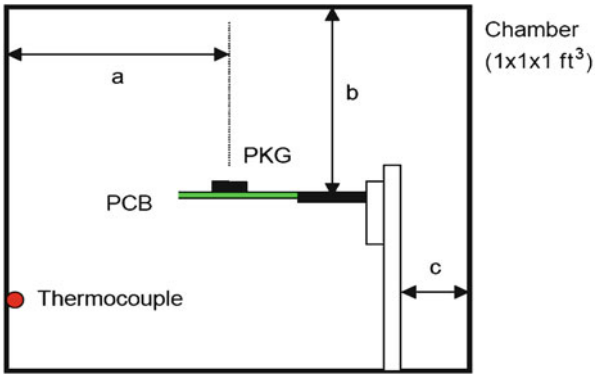


Fig. 6.10 Schematic of a still air chamber for the junction to ambient thermal resistance measurement test (*a*: 6.0 in., *b*: 6.5 in., *c*: 3.0 in., volume 12 × 12 × 12 in.^{3})

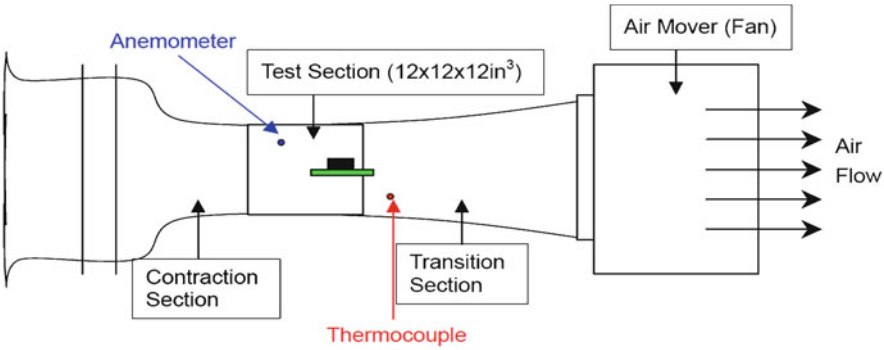


Fig. 6.11 Schematic of a forced air wind tunnel for the junction to ambient thermal resistance measurement test

major components are a still air chamber, PCB for the package mounting and a thermocouple. The chamber encloses one cubic-foot volume of still air and follows the JEDEC standard recommendations. The PCB is mounted horizontally (or vertically, if requested) in the chamber, and the reference temperatures for both the inside and the outside of the chamber are measured.

Forced Convection Environment

Figure 6.11 shows a wind tunnel for the junction-to-ambient thermal resistance test, also known as the $R\theta_{JA}$ measurement test under forced convection conditions. The test setup is similar to the natural convection environment except for the still air chamber. The wind tunnel dimension is 12 × 12 × 74 (in.^{3}) with a test duct of 6 in.

width. The temperature and air velocity are measured at the center of the tunnel and 6 in. ahead of the test board and package, respectively. The board and package are placed along the direction of the airflow. The air velocity is measured with a hot-wire anemometer probe, and the temperature is measured with the thermocouple.

6.2 Selection of a Thermal Test Board

For the junction-to-ambient thermal resistance measurement test, the selection of a thermal test board or PCB for package mounting is crucial in thermal performance characterization. The common standards for thermal test board selection can be referred in Sect. 6.2.3. The specific dimension and material are recommended in the JEDEC standards JESD51-3 [2] and JESD51-7 [3] for power packages. These standards provide consistency in the thermal resistance presentation of the packages offered by the various semiconductor companies. The basic material is FR-4 with a total thickness of 1.6 mm, and the basic dimensions of the test boards are given in Figs. 6.12 and 6.13 (refer to JESD51-3).

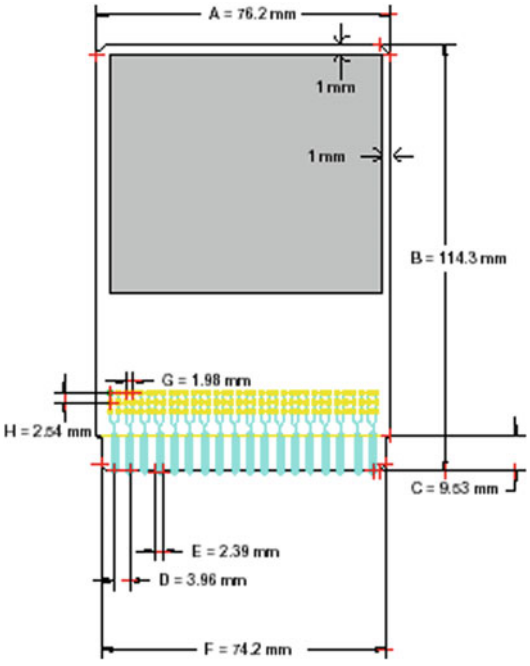


Fig. 6.12 PCB for packages <27.0 mm long 74.20 × 74.20 (mm^2) buried planes (reproduced with permission from JEDEC)

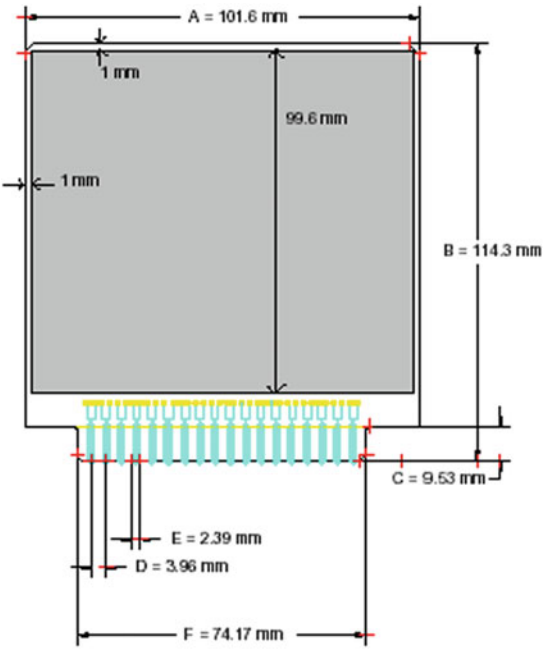


Fig. 6.13 PCB for packages >27.0 mm long 99.60 × 96.60 (mm^2) buried planes (reproduced with permission from JEDEC)

6.2.1 Low-Effective Thermal Test Board

Low-effective thermal conductivity test boards [2] are designed to simulate a worst board mounting environment from a thermal performance point of view based on JEDEC standard. These test boards have no internal copper planes, and are named 1s0p test boards or two layer boards. These are two layer boards with minimal copper traces electrically connected from each package to one of the edge connectors. Two 1 oz copper layers are covered on both sides of the test board.

6.2.2 High-Effective Thermal Test Board

High-effective thermal conductivity test boards [3] are fabricated to have two evenly spaced internal planes. These boards more closely reflect applications in which ground or power planes are used in the PCB. Figures 6.12 and 6.13 show internal plane areas in the test boards. Figure 6.14 shows the trace layers and layer thickness of a cross section in a high effective thermal test board.



Fig. 6.14 Cross section of multilayer PCB in JEDEC standard 6.15 SOP test board (pitch: 1.27 mm)

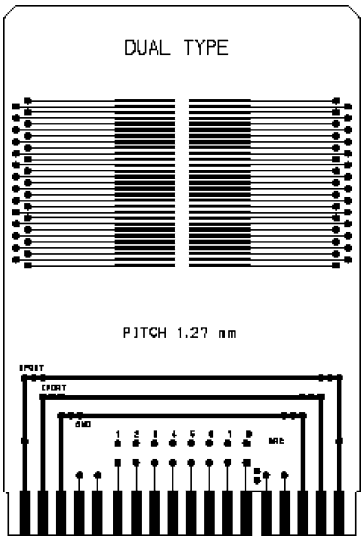


Fig. 6.15 SOP test board (pitch: 1.27 mm)

This test board is called a 2s2p (two signal plane and two power and ground planes) test board or four layers or multilayer board.

6.2.3 Thermal Test Board for Various Power Packages [4–6]

Figures 6.15–6.22 show thermal resistance test boards designed for various power package types. Figures 6.15–6.18 show the SOP dual types with different pitches.

Figure 6.19 gives the DPAK/D2PAK test board for discrete power packages. Figures 6.20 and 6.21 listed the test boards for power QFP with 0.6 and 0.8 mm pitches, respectively. Figure 6.22 shows the test board for the vertical insert power package. Selecting the test boards will be up to the power package type which will be reasonable to show the electrical and thermal performance of the power package.

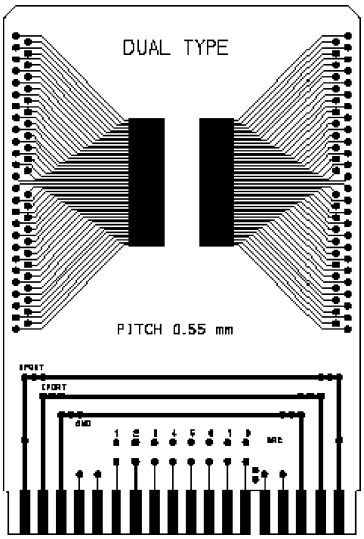


Fig. 6.16 SOP test board (pitch: 0.55 mm)

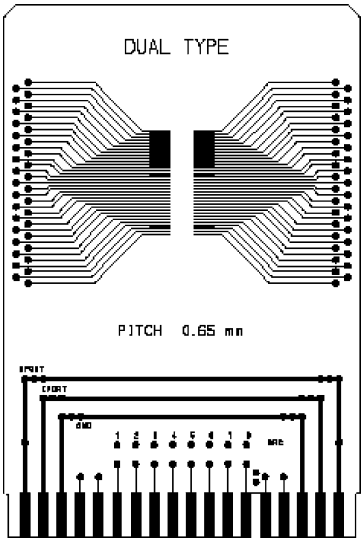


Fig. 6.17 SOP test board (pitch: 0.65 mm)

6.2.4 Standards for Thermal Test Board

The most common standards used for thermal test boards include the EIA/JEDEC standards and SEMI standards, below is the list of them.

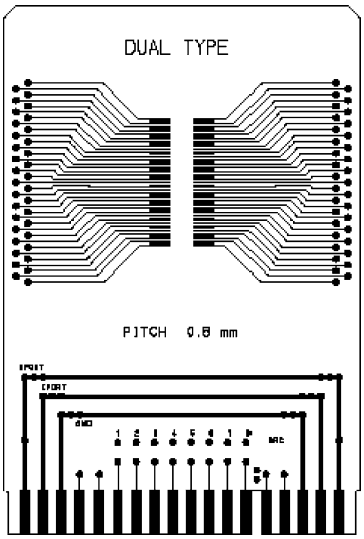


Fig. 6.18 SOP test board (pitch: 0.8 mm)

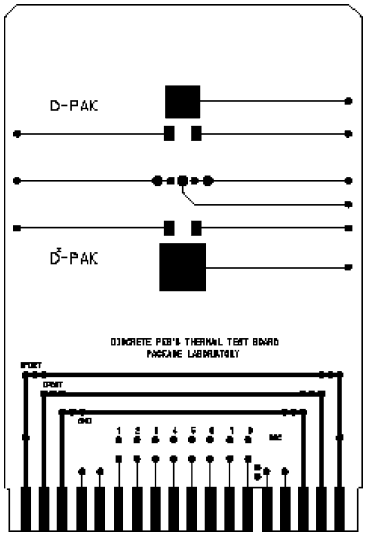


Fig. 6.19 DPAK/D2PAK test board

6.2.4.1 EIA/JEDEC Standards

JESD51 Methodology for the Thermal Measurement of the Component Packages (Single Semiconductor Device), 1995.

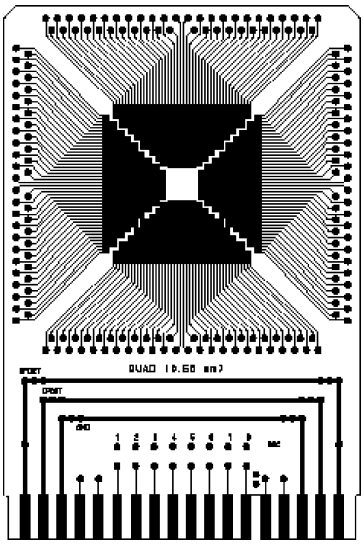


Fig. 6.20 QFP test board (pitch: 0.6 mm)

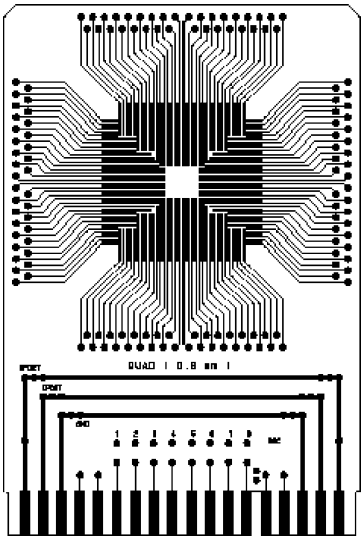


Fig. 6.21 QFP test board (pitch: 0.8 mm)

JESD51-1 Integrated Circuit Thermal Measurement Method—Electrical Test Method (Single Semiconductor Device), 1995.
JESD51-2 Integrated Circuit Thermal Measurement Environmental Condition—Natural Convection (Still Air), 1995.

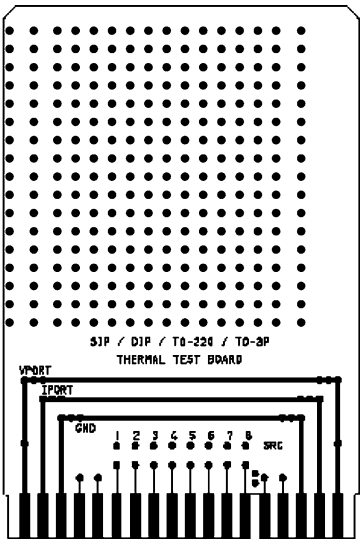


Fig. 6.22 Insert type test board (pitch: 2.54 mm)

JESD51-3 Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages, 1996.
JESD51-4 Thermal Test Chip Guidelines (Wire Bond-type Chip), 1997.
JESD51-5 Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms, 1999.
JESD51-6 Integrated Circuit Thermal Test Method Environmental Conditions-Forced Convection (Moving Air), 1999.
JESD51-7 High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages, 1999.
JESD51-8 Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board, 1999.
JESD51-9 Test Boards for Area Array Surface Mount Package Thermal Measurements, 2000.
JESD51-10 Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements, 2000.
JESD51-11 Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements, 2001.
JESD51-12 Guidelines for Reporting and Using Electronic Packaging Thermal Information, 2005.

6.2.4.2 SEMI Standards

G30-88 *SEMI Test Method*: Junction-to-Case Thermal Resistance Measurement of Ceramic Packages.

G42-96 *SEMI Test Method:* Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages.
G46-88 *SEMI Test Method:* Thermal Transient Testing for Die Attachment Evaluation of Integrated Circuit Packages.
G38-96 *SEMI Test Method*: Still- and Forced-Air Junction-to-Ambient Thermal Resistance Measurements of Integrated Circuit Packages.
G68-96 *SEMI Test Method*: Junction-to-Case Thermal Resistance Measurements in Air Environment for Semiconductor Packages.

6.3 Thermal Prediction, Management and Design

6.3.1 Estimation of Junction Temperature

In (6.1), assume that reference temperature T_x, power dissipation P, and the thermal resistance $R\theta_{jx}$ are known; the junction temperature T_j can be estimated through (6.1).

The reference temperature T_x can be measured directly using the thermocouple. The one important thing to keep in mind is that the reference temperature must be measured at the same location as was used in the thermal resistance measurement test. In the case of T_c, the case temperature, the reference temperature measurement location may be the package center or the hottest area from the previous test conditions. In the case of T_a in the ambient temperature, the reference temperature measurement location may be the temperature of the air that surrounds the operating package. Usually, defining the ambient temperature is not easy due to the complexity of an application set, and the airflows inside of it. In these situations, it is recommended that some other sites be used as the reference temperature measurement locations, i.e., outer leads, package top surface, etc. rather than the ambient temperature itself. The power dissipation P can be estimated by calculating switching losses during device operation. When the reference temperature, the thermal resistance $R\theta_{jx}$ and the power consumption are obtained, then the junction temperature calculation can be estimated using the following equation:

$$T_j(\text{estimated}) = R\theta_{jx} \cdot P + T_x \tag{6.7}$$

An example is: The prediction of the junction temperature.

Given conditions: $R\theta_{jc} = 1.2°C/W$ in the datasheet, case temperature $= 80°C$ (measured), applied power $= 40$ W (calculated from applied current and voltage).

The junction temperature is estimated as:

$$T_j = R\theta_{jc} \cdot P + T_c = 1.2 \cdot 40 + 80 = 128°C$$

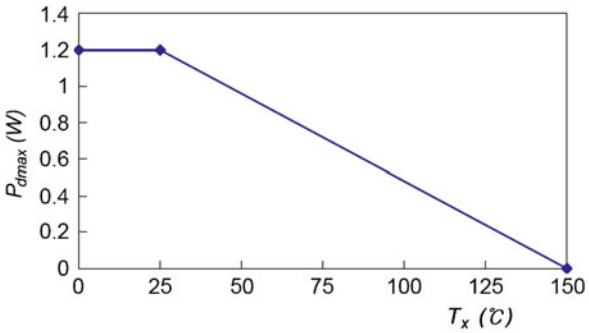


Fig. 6.23 Example of power decreasing curve

6.3.2 Estimation of the Maximum Power Dissipation

Equation (6.1) can be rewritten as follows:

$$P = (T_j - T_x)/R\theta_{jx} \tag{6.8}$$

Equation (6.8) indicates the power capability of a package under a given junction temperature, reference temperature, and thermal resistance. This relationship is used to calculate the maximum power consumption under a given condition, and is usually shown as the following power decreasing curve in Fig. 6.23.

Example is the prediction of the maximum allowable power dissipation.

Given conditions: $R\theta_{jc} = 2.0°C/W$ in the datasheet, the maximum case temperature to be maintained $= 70°C$ (designer's decision), maximum allowable junction temperature $= 150°C$ (restriction).

Allowable maximum power dissipation:

$$P = (T_j - T_c)/R\theta_{jc} = (150 - 70)/2.0 = 40\,W$$

6.3.3 Thermal Management and Design for Power Package

6.3.3.1 Effects of Power Package Design Variables

1. Device area and thickness
   Figure 6.24 shows that the thermal resistance of junction to case ($R\theta_{jc}$) as the function of the device area in two different power chips with two different thicknesses for a TO220 power package. As the device area increases, the thermal resistance decreases. It also shows that thinner BJT has significantly

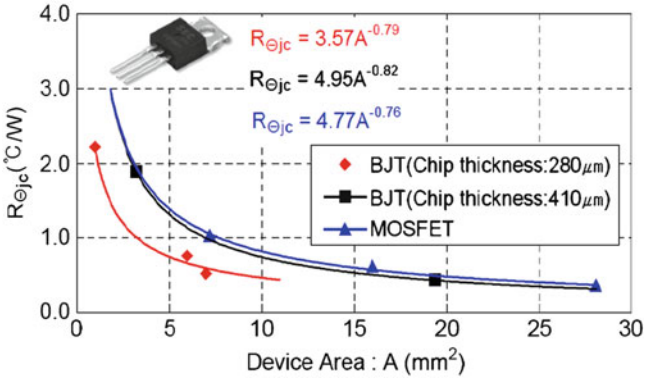


Fig. 6.24 Thermal resistance ($R\theta_{jc}$) vs. device area with different thickness of TO220 package

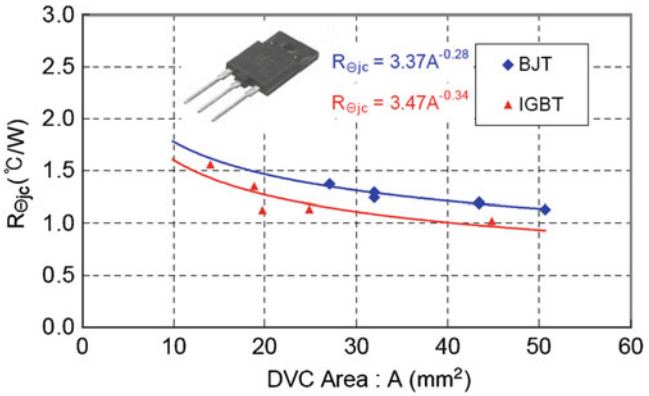


Fig. 6.25 Thermal resistance ($R\theta_{jc}$) vs. device area with different device (IGBT and BJT) of TO3PF package

lower thermal resistance. Figure 6.25 gives the trends comparison of thermal resistance ($R\theta_{jc}$) of junction to case of the BJT and IGBT devices with the same chip size in a TO3PF package. It can be seen that the IGBT die has lower thermal resistance.

2. Effect of different leads design with natural and forced conventions
   Figure 6.26 shows that the trends of thermal resistance ($R\theta_{JA}$) of junction to ambient vs. air speed with two different lead design for 48QFP and 48QFPH packages. The result disclosed that design of 48QFPH has better thermal performance, its thermal resistance is lower than the design of 48QFP.
3. Effect of thermal grease
   Figure 6.27 shows that the thermal resistance of junction to case ($R\theta_{jc}$) as the function of the device area with and without thermal grease for a TO220 power

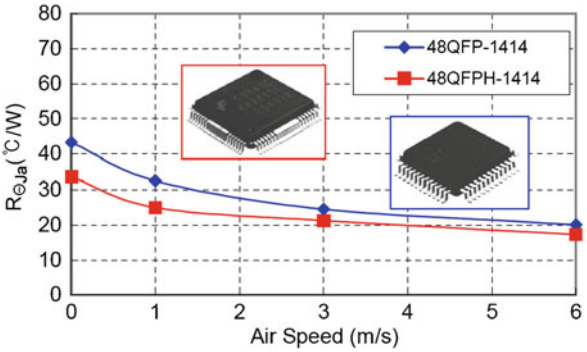


Fig. 6.26 Thermal resistance ($R\theta_{JA}$) vs. air speed with two different lead designs for QFP packages

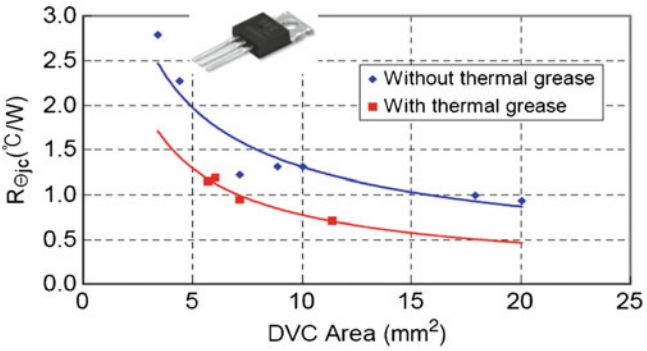


Fig. 6.27 Thermal resistance ($R\theta_{jc}$) vs. device area with and without thermal grease

package. The thermal resistance without the thermal grease is clearly higher than the case with thermal grease.

4. Effect of the thermal conductivity of epoxy mold compound (EMC)
   Figure 6.28 shows thermal resistance $R\theta_{jc}$ with two different thermal conductivities of EMC material in TO220F package. The EMC with larger thermal conductivity is better in thermal performance of the power package.
5. Effect of the gap between pad and the lead tip.
6. Effect of pad size
   Figure 6.29 shows the impact of the design gap between the pad and the tip of lead on the thermal resistance. As the gap becomes larger, the thermal resistance becomes significant greater. Figure 6.30 shows that the larger pad can effectively reduce the thermal resistance. Figure 6.31 shows the effect of metal layer and via size in a PCB design on the thermal resistance, the thermal resistance has shown the highest without the metal layer. Larger via size and the multilayer can improve the thermal performance of the PCB.

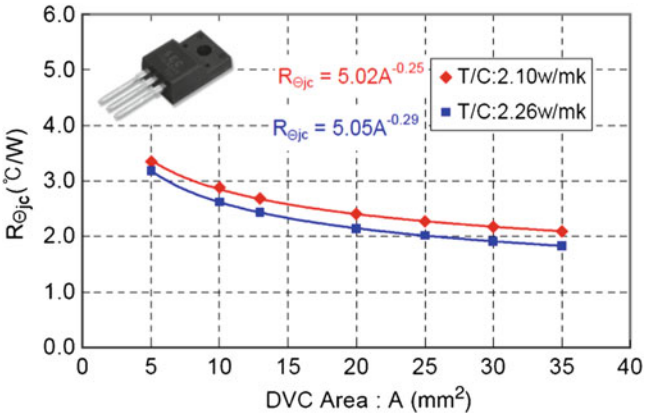


Fig. 6.28 Thermal resistance ($R\theta_{jc}$) vs. device area with two EMC materials

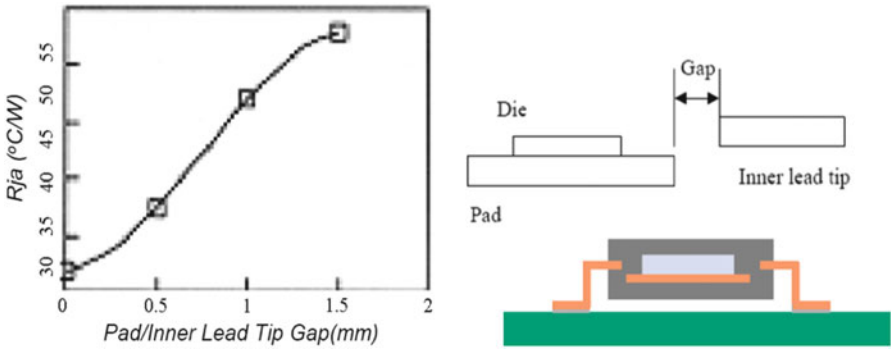


Fig. 6.29 Relationship between the thermal performance of a 28 mm, 160 lead QFP and the pad/inner lead tip gap

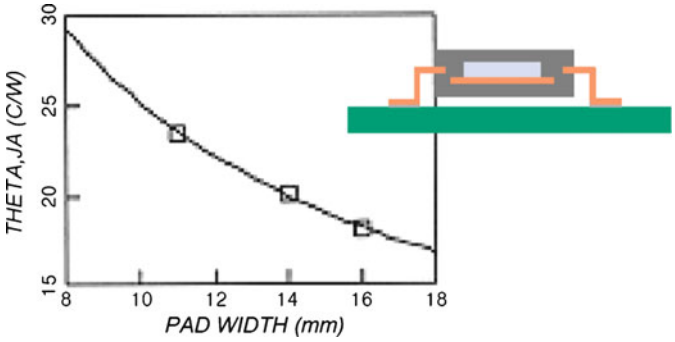
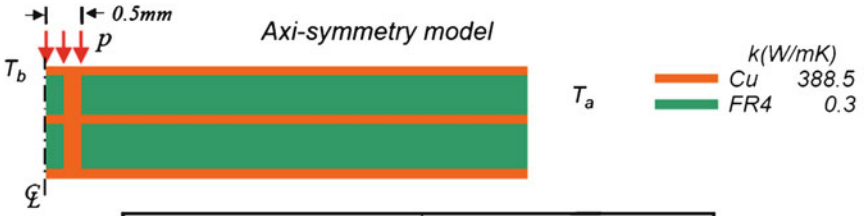


Fig. 6.30 Relationship between the thermal performance of a 208 lead, 28 mm TQFP and the pad width



Case	R_{ba} (°C/W)	
	1 oz. Cu	*2 oz. Cu*
0 S – 0 G	1388	-
1 S – 0 G	6.764	3.677
2 S – 0 G	6.764	-
2 S – 1 G	6.763	
2 S – 0 G – 0.2 mm Via	5.294	-
2 S – 0 G – 0.4 mm Via	3.655	-
2 S – 0 G – 0.6 mm Via	2.369	-

$$R_{ba} = \frac{T_b - T_a}{p}$$

Fig. 6.31 Impact of PCB metal layer and vias on the thermal resistance

6.3.3.2 Effects of Power Package Type

The thermal resistance is very up to the power package design and the package type. Below are the characteristics of the thermal performance with different power packages. Figure 6.32 shows that the thermal resistance of junction to ambient for different TO packages.

Figure 6.33 shows the thermal resistance of junction to ambient for SOT, DPAK, D2PAK, MLP, and LQFP packages. The D2PAK has the best thermal performance, next by MLP and LQFP. SOT 623 has the highest thermal resistance. Figure 6.34 shows the impact of package volumes and type on the thermal resistance of junction to ambient; the MLP and D2PAK have the larger volumes; therefore, both of the packages have the smaller thermal resistance.

Figure 6.35 shows the impact of air flow speed (natural and forced convention) on the thermal resistance of junction to ambient for different DIP packages. The high pin DIP package has the smaller thermal resistance. Figure 6.36 shows the impact of ambient air speed on the thermal resistance for different SOP packages.

Figure 6.37 shows the impact of air flow speed (natural and forced convention) on the thermal resistance of junction to ambient for different QFP packages. The high pin QFP package has the smaller thermal resistance. Figure 6.38 shows the impact of ambient air speed on the thermal resistance for 44 lead MLP package with different JEDEC boards.

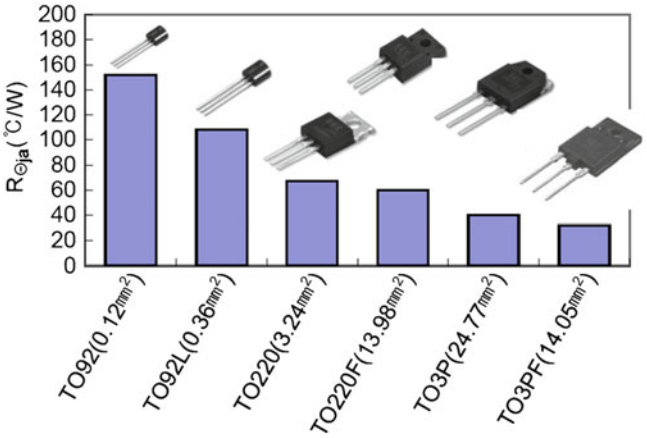


Fig. 6.32 Thermal resistance of junction to ambient ($R\theta_{JA}$) for through hole TO packages

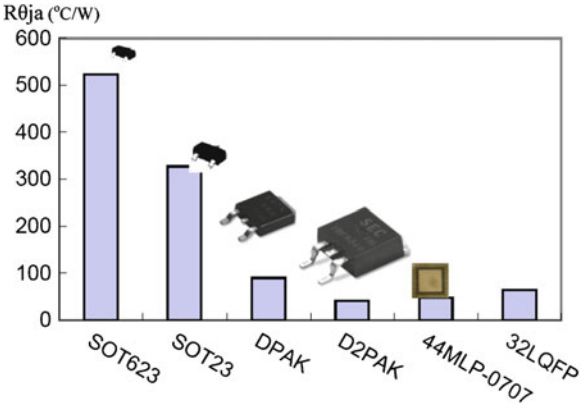


Fig. 6.33 Thermal resistance of junction to ambient ($R\theta_{JA}$) for different surface mount packages

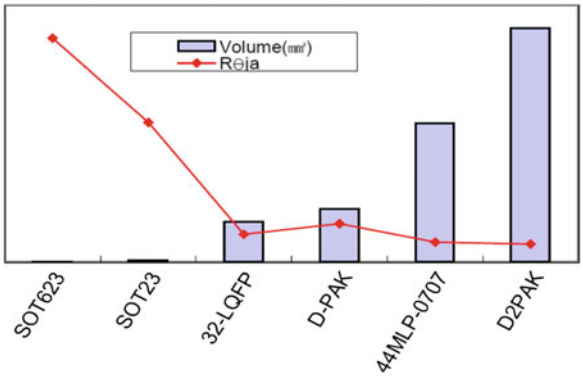


Fig. 6.34 Thermal resistance of junction to ambient ($R\theta_{JA}$) and package volume for different surface mount packages

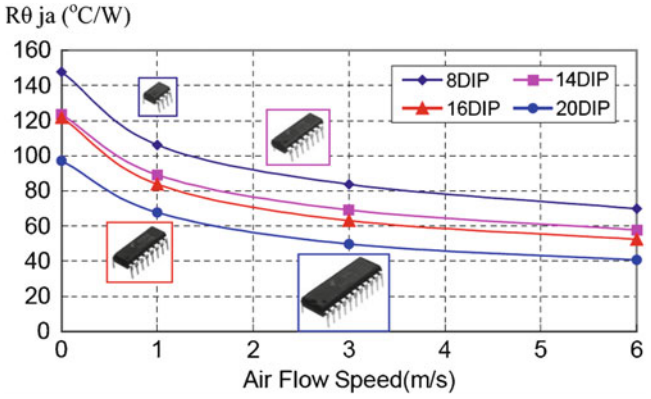


Fig. 6.35 Thermal resistance of junction to ambient ($R\theta_{JA}$) vs. air flow speed for different DIP packages

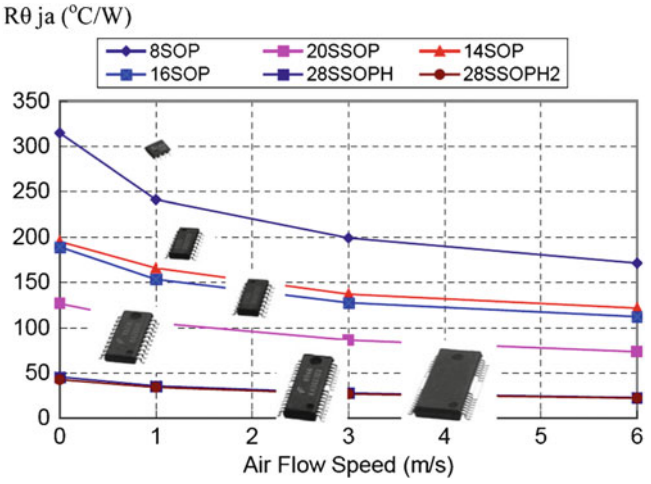


Fig. 6.36 Thermal resistance of junction to ambient ($R\theta_{JA}$) vs. air flow speed for different SOP packages

Figure 6.39 shows that the impact of the thermal vias on the thermal resistance of 44 lead MLP on a 1s2p JEDEC board. Figure 6.40 gives the comparison of the thermal resistance of junction to ambient vs. air speed of three type packages with different PCB copper trace thicknesses. The results show that the thicker the copper trace on PCB (more metal), the smaller the thermal resistance.

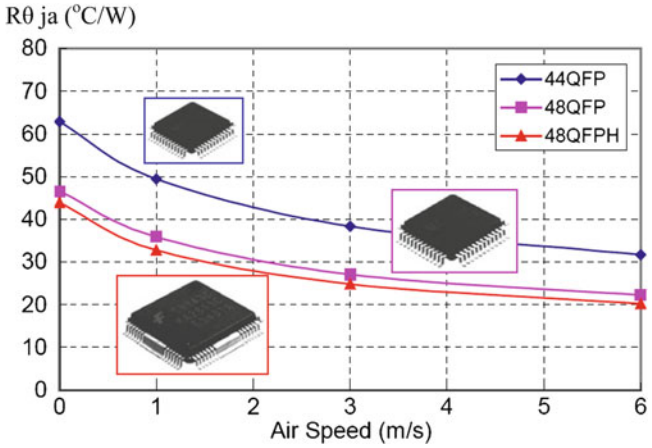


Fig. 6.37 Thermal resistance of junction to ambient ($R\theta_{JA}$) vs. air flow speed for different QFP packages

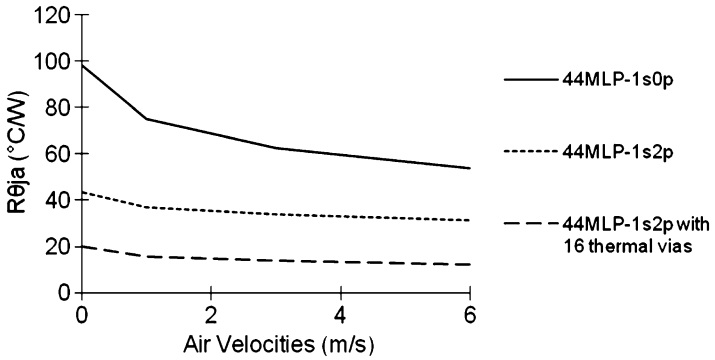


Fig. 6.38 Thermal resistance of junction to ambient ($R\theta_{JA}$) vs. air flow speed for MLP package with different JEDEC boards

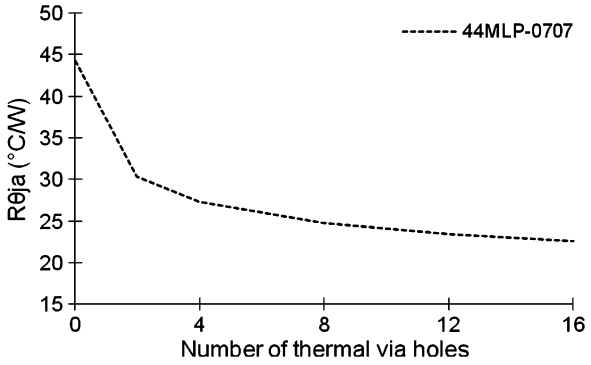


Fig. 6.39 Thermal resistance of junction to ambient ($R\theta_{JA}$) vs. thermal vias MLP package with (1s2p) JEDEC board

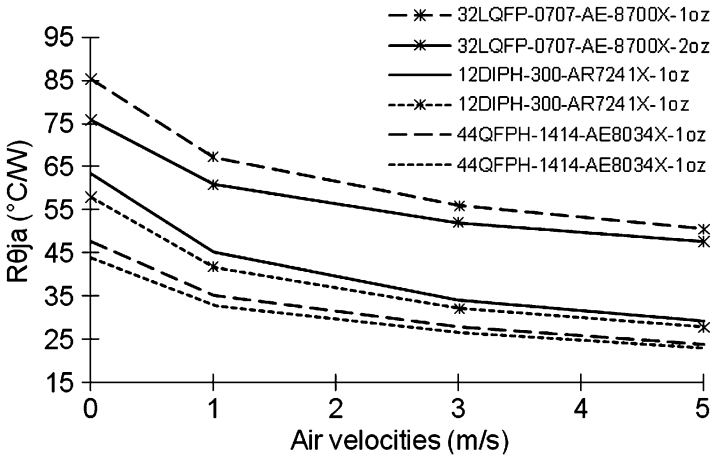


Fig. 6.40 Thermal resistance of junction to ambient ($R\theta_{JA}$) vs. air speed for LQFP, DIP, and QFPH packages with different PCB Cu trace thickness

6.4 Heat Transfer Analysis from Device to Board Level

The operational characteristics of silicon devices such as die are strongly influenced by device temperature. This section gives an application example of a heat transfer analysis from a device of silicon on insulator (SOI) to board level [7]. For SOI devices power dissipation is a much more significant challenge than for non-SOI devices. As a result the thermal design of SOI devices is vital to proper product performance. To maximize the engineering understanding of SOI circuits we develop a method to examine the combined system of SOI device and the package by finite element analysis. These results are compared to results obtained from a thermal equivalent electrical circuit model. The use of on die structures as an aide to heat dissipation from the device to the assembly package board level is explored.

6.4.1 SOI Device Operation and Design Consideration

The use of SOI for designing integrated circuit devices has several advantages as compared to LOCOS isolation. SOI technology provides complete electrical isolation for the individual devices. This eliminates substrate current issues, and reduces device capacitance. Heat generated during the operation of a device may be dissipated through several paths. These paths include through the bond wires and lead frame, the EMC, and through the silicon substrate, into the die attach pad (DAP) and the lead frame. For most IC devices the thermal path through the substrate and the dap is a major contributor for thermal dissipation. SOI technology

significantly lessens the conductivity on this path due to the bottom oxide. The performance of semiconductor devices that are typically used for creating the product's circuitry exhibit some form of temperature dependency. As an overview of the importance of this we briefly discuss the primary types of devices that are temperature sensitive, bipolar [8–10] and MOS transistors [11], resistors, and diodes. For example in the bipolar transistor, Vbe is strongly affected by temperature; as a result, the turn on behavior of this device in a circuit is affected. For a MOS transistor the drive characteristics and channel resistance are affected by changes in carrier mobility brought on by temperature changes. As the carrier mobility changes with temperature, the value of resistors shift, thereby changing bias conditions and currents within the circuit. There are numerous other sensitivities as well. The circuit designer must build in compensation for variations that occur due to thermal effects into the circuit. As a result the performance and size of the circuit is proportional to our ability to control thermal effects. While this study focuses on the output transistors, since they dissipate most of the power, it is important to note that the heat produced by the output cells will also affect the surrounding devices by heating them up.

A key design consideration for a SOI chip is how to effectively dissipate the heat from the transistor level through the package level into the ambient. There are a number of heat transfer papers in semiconductor industry that either discussed the transistor level heat problem or thermal flow in package assembly. In the heat flow analysis for a transistor level, the impact of heat flow through interconnect and assembly package is not considered. While in the heat transfer analysis of package level, the layout of transistor device and interconnect including the wires are neglected due to the difficulty of huge scale differences between device and assembly package levels. There are two major methods for heat transfer evaluation, one is through the computational fluid dynamics (CFD) based finite volume method (FVM), which is good for assembly package level but is not optimal at the device level. The other method is based on classical heat transfer equation (first law of thermodynamics) in a solid domain with three types of boundary conditions. Both methods have challenges to overcome in order to simulate heat transfer with natural convection. The non-CFD method is relatively simple and it is possible construct complicated conductive models from device to package level; however, to use it we need to determine the heat transfer convection coefficient.

This section investigates the heat transfer model for a SOI design that includes heat transfer at both the device level and at the package level, through the use of the solid finite element method. An iterative algorithm is developed to determine the convection heat transfer coefficients at the surfaces of the package that are exposed to ambient. A model that refines the local SOI device level with interconnect metallization and a global model that covers the assembly package with heat exchange to ambient are developed. Different device design parameters such as SOI thickness and different oxide isolation layouts are simulated to get the best heat transfer solution. Different die sizes and thicknesses are also studied in order to obtain the lowest thermal resistance and high heat transfer rates. Furthermore, the impact of assembly package system under natural convection and different air flow rates are simulated.

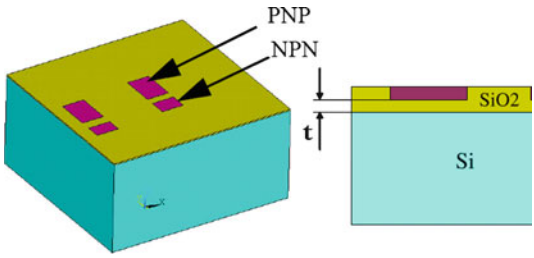


Fig. 6.41 Silicon device layout

Modeling results give the thermal resistances junction to ambient and between any design points of interest. Finally, a comparison between the FEA modeling solution and a simplified thermal network/test shows good agreement. This increases the confidence in our SOI design and shows the effectiveness of our heat modeling method from device level to assembly package board level.

6.4.2 FEA Modeling Analysis for the SOI Device and SO Assembly Package Level

The device and package board level system simulated using FEA included the circuit board, package and the product die. The die itself was simplified by ignoring the logic and control circuits, and only including the output transistors which are responsible for the majority of the heat dissipation. The two output circuits are made up of paired npn and pnp bipolar transistor arrays. The thermal load was applied uniformly to the body of the devices. The simplified circuit used is shown in Fig. 6.41. The left side of the figure shows the I/O cells considered. The right hand side of the figure shows a cross section where the thickness of the bottom oxide is denoted by t.

Figure 6.42 shows a SOIC eight package studied in this work. The package size in millimeters is $4.90 \times 3.90 \times 1.75$, with a lead pitch of 1.27 mm. The die thickness is 14 mils. The printed circuit board used is shown in Fig. 6.43. The board is based on a JEDEC standard board and was a two layer board with the dimensions (in millimeters) of 76.2×114.3, and a thickness of 1.6 mm. To simplify the simulation, the simulated board did not have the full traces but had a copper plate area with its thickness reduced to produce the same thermal conductivity as the actual board with traces.

Meshing the model was a significant issue since the size of the mesh at the transistor level was very small. In order to keep runtimes reasonable the mesh size at the PCB level needed to be significantly larger. Mesh size transitions need to be smooth to keep the numerical characteristics of the model acceptable. To simplify the problem, we scale the thickness of the copper plating on the PCB by the typical expected copper coverage on an etched board. This is an approximation that is

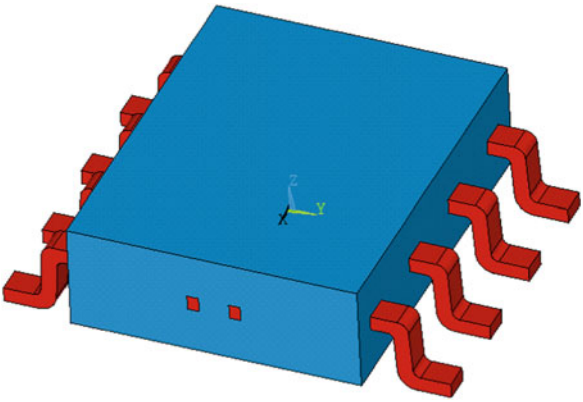


Fig. 6.42 The SO-8 package

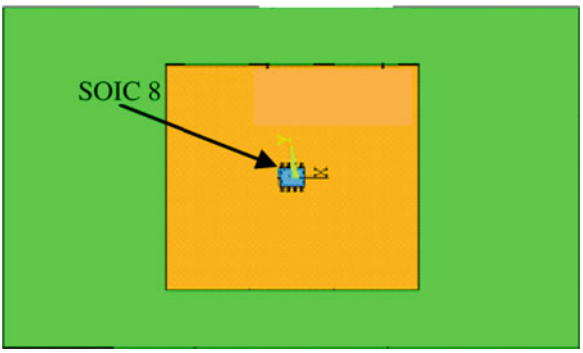


Fig. 6.43 The board level system with mounted SO-8 package

reasonable, since each application circuit board will have different etchings, and different thermal conductivities as a result.

In the simulations a continuous power input of 0.1 W per channel is used with an ambient temperature of 25°C. Simulations were done with both natural and forced convection. The forced convection used airspeeds of 250, 500, and 900 ft/min. Table 6.2 gives the thermal material properties for the FEA modeling.

6.4.3 Thermal Modeling Results and Discussion

The FEA models provide a good tool with which to explore potential design changes to improve the thermal characteristics. This study examined the potential benefits of changes to device size, oxide thickness changes, metallization, and die

Table 6.2 Material properties for FEA

Material	Thermal conductivity (W/mK)
Silicon	145
Mold compound	0.7
Die attach epoxy	2.4
Lead frame	277.0
30% coverage copper PCB	115.8
Copper	386
FR4 PCB	0.35
SiO_2	1.379

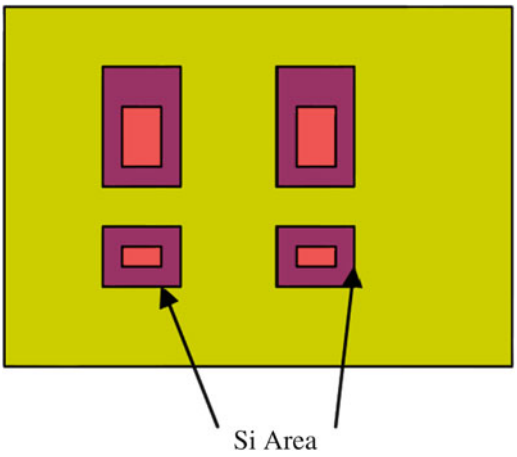


Fig. 6.44 Silicon mesa area increase

thickness. The measures used for evaluating changes were the θ_{JA}, and a similar measure, θ_{JB}, which is introduced to gauge the thermal dissipation through the bottom oxide. θ_{JB} is defined here to be a measure between the transistor tub and silicon below the bottom oxide. θ_{JB} is not defined to be to the exterior of the package (not like the regularly definition junction to the board).

Increasing the size of the silicon mesas containing the driver devices was examined. Figure 6.44 shows the change schematically. The area of the driver was expanded to area 2: 2× and area 3: 3× the size of the original die. To examine only the thermal effects the active area of the transistor was kept the same. Whether this would be done in the actual device would be dependent on the importance of a lower $R_{Ds(on)}$, as compared to other parameters, such as an increase in capacitance.

The data obtained and shown in Fig. 6.45 demonstrates that expanding the transistor area has little benefit by itself. Expanding the device itself would lower $R_{Ds(on)}$ and thus reduce the heat generation.

The effect of thickness of bottom oxide on thermal resistance can be seen in Fig. 6.46 to have a substantial effect on the thermal performance. This result is not unexpected since for a non-SOI circuit the thickness of the silicon die itself has a

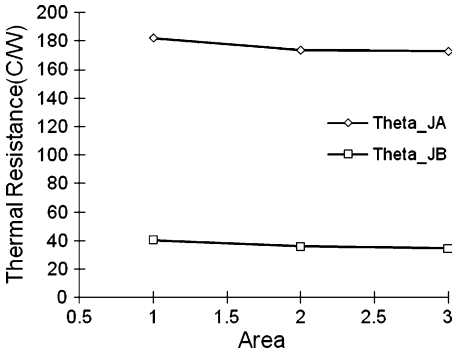


Fig. 6.45 Silicon mesa area results

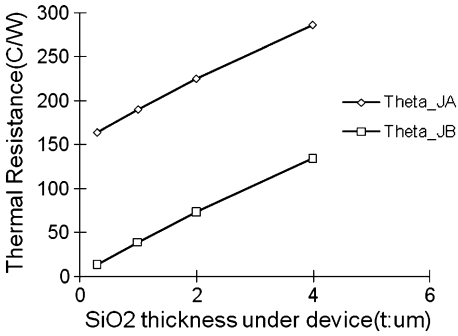


Fig. 6.46 Bottom oxide results

significant effect because the dap and package bottom provide a large amount of the heat sink capacity.

Figure 6.47 shows θ_{JA} as a function of airflow for two different epitaxial silicon thicknesses, d. The two curves overlay one another so the thickness of the silicon above the bottom oxide has virtually no effect on the thermal resistance, the difference in JA was about 0.5%. This result is not unexpected because the thermal conductivity of silicon is much higher than for the surrounding oxides.

The effect of varying the die thickness, as shown in Fig. 6.48 above for the side view of the die (at the center of the package), by back grinding the wafer was examined. This will change the silicon thickness below the bottom oxide. As the die thickness is decreased it should improve the thermal performance. However, we find that simply decreasing the die thickness actually increases the thermal resistance. The results are shown in Table 6.3. We see that the maximum temperature for the thinner die is higher, as is θ_{JA}. This seemingly contradictory result is a result of only changing the die thickness.

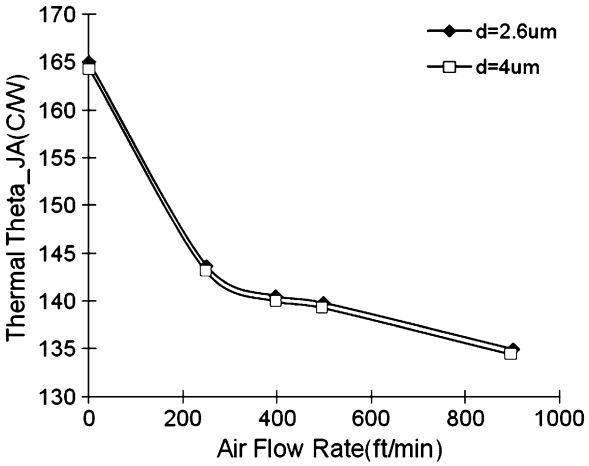


Fig. 6.47 Epitaxial silicon thickness *d* and airflow

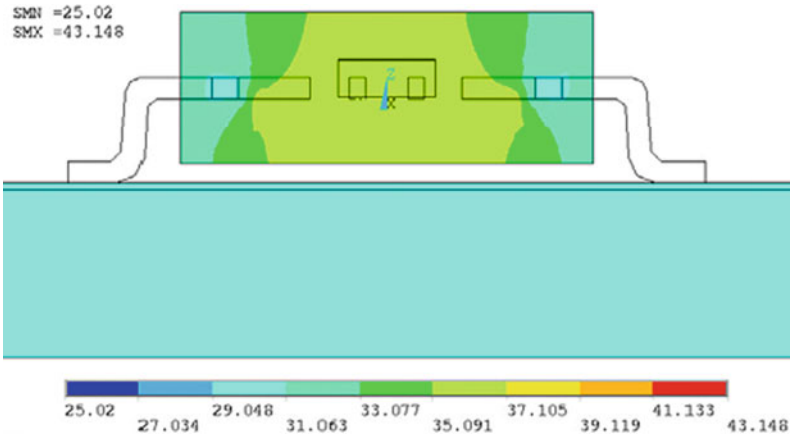


Fig. 6.48 Side view of the die and package

We note that if the die thickness is decreased and the same mold is used, the resulting thickness of the mold compound above the die will increase; as a result, the thermal resistance of this path increases. Thus, to gain the benefits of a thinner die, the mold must be changed so that the thickness of the mold compound does not increase. This result is valid for the package being considered for which the thickness of the mold compound above the die was substantially changed by the final wafer thickness. If the package has a much thicker mold compound thickness, this effect should become negligible. The effect of bond wires and the die metallization as thermal paths was considered. If the metal is not a significant thermal path, then we can safely ignore the metallization for future simulations. Figure 6.49 shows the die with the I/O cell metallization in place and bond wires attached.

Table 6.3 Die thickness vs. thermal resistance

Die thickness	8 mil	14 mil
T_{max}	44.7°C	43.2°C
θ_{JA}	197.0°C/W	181.5°C/W

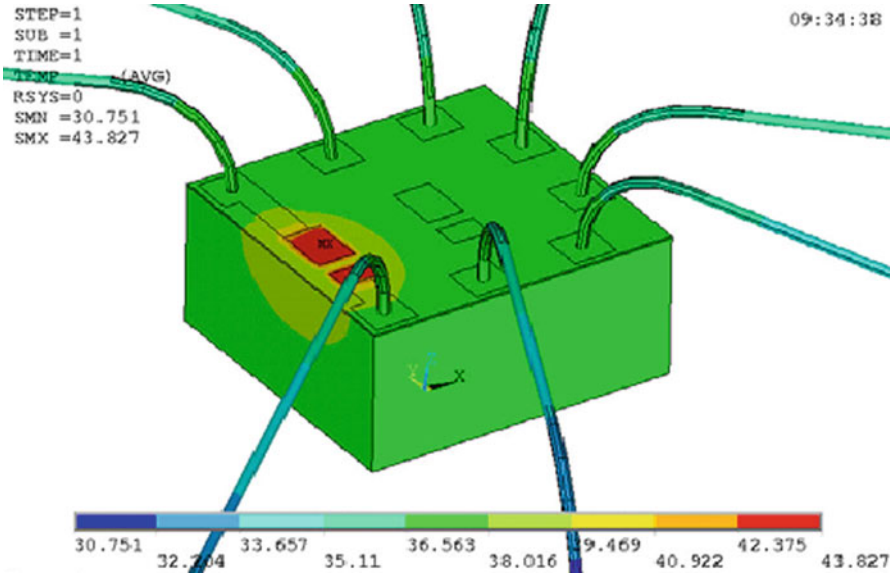


Fig. 6.49 Die with bond wires and I/O metals

This was compared to a similar chip where the metallization was not present. We can see from Fig. 6.49 that the bond wires only support a temperature gradient for a short distance. Figure 6.50 shows the die metallization, and similar to the bond wires, there is only a short distance that a thermal gradient is supported over before the metal temperature becomes the same as the underlying oxide and silicon. Thus, the metal may act as a local heat sink, but overall for the die, it provides little benefit. For the simulation without bond wires or circuit metallization considered, we obtained $\theta_{JA} = 190°C/W$. When bond wires and the I/O metal are included, the thermal θ_{JA} decreases to 188°C/W. The result of these two simulations shows that bond wires and the metallization change the result by 1%, so it is not important to consider them here.

The final comparison was done for the effect of die size. The simulations assumed that the power dissipation would be the same for the two die. This scenario typically occurs for a circuit if it is initially autorouted and later it is redesigned and is tightly hand packed. Figure 6.51 shows die with areas of 720 × 690 and 1,100 × 920 μm^2 at several airflow rates. For all airflows in the study, the θ_{JA} is substantially lower with the larger die case. The difference is nearly a constant 10°C/W.

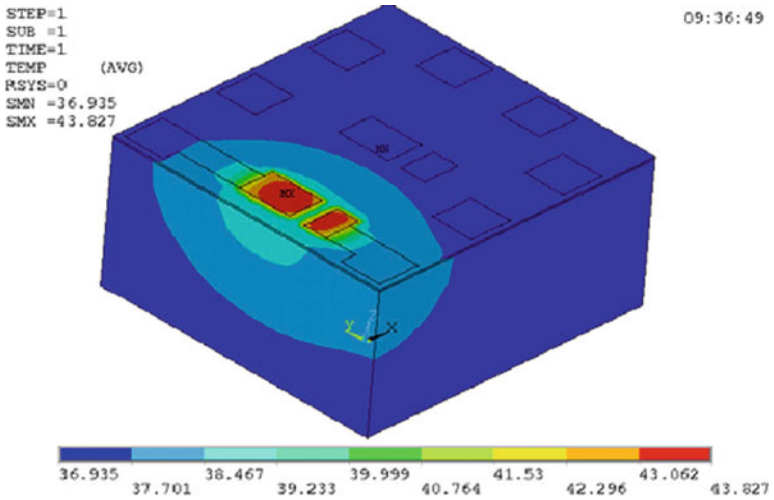


Fig. 6.50 Thermal distribution in metallization of die

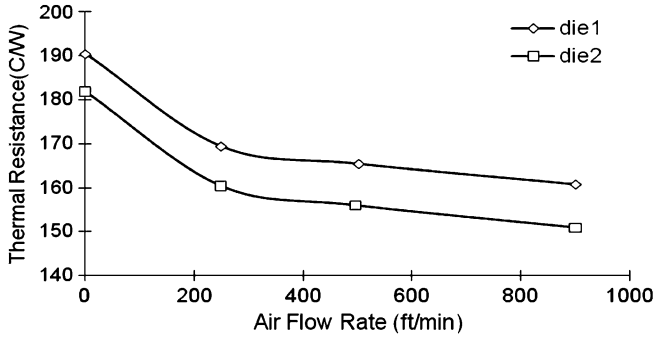


Fig. 6.51 Thermal resistance vs. air flow rate with two die areas (die 1 = 720 × 690 μm^2 and die 2 = 1,100 × 920 μm^2)

6.4.4 Equivalent Resistance Method with Thermal Net

The thermal characteristics of the SOI wafer were modeled using a resistor network [12, 13]. Figure 6.52 shows a schematic of the equivalent circuit that was used. In the equivalent circuit temperature plays the role of electrical potential in a normal electric circuit. The thermal equivalent circuit is made up of five resistors. Three R_{well} resistors model the thermal diffusion in the body well of the transistor. There is a resistor for each of the four sidewall oxide trenches, and one for the bottom oxide. Finally, a resistor representing the heat flow through the bulk of the silicon to the package DAP is obtained.

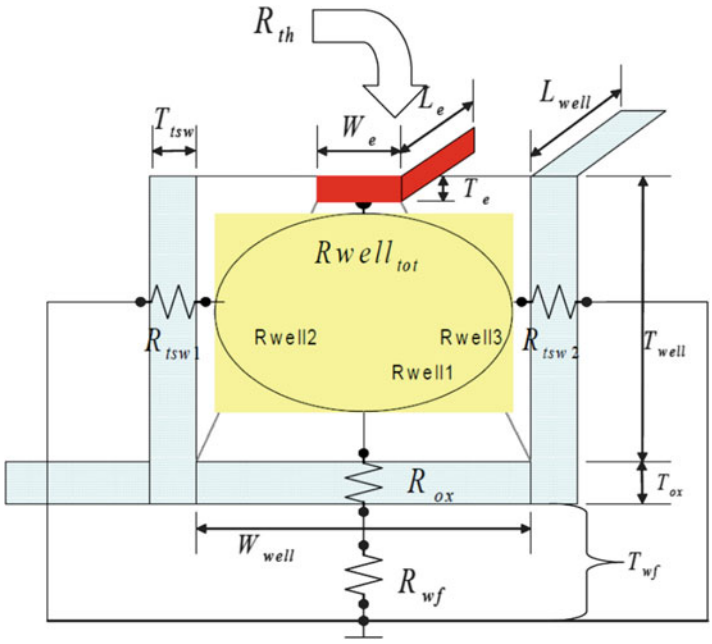


Fig. 6.52 Equivalent thermal circuit

The heat flow per unit area of the sidewall oxide is proportional to the temperature differences, and the area of the oxide. As a result, the resistors can be geometrically scaled. The heat source is taken to be the emitter of the device being considered. The first of the thermal resistors R_{well_1}, representing the thermal conduction towards the bottom oxide, can be calculated using equation (6.9) with the assumption of a trapezoidal distribution from the localized emitter heat source to the bottom oxide.

$$R_{\text{well}_1} = \frac{T_{\text{well}}}{k_{\text{si}} \cdot (L_{\text{e}} \cdot W_{\text{well}} - W_{\text{e}} \cdot L_{\text{well}})} \cdot \ln\left(\frac{L_{\text{e}} \cdot W_{\text{well}}}{W_{\text{e}} \cdot L_{\text{well}}}\right) \tag{6.9}$$

where T_{well}, L_{well}, and W_{well} are the thickness, length, and width respectively of the silicon well, L_{e} and W_{e} are the emitter length and width, respectively, k_{si} is the equivalent thermal conductivity of silicon.

The next resistors, R_{well_x}, represent the thermal conduction to the sidewalls and can be calculated as by equation (6.10)

$$R_{\text{well}_x} = \frac{(L_{\text{well}} - W_{\text{e}})}{k_{\text{si}} \cdot (L_{\text{e}} \cdot W_{\text{well}} - T_{\text{e}} \cdot L_{\text{well}})} \cdot \ln\left(\frac{L_{\text{e}} \cdot T_{\text{well}}}{T_{\text{e}} \cdot L_{\text{well}}}\right) \tag{6.10}$$

where T_{e} is the thickness of the emitter, and the index x is 2 or 3 for the two sides included.

The total resistance of the silicon well, $R_{\text{well}_{\text{tot}}}$, can be calculated with equation (6.10). This equation adds the resistor values as a set of parallel resistors.

$$R_{\text{well}_{\text{tot}}} = R_{\text{well}_1} || R_{\text{well}_2} || R_{\text{well}_3} \tag{6.11}$$

Next, the value of the resistors representing the oxide box surrounding the silicon well cavity is calculated.

$$R_{\text{ox}} = \frac{T_{\text{ox}}}{k_{\text{ox}} \cdot (W_{\text{well}} + a \cdot T_{\text{ox}}) \cdot (L_{\text{well}} + a \cdot T_{\text{ox}})} \tag{6.12}$$

Equation (6.12) calculates the equivalent resistance of the bottom oxide, R_{ox}. Where k_{ox} is the equivalent thermal conductivity of the oxide, a is a spreading function of the heat over the oxide of the adjacent wells, and T_{ox} is the thickness of the bottom oxide. From the FEA modeling, $a = 0.5$.

The thermal resistance of the trench sidewall, R_{tsw} can be calculated as

$$R_{\text{tsw}} = \frac{T_{\text{tsw}}}{2 \cdot k_{\text{ox}} \cdot T_{\text{well}} \cdot (\varepsilon_x \cdot W_{\text{well}} + \varepsilon_y \cdot L_{\text{well}})} + \frac{R_{\text{bulk}} + R_{\text{ox}}}{a_{xy} \cdot 4} \tag{6.13}$$

where T_{tsw} is the thickness of the sidewall trench oxide, ε_x and ε_y are spreading functions for the heat over the trench wall area. $\varepsilon_x = \varepsilon_y = 0.5$, based on FEA modeling.

The resistance of the wafer below the bottom oxide, R_{wf}, can be calculated as below equation (6.14)

$$R_{\text{wf}} = \frac{1}{4 \cdot k_{\text{si}} \cdot \sqrt{(W_{\text{well}} + a \cdot T_{\text{ox}}) \cdot (L_{\text{well}} + a \cdot T_{\text{ox}}) + \left(\frac{\pi \cdot (T_{\text{ox}} + T_{\text{tsw}})}{2}\right)^2}} \tag{6.14}$$

The overall value for the thermal resistance is then given as $R\text{th}_{\text{calc}}$ by equation (6.15)

$$R\text{th}_{\text{calc}} = R_{\text{well}} + \lfloor R_{\text{ox}} + R_{\text{wf}} \rfloor || R_{\text{tsw}} \tag{6.15}$$

In order to demonstrate accuracy of Rth calculations, the resulting values were correlated to the previously discussed FEA simulations which achieved results through a completely different approach. Each approach had slightly different assumptions. If the two approaches give similar results, it increases confidence in both methodologies. The 3D simulation assumed uniform heat source to well cavity. The Rth equations take into account spreading of heat from emitter as source to bottom and side oxides. The final compensated value calculated by the equivalent circuit method is: Rth = 1,037°C/W for both the PNP and the NPN. 3D simulations were taken on entire NPN and PNP output arrays. This translates to 16 PNP and 8 NPN devices on product output (24 devices total). The equivalent model needs to be scaled to match. The calculated Rth = 1,037/24 = 41.8°C/W,

Table 6.4 Comparison between the FEA and the thermal circuit method

	FEA (°C/W)	Thermal circuit method (°C/W)	Relative difference (%)
*R*th	39.6	41.8	5.8

while for the same conditions the FEA method returns the resistance 39.6°C/W (see Fig. 6.45, θ_{JB} at area 1). The difference in two results is 5.8% (see Table 6.4). The modeling results discussed have been verified by the development of products utilizing the predicted thermal resistance.

6.5 Multiple-Die Thermal Analysis

6.5.1 Multiple-Die Thermal Resistance Definition

Typical multiple die packages contain dies either in a vertical (stacked) arrangement or in a lateral (side by side placement) arrangement. Multiple die module and 3D stacked die packages are especially common today in power electronics [14] and in hand-held devices, especially in cell phones and digital cameras, which require fast turnaround, very high level of integration, and low cost that is characteristic in general for SiP solutions.

Considering the thermal coupling effect between the heating chips and the equation (6.1), the thermal resistance of junction to any reference temperature in a multiple chip system in package may be defined as

$$R_{ij} = \frac{T_{ij} - T_{\text{ref}}}{P_{\text{j}}} \tag{6.16}$$

where R is the thermal resistance of junction to a reference temperature point, i, $j = 1, 2$ as shown in Fig. 6.53.

The junction temperature at die 1 and 2 can be expressed as

$$\begin{aligned} T_1 - T_{\text{ref}} &= (T_{11} - T_{\text{ref}}) + (T_{12} - T_{\text{ref}}) \\ T_2 - T_{\text{ref}} &= (T_{21} - T_{\text{ref}}) + (T_{22} - T_{\text{ref}}) \end{aligned} \tag{6.17}$$

In general, one can say, that in a given test environment, a multidie package (having any kind of arrangement) is totally represented by its full thermal impedance matrix in the form shown by equation (6.18). Here, T_{j} represents the junction temperature of die j, R_{ii} describes the thermal resistance on die i and R_{ij} stands for the thermal resistance on die i with the coupling heating from die j. Multiplying the thermal resistance matrix $[R_{ij}]$ with the vector of power $[P_{\text{j}}]$ applied at the chips and plus the ambient temperature T_{a}, one can obtain the corresponding vector of the junction temperature T_{j} at all die.

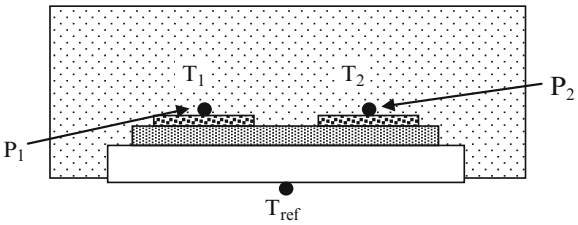


Fig. 6.53 A typical side by side placed die system

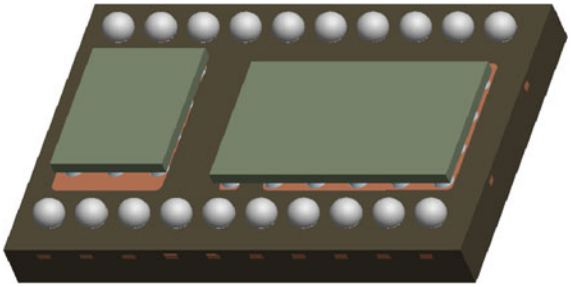


Fig. 6.54 An example of a multiple-die power package

$$[T_j] = [R_{ij}][P_j] + [T_a] \tag{6.18}$$

6.5.2 *Application of a Power Multiple-Die Thermal Resistance*

An example of the stacked die power system package is shown in Fig. 6.54 (as we have discussed it in Chap. 5), the larger die is the low side MOSFET and the smaller die is the high side MOSFET. There is an IC controller die which is stacked on the other side of the low side MOSFET dap. The package was mounted on a JEDEC 1s0p board. The JEDEC board for the stacked die power package is showed in Fig. 6.55. Figures 6.56 and 6.57 show two cases that the power has been applied to low side die and high side die separately. Due to the power dissipation in IC control is very small as compared to the two MOSFET die in this example, we do not consider the heat effect of IC die. The thermal resistances of junction to ambient $R\theta_{JA}$ with the power applied to low side die and high side die separately are measured and recorded in the Table 6.5. In this table, R_{11} is the thermal resistance of junction to ambient for low side die due to the power is applied to the low side die. R_{12} is the thermal resistance of junction to ambient for high side die due to the power is applied to the low side die. R_{21} is the thermal resistance of junction to ambient for low side die due to the power is applied to the high side die. R_{22} is the thermal resistance of junction to ambient for high side die due to the power is applied to high side die. After these thermal resistances are measured, we need to

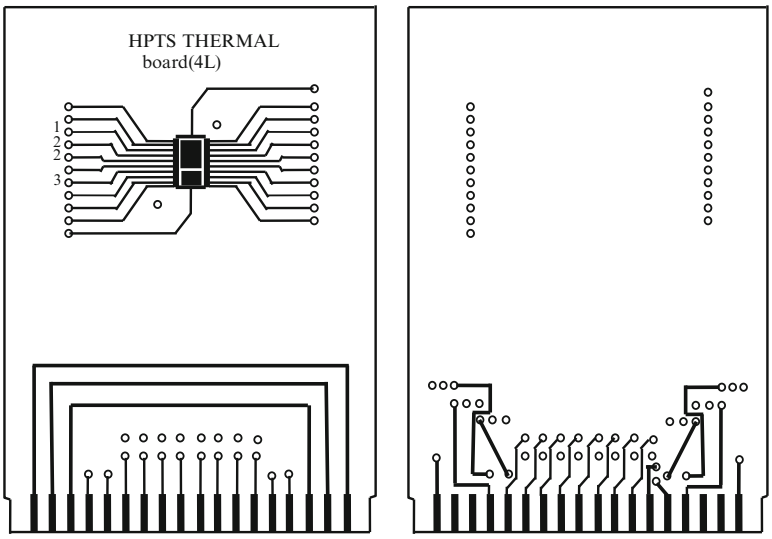


Fig. 6.55 The JEDEC board with 1s0p layout

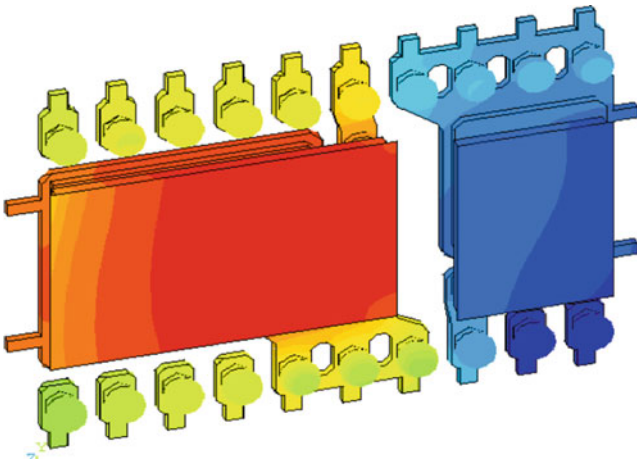


Fig. 6.56 Power is applied on the low side die

find out the junction temperatures of both high side die and lower side die. Based on equation (6.18), the junction temperatures (°C) on low side die and high side can be estimated as the follows:

$$\begin{bmatrix} T_{j1} \\ T_{j2} \end{bmatrix} = \begin{bmatrix} R_{11} & R_{12} \\ R_{21} & R_{22} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \end{bmatrix} + \begin{bmatrix} T_a \\ T_a \end{bmatrix} = \begin{bmatrix} 124.6 & 75.8 \\ 83.1 & 141 \end{bmatrix} \begin{bmatrix} 0.78 \\ 0.67 \end{bmatrix} + \begin{bmatrix} 25 \\ 25 \end{bmatrix}$$
$$= \begin{bmatrix} 173 \\ 184.3 \end{bmatrix} \tag{6.19}$$

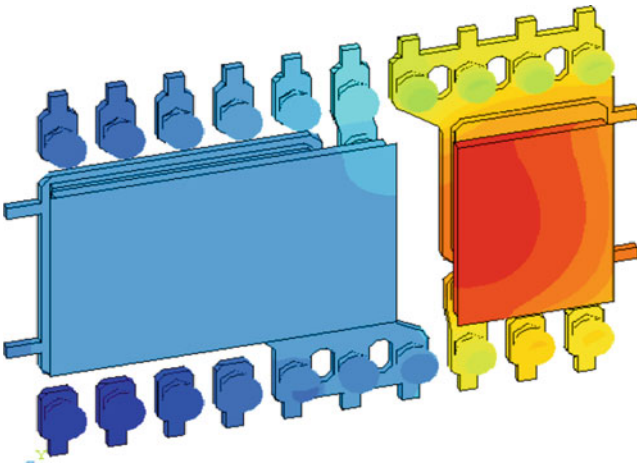


Fig. 6.57 Power is applied on the high side die

Table 6.5 The thermal resistance measurement of the stacked die power package

Power applied on low side (W)	T_a (°C)	R_{11} (°C/W)	R_{12} (°C/W)
0.78	25	124.6	75.8
Power applied on high side (W)	T_a (°C)	R_{21} (°C/W)	R_{22} (°C/W)
0.67	25	83.1	141

The junction temperature of low side die is 173°C and the junction temperature of high side die is 184.3°C.

Another example is a power package with six IGBT die, as shown in the schematic drawing of Fig. 6.58. Assume the power dissipation is 5.31 W on each chip. The ambient is under natural convention and the air and heat sink temperature is about 25°C. The reference point is selected at the package bottom center, which is the package case center point.

After applying the power on single chip one by one, and consider the heating coupling iterations between the six IGBT chips, the thermal resistance matrix of junction to case based on FEA can be written as:

$$[R_{ij}] = \begin{bmatrix} 1.75 & -0.0064 & -0.009 & 0.001 & -0.0011 & -0.005 \\ 0.012 & 1.696 & 0.012 & -0.002 & -0.007 & -0.002 \\ -0.008 & -0.0062 & 1.914 & -0.004 & -0.0010 & 0.005 \\ -0.004 & -0.081 & -0.009 & 1.823 & 0.093 & 0.004 \\ -0.007 & -0.077 & -0.006 & 0.109 & 1.81 & 0.115 \\ -0.009 & -0.081 & 0.0004 & 0.004 & 0.113 & 1.89 \end{bmatrix} \text{°C/W} \tag{6.20}$$

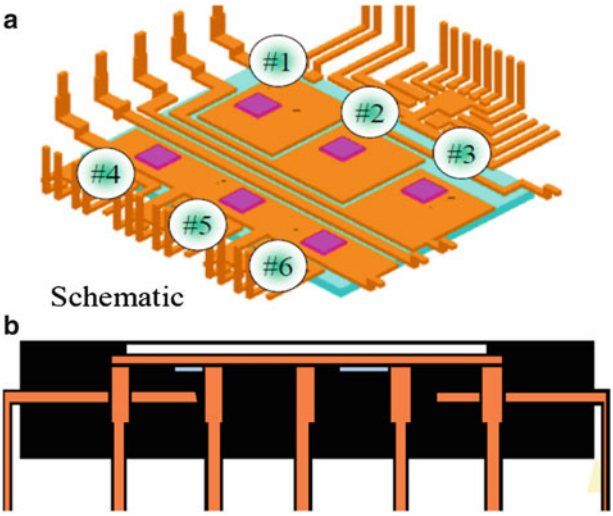


Fig. 6.58 The schematic drawing of the six die power package. (**a**) Lead frame and die. (**b**) Package side view

Through (6.20), it is easy to estimate the junction temperatures of each IGBT die. The measured thermal resistances of junction to the case for the IGBT individual chips are listed as below (except the No. 1 chip, due to the test failed):

$$[R_{ij}] = [\,\#.\#\quad 1.81\quad 1.94\quad 2.09\quad 2.22\quad 1.95\,]\ ^\circ\text{C/W} \tag{6.21}$$

Compared the diagonal resistance of the matrix (6.20) and the measured thermal resistance terms in (6.21), the max relative difference is at the No. 5 die, which is about 18%. The difference could be induced by either the test system error or the thermal contact resistance under the No. 5 chip.

6.6 Cooling for Power Packaging

6.6.1 Air Flow Cooling

Typical air flow cooling is designed through the power package structure itself or through the heat sinks. For lower power application like in the mobile phone or portable products, the power package design may include built-in heat sink like the exposed metal clip or the thick folded lead frame or the exposed drain or source directly. However, for median and high power, the external heat sink is necessary. This section majorly focuses on the external heat sink for the power packaging.

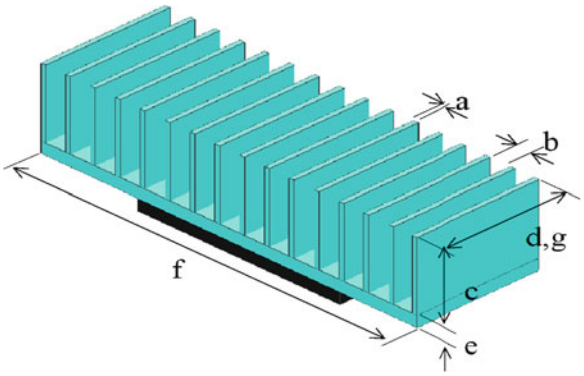


Fig. 6.59 A 16 fin external hest sink mounted on a power package

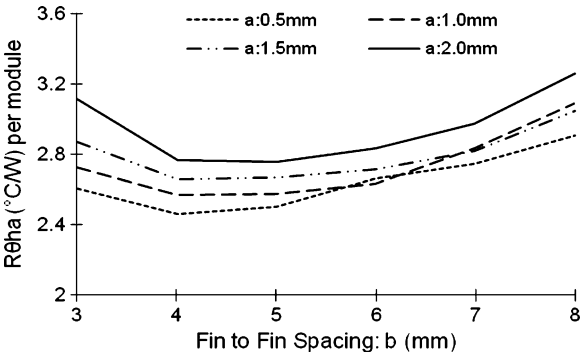


Fig. 6.60 The thermal resistance of heat sink junction $R\theta_{ha}$ to ambient vs. heat sink fin space with different fin thickness

6.6.1.1 External Heat Sink Design

In Fig. 6.59, the heat sink design variable a is the fin thickness; b is the fin spacing; c is the fin height; d is the fin length; e is the base plate thickness of the heat sink; f is the base plate width of the heat sink and g is the base plate length of the heat sink.

Figure 6.60 gives the thermal resistance of heat sink junction to the ambient $R\theta_{ha}$ vs. the design variable fin to fin spacing with different fin thicknesses. It can be seen from the Fig. 6.60 that there is an optimized fin to fin space (4 mm in this case) with the thinnest fin (0.5 mm).

Figure 6.61 shows that the thermal resistance of the heat sink junction to ambient changes with the fin and base plate lengths in natural convention and different air flow rates. The larger air flow speed and more fins have clearly reduced the thermal resistances.

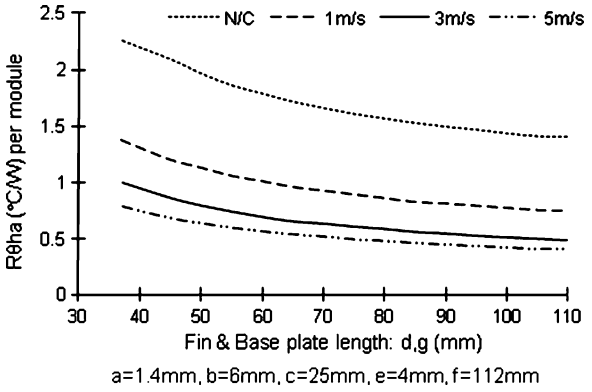


Fig. 6.61 The thermal resistance vs. fin/base plate length under different air flow speed

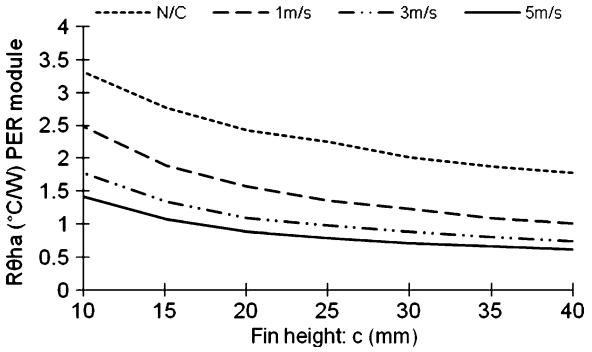


Fig. 6.62 The thermal resistance vs. fin height under different air flow speed

Figure 6.62 shows that the thermal resistance of the heat sink junction to ambient changes with the fin height in natural convention and different air flow rates. The larger air flow speed and high fin have clearly reduced the thermal resistances.

6.6.1.2 The Application of the External Heat Sink for Power Module

Figure 6.63 shows a nine fin heat sink mounted on a side by side placed power module. The parameters of the heat sink are as follows: fin thickness $a = 1.5$ mm, fin spacing $b = 6.0$ mm, fin height $c = 25$ mm, fin length $d = 37$ mm, base plate thickness $e = 4.0$ mm, base plate width $f = 61$ mm, and base plate length $g = 37$ m. The average thickness of thermal grease is about 50 μm; the ambient temperature is 40°C. The electrical parameters applied to the power module are as follows: The power applied to the IGBT is 3.2 W and to the FRD is 0.44 W; $V_{dc} = 300$ V; $f_s = 15$ kHz; $I_{rms} = 3.0$ A.

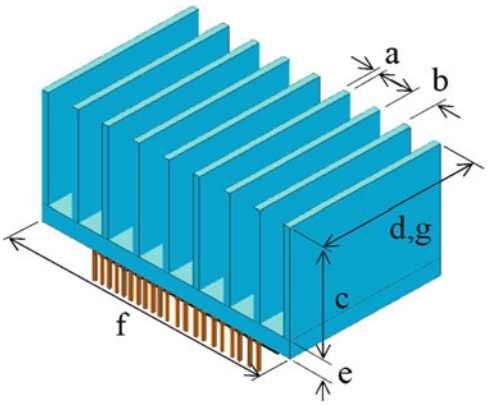


Fig. 6.63 A nine fin heat sink mounted on the power module

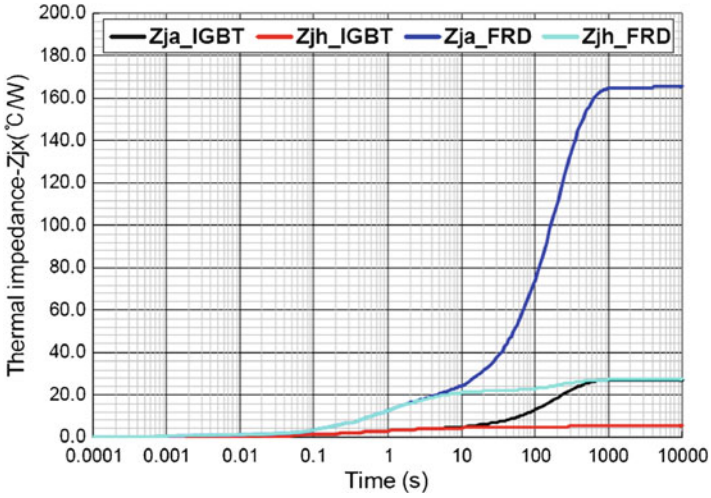


Fig. 6.64 Transient thermal impedances vs. time for the IGBT and FRD die junction to the ambient Z_{ja} and heat sink Z_{jh}

Figure 6.64 shows the transient impedances junction to ambient (Z_{ja}) and junction to heat sink (Z_{ja}) of power transistor IGBT and power diode FRD. The power diode FRD has much higher transient thermal impedances of both junction to ambient and heat sink than the IGBT die. Figure 6.65 gives the curve of transient thermal impedance junction to case (Z_{jc}) of IGBT die, it takes 1 s to reach the maximum temperature.

The cooling method may be taken different design styles from inside and outside power package. Figure 6.66 gives a design style that uses the ribbon bonding as the electrical connection and thermal path (internal heat sink).

Heat sink may also be mounted in double side of the power chip. Figure 6.67 shows the top and bottom heat sinks mounted on an IGBT die.

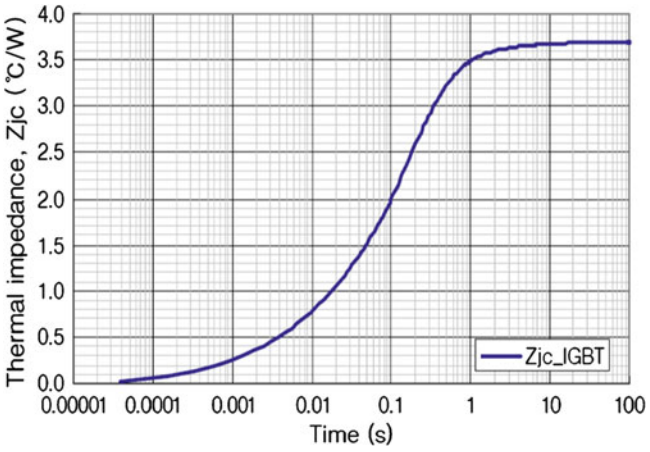


Fig. 6.65 Transient thermal impedances vs. time for the IGBT die junction to the case Z_{jc}

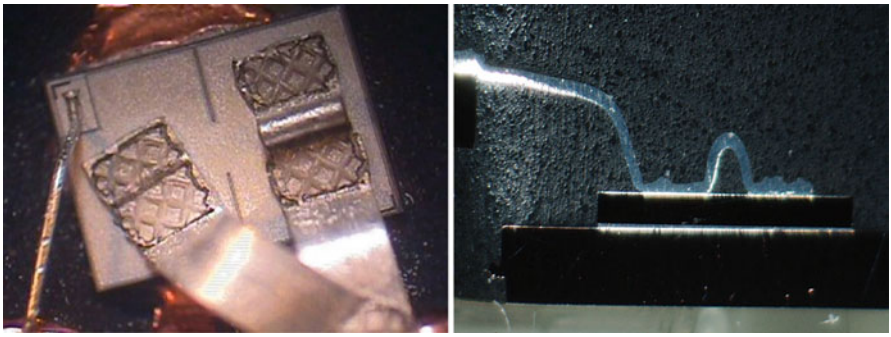


Fig. 6.66 Ribbon bonding as both electrical and thermal paths

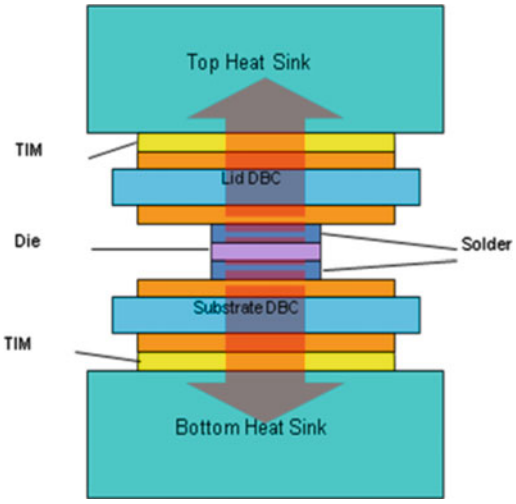


Fig. 6.67 Double side cooling for a power die

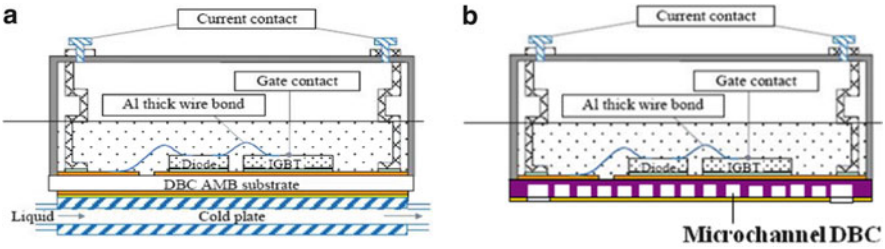


Fig. 6.68 Power module with DBC on the liquid cooling with tube cold plate and the direct microchannels on DBC. (**a**) Tube cold plate [15]. (**b**) DBC with microchannels

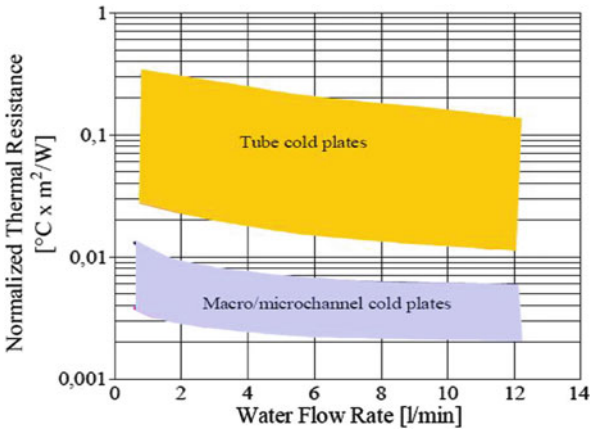


Fig. 6.69 Comparison with the tube cold plate and the macro/microchannel cold plate [15]

6.6.2 Other Cooling Methods

Besides the airflow cooling, there are liquid cooling, microchannel cooling, and the electrical-thermal cooling methodologies for high power application.

Figure 6.68 lists the power module sits on the tube cold plate with DBC (a) and the DBC is manufactured with microchannels (b) where the power chips are mounted. Figure 6.69 shows the comparison between the tube cold plate and the macro/microchannel cooling methods [15], the results showed that the macro/microchannel cooling is much better than the tube cold plate cooling method.

Figure 6.70 shows a concept of building the microchannel in back metal of a power die at wafer level, this idea may have very high efficiency to take the heat directly from power chip [16].

Figure 6.71 shows the example of the thermoelectronic cooling method which uses the P type and N type of the pellets to absorb the heat from top and reject heat from bottom. The power device may be mounted on top of the thermoelectronic cooling plate to take the heat out the power device.

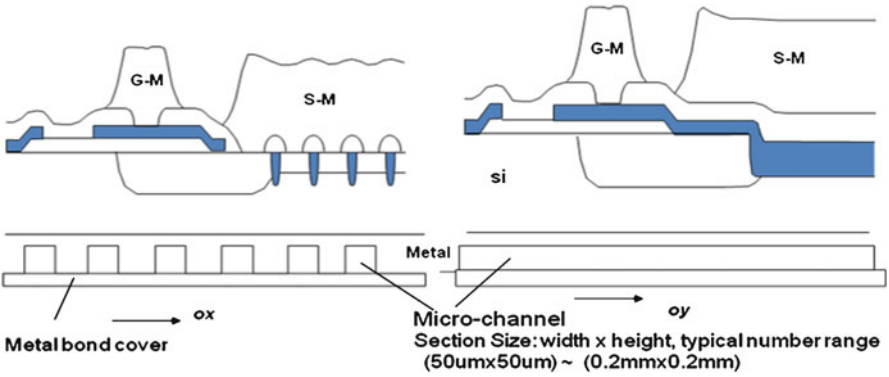


Fig. 6.70 Building the microchannel inside power die at wafer level

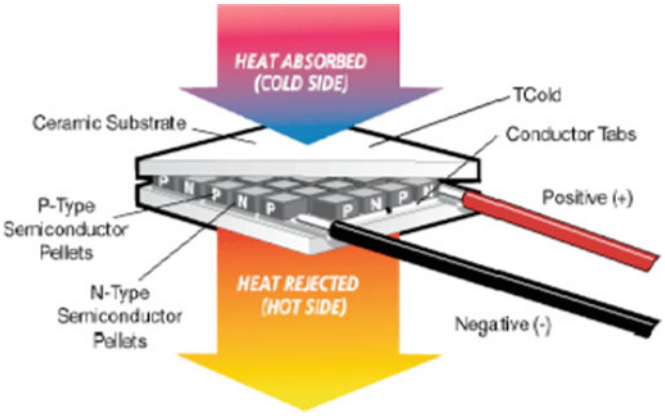


Fig. 6.71 Thermoelectronic cooling

6.7 Summary

This chapter first introduces the thermal resistance definitions and their measurement methods. Then, it introduces the thermal test boards based on JEDEC standards and shows how to select the thermal test boards for different type of power packages. The methods of prediction for the junction temperature and the maximum power dissipation are presented. The thermal analysis and management for different power packages with different design parameters are discussed. After that, this chapter gives a detailed example for the SOI power device heat analysis from device to the package assembly board level. The Multiple die thermal

resistance analysis by matrix method is presented next. Finally, the cooling methods for the power package are discussed with focus on air flow cooling and heat sink design, while other advanced cooling methods such as the microchannel cooling and thermoelectronic cooling are also listed as the reference.

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Chapter 7
Material Characterization for Power Electronics Packaging

The encapsulation of plastic power packages often produces interfacial shear stresses that can lead to failure during temperature cycling. Also surface mounted technology exposes the body of the plastic package to such high temperature during assembly that moisture-related mechanical failure of the package can occur. The selection of materials for both hermetic and nonhermetic package is influenced by the mechanical, electrical, and the thermal requirements of the power device and its surrounding electrical system and by the environmental to which the device will be exposed. The reliability of the packaged power device will depend not only on the characteristics of the individual materials but also on the interaction of package materials at interfaces during exposure to such stresses as thermal gradients, temperature cycling, moisture, and contamination.

7.1 Effect of Polyimide Coating on a MOSFET Die

A typical plastic power package is a package with epoxy mold compound (EMC), which includes silica fillers and resin. Often, the silica filler in the EMC material will contact the silicon die surface directly that will result in the damage of die surface in the loading environments. This section discusses the mechanical behavior of EMC with and without a polyimide coat between the EMC and die.

7.1.1 Issues of the Polyimide and EMC Materials

In general, the power device has multiple layers of dielectrics and polysilicon above the active silicon, which are in turn covered by one or more metal layers, and then passivated by a SiN film with bond pad openings on the top. Between the passivation SiN layer and mold compound, there can be a polyimide layer, as shown in Figs. 7.1 and 7.2 [1]. Polyimide coating may help to eliminate mold compound ions and may also act as a buffer layer to reduce stress from mold compound to die [2]. However, it

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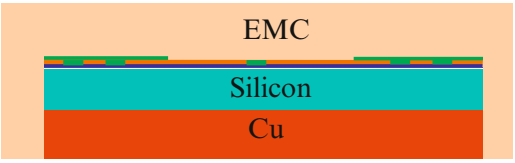


Fig. 7.1 Cross section of package

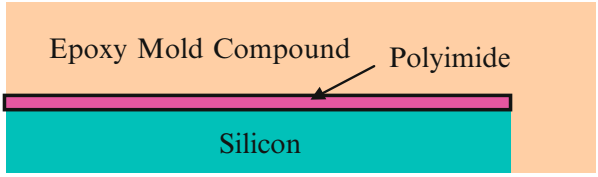


Fig. 7.2 Polyimide coating between silicon and epoxy mold compound

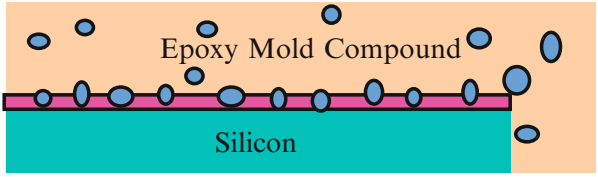


Fig. 7.3 Silica fillers penetrate through thin polyimide coating

is critical to understand the mechanical behavior of the polyimide coat itself. The ultra high thermal expansion coefficient of polyimide coating could be a risk for passivation if the polyimide coat is not well designed, especially when product is working at high temperature and heat is generated intermittently. A thick polyimide coating layer might induce higher stresses in the passivation than thin polyimide coating does. However, silica fillers in the mold compound could penetrate through the thin polyimide coating layers and contact passivation surface directly (see Fig. 7.3). The high thermal expansion coefficient of polyimide coating and hard silica fillers may cause high stress in the passivation.

The challenge here is how to describe the effect of the thin polyimide coat on passivation. If the tiny silica fillers in the EMC penetrate through ultrathin polyimide coat, how does it affect passivation stress distribution? When the polyimide coat thickness is increased and silica fillers do not penetrate through polyimide coat (see Fig. 7.4), how does it impact the passivation stress distribution? These are the material mechanical problems that this section targets. In this section, a 3D FEA model is developed to investigate the material effect of the polyimide coating and EMC with silica filler on passivation reliability. Polyimide coat material is assumed to glue other materials perfectly, while silica fillers are assumed to have two cases with and without contacting the passivation layer. The model that considers different

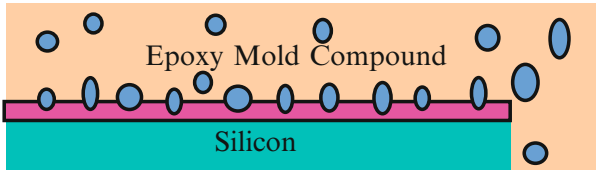


Fig. 7.4 Silica fillers do not penetrate through thick polyimide coating

Table 7.1 Material mechanical behavior parameters

Material	Modulus (MPa)	Poisson's ratio	CTE (ppm/°C)	Yield stress (MPa)
Heatsink	1.3034E5	0.35	17	
Plastic housing	6.2E3	0.4	30	
Solder	1.9E4	0.35	29.4	22.48
Polyimide	3.1E3	0.4	77.0	
Mold compound	1.215E4	0.35	$\alpha 1 = 19.2$ $\alpha 2 = 70.4$	
Silicon	1.69E5	0.23	3.20	
Passivation	2.75E5	0.24	4.00	
Metal PAD	7.03E4	0.346	23.2	110
Silica filler	3.4E5	0.14	0.5	

polyimide thickness, ideal model vs. actual model, silica fillers penetrating the polyimide layer, silica fillers contacting passivation, is fully investigated. The simulation results show that the polyimide coating and silica fillers in mold compound have significant impact on the passivation stress.

7.1.2 Assumptions, Material Properties, and Analysis Method

To conduct an effective simulation and analysis, the following assumptions are made:

1. Assume that the polyimide coating has uniform thickness (in reality, its thickness may not be uniform due to its viscosity).
2. Assume there are small silica fillers and big silica fillers in mold compound. All small silica fillers are same size and all big silica fillers are same size.
3. Assume silica fillers can penetrate through 5-μm polyimide coating.
4. Assume polyimide coating is glued to passivation, metal and mold compound perfectly, and silica fillers glued to mold compound and polyimide coating perfectly. Assume silica fillers have a contact with passivation, and they may have relative motion.

The basic material parameters are listed in Table 7.1 for a power package that is shown as in Fig. 7.5. Solder and metal PAD are nonlinear (bilinear) materials, all of the rest of the materials are considered to be linear elastic.

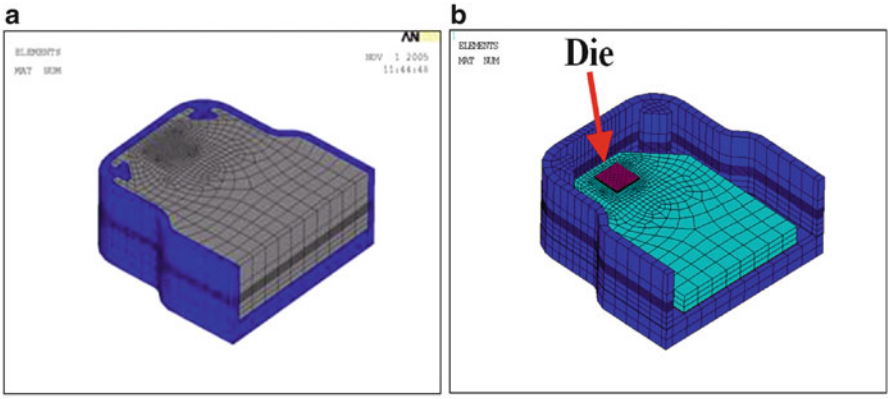


Fig. 7.5 A power package model for automotive application: (**a**) whole package model with EMC, (**b**) not show EMC

A finite element code, ANSYS®, is used in the modeling. A nonlinear transient thermal mechanical model is developed. Figure 7.5 shows the mesh of the global package model, which includes the die, die attach, heat sink, plastic housing and mold compound. One of the advantages of submodeling technique is that the small complicated transition regions can be eliminated in the global model without losing accuracy. Therefore, passivation and silica fillers in mold compound are neglected in the global model and only considered in the submodel.

The 2D drawing of the die and its 3D mesh in submodel is shown in Fig. 7.6. There is an uncovered area on the metal PAD, and the passivation around it is analyzed in the submodel. The submodel, which is cut from the global model, includes partial silicon, passivation, metal PAD, polyimide coating, and partial mold compound as shown in Fig. 7.7. Heat is generated intermittently when the device is in a circuit. Figure 7.8 shows the typical power vs. time in one cycle. Heat generated from silicon die lasts 0.02 s in one cycle, with the period of 2 s.

Measurement shows that the package's temperature increases from room temperature to about 82°C after thousands power pulses. In order to simulate this, two step analysis is needed. First, a thermal simulation is conducted with the initial uniform package temperature 82°C. Then, a mechanical stress simulation is followed with the transient temperature distribution from the thermal simulation as the input.

7.1.3 Analysis Model Without Considering the Silica Fillers in Mold Compound Material

The simulated results for passivation stress with and without polyimide coat (neglecting silica fillers in mold compound) are shown in Figs. 7.9 and 7.10.

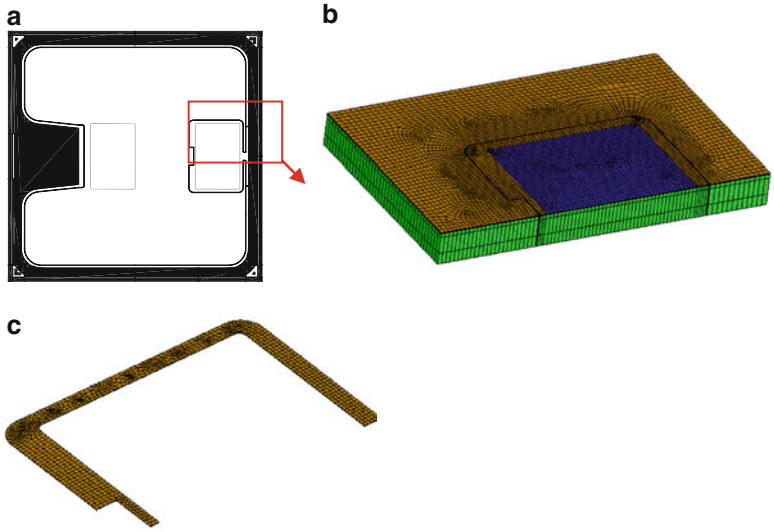


Fig. 7.6 Power die and part of the mesh in submodel: (**a**) 2D drawing of die, (**b**) mesh of die in submodel, (**c**) passivation around the uncovered metal PAD

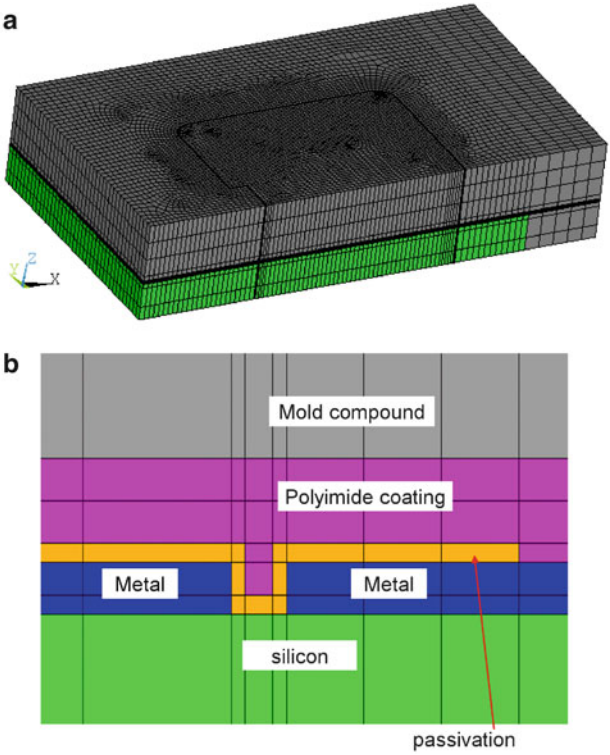


Fig. 7.7 Mesh of submodel (without silica fillers in mold compound): (**a**) submodel (**b**) cross section of the submodel

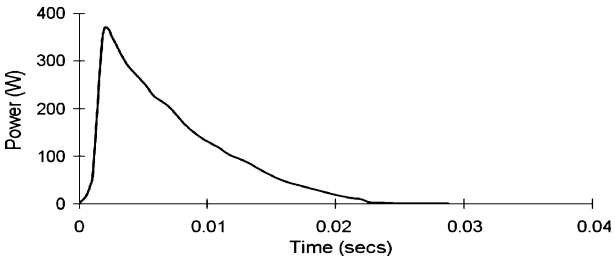


Fig. 7.8 Typical power vs. time in one cycle

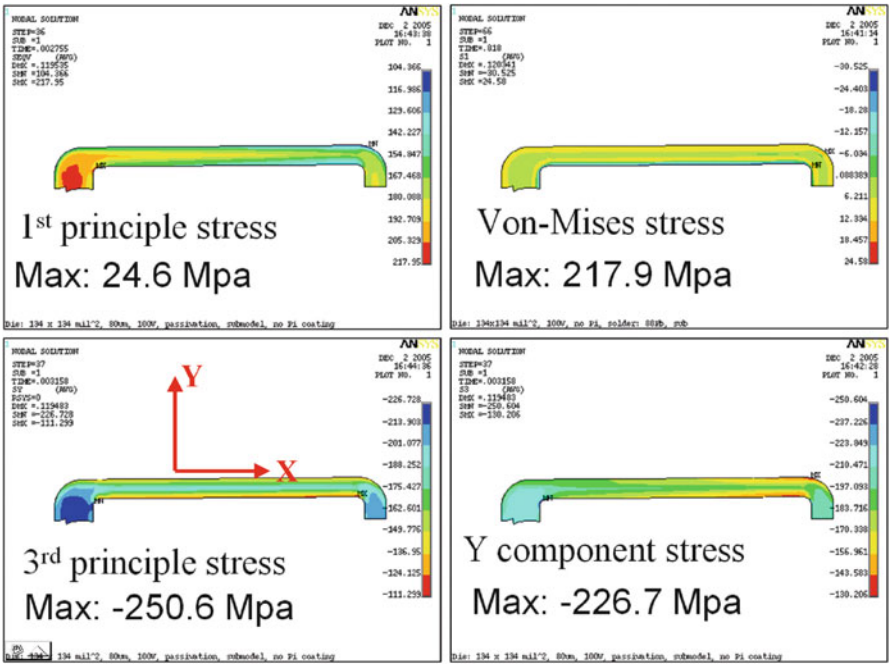


Fig. 7.9 Passivation stress contour (without polyimide coating above the passivation)

Figure 7.9 shows the passivation stress without polyimide coating above passivation. Figure 7.10 shows the passivation stress with 5-μm polyimide coating above passivation. It can be seen that the first and third principal stresses in passivation increase when 5-μm polyimide coating is applied above the passivation layer. However, the von Mises stress in passivation is decreased. But the difference is not significant as we expected.

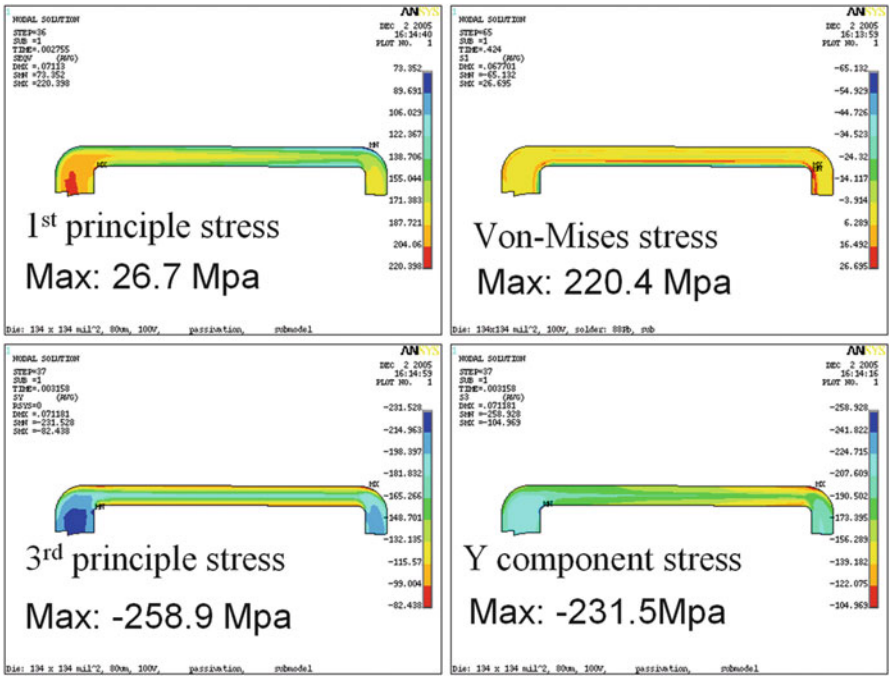


Fig. 7.10 Passivation stress contour (with 5-μm polyimide coating above the passivation)

7.1.4 Simulations Considering Silica Fillers in Mold Compound Material

1. Silica fillers in contact with passivation
   Silica fillers in mold compound which contact with passivation are illustrated in Figs. 7.11 and 7.12. Different sized silica fillers in mold compound are considered. Smaller size silica fillers are embedded in passivation slot. Larger size silica fillers are placed above passivation.

   For the model without polyimide coat, silica fillers are glued to mold compound and contact with passivation directly. For the simulation with 5-μm polyimide coating above passivation, silica fillers penetrate through polyimide coating and contact with passivation.

   The results of polyimide coating impact with consideration of silica fillers in mold compound are shown in Figs. 7.13 and 7.14. The max first principal stress in passivation increases from 64.3 to 216.6 MPa when a 5-μm polyimide coating, which is penetrated by silica fillers in the mold compound, is applied to passivation layer. This indicated that the worst case is when there is a polyimide coat and the

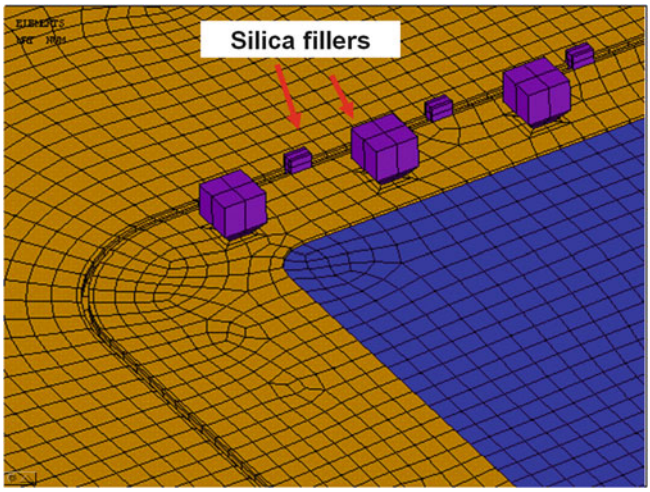


Fig. 7.11 Silica fillers of EMC in contact with passivation

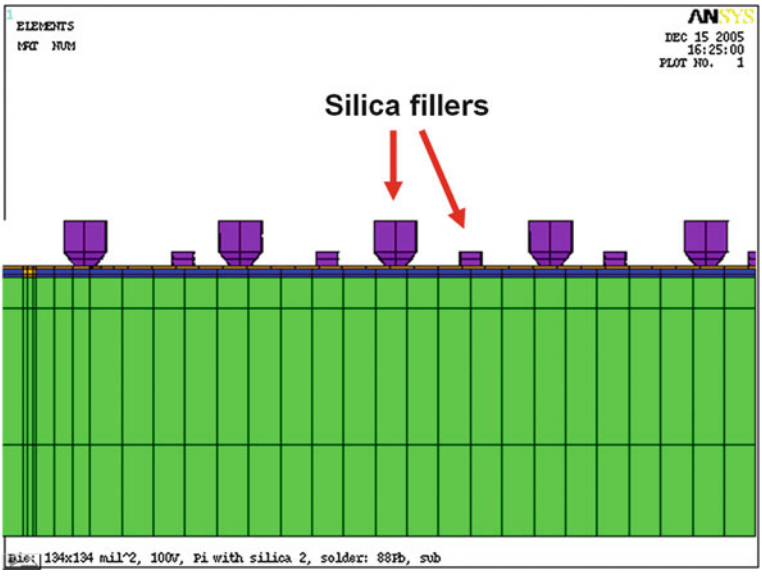


Fig. 7.12 Front view of silica fillers contact with passivation

silica fillers in mold compound have penetrated the polyimide to contact the passivation. This worst case is induced due to both the EMC material and the larger CTE mismatch at the interface between polyimide and passivation. While in the case without polyimide coat, the major stresses of passivation are due to the EMC with silica fillers.

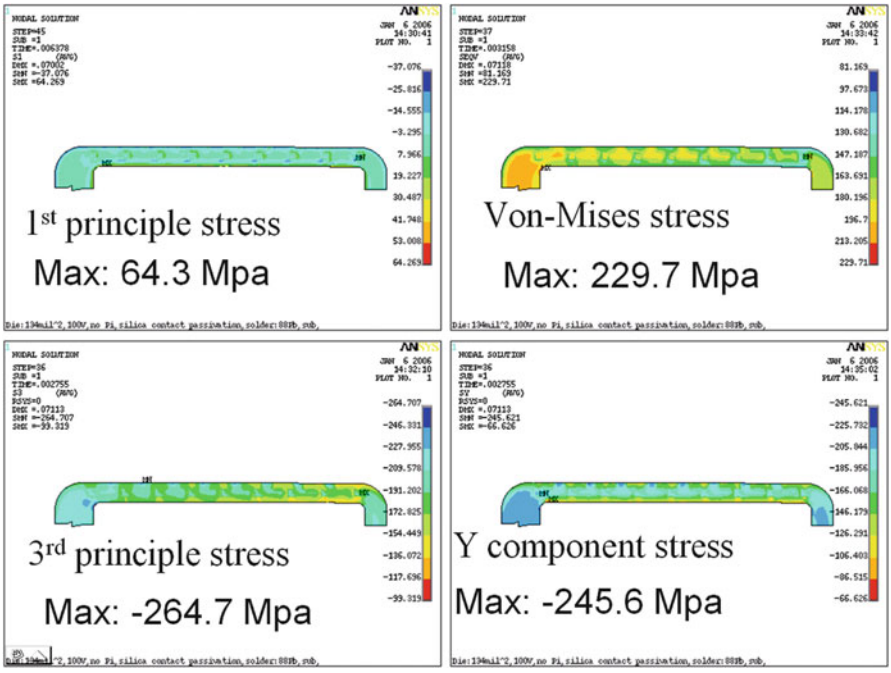


Fig. 7.13 Passivation stresses in model without polyimide

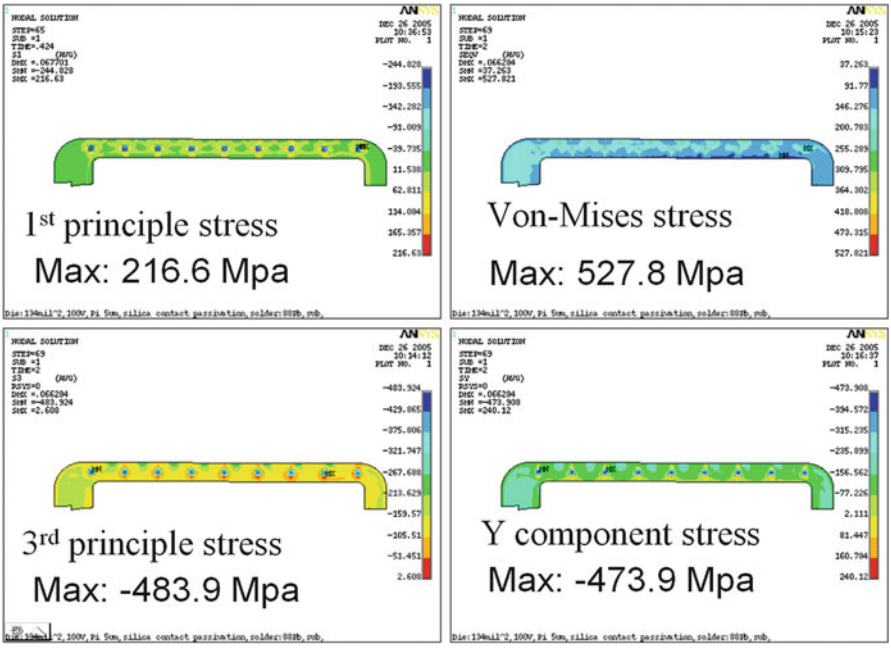


Fig. 7.14 Passivation stresses in model with silica fillers penetrating through 5-μm polyimide coating

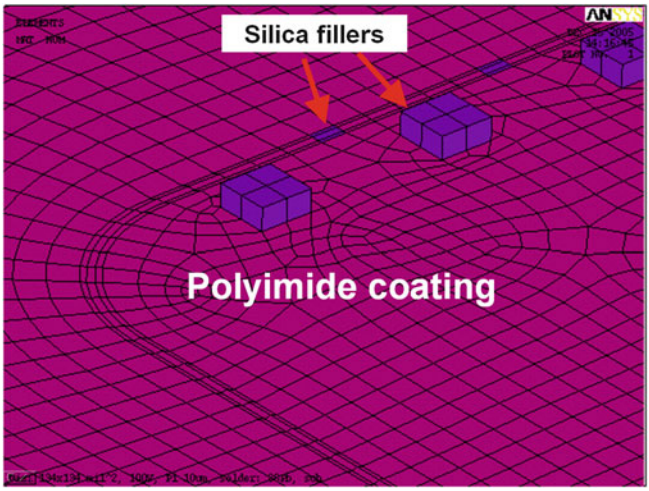


Fig. 7.15 Silica fillers are embedded in polyimide coating

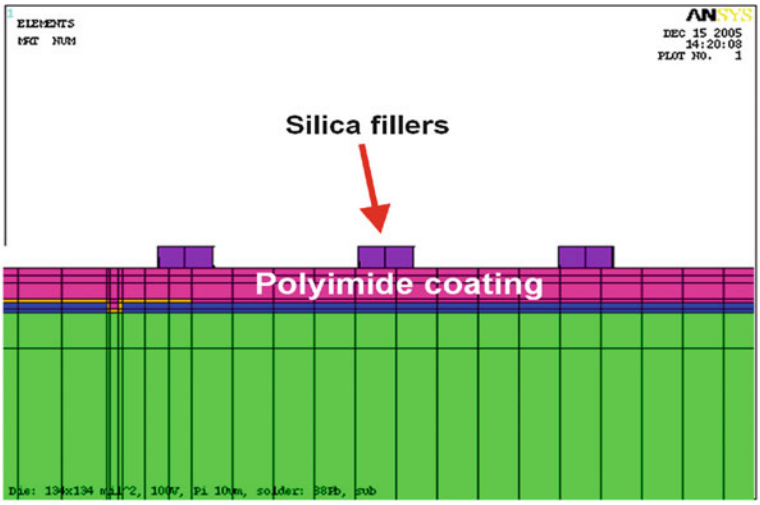


Fig. 7.16 10-μm thick polyimide coating above passivation

By comparing the simulation results in Figs. 7.9–7.14, it can be seen that the passivation stress with consideration of silica fillers in mold compound are much higher than that without consideration of silica fillers.

2. Silica fillers without contact with passivation.
   Figures 7.15–7.17 illustrate the mesh of silica fillers being embedded in thicker polyimide coating. The polyimide coating thickness is 10 μm, and silica fillers are embedded in polyimide coating in 5 μm. So the silica fillers do not contact with the passivation.

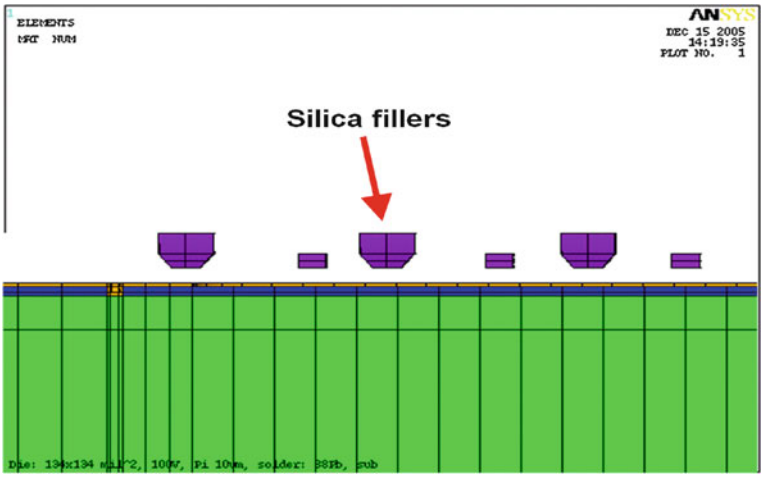


Fig. 7.17 Silica fillers are 5 μm above passivation

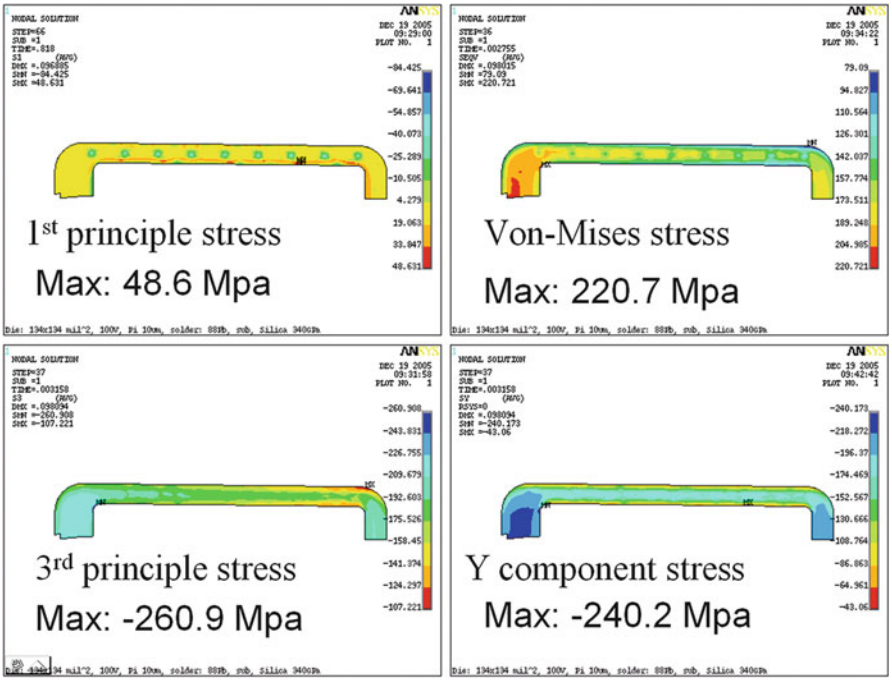


Fig. 7.18 Passivation stress contour (silica fillers not penetrating 10-μm polyimide coating)

The stress contour of passivation is shown in Fig. 7.18, with 10-μm-thick polyimide coating and no silica fillers penetrating through it during power pulse test. The max first principal stress on passivation is 48.6 MPa, which is much

lower than the case (216.6 MPa in Fig. 7.14) with thinner polyimide coating (5 μm) and silica fillers penetrating through it.

From the simulations in this section for the power package with the polyimide coat material and the EMC material with silica fillers, we can get the following three points for the polyimide coat material effect on the damage of die surface:

1. For the model neglecting silica fillers in mold compound, polyimide coating above passivation increases passivation stress a little bit. This may be induced by extra high CTE and low thermal conductivity of polyimide coating.
2. The impact of silica fillers in mold compound is significant. Silica fillers in the mold compound penetrating through thin polyimide coating generate extra high stress on passivation during power pulse test. This may be induced by both high CTE of polyimide coat material and high Young's modulus of silica fillers in EMC material.
3. A relatively thick polyimide coating above passivation can act as a buffer layer when silica fillers do not penetrate through it.

7.2 Die Attach Stress Analysis and Material Selection

7.2.1 Epoxy Die Attach Stress Analysis

Die attach stress analysis is import to determine the potential risk factors that cause die attach material delamination. This section targets the die attach of a perfect 3D package without any initial defects. The analysis includes the moisture soak, thermal hygro, and CTE stress simulation for the possible potential risk locations with max stress and moisture concettration.

The package used in the simulation is a 14-pin SOIC package [3] with a outer dimension of 8.6 × 3.9 mm, a thickness of 1.45 mm, a pad size of 2.54 × 2.03 mm with a thickness 0.2 mm. Initial die size is 0.965 × 0.889 mm with 0.38 mm thickness, initial die attach bond line is 0.0127 mm. The 3D SOIC model is showen in Fig. 7.19.

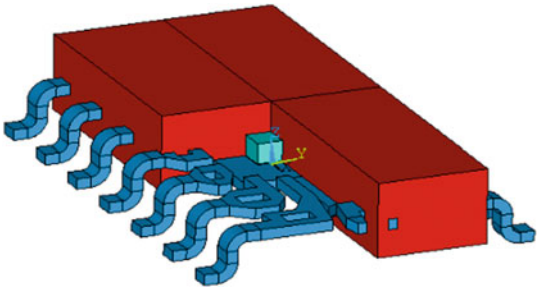


Fig. 7.19 SOIC package model

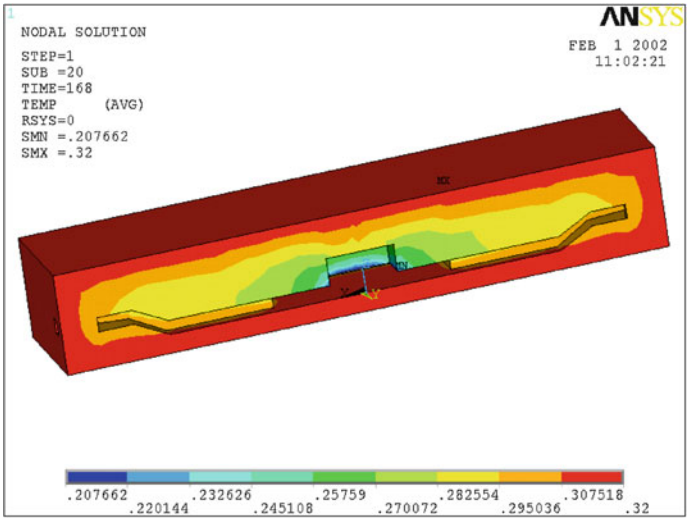


Fig. 7.20 Moisture soak at the end of 168 h

The Young's modulus of mold compound is 14.6 GPa at room temperature, and 0.8 GPa at 240°C, Poisson ratio is taken to be 0.3, CTE is 18 ppm/°C when temperature below T_g and 55 ppm/°C when temperature above T_g. The Young's modulus and Poisson's ratio of die attach is 1.2 and 0.3 GPa, respectively. The CTE number is 37 ppm/°C when temperature below T_g and 40 ppm/°C when temperature above T_g. The Young's modulus of Silicon is 131 GPa, Poisson ratio is 0.3 and the CTE is the 2.8 ppm/°C. For the pad and lead frame, the Young' modulus is 120.7 GPa, CTE is 17.1 ppm/°C, and the Poisson ratio is 0.3. The hygroscopic swelling coefficients are selected to be 2,600 ppm/wt.% for both mold compound and die attach materials.

Moisture soak simulation results are shown in Figs. 7.20 and 7.21, which gives the moisture soak after 168 h with 85°C/60%RH. The outer boundary of mold compound has the highest moisture, and the inner boundary at the internal surfaces of die, pad, and lead frame has the zero moisture flux. Moisture cannot penetrate the die and the pad with lead frames.

Figure 7.20 shows that after 168 h moisture soak, the mold compound is almost fully saturated. The minimum number of moisture concentration near the die and die attach is over 0.2 wt.%. Figure 7.21 shows the die attach moisture soak after 168 h. From this picture, it can be seen that most of the die attach area is not saturated with moisture. This is because that the die attach is a very thin layer trapped between the die and the pad which are both impermeable to moisture. However, at the perimeter of the die attach is saturated with moisture. This shows that if there is a initial crack located at the edge area of the die attach, it is filled with moisture.

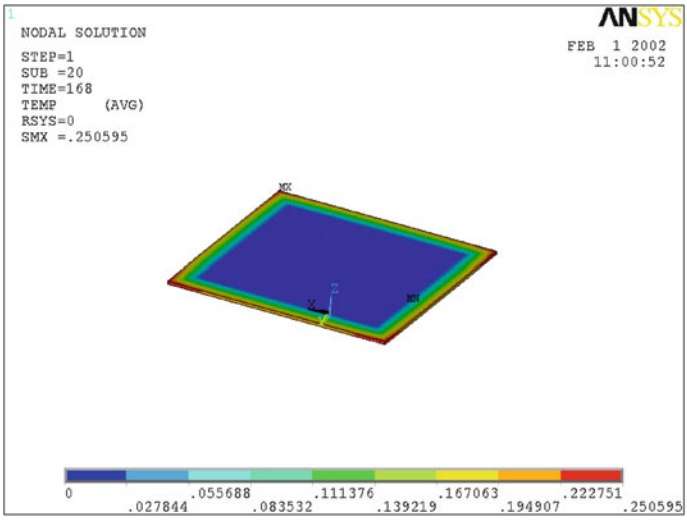


Fig. 7.21 Die attach moisture concentration

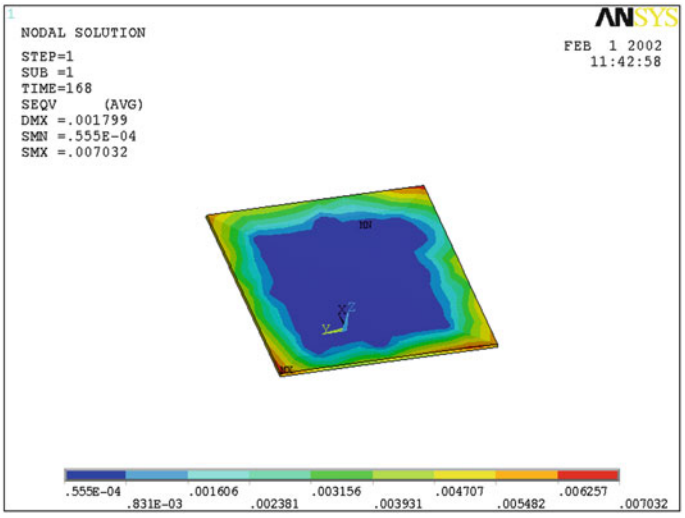


Fig. 7.22 Die attach hygrostress due to moisture only

The die attach hygrostresses due to the moisture are shown in Fig. 7.22. It can be seen that the hygrostress induced in die attach is small. The max stress appeared at the edge corner area.

Figure 7.23 shows that the total von Mises stress of mold compound and the die attach at reflow temperature 260°C. It has shown that the stresses at the interface

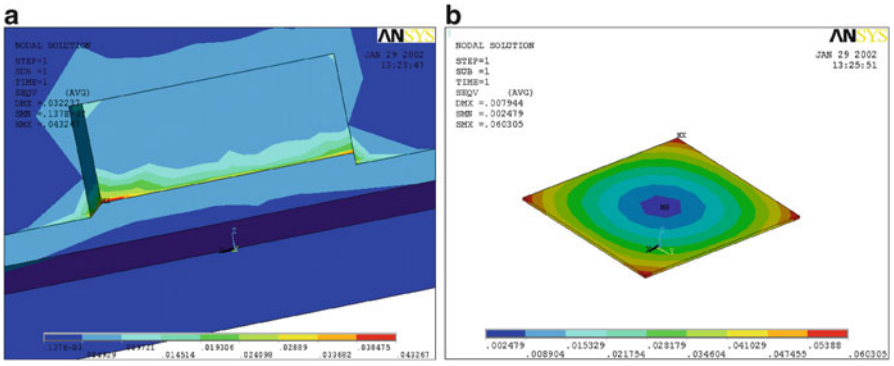


Fig. 7.23 von Mises stresses of EMC and die attach with die attach thickness 0.5 mil (unit: GPa): (**a**) EMC stress (**b**) die attach

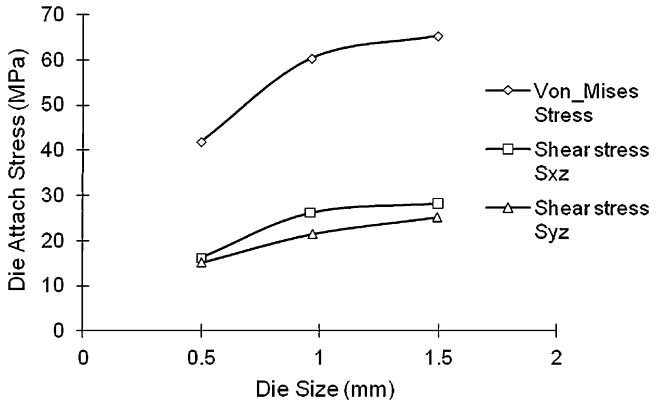


Fig. 7.24 Max die attach stress (MPa) vs. die size

edge among die attach, die, and mold compound are highest, the related position is likely to be an initiation point for die attach delamination.

Figures 7.24–7.26 have shown the von Mises stress and shear stress of die attach vs. with die attach thickness, die size and die thickness. It is found that increasing the die attach thickness can effectively decrease the stress. Reducing the die and pad sizes can effectively reduce the die attach stresses while increasing the die attach thickness can have a significant impact in reducing the die attach stresses.

Since the die attach material is important for the delamination, it should be careful to select the die attach materials. Table 7.2 shows the max stresses at the interface between die, die attach and EMC materials at reflow temperature. A group

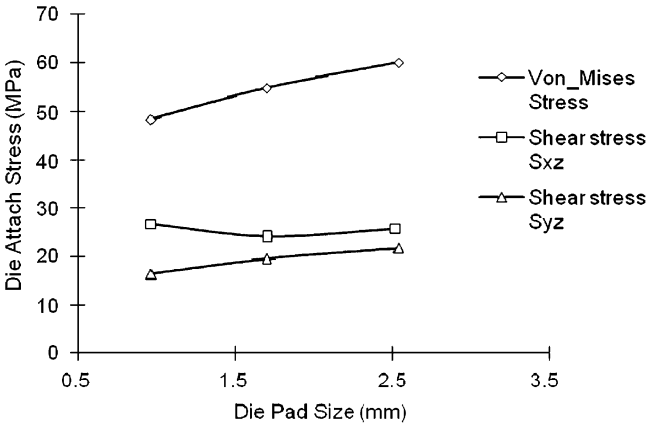


Fig. 7.25 Max die attach stress (MPa) vs. pad size

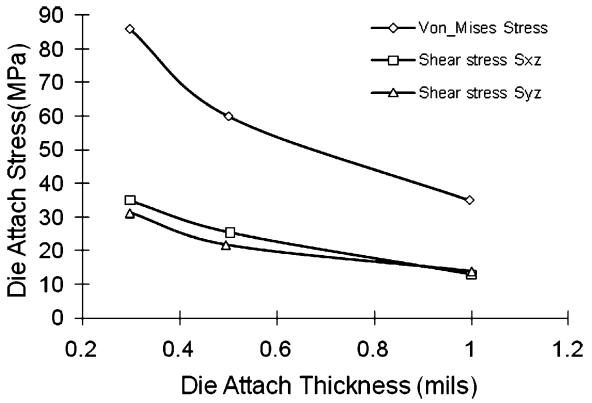


Fig. 7.26 Max die attach stress (MPa) vs. die attach thickness

of die attach materials have been considered while all the rest materials in SOIC14 are kept the same. From Table 7.2, it tells us that the stress behavior of die attach material DA4 at reflow temperature is the best, it induces the lowest stress in itself, EMC and die. Therefore, it would be a ideal option for selection. However, the die attach material selection also depends on the adhesion strength behavior at different temperatures, as well as the material cost. If a die attach material induces the higher stresses which are lower than its adhesive strength, but its material cost is lower than DA4, then this die attach material would be a good choice from cost-effective viewpoint.

Table 7.2 Die attach material comparison

Die attach material	DA1	DA2	DA3	DA4	DA5	DA6
Base material	Epoxy	Cynate ester	Polyimide	Acrylic resin	Acrylic resin	Epoxy
CTE alpha 1	40	37	31	12.7	6.1	77
CTE alpha 2	150	40	140	15.8	9.2	168
T_g (°C)	120	170	130	19	23	1
Young modulus (GPa)	3.94	3	3.0	0.35	4.1	1.8
Stress results (MPa)						
Die attach thickness 0.3 mil						
von Mises stress	205.8	166.02	182.0	33.2	203.7	130.85
Syz	70.86	59.8	61.8	12.7	76.2	44.64
Szx	74.73	62.3	67.1	13.67	78.6	49.64
EMC von Mises stress	59.05	51.4	55.3	77.85	45.53	64.19
Die von Mises stress	191.14	149.62	178.25	153.7	147.2	178.53
Die attach thickness 0.5 mil						
von Mises stress	176.21	121.08	148.1	22.78	152.4	105.23
Syz	62.18	41.8	51.6	8.01	57	36.48
Szx	79.42	47.5	65.13	9.28	63.3	45.92
EMC von Mises stress	45.46	35.76	40.23	50	32.7	47.12
Die von Mises stress	168.34	115.2	150.6	120.3	118.3	157.1
Die attach thickness 1.0 mil						
von Mises stress	140.88	75.67	112.6	11.89	100.64	77.56
Syz	49.1	26.35	37.3	4.15	39.4	25.36
Szx	56.79	28.98	44.3	4.73	42.3	30.33
EMC von Mises stress	31.61	20.81	26.5	25.94	19.58	30.42
Die von Mises stress	129.5	95.43	108.74	90.4	99.34	115.71

7.3 Epoxy Mold Compound Characterization

JEDEC identifies in J-STD-020C that all devices should be baked for 24 h minimum at 125 + 5/−0°C to remove moisture from the package so that it will be "dry" [4]. This bake is required prior to other reliability stresses [5], again to "dry" the plastic encapsulated devices. When this preparation technique was first established, most of the EMCs used comprised OCN/ECN Novolac resins with glass transition temperatures (T_g) significantly greater than this 125°C bake. The mold compounds that are used today have a variety of chemistries and often have T_g regions near or below the 125°C bake temperature. This change in mold compound chemistry has resulted in two unpredicted responses to the 125°C bake. Some mold compounds undergo additional cross-linking during this conditioning (drying) bake and will result in a more fully cured matrix. Additional mold compounds that have their T_g regions at or near this 125°C bake temperature will undergo a change in their inherent equilibrium state, known as physical aging. This results in a polymer network with a reduced free volume space between polymer chains that would

ultimately result in performance behavioral changes when the material is exposed to the moisture soak conditioning, and reflow preconditioning required prior to reliability testing.

7.3.1 Behavior of Epoxy Mold Compound Material

Several failure mechanisms within plastic encapsulated microcircuits (PEMs) associated to moisture ingress and ionic diffusion through the mold compound had been identified and characterized [6]. In order to characterize the reliability of the PEM, JEDEC (the semiconductor engineering standardization body of the Electronic Industries Alliance) identifies several reliability stress tests that are designed to bring out failure mechanisms associated to moisture exposure. As a "drying" step prior to accelerated environmental exposure, several of the JEDEC specifications [4, 5, 7] require a 24 h minimum bake at 125 + 5/−0°C to remove the resident moisture from the package. After this bake, the devices under test (DUT) are exposed to various elevated temperature and relative humidity environments. Failure mechanisms such as delamination, package cracking, corrosion, and intermetallic degradation (between the bond wire and the die pad) are routinely associated with the effects of moisture ingress and ionic mobility/diffusion through the molding compound.

The epoxy molding compounds utilized in the semiconductor industry today tend to be aromatic based Novolacs, Epoxies, or of other aromatic backbone structures. These EMCs are usually highly filled (75–90% by weight) with fused silica. Generally, the higher the filler loading, the lower the moisture weight gain. The backbone polymers tend to be hydrophilic in nature and based on the chemistry and filler loading can absorb up to approximately 0.55% by weight moisture when exposed to an 85°C/85%RH environment for 168 h. One of the fundamental results of this moisture absorbance is a corresponding drop in the observed glass transition temperature (T_g) due to the plasticization effect of moisture on the polymer network. In order to obtain these higher filler loadings (greater than approximately 80% by weight) non-Novolac resin chemistries are used. These novel chemistries typically have T_g region onset temperatures below 145°C (as measured by differential scanning calorimetry, DSC).

A study was performed to characterize the effect of moisture exposure on the T_g onset temperature for eight different mold compounds. The mold compound samples were initially dried in a vacuum desiccator for greater than 48 h, and then the baseline T_g onset was measured (by DSC). To follow the JEDEC standard for preconditioning (JESD22-A113D [5]), a second set of samples were baked for 24 h at 125°C, and then exposed to 85°C/85%RH for 168 h. The T_g onset temperature of the desiccated dry samples were compared to the baked/moisture soaked samples. For two of the mold compounds, the postbaked/moisture soaked samples had a higher T_g onset than the original desiccated sample. An additional experiment was performed whereby a third set of samples were baked for 24 h at 125°C and their corresponding T_g onset temperatures were measured (by DSC). Four of

Table 7.3 DSC T_g onset temperature for eight epoxy mold compounds

Mold compound designation	Desiccated T_g onset	24 h 125°C T_g onset	Bake then (85°C/ 85%RH) T_g onset	Note
A	97.68	108.61	103.4	
B	154.92	149.92/169.65	121.03/150.33	Dual step transition
C	128.82	142.88	132.18	Enthalpic recovery
D	119.16	120.25	112.43	
E	116.09	120.34	114.31	
F	131.61	143.33	129.9	Enthalpic recovery
G	103.61	105.61	101.16	
H	100.78	99.8	99.3	

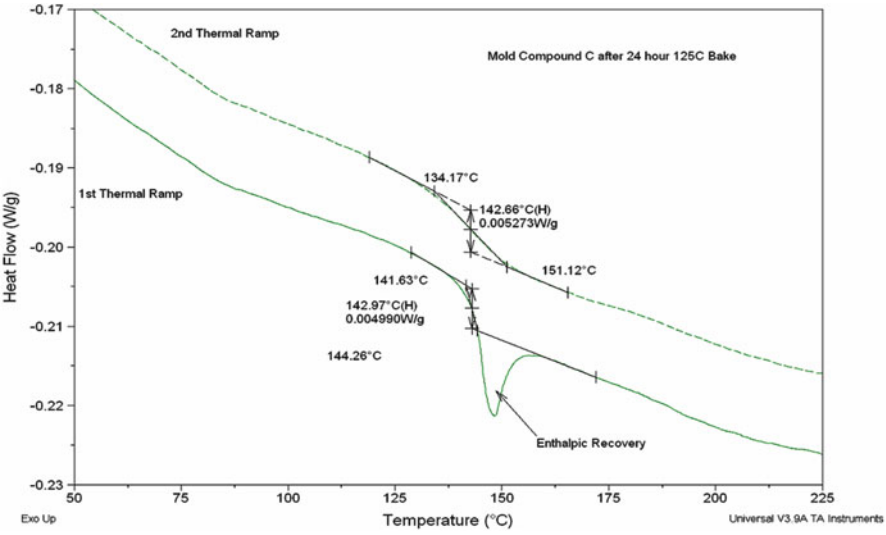


Fig. 7.27 DSC thermal scan of mold compound "C" exhibiting enthalpic recovery after 24 h 125°C bake on first thermal ramp and no peak on second thermal scan

the original eight mold compounds had a higher T_g onset temperature after the 24 h/125°C bake (Table 7.3), and two of these four exhibited an endotherm (enthalpic recovery) in the T_g region (Fig. 7.27). Enthalpic recovery detected by DSC is associated to a phenomenon known as physical aging (Fig. 7.28) [8]. The annealing peak noted in the aged polymer (after 24 h 125°C bake) is associated to the polymer being closer to its equilibrium state resulting in a long relaxation time. Upon heating this material above its T_g region, cooling and reheating the same sample, the annealing peak is eliminated and the apparent T_g onset reduces to that of the nonequilibrium state polymer. Associated to this phenomenon of physical aging (attainment of greater equilibrium) is a reduction in free volume space within the polymer network. This changZe in free volume space corresponds to a reduction in

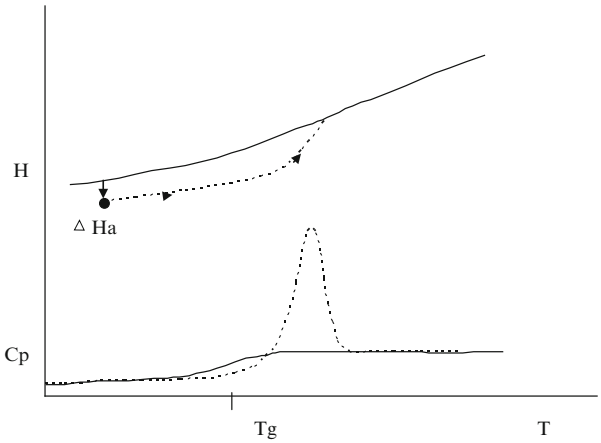


Fig. 7.28 Schematic of enthalpy and heat capacity as a function of temperature. The *solid line* is the ideal (nonaged) behavior and the *dashed line* is of an aged polymer exhibiting an annealing peak (note: the apparent heat capacity is the derivative of the enthalpy curve) [7]

coefficient of thermal expansion below the T_g. Vrentas et al. have shown that the diffusion coefficient of a physically aged polymer is significantly less than that for a nonaged polymer [9, 10]. This section describes the experimentation performed to verify that the behavior demonstrated by some mold compounds after baking for 24 h at 125°C is consistent with literature described behaviors of physically aged polymer systems. Additionally, FEA analysis is used to model the diffusion behavior of aged vs. non aged mold compounds in a 14-leaded SOIC PEM configuration.

7.3.2 Experimentation of Epoxy Mold Compound

Three EMCs (Sumitomo EME-7351LS, ShinEtsu KMC-288P3, and Cheil Industries SL7300HC) were characterized to evaluate their properties associated to the physical aging phenomena. Standard sized sample devices were transfer molded in a production environment such that the resulting units contained only mold compound (no lead frame, die, die attach adhesive, or bonding wires). All samples were post mold cured using vendor recommended conditions (generally 5 h at 175°C) in production curing ovens. One subset of these samples was baked for 24 h at 125°C and the other subset was placed in vacuum desiccation for >12 days. Samples were analyzed to determine the relevant input parameters listed in Table 7.4. The hygrothermal expansion methodology utilized was based on a technique described by Wong utilizing TMA and TGA to measure the dimensional change as a function of weight loss [11]. 170°C was selected as the isothermal condition for the coefficient of moisture expansion (CME) studies because it is significantly above the T_g

Table 7.4 The relevant input parameters characterized during this study

Input parameter	Test technique	Units
DSC T_g onset temp—dry (run1/run2)	DSC	°C
TMA T_g—dry (run1/run2)	TMA	°C
Alpha 1 CTE < T_g (ppm)—dry (run1/run2)	TMA	ppm
Alpha 2 CTE > T_g (ppm)—dry (run1/run2)	TMA	ppm
DSC T_g onset temp—wet (run1/run2)	DSC	°C
TMA T_g—wet (85°C/85%RH)—(run1/run2)	TMA	°C
Alpha 1 CTE < T_g (ppm)—wet (run1/run2)	TMA	ppm
Alpha 2 CTE > T_g (ppm)—wet (run1/run2)	TMA	ppm
Average % moist. wt. gain: order: 30°C/85%RH, 60°C/85%RH, 85°C/85%RH	JESD22-A120	%
Device	22-A120	cm^3
D(T) order: 30°C/85%RH, 60°C/85%RH, 85°C/85%RH	22-A120	mm^2/s
Ea	22-A120	eV
Csar(T, %RH) order: 30°C/85%RH, 60°C/85%RH, 85°C/85%RH	22-A120	mg/cm^3
CME (hygroscopic coefficient (TMA-RGA method))	TMA/TGA	mm^3/mg
Hygroscopic strain (CME*moist)	TMA/TGA	
TGA calculated filler content	TGA	%

for all three mold compounds (CME changes relative to the T_g). DSC T_g characterization was performed on a TA Instruments Q1000, with two thermal ramps per sample using a ramp method of 0–250°C at 10°C/min. TMA T_g and CTE characterization was performed on a TA Instruments Q400, with two thermal ramps per sample using an expansion probe with a force of 0.18 N and a ramp method of 10–250°C at 5°C/min. TGA weight loss analysis was performed on a TA Instruments Q50. All moisture gain studies were performed according to JESD22-A120 utilizing an ESPEC SH-241 moisture chamber. The three conditioning environments utilized in these studies were 85°C/85%RH, 60°C/85%RH, and 30°C/85%RH.

7.3.3 Test Result, Modeling, and Discussion

The KMC-288P3 and SL7300HC mold compounds exhibited physical aging enthalpic recovery after the 125°C 24 h bake as detected by DSC (Figs. 7.29 and 7.30). Both of these mold compounds also exhibited a statistically lower Alpha 1 (CTE below T_g) during the first run TMA thermal ramp compared to the corresponding vacuum desiccated data. This response is consistent with the reduction in free volume associated to physical aging. The EME-7351LS did not show evidence of physical aging after the drying bake (Fig. 7.31), and there was no statistical difference in the Alpha 1 of the first run for the baked to desiccated comparison. Tables 7.5–7.7 lists the test results for the input parameters listed in Table 7.4 for

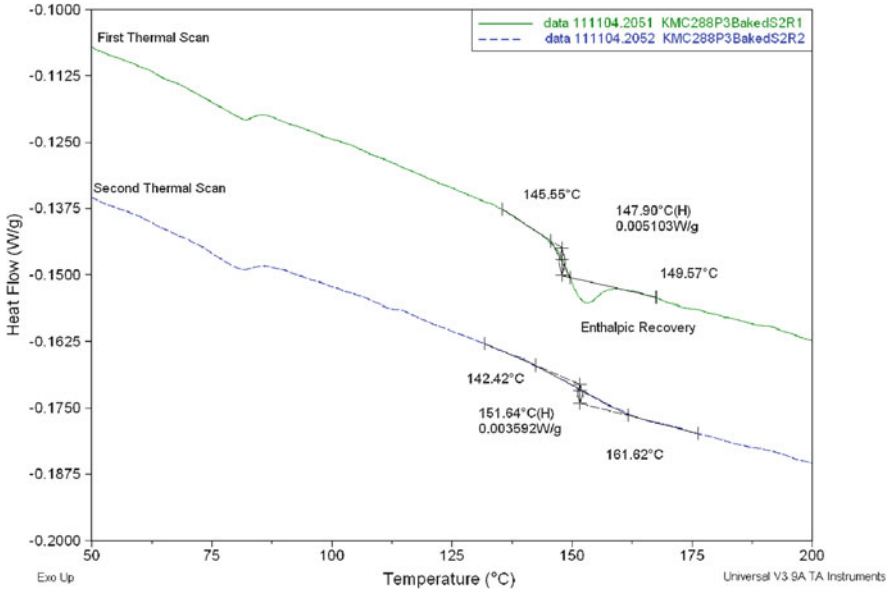


Fig. 7.29 DSC overlay of run1 vs. run2 thermal ramps after 24 h 125°C Bake—KMC-288P3 (enthalpic recovery)

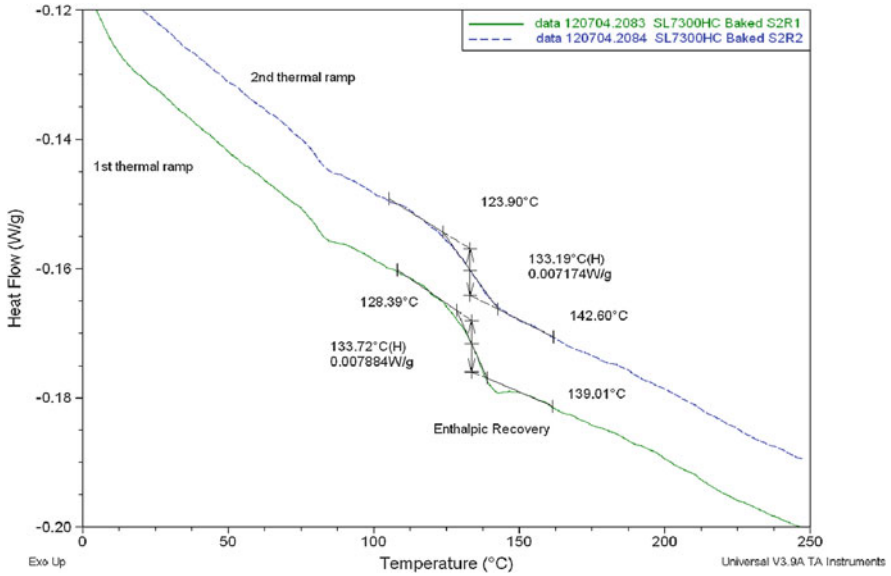


Fig. 7.30 DSC overlay of run1 vs. run2 thermal ramps after 24 h 125°C Bake—SL7300HC (enthalpic recovery)

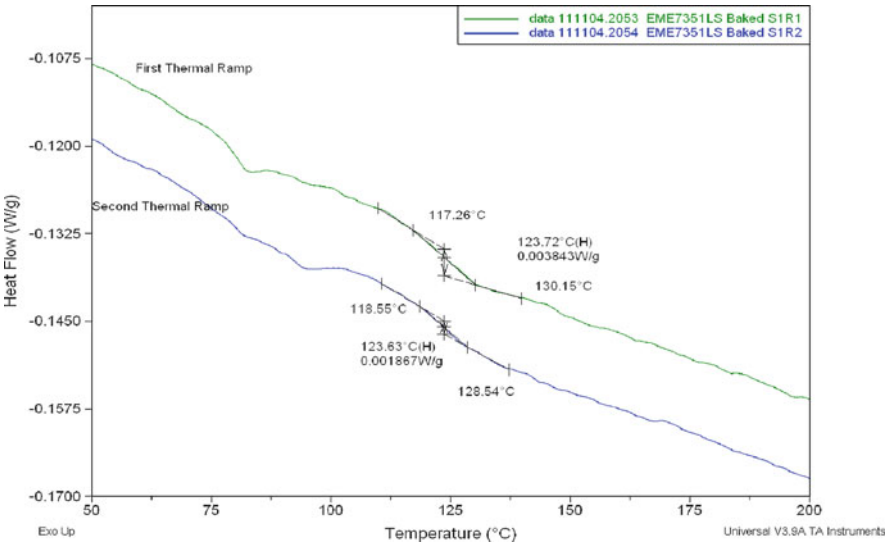


Fig. 7.31 DSC overlay of run1 vs. run2 thermal ramps after 24 h 125°C Bake—EME 7351LS (no enthalpic recovery)

Table 7.5 KMC-288P3 input data

Input parameter	Units	Baked 24 h at 125°C	Desiccated >12 days
Enthalpic recovery in run1		Yes	No
DSC T_g onset temp—dry (run1/run2)	°C	146.2/141.4	133.2/137.7
TMA T_g—dry (run1/run2)	°C	140.7/135.0	127.4/136.3
Alpha 1 CTE < T_g (ppm)—dry (run1/run2)	ppm	9.4/10.71	11.92/11.39
Alpha 2 CTE > T_g (ppm)—dry (run1/run2)	ppm	42.09/44.14	37.08/43.43
DSC T_g onset temp—wet (run1/run2)	°C		115.5/143.1
TMA T_g—wet (85°C/85%RH)—(run1/run2)	°C		108.3/146.16
Alpha 1 CTE < T_g (ppm)—wet (run1/run2)	ppm		7.5/8.2
Alpha 2 CTE > T_g (ppm)—wet (run1/run2)	ppm		19.5/29.8
Average % moist. wt. gain: order: 30°C/85%RH, 60°C/85%RH, 85°C/85%RH	%	0.15/0.27/0.36	0.17/0.27/0.36
Device	cm^3	0.076	0.076
D(T) order: 30°C/85%RH, 60°C/85%RH, 85°C/85%RH	mm^2/s	1.3E − 7, 3.93E − 7, 7.79E − 7 (curve fit)	1.35E − 7, 5.51E − 7, 8.54E − 7 (curve fit)
Ea	eV	0.3037 (curve fit)	0.3177 (curve fit)
Csar(T, %RH) order: 30°C/85%RH, 60°C/85%RH, 85°C/85%RH	mg/cm^3	4.81/4.64/7.73	4.98/5.09/7.82
CME (hygroscopic coefficient (TMA-RGA method))	mm^3/mg	0.443	0.5133
Hygroscopic strain (CME*moist)		0.001874	0.002431
TGA calculated filler content	%	83	83

Table 7.6 SL7300HC input data

Input parameter	Units	Baked 24 h at 125°C	Desiccated >12 days
Enthalpic recovery in run1		Yes	No
DSC T_g onset temp—dry (run1/run2)	°C	129.4/125.3	125.2/126.2
TMA T_g—dry (run1/run2)	°C	125.57/124.98	124.17/125.02
Alpha 1 CTE < T_g (ppm)—dry (run1/run2)	ppm	9.03/10.38	11.15/10.69
Alpha 2 CTE > T_g (ppm)—dry (run1/run2)	ppm	39.33/42.18	38.64/44.91
DSC T_g onset temp—wet (run1/run2)	°C		116.4/122.5
TMA T_g—wet (85°C/85%RH)—(run1/run2)	°C		112.36/123.35
Alpha 1 CTE < T_g (ppm)—wet (run1/run2)	ppm		8.66/10.95
Alpha 2 CTE > T_g (ppm)—wet (run1/run2)	ppm		30.49/44.75
Average % moist. wt. gain: order: 30°C/85%RH, 60°C/85%RH, 85°C/85%RH	%	0.18/0.20/0.23	
Device	cm^3	0.065913	
D(T) order: 30°C/85%RH, 60°C/85%RH, 85°C/85%RH	mm^2/s	3.84E − 7, 5.7E − 7, 9.97E − 7 (curve fit)	
Ea	eV	0.1578	
Csar(T, %RH) order: 30°C/85%RH, 60°C/85%RH, 85°C/85%RH	mg/cm^3	3.29/3.3/4.26	
CME (hygroscopic coefficient (TMA-RGA method))	mm^3/mg	0.5018	
Hygroscopic strain (CME*moist)		0.001301	
TGA calculated filler content	%	84	84

each mold compound. CME and Hygrostrain values were greater for the desiccated samples vs. the baked samples for both KMC-288P3 and EME-7351LS. However, the difference appears much greater with the KMC-288P3 (which shows enthalpic recovery). An issue associated to accurately identifying the time to 50% moisture weight gain ($t_{0.5}$) was noted for the 85 and 60°C conditions during the performance of JESD22-A120. This is a key factor in calculating the diffusion coefficient and activation energy. Due to the small device sample size (48ld or 56ld TSSOP) it was observed that the $t_{0.5}$ occurred prior to the first data point (24 h) and therefore a sixth order curve fit was applied to the data. This would indicate that the actual diffusion coefficients for these two conditions were probably higher than reported. One documented method for measuring sorption in an environmental chamber is a McBain-Baker apparatus [12]. Alternately, the sample dimensions can be manipulated to slow the diffusion rate. An alternative method for improving the accuracy of this measurement will be studied in future experiments.

The FEA software ANSYS was used to model the diffusion at both the center location die surface to mold compound (KMC288) interface, and at the bottom center lead frame to mold compound interface (Fig. 7.32). The moisture diffusion curves (C/C_{sat} vs. time) of baked vs. desiccated at both locations indicated the difference at the die surface to mold compound interface due to the greater depth of

Table 7.7 EME7351 LS input data

Input parameter	Units	Baked 24 h at 125°C	Desiccated >12 days
Enthalpic recovery in run1		Yes	No
DSC T_g onset temp—dry (run1/run2)	°C	116.5/117.8	114.5/116.6
TMA T_g—dry (run1/run2)	°C	115.58/112.63	112.6/114.66
Alpha 1 CTE < T_g (ppm)—dry (run1/run2)	ppm	9.52/10.02	10.19/9.54
Alpha 2 CTE > T_g (ppm)—dry (run1/run2)	ppm	41.65/42.50	43.08/43.43
DSC T_g onset temp—wet (run1/run2)	°C		110.4/114.04
TMA T_g—wet (85°C/85%RH)—(run1/run2)	°C		107.4/119.5
Alpha 1 CTE < T_g (ppm)—wet (run1/run2)	ppm		9.36/10.1
Alpha 2 CTE > T_g (ppm)—wet (run1/run2)	ppm		13.9/27.34
Average % moist. wt. gain: order: 30°C/85%RH, 60°C/85%RH, 85°C/85%RH	%	0.08/0.19/0.22	0.09/0.19/0.21
Device	cm^3	0.076	0.076
D(T) order: 30°C/85%RH, 60°C/85%RH, 85°C/85%RH	mm^2/s	1.79E − 7, 6.27E − 7, 1.04E − 6 (curve fit)	1.85E − 7, 7.0E − 7, 1.2E − 6 (curve fit)
Ea	eV	0.3018 (curve fit)	0.3174 (curve fit)
Csar(T, %RH) order: 30°C/85%RH, 60°C/85%RH, 85°C/85%RH	mg/cm^3	3.07/3.53/3.93	3.05/3.40/3.27
CME (hygroscopic coefficient (TMA-RGA method))	mm^3/mg	0.496	0.55
Hygroscopic strain (CME*moist)		0.001641	0.001759
TGA calculated filler content	%	86	86

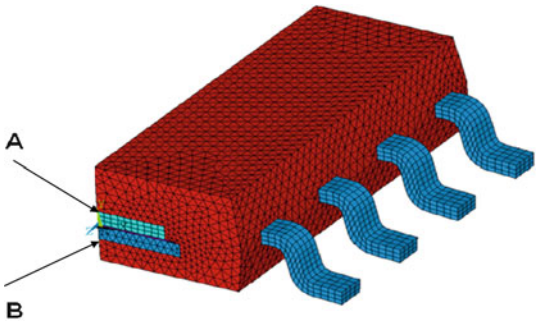


Fig. 7.32 The finite element model of SOIC8 package with EMC: KMC288

mold compound at this interface (Figs. 7.33 and 7.34). This translates to a moisture gradient over time representation depicted in Figs. 7.35 and 7.36. This generated model indicates that there would be less moisture at the die mold compound interface for the baked samples and conversely a greater concentration for the desiccated samples.

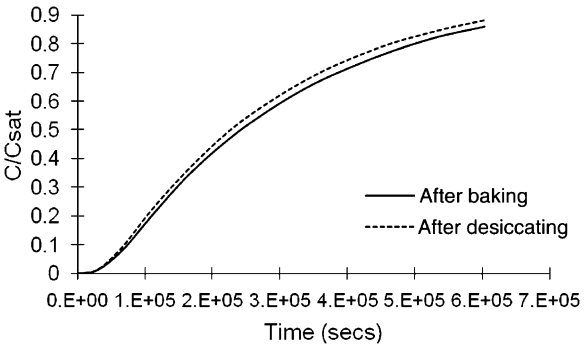


Fig. 7.33 Moisture diffusion comparison at point A (center point of interface between die surface and EMC)

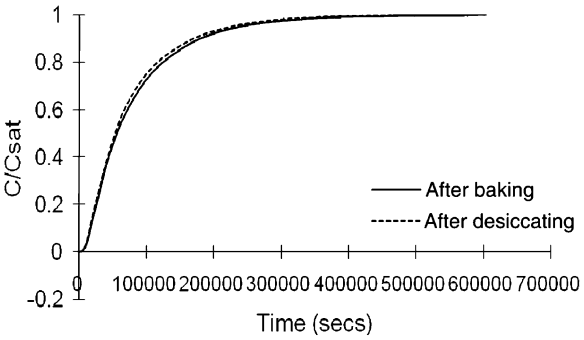


Fig. 7.34 Moisture diffusion comparison at point B (center point of interface between pad bottom surface and EMC)

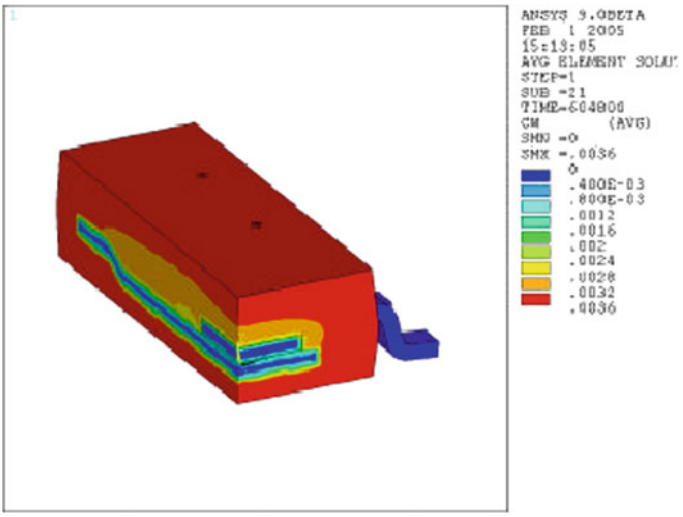


Fig. 7.35 Moisture diffusion gradient after 24 h 125°C bake and 168 h exposure to 85°C/85%RH

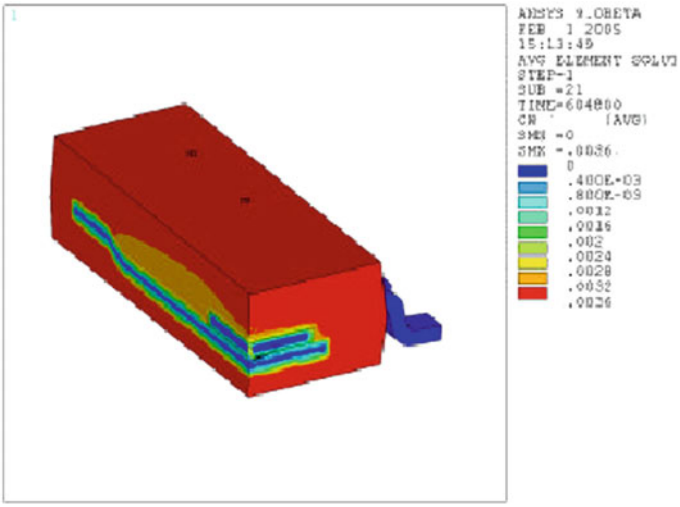


Fig. 7.36 Moisture diffusion gradient after >12 days vacuum desiccation and 168 h at 85°C/85%RH

Diffusion in glassy and rubbery polymers (below and above T_g) is dependent on the environmental temperature, the T_g of the polymer, the CTE, interstitial free volume space in the polymer, as well as the volume of the penetrant. Vrentas et al. put forth the following two equations representing these properties and their effect on Diffusion for glassy polymers [9, 10].

$$D = D_1 = \bar{D}_0 \exp\left[-\frac{E^*}{RT}\right] \exp\left[-\frac{\xi \hat{V}_2^*}{\hat{V}_{FH}/\gamma}\right] \tag{7.1}$$

$$\frac{\hat{V}_{FH}}{\gamma} = \frac{\hat{V}_2^0(T_{g2})}{\gamma_2}\left[f_{H2}^G + (\alpha_{2g} - \alpha_{c2g})(T - T_{g2})\right] \tag{7.2}$$

These diffusion equations ((7.1) and (7.2)) represent the penetrant diffusing both in and out of the polymer system (controlled by the concentration gradient associated to moisture). Therefore, if a polymer has experienced physical aging as a function of the JEDEC required "drying" bake, then the CTE correlating to the reduction in interstitial free volume will be reduced. This change in diffusion would impact both the rate of moisture absorbing into the polymer during the moisture soak as well as the rate of moisture desorption during reflow. For the reliability Failure Mechanics models, the implications of this change could affect the corrosion associated to moisture and ionic contamination ingress, as well as delamination during reflow. The ANSYS modeling of the moisture absorption of baked vs. vacuum desiccated samples indicates a significantly larger concentration of moisture at the die/mold compound interface with the desiccated samples; however, it is also reasonable

to expect that during the rapid reflow process, the moisture gradient would be such that the baked samples would have a higher concentration of moisture at this interface when compared to the desiccated samples. The integrated stress modeling put forth by Tong Yan Tee [13] to calculate the package stress induced during reflow identifies the Vapor Pressure model, Hygromechanical stress model, and the thermomechanical stress model as the three key factors that make up the reflow stress. The data presented would indicate that physical aging impacts the properties of the mold compound relating to all three of these stress models. Based on experimental error with identifying the $t_{0.5}$ value required for calculating the Diffusion coefficient [7], it was not possible to obtain the accuracy required for detecting the $t_{0.5}$ to allow for proper modeling of the desorption of moisture at reflow temperatures (230–260°C). This will be an area of concentration for future development. The data put forth in this section, clearly indicates that a number of commercially available mold compounds will be morphologically affected by the required 24 h 125°C bake required by certain JEDEC specifications and test methods. A goal of the JEDEC specifications is to provide a standard characterization method to allow for the consistent comparison of products. By changing the diffusion rate of moisture and potentially the cross-link density of some mold compounds, these devices may no longer be comparative. It is the recommendation of this study that all JEDEC specifications that require a drying step be modified to include a statement that requires characterization of the mold compound prior to baking the fully assembled devices. Based on the results of this characterization, if the baking condition changes the degree of cure or induces physical aging (change of equilibrium state) of the mold compound, then that material should be subjected to a different drying procedure. An alternative drying procedure used for this study was 12 days in vacuum desiccation. It has been determined that this duration of conditioning results in a comparatively dry sample.

7.4 Mechanical and Thermal Behavior of Ceramic/DBC Substrate

The role of the substrate in power electronics is to provide the interconnections to form an electric circuit (like a printed circuit board), and to cool the components. Compared to materials and techniques used in lower power microelectronics, these substrates must carry higher currents and provide a higher voltage isolation (up to several thousand volts). They also must operate over a wide temperature range (up to 150 or 200°C). Ceramic and direct bonded copper (DBC) are two commonly used substrates in power modules.

Ceramic is a brittle material in the temperature range of the assembly process, so its failure mechanism is mainly fracture. Ceramic cracks can be caused either by thermomechanical or by purely mechanical loads. In this section, the mechanical behavior of the ceramic substrate is investigated first in the assembly molding

process. The effects of both lead frame downset and support pin overpress are studied through the commercial finite element code ANSYS. Then, the thermal effect of both ceramic and DBC substrates is studied and discussed for understanding the behavior of DBC materials.

7.4.1 Ceramic Substrate in a Power Package

The power package examined here is a lead frame based system in package (SiP) power module which is built using multiple dies. It provides complete adjustable-speed motor drive control and fully integrated circuit protection for AC motors found in appliance applications such as washing machines and air conditioners. In the package [14], a ceramic substrate is attached to the lead frame pad through a silicone elastomer attach material. The ceramic substrate serves as a heat sink, as well as an electrical insulator due to its superior mechanical and electrical characteristics, such as relatively high thermal conductivity, excellent electrical insulation, good heat spreading, good corrosion resistant and hermetic properties. In addition, the thermal expansion coefficient of ceramic substrate is close to that of silicon, so no interface layers are required.

Ceramic is a brittle material in the temperature range of the assembly process. Its compressive strength is almost ten times higher than its tensile strength. If the assembly stress exceeds its failure criterion, the ceramic structure cracks. Ceramic cracks can be caused either by purely mechanical stress or by thermomechanical stress. A sudden and large change in package temperature may cause tremendous thermomechanical stresses at the ceramic-to-lead frame interfaces of the package, due to mismatch of the coefficient of thermal expansion between ceramic and lead frame. Impact loading is another common source of ceramic substrate cracks in packages. Poor equipment setup or debris under the package during back-end mechanical operations such as lead trimming may possibly cause ceramic cracks as well.

During SiP assembly process development, cracks in the ceramic substrate were found after the completion of the assembly molding process. Therefore, simulations of the SiP reliability, during assembly molding process, were conducted to find out the root cause of ceramic substrate cracks, and further to determine effective actions to avoid them. Simulation was shown to be an effective way to improve the robustness of the process.

7.4.1.1 Ceramic Substrate Layout in an Assembly Process

The schematic SiP package is shown in Fig. 7.37. Figure 7.38 is the top view of the package. Figure 7.39 represents the mold structure with ceramic substrate layout in an assembly process, in which two very narrow support pins press on the lead frame when the top and bottom cavities close during the assembly molding process.

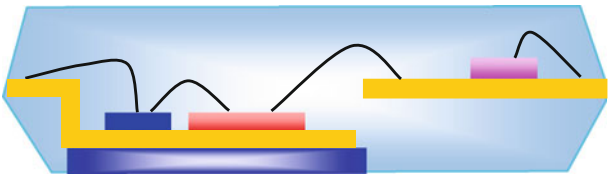


Fig. 7.37 Schematic representation of a power SiP package

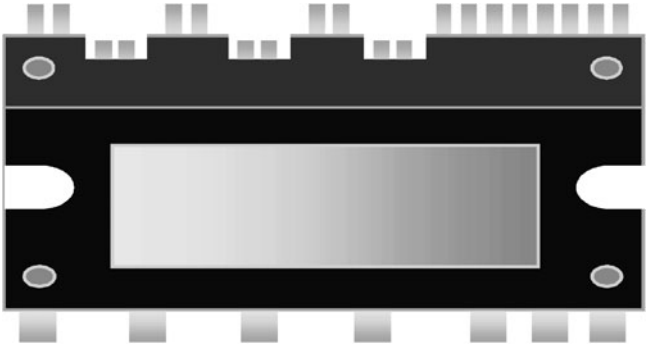


Fig. 7.38 A top view of a SiP package and its pins

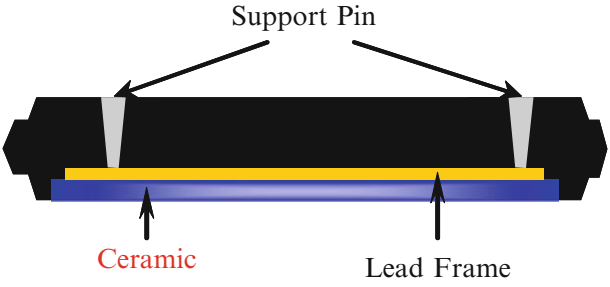


Fig. 7.39 Mold structure with ceramic substrate

From the cross section view of the package (Fig. 7.40) it can be seen that the location of the ceramic crack is just under the support pin. This suggests that the crack may possibly result from the mechanical impact of the support pins. In order to solve this problem efficiently, only the mechanical behavior of the ceramic substrate is considered, with the thermal effect neglected.

A simplified FEA model is used as sketched in Fig. 7.41. Only the ceramic substrate, part of the lead frame, part of the top and bottom cavity and two support pins are considered. The ceramic substrate is assumed to be elastic and the lead frame is assumed to be elastic, perfectly plastic. Both cavities and support pins are regarded as rigid materials. Rigid–flexible contacts are defined between the top

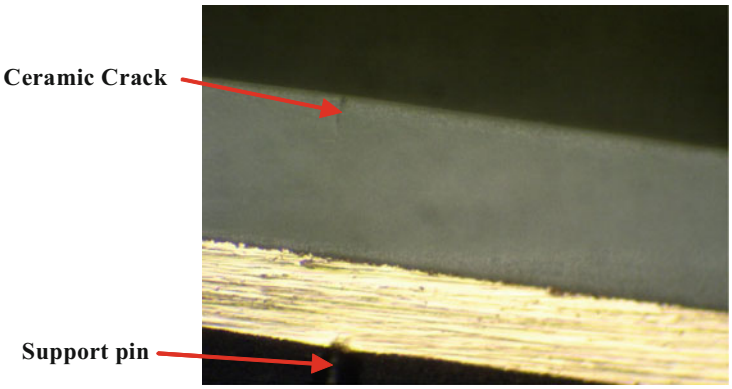


Fig. 7.40 Ceramic substrate crack in the SiP package

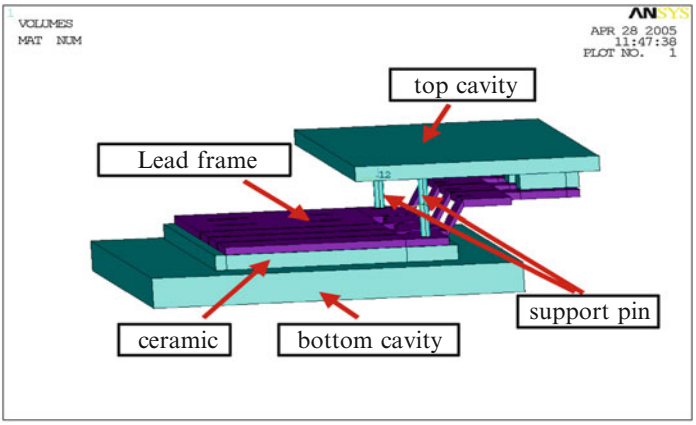


Fig. 7.41 The simplified SiP assembly model

cavity and lead frame, support pins and lead frame, bottom cavity and ceramic substrate, respectively. The mesh of the FE model is shown in Fig. 7.42.

7.4.1.2 The Modeling for the Mechanical Behavior of the Ceramics and Discussion

1. The effect of lead frame downset
   The SiP package is relatively large, and the lead frame is relatively flexible. During the die attach, ceramic substrate attach and wire bond assembly processes, the lead frame downset may change more or less. In this section, the change of the lead frame downset is investigated. Table 7.8 lists three different

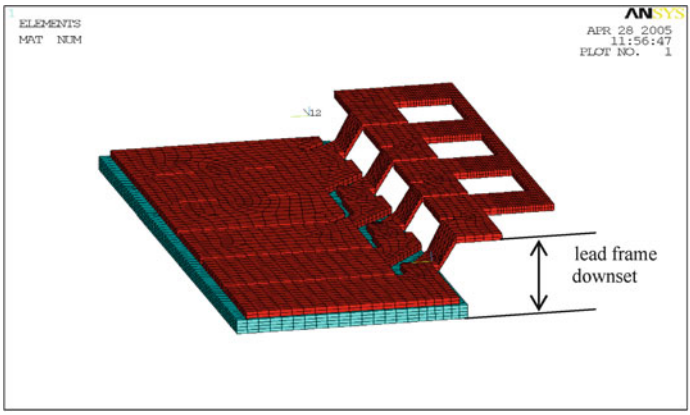


Fig. 7.42 Mesh of the assembly model

Table 7.8 Different lead frame downset values

	Lead frame downset (mm)	Remark
Model (a)	3.125	Normal case
Model (b)	3.05	
Model (c)	3.00	

lead frame downset values of the SiP model. The support pins have 0.04 mm overpress on the lead frame for the simulation of these three models.

Simulation results of the three models with different lead frame downsets are illustrated in Figs. 7.43 and 7.44, in which the contours of the first and third principal stresses are shown. It can be seen that the maximum first and third principal stresses on the ceramic substrate have almost the same value for the three different lead frame downsets. This indicates that the change of the lead frame downset before the assembly molding process is not likely a cause of the ceramic substrate crack.

2. Effect of support pin overpress
As seen in Figs. 7.39 and 7.41, two very narrow support pins press on the lead frame when the top and bottom cavities close during the assembly molding process. The tiny pin head produces high stress concentrations on the lead frame that transfers the stress into ceramic substrate and causes high local tensile stresses in the ceramic. The effect of the support pin overpress is investigated in this section. Table 7.9 lists different support pin overpress distances of two models.

Simulation results are illustrated in Figs. 7.45 and 7.46 for two models with different support pin overpress distances. The change of the support pin overpress tolerance has a large impact on the ceramic substrate stress. With a change of the support pin overpress distance from 0.04 to 0.1 mm, the maximum first principal stress on ceramic substrate increases from 493 to 722 MPa, and the maximum third principal stress increases from 1,300 to 1,800 MPa.

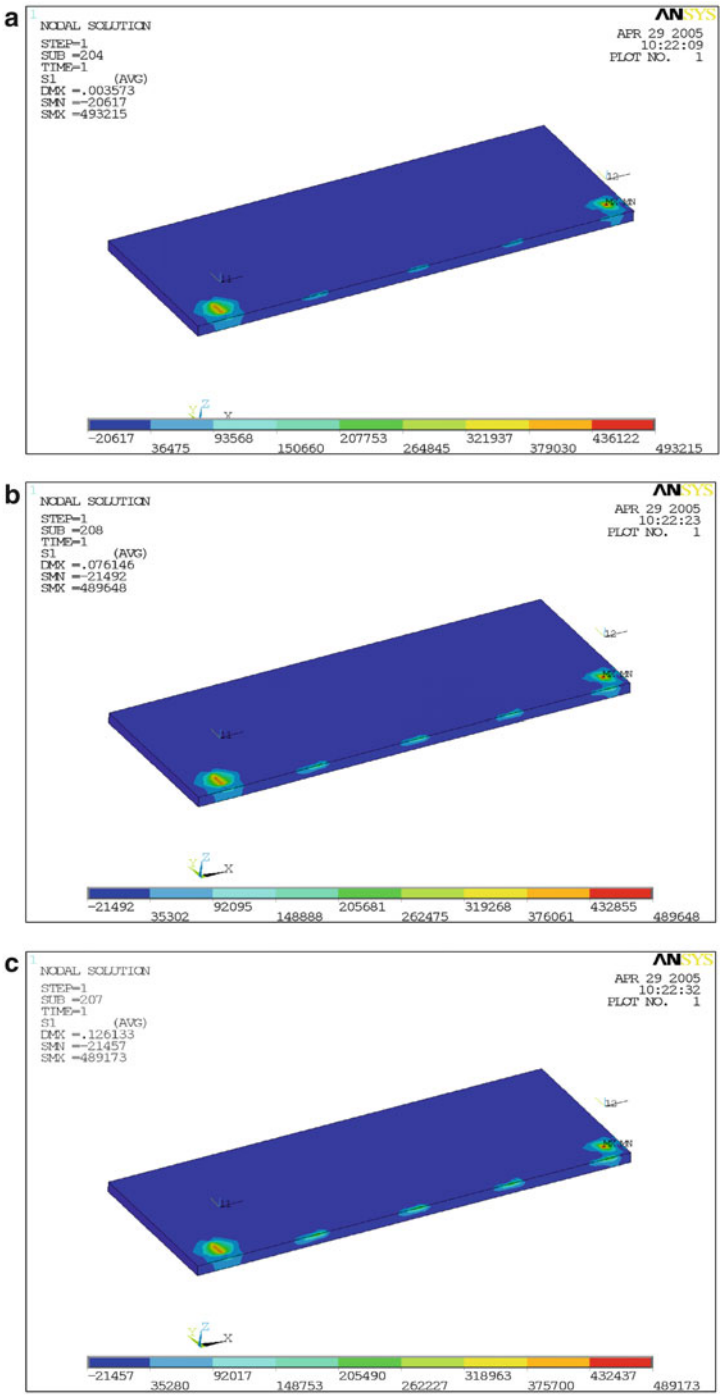


Fig. 7.43 Contours of the first principal stress on ceramic substrate for three models, maximum values: (**a**) 493 MPa, (**b**) 490 MPa, (**c**) 489 MPa

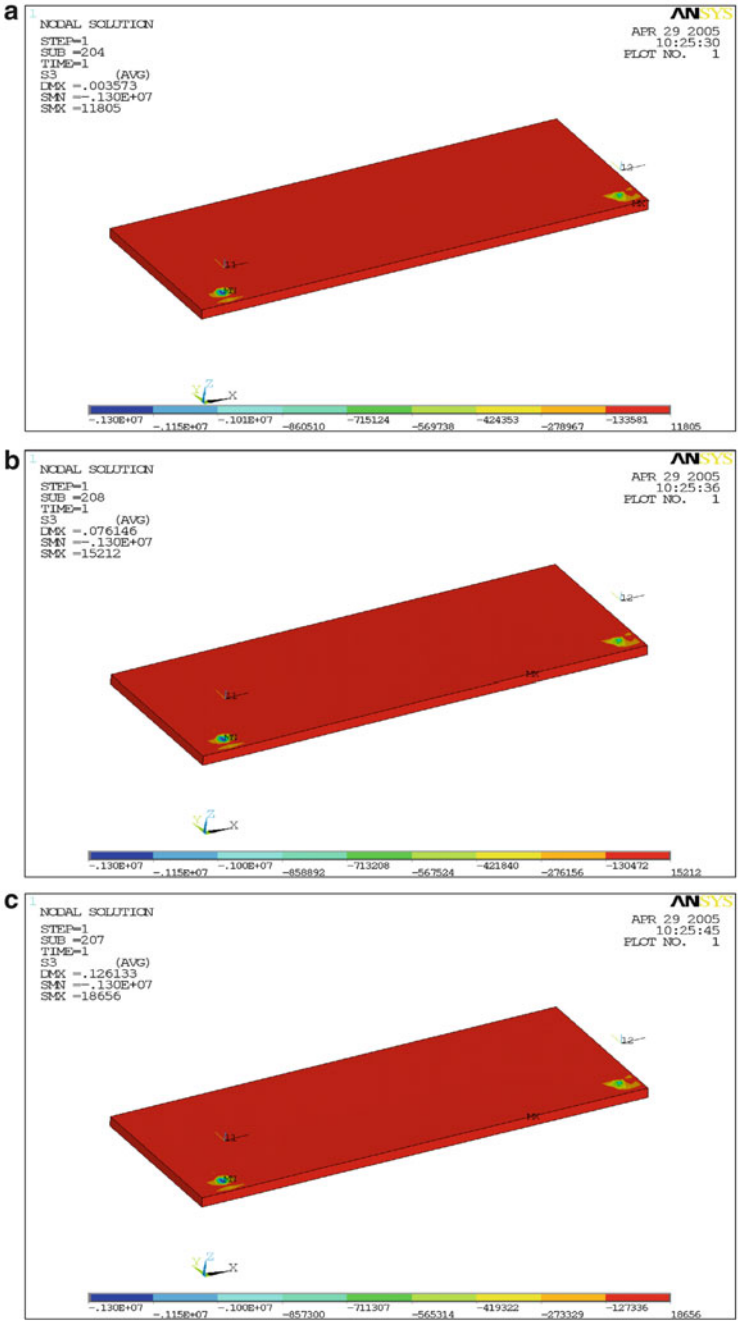


Fig. 7.44 Contours of the third principal stress on ceramic substrate for three models, maximum values: (**a**–**c**) 1,300 MPa

Table 7.9 Different support pin overpress distances

	Support pin overpress distance (mm)	Lead frame downset (mm)	Remark
Model (a)	0.04	3.125	Normal case
Model (b)	0.1	3.125	

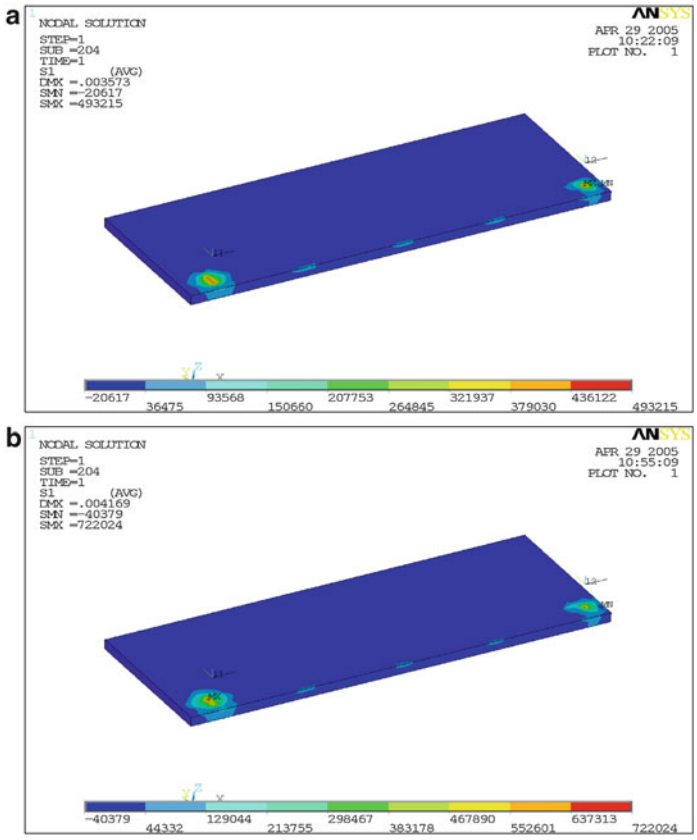


Fig. 7.45 Contours of the first principal stress on ceramic substrate for two models, maximum values: (**a**) 493 MPa, (**b**) 722 MPa

Reaction force on the support pins of the two models are listed in Table 7.10. The simulation results indicate that the force applied on the support pins has big impact on the stress of the ceramic substrate. Therefore, it should be controlled in a reasonable way. There is a trade-off balance. On the one hand, the cavity pressure should be large enough to press the ceramic substrate to contact with the bottom cavity, avoiding molding compound running between the bottom cavity and ceramic substrate. On the other hand, it should not be so large to induce too high stress in the ceramic substrate.

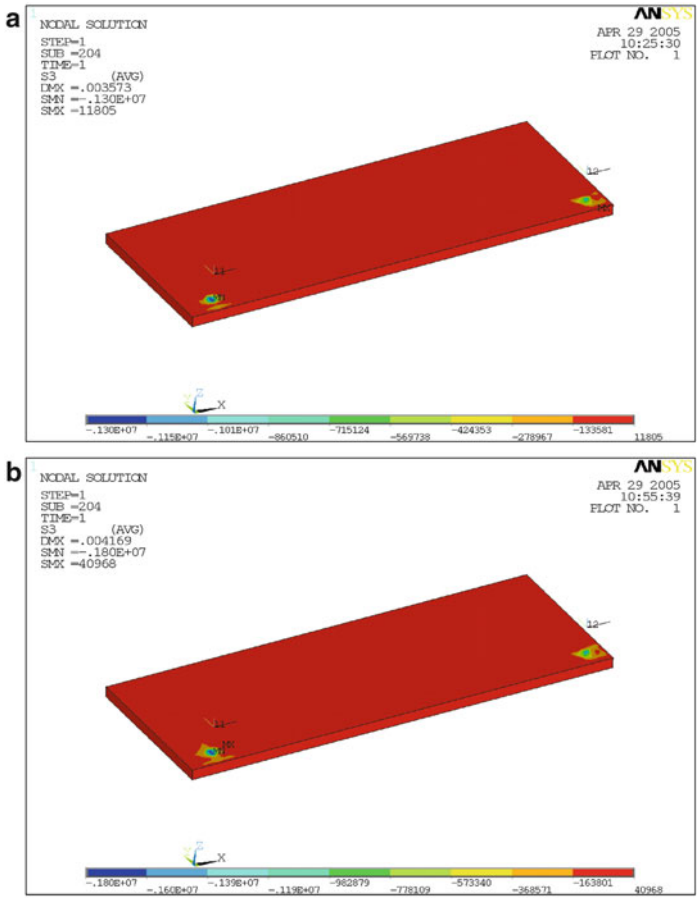


Fig. 7.46 Contour of the third principal stress on ceramic substrate for two models, maximum values: (**a**) 1,300 MPa, (**b**) 1,800 MPa

Table 7.10 Reaction force on support pins of the models

	Reaction force (N)	
	Pin 1	Pin 2
Model (a)	515	369
Model (b)	706	480

In order to effectively control the force acted on the lead frame by the support pin, a spring can be added at the back end of the support pin as shown in Fig. 7.47. According to the equilibrium of the force, the force of the spring should be equal to that applied to the lead frame by the support pin. Thus, the force of support pin can be controlled by the deformation of the spring according to Hooker's law. Furthermore, the elastic modulus of the spring can also be changed to meet the process conditions.

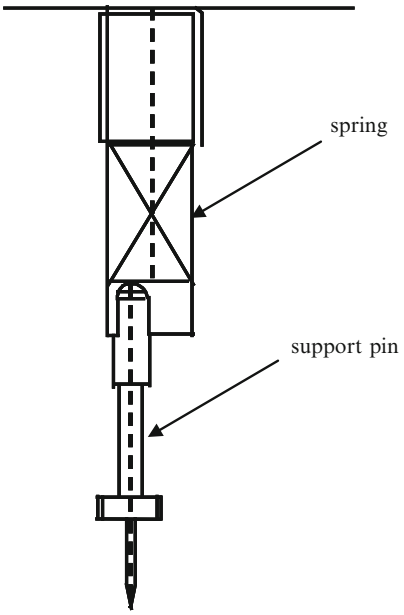


Fig. 7.47 Schematic representation of the support pin

The above studies address the ceramic substrate mechanical behavior and its failure in a lead frame based SiP during the assembly molding process. Both the effect of lead frame downset and the support pin overpress are simulated by the finite element. The simulation results have shown that the maximum first principal stress has almost the same value for three different lead frame downsets. This indicates that the change of the lead frame downset before the molding assembly process is not likely a cause of the ceramic substrate crack. However, the change of the support pin overpress tolerance has a large impact on the ceramic substrate stress. With the increment of support pin overpress, the maximum first principal stress in ceramic substrate increases significantly. Thus, the force of the support pin should be controlled effectively. This can be done by adding a spring at the back end of the support pin. By changing the elastic modulus of the spring and limiting the deformation of the spring, the ceramic substrate crack caused by the support pin overpress can be successfully avoided.

7.4.2 DBC Substrate

DBC means direct bond copper and denotes a process in which copper and a ceramic material are directly bonded. Normally, DBC has two layers of copper that are directly bonded onto an aluminum-oxide (Al_2O_3) or aluminum-nitride (AlN) ceramic base. The DBC process yields a superthin base and eliminates the need

Table 7.11 Properties of commonly available DBC

Uncladed ceramic	Aluminum oxide (Al_2O_3)	Aluminum nitride (AlN)
Purity	≥96%	≥97%
Dielectric strength	10 kV/mm	14 kV/mm
Thermal conductivity	24–28 W/mK	≥150 W/mK
Surface finish	Cu or electroless nickel plated Cu	Cu or electroless nickel plated Cu
Cu bonding strength	≥6 N/mm; 34.3 lb/in. (in accordance with DIN 53289)	≥3 N/mm; 17.2 lb/in. (in accordance with DIN 53289)
CTE	7.4 ppm (50–200°C)	5 ppm (25–200°C)
Application temperature (range)	−55 to 850°C	−55 to 850°C
Hydrogen embrittlement	Up to 400°C	Up to 400°C
Young's modulus	44,000 ksi	50,000 ksi
Tensile strength	26,000 psi	
Compressive strength	300,000 psi	300,000 psi

for the thick, heavy copper bases that were used prior to this process. Because power modules with DBC bases have fewer layers, they have much lower thermal resistance values and because the expansion coefficient matches silicon, they have much better power cycling capabilities (up to 50,000 cycles).

Properties of DBC ceramic substrates are good mechanical strength; mechanically stable shape, good adhesion and corrosion resistant. It has excellent electrical insulation, very good thermal conductivity, and super thermal cycling stability. The thermal expansion coefficient is close to that of silicon, so no interface layers are required. In addition, its good heat spreading may be structured just like printed circuit boards or "IMS substrates." It is also environmentally clean.

Advantages of DBC to the user are as follows: The 0.3-mm-thick copper layer permits higher current loading for the same conductor width. The excellent thermal conductivity provides the possibility of very close packaging of the power chips. This translates into more power per unit of volume and improved reliability of systems and equipment. The high insulation voltage results in improved personnel safety. DBC ceramic is the basis for the "chip-on-board" technology which represents the packaging trend for today and the future.

DBC ceramic substrates are the base materials of the future for both the construction and the interconnection techniques of electronic circuits. They will be employed as base material for electronic components with high values of power dissipation and demanding requirements concerning their thermal shock behavior as well as their failure rate, whenever normal printed circuit boards are no longer adequate.

Examples of application areas are power hybrids and power control circuits, power semiconductor modules, smart power building blocks, solid-state relays, high-frequency switch mode power supplies (SMPS), electronic heating devices, building blocks for automobile electronics, the military as well as aerospace technology. Table 7.11 lists the major properties of the DBC. Table 7.12 lists the basic design rule for DBC substrate material.

Table 7.12 Design rule for DBC substrates

Dimensions	Application dependent
Minimum width of Cu pattern	0.5 mm/19.7 mil
Minimum spacing between Cu patterns	0.5 mm/19.7 mil
Minimum spacing between Cu pattern and ceramic edge	0.35 mm/13.8 mil



Fig. 7.48 A typical DBC substrate with a chip mounted on it

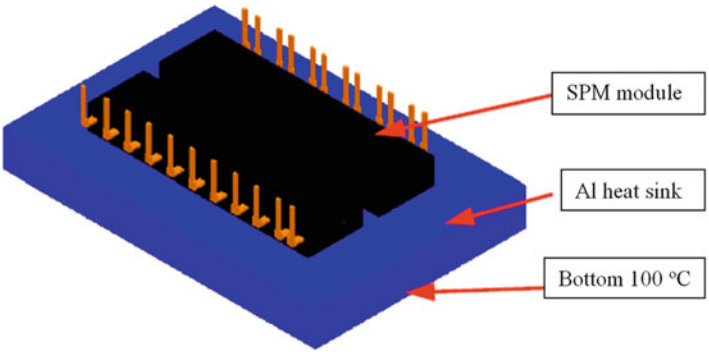


Fig. 7.49 A Fairchild power SPM module on a heat sink block with bottom temperature 100°C

Figure 7.48 shows a typical DBC substrate structure with a power chip mounted on it. Its top metal Cu is about 0.3 mm thickness and bottom Cu layer is about 0.2 mm thickness and the thickness of ceramic is about 0.63 mm.

7.4.3 Thermal Performance of Ceramic vs. DBC

As an application example, the thermal resistance of a Fairchild smart power module (SPM®) with both ceramic/lead frame and the DBC substrates is investigated. The SPM module is shown in Fig. 7.49. The internal two substrates (Ceramic and DBC) are shown in Fig. 7.50. This application example tries to show that the selection of different substrates will result in different thermal behaviors and will therefore impact the thermal resistance the power packages.

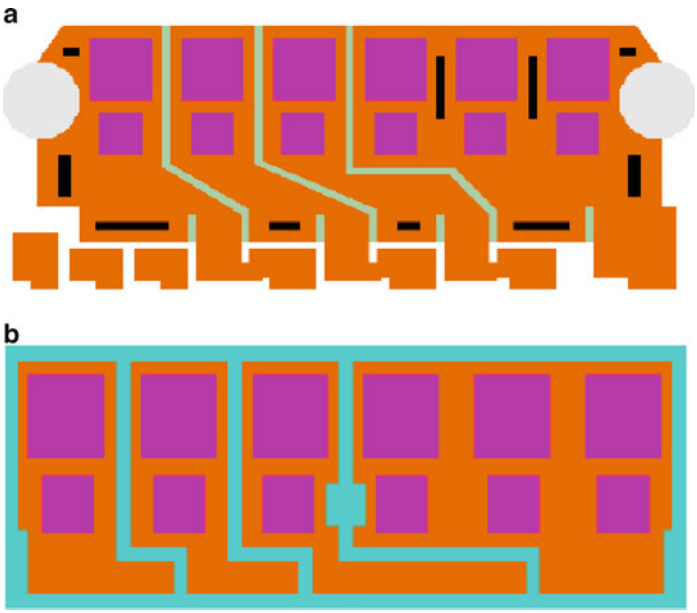


Fig. 7.50 Ceramic and DBC substrate layout in a Fairchild SPM module: (**a**) SPM module-A with ceramic Al_2O_3 (99.7%) substrate, (**b**) SPM module-B with DBC (Al_2O_3 96%) bonded with top and bottom Cu

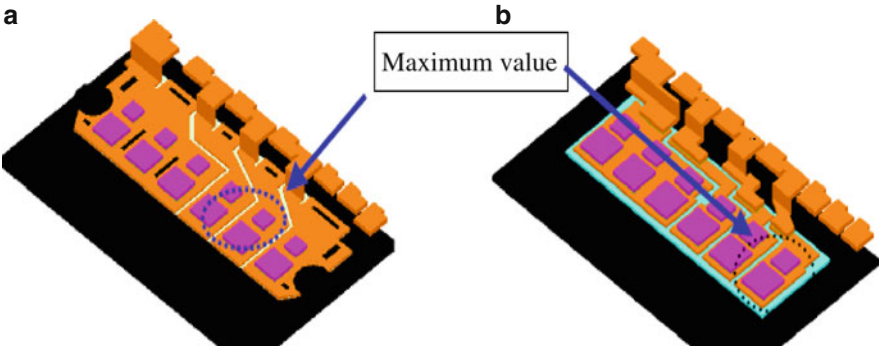


Fig. 7.51 The highest temperature location for the two substrates: (**a**) SPM module-A with ceramic substrate, (**b**) SPM module-B with DBC substrate

Figure 7.51 and the Table 7.13 give the result of the thermal analysis for the SPM power module with ceramic and DBC substrates. Figure 7.51 shows the location of maximum temperatures of the smart power module are different. Table 7.13 shows that the thermal resistance of the SPM module-B with DBC is better than the SPM module-A with ceramic substrates for both IGBT die and FRD die. In addition,

Table 7.13 Thermal resistance comparison (ceramic vs. DBC substrates) with 600 V/15 A

Thermal resistance	SPM-A	SPM-B
$R\theta_{jc}$ for IGBT (°C/W)	2.12	1.70
$R\theta_{jc}$ for FRD (°C/W)	2.44	2.21

Table 7.14 The effect of ceramic thickness of DBC on thermal resistance

Ceramic thickness in DBC (mm) (SPM-B)	Thermal resistance $R\theta_{jc}$ (°C/W) (chip center) with 15 A	Thermal resistance $R\theta_{jc}$ (°C/W) (package center) with 15 A
0.635	1.37	1.70
0.380	1.02	1.39
0.320	0.93	1.30
0.25	0.80	1.18

since the DBC is the ceramic material bonded with copper material at its top and bottom, its mechanical strength will be higher than the ceramic. Table 7.14 shows that the effect of the ceramic thickness in DBC on the thermal resistance $R\theta_{jc}$ of chip center and the package center of SPM module-B. The more inner the DBC, the smaller the thermal resistance.

7.5 Solder Material Characterization

This section introduces the solder material characterization for the power packages, in which the solder materials act as the solder die attach/bonding for MOSFET die or solder bumps forr wafer level chip scale power package. Since Pb-free solder materails are widely requested in the industry, this section majorly focuses on the mechanical characterization of a typical Pb-free solder material. Some common Pb solder material will be discussed at the end of this section. A series of tensile tests for Pb-free solder material 95.5Sn4.0Ag0.5Cu are conducted under a wide range of temperatures and constant strain rates to obtain the required data for characterization and for fitting the material parameters. Based on these test results, empirical equations of the tensile strength, elastic modulus, and yield stress are fitted as a functions of temperature. It is found that the temperature and strain rate have demonstrated crucial effects on tensile and creep properties of SnAgCu solder material. The test results have also displayed certain viscoplastic behavior, temperature dependence, strain rate sensitivity, and creep resistance. A procedure for the determination of the solder viscoplastic material parameters (Anand model) is discussed. In order to capture experimental data accurately, a modified Anand model with certain parameters which are the functions of the temperature and strain rate with the quadratic polynomial formula is discussed. Good agreements between the modified model prediction and experimental data have been obtained.

7.5.1 Introduction of the Solder Material Characterization

With the development of microelectronics and surface mounted technologies, there are a lot of researchers whose studies focus on studying the solder joint reliability of various Pb-solders. But Pb compound has been cited by International Environmental Protection Agency (IEPA) as one of the top 17 chemicals posing the greatest threat to human beings and the environment. As a result, developing feasible alternative lead-free solders for electronic assemblies is a necessity. There are many experimental data and constitutive models for SnPb based solder material, examples are 60Sn40Pb, 63Sn37Pb, and 62Sn36Pb2Ag [15–17]. In recent years, a lot of studies have been reported in extending these models to lead-free soldered assemblies. The viscoplastic material model called Anand model which has been used for SnPb solder material, is now applied to represent the inelastic behavior for lead-free solder material. ANSYS® finite element software offers the Anand model as a standard option with nine constants. Amagai et al. [18] have presented the Anand constants by tests for 95.75Sn3.5Ag0.75Cu and 98.5Sn1.0Ag0.5Cu, but it neglected to include one of the nine required constants, s_0, the initial value of deformation resistance. Kim et al. [19] published all nine constants, which has indeed updated the work by Amagai et al. for 98.5Sn1.0Ag0.5Cu. Rodgers et al. [20] have presented the test results for 95.5Sn3.8Ag0.7Cu, but their curves of Anand are quite different to those obtained by Reinikainen et al. [21] for 95.5Sn4.0Ag0.5Cu. Chen et al. [22] introduced a modified Anand model with h_0, the hardening coefficient, which is the function of temperature and strain rate. But this work just modifies the h_0 which might not be able to solve the entire problem with nine parameters. More work is needed in this research field of Pb-free material mechanical chacterization.

In this section, the material properties of 95.5Sn4.0Ag0.5Cu are tested and investigated with different temperatures and strain rates. The empirical equation for elastic modulus is fitted as a functions of temperature. The data of yield stress and tensile strength are determined as the function of temperature as well. Nine Anand constants are obtained using a nonlinear fitting procedure. To capture experimental curves more accurately, three parameters, namely, s_0, $\hat{s}$, and ξ are modified to be quadratic function of temperature and strain rate. The modified model has substantially improved the data fitting quality.

7.5.2 Solder Material Viscoplastic Constitutive Relation: Anand Model

Anand [23] developed a constitutive equation for the rate-dependent metals at high temperatures. It unifies the creep and rate-independent plastic behavior of the solder by making use of a flow equation and an evolution equation. The basic equations are listed as following.

The viscoplastic flow equation can be expressed as:

$$\dot{\varepsilon}_{\mathrm{p}} = A \exp\left(-\frac{Q}{RT}\right)\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{1/m} \tag{7.3}$$

where $\dot{\varepsilon}_{\mathrm{p}}$ is inelastic strain rate, A is preexponential factor, Q is activation energy, $R$is gas constant, T is absolute temperature, ξ is multiplier of stress, σ is equivalent stress, m is strain rate sensitivity.

The evolution equation follows:

$$\dot{s} = \left\{h_0(|B|)^a \frac{B}{|B|}\right\}\dot{\varepsilon}_{\mathrm{p}} \tag{7.4}$$

where

$$B = 1 - \frac{s}{s^*} \tag{7.5}$$

and

$$s^* = \hat{s}\left[\frac{\dot{\varepsilon}_{\mathrm{p}}}{A}\exp\left(\frac{Q}{RT}\right)\right]^n \tag{7.6}$$

where h_0 is the hardening/softening constant, a is the strain rate sensitivity of hardening/softening. The quantity s* represents a saturation value of deformation resistance s, associated with a set of given temperature and strain rate as shown in (7.6). $\hat{s}$ is a coefficient, and n is the strain rate sensitivity for the saturation value of deformation resistance, respectively. The set of Anand constitutive equations can account for the physical phenomena of strain-rate and temperature sensitivity, strain rate history effects, isotropic strain-hardening, and the restoration process of dynamic recovery.

There are nine material parameters of the unified rate-dependent Anand model A, Q/R, ξ, m, h_0, $\hat{s}$, n, a, and s_0 in (7.3)–(7.6). The last one s_0 is the initial value of the deformation resistances, which is needed in solution of the evolution of deformation resistance in (7.4).

The flow equation is similar to that used for describing the steady-state secondary creep but with the addition of an internal state variable defined as the deformation resistance, s, which depends on the temperature- and rate-dependent strain history of the material. The assumed relationship between the stress of the model and the deformation resistance variable can be written as

$$\sigma = cs, \quad c = (T, \dot{\varepsilon}_{\mathrm{p}}) \tag{7.7}$$

where, by definition,

$$c = \frac{1}{\xi}\sinh^{-1}\left(\frac{\dot{\varepsilon}_{\mathrm{p}}}{A}\exp\left(\frac{Q}{RT}\right)\right)^m \tag{7.8}$$

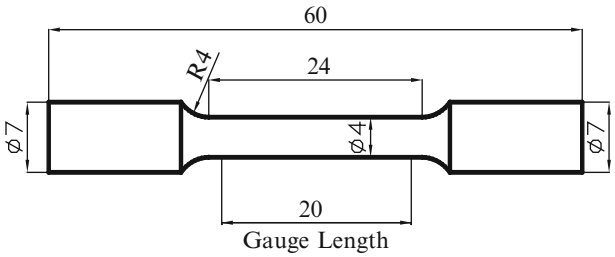


Fig. 7.52 Tensile test specimen for solder material

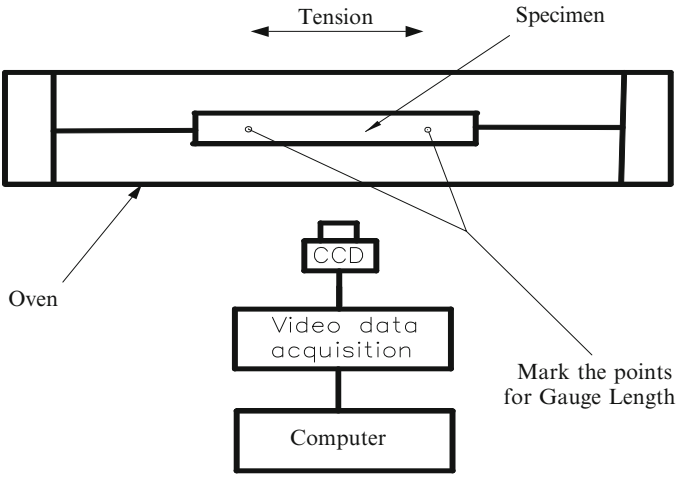


Fig. 7.53 Digital strain measurement system

7.5.3 Experiment Procedure

To obtain the data for the fitting parameters of the lead-free material 95.5Sn4.0Ag0.5Cu, a series of tensile tests under different temperatures (25, 75, and 150°C) and with different strain rates are carried out. The test specimens are made in a casting dog bone shape based on the ASTM E 8M-04 standard, with a diameter of 4 mm and a gage length of 20 mm as shown in Fig. 7.52. All the tests are performed using a Reger screw-driven universal test machine with a 3,000 N load cell and an integrated thermal chamber. The temperature is kept constant during testing.

The axial strain is obtained from an extensometer which is fixed on the specimen at room temperature. At high temperatures, a precision noncontact strain digital measurement technique, DSCM (digital speckle correlation method), is adopted to obtain the true strain of gage length. Two points are marked on specimen for gage length. When the test is conducted, data of two points are collected and analyzed through a charge coupled device (CCD) camera, video data acquisition system. Figure 7.53 shows the the noncontact digital strain measurement system.

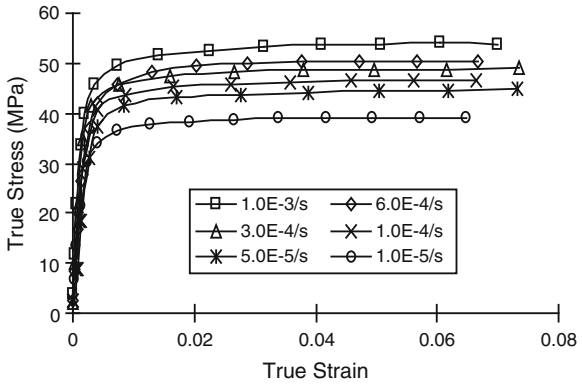


Fig. 7.54 True stress vs. true strain for 95.5Sn4.0Ag0.5Cu at 25°C and different strain rates

Note that tests should be carried out under constant strain rate conditions. However, due to the different function of our test equipment, the constant crosshead displacement rate is applied. The crosshead displacement rate is calculated from the strain rate according to the scale of the specimen. Each test must be repeated six times with the same condition, the same strain rate and the same temperature, based on the ASTM E 8M-04 standard. The test results of the stress and strain relations are processed by averaging all data in the six time tests.

The temperature dependent Young's modulus, yield stress and the tensile strength of the lead-free material can also be obtained from the stress–strain curves at the range of temperature from 25 to 175°C. The data of load and displacement collected in real time by the software of test machine are converted to true stress and true strain.

7.5.4 The Test and Characterization Results

Figures 7.54–7.56 show the true stress vs. true strain curve of 95.5Sn4.0Ag0.5Cu at three temperatures with a range of strain rates. It can be seen from these figures that there appear a general feature of strain hardening behavior at the beginning in the stress–strain curves, and the deformation behavior of 95.5Sn4.0Ag0.5Cu is highly rate dependent. After that, the plastic flow reaches the steady state. It can be seen that the tensile strength and yield stress increase with the strain rate increases.

Figures 7.57–7.59 summarize the true stress vs. true strain for 95.5Sn4.0Ag0.5Cu at strain rate 1.0E − 3/s, 1.0E − 4/s and 1.0E − 5/s with three temperatures. It can be seen from these figures that the deformation behavior of the solder is highly temperature dependent. Here, the value of saturation stresses can be obtained from constant displacement rate tests when the test has reached steady state. For example, with a strain rate of 1.0E − 4/s at 25°C, the stress saturates to about 45.2 MPa, as shown in Fig. 7.58. From those figures, one can get the saturation stresses at different

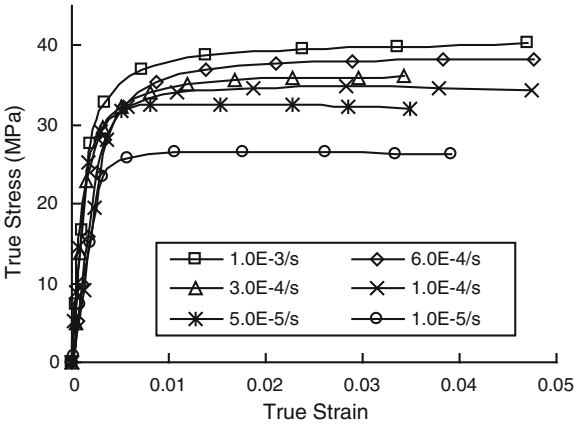


Fig. 7.55 True stress vs. true strain for 95.5Sn4.0Ag0.5Cu at 75°C and different strain rates

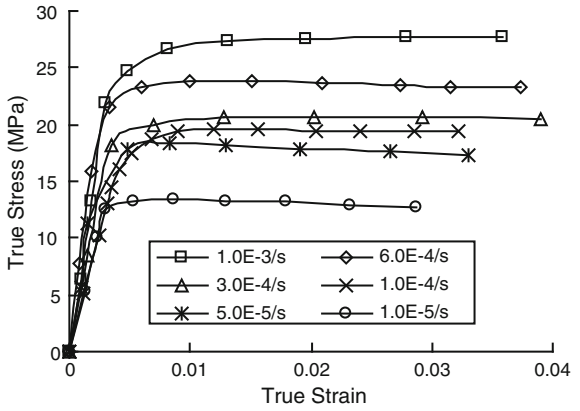


Fig. 7.56 True stress vs. true strain for 95.5Sn4.0Ag0.5Cu at 150°C and different strain rates

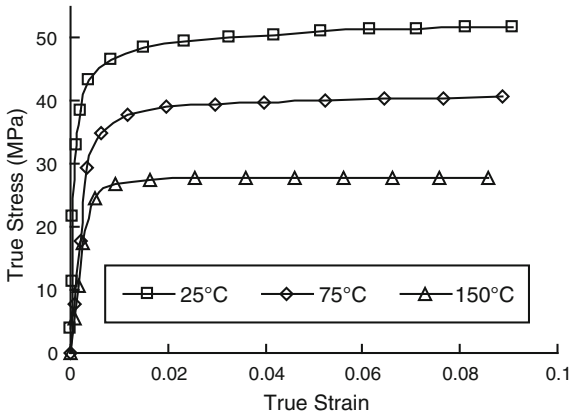


Fig. 7.57 True stress vs. true strain for 95.5Sn4.0Ag0.5Cu at strain rate 1.0E − 3/s and three temperatures

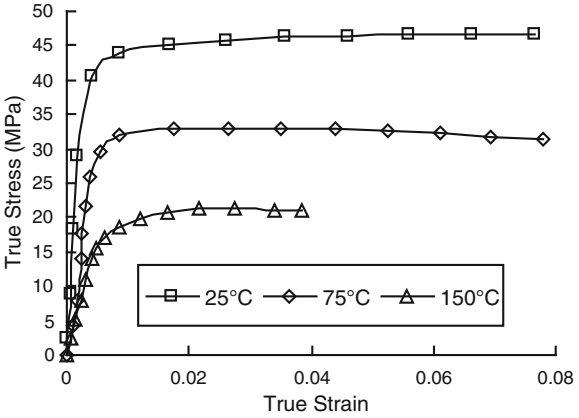


Fig. 7.58 True stress vs. true strain for 95.5Sn4.0Ag0.5Cu at strain rate 1.0E − 4/s and three temperatures

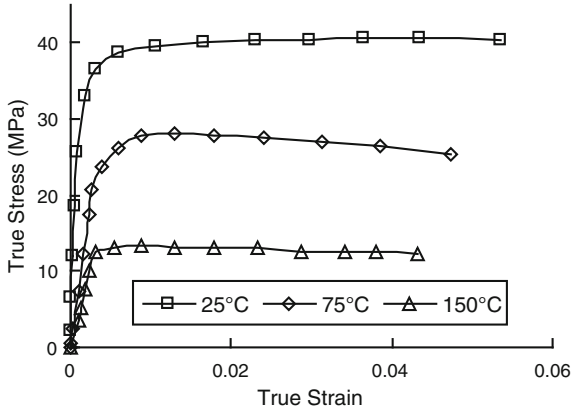


Fig. 7.59 True stress vs. true strain for 95.5Sn4.0Ag0.5Cu at strain rate 1.0E − 5/s and three temperatures

strain rates and different temperatures. With these test data, Anand parameters can be obtained based on a data fitting algorithm. It can also be seen that the tensile strength and yield stress increase while the temperature decreases.

Figure 7.60 shows the variation of the tensile strength and yield stress with temperature at the strain rate of 7.5E − 3/s. It can be clearly seen from Fig. 7.60 that the tensile strength and yield stress are directly related to temperature.

The temperature dependent Young's modulus for this lead-free material is also obtained from the stress–strain curves in the range of temperature from 25 to 175°C at 7.5E − 3/s.

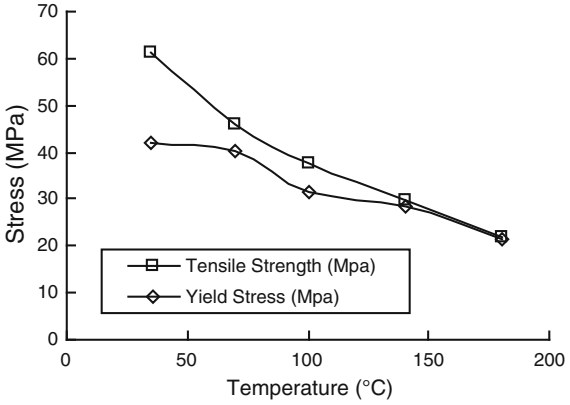


Fig. 7.60 Tensile strength and yield stress vs. temperature at strain rate 7.5E − 3/s

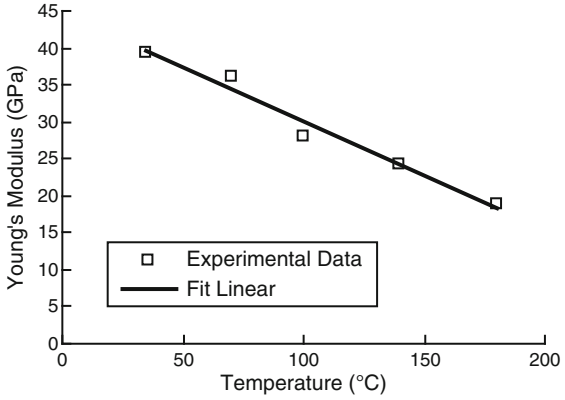


Fig. 7.61 Temperature dependent Young's modulus at strain rate 7.5E − 3/s

The results are plotted in Fig. 7.61. It has observed that the Young's modulus is approximately a linear function of temperature at strain rate 7.5E − 3/s:

$$E\ (\text{GPa}) = 44.7 - 0.146T\ (^{\circ}\text{C}) \tag{7.9}$$

We should indicate that, it is likely that because the tests are carried out on the cast test specimens, the results may not represent the true behavior of actual solder joint. In addition, the scale of the microstructure and the presence of intermetallics at the specimen surface might have an effect on the viscoplastic behavior. Finally, the annealing and aging of the specimens prior to testing could also affect the material properties. These factors have not been considered in this study.

7.5.5 Anand Model Parameter Data Fitting

In order to apply the Anand model to simulate the thermomechanical responses of solder joints in electronic packaging and surface mount technology, the material parameters of the constitutive relations must be determined first. The data of load and displacement at real time by the software of test machine are converted to true stress and true strain. Then they are fitted into Anand model parameters by First Optimization®, an effective nonlinear fitting software.

When the steady state plastic flow occurs, it reaches the saturation stress. For viscoplastic deformation behavior, this steady state plastic flow happens when the plastic flow has been fully developed and equals to the applied strain rate at a fixed temperature and a fixed strain rate. On the other hand, at a given stress and temperature, one can gain the steady state creep rate. This steady state creep rate is equivalent to the steady state plastic flow in constant strain rate testing when the saturation stress equals the given stress in steady state creep testing. The saturation stress can be obtained as follows:

$$\sigma^* = \frac{\hat{s}}{\xi}\left[\frac{\dot{\varepsilon}_p}{A}\exp\left(\frac{Q}{RT}\right)\right]^n \sinh^{-1}\left[\left(\frac{\dot{\varepsilon}_p}{A}\exp\left(\frac{Q}{RT}\right)\right)^m\right] \tag{7.10}$$

where the material parameters A, Q/R, m, n, and $\hat{s}/\xi$ in (7.10) can be fitted to the $\dot{\varepsilon}_p - \sigma^*$ pair data obtained from constant strain rate tests.

Values of the nine material parameters A, Q/R, ξ, m, h_0, $\hat{s}$, n, a, and s_0 of Anand model for 95.5Sn4.0Ag0.5Cu solder are determined by the procedures outlined as follows.

(a) Determination of the saturation stresses σ^* and steady state plastic strain rates from all the tests.
(b) Nonlinear fitting of A, Q/R, m, $\hat{s}/\xi$, and n in (7.10).
(c) Determination of ξ and $\hat{s}$. Using the values determined in step (b), the parameter ξ is selected such that the ratio of σ/s is less than unity, and $\hat{s}$ is then determined from the combined term $\hat{s}/\xi$.
(d) Nonlinear fitting of h_0, a, and s_0. The stress of Anand model can be expressed as

$$\sigma = \sigma^* - [(\sigma^* - cs_0)^{(1-a)} + (a-1)\{(ch_0)(\sigma^*)^{-a}\}\varepsilon_p]^{1/(1-a)} \tag{7.11}$$

with

$$c = \frac{1}{\xi}\sinh^{-1}\left(\frac{\dot{\varepsilon}_p}{A}\exp\left(\frac{Q}{RT}\right)\right)^m \tag{7.12}$$

The values of material parameters h_0, a, and s_0 are obtained from the $\sigma - \varepsilon_p$ curves (especially the transient state) with various temperatures and strain rates. In the fitting, the saturation stresses given in step (a) are also used. The material parameters for

Table 7.15 Fitted Anand model constants for SnAgCu405

Description	Symbol	Units	SnAgCu405
Initial value of s	s_0	MPa	20
Activation energy	Q/R	K	10,561
Preexponential factor	A	1/s	325
Stress multiplier	ξ	–	10
Strain rate sensitivity of stress	m	–	0.32
Hardening coefficient	h_0	MPa	8.0E5
Coefficient for deformation resistance saturation value	$\hat{s}$	MPa	42.1
Strain rate sensitivity of saturation value	n	–	0.02
Strain rate sensitivity of hardening coefficient	a	–	2.57

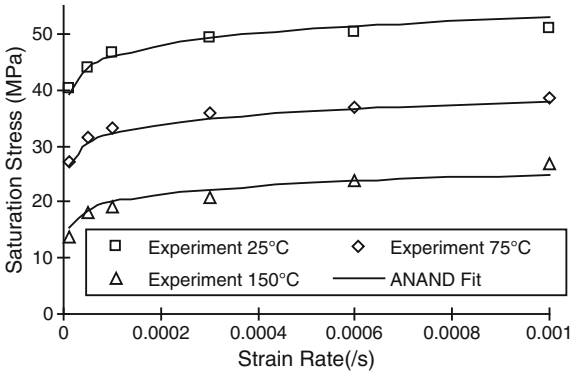


Fig. 7.62 Saturation stress from experiment and Anand fit at different temperatures

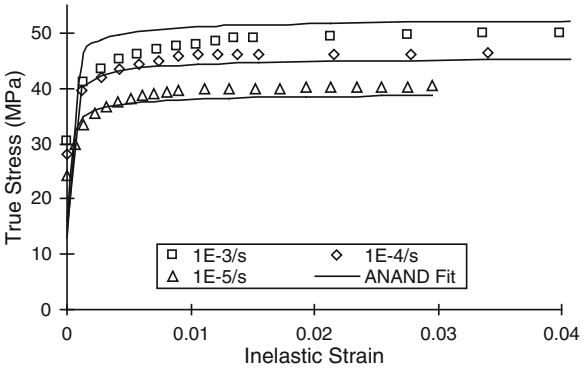


Fig. 7.63 Experiment data and Anand fit curve at 25°C

95.5Sn4.0Ag0.5Cu solder determined by following this procedure are listed in Table 7.15. It can be clearly seen from Fig. 7.62 that the saturation stress is temperature and strain rate dependent. Comparisons of the data fitting Anand curves with the test data of 95.5Sn4.0Ag0.5Cu solder are shown in Figs. 7.63–7.68, respectively.

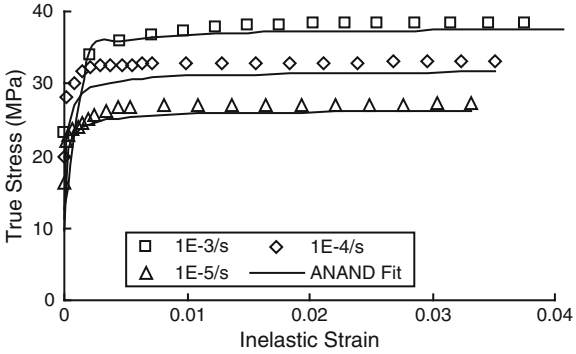


Fig. 7.64 Experiment data and Anand fit curve at 75°C

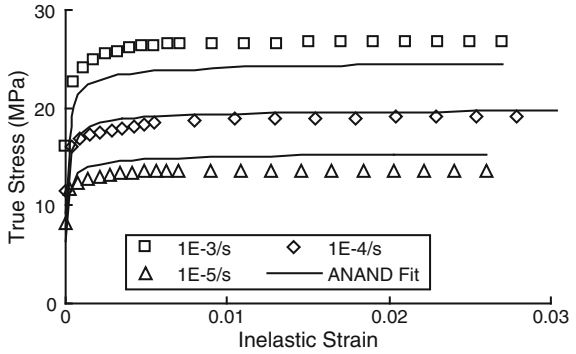


Fig. 7.65 Experiment data and Anand fit curve at 150°C

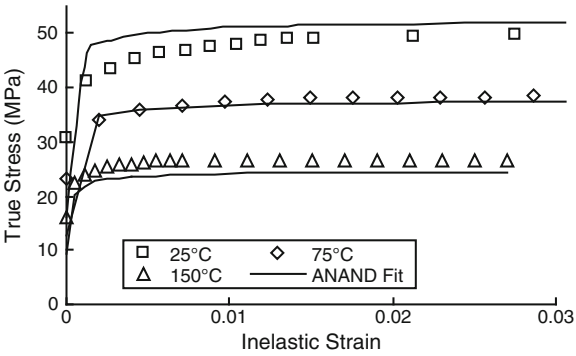


Fig. 7.66 Experiment data and Anand fit curve at 1E − 3/s

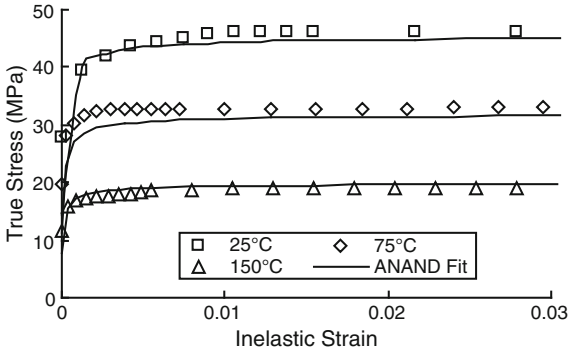


Fig. 7.67 Experiment data and Anand fit curve at 1E − 4/s

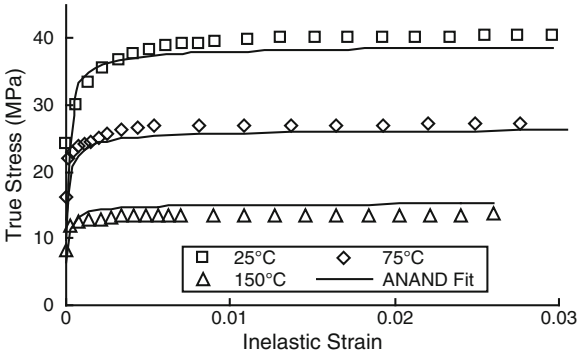


Fig. 7.68 Experiment data and Anand fit curve at 1E − 5/s

Above figures show that the Anand model fitiing curves can represent the nonlinear deformation behavior at different strain rate and temperatures. Nevertheless, the result of Anand model fitting is not perfect to us. One can see there are some deviations from the experimental data and some errors may also come from the experiments. The result shows that Anand model has limited ability to describe the temperature/strain rate cross dependent relationship, especially at high homologues temperature. A modified Anand model is proposed in the next section.

7.5.6 Modified Anand Model Parameter

As mentioned in previous section, Anand model needs more temperature sensitivity and strain rate sensitivity to fit lead free material better. Some researcher suggested modifying the s_0 as linearly temperature dependent [20]. Pei et al. [24] modified all

Table 7.16 Anand constants based on (7.13)

Description	Symbol	Units	SnAgCu405
Initial value of s	s_0	MPa	–
Activation energy	Q/R	K	12,480
Preexponential factor	A	1/s	4,223
Stress multiplier	ξ	–	–
Strain rate sensitivity of stress	m	–	0.34
Hardening coefficient	h_0	MPa	2.98E5
Coefficient for deformation resistance saturation value	$\hat{s}$	MPa	–
Strain rate sensitivity of saturation value	n	–	0.03
Strain rate sensitivity of hardening coefficient	a	–	1.98

Table 7.17 Three modified coefficients for (7.13)

Symbol	a_0	a_1	a_2	a_3	a_4
S_0	18	0.24967	−6.25E − 4	5,925	−3.63E6
$\hat{s}$	−7	0.33	−6.48E − 4	–	–
ξ	18.7	0.016	−1.1E − 4	–	–

nine parameters as linearly temperature dependent, this requires a large amount of work. However, after observation through test curves, it has found that some parameters are only slightly dependent on temperature. So those parameters could be treated as constants. In this study, three parameters, namely, s_0, $\hat{s}$, and ξ are further investigated based on our observation and study of the test data; they are considered as the functions of both temperature and rate dependent:

$$s_0 = a_0 + a_1 T + a_2 T^2 + a_3 \dot{\varepsilon}_p + a_4 \dot{\varepsilon}_p{}^2$$

$$\hat{s} = a_0 + a_1 T + a_2 T^2$$

$$\xi = a_0 + a_1 T + a_2 T^2 \tag{7.13}$$

Nonlinear optimization fitting method is used for the data fitting of the Anand model. The constants of this lead free solders are listed in Tables 7.16 and 7.17. The comparisons of the modified Anand model simulation with test curves of 95.5Sn4.0Ag0.5Cu are shown in Figs. 7.69–7.81, respectively.

Compare Figs. 7.62–7.68 with Figs. 7.69–7.75, it is obvious that the temperature and strain rate dependent Anand model fitting in Figs. 7.69–7.75 is much better than the initial version in Figs. 7.62–7.68. More parameters are an additional to this improvement. Even Chen et al. [22] modified h_0, the hardening coefficient, as both temperature and strain rate dependent. Nevertheless, just to modify the h_0 may not

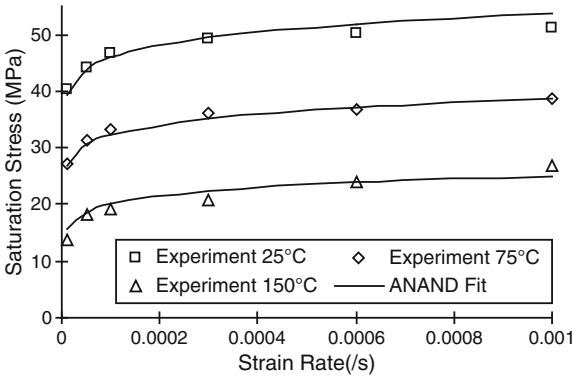


Fig. 7.69 Saturation stress from experiment and modified Anand fit at different temperatures

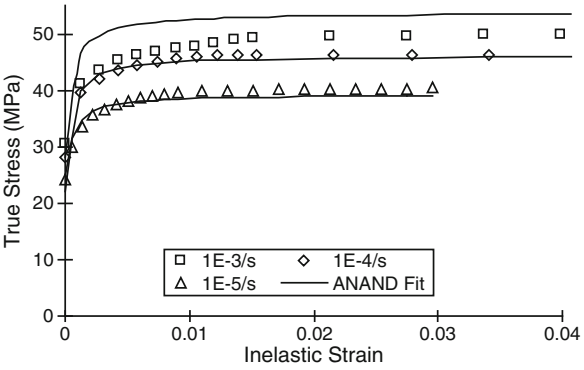


Fig. 7.70 Experiment data and modified Anand fit curve at 25°C

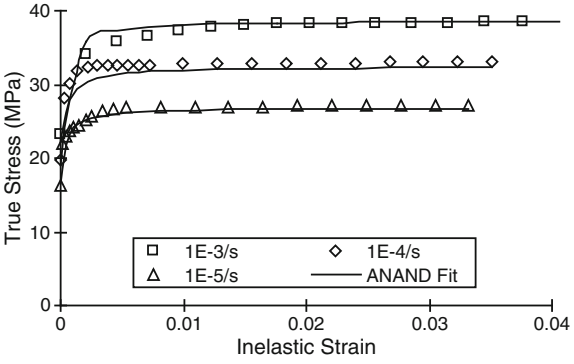


Fig. 7.71 Experiment data and modified Anand fit curve at 75°C

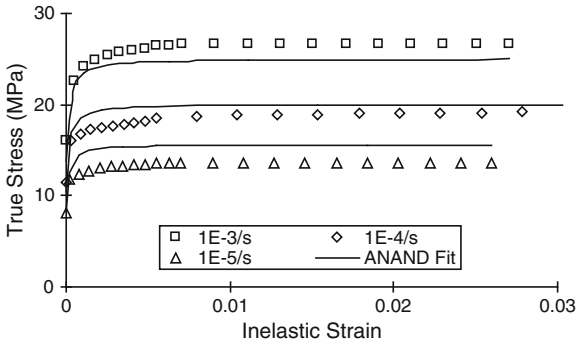


Fig. 7.72 Experiment data and modified Anand fit curve at 150°C

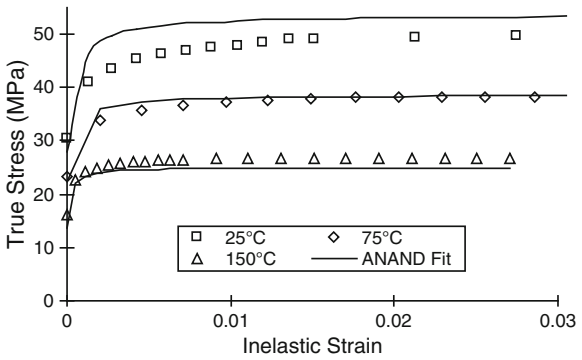


Fig. 7.73 Experiment data and modified Anand fit curve at 1E − 3/s

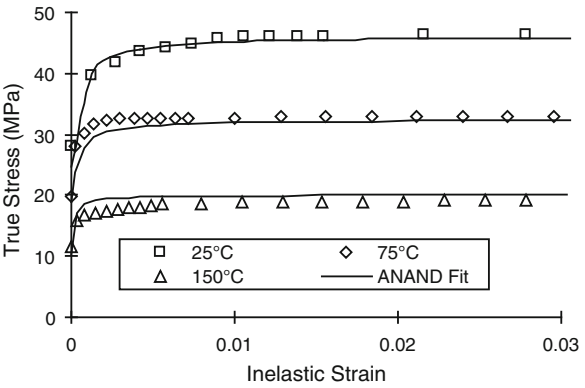


Fig. 7.74 Experiment data and modified Anand fit curve at 1E − 4/s

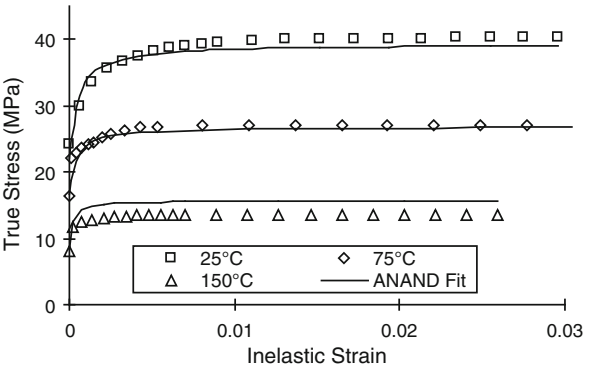


Fig. 7.75 Experiment data and modified Anand fit curve at 1E − 5/s

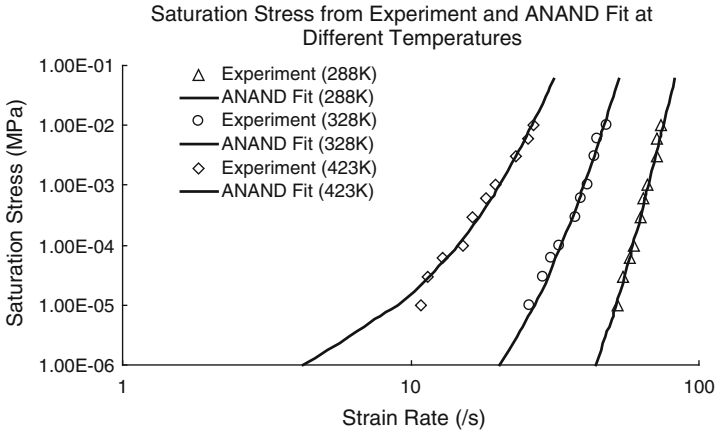


Fig. 7.76 The comparison of the Anand model data fitting curves with the tested data of 91.5Sn8.5Sb for the saturation stress

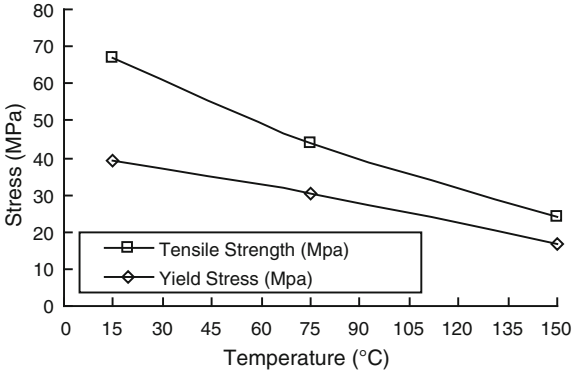


Fig. 7.77 The yield and tensile stress of the 91.5Sn8.5Sb

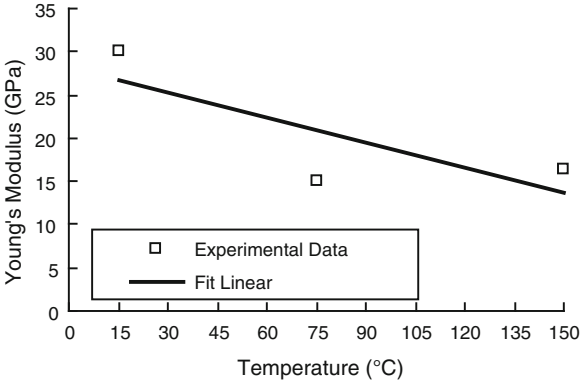


Fig. 7.78 The Young's modulus of the 91.5Sn8.5Sb

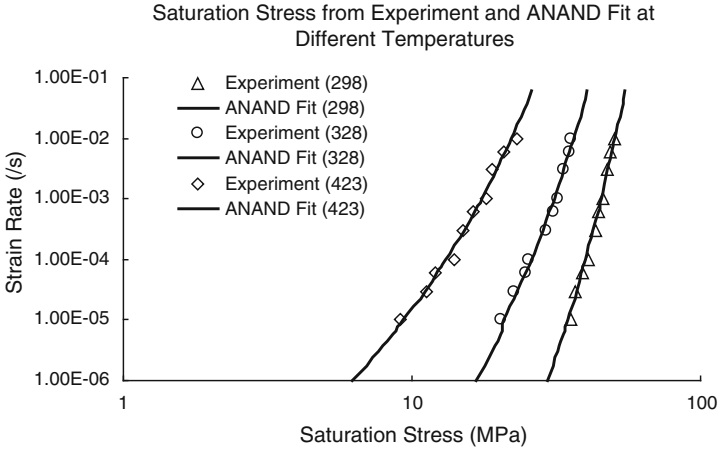


Fig. 7.79 The comparison of the Anand model data fitting curves with the tested data for the saturation stress for 92.5Pb5Sn2.5Ag solder material

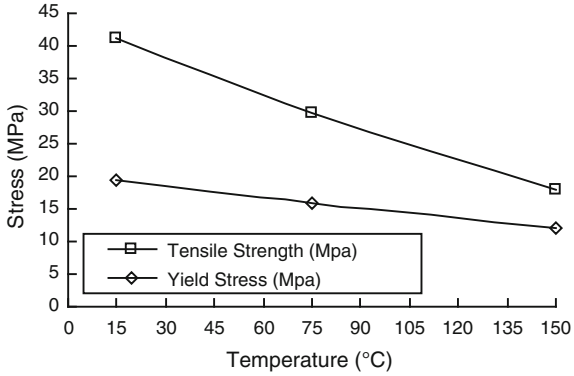


Fig. 7.80 The yield and tensile stress of the 92.5Pb5Sn2.5Ag

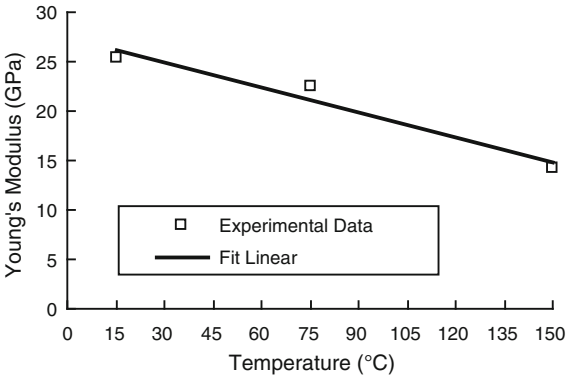


Fig. 7.81 The Young's modulus of the 92.5Pb5Sn2.5Ag

be able to effectivly solve the entire nine parameter system. The temperature dependence of other parameters in the model suggest the form of Anand model has its limitation on solder materials. Addidional models need to be explored to describe the deformation of solder material more accurately and more efficiently.

7.5.7 Discussions and Other Solder Materials

In this session, the characterization and tensile tests for Pb-free material 95.5Sn4.0Ag0.5Cu with different temperatures and strain rates have been conducted. It is found that this type of lead-free material has strong dependence on both test temperature and strain rate. The values of tensile strength and yield stress have directly related to temperature. The Young's modulus may approximately be expressed as a linear function of temperature.

The Anand material constitutive model is applied to represent the inelastic deformation behavior of this pb-free solder 95.5Sn4.0Ag0.5Cu. A data fitting procedure is introduced based on the nonlinear data fitting software First Optimization®. To fit the tested stress–strain curves more perfectly, a modified method is also discussed in this work. The materials parameters of Anand model obtained through the modified method are verified to see if it can predict the viscoplastic deformation behavior. As a result, the modified Anand model can indeed fit much better than the initial Anand model. The methodology has been applied to the lead-free material SAC family for characterization.

There are other type of Pb-free materials for power package that have been tested, such as 91.5Sn8.5Sb, its material characterization data fitting can be seen in Table 7.18.

Table 7.18 Anand parameter for Pb-free solder material 91.5Sn8.5Sb

Description	Symbol	Units	91.5Sn8.5Sb
Initial value of s	s_0	MPa	48.15
Activation energy	Q/R	K	13816.8
Preexponential factor	A	1/s	2.23E + 8
Stress multiplier	ξ	–	13.85
Strain rate sensitivity of stress	m	–	0.417
Hardening coefficient	h_0	MPa	291,215
Coefficient for deformation resistance saturation value	$\widehat{s}$	MPa	76.03
Strain rate sensitivity of saturation value	n	–	0.01
Strain rate sensitivity of hardening coefficient	a	–	2.34

Table 7.19 Anand parameter for solder material 92.5Pb5Sn2.5Ag

Description	Symbol	Units	92.5Pb5Sn2.5Ag
Initial value of s	s_0	MPa	33.82
Activation energy	Q/R	K	12,832
Preexponential factor	A	1/s	9.63E + 7
Stress multiplier	ξ	–	6.85
Strain rate sensitivity of stress	m	–	0.272
Hardening coefficient	h_0	MPa	16,915
Coefficient for deformation resistance saturation value	$\widehat{s}$	MPa	54.13
Strain rate sensitivity of saturation value	n	–	0.002
Strain rate sensitivity of hardening coefficient	a	–	1.74

Figure 7.76 gives the comparison of the data fitting curves of Anand model with the tested data for the saturation stress vs. strain rate at different temperatures for lead free material 91.5Sn8.5Sb. It shows the perfect agreement for the fitting and tested behavior of the saturation stress. The yield stress, tensile stress, and the Young's modulus as the function of the temperature are shown in Figs. 7.77 and 7.78.

Besides the lead free materials, there are also some Pb solder materials that the power packages are still used in the power industry, such as 92.5Pb5Sn2.5Ag. Table 7.19 lists the data fitting of the parameters of the Anand constitutive model. Figure 7.79 shows the comparison of the data fitting curves of Anand model with the tested data for the saturation stress vs. strain rate at different temperatures for the solder material 92.5Pb5Sn2.5Ag. It shows that the perfect agreement for the fitting and tested behavior of the saturation stress. The yield stress, tensile stress and the Young's modulus as the function of the temperature are shown in Figs. 7.80 and 7.81. The material behavior is very temperature dependent. As the temperature increases, the lead solder material becomes softer, and all the yield stress, tensile strength, and the Young's modulus decrease.

7.6 Lead Frame Material Characterization

Lead frame materials are widely used in power package due to its excellent electrical, thermal, mechanical performance and low cost. Understanding the material behavior of lead frame is critical for the design of power package and module.

The typical lead frames used for power packages are copper based material with surface plating, such as KFC-H, 12SnOFC-H, and C194. This section gives the test and characterization results of the mechanical properties for these lead frames. The test is based on ASTM E8M-04 for testing the Young's modulus, yield stress and tensile strength under different temperatures. Similar to Sect. 7.5, the axial strain is obtained from an extensometer which is fixed on the specimen at room temperature. At high temperatures, a precision noncontact strain digital measurement technique, DSCM (digital speckle correlation method), is adopted to obtain the true strain of gage length. Two points are marked on specimen for gage length. When the test starts, data of two points are collected and analyzed through a CCD camera, video data acquisition system (see Fig. 7.53). The tensile test temperatures are selected to be 25, 75, 150, 200, and 260°C. Figure 7.82 gives the test specimen. In Fig. 7.82, The gage length G is 50 mm, width of the specimen W is 12.5 mm, the thickness of the specimen is 0.2 mm, the radius of fillet R is 18 mm, the overall length of the test sample L is 276 mm, the length of reduced section A is 80 mm, the length of grip section is 60 mm, the diameter of the pin hole is 16 mm, and the edge distance from pins is 60 mm, the maximum distance P between both pins is 172 mm. The test sample size for each temperature is 6. Figure 7.83 shows the response of nonlinear stress and strain for KFC-H lead frame at 260°C with the loading rate 1 mm/min. The six test samples are quite consistent for the material tensile behavior at high temperature.

Figures 7.84–7.87 show the mechanical properties of the KFC-H lead frame as the function of the temperature. Basically, all the mechanical propeties decrease as the temperature increase. Notice that the interesting things are in Figs. 7.84 and 7.87. In Fig. 7.84, the maximum Young's modulus is not at room temperature but at the 75°C. While in Fig. 7.87, the enlongation keeps almost constant after 150°C.

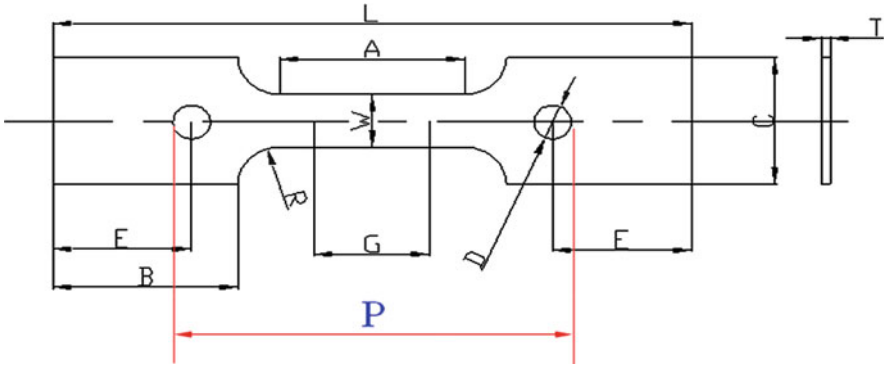


Fig. 7.82 Test specimen of lead frame based on ASTM E8M-04 standard

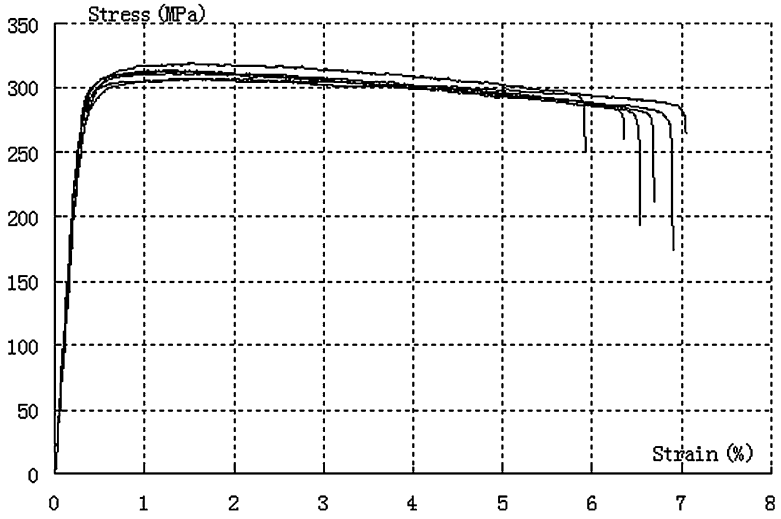


Fig. 7.83 The stress and strain relations at 260°C with the loading rate 1 mm/min for KFC-H material

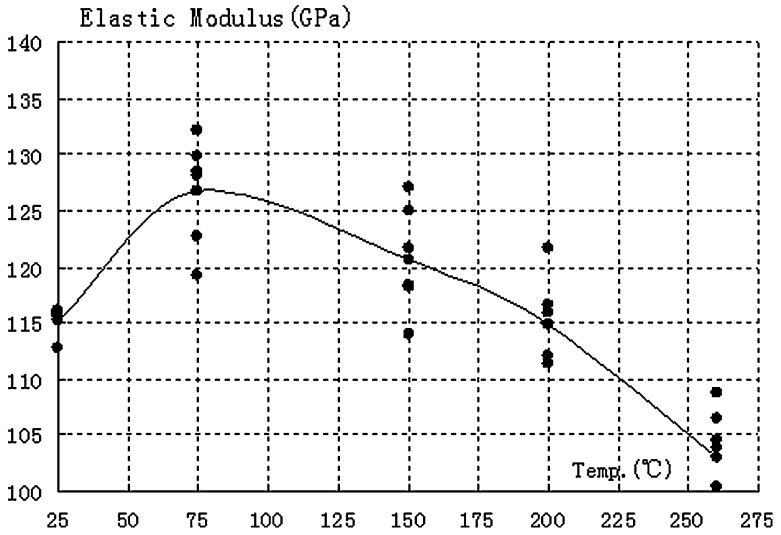


Fig. 7.84 The Young's modulus vs. the temperature with the loading rate 1 mm/min for KFC-H material

We expected the lead frame material becomes soft at higher temperature so that its material properties should beome more ductile. Therefore its enlongation value at high temperature should be larger than the low temperature. However, Fig. 7.87 does not show this trend as we expected.

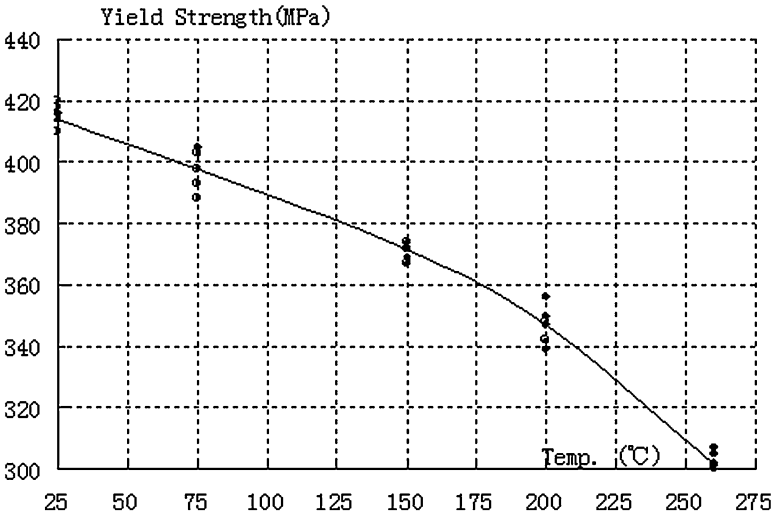


Fig. 7.85 The yield stress vs. the temperature with the loading rate 1 mm/min for KFC-H material

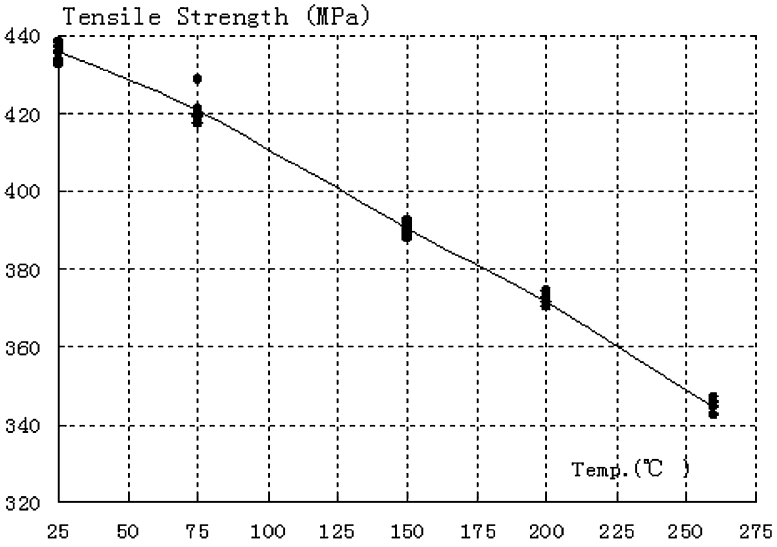


Fig. 7.86 The tensile strength vs. the temperature with the loading rate 1 mm/min for KFC-H material

Figures 7.88–7.91 list the mechanical properties of the 12SnOFC-H lead frame as the function of the temperature. All the mechanical propeties decrease as the temperature increase. However, Fig. 7.91 does not show this trend. After the 200°C,

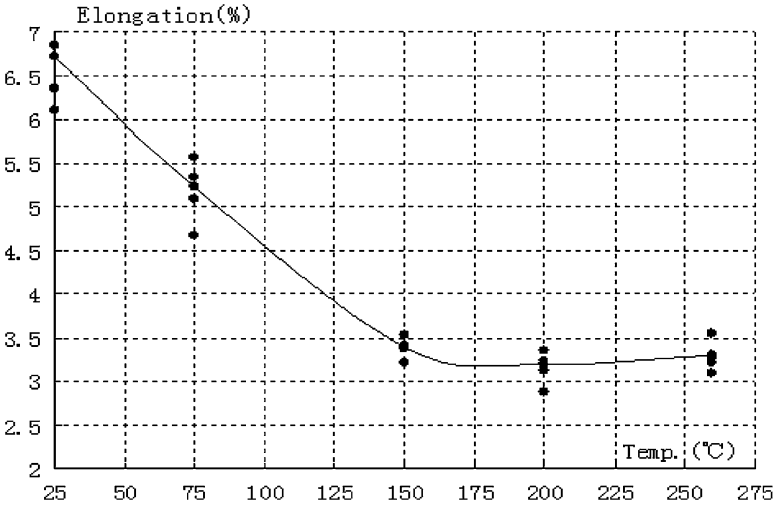


Fig. 7.87 The enlongation vs. the temperature with the loading rate 1 mm/min for KFC-H material

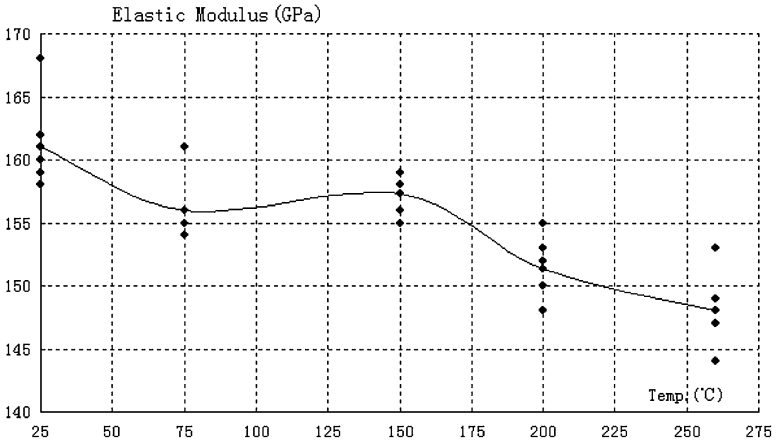


Fig. 7.88 The Young's modulus vs. the temperature with the loading rate 1 mm/min for 12SnOFC-H material

the enlongation increases as the temperature increases. Figures 7.92–7.95 list the mechanical properties of the C-194 lead frame as the function of the temperature, which have similar trends of 12SnOFC-H lead frame. After 175°C, the enlongation become larger. Compared to the three leadf rame materials, 12SnOFC-H has the

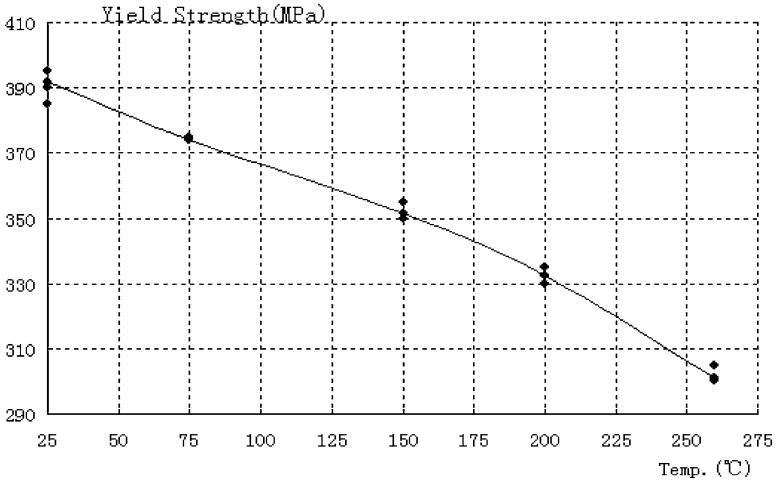


Fig. 7.89 The yield stress vs. the temperature with the loading rate 1 mm/min for 12SnOFC-H material

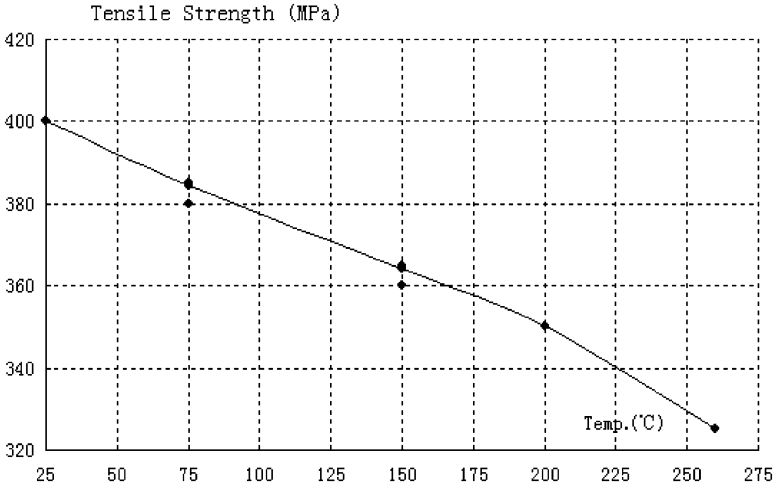


Fig. 7.90 The tensile strength vs. the temperature with the loading rate 1 mm/min for 12SnOFC-H material

higher Young's modulus but lower yield and tensile strengths. While KFC-H and C194 have lower Young's modulus but higher yield and tensile strengths. These different values might be due to the different surface platings and treatments.

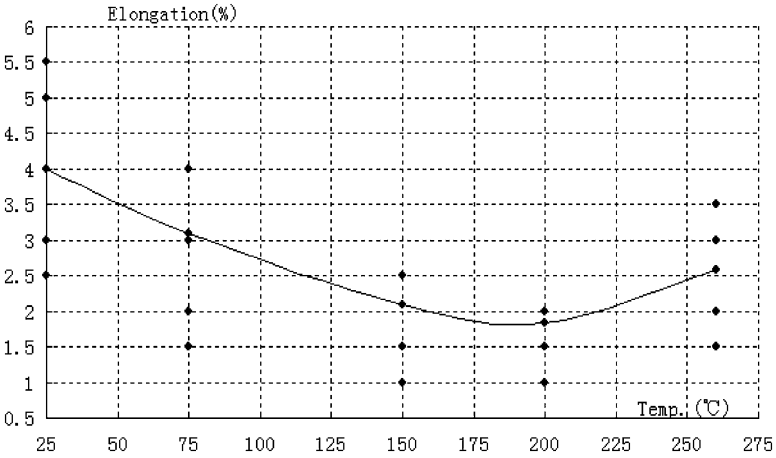


Fig. 7.91 The enlongation vs. the temperature with the loading rate 1 mm/min for 12SnOFC-H material

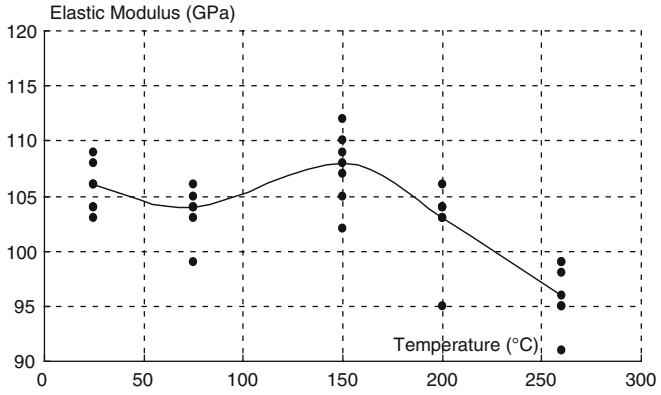


Fig. 7.92 The Young's modulus vs. the temperature with the loading rate 1 mm/min for C194 material

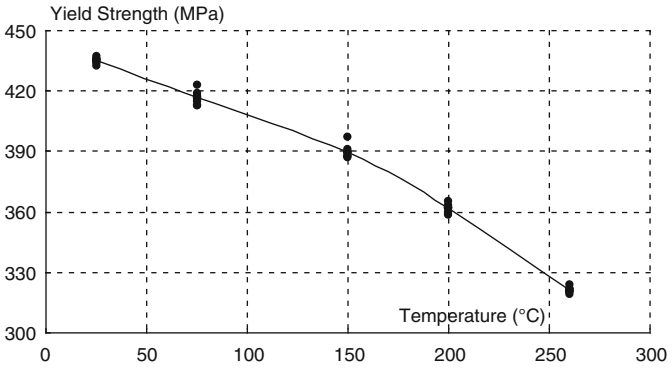


Fig. 7.93 The yield stress vs. the temperature with the loading rate 1 mm/min for C194 material

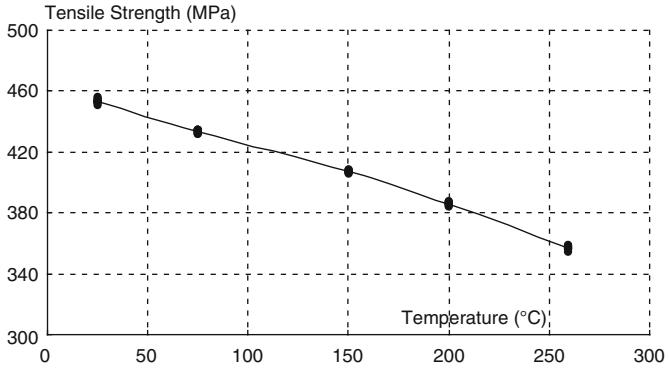


Fig. 7.94 The tensile strength vs. the temperature with the loading rate 1 mm/min for C194 material

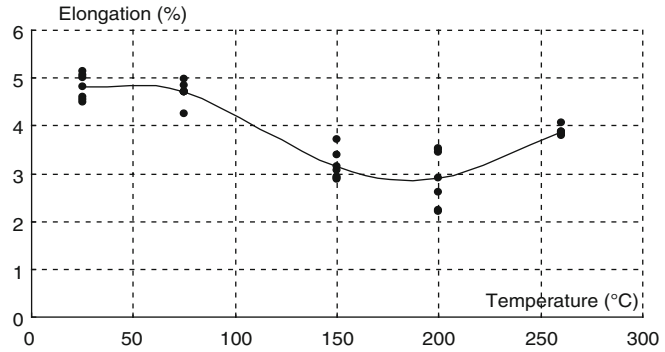


Fig. 7.95 The enlongation vs. the temperature with the loading rate 1 mm/min for C194 material

7.7 Summary

This chapter addresses the characteristics of the power packaging materials-related reliability problems in the power industry. It is unlike most of the other books on packaging materials in that it does not deal just with a distinct class of materials, or even a group of materials related by characteristics. Instead, it discusses a group of materials that are in many cases related not only because they are used together in power packages but also because they have the material mechanical behaviors under different loading environments such as temperatures and moisture. The first section gives the analysis of effect of polyimide coating on MOSFET die. Normally, the EMC in a power package includes silica fillers and resin. Often, the silica filler in the EMC material contacts the silicon die surface directly which results in

the damage of die surface in the loading environments. The polyimide can help to reduce the silicon surface damage. Next, the die attach characterization is introduced with consideration of the moisture. Different die attach materials are studied through material properties and stress analysis for the optimization of the die attach material selection. Then the characterization of EMC of power packaging is given in details, which describes the analytical methods for characterizing the change in equilibrium state, and explore the effect of the change in free volume space on the behavior of three mold compound systems. A drying procedure utilizing vacuum desiccation vs. baking method has been used for comparative purposes during subsequent characterization experiments. ANSYS modeling has been used to demonstrate the moisture diffusion rate through the mold compound of the package. Then, the mechanical and thermal behaviors of the ceramic/DBC substrate materials are studied and discussed. Compared to the materials and techniques used in lower power microelectronics, these substrates must carry higher currents and provide a higher voltage isolation (up to several thousand volts). They also must operate over a wide temperature range (up to 150 or 200°C). Then the characterization of solder material for power packaging is presented. The mechanical behaviors of typical Pb-free solder materials with some common Pb solder material are tested and discussed with viscoplastic material constitutive models. After that, the characterization of typical lead frame materials for power packaging is studied by the material tensile test finally.

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Chapter 8
Power Package Typical Assembly Process

Assembly manufacturing processes can be broken into front of line (FOL) and end of line (EOL) components, each having several process steps.

In FOL, typical processes include the wafer handling process, die pickup from tape that becomes more of a problem as die thinning becomes more extreme. FOL die attach processes can induce residual stresses due to process shrinkage and coefficient of thermal expansion (CTE) mismatch. Wire bonding processes can induce bond pad cratering or failure in the device under bond pad. In EOL, typical processes include molding process with curing stress and residual stress, molding ejection, and clamping process that can potentially cause cracking in molding compound, trim and form and singulation process that would induce the stress wave to crack the die or the epoxy molding compound (EMC). Before the actual assembly process, the virtual modeling and analysis is very important to find out the optimized solution and failure mode which can extremely benefit to enhance the quality and reliability of the power packaging, especially for new product development.

8.1 Wafer Handling Process

Wafer thinning for power application has become indispensable in semiconductor industry due to its many benefits such as improving device performance, reducing thermal resistance, increasing the device reliability, and making packages thinner [1, 2]. With the decrease of wafer thickness wafer warpage becomes larger. The excessive wafer warpage can result in handling issues (such as the taping and mounting) in production. A picture of actual power wafer warpage is shown in Fig. 8.1 and the wafer taping process is shown in Fig. 8.2 with the plastic tape and a soft roller.

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Fig. 8.1 Actual wafer warpage

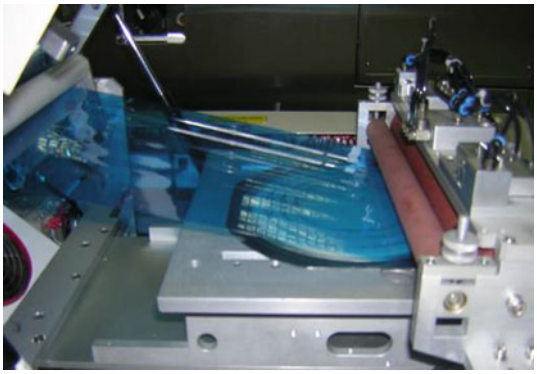


Fig. 8.2 Wafer taping process

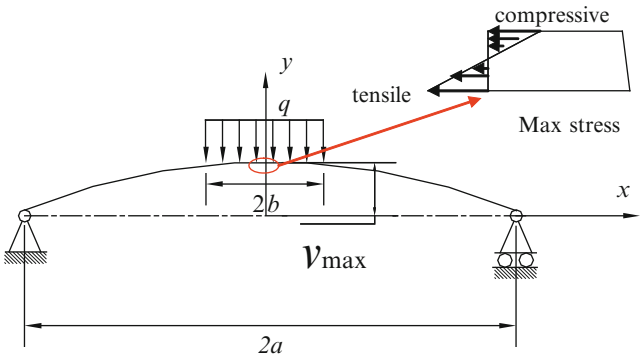


Fig. 8.3 Simplified model of thin wafer

In order to obtain the analytical solution of the wafer stress during wafer taping and mounting process, three assumptions are made: (1) After wafer grinding and before taping and mounting, the wafer has initial parabolic shape (see Fig. 8.3); (2) Only pure silicon material is considered; (3) Wafer edge is simply supported, after wafer taping and mounting process, wafer becomes flat. Its max stress location is shown in Fig. 8.3 as well.

According to assumption (1), the initial shape of wafer can be described as

$$f = \frac{a^2 - r^2}{a^2} v_{\max} \tag{8.1}$$

where a is the radius of wafer, r is radial distance within a, and $v_{\max}$ is the maximum deformation of the wafer at its center.

For uniformly distributed load within the range of radius b over the surface of the round wafer, its deformation/deflection can be formulated as the following based on the theory of plates and shells [3]

$$y = f - cq \tag{8.2}$$

where q is the uniform pressure load and the coefficient c has the following form,

$$C = \begin{cases} \dfrac{r^4}{64D} + \dfrac{b^2}{16D} \cdot \left[\dfrac{3+\upsilon}{1+\upsilon} \cdot a^2 - \dfrac{7+3\upsilon}{4(1+\upsilon)} \cdot b^2 - b^2 \ln \dfrac{a}{b} \right] \\ - \dfrac{b^2}{8D} \left[\ln \dfrac{a}{b} + \dfrac{1}{1+\upsilon} - \dfrac{1-\upsilon}{4(1+\upsilon)} \cdot \dfrac{b^2}{a^2} \right] \cdot r^2, \quad r \in [0, b] \\ \dfrac{b^2}{16D} \cdot \left[\dfrac{3+\upsilon}{1+\upsilon} \cdot a^2 - \dfrac{1-\upsilon}{2(1+\upsilon)} \cdot b^2 \right] + \dfrac{b^4}{16D} \cdot \ln \dfrac{r}{a} \\ + \dfrac{b^2}{8D} \left[\ln \dfrac{r}{a} - \dfrac{3+\upsilon}{2(1+\upsilon)} + \dfrac{1-\upsilon}{4(1+\upsilon)} \cdot \dfrac{b^2}{a^2} \right] \cdot r^2, \quad r \in [b, a] \end{cases}$$

where D is the flexural rigidity of the wafer plate, υ is the Poisson's ratio of the wafer material.

When $r \in [0, b]$, the stresses in the wafer plate can be derived as

$$\sigma_r = -\frac{3qb^2}{4t^3} z \left[(1-\upsilon) \frac{b^2}{a^2} - 4 - 4(1+\upsilon) \ln \frac{a}{b} + (3+\upsilon) \cdot \frac{r^2}{b^2} \right] \tag{8.3}$$

$$\sigma_\theta = -\frac{3qb^2}{4t^3} z \left[(1-\upsilon) \frac{b^2}{a^2} - 4 - 4(1+\upsilon) \ln \frac{a}{b} + (1+3\upsilon) \cdot \frac{r^2}{b^2} \right] \tag{8.4}$$

The maximum stress is at the wafer center where

$$\begin{aligned} \sigma_{\max} &= \sigma_r|_{r=0} = \sigma_\theta|_{r=0} \\ &= -\frac{3qb^2}{8t^2} \left[(1-\upsilon) \frac{b^2}{a^2} - 4 - 4(1+\upsilon) \ln \frac{a}{b} \right] \end{aligned} \tag{8.5}$$

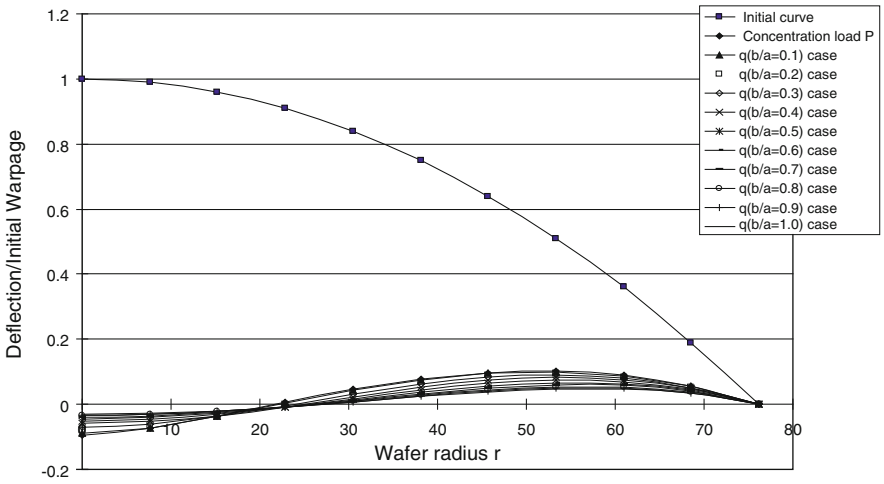


Fig. 8.4 Pressure loading q for making flat wafer with different ratio b/a

Table 8.1 Material parameters

Material	Elastic modulus (MPa)	Poisson's ratio
Silicon	160E3	0.23

If $v_{\max}$ and q are known, the deformation of the wafer can be obtained directly from (8.2). If the wafer becomes flat under an unknown pressure load q with a maximum warpage $v_{\max}$, q can be obtained by numerical method as follows

$$S = \sum_{i=1}^{n} y_i^2 = \sum_{i=1}^{n} (f_i - C_i P)^2 \tag{8.6}$$

$$\frac{\partial S}{\partial P} = 0 \Rightarrow q = \frac{\sum_{i=1}^{n} C_i f_i}{\sum_{i=1}^{n} C_i^2} \tag{8.7}$$

Then, the maximum stress in the wafer can be calculated from (8.5).

Figure 8.4 shows the pressure loads needed to make the approximated flat wafer with different ratio b/a based on (8.2)–(8.7)

The material property of wafer is listed in Table 8.1. For 6″ wafer, its radius is 152.4/2 mm. The thickness of wafer varies from 0.05 to 0.5 mm.

When b is equal to a, the wafer is subjected to uniformly distributed load over the entire surface. When b/a is equal to 0.1, it is assumed that the wafer is subjected to concentrated load of the value $\pi b^2 q$.

Table 8.2 Wafer thickness = 50 μm

b/*a*	0.1	0.6	1.0
q (MPa)	1.14E−4	4.19E−06	2.64E−06
Max stress (MPa)	15.8	8.40	7.58

Table 8.3 Wafer thickness = 100 μm

b/*a*	0.1	0.6	1.0
q (MPa)	9.09E−4	3.35E−05	2.11E−05
Max stress (MPa)	31.6	16.81	15.17

Table 8.4 Wafer thickness = 300 μm

b/*a*	0.1	0.6	1.0
q (MPa)	2.45E−2	9.04E−4	5.7E−4
Max stress (MPa)	94.8	50.42	45.5

Table 8.5 Die stress vs. tape and collet Young's modulus

Young's modulus		Tape stickiness			
Tape (MPa)	Collet (MPa)	fnfail (MPa)	fsfail (MPa)	Die thickness (μm)	Max first principal (tensile) stress S1 in die (MPa)
54	18.4	1.225	0.975	90	66
3,059	18.4	1.225	0.975	90	28
54	3,120	1.225	0.975	90	50.7
3,059	3,120	1.225	0.975	90	15.3

Assume that the maximum deflection at wafer center v_{max} is 3 mm. To make the wafer flat, the uniform pressure load q and maximum stress in the wafer are calculated and listed in Tables 8.2–8.4 for different wafer thickness and different ratio of b and a.

Wafer warpage is less than 3 mm in most handling cases. In actual assembly process, the plastic tape and soft roller will reduce contact stress on wafer (Fig. 8.2). The compressive strength of wafer is much higher than its tensile strength. From the results listed in Tables 8.2–8.5, the maximum stress in wafer is much lower than its tensile strength 170 MPa with weak fan-out area after backgrinding [4]. Our tensile test for the power wafer strength has shown that the minimum value of the wafer tensile stength is about 277.9 MPa (Fig. 8.5), which varies with the die thinning backgrinding rotation trace lines. This indicates that the thin wafer is quite safe during the wafer handling process.

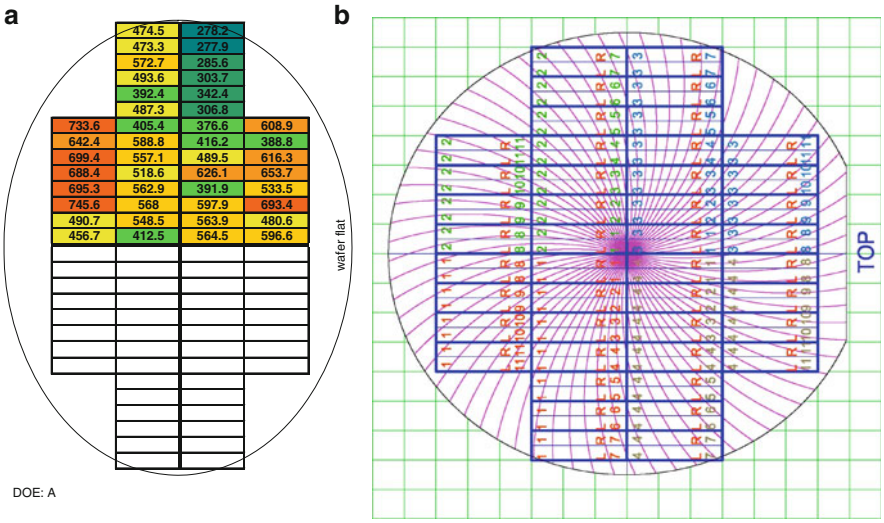


Fig. 8.5 The wafer tensile strength distribution. (**a**) The wafer tensile strength (MPa), (**b**) the cut chart of test samples in a wafer

8.2 Die Pickup

For the manufacturing process of package assembly, wafer is first adhered to tape and is sawn into the die as Fig. 8.6. After the wafer is sawed, die will be pick up and placed to the bond position on the lead frame [2].

As Fig. 8.7 shows that a vacuum pickup tool commonly known as a "collet" mounted on a bond head grabs the aligned die from the sawn wafer. The vacuum collet will push the die with a force to prevent air moving into the vacuum pipe. The die is then ejected from the wafer by one or more ejecton needles under the tape. The vacuum collet then pick the die up from the sawn wafer and attach it on the lead frame.

Figure 8.8 shows the structure of die holder. The ejection needles eject die throuth the holes in the die holder. The die holder is fixed during the whole die pickup process. The die holder fixes the tape through vacuum air in the holes.

Thin die (50–100 μm) is more and more widely used in small packages of high-power applications as it gives lower electrical resistance and better thermal dissipation, reduced space and weight. For thin wafer, die pickup operation is a critical aspect in the assembly manufacture process. The use of inappropriate tape stickiness, inappropriate ejection needles, and improper ejection parameter settings can cause die backside tool marks or microcracks that can eventually lead to die cracking. This analysis shows the impact of tape stickiness, die thickness on die stress during the die separation process from tape.

Figure 8.9 shows the model of the die pickup and the motion chart of the collet and ejector. Multiple 3D contact pairs are set up between collet and die, die and tape, tape and die holder, and tape and eject pins in the simulation.

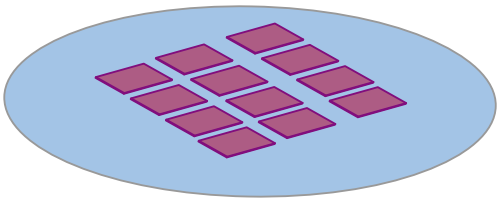


Fig. 8.6 Sawn wafer stuck to tape

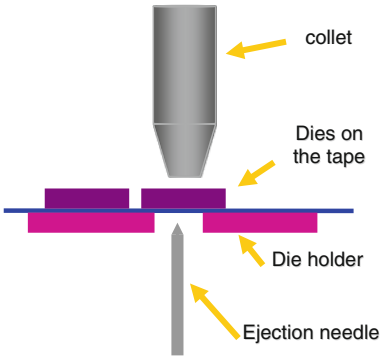


Fig. 8.7 Die pickup process



Fig. 8.8 Die holder with vacuum air holes

The collect contact force is a linear function of the ejection needle (ejector) motion height h, which can be discribed as $0.8 + kh$, where k is a contact coefficient. A debonding criterion for die surface and tape is developed to show the die separation process from tape. Transient dynamics modeling shows the stress distribution in the

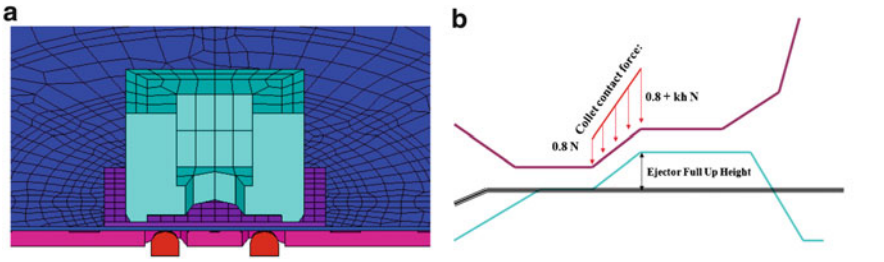


Fig. 8.9 Die pickup model and the motion chart. (**a**) The die pickup model, (**b**) motion chart of collet and ejection needle in die pack up

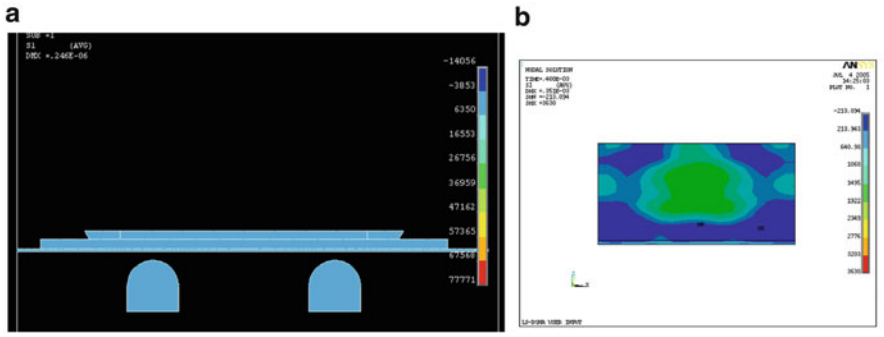


Fig. 8.10 Before the jection needle contact the tape. (**a**) Only collet contact the die, (**b**) die first principal stress S1 (Max: 4 MPa)

die so the process can be optimized and we can verify if the die strength is strong to withstand the dynamic pickup and ejectior stresses, especially for the thin power die. Figures 8.10–8.13 show the die pickup process and related die stress (1) Before the ejection needles contact the tape under the die; (2) The ejection needles hit the tape and the tape starts to separate from die under the vaccuum force of collet. At this time, the die stress reaches the higest; (3) The tape in the separating process in which the die stress decreases, and (4) The tape is totally separated from the die, and the die has been pick up by collet.

Figure 8.14 shows the tape's first principal stress and von Mises stress at phase 2. Figure 8.15 shows tape's first principal stress and von Mises stress at phase 3. The tape's stress will increase as the ejection needle ejects the die. The tape stress will act on the die edge first and move to the die areas that contacted by tips of ejection needles.

A parametric study about different collet and tape's Young's modulus, different die thickness and different tape stickiness are conducted and discussed. The results

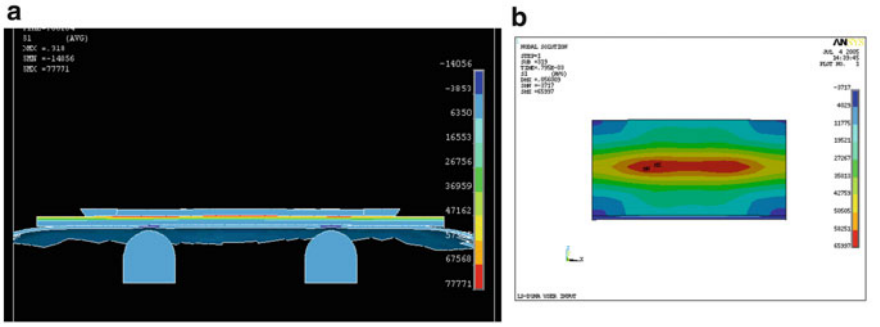


Fig. 8.11 The tape starts to separate from the die. (**a**) Pickup system stress, (**b**) die first principal stress S1 (Max: 66 MPa)

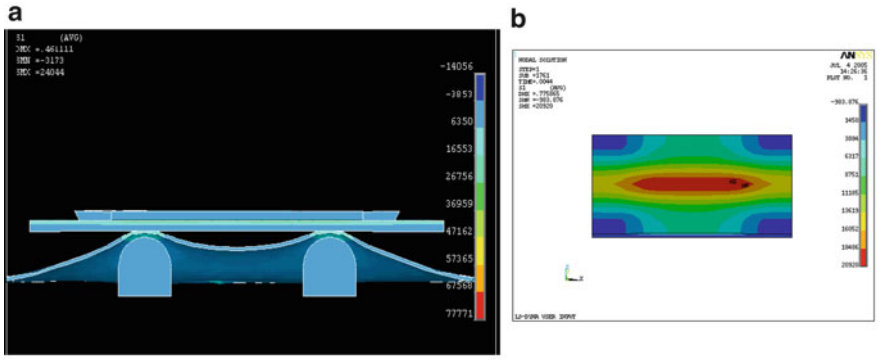


Fig. 8.12 The tape has been separated from most of the die area. (**a**) Tape is separating, (**b**) die first principal stress S1 (Max: 21 MPa)

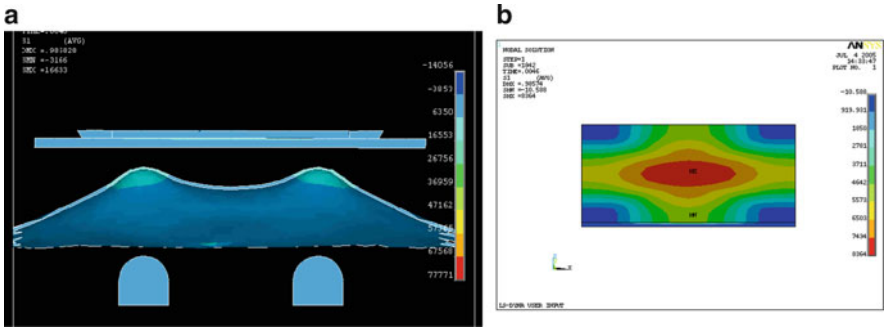


Fig. 8.13 Tape is totally separated and the die is picked up by collet. (**a**) Just separating tape from die, (**b**) die first principal stress S1 (Max: 8 MPa)

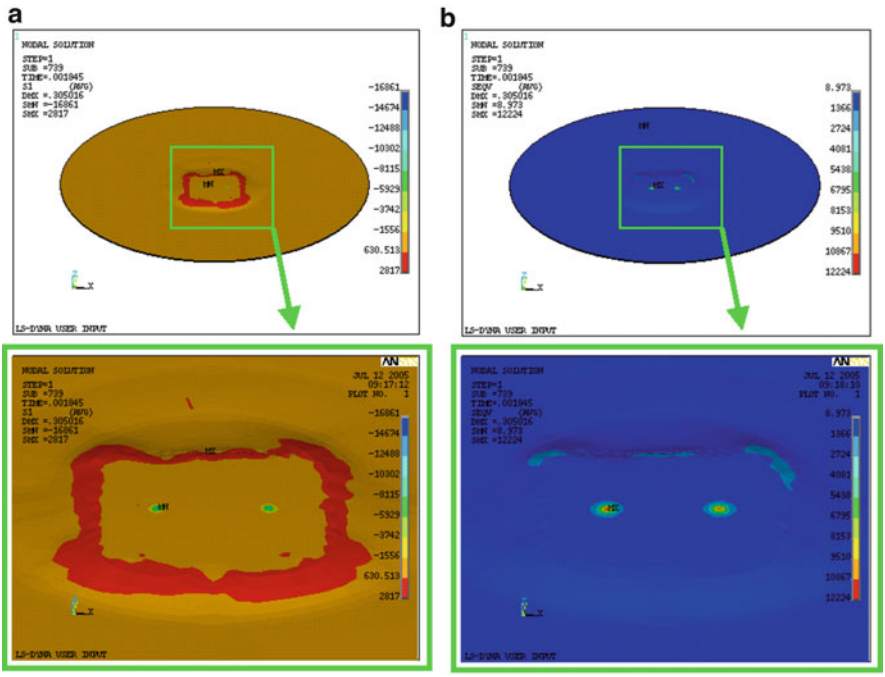


Fig. 8.14 Tape's stress when die begins to separate from the tape (location of max stress is die's edge). (**a**) Max first principal stress: 3 MPa, (**b**) Max von Mises stress: 12 MPa

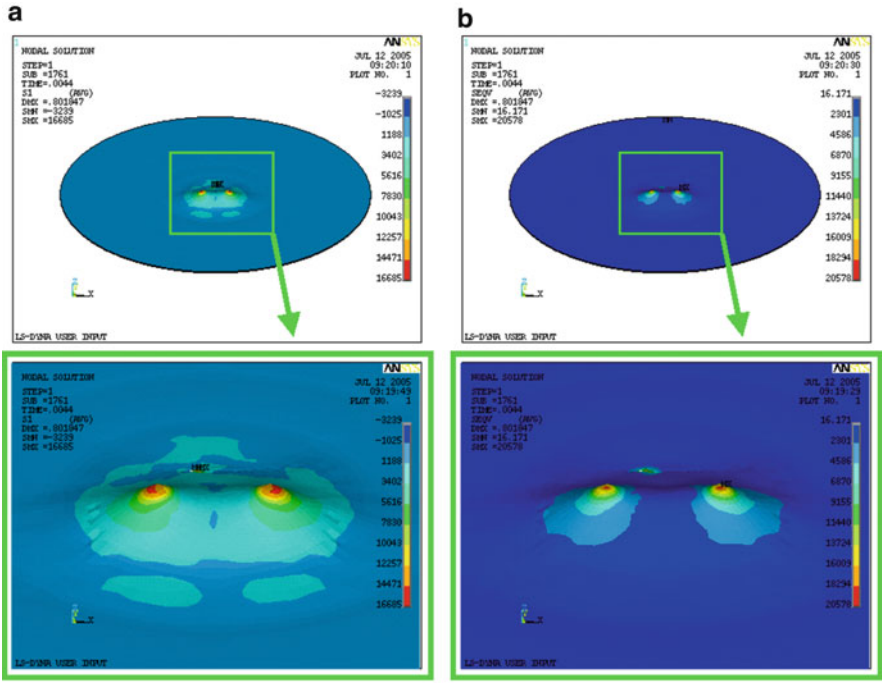


Fig. 8.15 Tape's stress when die is fully separated from the tape. (**a**) Max first principal stress: 17 MPa, (**b**) Max von Mises stress: 21 MPa

Table 8.6 Die stress vs. tape stickiness

Young's modulus		Tape stickiness			
Tape (MPa)	Collet (MPa)	fnfail (MPa)	fsfail (MPa)	Die thickness (μm)	Max first principal (tensile) stress S1 in die (MPa)
54	18.4	1.225	0.975	90	66
54	18.4	12.25	0.975	90	78.7
54	18.4	24.5	1.95	90	129.5

Table 8.7 Die stress vs. die thickness

Young's modulus		Tape stickiness			
Tape (MPa)	Collet (MPa)	fnfail (MPa)	fsfail (MPa)	Die thickness (μm)	Max first principal (tensile) stress S1 in die (MPa)
54	18.4	1.225	0.975	90	66
54	18.4	1.225	0.975	350	11.6
3,059	3,120	1.225	0.975	90	15.3
3,059	3,120	1.225	0.975	350	5.2

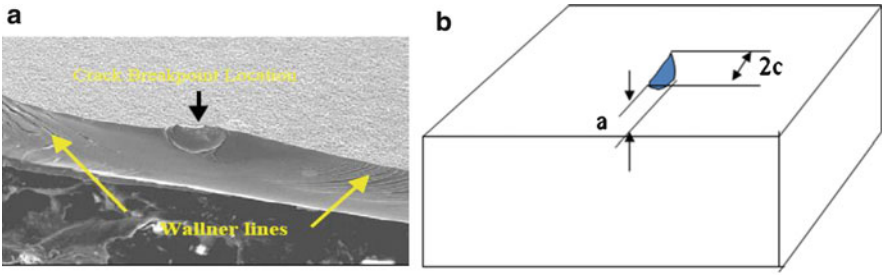


Fig. 8.16 The initial crack in die pickup process. (**a**) A initial tiny crack by ejection pin, (**b**) the crack model

of impact of collet and tape's Young's modulus, tape stickiness, and die thickness are shown in Tables 8.5 and 8.6.

Table 8.5 shows that the Young's moduli of tape and collet are much lower than silicon die's modulus. The higher Young's moduli of the tape and collet can reduce the die's first principal tensile stress.

Table 8.6 shows that die's first principal (tensile) stress S1 increases as the tape stickiness increases. In Table 8.6, as the tape's normal stickiness increases to 24.5 MPa and shear stickiness increase to 1.95 MPa, die will not be picked-up from the tape. Then, the tensile stress S1 on die is very large because the tape is firmly stuck on the die, particularly this will be harmful for the thin or ultrathin power die.

Table 8.7 shows the die first principal (tensile) stress S1 with different die thicknesses. Thinner die (90 μm thickness) has shown larger tensile stress. When the thickness of IGBT die is below 50 μm, the die would be possibly cracked. Figure 8.16 shows the possible die crack which was initially induced by the

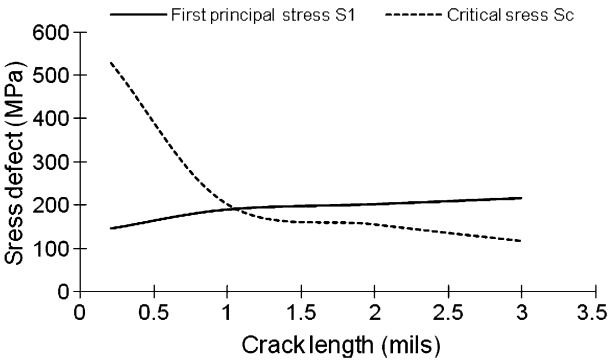


Fig. 8.17 The comparison of silicon die critical stress (*dot line*) and the die active stress (first principal stress with *solid line*)

ejection needle in the die pickup process. Figure 8.17 gives the comparison of silicon critical stress (dot line) and its active stress (first principal stress with solid line). From this Fig. 8.17, it can be seen that if the active stress is below the critical stress, the crack will not develop. In the case of Fig. 8.17, when the initial crack length is less than 1 mil, the die crack will not propagate. Therefore, for thinner die, it is important to design the ejection pin needle geometry or select the reasonable tape so that the ejection needle will not damage the die surface in pickup process.

8.3 Die Attach

There are two type of die attach processes, one is the regular die attach process in which the back side of die faces the DAP and another one is the flip chip die attach process in which the die active surface faces the DAP.

A typical soft solder die attach process is shown in Fig. 8.18.

As the vacuum collect head picks up the die with metallization from the wafer tape. A lead frame is held on the surface of heater block. The soft solder wire is then placed on the lead frame. The temperature of the heater block ramps up to the melting temperature of solder wire that makes the wire fuse. Finally, the die pick collet moves the die to the melt solder in the lead frame and as soon as the solder cools down, a solid connection is established. A controlled temperature profile is required to define the liquidus–solidus transition. The die attach process is a very nonlinear process that needs to develop a strong finite element method to get the converged solution.

Figure 8.19 shows a typical flip chip die attach process. A lot of effort has been made to minimize and optimize manufacturing steps for flip chip die attach processing with low cost. However, the quality and reliability have to be assured. Particularly, the assembly process induced stresses have to be reasonablely modeled.

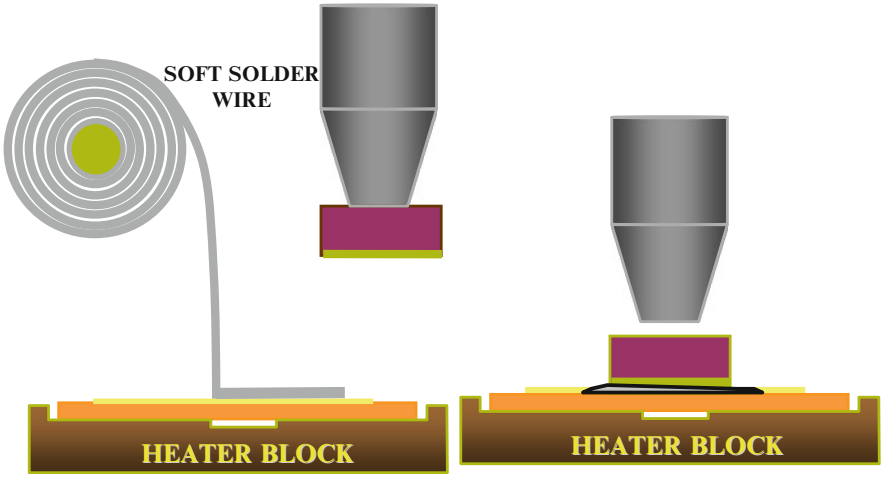


Fig. 8.18 Eutectic solder die attach process

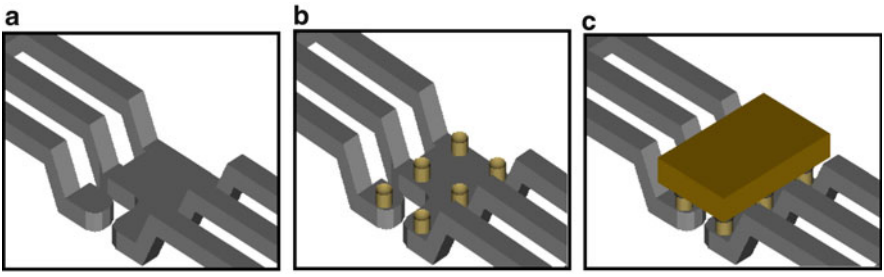


Fig. 8.19 Flip chip die attach processes. (**a**) Place lead frame, (**b**) place solder paste, (**c**) flip chip die attach and reflow

Many researchers have investigated process induced stress analysis for various plastic IC packages [5, 6]. Wang et al. [7] developed the process induced stresses of a flip chip packaging by sequential processing technique, which mainly targeted two stress free temperatures for bonding the silicon chip onto the substrate at 180°C and dispensing underfill material at 135°C. Mannan et al. [8] simulate the solder paste reflow coalescence for a flip chip assembly by CFD, but without the results of stress induced after reflow.

Typical assembly flip chip attach process includes place or screen print solder paste on lead frame, flip chip attach and reflows at 260 or 285°C. The reflow process is a very nonlinear process both in material and geometry. As it is well known, simulation results are influenced by the material models [9, 10], and the solution algorithm strategies [11]. From a material viewpoint, both solder ball and paste are characterized by deformation behavior which is dependent on temperature and time.

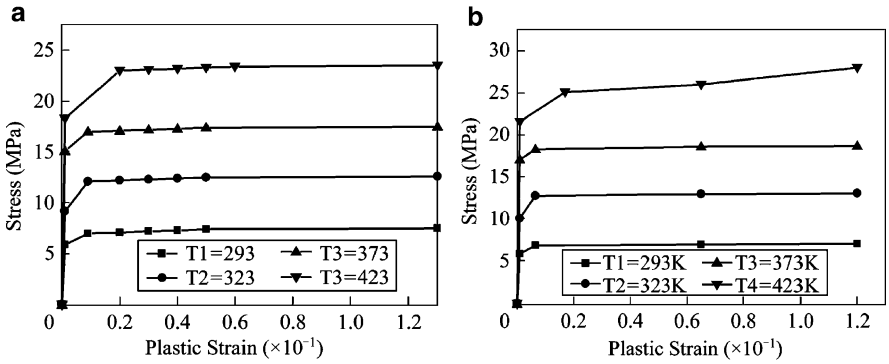


Fig. 8.20 Elastic plastic stress–strain relations for solder joint. (**a**) Solder ball, (**b**) solder paste

A correct solder joint material model is necessary to get reasonable results. On the other hand, a highly nonlinear system equations results, which must be solved by a highly efficient solution algorithm. Normally, the algorithm based on Newton's method with a tangent operator converges quickly if a trial solution inside the radius of convergence is obtainable and used as an initial guess [12].

8.3.1 Material Constitutive Relations

There are a lot of research efforts for the plastic and viscoplastic constitutive models (see [12] for a general relation and Qian's formulations [13] in semiconductor solder alloy application). Typically, an simple effective constitutive model, which shows good fitting capability [14] is a time-independent multilinear elastic plastic model which includes a time dependent creep model for solder joint's behavior. Anand's evolution model is also a useful model to predict viscoplastic property of hot metal material [15], which may reflect both transient and steady creep behavior. In this chapter, we assume that the die, UBM, passivation and Pad with lead frame are all linear elastic, the solder ball and paste are nonlinear. Three material models (multilinear elastic plastic temperature dependent model, Anand viscoplastic model and plastic with creep model) for both solder ball and paste will be used and discussed in the simulation framework. The multilinear elastic plastic temperature dependent relations [13] are presented in Fig. 8.20a for solder ball and Fig. 8.20b for solder paste. The Anand model [15] includes a sinh function model and a evolution equation:

$$\frac{\mathrm{d}\varepsilon_{\mathrm{vp}}}{\mathrm{d}t} = A[\sinh(\xi\sigma/s)]^{1/m}\exp\left(\frac{-Q}{kT}\right) \tag{8.8}$$

or, it can be written as

$$f_{\mathrm{ANAND}} = \bar{\sigma} = \frac{s}{\xi}\sinh^{-1}\left(\frac{\dot{\varepsilon}_{\mathrm{vp}}}{A}\exp\left(\frac{Q}{kT}\right)\right)^{m} \tag{8.9}$$

where the evolution equation,

$$\frac{\mathrm{d}s}{\mathrm{d}t} = \left\{h_0\left(\left|1-\frac{s}{s^*}\right|\right)\right\}^{a}\mathrm{sign}\left(1-\frac{s}{s^*}\right)\frac{\mathrm{d}\varepsilon_{\mathrm{vp}}}{\mathrm{d}t} \tag{8.10a}$$

and,

$$s^* = \hat{s}\left[\frac{\mathrm{d}\varepsilon_{\mathrm{vp}}/\mathrm{d}t}{A}\exp\left(\frac{Q}{kT}\right)\right]^{n} \tag{8.10b}$$

where the constants $Q/k = 11{,}935$ (K) for ball and 9,400 (K) for paste, which stands for the activation energy/Boltzmann's constant; $A = 3.785\text{e}7$ (1/s) for ball and 4.0e6 (1/s) for paste, which is a preexponential factor; $\xi = 5.91$ for ball and 1.5 for paste, means a multiplier of stress; $m = 0.143$ for ball and 0.3 for paste, which is the strain rate sensitivity index of stress; h_0 (unit: MPa) is the hardening/softening constant, its number is 1,579 MPa for both ball and paste; $\hat{s} = 13.79$ (MPa) is the coefficient for deformation resistance saturation value for both ball and paste; $n = 0.07$ is the strain rate sensitivity index of deformation resistance; a is the strain rate sensitivity of hardening/softening, $a = 1.3$ for both ball and paste.

For the elastic plastic and creep model, the elastic plastic relation is selected as in Fig. 8.20, the creep model is chosen to be a Norton's law as following

$$\dot{\varepsilon}_{\mathrm{creep}} = c\exp\left(\frac{-Q}{kT}\right)\sigma^{n} \tag{8.11}$$

The parameter c (1/s MPa) for solder ball is 1.936 and for paste is 100.6; n for solder ball is 11.03 and for for paste at 25°C: 4.434 and 285°C: 1.262; Q/k (K) is 1.1935e4 for solder ball and 8.45e3 for paste.

The CTE of solder ball is presented as in [13]. The Poisson ratios are selected as 0.4 for solder alloy and 0.35 for paste. The silicon is assumed to be linear elasticity and its Young's modulus and Poisson ratio are 169.5 and 0.278 GPa, respectively. The CTE of silion chip is 3.2 ppm/°C. The passivation is composed of elastic material, the Young's modulus is 4.2 GPa, Poisson's ratio is 0.34. CTE is 3.59 ppm/°C. The Young's modulus of UBM is 186.5 GPa, Poisson's ratio is 0.3, CTE is 12.4 ppm/°C. Lead frame is copper based material, its Young's modulus is 120.5 GPa, Poisson's ratio is selected as 0.3, CTE is 18.3 ppm/°C.

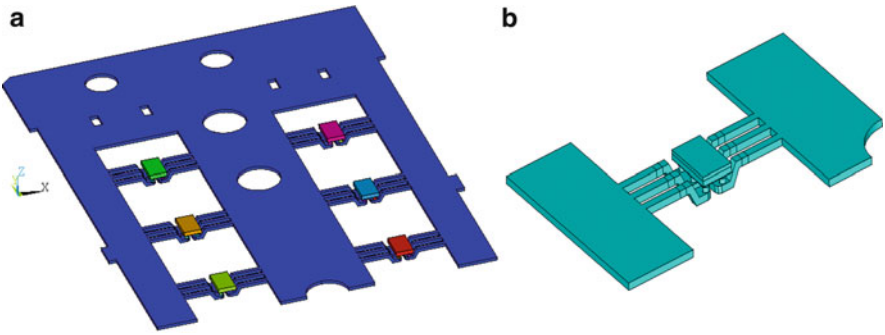


Fig. 8.21 A typical lead frame and flip chip attach model. (**a**) Strip lead frame with the flip chips, (**b**) a single flip chip die attach model

8.3.2 Die Attach Model and Reflow Profile

A typical flip chip attach on pad and lead frame is shown in Fig. 8.21, only one package with related uncut lead frame model is taken into consideration for analysis.

In the die attach processing; the package components include die, passivation, UBM, Solder Ball and paste, and lead frame. The die attach process is a very nonlinear process; its reflow curve is applied as in Fig. 8.22, the melting temperature for solder ball is 312°C, and the solder paste is 285°C. In order to simplify the problem, we assume the following: (1) Compression flow placement is perfectly done by the machine, no chip floating before reflow process; (2) The initial stresses induced before reflow temperature are too small to be considered; (3) The stress in solder paste is free at reflow temp 285°C (it almost fully melts at this temp), and it starts to be generated from 285°C cooling down. Based on these assumptions, the die attach simulation is presented through 3D model (see Fig. 8.23) [16].

Loading for Flip chip attach process: during the flip chip processing, the thermal loading is based on the reflow profile. The reflow profile has four phases: phase 1 (C1) is the preheating and ramp up with about rate 2.62°C/s for about 47 s; phase 2 (C2) is ramp up to 285°C with 2.8°C/s for about 30 s; phase 3 (C3) dwells 285°C for 13 s, solder paste melts at this phase; phase 4 (C4) cools down to room temp 25°C with a rate of 11.36°C/s (see Fig. 8.22).

8.3.3 FEA Simulation Result of Flip Chip Attach

All the simulations are carried out by finite element software ANSYS® to simulate the stress distribution during the flip chip attach of the power package. The simulation results are shown in Figs. 8.24–8.28.

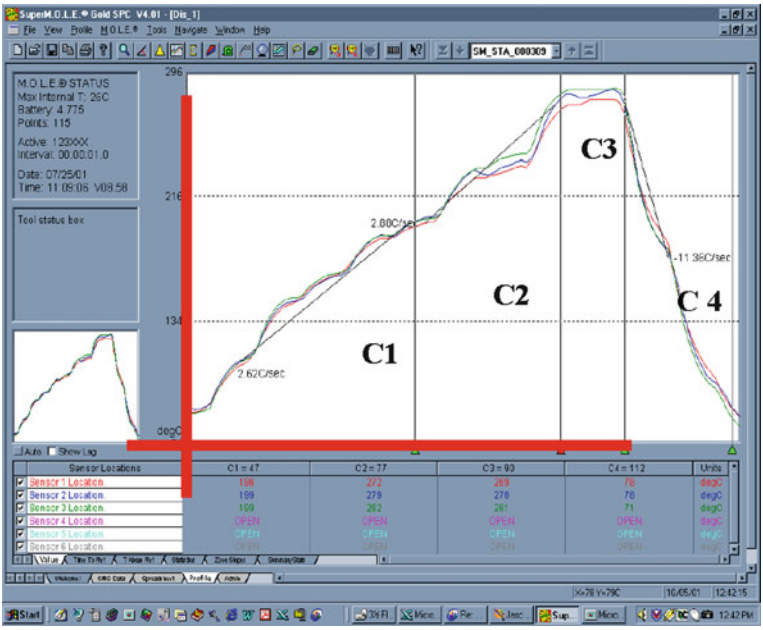


Fig. 8.22 The reflow profile of flip chip attach process

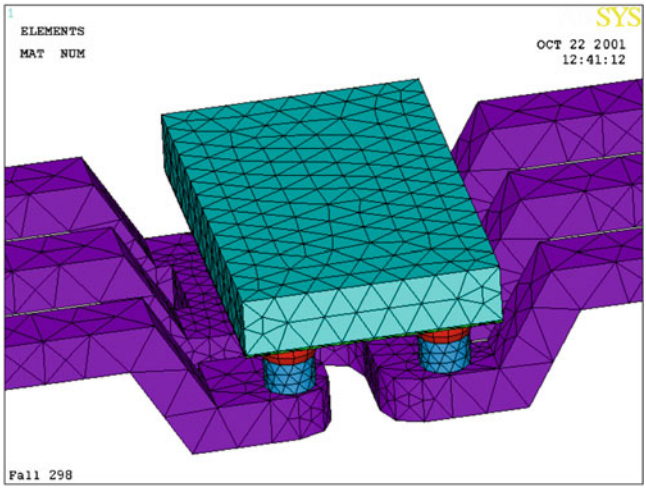


Fig. 8.23 3D model of the flip chip attach processing

Figure 8.24 shows the motion of the gate lead after reflow due to the die attach solder flow property in reflow. The position of gate lead is clearly moved a distance as compared to its initial location (dot line). The motion of the gate lead will result in the quality issue such as the gate lead lift or break.

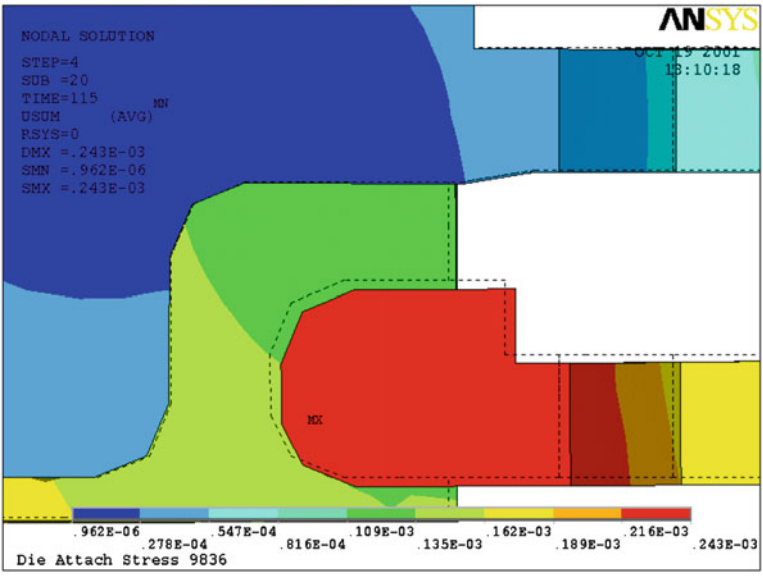


Fig. 8.24 The motion of the gate lead after reflow

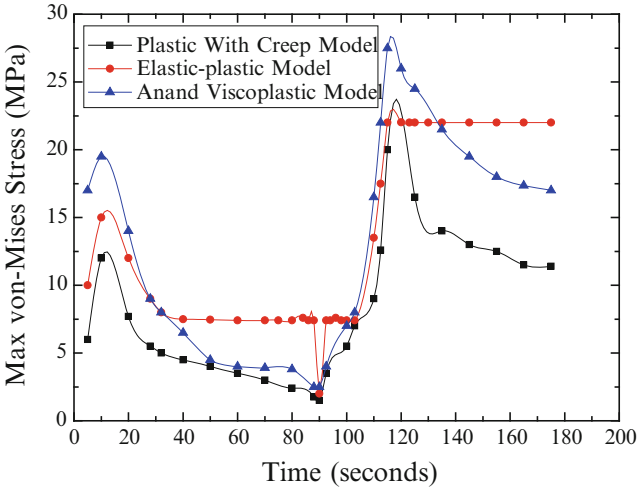


Fig. 8.25 Maximum von Mises stresses in solder ball with three material models

Figure 8.25 shows the history of maximum von Mises stress in solder ball vs. time in three material models (elastic plastic, Anand viscoplastic, and elastic plastic with creep models). From the figure it may be seen that the max von Mises stresses in three cases increase when the temp ramps up; the stress number is slightly higher than the yield strength at about 100°C. After that when the temp continues to ramp the stress decreases; this is because the yield stress of solder material becomes lower as the temperature increases.

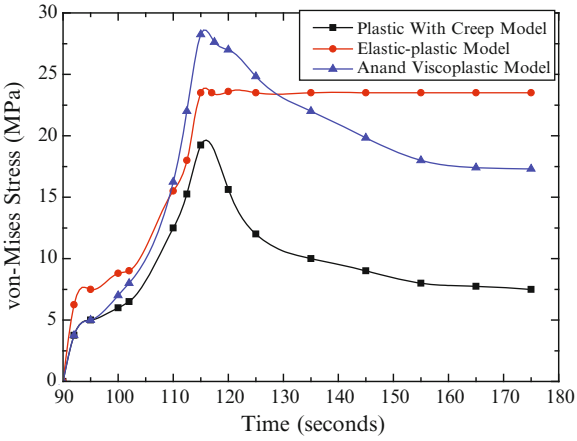


Fig. 8.26 Maximum von Mises stresses in paste with three material models

The stress in solder material will not be higher than its yield strength becase of the plastic flow properties. At the end of dwelling reflow temp 285°C, all the stresses reaches their lowest number. After the reflow temperature 285°C, the temp cools down and all the stresses increase and reach the highest number at the end of room temperature. In the pure elastic plastic and Anand viscoplastic models, the stress reaches the yield stress while the plastic and creep model does not. It seems that the stress number of Anand model is the highest at the end of reflow. The results further show that after end of reflow, if the package dwells at room temperature for 60 s, the stress is released for both Anand viscoplastic and elasticplastic with creep model.

Figure 8.26 shows the history of maximum von Mises stress in solder paste vs. time in three material models, the time range is from the melting point to the room temperature point, and then dwell 60 s. Basically during room temperature, the stress is very small due to the attach placement. When the temperature reaches reflow temperture 285°C, which is the melting point of the paste, the stress is free. Therefore, for the paste, we use two models, one is the element birth and death model, in which the paste elements are set to be dead from room temperature to 285°C, active right after 285°C and starting to cool point. This method makes it difficult to get a converged solution. Another method is the continuum model, which assumes the paste elements are active during the whole reflow process. Figure 8.27 gives the comparison of elastic plastic von Mises stresses with both element birth-death model and the continuum model. The results show that the maximum von Mises stress in continuum model have the similar behavior as in solder ball before melting point, while from melting point cooling down to room temperature, the stresses obtained by element birth and death model agree with the results of continuum model. The prediction of the continuum model is slightly higher than that of element birth and death model. Again, the Anand material model predicts a higher stress number (Fig. 8.26) at the end of reflow.

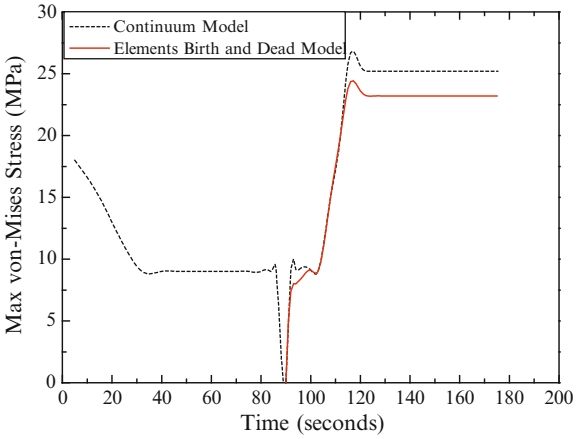


Fig. 8.27 Comparsion of elastic plastic von Mises stresses in paste with element birth-dead model and continuum model

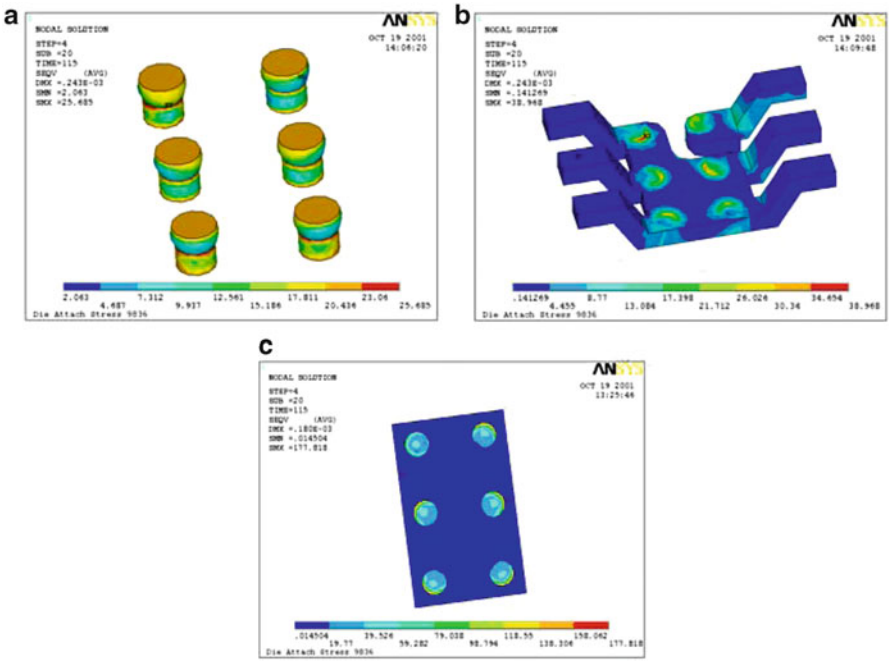


Fig. 8.28 von Mises stress in solder joint, lead frame, and UBM and passivation. (**a**) Solder joint, (**b**) lead frame, (**c**) UBM/passivation

Figure 8.28 shows the von Mises stresses distribution in the solder joint, lead frame, UBM, and passivation after reflow. The max stress in solder joint appeared in gate solder joint, which could be induced by the motion of the gate lead in reflow.

The stress number of the UBM edge in connection with solder ball is very high, which could be the potential factor for delamination.

8.4 Wire Bonding

Wire bonding is a critical process stage in the assembly process for the connection between the semiconductor chip and the external world [17]. By this stage, most of the device's costs have been absorbed, especially for the high density wire bonding and the bond pad over active (BPOA) design. To reduce the cost and obtain the optimized wire bonding solution, modeling of the wire bonding process has been used to help to determine the optimized wire bonding parameters and to help identify the potential failure mechanisms. It is known that the common failure modes of wire bonding are bond pad cratering, peeling and cracking below the bond pad. There are five major factors that relate to the failure modes and affect the quality of bonding process and bond pad devices [17, 18]: bonding force or deformation, ultrasonic amplitude and frequency, friction and intermetallic compounds between FAB and bond pad, substrate temperature, and time duration. In this chapter, the bonding capillary is considered as a rigid body due to high hardness. This results in a rigid and elastic plastic contact pair between the capillary and the FAB, while the contact surfaces between the FAB and the bond pad are a nonlinear contact pair with consideration of the dynamic friction. The Pierce strain rate dependent model is introduced to model the impact stain hardening effect.

Two topics of interest are presented in this section: (1) Ball wire bonding process with different parameters of capillary profile, FAB diameters, bonding temperature, and bond wire material properties; (2) Optimization of Al wire wedge bonding process.

8.4.1 Assumption, Material Properties, and Method of Analysis

When ultrasonic energy is applied to the FAB by capillary, it causes a reduction in yield strength and increases the mobility and density of dislocations after some dwell time. The strain rate is in the "slip by dislocation shifting region," as the deformation occurs, the material strain hardens. When the hardening material transmits energy to the ball–pad interface, slip planes shift at the interface, opening up new metal surfaces. Contact diffusion bonding (with intermetallic effects at certain temperature rises by dynamic friction), enhanced by ultrasonics, occurs at the newly exposed metal surfaces; as the frequency increases, after some point (e.g., 120 kHz or above), the FAB material may not be significantly softened at the beginning, while the strain rate is in the "simultaneous several lattice slip" region, the material behaves as a hard material transmitting energy to the ball–pad interface [18]. Ikeda et al. indicated [19] that a gold ball is impacted by a capillary at the

Table 8.8 Materials parameters

Material	Modulus (GPa)	CTE (ppm/°C)	Poisson ratio	Yield stress (GPa)
Silicon	169.5	3.2	0.23	
ILD	70.0	4	0.25	
TiW	117.0	10.2	0.25	
Al (Cu)	70.0	10	0.35	0.2 (25°C) 0.05 (450°C)
Au (FAB)	60.0	14	0.44	0.0327 (200°C)
W (plugs)	409.6	4.5	0.28	

loading speed of 0.98 N/s, which may result in the strain rate of the gold ball more than 1,000 1/s locally. Based on the Hopkinson impact bar tests by Ikeda, the yield stress of FAB with strain rate hardening may be approximated by:

$$\sigma_s = \sigma_0 + H'\dot{\varepsilon}^{pl} \tag{8.12}$$

where $\sigma_0 = 0.0327$ GPa, $H' = 0.00057$ GPa s.

Equation (8.12) can be further expressed as the rate dependent Peirce Model:

$$\sigma_s = \left[1 + \frac{\dot{\varepsilon}^{pl}}{\gamma}\right]^m \sigma_0 \tag{8.13}$$

where $m = 1$ and $\gamma = 561.4$ (1/s).

The material parameters are listed in Table 8.8; FAB, bond pad, and metal layers are nonlinear (bilinear) materials and all the rest of the materials are considered to be linear elastic.

A general finite element code, ANSYS®, is used in the modeling. Since the bonder capillary is considered as a rigid body due to high hardness, this leads to the rigid and elastic plastic contact pair between capillary and FAB. While the contact surfaces between FAB and bond pad are a nonlinear contact pair with consideration of the dynamic friction.

8.4.2 Ball Wire Bonding Process with Different Parameters

A conceptual 2D model is shown in Fig. 8.29, which is a cut from a typical die with three layer metallization and three dielectric (ILD) layers above the silicon. The typical diameter of a FAB is 70 μm, and the bond pad length is 90 μm. The bottom of silicon is fixed and two sides are constrained in horizontal direction. Figure 8.30 gives the capillary geometry of the wire bonding system. The capillary moves down a certain height (bonding height) to press the FAB with a high speed and different frequency. Figure 8.31 shows the initial FAB geometry before wire bonding and the final bond after wire bonding. Figure 8.32 shows an example of modeling result of a ball wire bonding process and the final deformed bond. From the Fig. 8.32, it can be seen that the dynamic stress has transferred to the device

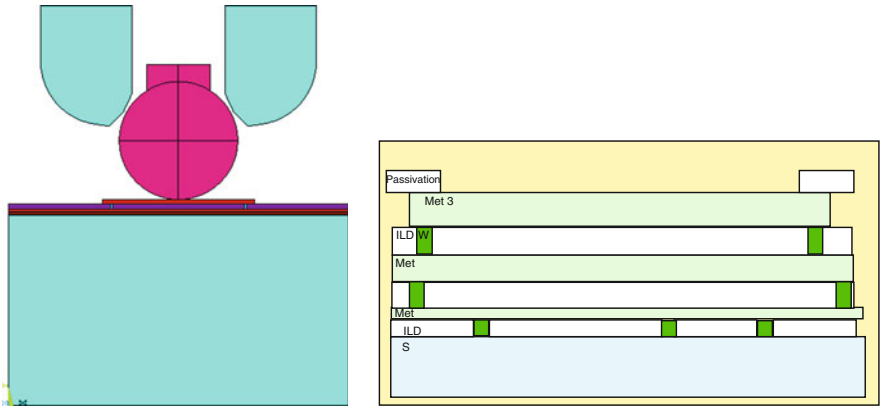


Fig. 8.29 Conceptual bond pad system

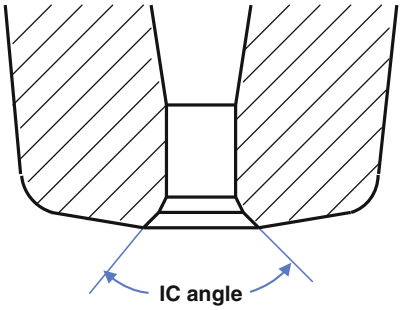


Fig. 8.30 Wire bonding capillary

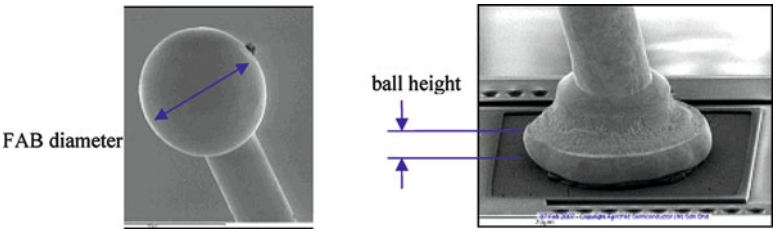


Fig. 8.31 FAB before wire bonding and after wire bonding

under the bond pad, which will potentially induce the cratering and crack for the ILD and device. Ball wire bonding parameters optimization and analysis are critical for the wire bonding process [20, 21]; this section presents the analysis of the capillary and ball wire bonding process parameter simulation with the bond wire pull test.

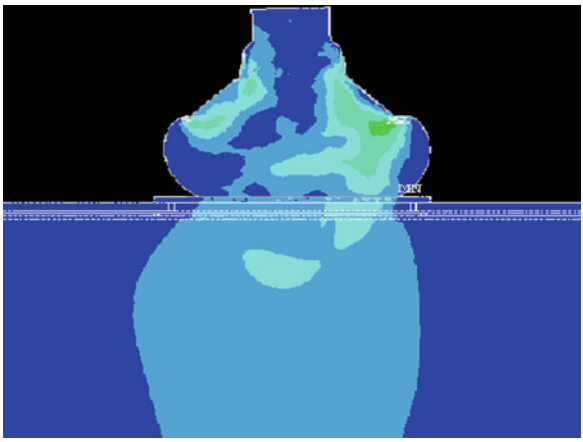


Fig. 8.32 The final deformed bond of wire bonding modeling

Table 8.9 Max stress on ILD layers

IC angle (degree)	S1 of ILD (MPa)	S3 of ILD (MPa)
70	63	282.3
90	61.4	283.5
120	61	305.9

Table 8.10 Max compressive stress at the ball–pad interface

IC angle (degree)	Sy of ball–pad interface (MPa)	Shear stress of ball–pad interface (MPa)
70	312.8	88.6
90	307.9	89.1
120	304.2	91.5

8.4.2.1 Impact of Capillary Profile

The results of impact of different capillary inside chamfer angles are shown in Tables 8.9 and 8.10. These results are obtained with a FAB diameter 2.8 mil and a bonding heater temperature 205°C.

Table 8.9 shows that the max first principal stress S1 (tensile) of ILD layer decreases as the capillary IC angle increases. However, its max third principal stress S3 (compressive) increases as the capillary IC angle increases. Since ILD has much larger compressive strength than its tensile strength, therefore, the larger IC angle benefits to reduce the tensile stress in ILD. Table 8.10 shows that the max Y component (vertical compressive) stress at the interface of ball and bond pad decreases as the capillary IC angle increases. But the max shear stress increases as the capillary IC angle increases.

Table 8.11 Max stress on ILD layers in different FAB diameters with the same bonding ball height

FAB diameter (mil)	S1 of ILD (MPa)	S3 of ILD (MPa)
2.8	61.4	283.5
2.9	68.1	320.2
3.0	141.6	403

Table 8.12 Max stress at the ball–pad interface in different FAB diameters with the same bonding ball height

FAB diameter (mil)	Sy of ball–pad interface (MPa)	Shear stress of ball–pad interface (MPa)
2.8	307.9	89.1
2.9	371.9	100.1
3.0	390.3	124.7

Table 8.13 Max stress on ILD layers in different FAB diameters with the same bonding force

FAB diameter (mil)	S1 of ILD (MPa)	S3 of ILD (MPa)
2.8	61.4	283.5
2.9	62.7	276.8
3.0	58.3	274.7

8.4.2.2 Effect of FAB Diameter

The effect of FAB diameter is investigated with either under the same squashed ball height or under the same bonding force. The capillary inside chamfer angle is 90° and the bonding temperature is 205°.

1. Impact of FAB diameter with the same squashed ball height
   Tables 8.11 and 8.12 give the stress comparison of the bond pad system and below structure with the same squashed ball height. Table 8.11 shows that the ILD layer's max first principal stress S1 and max third principal stress S3 increase as FAB diameter increases. Table 8.12 shows that both the max Y component vertical compressive stress and the max shear stress at the ball–pad interface increases also as FAB diameter increases. The above results indicate that the FAB diameter has significant impact on bond pad and device's stress.
2. Impact of FAB diameter with the same bonding force
   Tables 8.13 and 8.14 give the stress comparison of bond pad and below structure with the same bonding force.

   Table 8.13 shows that the ILD layer's max first principal stress S1 (tensile) increases slightly as the FAB diameter increases to 2.9 mil then decreases as the FAB diameter increase to 3.0 mil. The max third principal stress S3 (compressive) decreases as the FAB diameter increases. Table 8.14 shows that both the

Table 8.14 Max stress at the ball–pad interface in different FAB diameters with the same bonding force

FAB diameter (mil)	Sy of ball–pad interface (MPa)	Shear stress of ball–pad interface (MPa)
2.8	307.9	89.1
2.9	298.2	86.9
3.0	295.7	81

Table 8.15 Max stress on ILD layers at bonding temperature

Bonding temperature (degree)	S1 of ILD (MPa)	S3 of ILD (MPa)
190	57.2	277
205	61.4	283.5
220	68	276.3

max Y component (vertical compressive) stress and the max shear stress on ball–pad interface decreases as the FAB diameter increases. These results show that the FAB diameter's impact on bond pad and the device below is not very significant when the same bonding force is set as compared to the case with the same squashed ball height.

8.4.2.3 Effect of Bonding Temperature

Here, we discuss the effects of bonging substrate temperature only. The heat effect induced in the wire bonding process is not considered. Both the stress at bonding temperature and stress at room temperature are studied. The capillary IC angle is set to be 90°.

1. Wire bonding stress with three different bonding substrate temperatures
   Table 8.15 shows that ILD layer's max first principal stress S1 increases as bonding temperature increases. While the max third principal S3 (compressive) stress increases when the temperature ramps up to 205°C from 190°C, then it decreases after the temperature ramps up to 220°C. This may be induced by the metal layer's yield stress decreasing as the bonding temperature increases. A higher temperature allows a larger metal deformation which further induces a higher first principal stress (tensive/bend) in the ILD layer. The bonding force applied is the same for all three temperatures in Table 8.15.

   Table 8.16 shows stress comparison at ball–pad interface. The max Y component (vertical) stress has a slight increment when the bonding temperature increases to 205°C but then decreases when bonding temperature increases to 220°C. The max shear stress increases slightly when the bonding temperature increases.
2. Stress distribution when cooling down room temperature
   Table 8.17 shows that the max first principal stress S1 (tensile) on ILD layer increases when it cools down to the room temperature. However, the max third

Table 8.16 Max stress of the ball–pad interface at bonding temperature

Bonding temperature (degree)	Sy of ball–pad interface (MPa)	Shear stress of ball–pad interface (MPa)
190	303.7	88.9
205	307.9	89.1
220	287.6	89.3

Table 8.17 Max stress on ILD layers at 25°C

Bonding temperature (degree)	S1 of ILD (MPa)	S3 of ILD (MPa)
190	146.9	225.6
205	156.5	224.1
220	166.6	221.5

Table 8.18 Max stress of the ball–pad interface at 25°C

Bonding temperature (degree)	Sy of ball–pad interface (MPa)	Shear stress of ball–pad interface (MPa)
190	109.3	57.1
205	91.9	51.9
220	82.1	48.1

Table 8.19 Max stress on ILD layers with different FAB tangent moduli

Tangent modulus (MPa)	S1 of ILD (MPa)	S3 of ILD (MPa)
250	31.8	219.4
320	61.4	283.5
400	85.3	334.2

Table 8.20 Max stress of the ball–pad interface with different tangent moduli

Tangent modulus (MPa)	Sy of ball–pad interface (MPa)	Shear stress of ball–pad interface (MPa)
250	254.9	72.3
320	307.9	89.1
400	359	104.6

principal stress S3 (compressive) decreases slightly as temperature goes down to room temperature. Table 8.18 shows that both of the max Y component vertical compressive stress and the max shear stress at the ball–pad interface decrease as temperature cools to room temperature.

8.4.2.4 Effect of FAB Material Properties

The FAB material properties are defined as bilinear plastic material with an initial yield stress and three different tangent moduli. The results of different tangent modulus of FAB are shown in Tables 8.19 and 8.20 which are obtained with a FAB diameter of 2.8 mil and a bonding temperature of 205°C.

Table 8.21 wire pull test results

Bonding force (N)	Wire	Test units	Failed units	Average pull force (N)
0.2	A	24	1	0.1912
0.4	A	24	1	0.1893
0.2	B	24	0	0.1733
0.4	B	24	1	0.1727

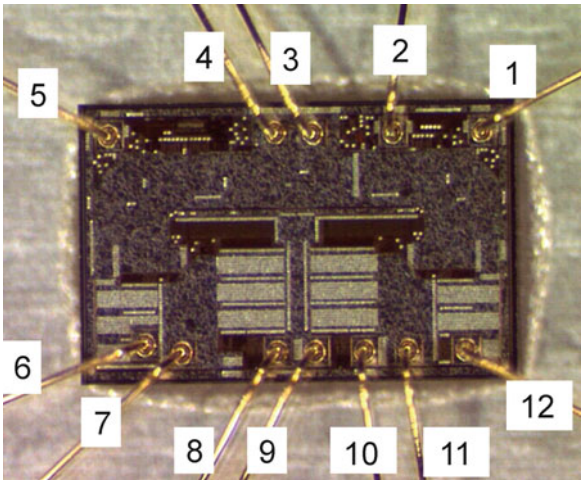


Fig. 8.33 A die with 12 bonded wires

Table 8.19 gives the max first principal stress S1 and the max third principal stress S3 comparison on ILD layer. Table 8.20 gives the max Y component vertical stress comparison and the max shear stress comparison at ball–pad interface. All above results show that all stresses increase as the FAB's tangent modulus increases. The FAB tangent modulus has significant impact on the stresses of bond pad and device; the harder the FAB, the higher stresses are induced in the wire bonding process.

8.4.2.5 Experimental Pull Test

Wire pull test results are shown in Table 8.21 and Figs. 8.33 and 8.34.

Table 8.21 gives comparison of bonding force and the FAB's tangent modulus. The parameters of bonding force selected for test are 0.2 and 0.4 N. Two types of wire are selected for comparison. The tangent modulus of wire A is higher than Wire B. A DOE test was conducted for these two parameters. There is no failing unit in the group with low bonding force and low wire tangent modulus. The other three groups have one failing unit each. Table 8.21 also shows that a lower FAB tangent modulus results in a lower average pull force.

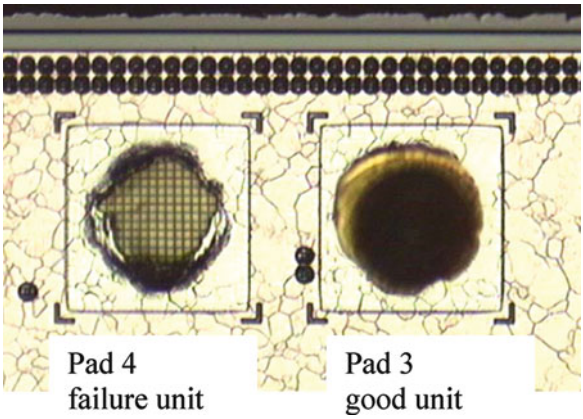


Fig. 8.34 Failing unit and good unit after wire pull test

Figure 8.33 shows the device with 12 bonded wires. Figure 8.34 shows pad 3 and pad 4 of the device after wire pull test. The wire bonded to pad 3 is a good unit which shows wire break at neck of the ball to a 5 mil distance above the ball. The wire bonded to pad 4 is a failing unit which shows metal lifting.

Through the above modeling and experimental study for a ball wire bonding, we learnt the following:

1. Increasing the FAB diameter and keeping the same ball height will require increasing the bonding force. All of the stresses in bond pad and device will increase at this case. Increasing the FAB diameter and keeping the same bonding force may decrease the Y component vertical stress but increase shear stress in bond pad and device.
2. Simulation results show that the capillary IC Angle and temperature does not have significant impact on stresses of bond pad and its below device.
3. There is a stress trade-off with different bonding temperature. When the bonding temperature increases, the ILD first principal stress (tensile stress) will increase while its Y component vertical stress Sy at the interface of ball and bond pad will decrease. When cooling down to room temperature, the ILD first principal stress will significantly increase.
4. Both modeling and experimental data shows a significant improvement in the wire pull test by reducing FAB's tangent modulus. This means harder FAB will induce more failures of bond wire lift.

8.4.3 Optimization of Wedge Bonding for a Power Package

Among the wire bond-related failure mechanisms wedge bond heel crack is quite common and critical in the power semiconductor industry [22, 23]. This section focuses on enhancing the robustness of Al wire wedge bond heel in a power

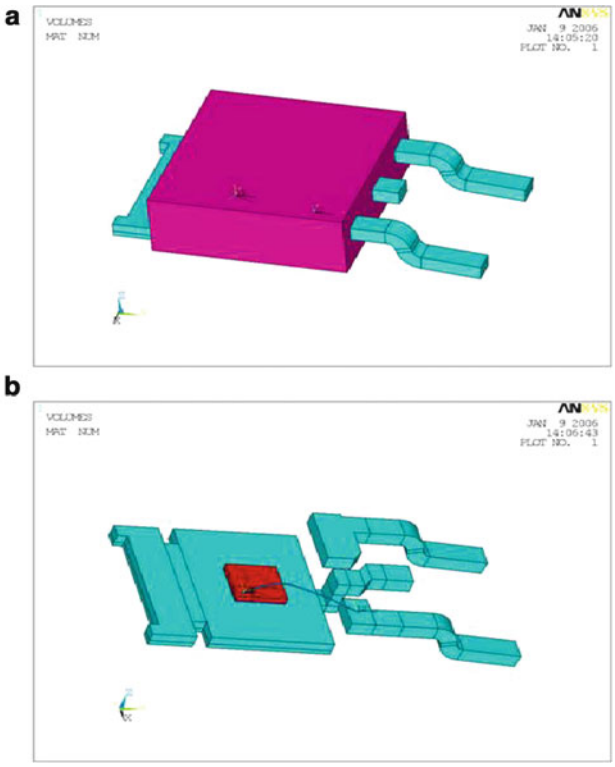


Fig. 8.35 A D-PAK model

package D-PAK under the reliability test of temperature cycling. The Al wire wedge bond shape can be approximately described by the wedge bond cross section, bond length, and wire loop profile. To understand the impact of these three parameters, an orthogonal test is designed with three factors and two levels. The wedge bond cross section is screened out as the most important factor from the simulation results by the nonlinear finite element code ANSYS®. Then, detailed DOE simulations on the wedge bond cross section are conducted to obtain the optimal one. According to this guidance, practical tests based on the shape of bond cross section under temperature cycling are carried out experimentally. Packages with two different bond cross sections of Al wire are tested in the reliability lab under temperature cycling. It is found that packages with the recommended Al wire bond cross sections are more robust, which confirms the simulation results.

8.4.3.1 Optimization of Al Wire Bond

A power type package D-PAK model is shown in Fig. 8.35. Since the gate wire failure is a common issue in the power semiconductor assembly, therefore, only a

Table 8.22 Material property data of D-PAK

	Young's modulus (GPa)	Poisson's ratio	Yield stress (MPa)	Tangent modulus (GPa)	CTE (ppm/K)
Silicon	162.5	0.22			2.8
Lead frame	118	0.345	330	3.3	17.7
Solder	13.79	0.35	29	0.29	28.7
Al wire	70	0.345	186	1.86	23.5
EMC	17	0.3			11; 47

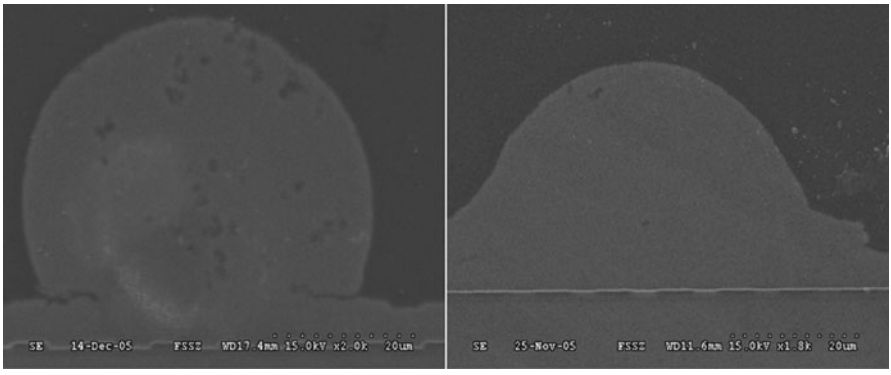


Fig. 8.36 Al wire bond cross section: (1) low deform, (2) high deform

2 mil Al gate wire is selected in the analysis (as shown in Fig. 8.35b). In this package, the Al wire, solder and lead frame are assumed to be bilinear elastic plastic materials. Die and molding compound are assumed as elastic materials. The detailed material property data are listed in Table 8.22.

The Al wire wedge bond shape can be approximately described by bond cross section, bond length, and wire loop profile. In order to understand the impact of the bond cross section, bond length, and wire loop profile, two levels of each parameter are considered (shown in Figs. 8.36–8.38). An orthogonal test is designed with three factors and two levels, and the orthogonal table L4 (2^3) is adopted (Table 8.23).

The loading condition is under the reliability test of temperature cycling (−65 to 150°C). The von Mises stress and plastic strain distribution in the Al wire of test 1 are shown in Figs. 8.39–8.42, respectively. It can be seen that the maximum von Mises stress and plastic strain in the wire occur around the bond heel area. The simulation results of the maximum von Mises stress and plastic strain for all the four tests are summarized in Table 8.24.

The DOE simulation results are then analyzed by the statistical software JMP®. Based on the plastic strain in the Al wire, the Pareto plot of estimates and prediction profile plot are shown in Figs. 8.43 and 8.44, respectively. A Pareto plot is a statistical quality improvement tool that shows frequency, relative frequency, and cumulative frequency of problems in a process or operation. It is a bar chart that

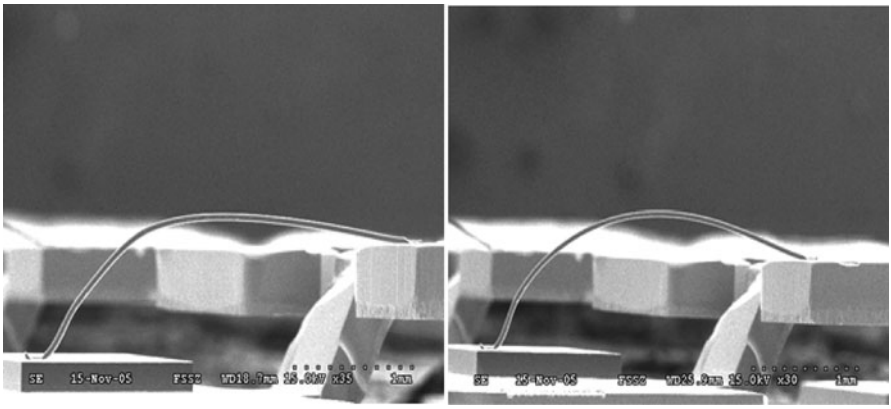


Fig. 8.37 Al wire bond loop profile: (1) tight loop, (2) high loop

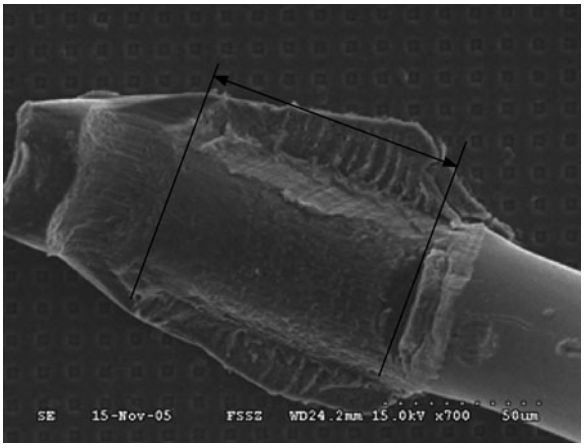


Fig. 8.38 Al wire bond length: (1) 90 μm, (2) 60 μm

Table 8.23 Orthogonal table L4 (2^3)

	Factors		
Test no.	Cross section	Bond pad length	Wire loop
1	1	1	1
2	1	2	2
3	2	1	2
4	2	2	1

displays severity (frequency) of problems in a quality-related process or operation in decreasing order, which makes a Pareto plot useful for deciding what problems should be solved first. The Prediction profiler displays prediction traces for each *X* variable. It is a way of changing one variable at a time and looking at the effects on the predicted response.

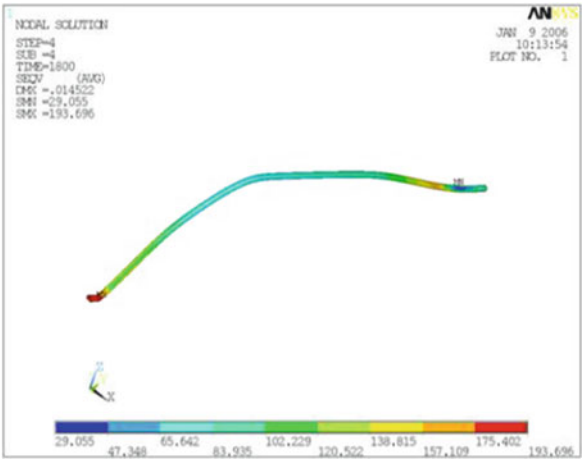


Fig. 8.39 von Mises stress in the Al wire

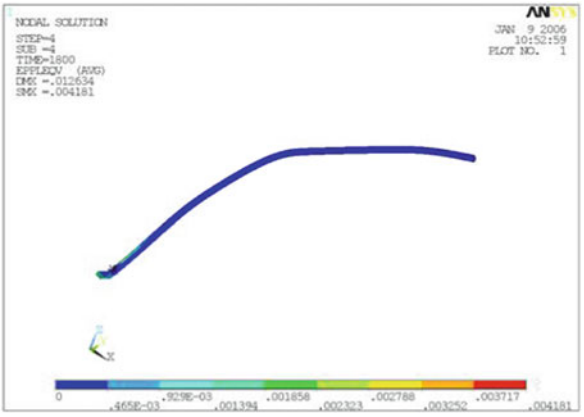


Fig. 8.40 Plastic strain in the Al wire

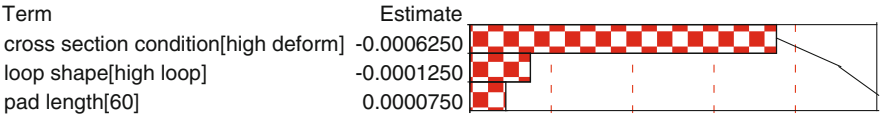


Fig. 8.41 Pareto plot of estimates

From Figs. 8.43 and 8.44, it can be concluded that the wedge bond cross section has the biggest impact on the plastic strain in the Al wire. The wedge bond length and wire loop profile have comparatively less impact. Therefore, the effect of bond

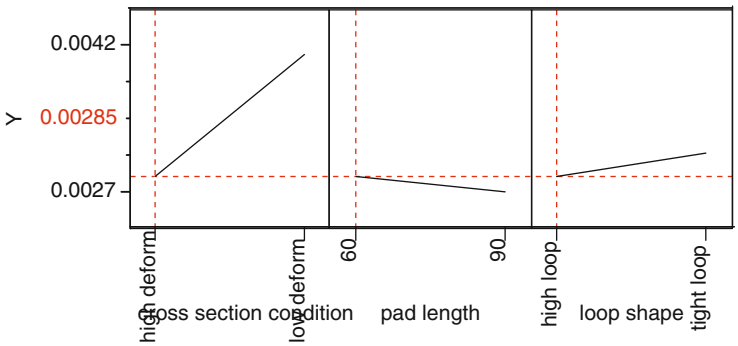


Fig. 8.42 Prediction profile plot

Table 8.24 Simulation results in the Al wire

	Factors				
Test no.	Cross section	Bond pad length	Wire loop	von Mises stress (MPa)	Plastic strain (%)
1	1	1	1	194	0.42
2	1	2	2	194	0.41
3	2	1	2	193	0.27
4	2	2	1	193	0.31

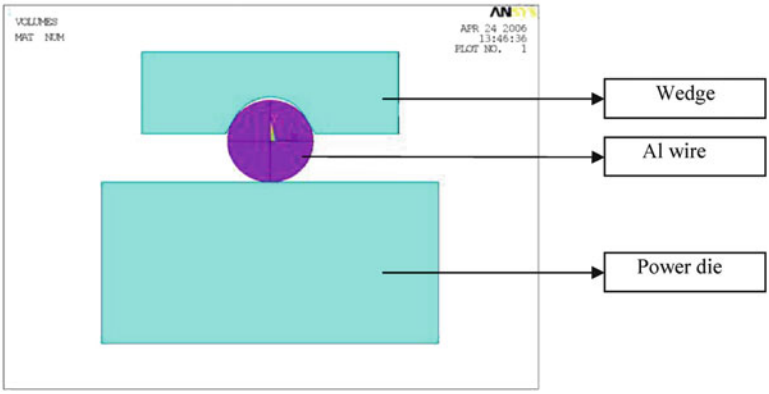


Fig. 8.43 FEA model of wire bond on die

cross section on the Al wire bond heel is investigated in the next section. In order to obtain longer fatigue life of Al wire, it is recommended to select wedge bond cross section with high deformation, long bond pad, and loose wire loop profile.

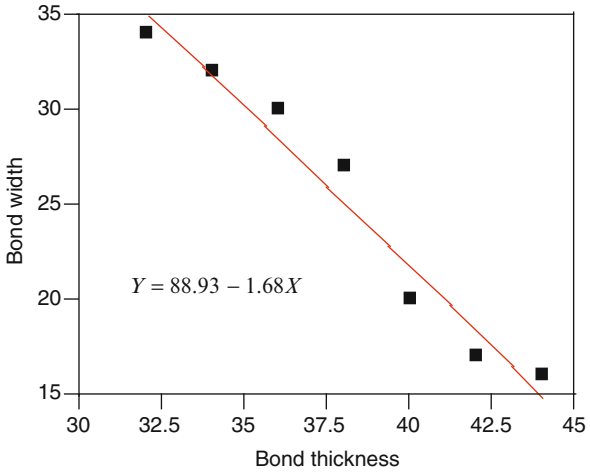


Fig. 8.44 Relationship between bond pad width and thickness

8.4.3.2 Optimization of Al Wire Wedge Bond Cross Section

As discussed in the previous section, the wedge bond cross section has the biggest impact on the Al wire bond heel. Because the wedge bond length has not much impact on the bond heel and a short bond length is helpful to get thick bond, the wedge bond length is fixed at 63.5 μm.

In the practical wire bond process it is hard to get the wedge bond cross section dimension. So different wedge bond cross section shapes are obtained by the FEA model as shown in Fig. 8.43. The relationship between wedge bond width and thickness is illustrated by linear regression in Fig. 8.44. The compressive bonding process is assumed for simplicity, with ultrasonic effect neglected. The wedge capillary and die are assumed to be rigid.

In total seven different Al wire wedge bond cross section shapes (listed in Table 8.25) are simulated under temperature cycling for a D-PAK. Figure 8.45 shows the von Mises stress distribution in the package with Al wire wedge bond cross section (4) in the Table 8.25. The von-Mises stress and plastic strain distribution in the Al wire bond heel for the same model are illustrated in Figs. 8.46 and 8.47, respectively. All the simulation results of the maximum von Mises stress and plastic strain in the Al wire bond heel are summarized in Table 8.26.

The maximum plastic strain in the Al wire bond heel with respect to the bond width is plotted in Fig. 8.48a. Considering the bonding capability in the wire bonding process and bondability between the Al wire and chip, the simulation results corresponding to bond pad width 20, 27, and 30 μm are analyzed in JMP® by curve fitting with second-degree polynomial as expressed in Fig. 8.48b and (8.14).

$$Y = -0.6830 + 0.0309X + 0.01043(X - 25.67)^2 \tag{8.14}$$

Table 8.25 Bond pad cross section shapes for DOE

Case	Thickness (μm)	Width (μm)	Cross section
1	44	16	
2	42	17	
3	40	20	
4	38	27	
5	36	30	
6	34	32	
7	32	34	

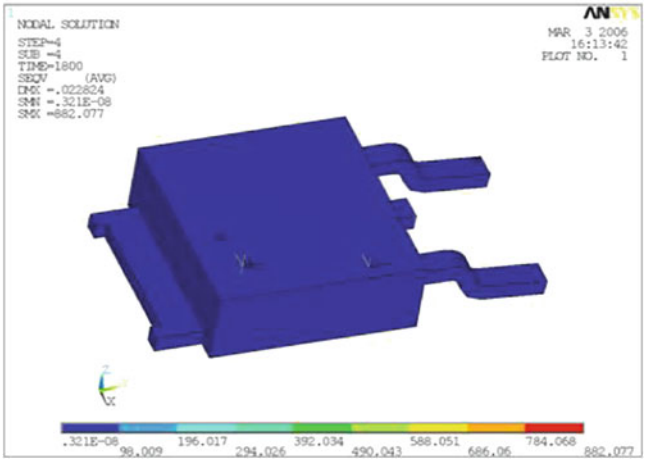


Fig. 8.45 von Mises stress in the D-PAK with the cross section (4)

where X is the bond width, and Y is the maximum plastic strain in the Al wire bond heel.

To get the minimum plastic strain, differentiate the equation (8.14) at both sides, and let $dY/dX = 0$. It is obtained that when the bond width is about 24 μm, the plastic stain reaches a minimum value of 0.087%. Therefore, from the view point of Al wire bond heel reliability under temperature cycling, the optimal wedge bond width from 24 to 27 μm is recommended according to the previous DOE results and

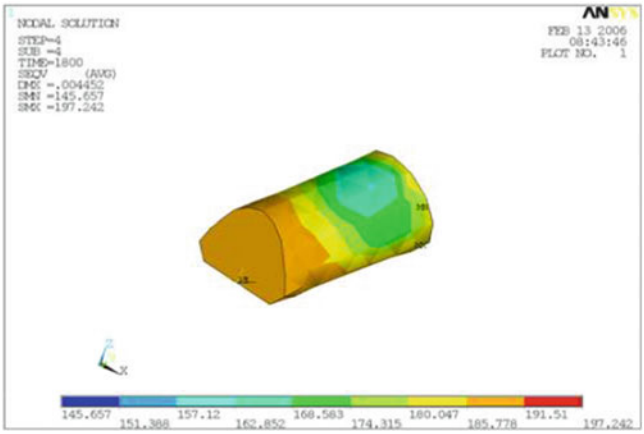


Fig. 8.46 von Mises stress in the wire bond heel

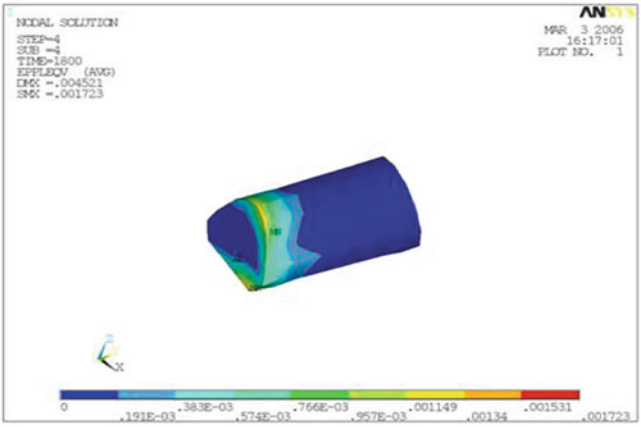


Fig. 8.47 von Mises plastic strain in the wire bond heel

Table 8.26 Simulation results in the Al wire bond heel with different cross sections

Case	Thickness (μm)	Width (μm)	von Mises stress (MPa)	Plastic strain (%)
1	44	16	192	0.14
2	42	17	193	0.17
3	40	20	190	0.27
4	38	27	189	0.17
5	36	30	194	0.44
6	34	32	194	0.42
7	32	34	193	0.38

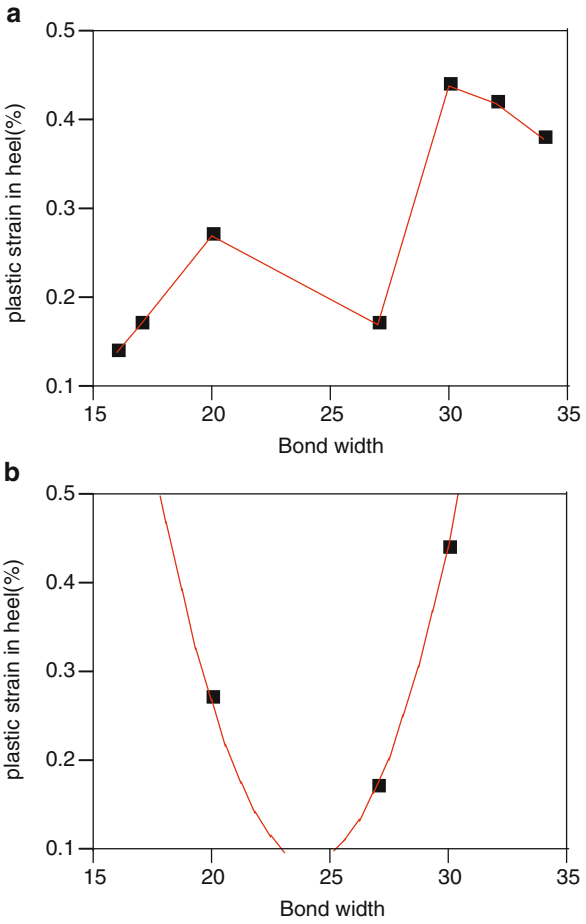


Fig. 8.48 Max plastic strain vs. bond pad width

JMP® analysis. According to the linear regression of bond width with respect to the bond thickness in Fig. 8.44, the corresponding wedge bond thickness should be 37–39 μm.

The maximum plastic strain in the Al wire bond heel with respect to the bond thickness is shown in Fig. 8.49a. The results corresponding to bond thickness 36, 38, and 40 μm are then analyzed in JMP® by curve fitting with second-degree polynomial as expressed in Fig. 8.49b and (8.15).

$$Y = 1.785 - 0.0425X + 0.04625(X - 38)^2 \tag{8.15}$$

where X is the bond thickness, and Y is the maximum plastic strain in the Al wire bond heel.

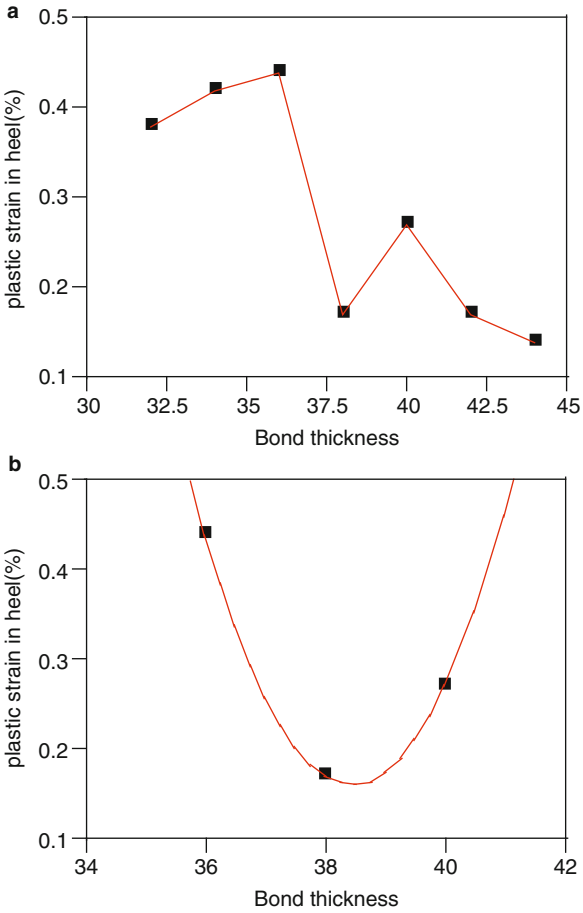


Fig. 8.49 Max plastic strain vs. bond thickness

By similar method, it can be obtained that when the wedge bond thickness is about 38.5 μm, the minimum plastic stain falls to 0.16%. Therefore, the optimal bond thickness from 38 to 40 μm is recommended from the view point of the Al wire bond heel reliability under temperature cycling. According to the linear regression of bond width with respect to the bond thickness in Fig. 8.44, the corresponding wedge bond width should be 22–25 μm.

8.4.3.3 Experimental Test

Three lots of D-PAK packages were produced in the process line according to the previous recommendations about the wire wedge bond shape. The wedge with the

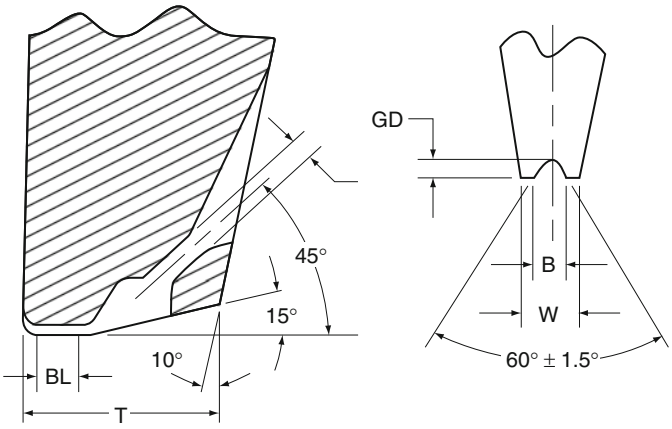


Fig. 8.50 Schematic drawing of wedge with BL 63.5 µm

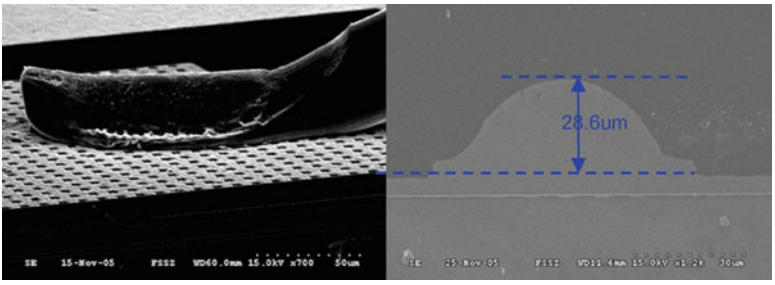


Fig. 8.51 Reference bond pad shape with thickness 28 µm

bond length (BL) 63.5 µm was used in the wire bonding process as shown in Fig. 8.50. By adjusting the wire bonder's parameters such as start and bond force, start and bond power, start and bond time, etc., the bond thickness is controlled and targeted to around 38 µm (as shown in Fig. 8.52) because it is difficult to measure the exact wedge bond width. After the wire bonding process, molding, plating, and trim/form processes are conducted to produce the D-PAK packages. Thereafter, all the packages are sent to reliability lab to do power cycling test, temperature cycling test (−65 to 150°C), and autoclave test. For comparison, one lot of packages with the regular (nonoptimized) bond thickness 28 µm (as shown in Fig. 8.51) is also tested as reference.

The reliability test results are summarized in Table 8.27 for three test lots (T1–T3) and one reference lot (R1). All four lots of packages pass the autoclave test and power cycling tests with 5, 10, and 15K cycles. For temperature cycling test, all four lots of packages pass 200 and 500 cycles. After 1,000 cycles, one package out of the three test lots fails, and eight packages out of one unoptimized lot failed due to wire bond heel crack issue, the optimized bond process failure rate is 4% of the nonoptimized process. According to the JEDEC standard, the

Table 8.27 Reliability test results

	PRCL (cycles)			ACLV	TMCL (cycles)		
Lot #	5K	10K	15K	96H	200	500	1,000
T1	0/77	0/77	0/77	0/77	0/77	0/77	0/77
T2	0/77	0/77	0/77	0/77	0/77	0/77	1/77
T3	0/77	0/77	0/77	0/77	0/77	0/77	0/77
R1	0/77	0/77	0/77	0/77	0/77	0/77	8/77

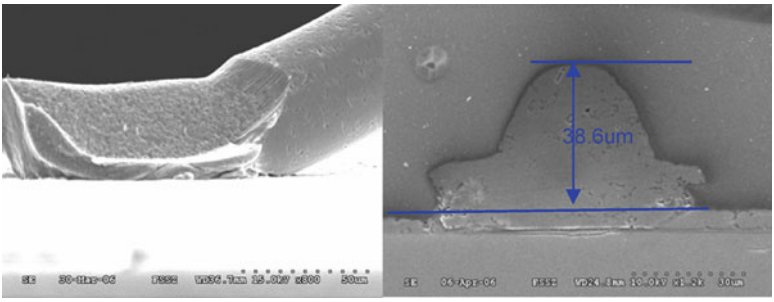


Fig. 8.52 Tested bond pad shape with thickness 38.6 μm

temperature cycling standard is 500 cycles for nonautomotive device. Therefore, all the packages pass the reliability test. By comparing the test results after 1,000 cycles of temperature cycling, it can be seen that the packages with the recommended wire bond pad shape are more robust than the normal cases. Further process optimization will be conducted to improve the Al wire bond heel performance with the optimized wedge bond shape (Fig. 8.52).

8.5 Molding

In the injection molding process, most of the molding compounds are initially liquid at high temperature. It changes to solid as the temperature decreases after some time and never changes back to liquid (thermoset). The material properties vary over temperature and time. This section discusses the molding flow process and the assembly operations after the molding.

8.5.1 Molding Flow Simulation and Analysis

Semiconductor chips are often encapsulated with an EMC for protection. Transfer molding technology has advantages for IC packages with small size, low cost, high productivity and liability. It has been used in various IC package as well as the

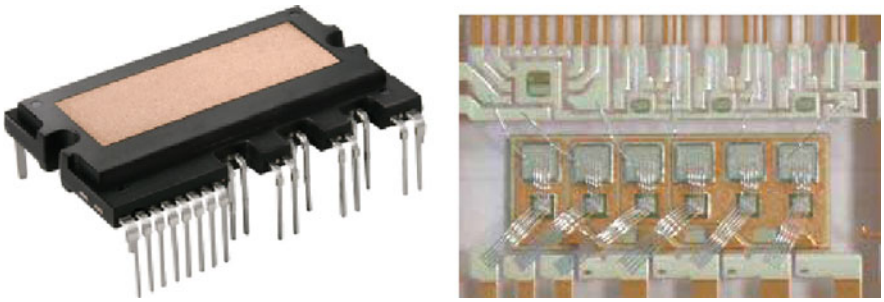


Fig. 8.53 A power module package with a group of IGBT die, diodes, and LV/HV die

various power packages. For better mold flow design and optimization of processing, the molding flow simulation and analysis are necessary

Figure 8.53 shows a power module package after the molding, which includes a group of power IGBT die, diodes, and LV and HV IC die.

8.5.1.1 Basic Formulation for 3D Mold Flow

Typically the thickness of the chip cavity is much smaller than its width, so the generalized Hele-Shaw approximation may be used [24, 25]. Because we are only interested in the filling stage of encapsulation where the degree of cure of the sample is low, the fluid elasticity is neglected, thus assuming the flow to be generalized Newtonian. Thus, we have the following equations for mold flow [24]:

$$\frac{\partial \rho}{\partial t} + \nabla \cdot (\rho v) = 0 \tag{8.16}$$

$$\rho \frac{Dv}{Dt} = -\nabla P + \nabla \cdot \boldsymbol{\tau} + \rho g \tag{8.17}$$

$$\rho C_{\mathrm{p}} \frac{DT}{Dt} = \nabla \cdot (k \nabla T) + \eta \dot{\gamma}^2 + \beta T \frac{DP}{Dt} + H \frac{D\alpha}{Dt} \tag{8.18}$$

$$\frac{D\alpha}{Dt} = (K_1 + K_2 \alpha^{\mu})(1 - \alpha)^{v} \tag{8.19}$$

where

$$K_1 = A_1 \mathrm{e}^{(-(E_1/T))}, \quad K_2 = A_2 \mathrm{e}^{(-(E_2/T))} \tag{8.20}$$

Equations (8.16)–(8.18) describe conservation of mass, momentum, and energy, respectively. The third term in (8.18) is the irreversible internal energy loss due to viscous dissipation. The last term in (8.18) represents the heat generated due to curing.

The stress tensor $\boldsymbol{\tau}$ ($= \boldsymbol{\sigma} + P\mathbf{I}$) is expressed explicitly as a function of the deformation rate tensor $\dot{\boldsymbol{\gamma}}$ (i.e., generalized Newtonian fluid model). Equations (8.19) and (8.20) are Kamal's curing equations.

Equations (8.16)–(8.18) are solved for an incompressible fluid by both a 3D Navier–Stokes and a 3D fast solution method. The fast solution method uses an approximation of the full Navier–Stokes equations and is generally sufficiently accurate for many cases of molding simulation.

For the viscosity, we use the Cross-Exponential-Macosko viscosity model. This model can be represented by the following equations:

$$\eta(\alpha, T, \dot{\gamma}) = \frac{\eta_0(T)}{1 + (\eta_0(T)\dot{\gamma}/\boldsymbol{\tau}^*)^{1-n}} \left(\frac{\alpha_g}{\alpha_g - \alpha}\right)^{(C_1 + C_2\alpha)} \tag{8.21}$$

$$\eta_0(T) = Be^{(T_b/T)} \tag{8.22}$$

In molding flow simulation, the venting analysis is to calculate the pressure drop of the air that passes through the vent and to include the effects of air pressure on the flow simulation of the microchip encapsulation process. Pressure drop through the vent can be calculated using the viscous flow analysis. Each vent can have different properties (dimensions, exit pressure). The volume of air connected to a vent can be calculated by adding the volume of all the nodes that are identified as air nodes connected to a vent. The viscosity of air is assumed to be constant [26]. The pressure of the air at the vent exit can be specified. There can be several vents connected to a cavity.

Neglecting the side wall effect, the formula of the pressure drop in a vent can be obtained as following [26]

$$\Delta p = \frac{12\eta QL}{h^3 w} \tag{8.23}$$

When side wall effect is considered, the pressure drop formula can be given by:

$$\Delta p = \frac{12\eta QL}{h^3 w} \times \frac{16}{3}\frac{l}{s} \tag{8.24}$$

$$s = \frac{16}{3} - \frac{1,024}{\pi^5}\frac{h}{w}\sum_{n=0}^{\infty}\frac{\tanh((2n+1)\pi w/2h)}{(2n+1)^5} \tag{8.25}$$

In the above equations, Δp is pressure drop at the vent, η is the viscosity, Q is the flow rate, l is the length of the vent, h is the thickness of the vent, and w is the width of the vent. When the pressure drop at the vent is small, the simulation value and the value obtained from the above analytical equations matched well.

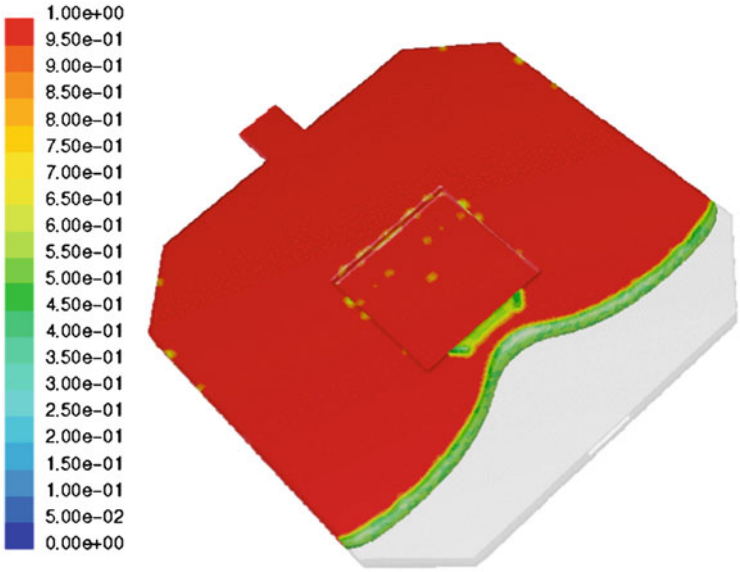


Fig. 8.54 A BGA molding filling process

8.5.1.2 Molding Flow Simulation Results

In this chapter, ANSYS-Fluent™ and Moldflow™ software are used for saving time and money during the power package development stage. The material properties of epoxy mold compound are listed as follows:

1. For reaction kinetics properties

   $H = 37{,}693$ J/kg, $B1 = 0$, $B2 = 0$, $m = 0.5955$, $n = 1.437$, $A1 = 0.1$/s, $A2 = 1.9381$/s, $E1 = 3670.9$ K, $E2 = 8886.54$.

2. Reactive viscosity model coefficients

   $n = 0.55$, $\tau^* = 0.0001$ Pa, $B = 1.8242\text{e} - 014$ Pa s, $\text{Tb} = 22549.7$ K, $c1 = 5.456$, $c2 = 0.4491$.

Two simulation examples are presented for the molding flow and curing processes.

Example A BGA filling and curing modeling for a single cavity.

Example A shows a BGA molding and curing case by ANSYS FLUENT software. Figure 8.54 gives the process of the molding flow filling the cavity of BGA. The simulation shows the flow front situation and the air track during the molding filling. Figure 8.55 shows the curing after molding injection. This contour figure gives the curing process in the BGA cavity which clearly shows the nonuniform curing distribution.

Example B Molding flow front simulation for a group of the cavities.

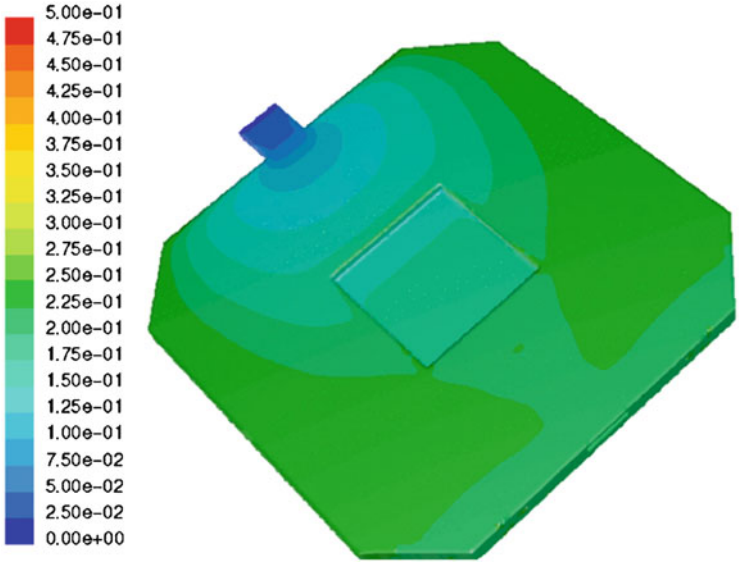


Fig. 8.55 The curing process at 50 s

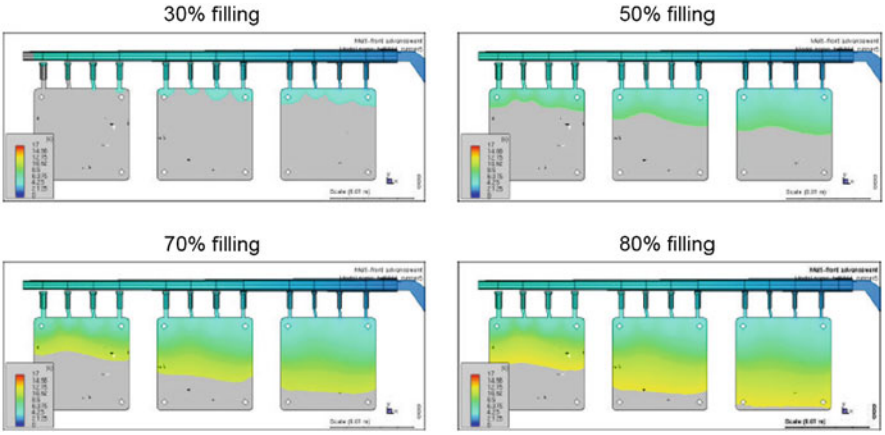


Fig. 8.56 Mold flow front and cavities filling in molding process

Figure 8.56 shows a three cavities molding flow model with a main runner and 12 subrunners. The simulation is completed through the Moldflow. It shows the mold flow front surface and different percentage of the mold filling. The cavity in right hand side is filled fast due to its location which is close to the entrance of main runner and the difference of mold pressure. This allows us to design the runner, subrunner, and gate system with reasonable and optimized method to keep a

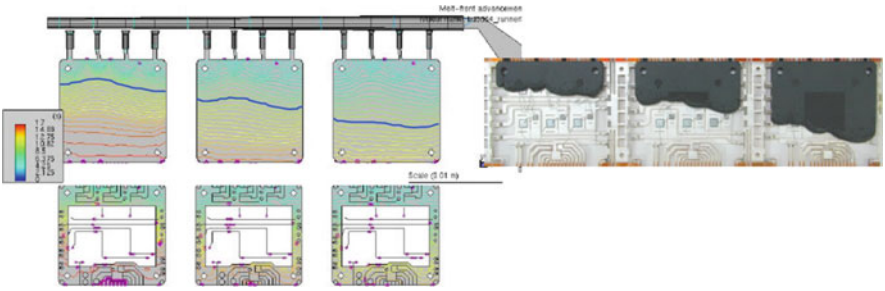


Fig. 8.57 Simulation result of mold flow front surface with comparison of snap shot image



Fig. 8.58 A picture of the cavity of in a mold die (© 2008 IEEE)

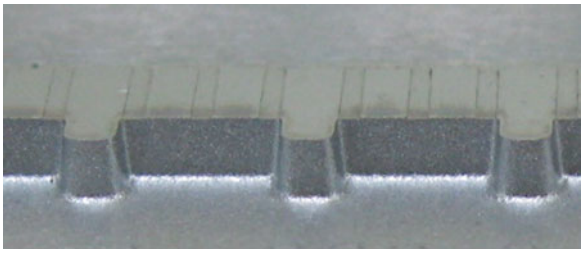


Fig. 8.59 A local photo of air vents (© 2008 IEEE)

relative uniform mold flow front speed in a cavity. Figure 8.57 gives the simulation result of the mold flow front and a snap shot image. It shows the simulation result agrees with the actual flow front of the molding process.

Example C Molding simulation with consideration of vent effects.

This example is selected from the molding flow study of Fairchild Semiconductor [26]. Figure 8.58 shows one cavity of an actual mold die, and Fig. 8.59 is a local image of the region indicated by red ellipse in Fig. 8.58.

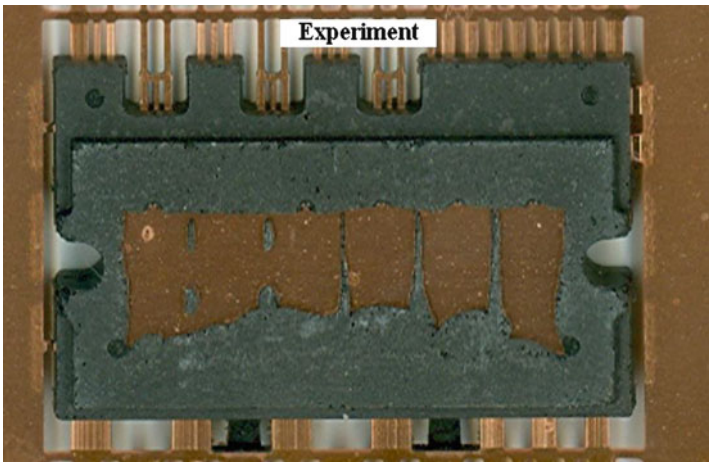


Fig. 8.60 Actual incomplete molding in package (© 2008 IEEE)

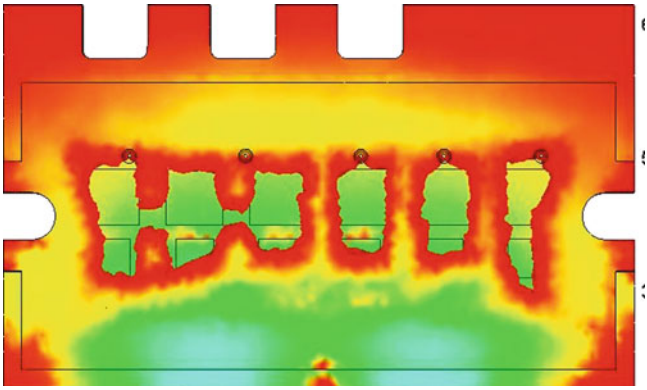


Fig. 8.61 Molding simulation result of package with air vent option (© 2008 IEEE)

After making finite element model including package and gate, air vents are added on the model. Figure 8.60 is a full power package type and has very small gap (less than 1 mm) between die attach pad and package bottom surface. It might have incomplete molding on back side of package, so this problem can cause some yield loss. Therefore, perfect mold ability is strongly needed to improve the design.

The result of molding modeling with air vent shows that the package has some air trap on the bottom side in center area when flow front reached the end of package, which is the root cause of the incomplete molding seen in Fig. 8.61. Figure 8.61 by simulation and Fig. 8.60 by actual molding correlate very well in mold flow front with air vent analysis.

Molding flow simulation is important for design and assembly process of IC packages with epoxy mold compound. It may help to improve the product quality

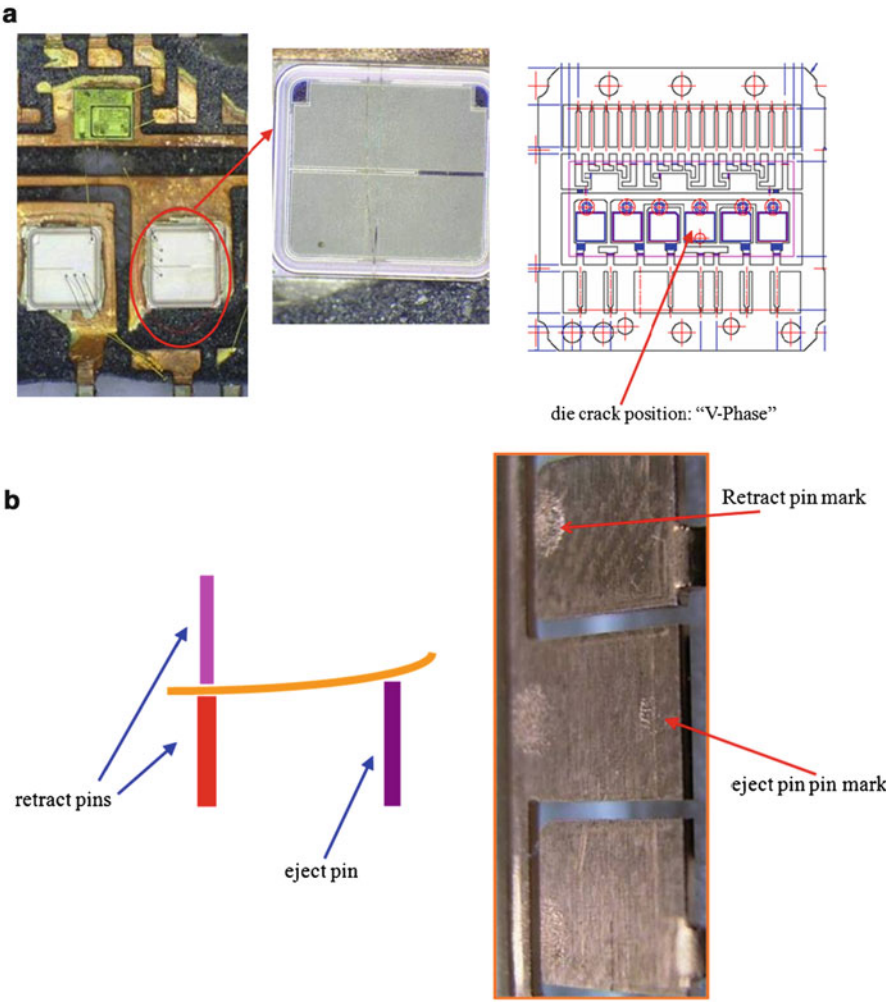


Fig. 8.62 The molding ejection and retract pins setup. (**a**) A typical crack on die in the ejection process after molding. (**b**) The retract pins, ejection pin and lead frame

and reliability such as to control and reduce the air trap in molding assembly process. This simulation can help the IC package design engineers and assembly manufacturing engineers to understand the mold flow front situation in single cavity and in a group of cavities with runner and subrunner system.

8.5.2 Molding Ejection

Molding ejection process starts after the molding injection and curing complete. A location pin in the mold will fix the lead frame position before the molding process. It insures the lead frame is located at the right place during the molding

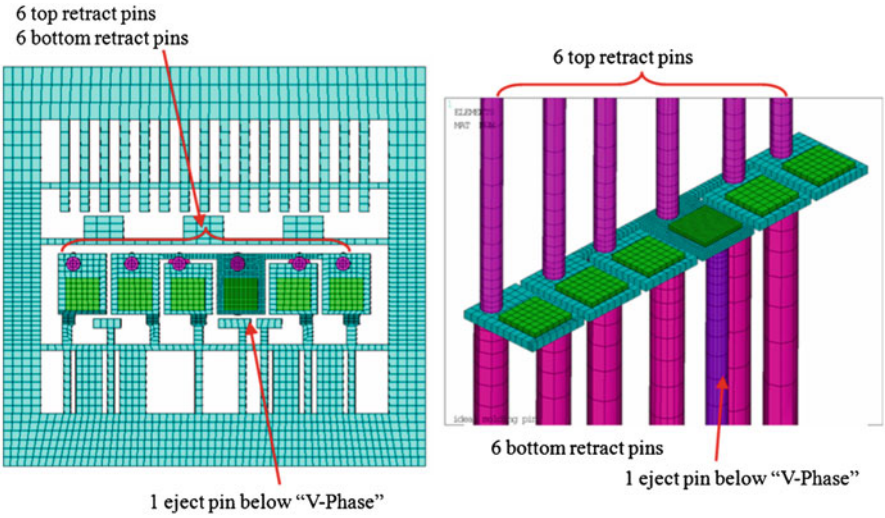


Fig. 8.63 Ejection model with 12 retract pins and 1 ejection pin

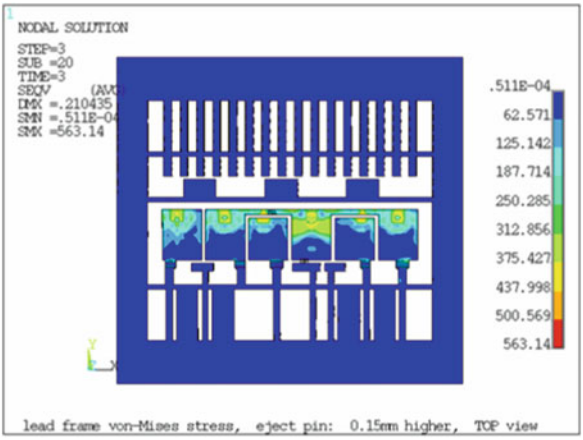


Fig. 8.64 von Mises stress of lead frame and die in ejection operation process

process. But it may also prevent the lead frame from being ejected from the mold because of the friction between location pin and lead frame. The purpose of molding ejection process simulation is to reduce the package failure. A typical molding ejection process with contact between lead frame, retract, and ejection pins are mounted as shown in Fig. 8.62, in which a common die crack is seen in Fig. 8.62a.

Figure 8.63 gives the ejection model which includes six top retract pins and six bottom retract pins and a ejection below V-phase die. Figure 8.64 shows the von Mises stress distribution of the lead frame with die in the operation process. It can be seen that the stress concentration appears at the dap and die.

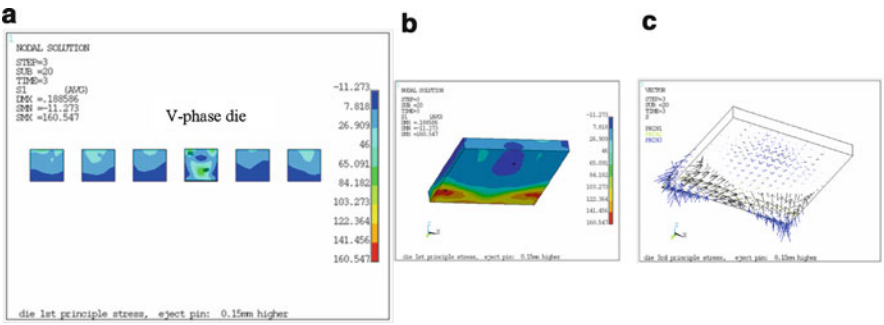


Fig. 8.65 First principal stress (tensile) on all IGBT die. (**a**) The stress distribution on all die, the maximum stress appears at V-phase die, (**b**) V-phase die maximum tensile stress: 160 MPa at bottom, surface (**c**) V-phase die maximum tensile stress direction (vector chart)

Table 8.28 The tensile stress S1 and compressive stress S3 in V-phase die

Mounting height from bottom retract pin to ejection pin (mm)	0	0.1	0.125	0.15	0.2
Max S1 on V-phase die (MPa)	117.3	125.1	144.5	160.5	182.3
Max S3 on V-phase die (MPa)	−33.8	−187.8	−212	−231.4	−255.8

Figure 8.65 shows the first principal (tensile) stress S1 on all IGBT die of the power module, in which the Fig. 8.65b, c particularly gives the V-Phase die first principal stress S1 and the stress vector directions. It shows the V-phase die is actually subjected to the larger bend tensile stresses at two sides of front bottom end of the die, which is the root cause to bend toward the die bottom and to induce the crack as shown in Fig. 8.62a.

Table 8.28 lists the first principal stress S1 (tensile) and the third principal stress S3 (compressive) on V-Phase die with different mounting heights from bottom retract pin to the eject pin. It can be seen that the ideal case is the mounting height of ejection pin is zero which induces the smallest tensile stress. As the mounting height of ejection pin increases, both the V-Phase stresses S1 and S3 increase significantly. While silicon die is a brittle material, it is tensile strength is much lower than its compressive strength, normally the tensile strength of silicon is between 170 and 500 MPa. The result in Table 8.28 shows that when the mounting height is larger than 0.15 mm, the silicon tensile stress will reach its lower end tensile strength, which needs more careful process.

8.6 Power Package Trim/Singulation

The use of lead frames during assembly processing is important for ease of handling and economics of scale for power packaging. The lead frame based power package has very good thermal conductivity to dissipate the heat from MOSFETs. These

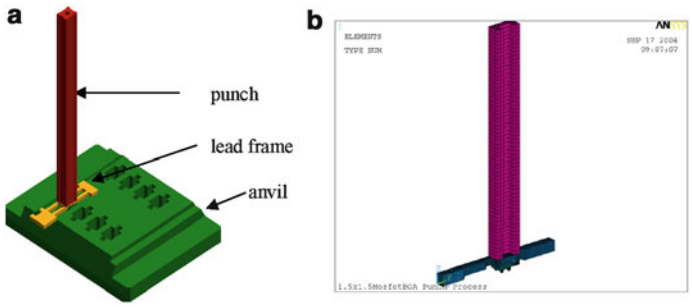


Fig. 8.66 Typical punch and lead frame for MOSFET BGA package. (**a**) Typical punch and lead frame, (**b**) a MOSFET BGA punch analysis model

lead frames can contain anywhere from one to thousands of individual products that must be singulated prior to completion. There are several methods by which singulation can be achieved, including saw or punch. The use of a punch is preferred for its speed and efficiency for the assembly process. In this section we looked at the use of a punch process to singulate assembled product, and in particular the use of FEA to model the stresses in the singulation process [27, 28]. This allows us to maximize final product yield and quality by minimizing the possibility of die cracking.

The advantages of using FEA simulation include lower cost and faster turn time. Simulation enables to reduce the experiment and try-out method that are too costly to be done by empirical methods. This includes the ability to optimize a package design under multiple requirements, for example we find that it may not be practical to empirically look at multiple combinations of materials, or lead frame geometry. Using simulation we can quickly and affordably find the conditions that optimize the cost, performance, and reliability under different sets of conditions.

8.6.1 Punch Process Setup

A simplified illustration of the tooling setup for the punch process is shown in Fig. 8.66a. The punch tooling consists of three pieces, the punch, its body guide, and the anvil. For the simulation, we assume the punch, guide, and anvil to be rigid bodies. A MOSFET BGA half punch model is seen in Fig. 8.66b.

A more detailed view of the primary section of the solid model is shown in Fig. 8.67. This illustration also shows the guide and punch relationship. Note the punch used in these studies is hollow in the region over the die. The action of the punch is such that when the punch is forced downwards, it cuts the lead frame and the freed lead frame falls through the anvil to a receptacle for collecting the units. The uniform and constant punch speed is very critical to assure the good quality for

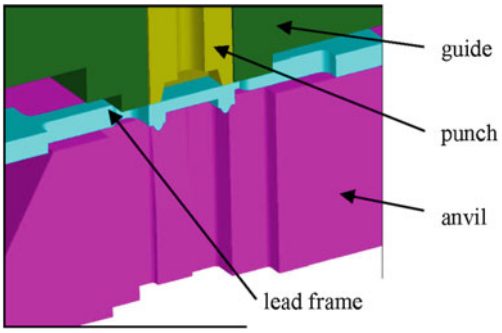


Fig. 8.67 Punch and lead frame

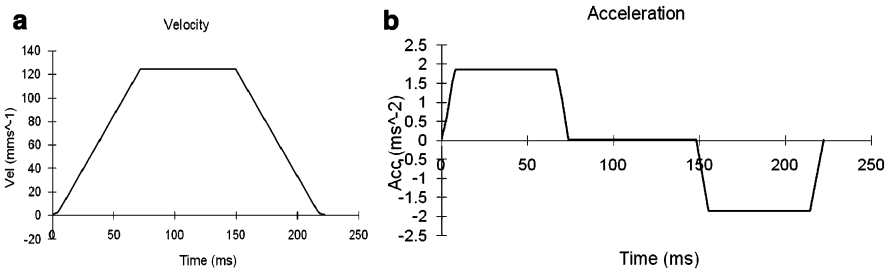


Fig. 8.68 The typical punch velocity and acceleration settings for the equipment. (**a**) Punch speed, (**b**) punch acceleration

Table 8.29 Materials parameters

	Lead frame	Silicon die	Die attach	Solder ball
Young's modulus (GPa)	117.72	169.5	41.6	23.5
Poisson's ratio	0.35	0.278	0.4	0.4
Density (kg/mm^3)	8.9E−6	2.39E−6	8.39E−6	1.13E−5
Failure strain	5–10%		20%	
Yield stress (MPa)	68.97		31	

the singulation process. The punch speed and acceleration settings for the singulation equipment are shown in Fig. 8.68.

Simulations were set up using the following material parameters in Table 8.29.

For the copper alloy an elastic plastic bilinear stress–strain relation is used. The copper alloy yield stress is 68.97E3 kPa, the tangent modulus is 6.897E6 kPa. For the purposes of the study, we assumed a strain failure criteria of 0.05–0.1 in the copper during the LS-Dyna simulations. AThis needs to be experimentally measured.

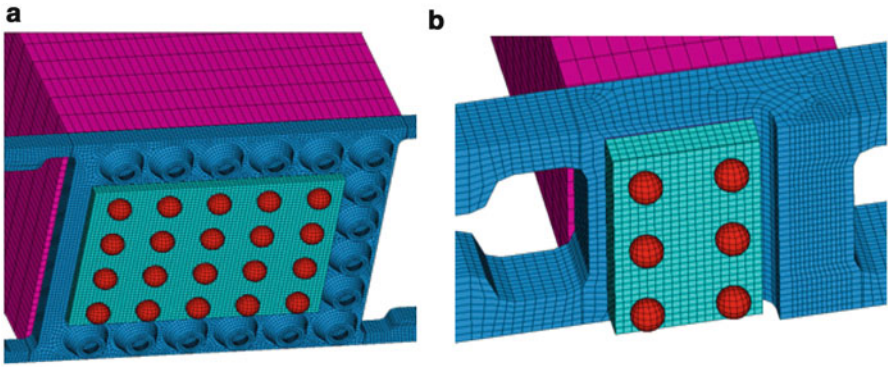


Fig. 8.69 Two MOSFET BGA design layouts: (**a**) 5 × 5 mm^2 MOSFET BGA, (**b**) 1.5 × 1.5 mm^2 MOSFET BGA

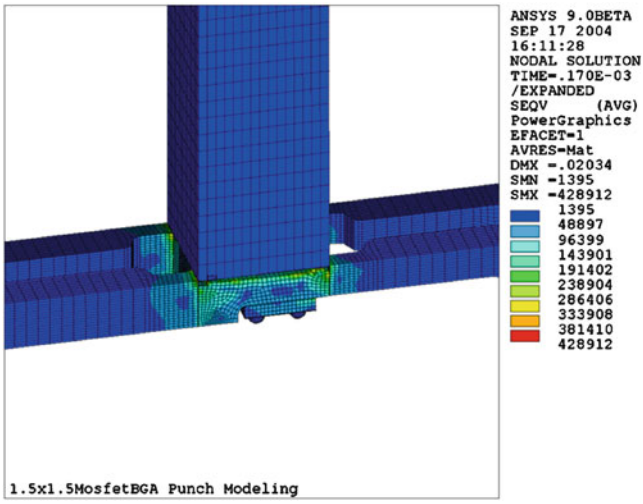


Fig. 8.70 Punching process of 1.5 × 1.5 mm^2 MOSFET BGA, Max von Mises stress: 429 MPa

8.6.2 Punch Process Analysis by LS-DYNA

The finite element program LS-Dyna was used to simulate the punch process. In setting up the analysis problem, we assume that the punch is a rigid body due to its very high hardness and Young's modulus. The punch has a constant velocity of 120 mm/s and no acceleration during the actual punch operation process (see Fig. 8.68). Figure 8.69 shows two MOSFET BGA models meshed with brick elements.

A short time after the initial contact there is a noticeable difference between the lead frame stress waves in two different MOSFET BGA designs. Figures 8.70 and 8.71 show the punch process simulations with the lead frame failure strain (LFS) 5%.

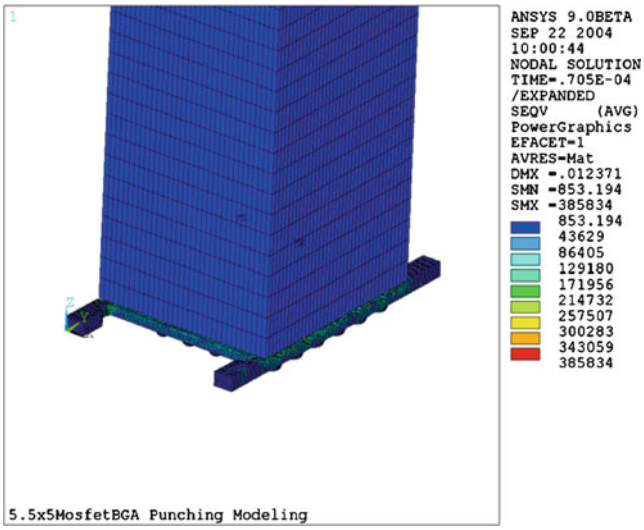


Fig. 8.71 Punching process of the 5 × 5 mm^2 MOSFET BGA Max von Mises stress: 385 MPa

Further examination of the stress in the die bears out the initial view. Figure 8.72 shows a comparison of the maximum von Mises stress that occurs in the die for two MOSFET BGA designs. The stress in the small die of 1.5 × 1.5 mm^2 MOSFET BGA is 2.58 times greater than the large die of 5 × 5 mm^2 MOSFET BGA.

Figure 8.73 shows a sequence of the die level stress as a function of time for two MOSFET BGA designs. The sequence shows the principal stress wave as it starts, propagates, and finally peaks at the die corners. This sequence provides a clearer understanding of the stress mechanisms within the device for small and large die.

Similarly we are able to map out the stress wave propagation in the die attach solder material. Figure 8.74 shows a snapshot of the von Mises stress in the die attach solder material.

The von Mises stress from the die attach propagates directly into the die itself as can be seen in Fig. 8.75.

Below Fig. 8.76 plots the time evolution of the peak first principal stress in the die during the punch process. The model uses a lead frame failure strain of 5%.

During the studies the effect of the failure strain rate of the lead frame, and the effect of die size was also examined. Figure 8.77 shows the maximum first principal stress, S1, in the die for two different die sizes in two different lead frame designs.

For the smaller of the two die the data shows that we will exceed the die failure criteria if the failure strain rate of the lead frame exceeds 7%. For larger die, there is little concern for likely lead frame design/material to be used.

Figure 8.78 shows the first principal stress on die of 1.5 × 1.5 mm^2 MOSFET BGA with die tilt to 0.2 mil. The maximum die peak stress reaches to 729.7 MPa. As compared to the regular case in Fig. 8.76a in which the peak stress is 322 MPa, the first principal stress S1 in the case of tilted die has increases 126%. Therefore,

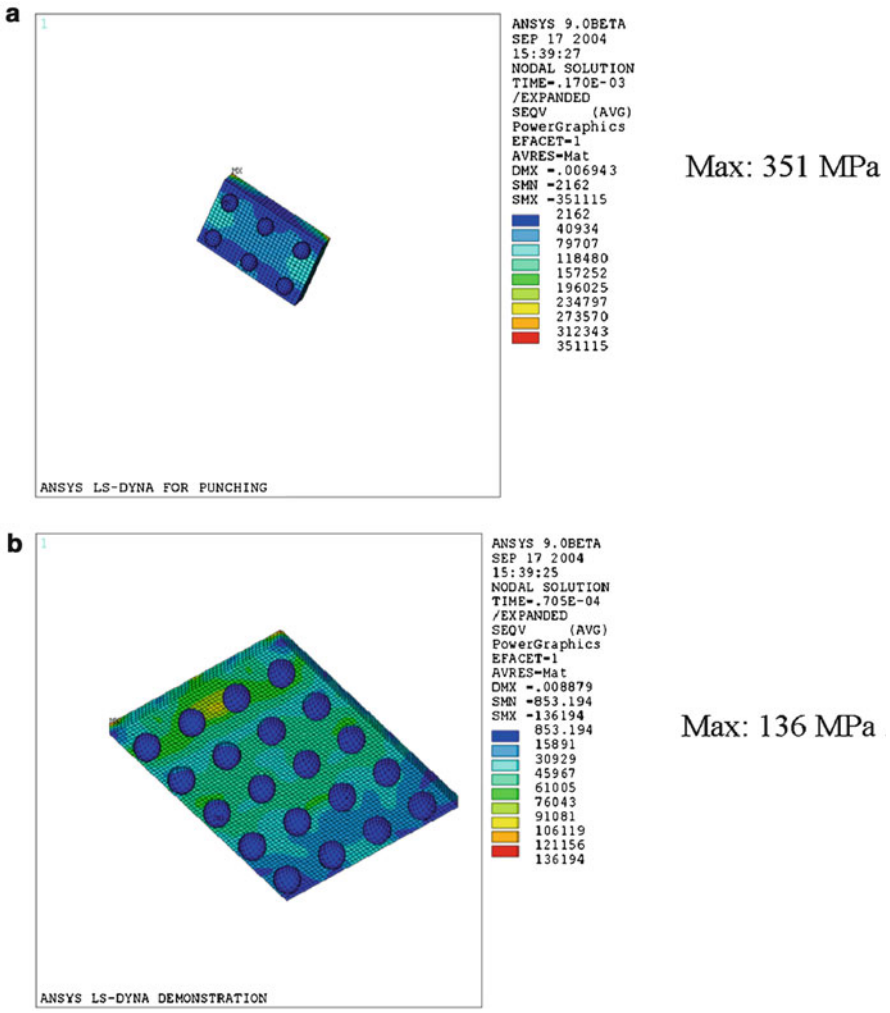


Fig. 8.72 The von Mises stress comparison of two MOSFET BGA designs in punch process. (**a**) von Mises stress of 1.5 × 1.5 mm^2 MOSFET BGA, (**b**) von Mises stress of 5 × 5 mm^2 MOSFET BGA

in the assembly process, controlling the die attach operation to avoid the die tilt is critical to reduce the die stress in punch process.

Figures 8.79 shows a design with precut grooves at lead frame and Fig. 8.80 shows the first principal stress in die, S1, with the grooves on the lead frame. As compared to the same peak stress without the groove (see Fig. 8.76a, peak stress S1: 322 MPa), it is significantly reduced by 45.6%. The simulation result shows a substantial beneficial effect of adding a groove to the lead frame.

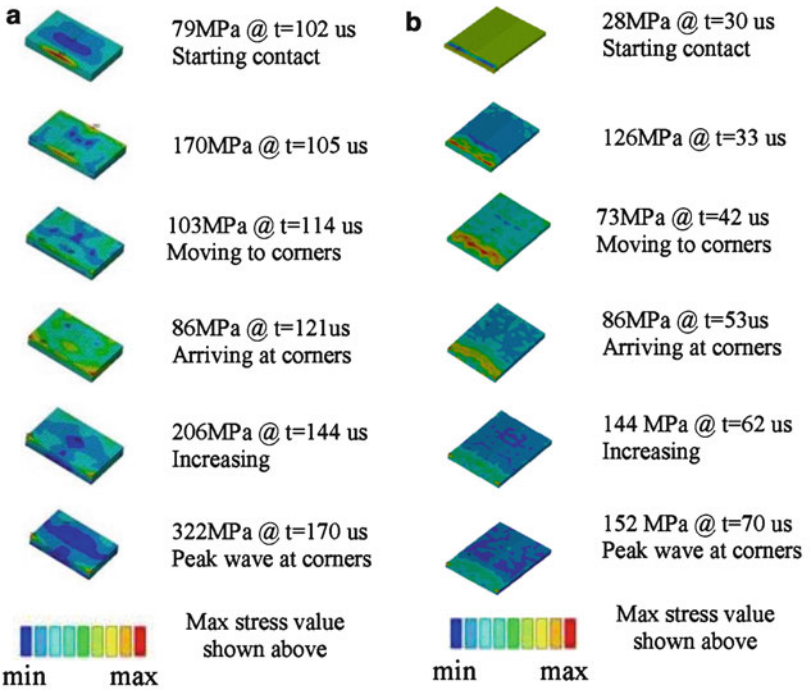


Fig. 8.73 Comparison of dynamic stress waves of two MOSFET BGA designs in punch process. (**a**) Principal stress S1 wave in die of 1.5 × 1.5 mm^2 MOSFET BGA, (**b**) principal stress S1 wave in die of 5 × 5 mm^2 MOSFET BGA

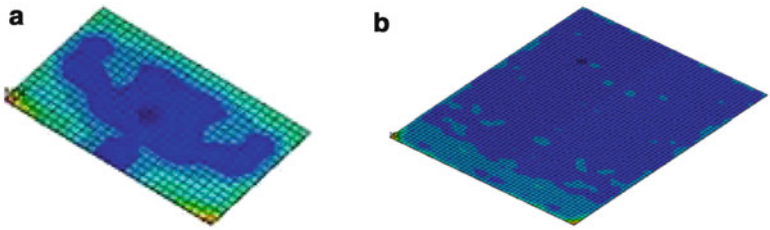


Fig. 8.74 The die attach von Mises stress distributions for two MOSFET BGA designs. (**a**) Die attach von Mises stress of 1.5 × 1.5 mm^2 MOSFET BGA, (**b**) die attach von Mises stress of 5 × 5 mm^2 MOSFET BGA

8.6.3 Experimental Data

In line experiments comparing grooved and ungrooved die were run to determine the efficacy of the grooved design. The test sample size consists of 1,280 units. Figure 8.81 below shows a good final unit. This unit is from the grooved sample set.

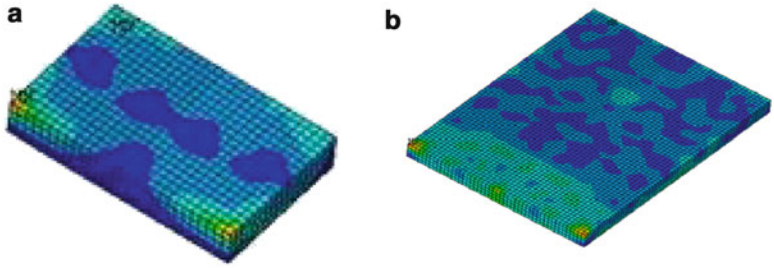


Fig. 8.75 The max von Mises stress distribution at the corners of the die: (**a**) 1.5 × 1.5 mm^2 MOSFET BGA, (**b**) 5 × 5 mm^2 MOSFET BGA

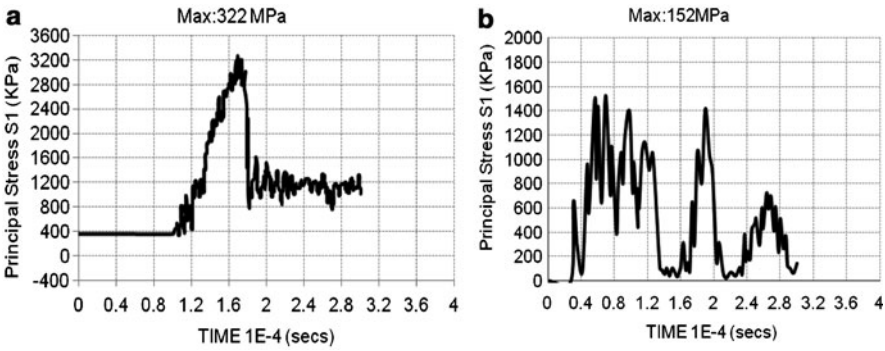


Fig. 8.76 The dynamic maximum first principal stress S1 vs. time with LFS = 5%. (**a**) 1.5 × 1.5 mm^2 MOSFET BGA, (**b**) 5 × 5 mm^2 MOSFET BGA

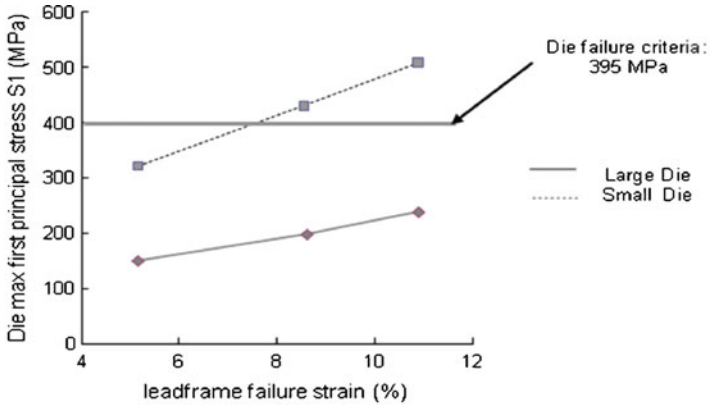


Fig. 8.77 First principal S1 in die vs. lead frame strain failure in 1.5 × 1.5 mm^2 (small die) and 5 × 5 mm^2 (large die) MOSFET BGA

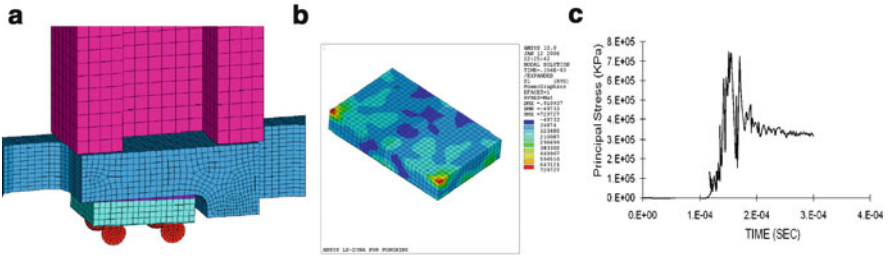


Fig. 8.78 The impact of die tilt of 1.5 × 1.5 mm^2 MOSFET BGA (Max S1 = 729.7 MPa). (**a**) Die tilt to 0.2 mil, (**b**) the first principal stress S1, (**c**) the dynamic curve of S1

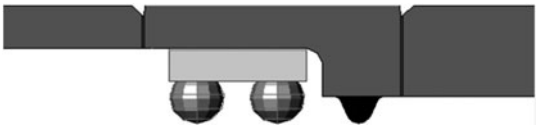


Fig. 8.79 MOSFET BGA with premade grooves at two sides of lead frame

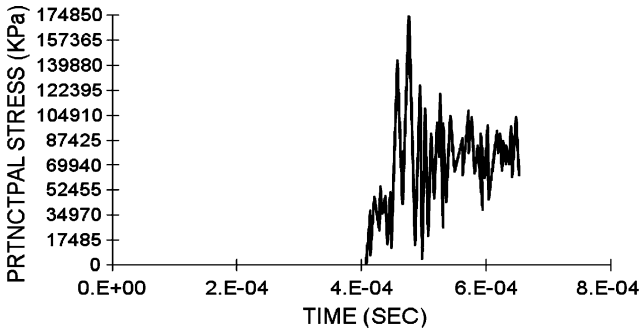


Fig. 8.80 The die first principal stress S1 vs. time (peak stress = 175 MPa)

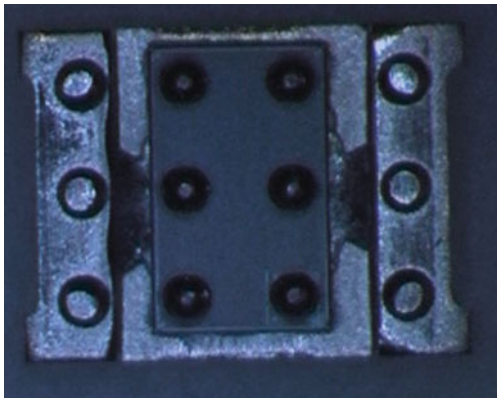


Fig. 8.81 Good die

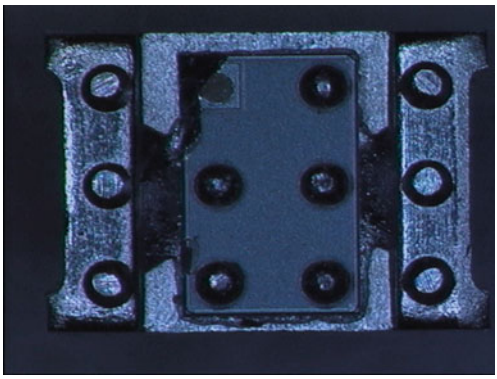


Fig. 8.82 Crack at die corner

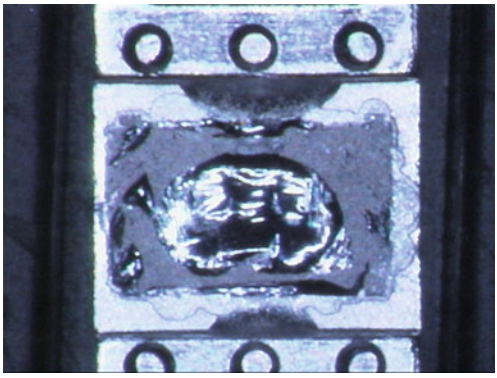


Fig. 8.83 Popped die

Two types of failure are seen with the ungrooved lead frames. These consist of cracked die, as is seen in Fig. 8.82, or package where the die has popped off due to cracking in the die attach material, as is seen in Fig. 8.83. Both pictures agree our modeling results that have shown highest stress at die corner area, as well as at die attach corner area.

The ungrooved lead frame packages displayed a failure rate of 3%. The grooved lead frame packages showed no failures.

The singulation process in the assembly of power packaging is a major operation step, there are a lot of factors needs to be carefully considered to avoid the package failure. From the modeling analysis, we may obtain the following:

1. Experimental data show a significant improvement in yield for packages built using a grooved lead frame, as predicted by the simulations.

2. The addition of a groove to the lead frame at the cut point is an effective aide to reducing the stress transmitted to the die and die attach.
3. There is an optimal depth and groove angle. The use of FEA techniques is useful in determining the optimum point. The use of FEA allowed the exploration of process improvements that would have been much more difficult to carry out experimentally.
4. In assembly process, controlling the die tilt to keep the uniform die attach thickness can significantly reduce the stress in the punch singulation.

8.7 Summary

This chapter presents the analysis for major power packaging assembly manufacturing processes in FOL and EOL.

The major FOL design and analysis include wafer handling, die pickup, die attach process, and wire bonding process. Transient dynamics modeling for die pickup process shows the stress distribution in the die so that the process can be optimized. A nonlinear material constitutive model is applied to the solder paste for the die attach process simulation. Wire bonding modeling method is used to simulate the ball bonding process with different capillary geometries, free air ball diameters and material behaviors, wire bonding substrate temperatures. The Wedge bonding optimization with different bond cross sections, bond lengths, and wire loop profiles for longer TMCL life is discussed.

In EOL, typical processes include molding process, molding ejection, and clamping process that can potentially cause cracking in molding compound, trim and form, and singulation process that would induce the stress wave to crack the die or the EMC. For the molding process simulation, material curing properties are the function of both time and temperature. Modeling can disclose the air tracks and the challenges of the EMC to fill the thin gap between EMC and lead frame in molding. For the molding ejection and clamping simulation, a 3D model is developed to show the stress at the power die that would induce the potential die failure in molding ejection process. Prior to trim and form, a clamping process is needed to flatten the lead frame due to warpage after molding. The simulation is applied to this process to make sure the clamping process will not damage the package. For the package Trim/Form/Singulation simulation, a 3D transient dynamic large deformation finite element method is used to determine what stresses are going to be induced while singulating the package, to check if the package can withstand punch stress waves and to determine potential design weaknesses. An effective method to reduce the punch stress on die is to make the recut grooves on lead frame. Also, control of the uniform die attach may avoid the larger stress induced by die tilt in the singulation process.

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Chapter 9
Power Packaging Typical Reliability and Test

Power semiconductors used in various high power electronics are exposed to different conditions as compared to plastic encapsulated package used for regular IC such as in the communication electronics. Controlling and converting high power simultaneously requires reliable control of both high voltage and high current. Control of electrical drives additionally results in frequent repetition of switch-on and switch-off processes that must meet special demands with respect to the internal mechanical design. While the low electrical losses occurring in components might be applied for communication electronics, these can be in the order of 100 W or higher power semiconductor components. These really considerable losses existing during the entire operation time of a converter must be dissipated to the environment by cooling surfaces. The semiconductors must be designed in the interior such as to withstand the continuously arising temperature gradients resulting from the losses in power cycling, and to satisfy various reliability tests in both component and board level.

9.1 Power Packaging Reliability and Test in General

This section introduces the general concepts of reliability life, failure rate, and typical reliability tests for power semiconductor packaging.

9.1.1 Reliability Life

According to the international standards, the term quality is defined as totality of characteristics of a power electronic product that bear on its ability to satisfy stated and implied needs. Reliability is the property of the power semiconductor to maintain all its functions during usage. Since it is not possible to determine the long range reliability of power semiconductor components prior to production

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release under realistic conditions, accelerated life tests must be applied which allow reliable results about the reliability of the components after a short test period. To achieve an acceleration effect, the reliability tests are carried out under greater stress than in application. According to the familiar failure rate curve (bathtub curve), we distinguish between early failures, random failures (failures with constant failure rate), and failures resulting from wear-out and fatigue. While applying a so-called "burn-in" for integrated circuits to catch early failures prior to the final application, this does not make sense for power semiconductors because of substantial higher costs. Provided that there is no misapplication caused by the user, early failures must be avoided by complete control and mastery of the manufacturing processes. Excluding short time overload during operation random failures are determined by reproducibility and safety margins of the manufacturing parameters. The early design phase of a product already decides about failures caused by wear-out and fatigue designing parts and processes and selecting the material.

9.1.2 Failure Rate

It is difficult to find a distribution function which will allow the whole bathtub curve. However, for each section of it, the Weibull distribution is applicable.

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right] \tag{9.1}$$

where

$F(t)$: probability that the device fails in the interval [0, t]
η: characteristic life
β: shape parameter
t: time; number of cycles

From this equation follows the failure rate (hazard function):

$$\lambda(t) = (\beta/\eta^{\beta}) \cdot t^{\beta-1} \tag{9.2}$$

The shape parameter means:

$\beta = 1$ constant failure rate (random failures)
$\beta < 1$ decreasing failure rate (early failures)
$\beta > 1$ increasing failure rate (wear-out, fatigue)

(a) Random failures
In terms of electrical failures usually the shape parameter $\beta = 1$ is applicable. This particular Weibull distribution then is called Exponential distribution

$$F(t) = 1 - \exp(-\lambda \cdot t) \tag{9.3}$$

where $\lambda = 1/\text{MTTF}$ the constant failure rate.

Failure rate often is estimated by experiment using the formula

$$\lambda = r/(n \cdot t) \tag{9.4}$$

where

r: number of failures
n: sample size
t: test time
MTTF: Mean time to failures, time in which 62.3% of devices failed

Because of statistical nature of this number an extended formula takes into account a confidence limit—Upper Confidence Limit (UCL) = 60% which is the common value. Moreover, it is possible to calculate reliability data by computer models. The available computer models, however, have not been developed for power semiconductors. The failure rate model according to MIL-HDBK 217 serves therefore for the time being only as a rough estimate.

$$\lambda[\mathrm{FIT}] = [(r + \Delta r)/(n \cdot t)] \times 10^9 \tag{9.5}$$

where Δr is the depending on confidence limit and number of failures; FIT is the failures in time.
Constant failure rates allow reliability prediction by using an acceleration factor. This acceleration factor is calculated by means of the Arrhenius equation:

$$a_\mathrm{f} = \exp\{E_\mathrm{a} \cdot [T2 - T1/(T1 \cdot T2)]/k\} \tag{9.6}$$

where

E_a: activation energy
k: Boltzmann's constant $k = 8.6 \times 10^{-5}$ eV/K
$T1$: absolute application junction temperature (K)
$T2$: absolute test junction temperature (K)

The above mentioned acceleration factor is applicable at constant temperature. In case of temperature differences (temperature cycle [TMCL], power cycle [PRCL]), other formulas have to be used.
To estimate life times for different ΔT frequently the Manson–Coffin relation is used which has been established originally for metals under low cycle plastic deformation. If plastic strain dominates, then

$$\mathrm{Nf} \approx C \cdot (\Delta T)^{-n} \tag{9.7}$$

where

Nf: number of cycles to failure
ΔT: temperature difference
C: A material dependent constant
n: an experimentally determined constant

An extended life prediction may be obtained through finite element analysis for the estimated life for thermal cycling and power cycling in Sect. 9.2.

(b) Early failures
Constant failure rate allows simple computation and prediction of life. In the regime of early failures, prediction of failure rate is a challenge and failure rate is strongly time dependent.

(c) Wear-out
Power semiconductors rarely come up to fatigue or wear-out. Even accelerated tests take a long time to show this. Usually, reliability tests are stopped at a time or number of cycles far from the fatigue.

9.1.3 Typical Reliability Tests for Power Package

Typical reliability tests used for power packages include

1. *Solder reflow preconditioning* (*PRECON*): The preconditioning stress sequence is performed for the purpose of evaluating the capability of semiconductor devices to withstand the stresses imposed by a user's printed circuit board assembly operation. A properly designed device (i.e., die and package combination) should survive this preconditioning sequence with no measurable changes in electrical performance. Furthermore, preconditioning of properly designed devices should not produce latent defects which lead to degraded reliability during life or environmental stress tests. Changes in electrical characteristics and both observable as well as latent physical damage during this stress sequence result principally from mechanical and thermal stresses and from ingress of flux and cleaning agents. Effects include die and package cracks, fractured wire bonds, package and lead frame delamination, and corrosion of die metallization. The preconditioning stress condition is listed in Table 9.1.
2. *Operating life* (*SOPL/DOPL*): The operating life test is performed for the purpose of demonstrating the quality and reliability of devices subjected to the specified conditions over an extended time period. Either a static or dynamic condition may be used, depending on the circuit type and the wafer fabrication technology. The specified test conditions (i.e., bias conditions, loads, clock inputs, etc.) are selected so as to represent the worst case conditions for the device. Unless otherwise specified in the detailed test procedure, the test is run at an ambient temperature of +125°C or above. Many device types are routinely run at +150°C ambient. Ambient temperatures above +170°C are generally considered impractical due to the physical limitations of circuit boards, sockets, device lead finishes, molding compound glass transition temperatures, etc.

Stress conditions	125–150°C, bias
Reference Industry Standard	JESD22-A108B [2]

Table 9.1 Preconditioning stress conditions

Step	Stress	Conditions
1	Initial electrical test	Room temperature
2	External visual inspection	40× magnification
3	Temperature cycling	5 cycles at −40°C (max) to +60°C (min) (step is optional)
4	Bake out	24 h (min) at 125°C
5	Moisture soak	Per MSL rating
6	Reflow	3 cycles per referenced profile
7	Flux application	10 s immersion in water soluble flux at room temp
8	Cleaning	Multiple DI water rinses
9	Dry	Room temperature
10	Final electrical test	Room temperature

Reference Industry Standard: JESD22-A113C [1]

Table 9.2 Package size classification

		Package volume (mm^3)		
		<350	350–2,000	>2,000
Package thickness	<1.6 mm	Small	Small	Small
	1.6–2.5 mm	Small	Medium	Large
	>2.5 mm	Medium	Large	Large

3. *Power cycle* (*PRCL*): The PRCL test is performed to determine the effects on solid-state devices of thousands of power-on/power-off operations such as would be encountered in an automobile or a TV set. The repetitive heating/cooling effect caused by multiple on/off cycles can lead to fatigue cracks and other degrading thermal and/or electrical changes in devices which generate significant internal thermal heating under maximum load conditions (i.e., voltage regulators or high-current drivers). This test forces junction temperature excursions at the rate of ~30 cycles per hour (typical for small packages). The power cycling stress conditions are shown in Tables 9.2–9.4.

Stress conditions	$\Delta T_J = 100$ or 125°C, on/off cycle dependent on package size

4. *High temperature reverse bias test* (*HTRB*): The HTRB test is configured to reverse bias major power handling junctions of the device samples. The devices are characteristically operated in a static operating mode at, or near, maximum-rated breakdown voltage and/or current levels. The particular bias conditions should be determined to bias the maximum number of solid-state junctions in the device. The HTRB test is typically applied on power devices.

Stress conditions	150°C T_J, biased
Reference Industry Standard	JESD22-A108B [2]

Table 9.3 On/off time

		$\Delta T_J = 100°C$	$\Delta T_J = 125°C$
Package size	Small	2 min on/2 min off	2 min on/2 min off
	Medium	3.5 min on/3.5 min off	3.5 min on/3.5 min off
	Large	5 min on/5 min off	5 min on/5 min off

Table 9.4 Number of cycles required

		$\Delta T_J = 100°C$	$\Delta T_J = 125°C$
Package size	Small	10,000	7,500
	Medium	8,572	4,286
	Large	6,000	3,000
	General	60,000/(on time + off time)	30,000/(on time + off time)

Reference Industry Standard: JESD22-A122 [3]

5. *High temperature gate bias test* (*HTGB*): The HTGB test biases gate or other oxides of the device samples. The devices are normally operated in a static mode at, or near, maximum-rated oxide breakdown voltage levels. The particular bias conditions should be determined to bias the maximum number of gates in the device. The HTGB test is typically used for power devices.

Stress conditions	150°C T_J, biased
Reference Industry Standard	JESD22-A108B [2]

6. *Temperature humidity biased test* (*THBT*): The steady-state temperature–humidity–bias life test is performed for the purpose of evaluating the reliability of nonhermetic packaged devices operating in humid environments. It employs severe conditions of temperature, humidity, and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective materials and the metallic conductors passing through it. When moisture reaches the surface of the die, the applied potential forms an electrolytic cell, which can corrode the aluminum, affecting DC parameters through its conduction, and eventually causes catastrophic failure by opening the metal. The presence of contaminants such as chlorine greatly accelerates the reaction as does excessive phosphorus in the PSG layers (passivation, dielectric or field oxide).

Stress conditions	85%RH, 85°C
Reference Industry Standard	JESD22-A101B [4]

7. *Highly accelerated stress test* (*HAST*): HAST is performed for the purpose of evaluating the moisture resistance of nonhermetic packaged devices operating in high humidity environments. Bias is applied minimizing current draw using alternating potentials wherever possible. The test approximates a highly

accelerated version of the THBT test. These severe conditions of pressure, humidity, and temperature, together with bias, accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors passing through it. When moisture reaches the surface of the die, the applied potential forms an electrolytic cell, which can corrode the aluminum, affecting DC parameters through its conduction, and eventually causes catastrophic failure by opening the metal. The presence of contaminants such as chlorine greatly accelerates the reaction as does excessive phosphorus in the PSG layers (passivation, dielectric or field oxide).

Care must be taken when using HAST as a stress technique for assembly packages that have mold compound and die attach materials with low T_g, since uncharacteristic failures may result.

Stress conditions	130°C, 85%RH, 18.6 psig or 110°C, 85%RH, 3 psig
Reference Industry Standard	JESD22-A110B [5]

8. *Autoclave* (*ACLV*): The ACLV (or pressure cooker) test is performed for the purpose of evaluating the moisture resistance of nonhermetic packaged devices. No bias is applied to the devices during this test. It employs severe conditions of pressure, humidity, and temperature not typical of actual operating environments that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors passing through it. When moisture reaches the surface of the die, reactive agents cause leakage paths on the surface of the die and corrode the die metallization, affecting DC parameters and eventually catastrophic failure. Other die-related failure mechanisms are activated by this method including mobile ionic contamination and various temperature and moisture related phenomena.

   The ACLV test is destructive and produces increasing failure rates when repetitively applied. It is useful for short-term, comparative evaluations such as lot acceptance, process monitors, and robustness characterization, but generates no absolute information, since accelerating factors relating to the operating environment are not well established. In addition, the ACLV test can produce spurious failures not representative of device reliability, due to excessive chamber contaminants. This condition is usually evidenced by severe external package degradation, including corroded device terminals/leads or the formation of conducting matter between the terminals, or both. The ACLV test is therefore not suitable for measurements of package quality or reliability.

   ACLV test is not required in the qualification of standard Fairchild products. However, during the development stages of a package ACLV can be used to understand inherent weakness in the technology. Cautions must be taken when interpreting results because failure mechanisms may be due to exceeding the

capabilities of the package, producing unrealistic material failures. ACLV may be a required test for some customers or markets, such as the automotive market.

Stress conditions	100%RH, 121°C, 15 psig
Reference Industry Standard	JESD22-A102C [6]

9. *Temperature cycle* (*TMCL*): The TMCL test is conducted for the purpose of determining the resistance of devices to alternating exposures at extremes of high and low temperatures. Permanent changes in electrical characteristics and physical damage produced during temperature cycling result principally from mechanical stress caused by thermal expansion and contraction. Effects of temperature cycling include cracking and delamination of packages, cracking or cratering of die, cracking of passivation, delamination of metallization, and various other changes in the electrical characteristics resulting from thermomechanically induced damage.

Stress conditions	Various. −40 to +125°C or −65 to +150°C are typical
Reference Industry Standard	JESD22-A104D [7]

10. *Board level temperature cycle* (*BTMCL*): The BTMCL test is intended to provide fatigue-related wear-out information on the solder joint attachment of devices to circuit boards. Daisy chain structure test devices are mounted to circuit boards and cycled through temperature extremes typically in the range of 0 to +100°C. During stress, the solder joint resistance is continuously monitored and a unit is considering failing when five cumulative incidences of elevated resistance (>1,000 Ω) are detected. Ideally, testing should continue until a cumulative 63% failure rate of the test sample has been observed.

Stress conditions	0 to +100°C, 2 cycles/h
Reference Industry Standard	IPC-SM-785 [8]

11. *High temperature storage life* (*HTSL*): The high temperature storage (also called the stabilization bake test) is employed for the purpose of determining the effects of storing devices at elevated temperatures without electrical stresses applied. It is also a useful test for determining the long term reliability of wire bonds which are susceptible to formation of intermetallic voids (such as gold wire bonds on aluminum bond pads).

    Devices under test are subjected to continuous storage in a chamber with circulated air heated to +150°C. At the end of the specified stress period, the devices are removed from the chamber, allowed to cool, and electrically tested. Interim measurements are made if specified in the detailed test procedure.

Stress conditions	150 or 175°C
Reference Industry Standard	JESD22-A103B [9]

12. *Reflow moisture sensitivity* (*MSL*): The purpose of this stress is to classify the sensitivity of nonhermetic solid-state Surface Mount Devices (SMDs) to

Table 9.5 Reflow MSL stress conditions

Step	Stress	Conditions
1	Initial electrical test	Per data sheet
2	External visual inspection	40× magnification
3	CSAM inspection	Classify and measure initial delamination levels
4	Bake out	24 h (min) at 125°C
5	Moisture soak	Per target MSL rating
6	Reflow	3 cycles per referenced profile
7	External visual inspection	40× magnification
8	Final electrical test	Per data sheet
9	CSAM inspection	Classify and measure final delamination levels
10	Final electrical test	Room temperature

Reference Industry Standard: J-STD-020C [10]

moisture-induced stress so that they can be properly packaged, stored, and handled to avoid subsequent thermal/mechanical damage during the assembly solder reflow attachment and/or repair operation. Table 9.5 lists the Reflow MSL condition.

13. *Resistance to solder heat* (*RSDH*): The RSDH test is intended to determine whether devices can withstand the effects of the heat to which they will be subjected during soldering of their terminations. The heat can be conducted through the termination into the device package, radiated from the solder bath to the body of the device, or through direct contact with the solder wave. In order to establish a standard test procedure for the most reproducible method, the solder dip method is used because of its more controllable conditions.

    During this procedure, through hole devices under test have their leads immersed in a solder bath heated to 260°C (SnPb processing) or 270°C (Pb-free processing) for a duration of 10 s. The devices are then cooled and tested. Endpoint measurements include electrical testing as well as visual inspection for mechanical damage such as cracks, etc.

    Small surface mount products (typically those with packages $<5.5 \times 12.5$ mm and DAP $<2.5 \times 3.5$ mm) must be fully submerged in the solder bath for a minimum of 5 s. It is recommended to preheat the samples prior to solder immersion at a rate of less than 4°C/s to a maximum preheat temperature of 140°C. Care should be taken to fully investigate any failures that occur on products that are not preheated, as the severe shock of solder immersion without preheating can overstress the package.

RSDH stress conditions	260°C, 10 s (through hole products in a SnPb board assembly process) 270°C, 10 s (through hole products in a Pb-free board assembly process) 260°C, 5 s (surface mount products in a SnPb board assembly process) 270°C, 5 s (surface mount products in a Pb-free board assembly process)
Reference Industry Standard	JESD22-B106C [11]

14. *Lead integrity*: The lead integrity test provides various methods for determining the integrity of device leads, welds, and seals. For hermetic packaged devices only, this test is followed by a hermeticity test to determine any effect of the stresses applied on the seal as well as on the leads.

    Devices under test are subjected to one or more mechanical stress sequences (tension, bending, fatigue, or torque) appropriate to the type of leads on the package.

Reference Industry Standard	JESD22-B105B [12]

15. *Mark permanency*: The purpose of the mark permanency or resistance to solvents test is to verify that the markings on the device package will not become illegible when subjected to solvents or cleaning solutions commonly used for removing flux residue from printed circuit boards.

    Devices under test are exposed to a series of solvents while the markings are brushed with a toothbrush. The markings must not become illegible as a result of the exposure.

    This test is not required for laser marked packages.

Reference Industry Standard	JESD22-B107A [13]

16. *Flammability*: This procedure assesses the flammability of the plastic materials used in the assembly of the packaged semiconductor device. This testing is not performed internal to Fairchild Semiconductor. Instead, a certificate of compliance to the UL94 test standard is required for the plastic materials used in semiconductor package. This should be obtained from the mold compound or resin supplier or from Underwriters Laboratories directly.

Reference Industry Standard	UL94 [14]

17. *Solderability*: The purpose of the solderability test is to determine the solderability of all external package terminations that are normally joined by a soldering operation. This determination is made on the basis of the ability of these terminations to be wetted or coated by solder. These procedures will verify that the treatment used in the manufacturing process to facilitate the soldering is satisfactory and that it has been applied to the required portion of the part which is designed to accommodate a solder connection. An accelerated aging test is included in this test method.

    The referenced standard also provides optional conditions for aging and soldering for the purpose of allowing simulation of the soldering process to be used in the device applications. It provides procedures for dip and look solderability testing of through hole, axial and SMDs and reflow simulated use testing for surface mount packages.

Table 9.6 WMSL stress conditions

Step	Stress	Conditions
1	Initial electrical test	Room temperature
2	External visual inspection	40× magnification
3	CSAM inspection	Classify and measure initial delamination levels
4	Bake out	24 h (min) at 125°C
5	Moisture soak	Per target MSL rating
	Preheat	Room temp to 140°C in minimum of 80 s
6	Solder immersion	1 full immersion, 10 s minimum
		260°C for SnPb board assembly processes
		270°C for Pb-free board assembly processes
7	External visual inspection	40× magnification
8	Final electrical test	Per data sheet
9	CSAM inspection	Classify and measure final delamination levels
10	Final electrical test	Room temperature

Reference Industry Standard: JESD22A-111 [16]

Using the dip and look procedure, devices under test are first "aged" by exposure to steam for a period of 8 h. After aging the leads of the device are fluxed and dipped in a solder bath heated to a temperature of 215°C (SnPb board assembly processing) or 245°C (Pb-free board assembly processing) for 5 s.

Reference Industry Standard	JESD22-B102C [15]

18. *Wave solder moisture sensitivity* (*WMSL*): The purpose of this stress is to classify the sensitivity of nonhermetic solid-state SMDs to moisture-induced stress resulting from a full immersion wave solder board mounting process so that they can be properly packaged, stored, and handled to avoid subsequent thermal/mechanical damage during the assembly solder reflow attachment and/or repair operation. The wave solder MSL stress condition is listed in Table 9.6.
19. *Solder immersion preconditioning* (*WVSLDR*): The WVSLDR stress sequence is performed for the purpose of evaluating the capability of semiconductor devices to withstand the stresses imposed by a user's waver solder printed circuit board assembly operation. In this type of board assembly process it is common for small surface mount products to be glued to the back side of a board and be completely immersed in the solder wave at the same time that the through hole parts on the top side of the boards are solder with the wave. The solder temperature will be 260°C for SnPb board assembly processes and 270°C for Pb-free board assembly processes.

    A properly designed device (i.e., die and package combination) should survive this preconditioning sequence with no measurable changes in electrical performance. Furthermore, preconditioning of properly designed devices should not produce latent defects which lead to degraded reliability during life or environmental stress tests. Changes in electrical characteristics and both observable as well as latent physical damage during this stress sequence result principally from mechanical and thermal stresses and from ingress of flux and

Table 9.7 WVSLDR stress conditions

Step	Stress	Conditions
1	Initial electrical test	Room temperature
2	External visual inspection	40× magnification
3	Temperature cycling	5 cycles at −40°C (max) to +60°C (min) (step is optional)
4	Bake out	24 h (min) at 125°C
5	Moisture soak	Per MSL rating
6	Preheat	Room temp to 140°C in minimum of 80 s
7	Solder immersion	1 full immersion, 10 s minimum
8	Flux application	10 s immersion in water soluble flux at room temp
9	Cleaning	Multiple DI water rinses
10	Dry	Room temperature
11	Final electrical test	Room temperature

Reference Industry Standard: JESD22A-111 [16]

cleaning agents. Effects include die and package cracks, fractured wire bonds, package and lead frame delamination, and corrosion of die metallization. The test stress condition is given in Table 9.7.

20. *Board level drop test*: This test is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment, where excessive flexure of a circuit board causes product failure. It is particularly applied to the power MOSFET wafer level chip scale package (WL-CSP).

    Experience with different board orientation has suggested that the horizontal board orientation with components facing down results in maximum PCB flexure and, thus, the worst orientation for failures. Therefore, it requires that the board shall be horizontal in orientation with components facing in downward direction during the test. Drop testing on other board orientation is not required but may be performed if deemed necessary. However, this is an additional test option and not a replacement for testing in required orientation.

    Drop test requires JEDEC Condition B (1,500 Gs, 0.5 ms duration, half-sine pulse), as listed in JESD22-B111 or in JESD22-B104-B, as the input shock pulse to the printed circuit assembly. This is the applied shock pulse to the base plate and shall be measured by accelerometer mounted at the center of base plate or close to the support posts for the board. Other shock conditions, such as Condition H (2,900 Gs, 0.3 ms duration), in addition to the required condition can also be used. In situ electrical monitoring of daisy chain nets for failure is required during each drop. The electrical continuity of all nets should either be detected by an event detector or by a high-speed data acquisition system. The event detector should be able to detect any intermittent discontinuity of resistance greater than 1,000 Ω lasting for 1 μs or longer. The high-speed data acquisition system should be able to measure resistance with a sampling rate of 50,000 samples per second or greater.

Reference Industry Standard	JESD22-B111 [17]

9.2 Power and Thermal Cycling

This section discusses the reliability test of electronic package in power cycling, thermal cycling, and solder joint fatigue life prediction. A nonlinear material model for die attach solder material is introduced, and an advanced finite element methodology is developed to target the coupled thermal-mechanical problem. For power cycling, a transient thermal analysis is presented, that will show the thermal propagation as the power turned on and off, and the resulting temperature gradients. Then we use the cyclic transient temperature loads to apply to the model for the nonlinear cycle stress analysis. For thermal cycling, the cycle temperature is directly applied to the model. The detail study regarding the solder joint stress loops and the fatigue with and without the underfill is conducted. The discussion and correlation with experimental data and actually process induced cracking are presented. This section also discusses the impact of process on the reliability of package, such as impact of die attach process of power package, clean and nonclean process for flip chip solder joints.

9.2.1 Background

Power cycling and thermal cycling are critical reliability tests for power semiconductor packages, intended to detect problems that may cause thermal-mechanical and electrical failures. Power cycling simulation consists of: (1) a transient thermal simulation resulting from die power cycling—with the heat source being the transistor device at silicon die in this package. (2) A nonlinear mechanical stress simulation for the preceding assembly process, where the transient thermal simulation results provide the thermal loads. In contrast, in thermal cycling tests, the thermal load is considered as a uniform load that is applied to the whole device. There are many papers that have demonstrated solder joint reliability and life prediction by different nonlinear material constitutive relationships, Darveaux and Mawer [18] published thermal and power cycling limits for plastic BGA. Ham et al. [19] compared power cycling simulation to Moire interferometry measurements results, and the deformation agreed well with finite element predictions. Syed [20] gave the predicting methodology within 25% accuracy for solder joint reliability in thermal, power, and bend cycles. However, few works have shown the impact of assembly process on package power cycling and thermal cycling, such as the process variations inherent in die attachment.

This section investigates the impact of die attach process on the power cycling and thermal cycling for a discrete style TO220 package [21]. The goal is to study the potential risk on die and bond line in PRCL and TMCL. A typical die tilt model is presented based on the observation of an actual die attach process. A nonlinear model for die attach solder material is introduced, and an advanced nonlinear FEA methodology is developed to target the thermal-mechanical coupled problem.

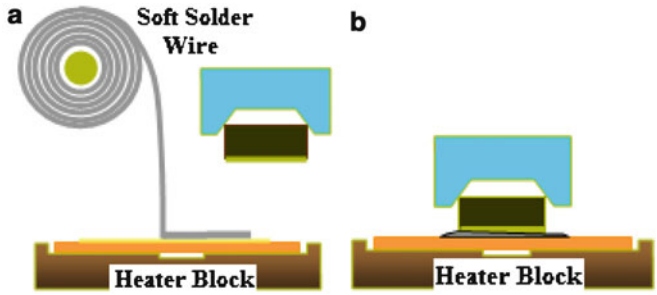


Fig. 9.1 Eutectic solder die attach process. (**a**) Wire melting. (**b**) Die attaching

For power cycling, the transient thermal analysis is presented, which will show the thermal propagation as the power turned on and off, and the resulting temperature gradients, then we use the cyclic transient temperature loads to apply to the model for the nonlinear cycle stress analysis. For thermal cycling, the cycle temperature is directly applied to the model. A parametric study for different die size and thicknesses, with the die tilt due to the die attach process is conducted and discussed. From the study, we will have a better understanding of the root causes of how the assembly die attach process impacts the power cycling/thermal cycling failure, which will help to identify potential controls to improve the assembly reliability.

9.2.2 Die Attach Process and Material Relations

Typical eutectic die attach process is shown in Fig. 9.1.

A die pickup head with cavity picks the die with bottom metallization. A lead frame is held on the surface of heater block. The soft solder wire is then placed on the lead frame. The temperature of heater block ramps up to the melting temperature of solder wire that makes the wire fuse. Finally the die pickup head moves the die to the melt solder in the lead frame. The die attach process, if in an improper assembly operation, might induce different bond line thicknesses or make the die tilt. Figure 9.2 shows one a worst case tilted die example due to the die attach process and the 3D model (hiding the EMC) of a typical TO220 package.

In order to better describe the behavior of die attach solder material under a cyclic thermal load, the Anand model that includes a sinh function model and an evolution equation is adopted (Brown et al. [22], and Sect. 7.5.2 in Chap. 7):

$$\frac{d\varepsilon_{vp}}{dt} = A[\sinh(\xi\sigma/s)]^{1/m} \exp\left(\frac{-Q}{kT}\right) \tag{9.8}$$

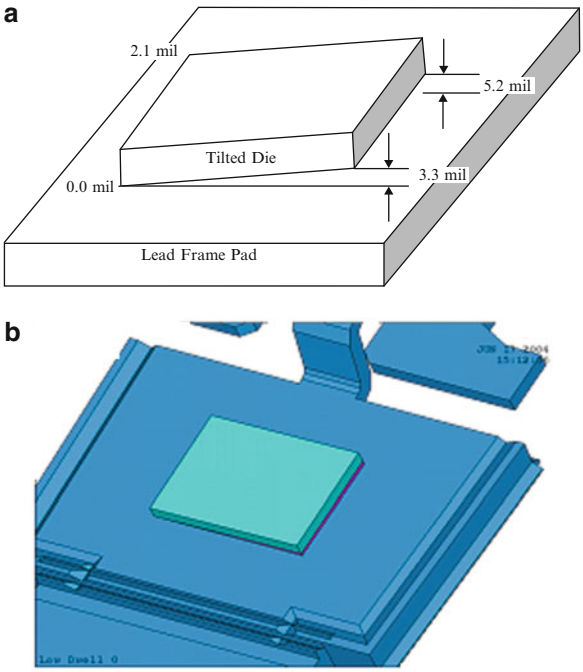


Fig. 9.2 Tilted die due to die attach process. (**a**) A tilted die. (**b**) 3D model of die attach and tilted die

or, it can be written as

$$f_{\text{ANAND}} = \bar{\sigma} = \frac{s}{\xi}\sinh^{-1}\left(\frac{\dot{\varepsilon}_{\text{vp}}}{A}\exp\left(\frac{Q}{kT}\right)\right)^{m} \tag{9.9}$$

where the evolution equation,

$$\frac{\mathrm{d}s}{\mathrm{d}t} = \left\{h_0\left(\left|1 - \frac{s}{s^*}\right|\right)\right\}^{a}\operatorname{sign}\left(1 - \frac{s}{s^*}\right)\frac{\mathrm{d}\varepsilon_{\text{vp}}}{\mathrm{d}t} \tag{9.10}$$

and,

$$s^* = \hat{s}\left[\frac{\mathrm{d}\varepsilon_{\text{vp}}/\mathrm{d}t}{A}\exp\left(\frac{Q}{RT}\right)\right]^{n} \tag{9.11}$$

where the die attach solder material used in this paper is 92.5Pb5Sn2.5Ag, the related material constants for above (9.8)–(9.11) are: $Q/R = 11{,}935$ (K) which stands for the ratio of activation energy Q and the gas constant R; $A = 3.785\text{e}7$ (1/s) which is a preexponential factor; $\xi = 5.91$ means a multiplier of stress;

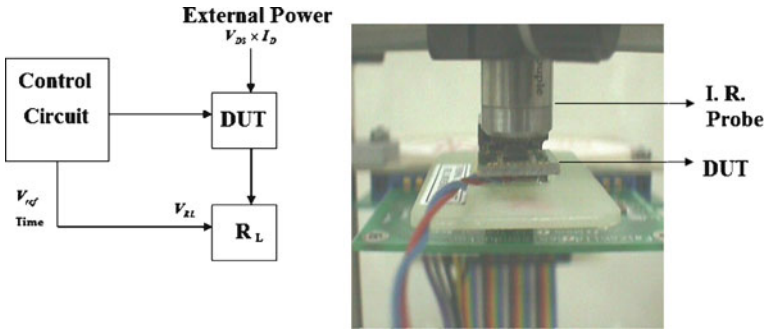


Fig. 9.3 Simplified block diagram of PRCL circuitry

$m = 0.143$ is the strain rate sensitivity index of stress; $h_0 = 1{,}379$ (MPa) is the hardening/softening constant; $\hat{s} = 9.79$ (MPa) is the coefficient for deformation resistance saturation value; $n = 0.07$, is the strain rate sensitivity index of deformation resistance; $a = 1.3$ is the strain rate sensitivity of hardening/softening.

9.2.3 Power Cycling Modeling and Discussion

A simplified block diagram of the PRCL circuitry is shown in Fig. 9.3. The device is powered by an external DC power supply. A resistor (RL) is connected in series with the DUT. A control circuit monitors certain predefined parameters and actively participates in the power cycling process. These predefined parameters are the heating power, on/off time durations and reference voltage (V_{ref}) which are manually set before running the test.

Figure 9.4a shows the power cycling due to the power on 2 min and off 2 min. This will be the input for the package modeling. Because the heat source is caused by the current going though the die, this will induce the gradient of temperature distribution by on/off load condition in the package, which is different from the thermal cycle where the temperature will be applied as a uniform loading. Figure 9.4b shows test TMCL. Figure 9.5 gives the 3D model and mesh of TO220 package. The power is applied in such that the junction temperature of package in PRCL will be about 125°C (Mid-STD-7500 Method 1037.2).

Figure 9.4 gives the temperature distribution of a typical PRCL, it shows the transient temperature change in a cycle from the thermal model. These transient temperature results at all nodes of the model are saved in a database which then is used as the temperature load to be applied to the thermal-mechanical model for PRCL stress simulation. Four cycles are used in the simulation. The PRCL stress results are shown in Figs. 9.6–9.10 and Tables 9.8 and 9.9. Figure 9.7 shows the von Mises stress distribution inside the package (hiding the EMC) when power is off 2 min, the max stress appears at the smallest case with largest die thickness. Figure 9.8 shows the first principal stress with different die size and thickness.

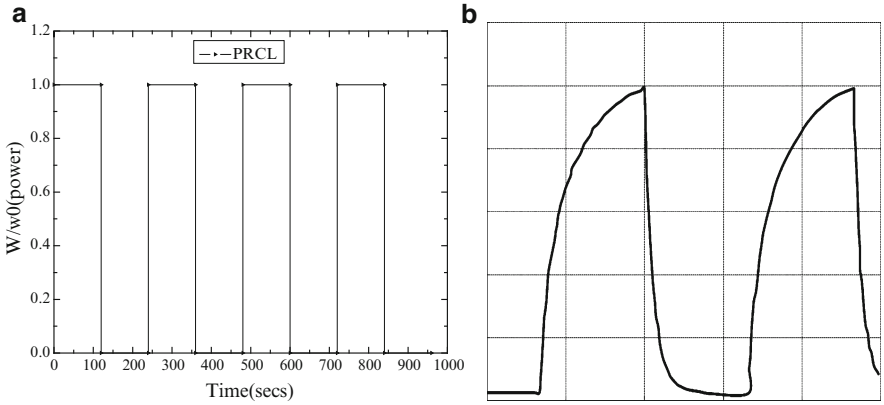


Fig. 9.4 Power cycles (2 min on and 2 min off). (**a**) Power on/off. (**b**) Temperature curve

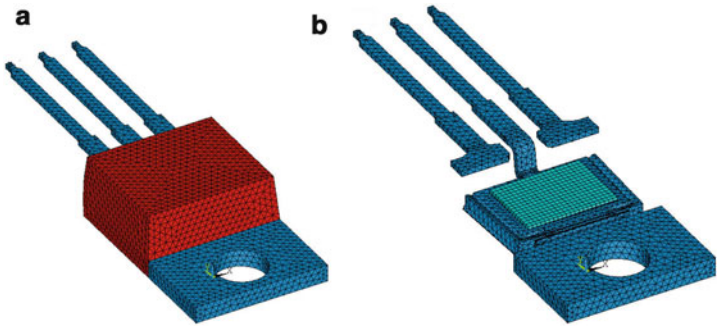


Fig. 9.5 TO 220 model and mesh. (**a**) Meshed model. (**b**) Hide the EMC

From Fig. 9.8 it may be seen that the max stress locates at the point of die that has contacted the pad due to tilt. Table 9.8 gives the comparison of first and third principal stress, max shear stress, and von Mises stress. It shows that most of the die is in compressive stress status, the greatest von Mises stress, third principal stress, and shear stress appear at the smallest size die with biggest die thickness. Figures 9.9 and 9.10 show the von Mises stress distribution of die attach and the loops of effective stress–strain. Table 9.9 gives the comparison of effective strain, von Mises stress, and the plastic strain energy density. The results show that the largest effective strain and stress appears in the die attach material for the largest die size. It locates at the point that die has contacted the pad (BLT = 0.0) due to tilted die. The tensile strength of die attach material 92.5Pb5Sn2.5Ag is about 30 MPa and failure strain is 0.4 based on Vendor's test data. Although the die attach von Mises stress is lower than the tensile strength, after many cycles if the effective strain is accumulated to a value that is higher than the failure strain, the die attach will fracture.

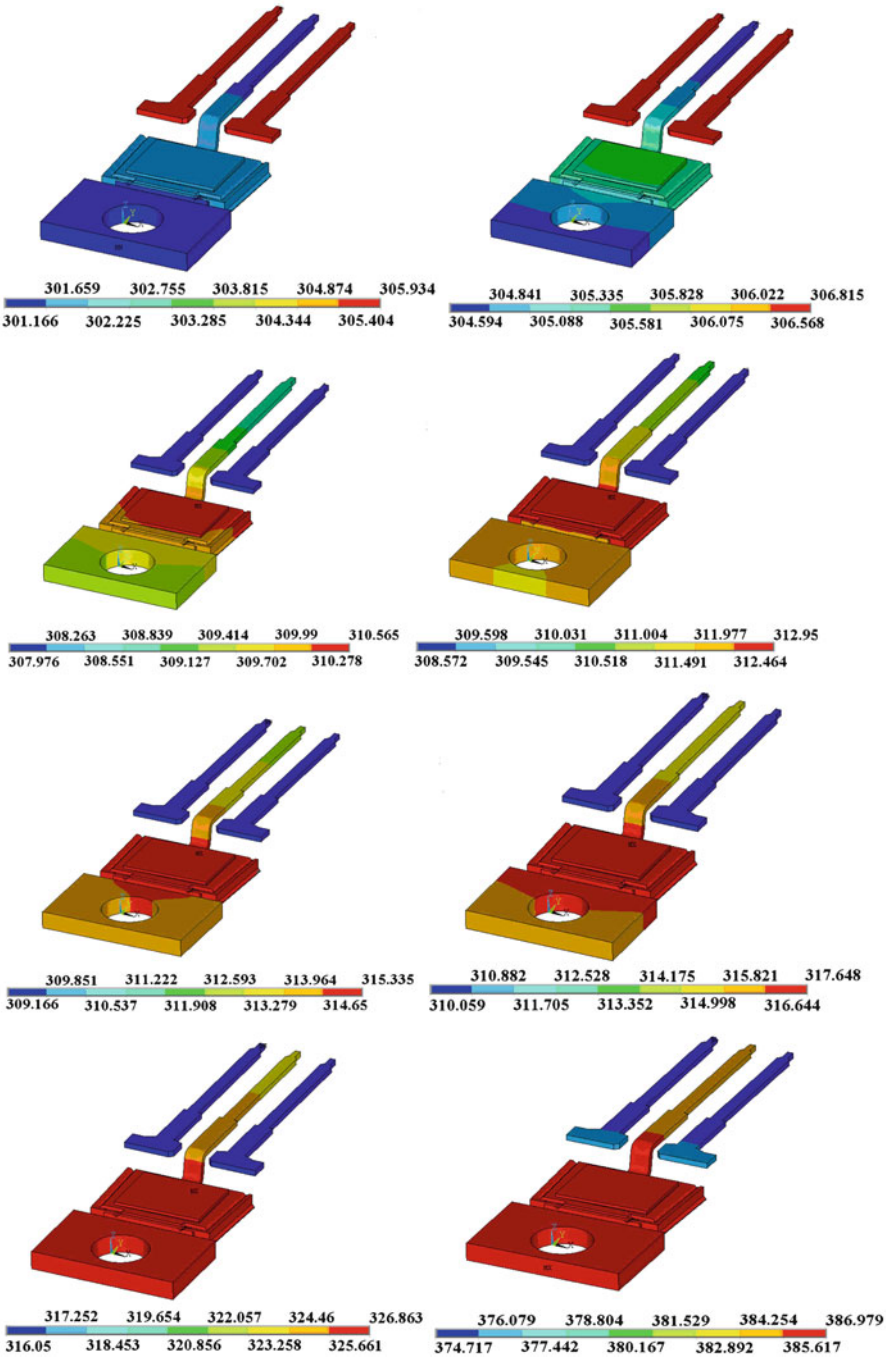


Fig. 9.6 Transient temperature distribution in PRCL with die size 175 × 240 × 8 mil

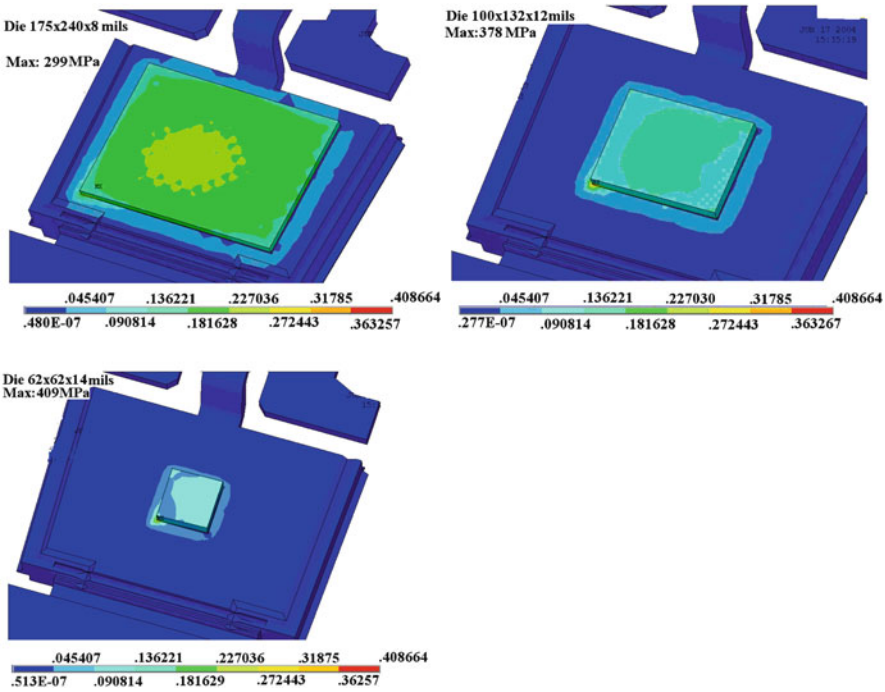


Fig. 9.7 von Mises stresses in three different dies when power is off 2 min during PRCL

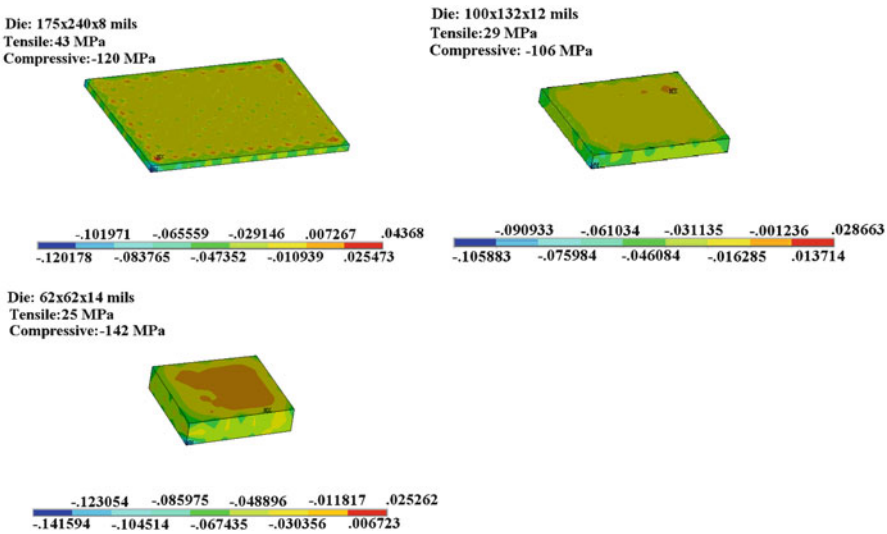


Fig. 9.8 First principal stresses in three different dies when power is off 2 min in PRCL

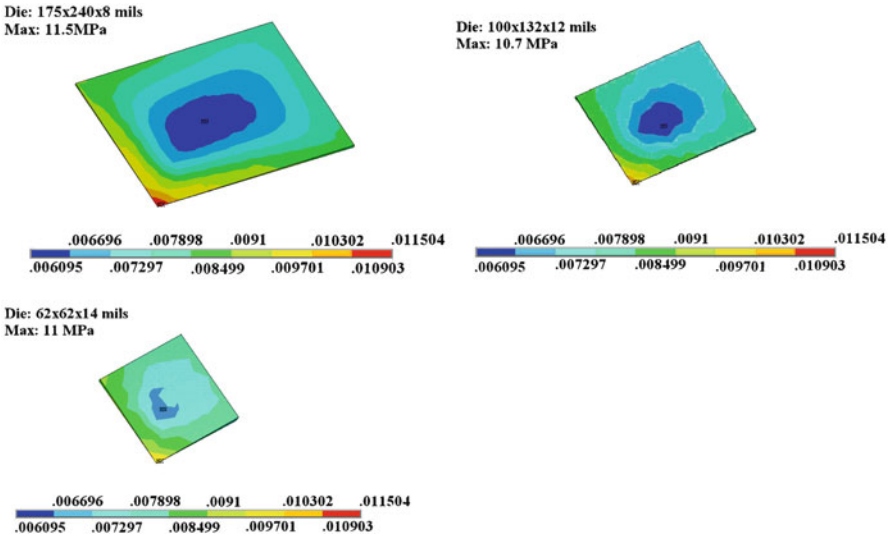


Fig. 9.9 von Mises stresses in die attach with three different dies when power is off 2 min in PRCL

9.2.4 Thermal Cycling Modeling and Discussion

Thermal cycling that is different from the power cycling. In the thermal cycling, thermal load temperature is considered as a uniform load and is applied to everywhere of the package, so there is no temperature gradient generated during thermal cycling. Figure 9.11 gives the temperature load cycles vs. time.

The TMCL stress results are shown in Figs. 9.12–9.16 and Tables 9.10–9.12. Figure 9.12 shows the first principal stress with different die size and thickness. The results show that the max stress locates at the point BLT = 0.0. Table 9.10 gives the comparison of first and third principal stress, max shear stress, and von Mises stress. The greatest von Mises stress, third principal stress, and shear stress appear at the smallest size die with biggest die thickness. This case is similar to the PRCL when power off 2 min. However, the max third principal stress in TMCL is 1,004 MPa that is about 1.67 times greater than PRCL and is lower than the compressive strength of silicon (about 1,100 MPa [21]). Figures 9.13 and 9.14 show the von Mises stress distribution of die attach and the loops of effective stress–strain in TMCL. Table 9.11 gives the comparison of effective strain, von Mises stress, and the plastic strain energy density when temperature ramps to −55°C. The results show that max von Mises stress appears at the point of BLT = 0.0. The max die attach von Mises stress in TMCL is about 2.68 times greater than PRCL. All of the die attach von Mises stresses in three die cases have reached the die attach tensile strength, 30 MPa. However, the three max effective strains of die attach are much lower than the material failure strain (0.4 based on vendor's test data).

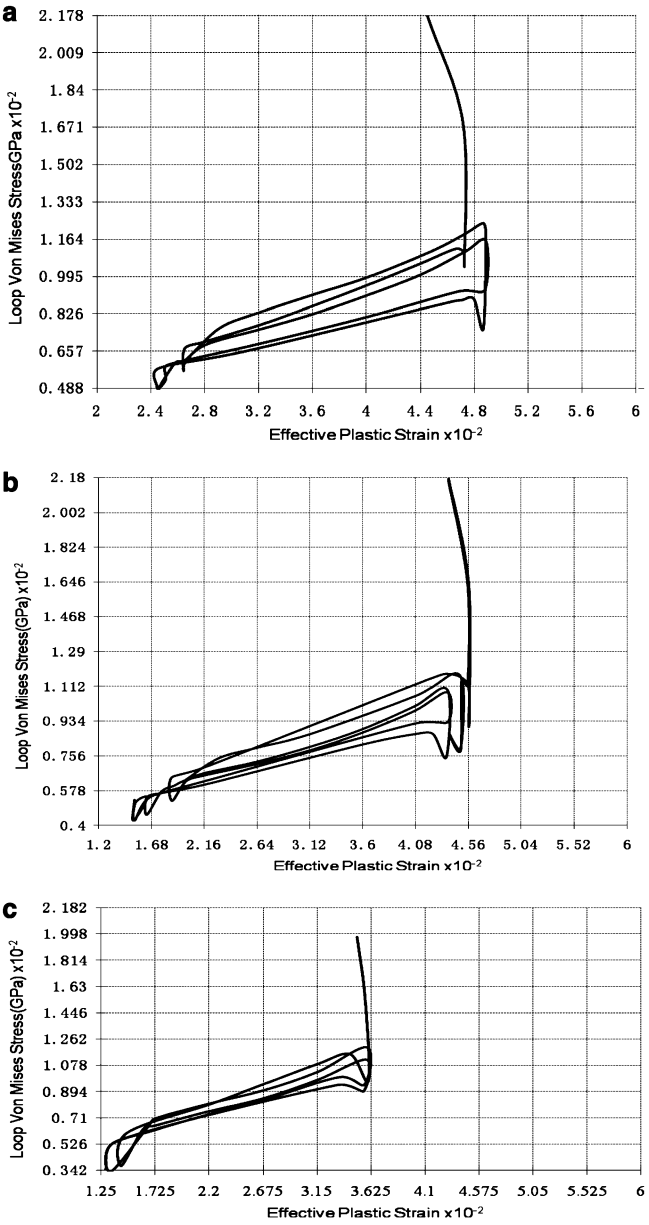


Fig. 9.10 Effective stress–strain loops of die attach in PRCL. (**a**) Die 175 × 240 × 8 mil. (**b**) Die 100 × 132 × 12 mil. (**c**) Die 62 × 62 × 14 mil

Table 9.8 Max die stress results when power off 2 min in PRCL

Die size	S1 (MPa)	S3 (MPa)	Sxy max shear stress (MPa)	von Mises stress (MPa)
Die 1: 175 × 240 × 8 mil	43 (T)	−427 (C)	+94	299
	−120 (C)		−80	
Die 2: 100 × 132 × 12 mil	29 (T)	−538 (C)	+64	378
	−106 (C)		−110	
Die 3: 62 × 62 × 14 mil	25 (T)	−600 (C)	+46	409
	−142 (C)		−136	

Reference temperature $T_g = 150°C$
T tensile stress; *C* compressive stress

Table 9.9 Max die attach stress, strain and energy density when power off 2 min in PRCL

Die size	Max effective strain	Max plastic strain energy density (MPa)	von Mises stress (MPa)
Die 1: 175 × 240 × 8 mil	0.0489	2.1	11.5
Die 2: 100 × 132 × 12 mil	0.0439	2.2	10.7
Die 3: 62 × 62 × 14 mil	0.0355	1.7	11.07

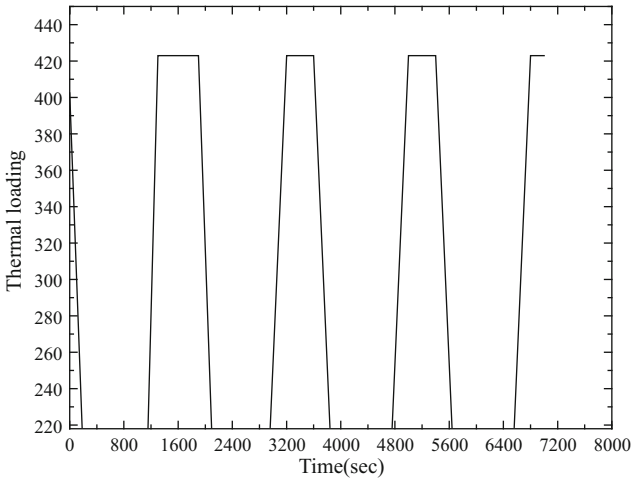


Fig. 9.11 Temperature cycle (−55 to 150°C)

The results in Table 9.11 further indicate that as the die size decreases and die thickness increases, the max principal stress on die increases while the max effective strain reduces.

Figure 9.15b show the stress impact of tilted die on pad, it can be seen that the stress peaks sharply at around BLT = 0.0 as well as highest principal stress in EMC. Table 9.13 gives the max stresses of die (100 × 132 × 12 mil) with different die attach thickness for an ideal die attach process with die tilt. By comparing Tables 9.13 and 9.10 (die 2), it may be seen that all of the stresses in Table 9.13 are

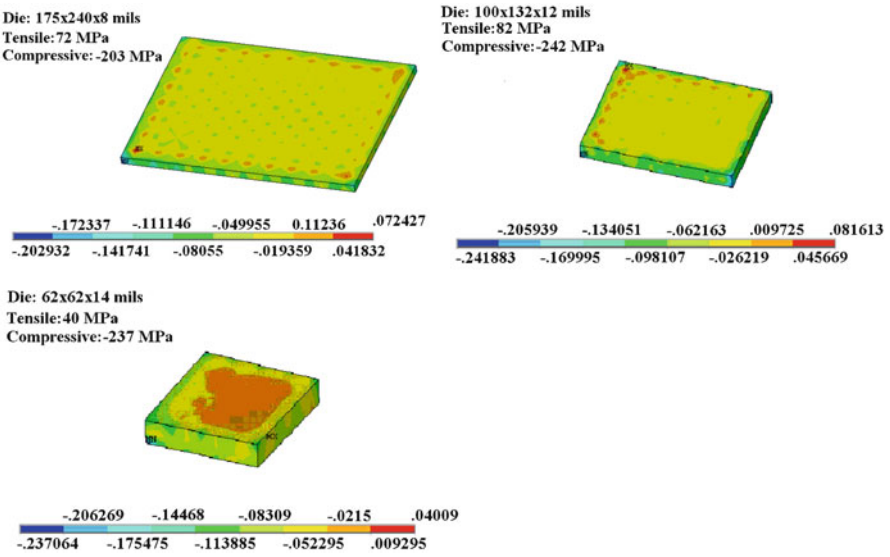


Fig. 9.12 First principal stresses in three different dies when temperature ramps to −55°C. *T* tensile;*C* compressive

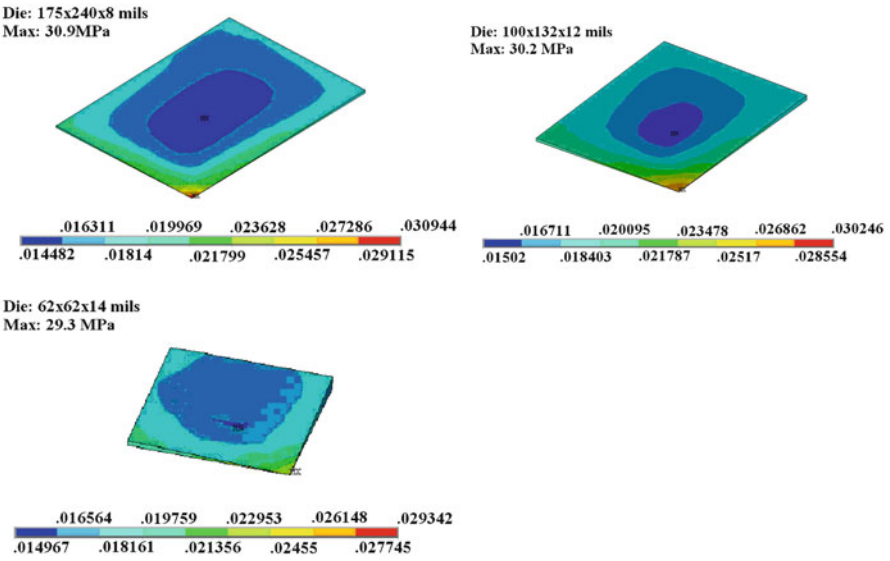


Fig. 9.13 von Mises stresses in die attach with three different dies when temperature ramps to −55°C

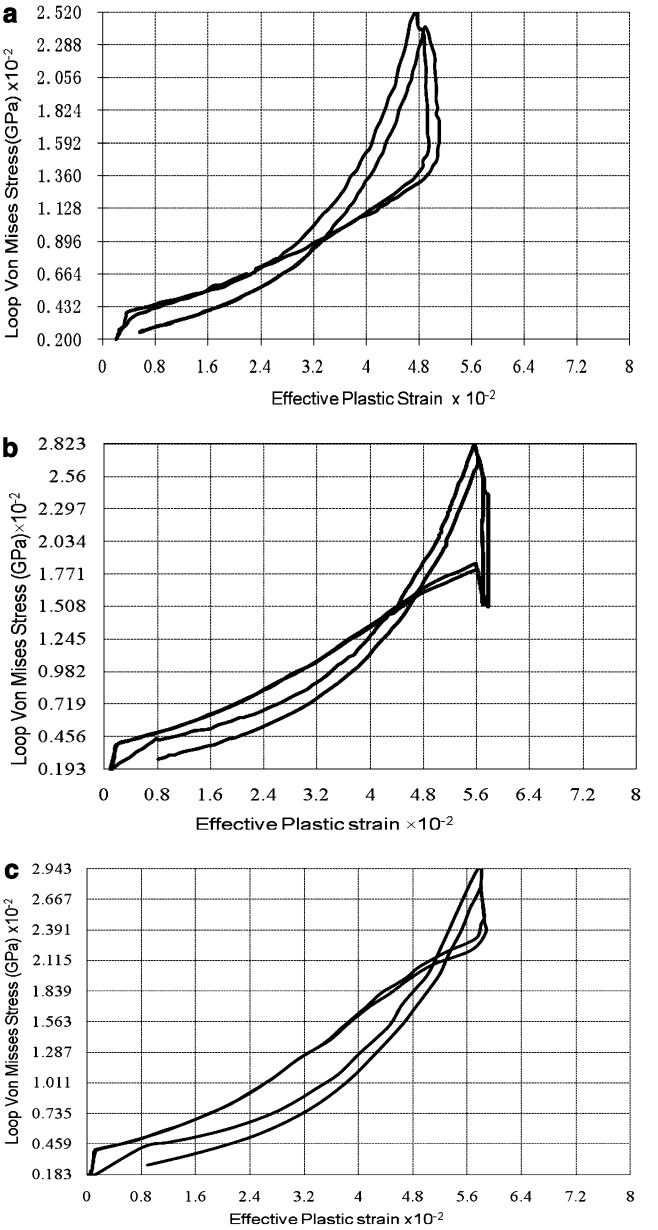


Fig. 9.14 Effective stress–strain loops of die attach in TMCL. (**a**) Die 175 × 240 × 8 mil. (**b**) Die 100 × 132 × 12 mil. (**c**) Die 62 × 62 × 14 mil

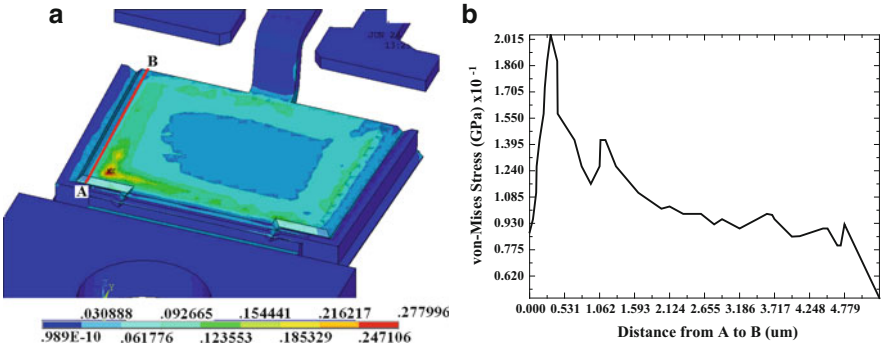


Fig. 9.15 Stress concentration induced at pad due to BLT = 0.0 in TMCL. (**a**) von Mises stress with tilted die. (**b**) von Mises stress along line AB

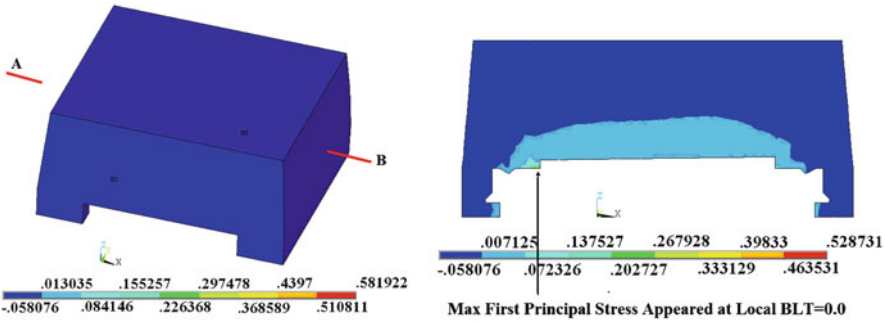


Fig. 9.16 First principal stress of EMC in TMCL

Table 9.10 Max die stress results in TMCL at −55°C

Die size	S1 (MPa)	S3 (MPa)	Sxy max shear stress (MPa)	von Mises stress (MPa)
Die 1: 175 × 240 × 8 mil	72 (T)	−708 (C)	+157	497
	−203 (C)		−130	
Die 2: 100 × 132 × 12 mil	82 (T)	−947 (C)	+173	646
	−242 (C)		−187	
Die 3: 62 × 62 × 14 mil	40 (T)	−1,004 (C)	+77	683
	−237 (C)		−226	

Reference temperature $T_g = 150°C$
T tensile stress; *C* compressive stress

Table 9.11 Max die attach stress, strain and energy density in TMCL at −55°C

Die size	Max effective strain	Max plastic strain energy density (MPa)	von Mises stress (MPa)
Die 1: 175 × 240 × 8 mil	0.077	5.6	30.9
Die 2: 100 × 132 × 12 mil	0.064	5.1	30.2
Die 3: 62 × 62 × 14 mil	0.058	4.6	29.3

Tensile strength: 30 MPa; failure strain: 0.4

Table 9.12 Max die stress results with different BLT in TMCL at −55°C

BLT (mil)	S1 (MPa)	S3 (MPa)	Sxy max shear stress (MPa)	von Mises stress (MPa)
0.0	13 (T)	−717 (C)	+123	475
	−184 (C)		−142	
2.1	21 (T)	−606 (C)	+113	452
	−109 (C)		−156	
3.3	38 (T)	−613 (C)	+114	457
	−104 (C)		−160	

Reference temperature $T_g = 150°C$
T tensile stress; *C* compressive stress
Die size: 100 × 132 × 12 mil without die tilt

Table 9.13 Materials properties

Materials	Young's modulus *E* (GPa)	Poisson's ratio *v*	CTE α (10^{-6}/K)	Yield strength *Y* (MPa)	Toughness K_{Ic} (MPa $m^{1/2}$)
EMC	17	0.3	24	98–150	
BPSG	64	0.17	2.78		
Silicon die	162.5	0.22	2.8		
Poly gate	162.5	0.22	2.8		
SiN	275	0.24	4		5.8–8.5
Al	70.34	0.346	23.2	110	
Cu	130	0.33	17	345–310	

less than the stress results in die 2 of Table 9.10. The max first principal stress S1 of Table 9.13 (with BLT = 2.1 mil) is less about 2.2 times than max S1 in Table 9.10, and the third principal stress S3 of Table 9.13 is less 1.56 times than S3 in Table 9.10.

Die crack is a big concern for the product due to the tilted die in PRCL and TMCL. Based on the modeling results that we have confidence that the tilted die (due to die attach process) will not induce the die crack even in the worst die tilted case. This matches the PRCL and TMCL test results from our manufacturing site in Suzhou that showed after PRCL and PRCL tests, no die crack is found. The von Mises stress of die attach in TMCL has reached its yield strength but its effective strain is still much lower than its failure strain. However, after many cycles once the effective strain of both PRCL and TMCL is accumulated to some value that is higher than the failure strain, the die attach will appear fracture. Figure 9.17 shows such fracture in the die attach after 10k PRCLs.

The above studies show the PRCL and TMCL tests and the impact of die attach process. They are part of the efforts for assembly reliability. Three interesting findings are listed below:

1. The impact of tilted die to the stress in PRCL and TMCL is significant. That will induce first principal stress 2.2 times greater and third principal stress 1.56 times greater than the case without die tilt. The tilted die will also induce highest EMC and pad stress. Therefore, controlling the die attach process to get uniform die

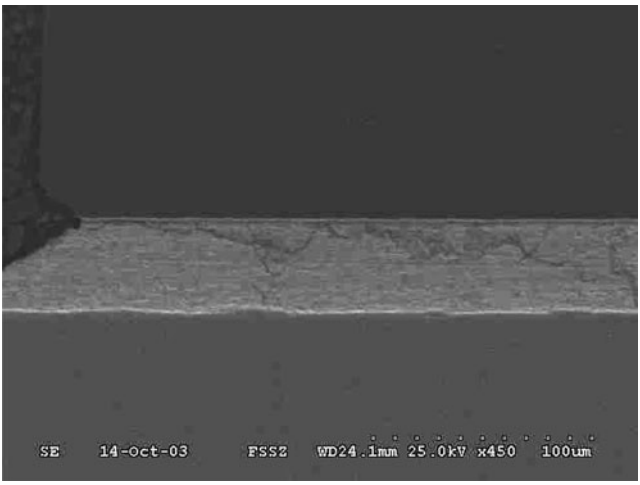


Fig. 9.17 Die attach fracture found after 10k PRCLs

attach thickness without die tilt is important for reducing stress in PRCL and TMCL.

2. The max stresses in TMCL of this paper are higher than that of PRCL. This is up to the temperature range in PRCL and TMCL. In the current PRCL and TMCL conditions, the principal stresses in die are not higher than the silicon failure criterion even at the worst die tilt case. However, for eutectic die attach material, the accumulated effective strain is the root reason to make the fracture after many cycles even if the stress is lower than yield strength.
3. There is also an optimization geometry for die size and thickness, thicker die will induce higher stress, while the die size has a trade-off combination. In this paper, $100 \times 132 \times 12$ mil die seems to be the best solution after consideration of both with and without die tilt, and all of the stress components.

9.3 Power Packaging Passivation Crack Analysis

Power package is widely used in motor vehicle, power industry. The basic structure for a typical power package D-PAK is as follows. On silicon substrate, many thin layers of dielectrics and polysilicon as gates are built for the electronic function, which in turn is covered by a metal layer, and then passivated by SiN film partially on the top (Fig. 9.18). The whole die is cured by epoxy molding compound (EMC) at 175°C. The EMC has a larger CTE than the silicon, so the EMC board would contract more than the silicon die upon cooling. But the bonding resists sliding between them, and hence, shear stresses develop on the interface of die and EMC, concentrated at the edges and corners and pointing to the center. During qualification test, the temperature loading cycles between −65 and 150°C, or slightly different, but the high end temperature is usually lower than the

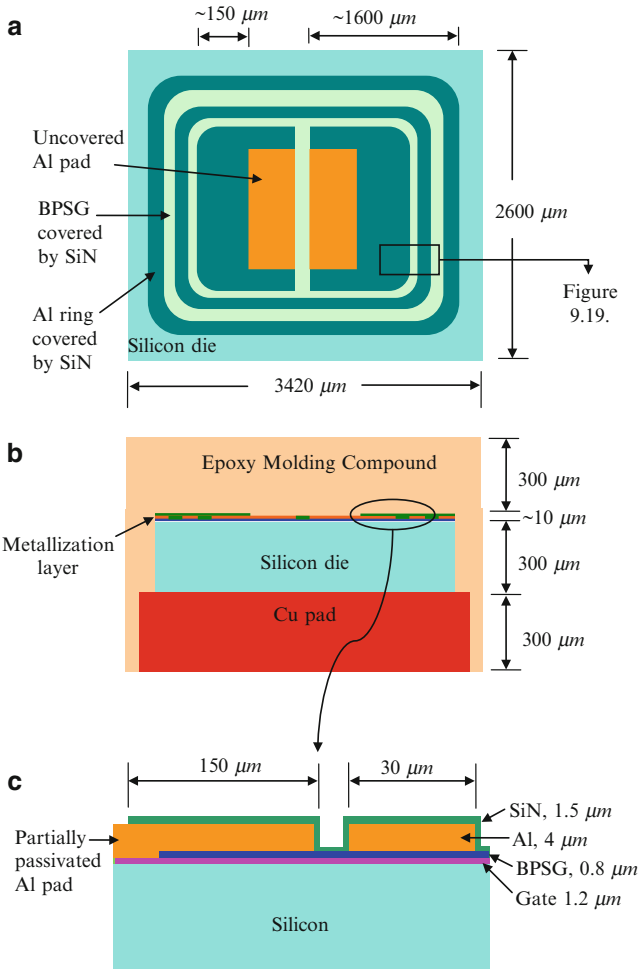


Fig. 9.18 D-PAK structure. (**a**) Top view. (**b**) Cross section. (**c**) Magnified view of the metallization of the *lower right corner*

curing temperature. Consequently, the magnitude of shear stresses varies with the loading temperature, but the direction is never reversed. This shear stress is partly sustained by the membrane stress in the passivation film, and partly transmitted to the metal film as a shear stress in the metal [23–25]. The metal film also has a larger CTE than silicon substrate. If the metal yields in every cycle, the plastic shear strain deforms in the same direction as the shear stress, i.e., the metal film will ratchet toward the die center. Otherwise, it deforms elastically within the shakedown region. The ratcheting of metal film could build up huge stress in the passivation film. When the tensile stress is high enough to initiate the flaws, the passivation cracking will happen. Figure 9.19a, b show the micrograph and SEM of a part of the D-PAK

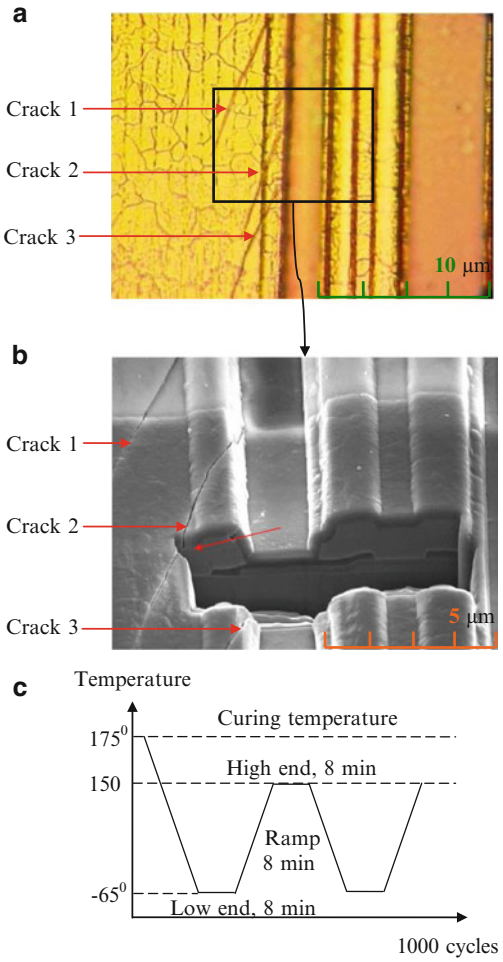


Fig. 9.19 (**a**) Micrographs of a die surface near the lower right corner of D-PAK after 1,000 temperature cycles. (**b**) SEM photo with FIB cut. Cracks develop in the passivation film over the blanket aluminum film close to the boundary, but are rarely observed in stripe. (**c**) Temperature loading in qualification test

after 1,000 TMCLs. Cracks initiate and grow near the edges in the SiN film above the wide aluminum pad, but rarely happen on the SiN film above the narrow aluminum ring. Figure 9.19c plots the loading condition in the test.

Based on the previous study of the ratcheting-induced cracking in passivation film, we want to answer a series of questions and discuss the designs method to avoid such failure modes for a typical power package D-PAK. Under what condition does the metal film ratchet? How could it be avoided? If the metal film ratchets, what is the largest stress level in the passivation film? How many cycles do the cracks need to fail the device? What failure criterion should we use to assess the

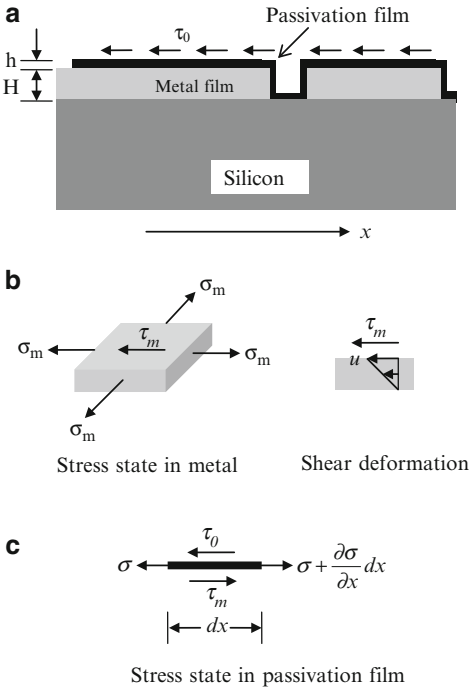


Fig. 9.20 (**a**) A partially passivated blanket film and a fully passivated stripe lie on the substrate. (**b**) The stress state in the metal film and shear flow. (**c**) The stress state in the passivation film

power device? Can the device be immortal if we modify the design? In order to answer these questions, the plan of this section is as follows. Following the above introduction Sects. 9.3.1 and 9.3.2 applies the ratcheting diagram and the relation of the stress level in passivation with the number of cycles to estimate the critical number of cycles to initiate the cracks by using the Griffith criterion. Section 9.3.3 gives the relation between the cracking behavior and the number of cycles, from the initiation, the propagation to the failure. Section 9.3.4 discusses some simple, but effective design modifications to avoid ratcheting and cracking. Section 9.3.5 makes the conclusion.

9.3.1 Ratcheting Deformation Mechanism

Figure 9.20 illustrates the structures to be studied as the model for D-PAK. The passivation film, thickness h, lies on the metal underlayer, thickness H, which inturnlies on the semi-infinite substrate. The film is elastic, the underlayer is elastic–perfectly plastic, and the substrate is also elastic. Both the blanket film and the stripe are considered here. In this model, we neglect the gate and BPSG based on

the following argument. From Table 9.13, the gates and BPSG have the similar CTE with silicon substrate, and they are just thin layer above silicon, so the mismatch stresses in these two layers are very low. Even though the metal layer ratchets, it does not accumulate stresses in them. Moreover, the in-plane deformations of metal and passivation films are constrained by silicon substrate, and the out-of-plane shear deformation also is independent of gate and BPSG, so these two layers do not affect the ratcheting in metal and the cracking in passivation.

9.3.1.1 Deformation Mechanism Map of Metal Layer

The metal film is assumed to an elastic–perfectly plastic solid with the coefficient of thermal expansion (CTE) α_m, Young's modulus E_m, Poisson's ratio ν_m, and the temperature-independent isotropic yield strength Y_m. The substrate is elastic with CTE α_s. As shown in Fig. 9.20b, the metal film is under biaxial in-plane stress $\sigma_m = E_m(\alpha_m - \alpha_s)(T_H - T_L)/(1 - \nu_m)$ due to the temperature change, and a shear stress τ_m on the top surface, which is transmitted through the passivation film originally, induced by packaging. The film and the substrate are well bonded, and have the same in-plane net strain at all time. So the von Mises yield condition can be expressed by the ellipse [2]:

$$\left[\frac{E_m(\alpha_m - \alpha_s)(T_H - T_L)}{2(1 - \nu_m)Y_m}\right]^2 + 3\left(\frac{\tau_m}{Y_m}\right)^2 = 1 \tag{9.12}$$

If the metal film yields every cycle, the J_2 flow theory dictates that the plastic shear strain increment $d\gamma^p$ has the same sign as the shear stress τ_m. Hence, the total shear strain accumulates cycle by cycle toward the die center because the shear stress τ_m does not change the direction.

Huang et al. [23–25] found the deformation mechanism in metal film and plotted the ratcheting diagram as in Fig. 9.21, which is spanned by the normalized shearstress, τ_m/Y_m, and the normalized temperature range, $E_m(\alpha_m - \alpha_s)(T_H - T_L)/(1 - \nu)Y_m$. The plane is divided into four regimes: plastic collapse, shakedown, and ratcheting, and cyclic plastic deformation. The practical implications of Fig. 9.21 are as follows: a given pair of the normalized shear stress and the normalized temperature range corresponds to a point in the diagram. If $\tau_m/Y_m \geq 1/\sqrt{3}$, the metal film plastically deforms under the shear stress alone without the aid of the temperature change, and therefore, the point falls in the plastic collapse regime. From Table 9.13, we can see that the yield strength of EMC is comparable to that of Al, or even larger. Hence, if the temperature loading range is very large, the plastic collapse could happen. In this situation, the design has to be modified either to decrease the yield strength of molding compound, or to increase that of the metal film, e.g., Cu, in order to bring the structure out of the plastic collapse regime.

If $\tau_m/Y_m < 1/\sqrt{3}$ and the temperature range satisfies the condition of $E_m(\alpha_m - \alpha_s)(T_H - T_L)/(1 - \nu_m)Y_m > 2$, the point falls in the ratcheting regime, and so the metal film ratchets incrementally as the TMCLs, no matter how small

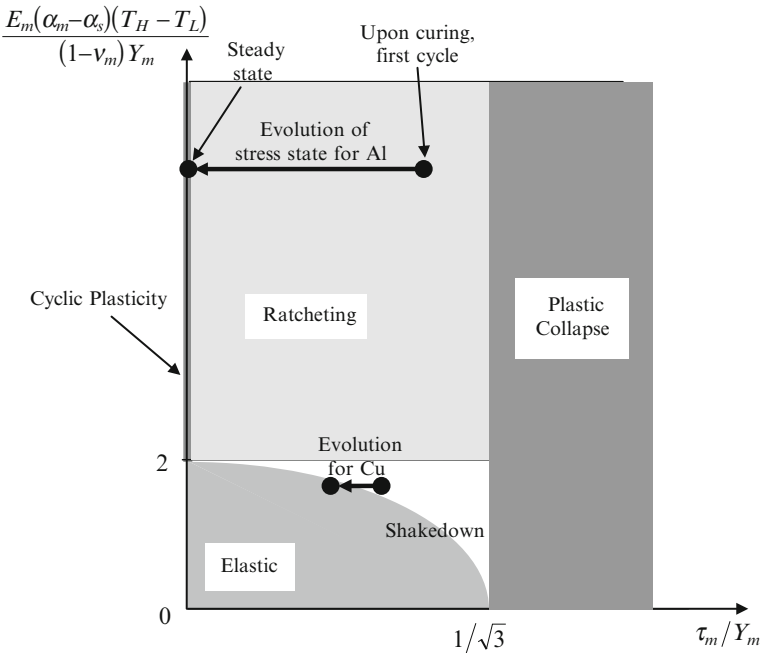


Fig. 9.21 The ratcheting diagram for the elastic and perfectly plastic metal film. The plane is divided into four regimes: plastic collapse, shakedown, ratcheting, and cyclic plastic deformation

the shear stress is, so long as does not vanish. The shear stress is originally transmitted through the passivation film, and relaxes cycle by cycle by plastic flow. At the end, the shear stress relaxes to zero, the ratcheting stops, and the metal film goes into the regime of cyclic plastic deformation. Meanwhile, the stress state in passivation reaches the steady state.

If $\tau_m/Y_m<1/\sqrt{3}$ and the temperature range satisfies the condition of $E_m(\alpha_m-\alpha_s)(T_H-T_L)/(1-\nu_m)Y_m<2$, the metal film may plastically deform at the early stage if the point is above the ellipse. But once the shear stress relaxes and the point goes into the ellipse, the metal film deforms elastically afterward. *So this is the shakedown regime*, *which should be the design goal*. The shakedown temperature range can be extended if the yield strength of the metal film is larger, or if the CTE mismatch is smaller, or if the temperature range is narrow.

To accelerate the qualification test, the engineer sometimes uses a temperature range larger than that in the normal use. The observation of ratcheting in test cannot predict the same results in normal use. A simple-minded extrapolation could be misleading.

Ratcheting is a very common phenomenon in Al metallization, but no report about Cu metallization. Let's use this diagram to answer the difference. And it also gives us the idea of improvement of design. Assume the structure is the same, the temperature loading range is also the same, and all other materials are also the same

except the metal. Using the values listed in Table 9.13, and under the typical loading condition used in qualification test as Fig. 9.19c, if aluminum is used, $E_m(\alpha_m - \alpha_s)(T_H - T_L)/Y_m(1 - \nu_m) = 4.29>2$, so the aluminum film yields in every thermal cycle. Hence, any shear stress upon curing could lead ratcheting. By contrast, if Cu is used, $E_m(\alpha_m - \alpha_s)(T_H - T_L)/Y_m(1 - \nu_m) = 1.77<2$, so the copper film would ratchet only if the shear stress is very large. If we use the yield strength of EMC as a limit estimate, $\tau_m/Y_m = 0.29$. The point is just above the ellipse, so the copper film could ratchet at the beginning of test. But the shear stress τ_m will relax cycle by cycle, and so the copper film will go into the shakedown regime after certain cycles. Only if the passivation film does not crack before the copper film shakes down, it will never crack in the future cycles.

9.3.1.2 Linear Ratcheting Formula

When $E_m(\alpha_m - \alpha_s)(T_H - T_L)/(1 - \nu_m)Y_m>2$, and the shear stress τ_m is much smaller than its yield strength Y_m, the plastic shear strain rate per cycle vs. the shear stress can be approximated by a linear relation [25]:

$$\frac{\partial \gamma^p}{\partial N} = \frac{\tau_m}{\eta} \tag{9.13}$$

where η, *the linear ratcheting coefficient*, is defined as follows:

$$\eta = \frac{E_m}{12(1 - \nu_m)} \left[\frac{E_m(\alpha_m - \alpha_s)(T_H - T_L)}{(1 - \nu_m)Y_m} - 2 \right]^{-1} \tag{9.14}$$

For example, if $\tau_m/Y_m<0.2$, then the error is less than 10%.

In the temperature range of Fig. 9.19c, all the materials in the structure do not creep, so dwelling time at high end and low end does not affect the analysis. In practice, it takes time for the structure to reach uniform temperature state during the testing, but in analysis and FEA simulation, just the loading range matters. So no matter linear or sinusoidal ramping, dwelling or not dwelling, they will lead to the same results.

9.3.1.3 Stress Level vs. the Number of Cycles

Because we apply the linear ratcheting relation in the following study, we can apply the linear superposition principle. Therefore, the stress state in the passivation film can be superimposed by the solution of 1D problem [23, 25].

As shown in Fig. 9.20c, the equilibrium equation can be written as $\partial\sigma/\partial x + (\tau_m - \tau_0)/h = 0$. Let $u(x,N)$ be the displacement and then the stress can be written as $\sigma = \bar{E}_p \partial u/\partial x$, where $\bar{E}_p = E_p/(1 - \nu_p^2)$, and E_p and ν_p Young's

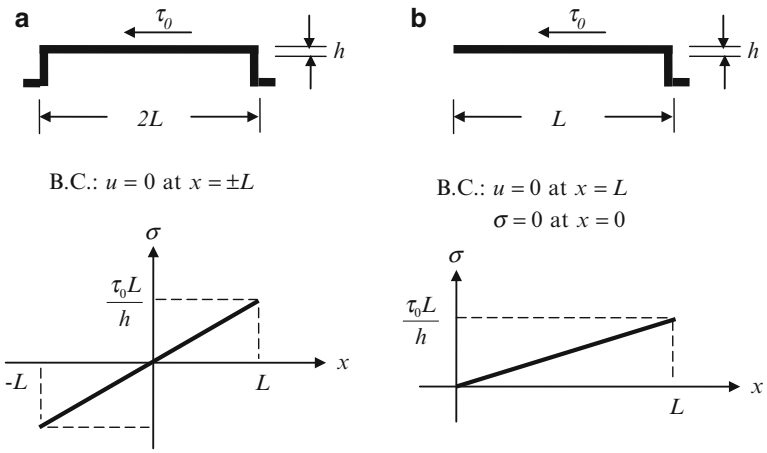


Fig. 9.22 Stress distribution in steady state for two geometries. (**a**) Two ends are fixed. (**b**) One end fixed, the other free

modulus and Poisson's ratio of passivation film. Moreover, the ratcheting shear strain relates to the displacement as $\gamma^{\mathrm{p}} = u/H$, as shown in Fig. 9.20b. Combined with the linear ratcheting relation (9.13), the governing equation becomes a diffusion-like equation with source term:

$$\frac{\partial u}{\partial N} = D\frac{\partial^2 u}{\partial x^2} - \frac{\tau_0 H}{\eta} \tag{9.15}$$

where $D = hH\bar{E}_{\mathrm{p}}/\eta$ is the ratcheting diffusivity, and the shear stress τ_0 is assumed to be a constant for simplicity. Equation (9.15) can be solved analytically by imposing the initial and boundary conditions.

Figure 9.22 plots the normal stress distribution of the passivation film in steady state for two kinds of geometries. In Fig. 9.4a, both ends are bonded with silicon substrate, so the boundaries are fixed, i.e., $u = 0$ at $x = \pm L$. In Fig. 9.21b, the right end is bonded to the silicon substrate, but the left end is free, i.e., boundary conditions are $u = 0$ at $x = L$, and $\sigma = 0$ at $x = 0$. In steady state, $\partial u/\partial N = 0$, so the stress distribution can be easily solved for both cases, i.e., linear distributed along x, with largest stresses on the right edge [25].

$$\sigma_{\mathrm{ss}} = \frac{\tau_0 L}{h} \quad \text{at } x = L \tag{9.16}$$

The characteristic number of cycles to reach the steady state can be estimated by

$$N_0 = \frac{L^2}{D} = \frac{L^2}{hH}\frac{\eta}{\bar{E}_{\mathrm{p}}} \tag{9.17}$$

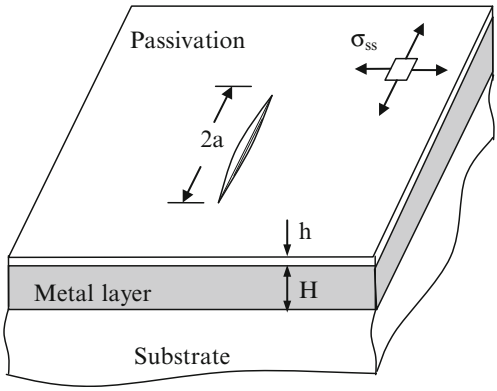


Fig. 9.23 A finite initial crack, with length $2a$, in the blanket film

The complete solution of (9.15) can be written as a series by solving IBVP with the initial condition of $u = 0$ at $N = 0$. Because the first term in the series dominates when the $N > 0.05N_0$, the maximum tensile stress build-up on the right edge can be approximated by the following:

$$\sigma \approx \sigma_{ss}\left[1 - \frac{8}{\pi^2}\exp\left(-\frac{\pi^2}{4}\frac{N}{N_0}\right)\right] \tag{9.18}$$

We can easily extend the above 1D analysis to 2D case just by superposition. As shown in Fig. 9.18a, the passivation if narrow in one direction, but long in the other. Hence, the final steady state can be reached when ratcheting stops in the longer direction. During thermal cyclic loading, the in-plane deformation of both the film and underlayer is constrained by the substrate. The thermal mismatch adds another uniform biaxial stress state in the film, and its maximum is $E_p(\alpha_s - \alpha_p)(T_H - T_L)/(1 - \nu_p)$. Because the CTEs of Si and SiN are very close, as shown in Table 9.13, the contribution of this stress is just on the order of 10 MPa. Compared to the huge stress accumulated during ratcheting, on the order of 1 GPa, this misfit stress is negligible.

9.3.1.4 Delayed Cracking

If there is an initial crack, with length $2a$, in the blanket passivation film, as in Fig. 9.23, the metal layer ratchets and loses the constraint gradually to open the crack; meanwhile, the stress field near the crack relaxes in the crack wake, but intensifies around the crack tip [26–30]. The *length scale of the relaxation*, l, is easily identified as $\sqrt{DN}$ from (9.15). It can be written explicitly as follows:

$$l = \sqrt{NhH\bar{E}_p/\eta} \tag{9.19}$$

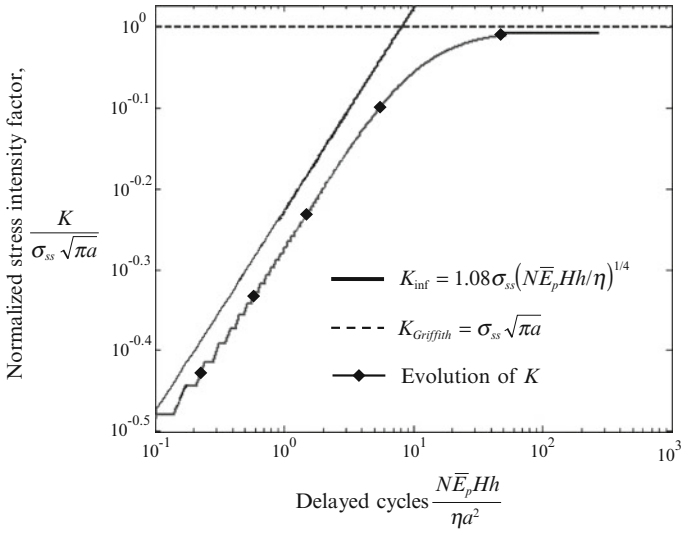


Fig. 9.24 Normalized stress intensity factor as a function of normalized cycles for a finite crack in a blanket film in log–log plot. The two asymptotic limits, Griffith crack and infinite crack, are also plotted in this figure

So the stress intensity factor can be written as $K = \sigma_{ss}\sqrt{a} \cdot f(v_p, l/a)$, which can be solved numerically [31].

In early stage of the relaxation, $l \ll a$, the crack behaves like an infinite crack modulated by underlayer ratcheting, so the stress intensity factor depends on the relaxation length l, and is of the form:

$$K_{\inf} = \kappa\sigma_{ss}[NhH\bar{E}_p/\eta]^{1/4} \tag{9.20}$$

where κ is a function of Poisson's ratio v_p. It has been solved numerically and tabulated in ref. [27]. For the SiN passivation film, $v_p = 0.24$, we interpolate it as $\kappa = 1.08$.

After certain cycles, the relaxation region is much larger than the crack size, $l \gg a$, i.e., the metal underlayer loses the constraint completely, so the passivation film becomes free-standing. Hence, the crack behaves like a Griffith crack, and the stress intensity factor approaches:

$$K_{\text{Griffith}} = \sigma_{ss}\sqrt{\pi a} \tag{9.21}$$

Consequently, the stress intensity factor K has two asymptotic limits, as shown in Fig. 9.24, in which the normalized stress intensity factor $Kh/\tau_0 L\sqrt{\pi a}$ vs.

the normalized number of TMCLs $NhHE_p/a^2\eta(1-\nu_p^2)$ is plotted. As we know, the in-plane stresses evolve with the TMCLs and the crack behaves in mixed mode, but the above analysis captures all the physics and is easy to use for the case of steady state.

A device would be immortal if the flaws keep stationary in the passivation film as originally induced in manufacturing process. This requires the stress intensity factor is always less than the toughness of passivation film, i.e., $K<K_c$. Hence, if the toughness is above the Griffith limit, i.e., $K_c>\sigma_{ss}\sqrt{\pi a}$, there is no crack initiation; on the contrary, the crack will initiate and grow after delayed cycles. So the question of cracking or not becomes a fundamental one in fracture mechanics. It depends on the stress level and flaw size. Stress level in steady state can be obtained by solving BVP, and the flaw size should be measured by experiments. Then, applying Griffith criterion, (9.21), we know if or not cracking will initiate.

The critical stress to initiate cracks, or the fracture strength σ_c, can be calculated by Griffith criterion if the flaw size is known, i.e., $\sigma_c = K_c/\sqrt{\pi a}$, or just measured by experiments. Considering (9.18), we can estimate the critical number of cycles of initiation N_i as follows:

$$\frac{N_i}{N_o} = -\frac{4}{\pi^2}\ln\left[\frac{\pi^2}{8}\left(1-\frac{\sigma_c}{\sigma_{ss}}\right)\right] \tag{9.22}$$

Notice that (9.22) holds only when $\sigma_{ss}>\sigma_c$; otherwise, the crack will keep stationary. Also we can see that it makes sense when $\sigma_{ss}<5.28\sigma_c$, otherwise, N_i is negative. This is because we just keep the first term of the series in (9.18) as an approximation. But we can know that cracks initiate very soon in the regime of $\sigma_{ss}>5.28\sigma_c$. Figure 9.25 plots the normalized number of cycles of crack initiation vs. the normalized stress level in steady state. The whole plane is divided into three regimes: no crack initiation, delayed cracking as (9.22), and catastrophic cracking.

In order to obtain the accurate number of cycles for the 2D case, we need to do multilevel FEA, e.g., package level FEA for the distribution of $\tau_0(x,y,N)$, metal-film scale FEA for $\sigma_{\alpha\beta}(x,y,N)$. Moreover, the stress intensity factor also depends on the flaw size, which is manufacturing dependent and should be measured by experiment.

In the above analysis, the interfacial shear stress τ_0 may vary with position and evolve with the loading. It concentrates on edges and corners, where the stress state is complicated (e.g., the normal peeling). Even though it can be solved by FEM, but it varies case by case. We have to recalculate if we change any of the parameters, such as the materials, the geometries, and loading conditions. So it is hard to predict accurate number of cycles by a simple formula. But, the interfacial shear stress is limited by the shear yield strength of EMC, which is an *upper bound*. Hence, it corresponds to an *upper bound* of stress level in passivation, and so to the *lower bound* of the number of cycles for the crack initiation. Hence, *the increase of lower bound of critical number of cycles of initiation should be the design goal*.

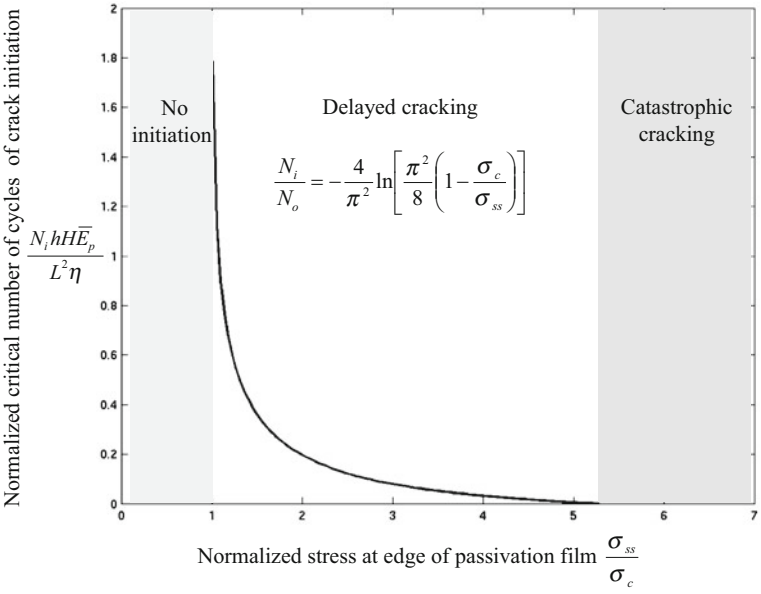


Fig. 9.25 Normalized critical number of cycles to initiate the crack vs. the normalized steady state stress level. If the steady state stress level is less than fracture strength, the crack remains stationary; if it is between $\sigma_{ss} = 1 - 5.28\sigma_c$, (9.22) applies; otherwise, the crack initiates and grow very soon

If no crack initiates before it reaches the steady state, then ratcheting-induced passivation cracking will never happen. Otherwise, we need to do thorough calculation to check.

9.3.1.5 Example

In the following [32], we use Fig. 9.25 to check if the passivation cracks or not in the current D-PAK (Fig. 9.18), and to estimate the lower bound of the number of cycles of crack initiation by (9.22).

Using the values in Table 9.13 and Fig. 9.18, and the shear stress $\tau_0 = 50$ MPa, the steady $\sigma_{ss} = 5$ GPa at the edge of the middle blanket film, and the characteristic number of cycles is about $N_0 = 50$. From Table 9.13, if we use 5.8 MPa $m^{1/2}$ as the fracture toughness of SiN, and assume the largest initial crack length is comparable to the thickness, 1.5 mm, then the critical stress to initiate the crack would be $\sigma_c = 4.73$ GPa. Hence, from Fig. 9.25 and (9.22), it takes at least 55 cycles for crack initiation. In the narrow stripe, $\sigma_{ss} = 500$ MPa at the edge. So that cracking is less likely to happen. The above conclusion can be verified by experimental pictures in Fig. 9.19.

9.3.2 Growth of the Crack and Critical Width

9.3.2.1 Growth of Cracks

Except the length scales L, the width of passivation film, and l, the relaxation region, the problem has another length scale:

$$\Lambda = \left(\frac{K_c}{\sigma_{ss}}\right)^2 \tag{9.23}$$

For a moving crack, the length scales the zone over which the stress field varies rapidly. And so it defines a scale of cycles:

$$N = \frac{\Lambda^2}{D} = \frac{K_c^4 h^3 \eta}{\tau_o^4 L^4 H \bar{E}_p} \tag{9.24}$$

This number of cycles allows events over the length scale Λ to take place. The crack velocity increases with number of cycles after initiation, and attains a steady value after the tip moves a distance about Λ. Dimensional consideration require that the steady velocity for a crack in a blanket film obey the scaling law:

$$V = \chi \frac{\Lambda}{N} = \chi \frac{\bar{E}_p H L^2 \tau_o^2}{\eta h K_c^2} \tag{9.25}$$

where χ is a dimensionless number depending on Poisson's ratio. Liang et al. [28] gave $\chi \approx 0.5$ for $v = 0.3$ by numerical analysis. Suo et al. [31] studied the ratcheting-induced passivation cracking behavior and plotted out the relations between the crack extension, velocity and the number of cycles. We can apply the same method to passivation cracking in DPAK.

9.3.2.2 Critical Width

If the width of the stripe is less than the crack propagation scale, i.e., $2L<\Lambda$, then the stress intensity factor can never approach K_c. So the critical width of stripe is:

$$L_c = 0.8\left(\frac{K_c h}{\tau_o}\right)^{2/3} \tag{9.26}$$

below which the crack never grow no matter how long the crack is. Based on this equation, and put the value in, we can estimate that the critical width is 25 μm for partially passivated film, 50 μm for fully partially passivated stripe.

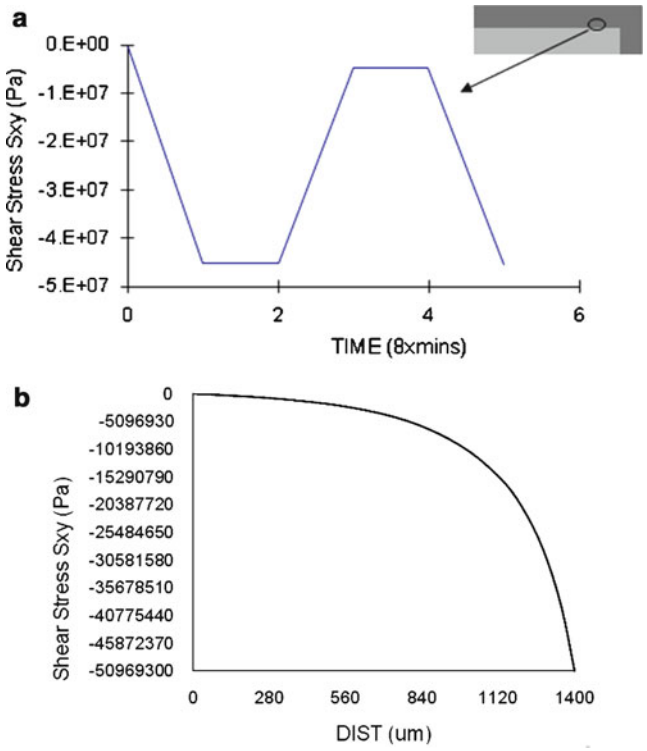


Fig. 9.26 Interfacial shear stress evolution if there is NO buffer layer. (**a**) Interface shear stress Sxy in a cycle. (**b**) Interfacial shear stress along interface at $T = -65°C$

9.3.3 Design Modification

From the study of Sects. 9.3.2 and 9.3.3, we consider the following design modifications to avoid passivation cracking [32].

9.3.3.1 Buffer Layer

If we add an extra much compliant buffer layer between EMC and silicon die, e.g., polyimide or silicone, the shear stress τ_0 could reduce one order of magnitude, and so does the stress level in steady state. Correspondingly, the lower bound of critical number of cycles of crack initiation, N_i, could increase several orders of magnitude. Or this design modification brings the device into safe regime, i.e., no crack initiation at all.

The comparisons are plotted in Figs. 9.26 and 9.27.

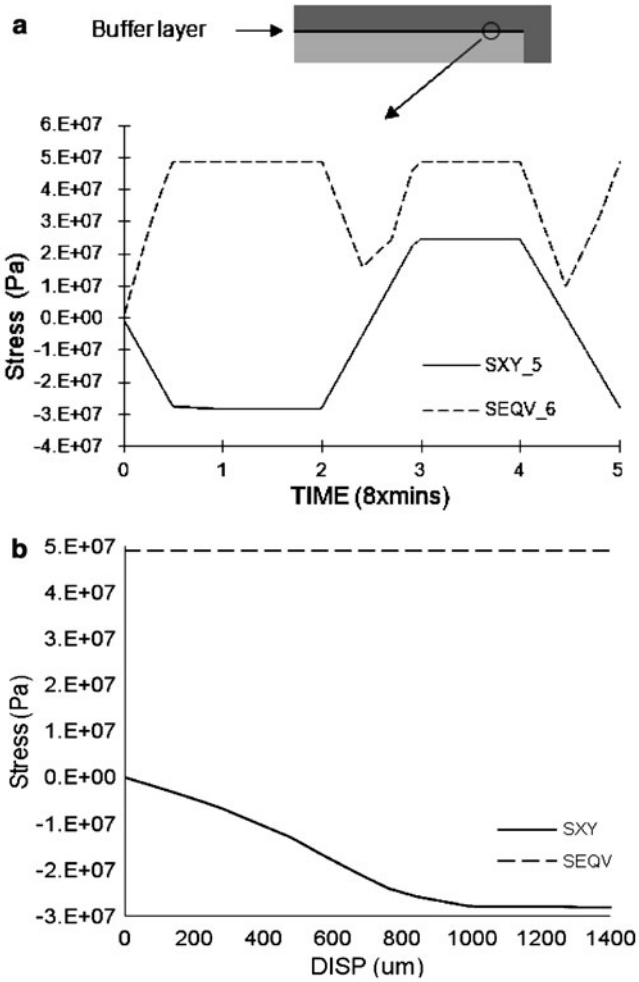


Fig. 9.27 Interfacial shear stress evolution if there is a buffer layer. (**a**) Stress in a cycle due to the buffer layer. (**b**) Interfacial stress along the interface at $T = 65°C$

9.3.3.2 Small Passivation Width

The reduction of width and length and the increase of thickness of passivation also could reduce the stress level. In the era of miniaturization, the change of large or long passivation film to small or narrow pads is a practical method.

Cut slot or just use narrow passivation. Because if we use slot skill, stress concentration around the corners of slot is very high; hence, the simplest thing is to just narrow the width down. In Fig. 9.28, a lower right corner is simulated by

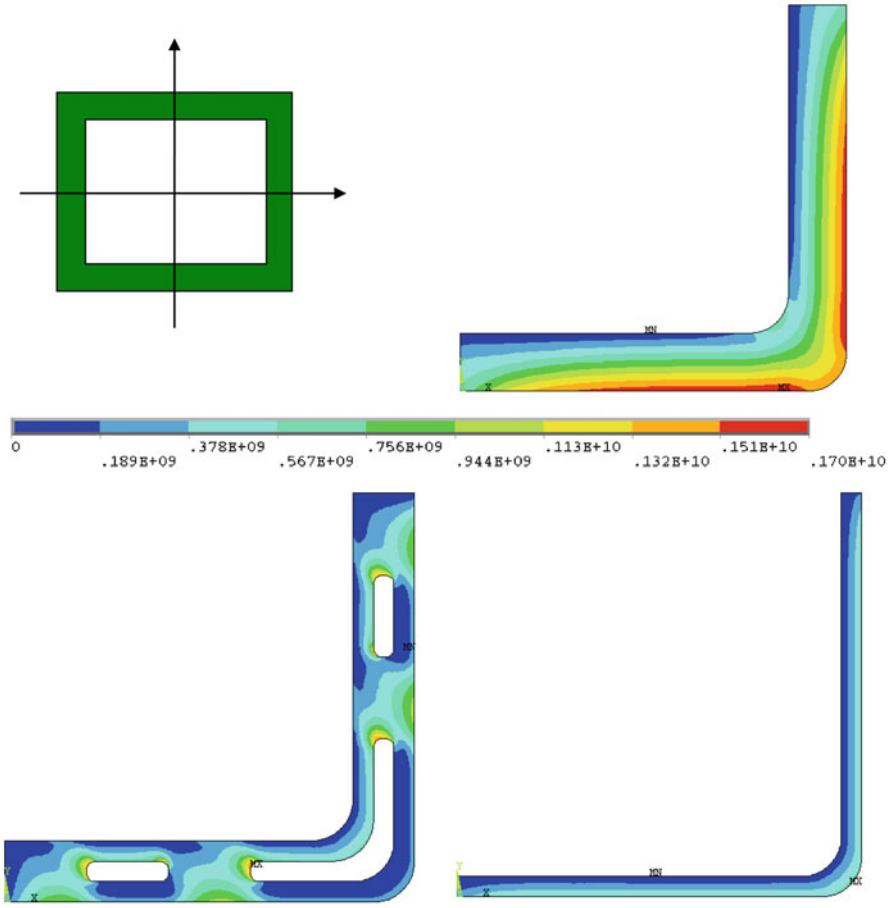


Fig. 9.28 Steady-state stress distribution in the passivation film

ANSYS®. The original design and the slot technique, and the narrow stripe are shown. Obviously, the stress level at steady-state is reduced much.

9.3.4 Discussion

Ratcheting-induced cracking in passivation film is very common in microelectronic devices. In order to estimate the lifetime in terms of TMCLs, and to avoid this failure mode, 1D simplified model is used. Bree diagram is plotted to check if the ratcheting could happen or not, and the diagram of crack initiation is plotted as the criterion of failure. In addition, the lower bound of the critical number of cycles to initiate the

cracks, i.e., the lifetime, can be estimated by a simple formula. At the end, several suggestions for the design modification are simple, effective and easy to apply in practice.

9.4 Power Packaging Wafer Probing Test and Analysis

The bond pad metallization structure in the power device is shifting from aluminum to copper in recent years. Fundamentally the Young's modulus and yield strength of copper are much higher than aluminum materials. Another advantage of copper is the improved electrical conductivity compared to Al. However, copper oxide, unlike aluminum oxide, cannot act as a protective film to keep the underlying copper layer from further oxidation while exposed to air at the elevated temperature [33]. Reliable bond wire cannot be formed on such oxidized copper surface. Probing bare copper bond pads also challenges existing wafer-probe technology. In order to prevent copper oxidization, one method currently utilized in the semiconductor industry is to add an extra aluminum layer on the copper bond pad [34, 35]. This method will add extra cost in the copper-Fab process. Some research proposed to add an ultra-thin (<30 A) inorganic passivation layer on copper pads [36]. One disadvantage of this method is that the passivation layer would need to be deposited after wafer probing test which also infers that oxidation on the wafer would need to be cleaned off before the passivation film is deposited. In this section, a new method of using copper bond pad with two extra thin layers of Ni and Au is proposed. Reliable bond wire can be formed since the top layer of the bond pad is gold. In order to avoid cracks in interconnect structure and passivation layer, the thickness of Cu, Ni and SiN is optimized by finite element simulations.

Cost competitiveness is a major driving force in the semiconductor industry. Die size reduction is a top priority for cost competitiveness. Advances in processing technology have shrunk the device sizes, resulting in a smaller die core size. However, the space below wire-bond pads has remained relatively underutilized because of the reliability concern that the wire bonding stress and probing stress can cause failures in the underlying devices. In this section [37], a layout technology, termed Bond Pad Over Active (BPOA), is developed to allow the placement of bond pads over active silicon. The reliability of the copper bond pad based BPOA structure is studied during the wafer probing test.

Wafer probing tests are used to evaluate the electrical performance for most manufactured semiconductor devices before assembly. During the test, both electrical and mechanical contacts are made between the probe tip and the bond pad. This may impact the structures below the bond pad, such as dielectric layers and active devices. It may induce very high stress in dielectric and passivation layers since the contact area of probe tip is very small. Both 2D and 3D models are used in the simulations. The impact of passivation thickness and bond pad metal layer thickness is investigated, as well as the probe tip shape and friction between the probe and bond pad. Simulation results show that the trends of different parameters impact of 2D results match well with the 3D results.

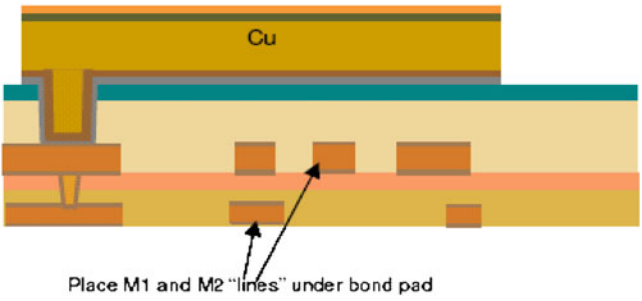


Fig. 9.29 Copper bond pad structure

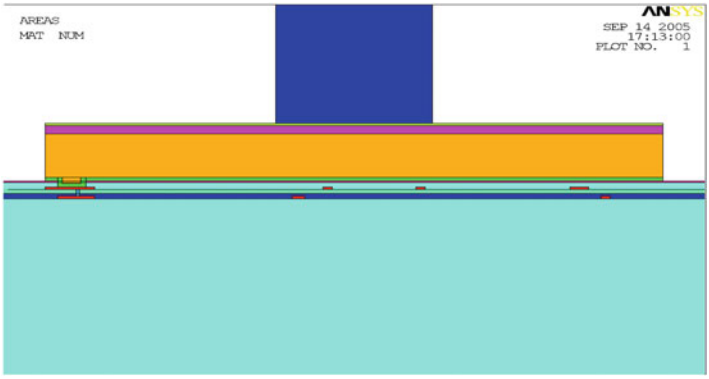


Fig. 9.30 Copper pad FEA 2D solid model (flat probe tip)

9.4.1 2D Analysis Model

Firstly, a 2D model of the copper based strucutre during probing is built. The advantages of such a model are its few meshing constraints, small file size, and fast solution time. It is acceptabel to use the 2D modeling results for comparative purposes rather than to predict absolute values. A copper based bond pad structure is shown in Fig. 9.29. The active circuits are under the bond pad. The bond pad includes an Au film at top, then a Ni film and a thick copper layer and a TiW film at the bottom. Below TiW it is the SiN layer. Then the vias, M1, M2 lines and TEOS layers. The FEA solid model and mesh are shown in Figs. 9.30 and 9.31.

The relationship between probe over travel (OT) and probe tip force has been thoroghly studied in [38], which is listed in Table 9.14. The friction coefficient in the contact model between bond pad and probe tip is 0.3–0.6 (probe tip vs. Au film and then penetrate through Au and Ni films to contact copper). In order to examine the impact of friciton, different friction coefficients are selected for the modeling.

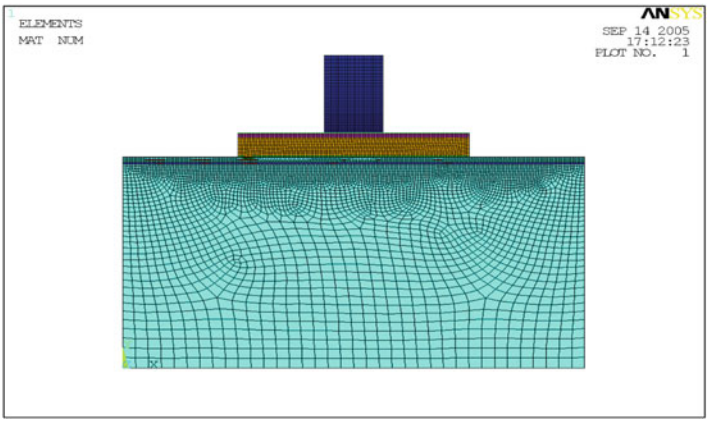


Fig. 9.31 Bond pad model with mesh

Table 9.14 OT vs. contact force (BCF = 2.15 g/mil)

Over travel (mil)	Contact force P (g)	Contact force P (mN)	Contact pressure p (GPa)
2	4.31	42.2	0.0833
4	8.62	84.4	0.167
6	12.93	126.7	0.25
8	17.2	168.9	0.333
10	21.55	211.1	0.417

The horizontal probe scrub (DX) during probe touch down is about 15 μm based on testing. Probe tip is subjected to two loads. One is the probe OT which is converted into probe tip pressure, and the other is the probe scrub.

9.4.2 Simulation Results and Discussion of 2D Model

1. Effect of M2 thickness
   The model parameters and simulation results of the metal 2 layer thickness effect are summarized in Table 9.15. For these two simulations, the probe OT is fixed at 10 mil. It is indicated that the change of metal 2 thickness has little impact on the maximum first principal stress in TEOS and nitride layer.
2. Effect of copper pad thickness
   Five different copper pad thickness is investigated, and the other model parameters are listed in Table 9.16. The probe OT is also fixed at 10 mil. The simulation results show that reducing the thickness of Cu could reduce the first principal stress for both TEOS and SiN; however, it seems that there exists an optimization point.

Table 9.15 Effect of M2 thickness

Model parameters						Simulation results	
Met 2 (μm)	D3 (μm)	SiN (μm)	Cu (μm)	Ni (μm)	Au (μm)	S1 in TEOS (MPa)	S1 in SiN (MPa)
0.55	1	0.8	10	2	0.5	54	244
0.9	1	0.8	10	2	0.5	54	247

Table 9.16 Effect of copper pad thickness

Model parameters						Simulation results	
Met2 (μm)	D3 (μm)	SiN (μm)	Cu (μm)	Ni (μm)	Au (μm)	S1 in TEOS (MPa)	S1 in SiN (MPa)
0.55	1	0.4	15	2	0.5	86	330
0.55	1	0.4	10	2	0.5	73	293
0.55	1	0.4	5	2	0.5	57	249
0.55	1	0.4	3	2	0.5	51	234
0.55	1	0.4	2	2	0.5	47	284

Table 9.17 Effect of Ni layer thickness

Model parameters						Simulation results	
M2 (μm)	D3 (μm)	SiN (μm)	Cu (μm)	Ni (μm)	Au (μm)	S1 in TEOS (MPa)	S1 in SiN (MPa)
0.9	1	0.4	10	1	0.5	43	178
0.9	1	0.4	10	3	0.5	49	198
0.9	1	0.4	10	5	0.5	54	213
0.9	2	0.4	10	1	0.5	44	184
0.9	2	0.4	10	3	0.5	50	204
0.9	2	0.4	10	5	0.5	56	219
0.9	3	0.4	10	1	0.5	45	189
0.9	3	0.4	10	3	0.5	51	209
0.9	3	0.4	10	5	0.5	57	225

3. Effect of Ni layer thickness
   Three different Ni layer thicknesses are investigated, and the other model parameters are listed in Table 9.17. The probe OT is fixed at 6 mil for all the simulations. It can be seen that the maximum first principal stress in TEOS and nitride layer increases with the increase of Ni layer thickness. The dielectric layer 3 has very little impact on the stresses in TEOS and nitride layer.The Ni layer thickness has similar impact on the TEOS and nitride as the copper layer thickness. The max first principal stress of TEOS and nitride locates around the area under the edge of the bond pad. This may explain the effect of copper and Ni layer effect.
4. Effect of SiN layer thickness
   Three different SiN layer thicknesses are investigated, with the other model parameters listed in Table 9.18. The probe OT is fixed at 6 mil for all the

Table 9.18 Effect of SiN layer thickness

Model parameters						Simulation results	
M2 (μm)	D3 (μm)	SiN (μm)	Cu (μm)	Ni (μm)	Au (μm)	S1 in TEOS (MPa)	S1 in SiN (MPa)
0.9	1	0.4	10	3	0.5	49	198
0.9	1	0.8	10	3	0.5	37	164
0.9	1	1.2	10	3	0.5	31	156
0.9	2	0.4	10	3	0.5	50	204
0.9	2	0.8	10	3	0.5	37	169
0.9	2	1.2	10	3	0.5	32	161
0.9	3	0.4	10	3	0.5	51	209
0.9	3	0.8	10	3	0.5	38	173
0.9	3	1.2	10	3	0.5	32	164

Table 9.19 Effect of probe OT

Model parameters						Simulation results	
D3 (μm)	SiN (μm)	Cu (μm)	Ni (μm)	Au (μm)	OT (mil)	S1 in TEOS (MPa)	S1 in SiN (MPa)
1	0.4	5	1	0.5	2	11	49
1	0.4	5	1	0.5	4	22	97
1	0.4	5	1	0.5	6	33	147
1	0.4	5	1	0.5	8	43	193
1	0.4	5	1	0.5	10	52	234

simulations. It can be seen that the maximum first principal stress in TEOS and nitride layer decreases with the increase of nitride layer thickness. It is also confirmed that the dielectric layer 3 has very little impact on the stresses in TEOS and nitride layer.

5. Probe OT effect
   In order to study the effect of probe OT, the metal layer 2 is fixed at 0.9 μm. The other model parameters are listed in Table 9.19, and the simulation results are illustrated in Table 9.19 and Fig. 9.32. The simulation results show that the maximum first principal stress in TEOS and nitride layer increases with the increase of probe OT, and it has the most impact on the SiN layer. This agrees with the results in [39].

9.4.3 3D Model

In order to accurately capture the effects of vias and line layout and further reduce the computation error induced by the assumption of the 2D model, a 3D model is built to study the probing test. But the 3D model takes much longer simulation time. The FEA model and mesh are shown in Figs. 9.33 and 9.34, with half model used because of symmetry.

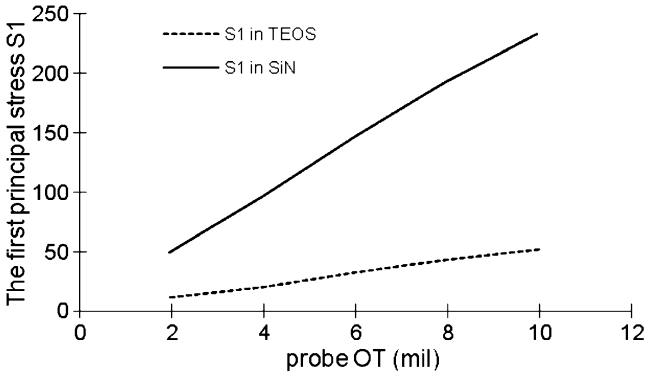


Fig. 9.32 Effect of probe OT

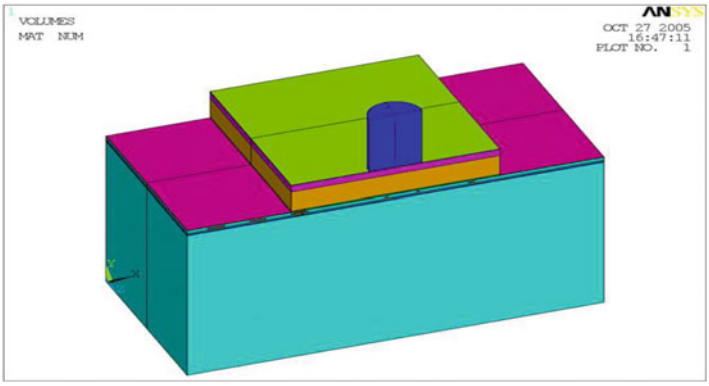


Fig. 9.33 3D solid model (flat probe tip)

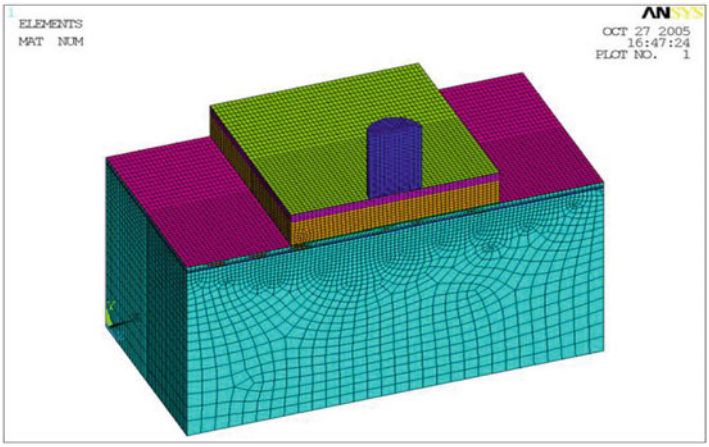


Fig. 9.34 Mesh of the 3D solid model (flat probe tip)

Table 9.20 Model parameters

Model parameters (thickness)							
Met2 (μm)	D3 (μm)	SiN (μm)	Cu (μm)	Ni (μm)	Au (μm)	OT (mil)	DX (μm)
0.9	1	0.4	15	5	0.5	6	15

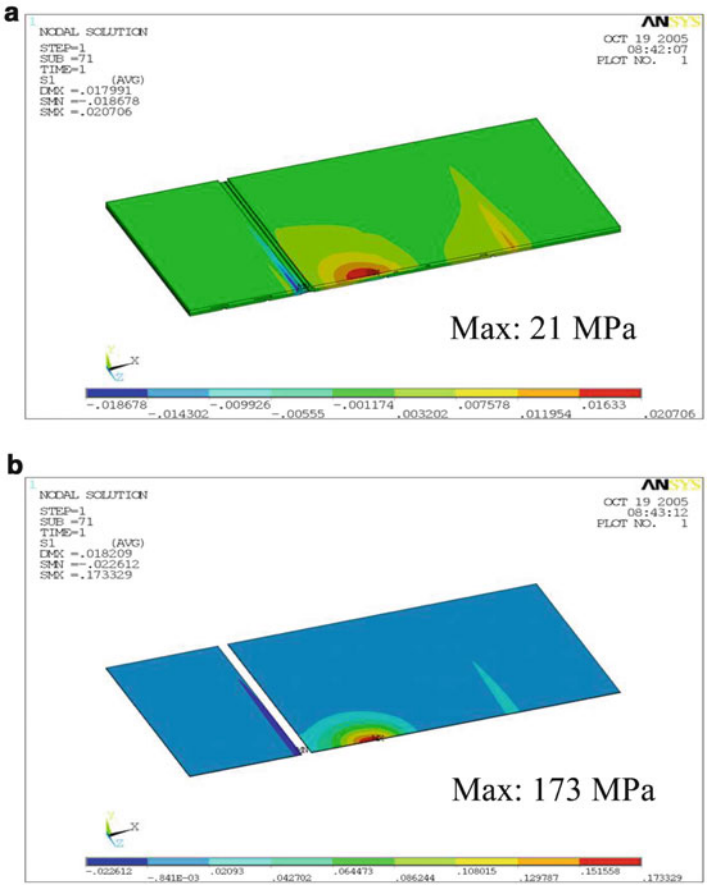


Fig. 9.35 Contour of the first principal stress for round probe tip: (**a**) TEOS, (**b**) nitride layer

9.4.4 Simulation Results and Discussion of 3D Model

1. Effect of probe tip shape
   The model parameters listed in Table 9.20 are used for the 3D simulations. Three types of probe tip shape: flat, flat/round and round are studied to check the effect on the TEOS and nitride layer. The friction coefficient between probe and bond pad is fixed at 0.35. The first principal stress contour in TEOS and nitride layer with the round probe tip is shown in Figs. 9.35a and 9.36b, respectively.

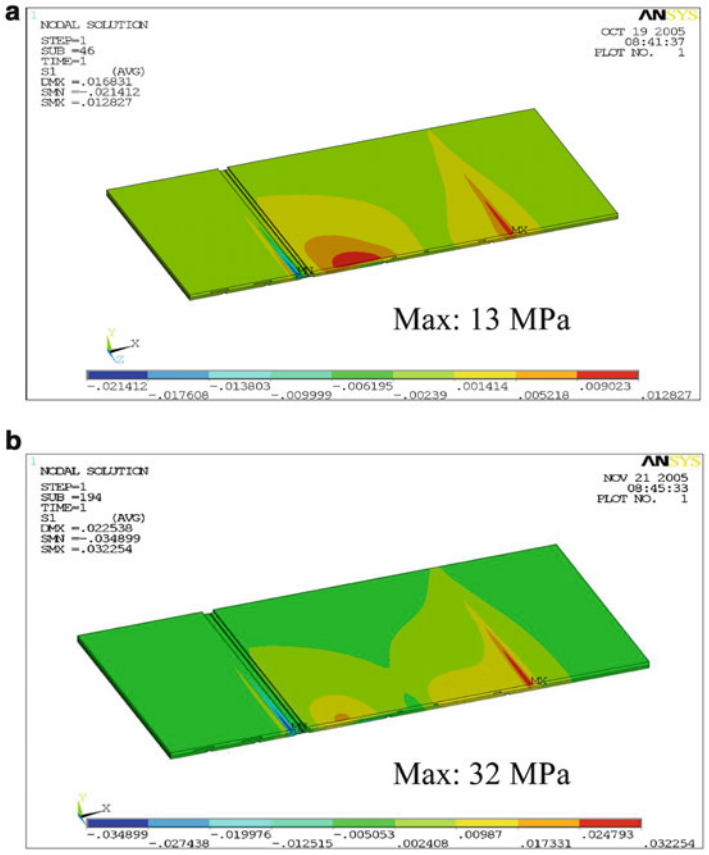


Fig. 9.36 Contour of the first principal stress in TEOS for flat/round probe tip: (**a**) $f = 0.35$, (**b**) $f = 0.8$

The results comparison for the three types of probe tip is illustrated in Fig. 9.37. It can be seen that the flat probe tip generates the lowest stress and the round probe tip generates the highest stress. This agrees well with the previous study in [39].

2. Effect of friction between probe and bond pad
   The model parameters listed in Table 9.20 are adopted. In order to study the effect of friction between the probe and the bond pad, two friction coefficients are used for comparison. One is 0.35, the other is 0.8. The first principal stress contours of TEOS and nitride layer are shown in Fig. 9.38 with flat/round probe tip. The simulation results of different friction coefficient between probe tip and bond pad are shown. It can be seen that with the increase of the friction coefficient, the max first principal stress in both TEOS and nitride layer increases, and it has more impact on the TEOS stress than the nitride layer stress. This also agrees with the 2D case in [39].

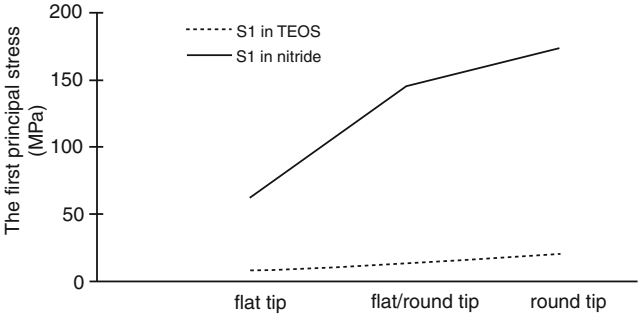


Fig. 9.37 The first principal stress comparison for different probe tip shape

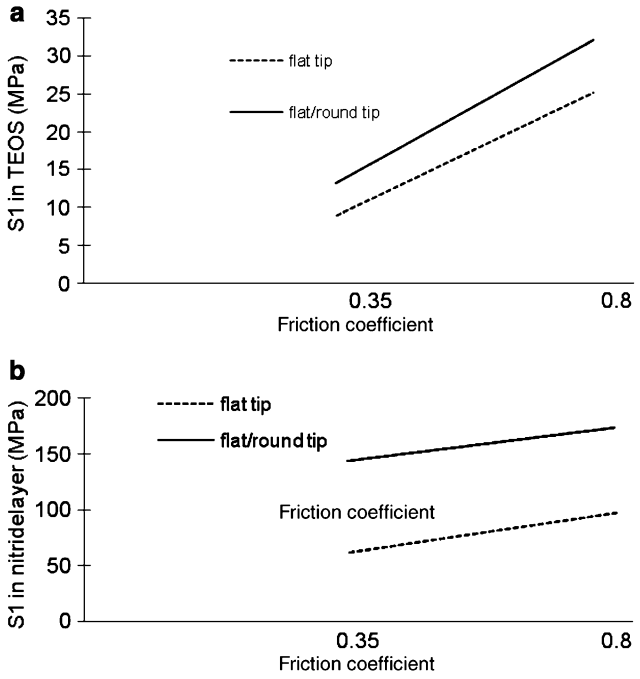


Fig. 9.38 Effect of friction coefficient. (**a**) Tensile stress S1 in TEOS layer. (**b**) Tensile stress S1 in nitride layer

By comparing the 3D simulation results with the 2D case, it is found that the trends match well for each different parameter's impact. Therefore, the 2D model can be used if only for comparative purposes to compare each parameter's impact with the benefit of fast simulation time. Another observation is that the absolute result values of the 3D model are lower than that of the 2D model. This may result from the improper assumptions in the 2D model. So the 3D model is recommended if failure criterion is used to judge the models reliability performance.

In this section, both 2D and 3D probing simulations of copper bond pad based BPOA structure are conducted. According to the 2D simulation results, thinner bond pad, thicker SiN layer and smaller probe OT generate the best result from the viewpoint of the mechanical stress. However, these parameters should be balanced-off according to other factors such as the process feasibility and equipment parameters. Simulation results show that the trends of different parameters impact from 2D results match well with the 3D results. So the 2D model can be used for comparative purposes only. However, the 3D model is recommended if a failure criterion is used to judge the model reliability performance.

9.5 Influence of Heat Sink Mounting Procedure on Power Package Reliability

In this section, the influence of heat sink mount process on the power package reliability is discussed. Different lead frame design and lead frame material options for a power packages are provided for modeling optimization. In simulation, the dynamic procedure of heat sink mounting process is simplified as a qusi static problem. A half package model is built due to its symmetrical structure. In addition, the advanced simulation techniques including both contact analysis and pretension method are introduced to simulate the mounting process. Maximum torque within recommended torque range is applied on different package designs for optimization of the mounting process. Meanwhile possible problems with die cracking and EMC can be predicted. In order to verify the results, actual heat sink mounting process is performed with both previous package design and the optimized package design. Comparison between both designs prove that the optimized package designed by simulation is more robust and reliable.

9.5.1 Background

A heat sink is used to improve heat dissipation to keep device temperatures within limits required to assure reliability of electronics equipment.

Screw mounting is a traditional assembly method, which is still widely used due to quick and easy assembly or disassembly process. In this mounting assembly process, it is very important to find a proper mounting torque. With a low mounting torque, thermal contact resistance will increase due to poor thermal contact under insufficient contact pressure; with a high mounting pressure, large deformation may result in a bad thermal contact and a large thermal resistance. Recently several researchers have focused on thermal aspects and how to enhance package thermal performance more efficiently [40, 41], while few sections have investigated the reliability of the heat sink mounting process. However, the reliability issue is

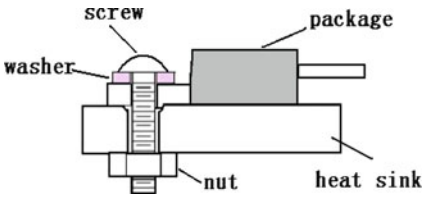


Fig. 9.39 Structures of screw mounting

Table 9.21 Basic material properties [42]

	Ex (MPa)	Nuxy	YS (MPa)	TM (MPa)
Lead frame	130,000	0.35	425	4,250
EMC	16,000	0.35		
Solder	20,000	0.44	28.5	285
Die	161,000	0.2		
Screw, nut, washer	200,000	0.3	379	3,790
Heat sink	70,300	0.346	145	1,450

always a concern because a perfect heat sink design should always be a balance of its thermal and reliability factors.

This section focuses on the reliability analysis in the heat sink mounting process. During screw mounting, a power package is placed on the heat sink, and is fastened by a screw, nut, and washer as shown in Fig. 9.39.

In the screw mounting process, the package internal heat sink and external heat sink are axially fasten by screw and nut. Therefore, the pretension technique in modeling is a method to apply axial force including pretension and recompression to axial object via pretension element. So this section will use the pretension technique as an effective tool to simulate the screw mounting process. Two studies are involved: (1) Impact of lead frame structure to package reliability. (2) Impact of lead frame material properties (Young's modulus and yield strength) to package reliability.

9.5.2 A Model of Heat Sink Mounting for Power Packaging

1. Material properties
   Material properties are listed in Table 9.21; herein, YS stands for yield strength, and TM stands for tangent modulus. Lead frame, die attach solder, heat sink, screw, nut, and washer are all supposed to be elastic–plastic material. In addition, elastic–plastic materials' tangent modulus is estimated to be ten times as its yielding strength due to lack of availability of such data.
2. A model of the heat sink mounting
   A single die power package TO220 is selected here for the heat sink mounting analysis. The package consists of silicon die, die attach solder, lead frame, bond

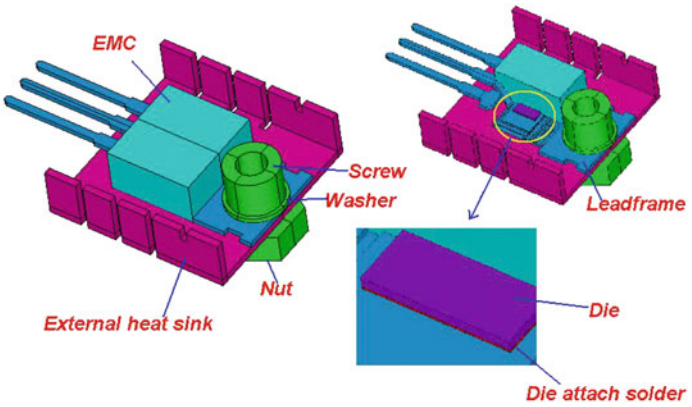


Fig. 9.40 Solid model of the power package heat sink mounting

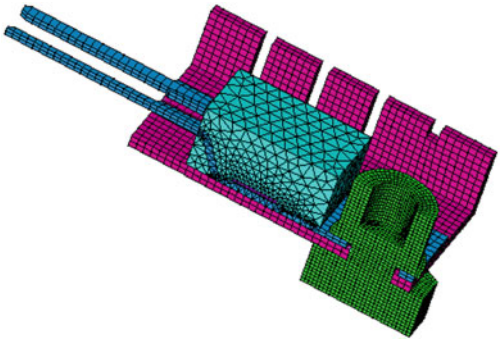


Fig. 9.41 FEA model and mesh

wires, and epoxy mold compound. Bond wires are neglected for simplicity. Detailed structures and meshing are shown in Figs. 9.40 and 9.41.

3. Assumptions
   The following assumptions are made to simplify the problem and speed up simulation:

   1. The dynamic procedure of mount process is simplified as a quasi static problem, and the stress induced by vibration during mounting is ignored.
   2. A half package model is built to reflect whole stress field in package in order to reduce model size and simulation time due to symmetry.
   3. Due to the axial fastening force, a pretension modeling technique is used. The screw line is not considered, the screw, washer, and nut are built into a unitary body.

   Boundary conditions are set as shown in Fig. 9.42, we first build a half model of the package with exteral heat sink, and set symmetry boundary conditions.

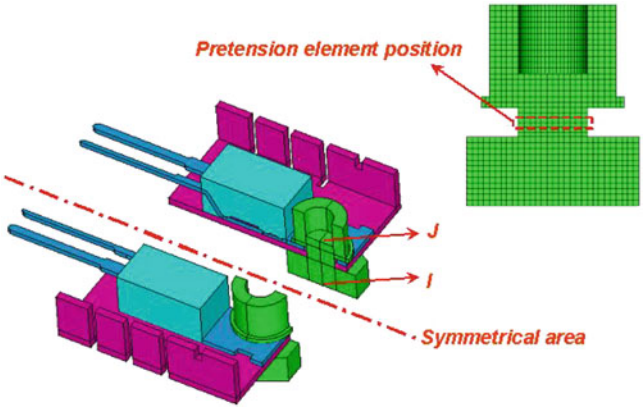


Fig. 9.42 Constraint and load setting

Then, we constrain the three displacement degrees of freedom (x, y, z) at mid point of bottom nut "I"; and constrain two displacement degrees of freedom (x, y) at keypoint "J." In addtion we, set three contact pairs: (1) between screw and package internal heatsink, (2) between package internal heat sink and external heat sink, and (3) between external heat sink and nut. Finally, we create pretension section at the mid point of the screw.

A fastening torque can be transferred to the axial force of the screw as described in (9.27) [43].

$$F = \frac{2T}{d_{\mathrm{m}}}\left(\frac{l + \pi\mu d_{\mathrm{m}} \sec\alpha}{\pi d_{\mathrm{m}} - \mu l \sec\alpha}\right) \tag{9.27}$$

Here, l, d_{m}, μ, and α are the pitch, mean diameter, friction coefficient, and thread angle, respectively. Based on the equation, we can obtain that the axial force for maximum recommended torque is around 1,633 N for the model in this section.

9.5.3 Impact of Lead Frame Design to Package Reliability

Lead frame design plays a very important role for power package development. Three lead frame designs are shown in Fig. 9.43.

The major difference of the three designs is the difference of the groove design area between die attach and package case. Three designs include 3 grooves, 2 grooves, and 1 groove, separately. These grooves are used to release stress induced by heat sink mounting process so that the potential for silicon die damage will be reduced. In addition, delamination between lead frame and EMC can be improved.

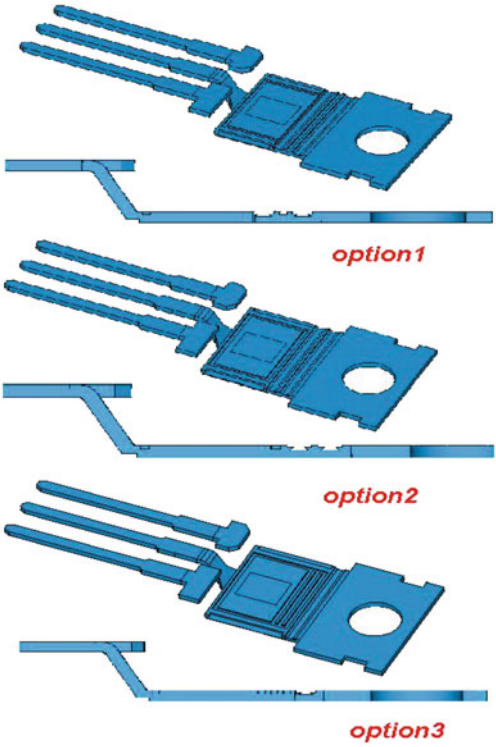


Fig. 9.43 Different lead frame design options

As it is known that the silicon die is a brittle material, so its first principal stress can reflect its possibility of cracking if the active stress on die exceeds the silicon tensile strength; EMC is normally taken as viscoplastic material, but it is still can be treated as brittle material at room temperature due to the quick mounting process. So its first principal stress, pull stress across interface between lead frame and EMC, and shear stress along the interfaced are considered to reflect the possibility of EMC cracking and the possibility of delamination.

A typical von Mises stress contour of the lead frame for design 1 is shown in Fig. 9.44. We can find that high stress region locates around screw joint position. Its maximum value is about 637.3 MPa, which exceeds the copper's yield stress. This shows that the lead frame has local elastic plastic deformation at the high stress region.

Figure 9.45 shows the first principal stress on die for all three lead frame design options. The maximum stress appears at the center of bottom edge near the mounting side, from 3.4 to 3.9 MPa, which obviously is far below typical silicon die tensile strength 236 MPa [42]. So die will not crack for all three options during heat sink mounting process with the maximum recommended torque; in addition,

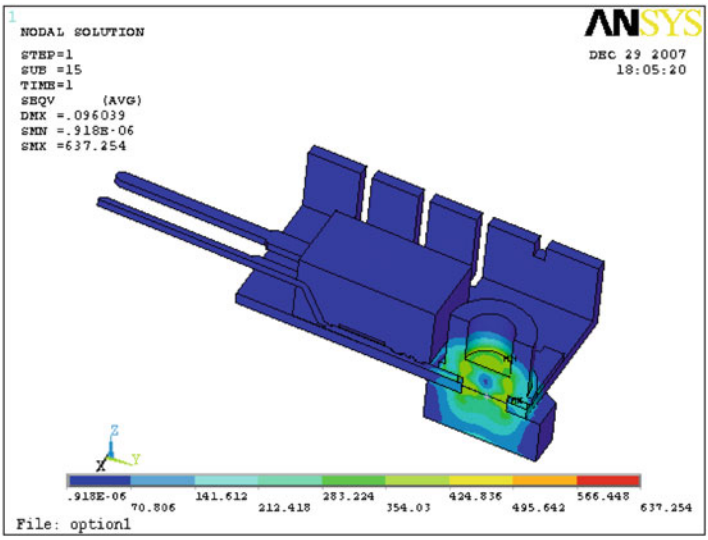


Fig. 9.44 von Mises stress contour for half model of lead frame design 1 (Max: 637.3 MPa)

based on the stress difference on die between different designs, we can find that the first principal stress is not sensitive to the lead frame structure.

Figure 9.46 gives the peeling stress Sz distribution on EMC. Sz is across the interface which stands for pull stress. The results show that mounting process with lead frame option 1 gives smallest stress, while lead frame option 3 gives relative larger stress. The peeling stress Sz may be the root cause to induce the possible delamination between lead frame and EMC if the adhesion strength is less than 110 MPa.

All the stresses components with maximum first principal stress S1 of die and EMC, maximum peeling stress Sz and shear stress Sxy of EMC which are based on different lead frame designs, are summarized in Fig. 9.47. Results show that die will not be cracked for any of the three lead frame designs. EMC cracking or delamination at interface of EMC and lead frame are of greater concern. Maximum stress level appears in option 3, while the minimum stress level appears in option 1. Design option 1 reduces the first principal stress and z axial stress of EMC by nearly half, as compared to design option 3. Therefore, design one is most resistant to damage during heat sink mounting process.

9.5.4 Impact of Lead Frame Material Property

Different lead frame materials will have different material mechanical properties, which can have an influence on the package reliability. During the heat sink mounting process, Young's modulus and yield strength are considered as two major factors which will impact the results.

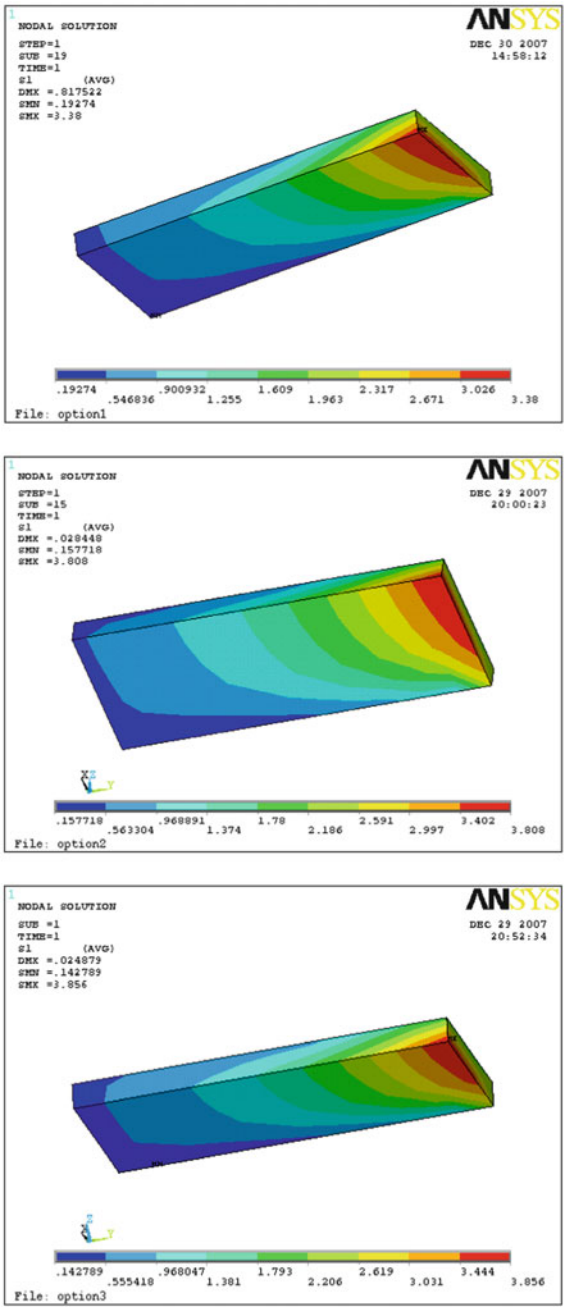


Fig. 9.45 First principal stress on half die with three lead frame options. Option 1, Max stress 3.4 MPa. Option 2, Max stress 3.8 MPa. Option 3, Max stress 3.9 MPa

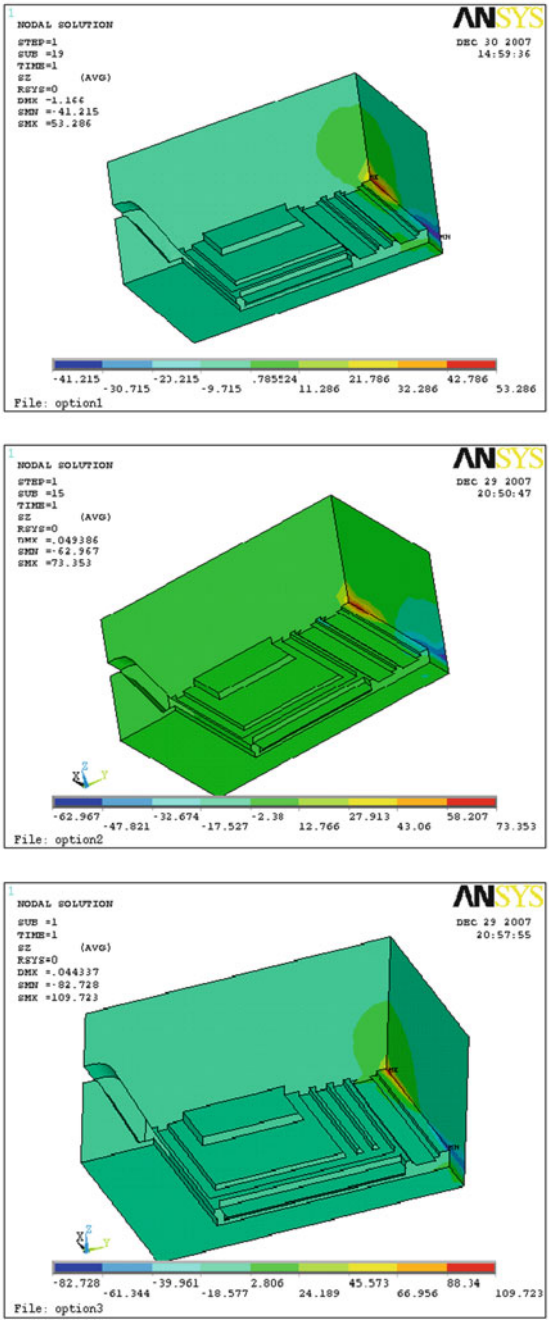


Fig. 9.46 Peeling stress Sz on half EMC with three lead frame options. Option 1, Max stress: 53.3 MPa. Option 2, Max stress: 73.4 MPa. Option 3, Max stress: 109.7 MPa

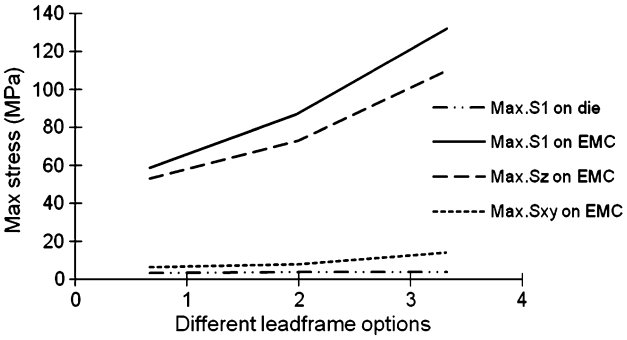


Fig. 9.47 Maximum stress on die and EMC for different lead frame designs

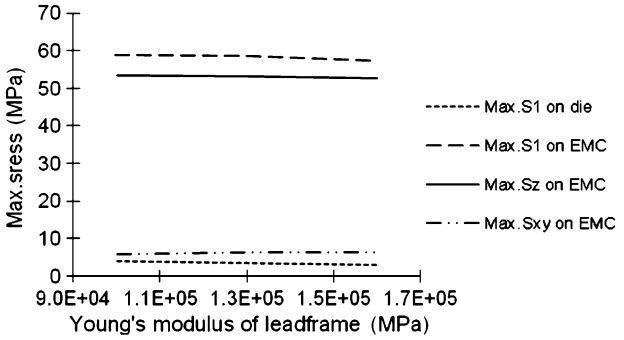


Fig. 9.48 Maximum stress on die and EMC for different Young's modulus of lead frame

First the impact of Young's modulus of lead frame is investigated. All materials properties, except the lead frame Young's modulus, are based on the data in Table 9.21. Previous result based on lead frame design 1 is used as the reference case. Two additional simulated experiments are run, in the first the Young's modulus is set to 100,000 and 160,000 MPa. All results, including the reference case, are shown in Fig. 9.48.

In Fig. 9.48, all curves are nearly flat, which means that maximum stress on the die and EMC will not change much as the Young's modulus of the lead frame is increased.

Similarly, the impact of the yield strength of the lead frame is investigated. All materials properties except lead frame yield strength are based on the data in Table 9.21. The previous result based on lead frame design 1 is also set as reference case. Two additional simulated experiments are run. The yield strengths are set as 300 and 600 MPa. All results, including the reference case, are indicated in Fig. 9.49.

As shown in Fig. 9.49, the yield strength of lead frame has very little influence on maximum stress of die and EMC.

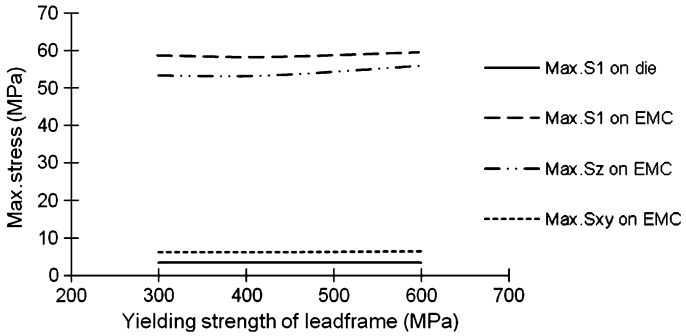


Fig. 9.49 Maximum stress on die and EMC for different yielding strength of lead frame designs

Table 9.22 Failure ratio comparison between design 1 and 3

	Delamination or die cracking problems (fails/total samples)			
Torque	6 kgf cm	9 kgf cm	12 kgf cm	15 kgf cm
Previous package design (option 3)	7/20 (35%)	11/20 (55%)	14/20 (70%)	14/20 (70%)
Optimized package design (option 1)	0/20	0/20	0/20	0/20

In short, both Young's modulus and yielding strength will not significantly impact the stress in the heat sink mounting process. To design a robust package, it is not necessary to choose different lead frame materials.

9.5.5 Actual Heat Sink Mounting Test

Actual heat sink mounting test was performed, and previous package design (option 3)and optimized package design (option 1) are compared. Four levels of torque areapplied on the samples. Twenty packages are selected to be tested for each torque level. The failure ratio of the test are listed in Table 9.22.

The test result shows that the optimized package design (option 1) is robust and even at large torque 15 kgf cm, there is still no any delamination and die cracking problems.

9.5.6 Discussion

This section investigates the influence of heat sink mounting on the reliability of package. Two studies are involved: (1) Impact of lead frame design on package

reliability and (2) Impact of lead frame material properties (Young's modulus and yielding strength) on package reliability. Simulation results show that all three lead frame designs with grooves can secure die from damage during screw mounting and lead frame design 1 is the most robust, which will improve reliability issue for both EMC cracking and delamination at interface of lead frame and EMC. While different lead frame materials do not have significantly impact to the stress induced by the heat sink mounting process, it is not recommended to design a robust package by the way choosing different lead frame material. Finally, actual screw mounting test proves that the optimized package design is the most robust, and even with large torque 15 kgf cm, there is still no any delamination and die cracking problems.

9.6 ACLV Moisture Analysis of Power Package

Moisture induced die surface metal layer corrosion is a critical reliability problem which may cause eletrical failures. In this section, the impact of solder overflow and moisture absorption of mold compound on the die surface metal layer in ACLV are investigated. Comprehensive analysis of the modeling results for die surface metal layer moisture concentration is presented. The assembly process is optimized to reduce solder overflow after the modeling. Practical tests of the solder overflow and moisture absorption factors of mold compound are carried out. Both modeling and testing have confirmed that solder overflow and mold compound's moisture absorption have a significant impact to die surface metal layer's moisture concentration.

Assembly process induced faults (such as solder overflow) and moisture absorption in mold compound could generate high moisture concentration at the die surface metal layer [44–46]. It would induce metal corrosion. Delamination between soft solder and mold compound would appear if the adhesive strength becomes low at high moisture absorption levels. Solder overflow and moisture absorption will speed up the delamination at the die surface metal layer during ACLV test. This issue has been existed in the industry for a long time, but there are few studies that have shown effective methodology how to resolve it.

The work of this section inclides two parts: The first part is to check the impact of solder overflow and to compare die surface metal layer's moisture concentration between solder overflow model and solder without overflow model. The second part is to investigate the moisture absorption of mold compound. Both with solder overflow model and without solder overflow models are investigated. Moisture concentration level on the die metal layer is simulated with different mold compounds under the ACLV test conditions (96 h 121°C/100%RH). Finally, comprehensive analysis of the simulation results for die surface metal layer moisture concentration is presented. The assembly process is optimized to reduce solder overflow after the modeling.



Fig. 9.50 Melt solder on DAP of a lead frame

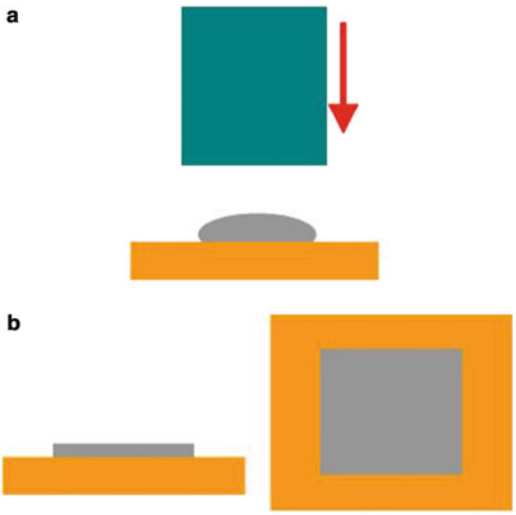


Fig. 9.51 Melt solder flattening. (**a**) Melt solder flattening. (**b**) Flattened melt solder

9.6.1 Solder Overflow in Die Attach Process and Finite Element Models Description

During the eutectic die attach process, a lead frame is held on the surface of heater block. The soft solder wire is then placed on the lead frame. The temperature of the heater block ramps up to the melting temperature of solder which makes the wire fuse. The melt solder is not flat due to surface tension (as shown in Fig. 9.50). It will be flattened to reduce die tilt and increase solder coverage. A typical melt solder flattening process is shown in Fig. 9.51. A smoothing tool in the solder attach equpiment moves down and flattens the melt solder and changes the round solder

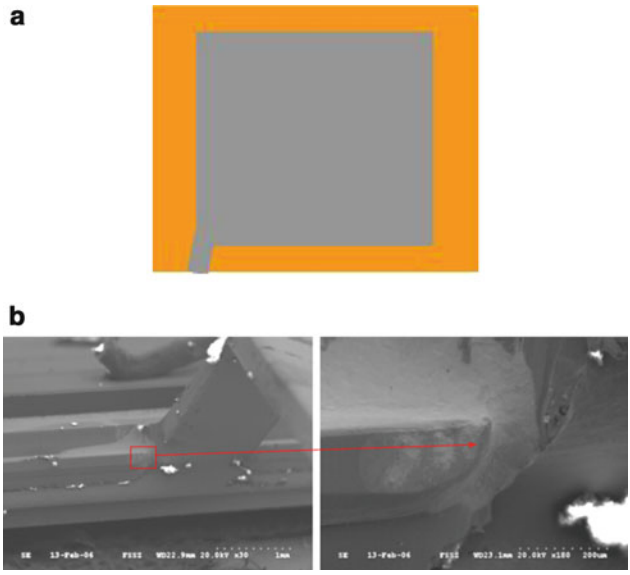


Fig. 9.52 Solder overflow in lead frame. (**a**) Solder overflow due to die attach process. (**b**) Actual picture of solder overflow

bump into square shape. Finally, the die pickup tool takes the die and moves the die to the flattened melt solder on the lead frame.

Demands for larger die sizes have driven an increasement of solder size in package, which may induce solder overflow in the melt solder flattening process. Figure 9.52 shows a solder overflow example. Solder overflow appears beside the middle lead. A solder overflow finite element model is generated based on this real example. Figure 9.53 shows the 3D finite element mesh of a typical TO220 package and solder overflow from lead frame. Lead frame, solder, die, wire bonding, and epoxy mold compound are considered in this model. The size of die is 4.7 $\times$ 6 mm with 0.3 mm thickness. With solder overflow model, solder size (5.2 $\times$ 6.2 mm with 0.05 mm thickness) is a little larger than die size. For the model without solder overflow, solder size is same as die size.

Ideal model without the solder overflow is also included in the study. For the solder overflow model, the initial delamination between the overflowed solder and mold compound due to the low adhesive strength between solder and mold compound is introduced. The initial delamination may propagate during ACLV test due to CTE mismatch of different material in package. In order to solve the problem effectively, only the initial delamination is considered in simulation.

The saturated moisture concentration of mold compound is 1.14E $-$ 2 mg/mm^3. Moisture diffusivity is 3.47E $-$ 06 mm^2/s. In the second part of the simulation work, the new mold compound's saturated moisture level is 0.84E $-$ 2 mg/mm^3, and moisture diffusivity is 2.41E $-$ 06 mm^2/s.

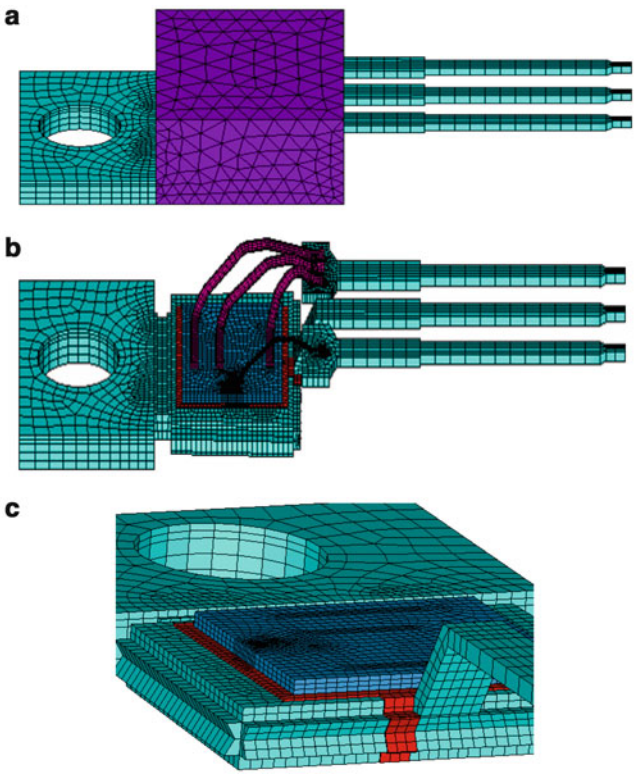


Fig. 9.53 Solder overflow from lead frame DAP. (**a**) Mesh of the 3D model. (**b**) Mesh of 3D model (hiding the EMC). (**c**) Mesh of solder overflow from lead frame

9.6.2 Effect of Solder Overflow

Die size is selected relative large. Moisture concentration at die surface metal layer may be quite different after the ACLV test. Six different positions at die surface metal layer are compared throughout the ACLV test. Since the gate area is much smaller than source area, one position is selected at gate metal area and the other five positions are selected at source metal area (as shown in Fig. 9.54) in the models.

The moisture cannot penetrate the lead frame; therefore, the diffusion path is through the mold compound. Moisture diffuses into the package through the top surface, the vertical surface, and the bottom surface of mold compound, as shown in Fig. 9.55.

Moisture soak simulation results are shown in Figs. 9.56 and 9.57. Figure 9.56 shows moisture concentration history at five positions of metal layer of die top surface in the ACLV test without solder overflow. Moisture concentration at position source 1 is much higher than that of the rest four source positions. The reason is that the position of source 1 is near the left surface of mold compound.

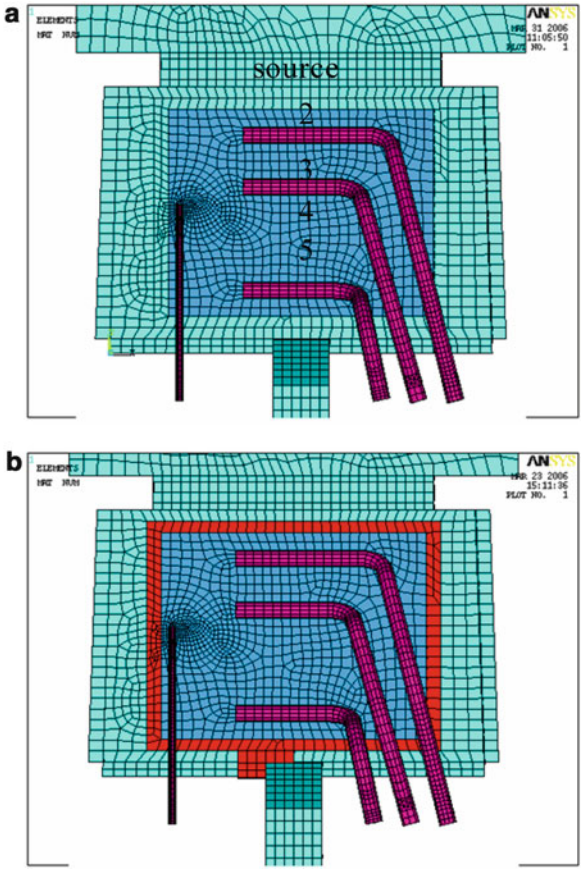


Fig. 9.54 Mesh of lead frame, solder, die, and wire bonding. (**a**) Without solder overflow. (**b**) With solder overflow

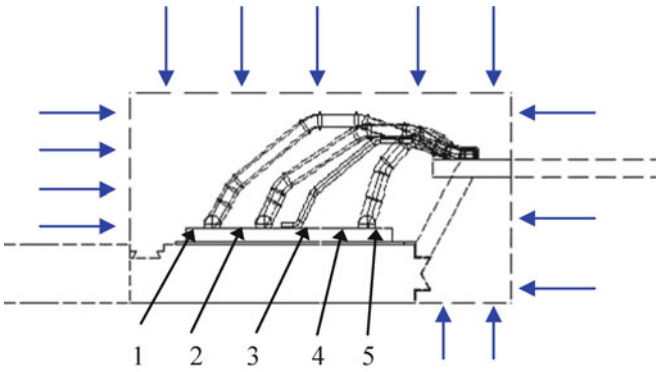


Fig. 9.55 Moisture diffuses into the package through mold compound surface

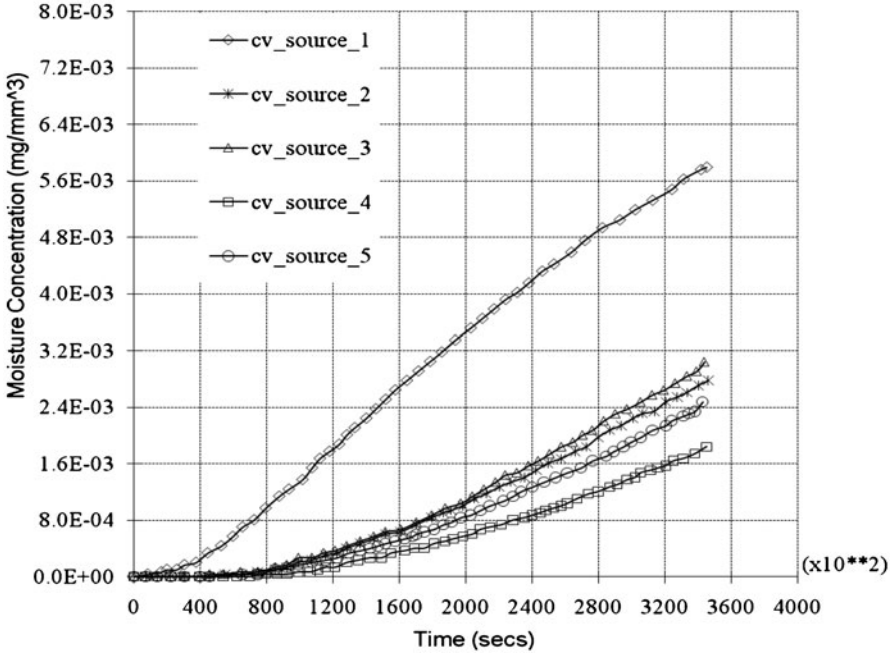


Fig. 9.56 Moisture concentration history of mold compound at die surface without solder flow

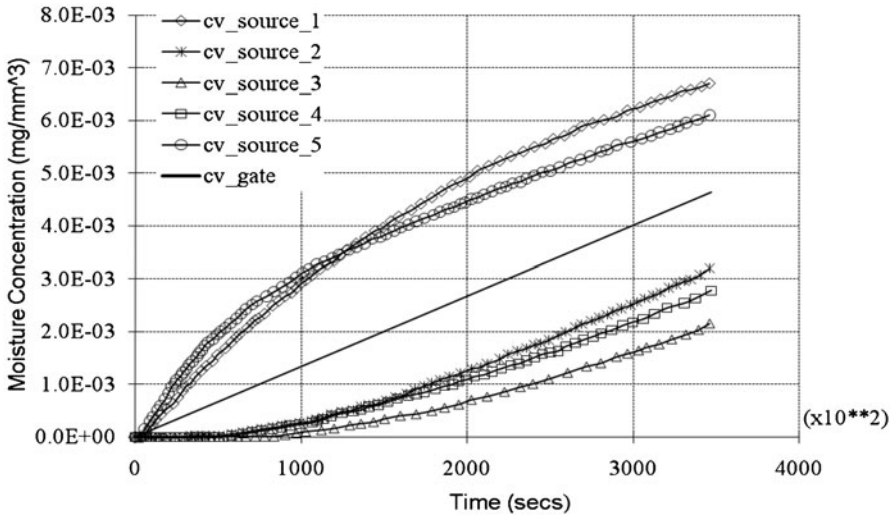


Fig. 9.57 Moisture concentration history of mold compound at die surface with solder flow

Moisture can diffuse through mold compound and reach position source 1 relative fast. Figure 9.57 shows moisture concentration history at the same five positions in ACLV test with solder overflow. As compared to the model without the solder

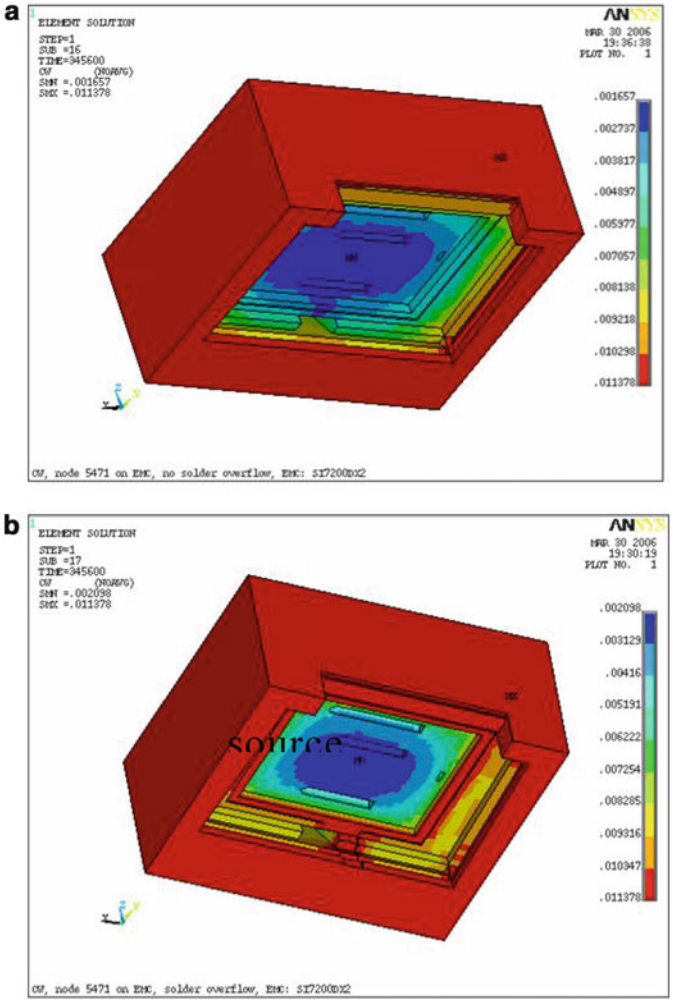


Fig. 9.58 Moisture concentrate contour of EMC. (**a**) Without solder overflow. (**b**) With solder overflow

overflow, moisture concentrations at all of the five positions increase. Moisture concentration at position of source 5, which is near the delamination area between mold compound and solder, increases dramatically.

Figure 9.58 gives simulation results of moisture soak after 96 h at 121°C/100% RH. The outer boundary and delamination area of mold compound has the highest moisture, and the inner boundary at the internal surface of die has much lower moisture levels. Table 9.23 gives the moisture concentration of six positions (gate and source) with and without solder overflow after 96 h with 121°C/100%RH.

Table 9.23 Moisture concentration at die surface metal layer after ACLV test

	Moisture concentration (1E − 3 mg/mm^3)					
	Gate	Source				
	1	1	2	3	4	5
No solder overflow	2.95	5.74	2.74	1.77	1.77	2.42
Solder overflow	4.84	7.37	3.27	2.12	2.72	6.06

Table 9.24 Moisture concentration of die surface metal layer after ACLV test (without solder overflow)

	Moisture concentration (1E − 3 mg/mm^3)					
	Gate	Source				
	1	1	2	3	4	5
Initial EMC	2.95	5.74	2.74	1.77	1.77	2.42
New EMC	1.14	3.13	1.05	0.59	0.58	0.86

Table 9.25 Moisture concentration of die surface metal layer after ACLV test (with solder overflow from lead frame)

	Moisture concentration (1E − 3 mg/mm^3)					
	Gate	Source				
	1	1	2	3	4	5
Initial EMC	4.84	7.37	3.27	2.12	2.72	6.06
New EMC	2.48	4.57	1.35	0.71	1.10	3.65

9.6.3 Effect of Mold Compound

The effect of the moisture absorption in different mold compound is investigated in this section with comparison of a new mold compound and the initial mold compound. The comparison result of the two mold compounds is listed in Tables 9.24 and 9.25.

Table 9.24 gives moisture concentration comparison in die metal layer of the two mold compounds without solder overflow. Table 9.25 gives comparison of two mold compounds with solder overflow. The results show that the low moisture absorption mold compound induces lower moisture concentration at die metal layer.

9.6.4 Process Improvement and Experimental Data

A solder rim is introduced around the melt solder during the solder flattening process (see Fig. 9.59). The solder rim will clamp the lead frame DAP and prevent solder overflow when the solder is flattened.

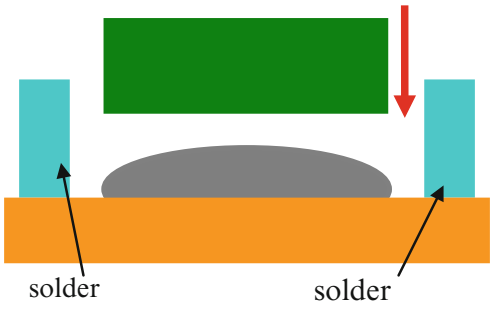


Fig. 9.59 Solder flattening process improvement

Different mold compound, with and without solder overflow packages were run to determine the efficiency of process and material change. The sample size consists of 308 U. Figure 9.60 shows the electrical test results after ACLV (96 h, 121°C/100%RH). For the initial mold compound, there are five failures in without solder overflow units and eight failures in with solder overflow units. For the new mold compound, there is one failure in with solder overflow units and no failure in without solder overflow units.

From the above study, we learnt both the effect of assembly process induced faults (solder overflow) and the moisture absorption in mold compound:

1. Moisture absorption of mold compound has a larger impact on die surface metal layer with solder overflow after ACLV test.
2. Experimental data shows a significant improvement in reliability for package by using a solder rim during the die attach process and using low moisture absorption mold compound, as predicted by the simulations.

9.7 Drop Test Reliability of Wafer Level Chip Scale Package

The trends of next-generation WL-CSP are toward thinner and finer pitch with micro bumps, this is true for both power and analog chips. The mechanical shock resulted from mishandling during transportation or customer usage may cause WL-CSP package solder joints failure [47]. Since the board level drop test is a key qualification test for portable electronic products, it is becoming a topic of great interest by many researchers [48, 49]. Most of the drop test and modeling works focus on the failure mode which was based on solder joint. The impact of WL-CSP design, such as geometry of the UBM, metal stack under UBM, the polyimide and the solder joint height, has not yet been fully investigated. This section addresses these WLCSP design variables and their impacts on the drop test performance.

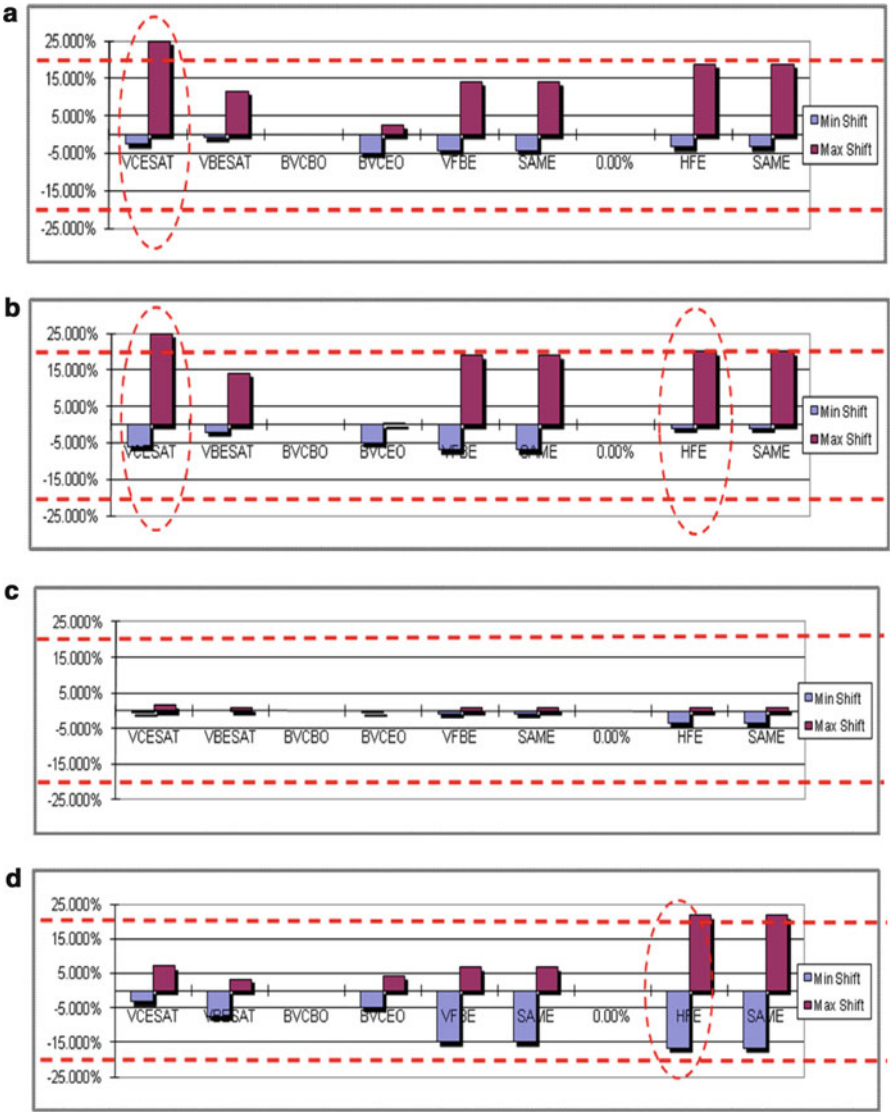


Fig. 9.60 Electrical test results after ACLV test. (**a**) Without solder overflow, high moisture absorption of mold compound (initial mold compound). (**b**) With solder overflow, high moisture absorption of mold compound (initial mold compound). (**c**) Without solder overflow, low moisture absorption of mold compound (new mold compound). (**d**) With solder overflow, low moisture absorption of mold compound (new mold compound)

9.7.1 WL-CSP Drop Test and Analysis Model Setup

The drop test setup is based on the JEDEC Standard JESD22-B111 [17]. The board, with a dimension of 132 × 77 × 1.0 mm, accommodates 15 components of the same type in a three row by five column format.

Due to the symmetry, a quarter finite element model (66 × 38.5 × 1 mm) of a JEDEC board with WLCSP chips is selected. Figure 9.61 shows a finite element model of the lower left quarter part of the test board with six components U1, U2, U3, U6, U7, and U8, which are numbered according to the JEDEC Standard. The line AB in Fig. 9.61a is defined across the board with a distance of 1 mm away from edges of components U1–3. There are six corner points on PCB defined 1 mm below each of the six packages and 1 mm distance left from each of the six packages.

Figure 9.61b shows the finite element model of the cross section of the corner joint for a WL-CSP structure. The basic setting includes a 2.7-μm thick aluminum pad, 2 μm thick UBM with 0.5 μm Au and 0.2 μm Cu, a 0.9 μm thick passivation that covers 5 μm edge of the aluminum pad. A 10 μm thick polyimide layer is above the passivation and the aluminum pad. There is a 200 μm diameter via open in the polyimide layer; its side wall angle (between its slope and the bottom surface) is 60°. The UBM connects to the aluminum pad through the via and the solder is placed on the UBM and connect to copper post on the PCB board.

Table 9.26 defines the elastic modulus, Poisson's ratio, and density of each material. The silicon, passivation, polyimide, PCB, and UBM are considered as linear elastic material, while the solder ball, aluminum pad, and PCB copper pad are considered as the nonlinear material properties. Table 9.27 gives the nonlinear property for solder SAC405 that is considered as a rate-dependent Peirce model, see (9.28). The data was obtained through the Hopkinson dynamic material high speed impact test.

$$\sigma = \left[1 + \frac{\dot{\varepsilon}^{\mathrm{pl}}}{\gamma}\right]^{\mathrm{m}} \sigma_0 \tag{9.28}$$

where σ is the dynamic material yield stress, $\dot{\varepsilon}^{\mathrm{pl}}$ is the dynamic plastic strain rate, σ_0 is the static yield stress, m is the strain rate harden material, and γ is the material viscosity parameter.

The direct acceleration input (DAI) method is applied in this study. In this method, an acceleration impulse is applied as an inertia that is specified with thelinear acceleration of the structure at each time step. The surfaces of mounting holes are constrained during dynamic impact. Therefore, the problem formulation becomes

$$\{M\}[\ddot{u}] + \{C\}[\dot{u}] + \{K\}[u] = \left\{ \begin{array}{ll} -\{M\}1,500\ \mathrm{g}\ \sin\dfrac{\pi t}{t_{\mathrm{w}}} & \text{for } t \le t_{\mathrm{w}},\ t_{\mathrm{w}} = 0.5 \\ 0 & \text{for } t \ge t_{\mathrm{w}} \end{array} \right\} \tag{9.29}$$

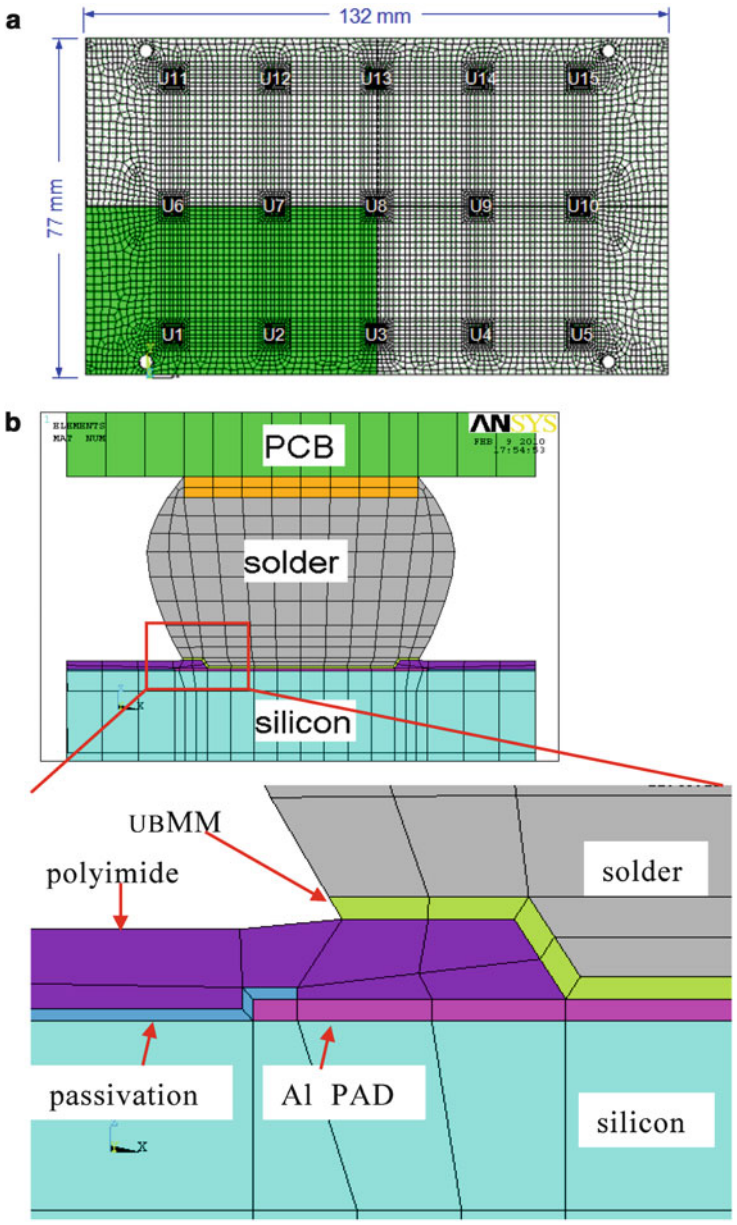


Fig. 9.61 Finite element model of the WLCSP. (**a**) Finite element model of PCB with quarter chip units (U1–8). (**b**) The cross section and design variable

Table 9.26 Elastic modulus, Poisson ratio, and density of each material

	Modulus (GPa)	Poisson ratio	Density (g/cm^3)
Silicon	131	0.278	2.33
Solder	26.38	0.4	7.5
Passivation	314	0.33	2.99
Polyimide	3.5	0.35	1.47
PCB	Ex = Ey = 25.42	Nuxy = 0.11	
	Ez = 11	Nuxz = Nuyz = 0.39	
	Gxz = Gyz = 4.91		1.92
	Gxy = 11.45		
Cu PAD	117	0.33	8.94
Al PAD	68.9	0.33	2.7
UBM	196	0.304	9.7

Table 9.27 Rate-dependent Peirce model of solder SAC405

	Static yield stress (MPa)	γ	m
Solder (SAC405)	41.85	0.00011	0.0953

With initial conditions

$$[u]_{t=0} = 0$$

$$[\dot{u}]_{t=0} = \sqrt{2gh} \tag{9.30}$$

where h is the drop height, and the constraint boundary condition is

$$[u]_{\text{at_holes}} = 0 \tag{9.31}$$

9.7.2 Drop Impact Simulation/Test with Different Design Variable and Discussion

9.7.2.1 Impact of Design Variable Polyimide Side Wall Angle

The polyimide layer connects both the aluminum pad and UBM, see Fig. 9.61b.

Figure 9.62 shows the max peeling stress comparison of the solder, copper pad, and aluminum pad with different polyimide side wall angles at location U1. The stresses in the copper pad, aluminum pad, and solder interface connected to the copper pad show that there is no significant difference with different polyimide side wall angles. However, there is impact on the solder joint interface that adhered to UBM.

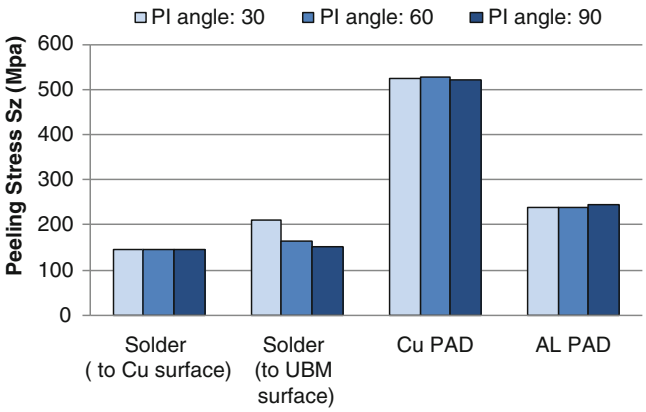


Fig. 9.62 Comparison of max peeling stress at U1 with different polyimide side wall angle

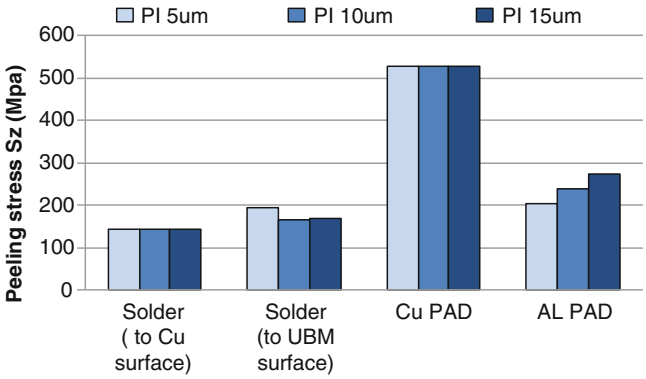


Fig. 9.63 Comparison of max peeling stress at U1 of different polyimide thickness

9.7.2.2 Impact of Design Variable Polyimide Thickness

The polyimide thickness is selected to be 5, 10, and 15 μm, respectively. Figure 9.63 shows the peeling stress for the solder, copper pad and aluminum pad with different polyimide thickness at location U1. The peeling stress on the aluminum pad increases as polyimide thickness increases from 5 to 15 μm. The solder stress at the interface with UBM decreases when the polyimide thickness increases from 5 to 10 μm; however, after 10 μm, there is no significant difference.

9.7.2.3 Impact of Design Variable UBM Structure

A copper UBM structure is designed to compare with the existing 2 μm nickel standard UBM with 0.5 μm Au and 0.2 μm Cu. The thickness of copper UBM is 8 μm.

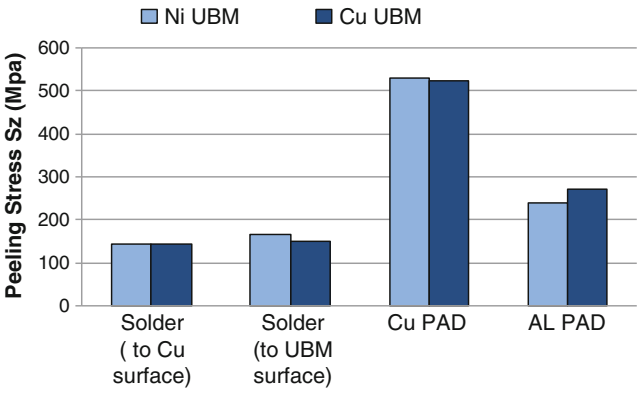


Fig. 9.64 Comparison of max peeling stress at U1 with two different UBM designs

Figure 9.64 shows the peeling stress comparison for the solder joint, copper pad, and aluminum pad with copper UBM and with standard UBM of the package at location U1. From Fig. 9.64, it can be seen that the peeling stress on the solder joint interface attached to the standard UBM is greater than that attached to the copper UBM. However, the peeling stress on Al pad with copper UBM is greater than standard UBM.

9.7.2.4 Impact of Design Variable Aluminum Pad Thickness

Different aluminum pad thicknesses with 0.8, 2, 2.7, and 4 μm are simulated.

Figure 9.65 gives the polyimide stresses vs. the Al pad thickness and its correlation with the drop test life (dot line). There is a optimized Al thickness from both modeling and drop test result.

9.7.2.5 Impact of Design Variable Solder Joint Height

Different solder joint heights with 50, 100, 200, and 300 μm are considered. Figure 9.66 gives the trends of solder joint plastic energy density with different heights. In all three package locations, the higher the solder joint, the less the plastic energy density. This indicates that the higher solder joint height can help to improve the WLCSP drop test dynamic plastic energy performance.

9.7.3 Drop Test

The drop test was done based on JEDEC Standard JESD22-B111. The test condition is 1,500 g with half sine wave in 0.5 ms. Drop count is 1,000. A total of 90 U were investigated and mounted on eight JEDEC PCBs for two groups with and

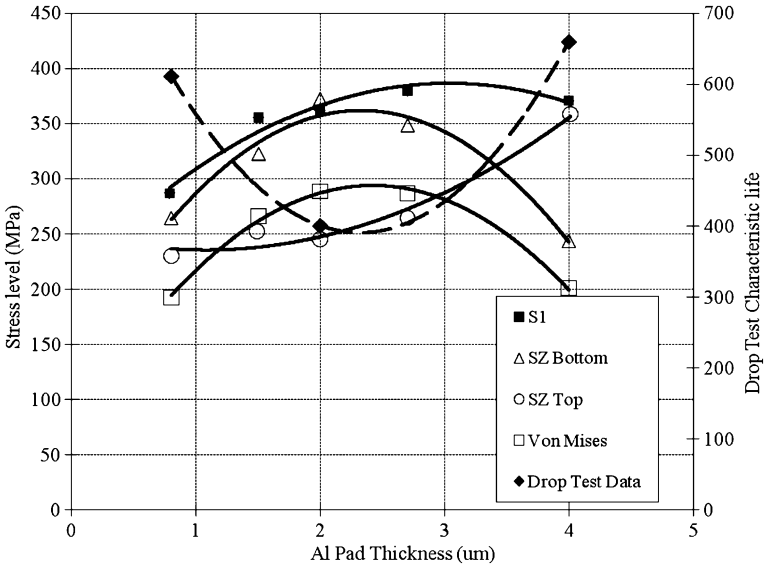


Fig. 9.65 PI stress vs. Al pad thickness

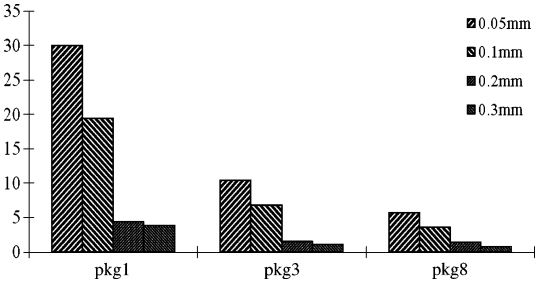


Fig. 9.66 Plastic energy density of solder joint (MPa)

without the vias under the copper pads. Most of the failure of the solder joints appeared at the PCB corner location U5, U11, and U15. Figure 9.67 gives the copper pad/crack which locates at the interface of solder and copper to the PCB at U15. The test results have correlated the simulation result that the max first principal strain appears at the location of U1 which has the same behaviors of U5, U11, and U15 due to the model symmetric property (see Fig. 9.68). Figure 9.68 gives the first principal strain curves at the interface of the copper pad, solder, and PCB with the different package location U1, U3, and U8. The failure rank is U1 > U3 > U8. When the dynamic first principal strain reaches the failure strain, the copper pad/trace will break/crack.

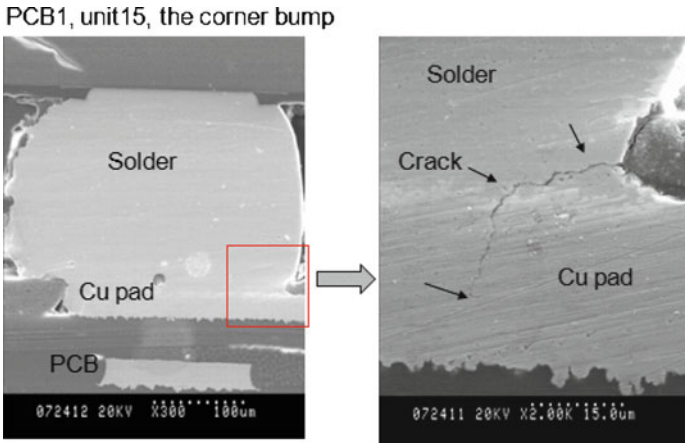


Fig. 9.67 Drop test failure mode at corner joint of U15 location

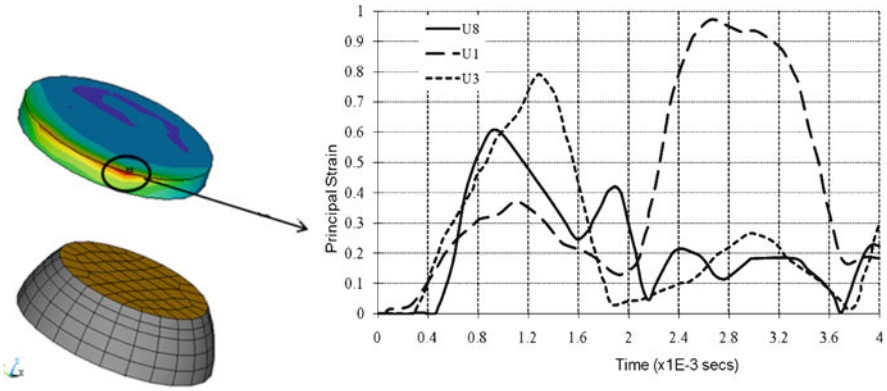


Fig. 9.68 First principal strains of copper pad at the interface of solder, copper pad, and PCB with package location U1, U3, and U8

9.8 Summary

This chapter introduces the reliability analysis and tests in power semiconductor packaging. First, the general concepts of general reliability life and failure rate are presented following by typical reliability tests with industry standards, such as the JEDEC Standards. Then, this chapter addresses the typical reliability issues in power packaging which includes the thermal cycling, power cycling, passivation crack, probing test, drop test, preconditioning and the delamination, and the power packaging mounting. Thermal and power cycling tests are studied to check if the power package can withstand the uniform or gradient TMCL loads. The stress

evolution and the solder paste delamination in the thermal cycling and power cycling are examined. The impact of the power die tilt on the stress of the power package is discussed. The passivation crack on the power die surface is always a challenge in the industry. Therefore, this chapter introduces the fundamental theory of the ratcheting plastic deformation and investigates the root cause of the passivation crack. The design methodologies to avoid the passivation cracks are presented. In wafer probing test, both electrical and mechanical contacts are made between the probe tip and the bond pad. This may damage the structures below the bond pad, such as dielectric layers and active devices. The failure mechanism of the wafer with copper bond pad in the probing test is studied. The numerical design of experimental (DoE) analysis with different thickness of stack materials and probing parameter is conducted for the product optimization. The influence of heat sink mount process on the power package reliability is investigated. Different lead frame design and lead frame material options for a power package are provided for analysis and optimization. The moisture related reliability analysis for power package is studied in ACLV. Finally, the drop test for solder joint reliability is discussed with the impacts of different design variables. This chapter does not include the reliability analysis for power device level, such as the IGBT and MOSFET transistors, the device interconnect failure mechanisms, and relationship with packaging; such information may be found at JEDEC Standard JEP 122F [50].

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Chapter 10
Power Packaging Modeling and Challenges

Modeling and simulation of power electronic packaging design, reliability, and assembly is a multidisciplinary activity that relies on the expertise of the complex processes, almost all the material types, detailed process windows, and are sequence dependent, a very challenging task for both academic people and practicing engineers [1, 2]. Modeling and simulation has been classified in the ITRS Road Map [3] in the past years to be one of the cutting-edge technologies that must be mastered to enable rapid progress in this first industry. The importance of modeling and simulation has been witnessed by the increasing number of design engineers in each corporation from 20% in early 1980s to 80% in today in terms of recruited engineers, as it is essential to design and make the product so as to be first time pass.

The most popular methodology of design, reliability, testing, assembly, and manufacturing is named Design for X (DFX, here X refers to manufacturing, assembly, testing, reliability, maintenance, environment, and even cost), which has been widely adopted by those multinational and small high-tech start-up companies. The design methodology is being adjusted to meet the requirements of a full-life cycle, so-called "concept/cradle-to-grave" product responsibilities, coined by Dr. Walter L. Winterbottom of Ford Science Lab [4]. Today, the modeling methodology has been applied in semiconductor industry.

10.1 Modeling Role in Power Electronic Industry

A power packaging module and related application systems, like any other electronic systems, involve a lot of manufacturing processes from film deposition, etching, chip to wafer and wafer to wafer bonding, dicing/singulation, and extensive reliability testing for extended-life goals of many critical products such as those used for automotive electronics, portable power electronics, high power module, etc. The defects in terms of voids, cracks, delaminations, microstructure

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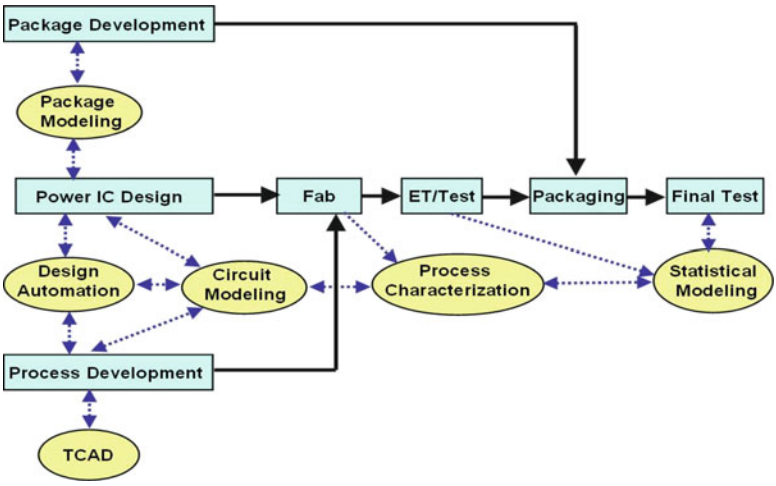


Fig. 10.1 The diagram of the modeling in all areas of power semiconductor

changes can be induced in any step and may interact and grow in subsequent steps, imposing extreme demands on the fundamental understanding of stressing and physics of failures. Currently, the testing programs have been extensive to assure reliability during the product development. Iterative, build-test-fix-later process has long been used in new product development, significant concerns are being addressed as cost-effective and fast time to market needs may not be achievable with such an approach. In the sense of high reliability, system hardware design and manufacturing and testing are costly and time-consuming, and severely limit the number of design choices within the short time frame and no enough time to explore the optimal design. With the current situation of 3–6 months for each generation of IC chips, it is challenging to achieve truly optimal and innovative products with so many constraints in design. Design procedure must be modified and DFX must be used so as to achieve preventive with integrated consideration of manufacturing processes, testing, and operation.

ITRS SiP 2009 white paper [1] for assembly and packaging describes a future vision of chip-package system codesign: (a) one tool for simultaneous design enabled by a multiuser, cross-functional EDA + system analysis + knowledge-based tool. (b) A wizard-like interface, automatically constructs baseline design for each component based on a series of user questions, analysis, and an expert system for technology selection and design rules. These ideas cover stress/mechanical modeling, thermal chip-package system, and electrical chip-package system. This indicates a modeling trend of the industry is toward package system design automation. Figure 10.1 [2] shows the modeling role in all areas of the semiconductor industry from power IC design to final product, in which the yellow color areas stand for the modeling role for each process, these include the design automation for power IC design, power circuit modeling, TCAD for device and process, process modeling for Fab, packaging modeling for power package

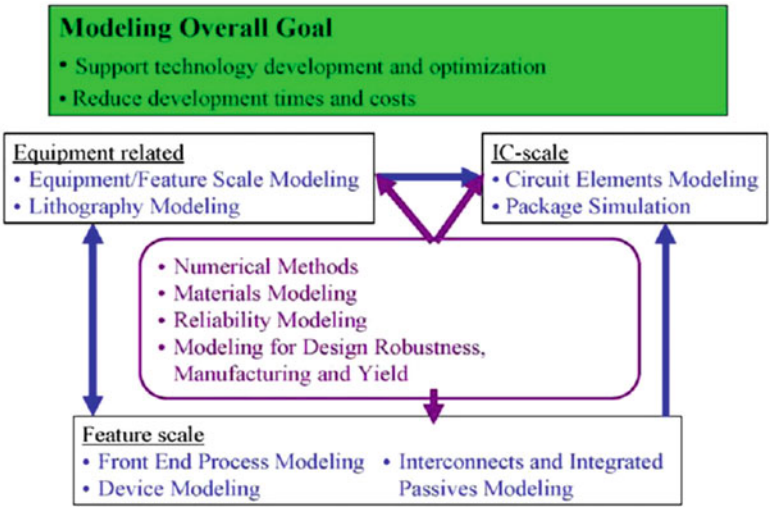


Fig. 10.2 The function of modeling and simulation [3]

development that includes the package design, reliability, test, and assembly process. The statistical modeling also takes care from the electrical test, the manufacture process to the final test.

Suppliers of the modeling and simulation capability are mainly universities and research institutes funded by government and/or industry projects. Modeling and simulation vendors play an important role in the development of those capabilities, and are in most cases the interfaces between R&D and the end customer in industry, customizing the R&D results into commercially supported simulation tools. Simulation efforts in semiconductor industry mainly focus around the adaptation and application of the simulation capabilities to the development and optimization of IC technologies, devices, and packaging.

The development of new modeling capability generally requires long-term research, and increasingly interdisciplinary activities, which can be carried out best in an academic or a laboratory setting. For this reason, a vigorous research effort at universities, research institutes, and industry is a prerequisite for success in the modeling area, together with a close cooperation with critical issues in industry, along the simulation food chain as shown in Fig. 10.2 [3]. Because the necessary basic work generally needs significant development time, it is vital that adequate research funds will be made available in a timely manner in order to address the industry's future critical needs.

Figure 10.2 shows the basic function of the modeling and simulation in semiconductor. It is a general chart, but particularly in power semiconductor industry, the goal is to support the power technology (power IC, device and packaging) development and optimization to reduce the design cycle and cost. The fundamental function of the modeling and simulation includes three parts:

(1) The power IC, packaging and module as well as the board level system; (2) The environmental related modeling that includes power packaging assembly process level; (3) Three-dimensional (3D) feature scale level that includes the front-end process modeling, interconnects/3D/TSV/RDL, and passive modeling. Those functions need the continuous innovation for numerical methods, new material and process method (example is to use molecular dynamics to predict the material behaviors), new reliability modeling methodology development, new modeling methodology for the power packaging assembly, and the modeling for power design robustness.

10.2 Challenges of Modeling Tools and Methodology

10.2.1 Challenges of Modeling Tools

There are various tools for the power semiconductor industry. Most modeling tools for packages are based on finite element analysis (FEA). Typical finite element software packages used today for power electronics are ANSYS® (including Ansoft®), Abaqus®, Cosmos®, and a lot of CAD and optimization software for the packaging level. There are also a lot of software for device level such as Cadence® and Syncronicity. Those modeling tools are the major sources and supports of the modeling and simulation for the power semiconductor industry today. However, as the trends of power packaging toward the next generation with high power density, miniaturization (for low power application), the challenges for the modeling tools and methodology become more and more significant. Below are the challenges listed from the white book of ITRS, 2009 [3].

Front-end process modeling for nanometer structures—Most important and challenging in the area of front-end process modeling is the modeling of ultrashallow junction formation, which starts from very low energy implant and especially focuses on the thermal annealing and diffusion of dopants. Cluster and cocktail implants and plasma doping must be modeled as alternatives to create shallow junctions, as well as the formation of doped epitaxial layers, including their shape and morphology, defect status, and stress. Anisotropy in models and parameters potentially introduced by thin layers must be investigated. In view of the need to increase carrier mobilities in the channel, the modeling of stress and strain and their influence on diffusion and activation has become critical, especially for strained silicon, SiGe, and for SOI structures. Moreover, stress history and nonlinear history during process sequences is important and must be simulated. Model development, calibration, and evaluation as well as process characterization require numerous experimental activities and large progress in the metrology for dopants, defects, and stress, especially regarding 2D- and 3D measurements. To enable efficient and accurate 3D simulation, meshing for moving boundaries needs to be strongly enhanced.

Nanoscale device simulation capability: *Methods, models, and algorithms that contribute to prediction of semiconductor limits*—A fundamental question of the power microelectronics industry continues to be what are the ultimate limits of semiconductor technology and devices. The key requirement to deal with this challenge is predictive simulation of materials, processes, and device behavior including reliability. Material models are needed especially for gate-stacks including high-κ materials, for stress-engineered, SiC and Ge channels, for interconnects including size-dependent resistivity of copper and low-κ dielectrics, and for nonlinear photoresists. Quantum-based and nonequilibrium device level simulations are needed such as atomic dynamic modeling simulation methodology. Simulations must also be applicable beyond standard power semiconductor. Besides accuracy, efficiency and robustness are key issues. Both atomistic and process-induced fluctuations critically affect the manufacturability of the ultimate power devices and must therefore be dealt with in simulation.

Electrical-thermal-mechanical-multiphysics modeling for interconnections and packaging—Performance and reliability of integrated circuits is increasingly affected by interconnects and packaging. Electrical (resistance, inductance, and capacitance [RLC]), thermal, and mechanical properties highly interact with each other and must therefore be simulated together in a multiphysics environment. Reliability issues requiring modeling include electromigration, stress voiding, integrity and adhesion of thin films, surface roughness, silicon die crack, solder joint plastic deformation and crack, package fracture, bond wire lift and fusing, delamination, corrosion, and various failure mechanisms in assembly manufacturing and reliability testing. Through silicon vias and thin stacked die request new or largely extended simulation tools. Size effects (microstructure, surfaces) and variability of thinned wafers are important issues to be simulated. The capability to withstand the heat produced in the power IC/MOSFETs and to transport it off the chip is getting a top-level concern with further increasing densities. New materials such as low-κ, SiC are being introduced to meet the targets of the road map. Thermal modeling of these new materials is also required. Due to their variety and lack of knowledge of their properties, these new materials require large efforts on the development of models. The challenges are being addressed below:

(a) Model thermal-mechanical, thermodynamic, and electrical properties of low κ, high κ, SiC and conductors for efficient on-chip and off-chip SiP and wafer level packages, including power management, and the impact of processing on these properties especially for interfaces and films under 1 μm dimension.
(b) Thermal modeling for 3D ICs and assessment of modeling tools capable of supporting 3D designs. Thermomechanical modeling of Through Silicon Vias (TSV) and thin stacked dies (incl. adhesive/interposers), and their impact on active device properties (stress, expansion, keep out regions, etc.). Size effects (microstructure, surfaces, . . .) and variability of thinned wafers.

(c) Signal integrity modeling and power/heat management for stacked die packaging system.
(d) Model effects which influence reliability of interconnects/packages including 3D integration (e.g., stress voiding, electromigration, fracture, dielectric breakdown, piezoelectric effects).
(e) Physical models to predict adhesion and delamination on interconnect-relevant interfaces (homogeneous and heterogeneous).
(f) Dynamic simulation of mechanical problems of flexible substrates and packages under impact such as drop test, vibration, and transportation.
(g) Models for electron transport in ultrafine pitch package development such as the pitch less 0.3 mm of power IC WL-CSP.
(h) Supporting heterogeneous integration (SoC + SiP) by enhancing CAD-tools to simulate mutual interactions/coupling of building blocks, interconnect, dies on wafer level and in 3D and package

Modeling of chemical, thermomechanical, and electrical properties of new materials—Increasingly new materials need to be introduced in technology development due to physical limits that otherwise would prevent further scaling. This introduction is required especially for gate stacks, interconnect structures, and photoresists, and furthermore for Emerging Research Power Devices (ERPD). In consequence, equipment, process, device, and circuit models must be extended to include these new materials. Especially, computational material science tools need to be developed and applied to contribute to the assessment and selection of new materials in order to reduce the experimental effort, and to contribute to the databases required for semiempirical package design.

10.2.2 Numerical Methods of Tools

Numerical methods and algorithms need improvement to support the growing complexity of physical phenomena in power device and packaging [3]. For example, more accurate solutions of the Boltzmann transport equation in device or wafer level simulation are required. To include stress and strain and several defect species and complexes in the simulation of dopant diffusion and activation requires dealing with an increasing number of coupled partial differential equations over the device grid. Moreover, physical processes with different intrinsic time- and/or length scales critically influence each other, and have to be simulated adequately in a coupled manner—point-defect diffusion occurs on a several orders of magnitude faster time scale than macroscopic process time. Recently, an increasing demand has been put on the simulation of electromagnetic effects in electrical modeling such as the skin effect in conductors in a power device and package, the proximity effect and the substrate coupling. These are examples of how increased requirements on predictability and accuracy of models induce more complex models in device and wafer level power electronics and, in turn, drive the numerical

methods and solver technology from linear toward nonlinear and parallel algorithm. The same for numerical methods of 3D power electronic packaging modeling, including power package component level, board level and strip level in assembly process, nonlinear geometry and material behavior, multiscale from atomic scale, micro- to macrolevel and multiphysics that includes the coupling of thermal, moisture, mechanical, and electrical issues. This requires the high-efficiency numerical algorithm and the robust computational capability of the hardware to solve such complex engineering problems. Typical example for larger deformation with both geometry and material nonlinear is the strip warpage after molding process, strip modeling is a very typical multiscale problem, its model is very big. Typical multiphysics problem is the electromigration for a power wafer level chip scale package which couples the electrical, thermal and mechanical fields, and needs to develop fast user subroutine to support the fast simulations. For such coupling problem, normally it is very challenging to develop the direct coupling multiphysics fields with numerical method with multiple independent variables; however, the indirect coupling strategy is a possible method, like to couple the electrical and thermal simulation first, then to run the mechanical simulation based on the result of electrical and thermal coupling simulation.

Meshing for the efficient and accurate solution of differential equations has become a major issue because power IC device/package architectures are now essentially 3D; an example is the 3D interconnects and TSVs. The increase of the numbers of steps to be included in the process simulation, and especially the frequent use of automated simulation splits to investigate process options and the sensitivity of electrical power device/packaging data on process details requires completely automated mesh generation. This automated mesh generation must be reliable for all kinds of power device/packaging geometries and distributions of volume variables, with a failure rate at least two orders of magnitude below current tools. In addition, meshing tools must be capable of resolving all critical features of the power device and packaging, like small geometry features or steep dopant gradients, without unacceptable drawbacks in terms of mesh nodes, computation time needed for mesh generation, or adaptation in the refinement as well as the coarsening direction. A major concern is to combine the very different scale in the simulation problem: the on-chip features are on the nanometer to micron scale whereas the equipment scale is in the centimeter range. Automatic mesh generation and adaptation is especially important to resolve critical features of multiscale power packaging geometry and the wafers to be processed, while avoiding a too high number of mesh nodes. This problem gets severe when coupling multiphysics and multiscale simulation. Several current tools for computational fluid dynamics (CFD) calculations suffer from a complicated procedure to define the geometry to be simulated and to provide necessary information for mesh generation in 3D power device process, as well as in thermal simulation for the wafer level power system in packaging.

Modeling research and development are needed for the robust solution techniques, which means that in general an optimization sequence avoids local minima where the flow gets trapped. Techniques need to be developed for how to escape from these traps without fully destroying the result achieved so far. These strategies should then be implemented in the software tools in order to facilitate their respective ease of use. Research is also needed on developing robust and efficient parameter extraction algorithm. Without a well-calibrated parameter set, simulators lose their practical values. However, calibration work is frequently a time-consuming and delicate issue, due to a large number of parameters and the so-called "local minimum problem." Some algorithms, such as genetic algorithm (GA), may be good candidates to solve this problem, but only if remarkable improvements in its efficiency are realized. Furthermore, it is not always guaranteed to obtain a set of complete measurements for calibration. A novel methodology for efficiently calculating stochastic variations in models is needed to meet the strong requirements of evaluating and/or simulating deviations of power device performances due to uncontrollable fluctuation or variations under 3D/TSV packaging process. Traditional computing approaches such as the Monte-Carlo method require a prohibitively large number of trials, as the number of fluctuating variables increases. It will be necessary to introduce new algorithms for this purpose, such as numerical methods to solve stochastic partial-differential-equations.

It is important to choose and combine tools from different sources in order to best meet their requirements—e.g., tools from vendor A for some parts of process simulation, tools from vendor B for the rest of process simulation and for power device simulation, tools from vendor C for power packaging simulation, vender D for computational material. This needs at least open and documented interfaces between the various tools, or in the ideal case even interfaces which are standardized for a certain kind of data transfer, e.g., from 3D dopant to 3D device simulation, from 3D interconnect/TSV level to the package level for the multiscale and multiphysics simulation. Whereas such open or even standardized interfaces would be very beneficial for the users to realize the codesign automation, they are unfortunately not necessarily in the interest of the software suppliers.

10.2.3 The Next Step of Modeling Tool

Modeling and Simulation software tools span the entire power semiconductor world. These tools are being used daily with increasing efficiency. Increase cross-disciplinary efforts will be vital in order to leverage on the expertise of fields that were originally not related and are now needed to work together to cope with the challenges outlined in this document. Adequate resources for research must be mobilized and directed to efficiently work toward the technical solutions for the challenges and requirements defined. Collaborations between industry and research institutes both at universities and at independent laboratories must continue to be enhanced and extended to guide

the activities toward the industrial requirements detailed in this road map. The collaboration must also include the promotion and enabling of short, middle to long term research actions needed in Modeling and Simulation, which is generally precompetitive and therefore an excellent field for broad cooperation.

Software research companies, institutes, and universities must be strongly encouraged to standardize and/or open up some of their universally used modeling and simulation modules to avoid multiple work in the precompetitive area. In the ideal case, there should be supplier-independent standard interfaces that allow for the combination of tools from different sources, or at least standardized model-interfaces that allow R&D institutes to focus on the development of added-value features, like new models, while being compatible with supported software environments from the beginning and in this way reduce time-to-application. Existing proprietary model interfaces of some commercial tools have already proven to strongly promote cooperation with research institutes and universities and, in turn, strongly accelerated model development and its use in industry. Standardization of interfaces would largely enhance that benefit. The semiconductor industry can have a central role in this respect by requesting such standardization when deciding about their software investments.

The most important general technical development needed in the field of Modeling and Simulation is that of integration—not only between different processes, process to device, device to package, but also between different levels of description. In some cases the Modeling and Simulation software tools are linked together (such as traditional process and device simulators, CAD design tools, power packaging modeling), while in many other areas the software tools are still separated. If one examines the cycle time for development of a new technology, much of that time and cost is not in the individual module development, but at the integration level. There is a continued strong need for Modeling and Simulation tools to be better linked for determining unforeseen interactions of one step on the next. The efforts are needed for the following areas:

1. The interfacing of materials structural simulation tools and methodologies with software that predicts electronic properties. An example where these tools would be useful is in the development of next generation power device with TSV/3D integration.
2. The integration of chip performance tools and methodologies with multiphysics and multiscale for power package thermal, mechanical, and electrical simulation tools to create a codesign environment. Structured data sets that contain needed physical constants that facilitate parameter passing between tools. The integration of power device simulators with robust methods for creating compact models and device files for design.
3. A hierarchy of closely coupled simulation tools and methodologies must be developed. This would allow the industry to select the most appropriate level of description for their simulation problems in question, along with appropriate and efficient data transfer when the application requires investigations at different levels (for example, from power device level model to the packaging level).

10.3 Modeling Requirements in Semiconductor

Based on the white book of IRTS of Modeling and simulation [3], below is a list of the modeling requirements in power semiconductor.

10.3.1 Front-End Process Modeling

Front-end process modeling includes the simulation of the physical effects of manufacturing steps used to build power transistors up to metallization. These areas are important for understanding and optimizing transistor fabrication, pushing the limits of scaling traditional planar devices, and evaluating process issues in alternative device architectures. The needs for modeling are driven by the reduction of feature size in scaling transistors and by the increasing number of new materials being considered to overcome scaling roadblocks. These not only cause higher demands on model accuracy but also require models for effects considered as second order effects in the previous node, or models of new materials, material properties, and doping techniques as well as the introduction of new simulation flows.

With the reducing thermal budget, accurate lateral doping and damage distributions need to be modeled. Monte Carlo implant models are definitely required for application that cannot be adequately addressed by analytic models, for example, doping of sidewalls of narrows trenches and TSV, channel doping steps. Analytic models will need to be refined with respect to lateral dopant and damage distributions. Modeling needs to be extended to include damage kinetics during the ion implant process step especially for "cocktail ion implant" and subsequent annealing process in silicon and silicon related materials. Advanced process models will be needed for the modeling of metal-stable dopant activation (above solid solubility). These should include activation kinetics considering the reduced front-end thermal budget and deactivation kinetics during subsequent backend processing. Models for surface and interface diffusion will be needed. These include interactions with SiO_2 and new gate dielectric materials. Process models for diffusion/activation in alternative materials (such as SiGe, SiGe:C, GeSi, or Ge) need also to be improved, as well as those for very thin body (such as SOI) needed with or without any intrinsic mechanical stresses where interaction with interfaces is of first order.

As engineering of mechanical stress effects for device mobility improvement is becoming increasingly important, models for the effect of stress on reliability, dislocation generation, and dopant diffusion need to be developed. Intrinsic stress resulting from all process steps including those coming from material texture modification and including stress generated by the presence of impurities, clusters, and extended defects must be considered over the full range of temperatures used in processing and must be transferred to device simulation tools. Thin film growth

needs to be better modeled, including the reliability impact of stress in corners and small 3D structures, as well as the defect generation in such a structure.

Feature-scale models for deposition and etching, including chemical mechanical polishing (CMP), need to be linked to equipment simulation. This linkage will allow determination of the influence of equipment settings on feature topography as well as on inhomogeneities on the wafer and from wafer to wafer. This should also result in more physical feature scale models in particular for the last introduced deposition techniques such as chemical vapor deposition (MOCVD) and for epitaxial growth of semiconductors and dielectrics. Modeling of these processes will become more critical as the industry moves beyond planar MOS to more complex device structures and 3D integration schemes. For each of these front-end modeling areas, approaches need to be developed to enable estimation of the performance impact of variation in critical front-end process steps. These include random effects such as random dopant fluctuation and systematic effects such as within-wafer etch variation. These effects, tightly linked to modeling of equipment such as lithography variations due to proximity effects and line edge roughness, are required for a better design for manufacture (DFM) strategy.

10.3.2 Power Device Modeling

Device modeling refers in general to a suite of models and methods describing carrier transport in materials. Models range from the simple drift diffusion, which solves Poisson and continuity equations, to more complex and high current density as the energy balance, which solve some higher moment simplification of the Boltzmann equation. In addition, the complex physics of today's devices mandates at times the usage of Monte Carlo codes, which stochastically solve the Boltzmann equation, and the usage of Schrödinger solvers that account for quantum effects. The choice of the appropriate model depends on the problem and the level of details required and it is therefore left to the user. Despite the significant advances of recent years in both numerical methods and physics, continuing development is required to meet the increasingly challenging industry needs for device exploration and optimization. Device modeling is used for scaling studies and technology optimization; therefore, the ability to correctly represent today's performance and predict tomorrow's limitations is paramount.

Stress and strain—Different materials in source-drain regions and layer stacks as well as the thermal budget of processing result in stress and strain fields that increasingly determine the device characteristics. In order to predict currents correctly for all possible channel orientations a full-tensorial description of arbitrary stress fields has to be included. Comprehensive models must include the effect on band-structure (band-edges, effective density-of-states and masses). The effects on mobility are of paramount importance, especially the nonlinearities for GPa stress fields. They include anisotropic piezo-resistivity, which is caused mostly by

the effective masses but also by momentum relaxation times, as well as stress dependence of saturation velocity.

Contact resistance—With shrinking device dimensions, the contact resistance contribution to the total device resistance (channel, S/D, contact) will increase and play a more important role in predictive simulation of the current-voltage characteristics and transconductance. A correct modeling of contact and sheet resistance (high doping activation and mobility) is a prerequisite for a correct device description and a possibility for contact engineering (e.g., by Fermi-level depinning reducing Schottky barrier height). The contact resistance contribution to the $R_{ds(on)}$ is particular important for discrete power device.

3D modeling—The multiphysics coupling at various power device requires a full 3D device modeling taking into account realistic 3D geometries and doping distributions. Effects such as gate line edge roughness or width dependence greatly impact devices output characteristics and they need to be taken into account during device optimization studies. This implies that 3D simulations are no longer reserved for occasional, limited use but are a real need for everyday tasks. Therefore, device editors productively coupled to process emulators and simulators, meshing algorithms and solvers have to be enhanced to the point that 3D tools have complexity and computational requirements similar to 2D. In addition, as the shrinking device size, the electromigration or metal migration will become significant, this requires the prediction of the 3D voids/hillock as well as their location.

Dopant, geometric and structural fluctuations—Ever shrinking geometries have created a singular problem unlike any other: Because of the small volumes involved modest fluctuations of implanted dopants will give rise to considerable differences in doping concentration, which in turn will have a tremendous impact on devices characteristics. Similar effects arise from fluctuations in trap concentrations, poly grains size, as well as of gate dielectric and UTB (ultrathin body)-SOI silicon layer thickness. Such fluctuations will broaden the device parameters distribution and will therefore need to be taken into account for any optimization or manufacturability study. In this regime, each single device type will have to be represented by an entire distribution of devices with random doping concentration (producible, for example, via Monte Carlo methods) and preferably in 3D, which reemphasize the need of fast 3D simulators.

LDMOS, *VDMOS*—Development of LDMOS, VDMOS and bipolar specific models lag behind that of models aimed at conventional CMOS scaling despite being as much or possibly more necessary. Consequently, support of power device LDMOS, RF, analog and mixed-signal CMOS, BiCMOS, and bipolar circuit design requires enhancements, especially in the numerical treatment of small signal analysis and large signal behavior (transient). Efficient tools are needed to analyze device performance, to characterize nonquasistatic effects, to minimize the requirement for time- and cost-intensive power device and RF measurements and to provide predictive data in the downscaled regime. Device simulation integrated with power device and RF circuit or mixed-mode simulation could ease optimization but will require

efficient algorithms. When coupling circuit and device simulations, calculations for different devices will need to be run in parallel, thus requiring the necessary hardware and software support. The employed models will have to take into account all models needed for DC, like surface-quantization, direct gate tunneling, impact ionization, stress effects, etc. Comprehensive modeling must cover all the important internal noise sources from the sub-kHz up to the high frequency switch function (above MHz) for power device. Finally, self-heating of devices and circuits and frequency dependency of physical parameters must be taken into account.

10.3.3 Modeling of Interconnects Passives

Interconnects/3D/TSV/RDL continue to play an important role as a limiting factor for staying in pace with Moore's law to double the transistor and interconnect densities every 2 years [3]. This refers both to their electrical performance and to their reliability, and in turn requires coupled electrical, mechanical, and thermal simulation. The need for simulation in 3D interconnects and critical dimensions also increases. Concerning reliability due to the size shrinkage of interconnects, electromigration, stress voiding, and extrusion/hillock are most important aspects, especially for high current density in power device. Both electrical performance and reliability are critically influenced by process conditions and material properties including the microstructure of copper and dielectric materials. Performance and reliability critically depend on design, but with further shrinking distances and cross sections the deviations from ideal 3D/TSV/RDL structures resulting from real fabrication processes is another important factor. Similar to front-end technology, both the modeling of the fabrication and then the modeling of the performance and reliability of interconnects is required. Passives in power electronics include resistor, inductor and capacitor. The active power devices combine with the passives to form various converter, inverter and control switches with half and full bridge. Recent years, there are wafer level passives play very important roles for the wafer level power packaging and RF application integrated with 3D interconnects/TSV and RDL, which has made it possible for the very high operation frequency. The ability to predict the electrical and parasitic properties of complex interconnect structures continues to be a challenge. Software tools and methodologies that link process results to results at the IC level, that identify reliability issues or design deficiencies, that give the designer capabilities to explore alternative interconnects easily are needed.

Understanding of the coupled thermal and mechanical performance properties of thin multilayer films becomes critical in the power semiconductor device. Structural and compositional properties of thin films need to be obtained and related to reliability effects not only for thin multilayer films but also for thin multilayer films patterned for critical dimensions. The mechanical properties of these thin films, such as fatigue, fracture, and stress voiding, also affect reliability performance. Thermal cycling (TMCL) can trigger fractures that may not be foreseen, an

example is the ratcheting deformation in TMCL that results in the cracks on passivation film of the power device.

An important reliability risk factor is the thermal intrinsic residual stresses in multilayer thin films. Each thermal process causes microstructural transformation of metal films which in turn induces residual stresses. Modeling of mechanisms of grain growth and transformation will improve understanding of entire stress budget in thin films which influences nucleation and propagation of cracks. Simulation tools are needed to study these effects more effectively than by experiment alone. Delamination occurrences have drastically increased following low-κ integration. Brittle fractures, located at interfaces, cannot be address anymore with commonly used stress based analyses. Continuum mechanic laws do not remain valid and tools dedicated to fracture mechanics, such as energy based ones, must be developed. On the other hand, on top of numerical issues, novel failure analysis techniques are enabled for correlation purpose. This is particularly true for fracture mechanics, for which the understanding remains one of the bottleneck. In that frame, 3D views of the crack features, in situ non destructive observation and tracking of the delamination propagation will bring crucial insights for failure criteria development. As for the need to define worst cases of test structures and ensure that experimental reliability results indeed correspond to real life conditions of devices, the electromigration related issues must be simulated. Even in thermomechanical induced stress, critical dimension reduction also tends to invalidate the commonly used approaches in material models: For example, microstructural effects in copper lines, or pore effects in dielectrics will became a dominant factor. Multiscale and multiphysics simulation must be precisely carried out to bridge these scales. For the physically and microstructural small cracks (for example, nanoscale cracks), the classical continuum mechanics concept may not be valid and micromechanics treatment of the material with damage mechanics at the microscopic material scales would be more appropriate.

10.3.4 Circuits Modeling

An important task for circuit modeling is to achieve concurrent device/circuit development, dealing with the increasing amount and intensity of interactions between e.g., devices, layout, density, parasitics, and so on. Accurate modeling of circuit behavior, including parasitics, is crucial for first-time-right designs. Process and device simulations can support the extraction of early information for new technologies. Models that relate material properties to electron transport strongly enhance the predictability of these models for future technologies. The models should take into account statistics and variations of the processing, including statistical correlations for feasibility of manufacturability. Preferably, these (statistical) models should be available long before process qualification. This enables chip design before technology release, enabling a fast product ramp-up once the technology is qualified.

Circuit models are key to chip design productivity. Model accuracy and CPU efficiency are two opposing requirements leading to a hierarchy of models. The most

accurate models are used to simulate small circuits. Less accurate models are derived to simulate larger circuits, and so forth. Similarly, this dichotomy implies a hierarchy of models at several structural levels—device level, cell level, and block level, although it may also be possible to simulate a whole chip with accurate models without hierarchical simulations. Historically, analog simulation needs have driven the development of circuit element models. Both analog and power IC designers then use these models. The increasing number of (analog, digital, and power IC) devices per chip necessitates faster models and improved convergence in the simulation tools. Device models will include many more detailed effects. Parasitic effects, such as resistance, inductance, and capacitance, as well as quantum effects, leakage, noise, distortion and nonquasistatic effects have become of more importance. Robust and accurate parameter of resistance, inductance, and capacitance (RLC) extraction algorithms are essential for each electrical model. The importance of interconnect modeling increases with the stronger contribution to circuit delays and cross talk. The complexity and the size of the interconnect network poses serious challenges. Different applications need models for different effects, like cross talk, matching, inductive coupling (also in 3D), skin effects, and size effects. Temperature effects will get more important for SOI-based and thin-film devices. Hence, self-heating and mutual heating and cooling effects should be modeled in more detail over the full chip. ESD is becoming one of the most serious reliability problems in future processes. Predictive circuit-level simulation, based on device level compact models, is essential to guarantee safe chip-design. In addition, the prediction of electromigration from interconnect layout needs improvements to avoid void to induce the line breaking and hillock to short the lines.

10.3.5 Power Package Level Simulation

Power package codesign is a key crosscut issue with system-level considerations becoming increasingly important. In the past a package designer might have been presented with the die footprint including the placement of the die I/O pads as well as the placement of the I/O connections to the printed circuit board (PCB). With increasing pin counts and overall size constraints, this practice often results in packages that are unreasonably expensive or that cannot be manufactured. Beyond being routable and manufacturable, a power package must meet demanding requirements with respect to signal integrity, power, temperature, and mechanical integrity. The required integrated electrical, thermal, and mechanical simulations must be performed with consideration of the die and the system, and this is possible only with communication enabled by codesign tools. A properly designed codesign tool will interact directly with both the package and die databases and have the capability of communicating results between the two.

The common electrical package models today are lumped discrete models such as SPICE. There will continue to be demand for such models due to their simplicity

and speed of simulation. Modeling of power and ground structures in the package is extremely important. Current bottlenecks, noise, and simultaneous switching issues are critically important with repercussions for thermal analysis. It is difficult to ascertain if enough decoupling capacitors have been placed in the correct places to guarantee performance, or perhaps too many have been added, thereby negatively impacting cost and package size.

Generating electrical models for simulation is creating new challenges with regard to numerical methods. Package geometries are such that there is no substitute for fully 3D field-solver extraction. In a flip-chip package there are some-times so many layers and power and ground structures that the extraction of a single signal net may be very costly. In a multichip module (MCM) there may be longer traces that couple many nets together, requiring a very large minimal set for extraction. In either case, decomposing the problem into smaller pieces introduces significant fictitious fringing spoiling the power/ground extraction. The development of scalable field-solver engines that can manage full-package extraction is essential; scalability will likely be achieved through implementation on a parallel cluster. At the same time, efficiencies with regard to time and memory consumption need to be further improved.

However, besides the electrical modeling, inherent and thermally induced mechanical stresses throughout the layer stack must be identified and modeled. The low-κ dielectrics often have reduced mechanical integrity, while at the same time thermal stresses are more severe. The stresses are especially enhanced with nonuniform heating induced by the die, by current bottlenecks in the ground and power planes, and with reduced thermal conductivity.

In addition to specific failure mechanisms and front-end back interactions induced by new material integrations, the increasing complexity of power packaging options drives the need for improved modeling to reduce cost and development time. Since process windows and main influent parameters are definitely dependent on the packaging options, generic modeling cannot be applied anymore and actual product configurations must be considered. Furthermore, the whole process flow, including front-end, assembly, and packaging steps, must be simulated to examine residual stresses, critical loading conditions, and thus optimize both package and interconnect features. This would finally lower the cycle time to introduce new power products while ensuring device integrity.

10.4 Modeling Methodologies Needed in Power Packaging

The basic modeling methodologies needed in power packaging include packaging electrical modeling and thermal-mechanical modeling. Thermal mechanical modeling includes package thermal design, packaging assembly, and package reliability.

10.4.1 The Methodologies of Power Packaging Electrical Modeling

Power package electrical modeling includes building the electrical model library; modeling for package resistance, inductance, and capacitance (RLC); 3D extraction for resistance, inductance, and capacitance; Power package electrical-thermal coupling for current fuse capability; Power unclamped inductive load or switch (UIL/UIS) test simulation and the electromigration modeling that is multiphysics with coupled electrical, thermal, and the structural fields.

Typically electrical modeling methodologies list (see Chap. 12 for more details)
Method for power package electrical resistance and inductance modeling and extraction
Method for power package capacitance modeling and extraction
Method for converting the RLC parameters to spectre netlist for spice modeling
Method for power package parasitic RLC extraction and efficiency calculation
Method for power package current fuse capability simulation
Method for power package UIL/UIS test simulation
Method for power package electromigration simulation

10.4.2 The Methodologies of Power Packaging Thermal-Mechanical Modeling

Thermal-mechanical modeling methodologies for power are very important in power electronics. In general, the thermal-mechanical modeling includes the power package thermal design, power package assembly, and power package reliability analysis.

The typical thermal-mechanical modeling methodologies for power package include the following:

1. Methodologies for thermal design

   Method for thermal simulation and thermal resistance extraction
   Method for transient thermal simulation
   Method for multiple die thermal simulation and management.
   Method for thermal simulation for 3D/TSV for power packaging
   Method for thermal simulation for stack die and embedded power packaging

2. Methodologies for power package assembly process

   Method for power wafer deposition and warpage simulation
   Method for power wafer back grind and metallization
   Method for power wafer sorting/probing process
   Method for power die pickup process simulation

Method for die attaching/bonding process
Method for wire bonding (including copper wire bonding) process
Method for copper stud bumping simulation
Method for molding injection/curing process
Method for mold ejecting process
Method for power packaging clamping process
Method for product singulation (trim/form/punch) process
Method for power package heat sink mount process simulation
Method for assembly 3D/TSV power packaging
Method for assembly stacked and embedded die power packaging
Method for the design for the assembly by probability modeling

3. Methodologies for power package reliability analysis

Method for thermal cycling simulation, solder joint reliability, and life prediction
Method for power cycling simulation, solder joint reliability, and life prediction
Method for solder reflow process and wave soldering simulation
Method for power packaging drop test simulation
Method for power package bending simulation
Method for power package passivation crack simulation
Method for power package die crack simulation
Method for power package moisture diffusion simulation
Method for power package hygroscopic stress simulation
Method for vapor pressure simulation
Method for delamination simulation
Method for precondition simulation
Method for ACLV stress simulation
Method for time to failure due to electromigration
Method for the 3D/TSV/Stack/embedded die reliability simulation
Method for the design for the reliability and optimization

As the development of next generation power packaging with 3D/TSV/stack/embedded die technology, the need for the new modeling methodologies is definitely increasing. There may need to develop new and advanced modeling technologies to meet these requirements for the new power products.

10.5 Advanced Modeling Techniques

One of the major advanced modeling techniques for power packaging is the finite element method. This session will introduce the basic finite element method and its advanced modeling skills [4, 5].

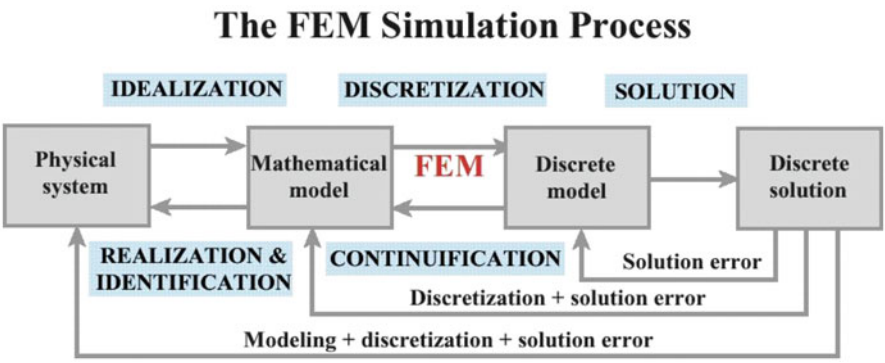


Fig. 10.3 The finite element simulation process

10.5.1 Finite Element Method

The finite element method is a numerical analysis technique for obtaining approximate solutions to a wide variety of engineering problems. The solution of a continuum problem by the finite element method always follows an orderly step-by-step process.

1. Discretize the continuum. The first step is to divide the continuum or solution region into elements
2. Select interpolation function. The next step is to assign nodes to each element and then choose the interpolation function to represent the variation of the field variable over the element.
3. Find the element properties. Once the finite element model has been established (that is, once the elements and their interpolation functions have been selected), we are ready to determine by the matrix equations expressing the properties of the individual elements
4. Assemble the element properties to obtain the system equations. To find the properties of the overall system modeled by the network of elements, we must assemble all the element properties
5. Impose the boundary conditions. Before the system equations are ready for solution they must be modified to account for the boundary conditions of the problem
6. Solve the system equations. The assembly process gives a set of simultaneous equations that we solve to obtain the unknown nodal values of the problem
7. Make additional computational if desired. Many times we use the solution of the system equations of calculate other important parameters

The finite element simulation process can be summarized as in Fig. 10.3.

10.5.1.1 Basic Finite Element Equations

We begin with the virtual work principle:

$$\int_V \boldsymbol{\sigma} : \delta \boldsymbol{D} \, \mathrm{d}V = \int_s \boldsymbol{t}^{\mathrm{T}} \cdot \delta \boldsymbol{v} \, \mathrm{d}S + \int_V \mathbf{f}^{\mathrm{T}} \cdot \delta \boldsymbol{v} \, \mathrm{d}V \tag{10.1}$$

The left-hand side of this equation (the internal virtual work rate term) is replaced with the integral over the reference volume of the virtual work rate per reference volume defined by any conjugate pairing of stress and strain:

$$\int_{V^0} \boldsymbol{\tau}^{\mathrm{c}} : \delta \boldsymbol{\varepsilon} \, \mathrm{d}V^0 = \int_s \boldsymbol{t}^{\mathrm{T}} \cdot \delta \boldsymbol{v} \, \mathrm{d}S + \int_V \mathbf{f}^{\mathrm{T}} \cdot \delta \boldsymbol{v} \, \mathrm{d}V \tag{10.2}$$

where $\boldsymbol{\tau}^{\mathrm{c}}$ and $\boldsymbol{\varepsilon}$ are any conjugate pairing of material stress and strain measures. The particular choice of $\boldsymbol{\varepsilon}$ depends on the individual element

The finite element interpolator can be written in general as

$$\boldsymbol{u} = \boldsymbol{N}_{\mathrm{N}} u^{\mathrm{N}} \tag{10.3}$$

where $\boldsymbol{N}_{\mathrm{N}}$ are interpolation functions that depend on some material coordinate system, u^{N} are nodal variables, and the summation convention is adopted for the uppercase subscripts and superscripts that indicate nodal variables.

The virtual field, $\delta \boldsymbol{v}$, must be compatible with all kinematic constraints. Introducing the above interpolation constrains the displacement to have a certain spatial variation, so $\delta \boldsymbol{v}$ must also have the same spatial form:

$$\delta \boldsymbol{v} = \boldsymbol{N}_{\mathrm{N}} \delta \boldsymbol{v}^{\mathrm{N}} \tag{10.4}$$

The continuum variational statement (10.2) is, thus, approximated by a variation over the finite set $\delta \boldsymbol{v}$.

Now $\delta \boldsymbol{\varepsilon}$ is the virtual rate of material strain associated with $\delta \boldsymbol{v}$, and because it is a rate form, it must be linear in $\delta \boldsymbol{v}$. Hence, the interpolation assumption gives

$$\delta \boldsymbol{\varepsilon} = \boldsymbol{\beta}_{\mathrm{N}} \delta \boldsymbol{v}^{\mathrm{N}} \tag{10.5}$$

where $\boldsymbol{\beta}_{\mathrm{N}}$ is a matrix that depends, in general, on the current position, $\boldsymbol{x}$, of the material point being considered. The matrix $\boldsymbol{\beta}_{\mathrm{N}}$ that defines the strain variation from the variations of the kinematic variables is derivable immediately from the interpolation functions once the particular strain measure to be used is defined.

Without loss of generality, we can write $\boldsymbol{\beta}_{\mathrm{N}} = \boldsymbol{\beta}_{\mathrm{N}}(\boldsymbol{x}, \boldsymbol{N}_{\mathrm{N}})$, and, with this notation—the equilibrium equation is approximated as

$$\delta v^{\mathrm{N}} \int_{V^0} \boldsymbol{\beta}_{\mathrm{N}} : \boldsymbol{\tau}^{\mathrm{c}} \, \mathrm{d}V^0 = \delta v^{\mathrm{N}} \left[\int_s \boldsymbol{N}_{\mathrm{N}}^{\mathrm{T}} \cdot \boldsymbol{t} \, \mathrm{d}S + \int_V \boldsymbol{N}_{\mathrm{N}}^{\mathrm{T}} \cdot \mathbf{f} \, \mathrm{d}V \right] \tag{10.6}$$

since the δv^{N} are independent variables, we can choose each one to be nonzero and all others zero in turn, to arrive at a system of nonlinear equilibrium equations:

$$\int_{V^0} \boldsymbol{\beta}_{\mathrm{N}} : \boldsymbol{\tau}^{\mathrm{c}} \, \mathrm{d}V^0 = \int_s \boldsymbol{N}_{\mathrm{N}}^{\mathrm{T}} \cdot \boldsymbol{t} \, \mathrm{d}S + \int_V \boldsymbol{N}_{\mathrm{N}}^{\mathrm{T}} \cdot \mathbf{f} \, \mathrm{d}V \tag{10.7}$$

this system of equations forms the basis for the (standard) assumed displacement finite element analysis procedure and is of the form

$$F^{\mathrm{N}}(u^{\mathrm{M}}) = 0 \tag{10.8}$$

as discussed above. The above equations are valid for static and dynamic analysis if the body force is assumed to contain the inertia contribution. In dynamic analysis, however, the inertia contribution is more commonly considered separately, leading to the equations

$$M^{\mathrm{NM}} \ddot{u}^{\mathrm{M}} + F^{\mathrm{N}}(u^{\mathrm{M}}) = 0 \tag{10.9}$$

For the Newton algorithm (or for the linear perturbation procedure) we need the Jacobian of the finite element equilibrium equations. To develop the Jacobian, we begin by taking the variation of (10.1), giving

$$\begin{aligned} &\int_{V^0} (\mathrm{d}\boldsymbol{\tau}^{\mathrm{c}} : \delta\boldsymbol{\varepsilon} + \boldsymbol{\tau}^{\mathrm{c}} : \mathrm{d}\delta\boldsymbol{\varepsilon}) \, \mathrm{d}V^0 - \int_s \mathrm{d}\boldsymbol{t}^{\mathrm{T}} \cdot \delta\boldsymbol{v} \, \mathrm{d}S - \int_s \boldsymbol{t}^{\mathrm{T}} \cdot \delta\boldsymbol{v} \, \mathrm{d}A_{\mathrm{r}} \frac{1}{A_{\mathrm{r}}} \mathrm{d}S \\ &\quad - \int_V \mathrm{d}\mathbf{f}^{\mathrm{T}} \cdot \delta\boldsymbol{v} \, \mathrm{d}V - \int_V \mathbf{f}^{\mathrm{T}} \cdot \delta\boldsymbol{v} J \frac{1}{J} \mathrm{d}V = 0 \end{aligned} \tag{10.10}$$

where d( ) represents the linear variation of the quantity ( ) with respect to the basic variables (the degrees of freedom of the finite element model). In the above expression $J = |\mathrm{d}V/\mathrm{d}V^0|$ is the volume change between the reference and the current volume occupied by a piece of the structure and, likewise, $A_{\mathrm{r}} = |\mathrm{d}S/\mathrm{d}S^0|$ is the surface area ratio between the reference and the current configuration. The Jacobian matrix is obtained by restricting the above variation, allowing variations in the nodal variables, u^{N}, only. Let such a restricted variation be indicated by $\partial_{\mathrm{N}} = \partial/\partial u^{\mathrm{N}}$. Examining (10.3) term by term with this in mind, we proceed as follows. The first term contains $\mathrm{d}\boldsymbol{\tau}^{\mathrm{c}}$. We now assume that the constitutive theory allows us to write

$$\mathrm{d}\boldsymbol{\tau}^{\mathrm{c}} = \boldsymbol{H} : \mathrm{d}\boldsymbol{\varepsilon} + \boldsymbol{g} \tag{10.11}$$

where $\boldsymbol{H}$ and $\boldsymbol{g}$ are defined in terms of the current state, direction of straining, etc., and on the kinematic assumptions used to form the generalized strains. From the choice of generalized strain measure and interpolation function,

$$\partial_{\mathrm{N}} \boldsymbol{\varepsilon} = \frac{\partial \boldsymbol{\varepsilon}}{\partial u^{\mathrm{N}}} = \boldsymbol{\beta}_{\mathrm{N}} \tag{10.12}$$

from the above constitutive assumption,

$$\partial_{\mathrm{N}}\boldsymbol{\tau}^{\mathrm{c}} = \boldsymbol{H} : \boldsymbol{\beta}_{\mathrm{N}} \tag{10.13}$$

now, since $\delta\boldsymbol{\varepsilon}$ is the first variation of $\boldsymbol{\varepsilon}$ with respect to nodal variables,

$$\delta\boldsymbol{\varepsilon} = \partial_{\mathrm{M}}\boldsymbol{\varepsilon}\delta u^{\mathrm{M}} = \boldsymbol{\beta}_{\mathrm{M}}\delta u^{\mathrm{M}} \tag{10.14}$$

thus, the first term in (10.10) of the Jacobian matrix can be written as

$$\int_{V^0} \boldsymbol{\beta}_{\mathrm{M}} : \boldsymbol{H} : \boldsymbol{\beta}_{\mathrm{N}}\, \mathrm{d}V^0 \tag{10.15}$$

which is the usual "small-displacement stiffness matrix," except that, since the strain measure $\boldsymbol{\varepsilon}$ will is always nonlinear in displacement, the $\boldsymbol{\beta}_{\mathrm{N}}$ in this term is a function of displacement.

The second term in (10.10) is

$$\int_{V^0} \boldsymbol{\tau}^{\mathrm{c}} : \mathrm{d}\delta\boldsymbol{\varepsilon}\, \mathrm{d}V^0$$

which can be rewritten as

$$\int_{V^0} \boldsymbol{\tau}^{\mathrm{c}} : \partial_{\mathrm{N}}\delta\boldsymbol{\varepsilon}\, \mathrm{d}V^0$$

and further leads

$$\int_{V^0} \boldsymbol{\tau}^{\mathrm{c}} : \partial_{\mathrm{N}}\boldsymbol{\beta}_{\mathrm{M}}\, \mathrm{d}V^0$$

where this term contributes to the Jacobian and is the "initial stress matrix."

The external load rate terms in (10.10) are considered next. In general, these load vectors can be written

$$\boldsymbol{t} = \boldsymbol{t}(\lambda, \boldsymbol{x}) \quad \text{and} \quad \mathbf{f} = \mathbf{f}(\lambda, \boldsymbol{x}) \tag{10.16}$$

where λ represents the externally prescribed loading parameters. Whether the load depends on position or not, it is up to the particular load type, but common types of loading (pressure, centrifugal load) do depend on position—for example, if $\boldsymbol{t}$ is caused by pressure on the surface, $\boldsymbol{t}$ depends on the pressure magnitude, on the direction of the normal to the surface, and on the current surface area: the latter two are functions of the current position of points on the surface. The variation of the load vector with nodal variables can then be written symbolically as

$$\partial_{\mathrm{N}}\boldsymbol{t} + \boldsymbol{t}\frac{1}{A_{\mathrm{r}}}\partial_{\mathrm{N}}A_{\mathrm{r}} = \boldsymbol{Q}^{\mathrm{S}}_{\mathrm{N}} \tag{10.17}$$

$$\partial_{\mathrm{N}}\mathbf{f} + \mathbf{f}\frac{1}{J}\partial_{\mathrm{N}}J = \boldsymbol{Q}_{\mathrm{N}}^{\mathrm{V}} \tag{10.18}$$

and then writing

$$\delta\boldsymbol{v} = \boldsymbol{N}_{\mathrm{M}}\delta\boldsymbol{v}^{\mathrm{M}} \tag{10.19}$$

where $\boldsymbol{N}_{\mathrm{M}}$ is obtained directly from the interpolation functions, we can write the Jacobian terms pertaining to the last four terms of (10.10) as

$$-\int_s \boldsymbol{N}_{\mathrm{M}}^{\mathrm{T}} \cdot \boldsymbol{Q}_{\mathrm{N}}^{\mathrm{S}}\, \mathrm{d}S - \int_V \boldsymbol{N}_{\mathrm{M}}^{\mathrm{T}} \cdot \boldsymbol{Q}_{\mathrm{N}}^{\mathrm{V}}\, \mathrm{d}V$$

these are commonly called the "load stiffness matrix." The actual form of the load stiffness is very much dependent on the type of load being considered

The complete Jacobian matrix is then

$$\begin{aligned} K_{\mathrm{MN}} = &\int_{V^0} \boldsymbol{\beta}_{\mathrm{M}} : \boldsymbol{H} : \boldsymbol{\beta}_{\mathrm{N}}\, \mathrm{d}V^0 + \int_{V^0} \boldsymbol{\tau}^{\mathrm{c}} : \partial_{\mathrm{N}}\boldsymbol{\beta}_{\mathrm{M}}\, \mathrm{d}V^0 \\ &- \int_s \boldsymbol{N}_{\mathrm{M}}^{\mathrm{T}} \cdot \boldsymbol{Q}_{\mathrm{N}}^{\mathrm{S}}\, \mathrm{d}S - \int_V \boldsymbol{N}_{\mathrm{M}}^{\mathrm{T}} \cdot \boldsymbol{Q}_{\mathrm{N}}^{\mathrm{V}}\, \mathrm{d}V \end{aligned} \tag{10.20}$$

with the advances of various kinds of commercial finite element software, most of procedures described above have been automated. The challenges arise that the general-purpose finite element software is used to specific problems such as in microelectronics with advanced analysis techniques and methods.

10.5.1.2 Nonlinear Solution Methods

The finite element modeling usually relates to nonlinear problem and can involve from a few to thousands of variables. In terms of these variables, the equilibrium equations obtained by discretizing the virtual work equation can be written symbolically as

$$F^{\mathrm{N}}(u^{\mathrm{M}}) = 0 \tag{10.21}$$

where F^{N} is the force component conjugate to the Nth variable in the problem and u^{M} is the value of the Mth variable. The basic problem is to solve (10.2) for the u^{M} throughout the history of interest.

Many of the problems are nonlinear and history-dependent, so the solution must be developed by a series of "small" increments. Two issues arise: how the discrete equilibrium statement (10.21) is to be solved at each increment, and how the increment size is chosen.

Newton's method is generally used as a numerical technique for solving the nonlinear equilibrium equations. The motivation for this choice is primarily the convergence rate obtained by using Newton's method compared to the convergence rates exhibited by alternate methods (usually modified Newton or quasi-Newton methods) for the types of nonlinear problems. The basic algorithm of Newton's method is as follows. Assume that, after an iteration i, an approximation u_i^{M}, to the solution has been obtained. Let c_{i+1}^{M} be the difference between this solution and the exact solution to the discrete equilibrium (10.21). This means that

$$F^{\mathrm{N}}(u_i^{\mathrm{M}} + c_{i+1}^{\mathrm{M}}) = 0 \tag{10.22}$$

expanding the left-hand side of this equation in a Taylor series about the approximate solution then gives

$$F^{\mathrm{N}}(u_i^{\mathrm{M}}) + \frac{\partial F^{\mathrm{N}}}{\partial u^{\mathrm{P}}}(u_i^{\mathrm{M}})c_{i+1}^{\mathrm{P}} + \frac{\partial^2 F^{\mathrm{N}}}{\partial u^{\mathrm{P}}\partial u^{\mathrm{Q}}}(u_i^{\mathrm{M}})c_{i+1}^{\mathrm{P}}c_{i+1}^{\mathrm{Q}} + \cdots + = 0 \tag{10.23}$$

if u_i^{M} is a close approximation to the solution, the magnitude of each c_{i+1}^{M} will be small, and so all but the first two terms above can be neglected giving a linear system of equations:

$$K_i^{\mathrm{NP}} c_{i+1}^{\mathrm{P}} = -F_i^{\mathrm{N}} \tag{10.24}$$

where

$$K_i^{\mathrm{NP}} = \frac{\partial F^{\mathrm{N}}}{\partial u^{\mathrm{P}}}(u_i^{\mathrm{M}}) \tag{10.25}$$

is the Jacobian matrix and

$$F_i^{\mathrm{N}} = F^{\mathrm{N}}(u_i^{\mathrm{M}}) \tag{10.26}$$

the next approximation to the solution is then

$$u_{i+1}^{\mathrm{M}} = u_i^{\mathrm{M}} + c_{i+1}^{\mathrm{M}} \tag{10.27}$$

and the iteration continues.

Convergence of Newton's method is best measured by ensuring that all entries in F_i^{N} and all entries in c_{i+1}^{N} are sufficiently small. Both these criteria are checked by default in a solution.

Newton's method is usually avoided in large finite element codes, apparently for two reasons. First, the complete Jacobian matrix is sometimes difficult to formulate; and for some problems it can be impossible to obtain this matrix in closed form, so it must be calculated numerically—an expensive (and not always reliable) process.

Secondly, the method is expensive per iteration, because the Jacobian must be formed and solved at each iteration. The most commonly used alternative to Newton is the modified Newton method, in which the Jacobian in (10.25) is recalculated only occasionally (or not at all, as in the initial strain method of simple contained plasticity problems). This method is attractive for mildly nonlinear problems involving softening behavior (such as contained plasticity with monotonic straining) but is not suitable for severely nonlinear cases.

Another alternative is the quasi-Newton method, in which (10.24) is symbolically rewritten

$$c_{i+1}^{\mathrm{P}} = -[K_i^{\mathrm{NP}}]^{-1} F_i^{\mathrm{N}} \tag{10.28}$$

and the inverse Jacobian is obtained by an iteration process.

There are a wide range of quasi-Newton methods. The more appropriate methods for structural applications appear to be reasonably well behaved in all but the most extremely nonlinear cases—the trade-off is that more iterations are required to converge, compared to Newton. While the savings in forming and solving the Jacobian might seem large, the savings might be offset by the additional arithmetic involved in the residual evaluations (that is, in calculating the F_i), and in the cascading vector transformations associated with the quasi-Newton iterations. Thus, for some practical cases quasi-Newton methods are more economic than full Newton, but in other cases they are more expensive.

When any iterative algorithm is applied to a history-dependent problem, the intermediate, nonconverged solutions obtained during the iteration process are usually not on the actual solution path; thus, the integration of history-dependent variables must be performed completely over the increment at each iteration and not obtained as the sum of integrations associated with each Newton iteration, c_i. This is done by assuming that the basic nodal variables, u, vary linearly over the increment so that

$$u(\boldsymbol{\tau}) = \left(1 - \frac{\boldsymbol{\tau}}{\Delta t}\right) u(t) + \frac{\boldsymbol{\tau}}{\Delta t} u(t + \Delta t) \tag{10.29}$$

where $0 \leq \boldsymbol{\tau} \leq \Delta t$ represents "time" during the increment. Then, for any history-dependent variable, $g(t)$, we compute

$$g(t + \Delta t) = g(t) + \int_t^{t+\Delta t} \frac{\mathrm{d}g}{\mathrm{d}\boldsymbol{\tau}}(\boldsymbol{\tau})\, \mathrm{d}\boldsymbol{\tau} \tag{10.30}$$

at each iteration.

The issue of choosing suitable time steps is a difficult problem to resolve. First of all, the considerations are quite different in static, dynamic, or diffusion cases. It is always necessary to model the response as a function of time to some acceptable level of accuracy. In the case of dynamic or diffusion problems, time is a physical dimension for the problem, and the time stepping scheme

must provide suitable steps to allow accurate modeling in this dimension. Even if the problem is linear, this accuracy requirement imposes restrictions on the choice of time step. In contrast, most static problems have no imposed time scale, and the only criterion involved in time step choice is accuracy in modeling nonlinear effects. In dynamic and diffusion problems, it is exceptional to encounter discontinuities in the time history, because inertia or viscous effects provide smoothing in the solution. However, in static cases sharp discontinuities (such as bifurcations caused by buckling) are common. Softening systems, or unconstrained systems, require special consideration in static cases but are handled naturally in dynamic or diffusion cases. Thus, the considerations upon which time step choice is made are quite different for the three different problem classes.

Both "automatic" time step choice and direct user control for all classes of problems are provided. Direct user control can be useful in cases where the problem behavior is well understood (as might occur when the user is carrying out a series of parameter studies) or in cases where the automatic algorithms do not handle the problem well. However, the automatic schemes are based on extensive experience with a wide range of problems. Therefore, it generally can provide a reliable approach.

One other ingredient in this algorithm is that a minimum increment size is specified, which prevents excessive computation in cases where buckling, limit load, or some modeling error causes the solution to stall. This control is handled internally, with user override if needed. Several other controls are built into the algorithm; for example, it will cut back the increment size if an element inverts due to excessively large geometry changes. These detailed controls are based on empirical testing.

In dynamic analysis when implicit integration is used, the automatic time stepping is based on the concept of half-step residuals. The basic idea is that the time stepping operator defines the velocities and accelerations at the end of the step $(t + \Delta t)$ in terms of displacement at the end of the step and conditions at the beginning of the step. Equilibrium is then established at $(t + \Delta t)$ which ensures an equilibrium solution at the end of each time step and, thus, at the beginning and end of any individual time step. However, these equilibrium solutions do not guarantee equilibrium throughout the step. The time step control is based on measuring the equilibrium error (the force residuals) at some point during the time step, by using the integration operator, together with the solution obtained at $(t + \Delta t)$, to interpolate within the time step. The evaluation is performed at the half step $(t + \Delta t/2)$. If the maximum entry in this residual vector—the maximum "half-step residual"—is greater than a user-specified tolerance, the time step is considered to be too big and is reduced by an appropriate factor. If the maximum half-step residual is sufficiently below the user-specified tolerance, the time step can be increased by an appropriate factor for the next increment. Otherwise, the time step is deemed adequate. The algorithm is somewhat more complicated at traumatic events such as impact. Here, the time step can also be adjusted based on the magnitude of residuals in the first or second iteration following such events.

Clearly, if these residuals are several orders of magnitude greater than those permitted, convergence is unlikely and the time step is altered immediately to avoid unproductive iteration.

10.5.2 Advanced Modeling Techniques in Finite Element Analysis

10.5.2.1 Submodeling

Submodeling or global-local-modeling is a finite element technique used to get more accurate results in a region of interest. Often in finite element analysis, the finite element mesh may be too coarse to produce satisfactory results in a region of interest, such as a stress concentration region in a stress analysis. The results away from this region, however, may be adequate.

To obtain more accurate results in such a region, there are two options: (a) reanalyze the entire model with greater mesh refinement, or (b) generate an independent, more finely meshed model of only the region of interest and analyze it. Obviously, option (a) can be time-consuming and costly (depending on the size of the overall model). Option (b) is the submodeling technique.

Submodeling is also known as the cut-boundary displacement method or the specified boundary displacement method. The cut boundary is the boundary of the submodel, which represents a cut through the coarse model are specified as boundary conditions for the submodel.

Submodeling is based on St. Venant's principle, which states that if an actual distribution of stress and strain is altered only near the regions of load application. This implies that stress concentration effects are localized around the concentration; therefore, if the boundaries of the submodel are far enough away from the stress concentration, reasonably accurate results can be calculated in the submodel.

Aside from the obvious benefit of giving more accurate results in a region of the model, the submodeling technique has other advantages:

1. It reduces, or even eliminates, the need for complicated transition regions in solid finite element models.
2. It makes easier to experiment with different designs for the region of interest.
3. It helps in determining the adequacy of mesh refinement. Some restrictions for the use of submodeling are.
4. It is valid only for solid elements and shell element.
5. The principle behind submodeling assumes that the cut boundaries are far enough away from the stress concentration region. It is necessary to verify that this assumption is adequately satisfied.

Below, Fig. 10.4 is an example of the application of submodeling technique in ANSYS.

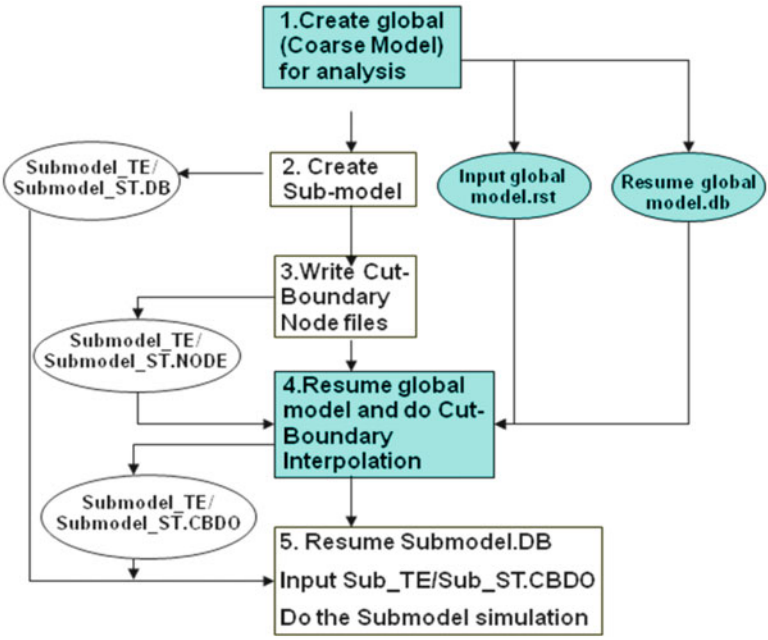


Fig. 10.4 Flowchart of the submodeling technique with ANSYS

10.5.2.2 Substructure Modeling

Substructuring is a procedure that condenses a group of finite elements into one element represented as a matrix. This single matrix element is called a superelement.

One of the reasons for substructuring is to reduce computer time. Example of this reason is nonlinear analyses of structures that contain repeated geometrical patterns. In a nonlinear analysis, one can substructure the linear portion of the model so that the element matrices for that portion need not be recalculated for every iteration. In a structure with repeated patterns, one can generate on superelement to represent the pattern and simply make copies of it at different location, thereby saving a significant amount of computer time. Another reason is to allow solution of very large problems with limited computer resources. An example of this reason is an analysis that is too large for the computer in terms of wave front size or disk space requirements. In such a situation, one can analyze the model in pieces, where each piece is a superelement small enough to fit on the computer.

The advantages of substructuring are as follows:

1. Separates linear and nonlinear parts of the model
2. Allows repetition of symmetrical or identical parts of the model for linear elastic analysis

3. Separates large models into multiple, moderate-size models
4. Separates fixed model parts from parts of the model that may undergo design changes

The disadvantages of substructuring are the large amount of data that must be stored on the database, and the substructure must be linear.

In finite element implementation, the superelement generation step is done for every superelement at a certain level. The use of superelements in subsequent finite element running runs is done at highest level. The recovery of solution within a certain superelement can or cannot be done for every superelement.

10.5.2.3 Adaptive Mesh Generation

The adaptive mesh generation is an advanced technique for estimating mesh discretization error for certain types of analyses. Using this measure of mesh discretization error, the program can then determine if a particular mesh is fine enough. If not, the program will automatically refine the mesh so that the measured error will decrease. The adaptive mesh generation capability increases the number of element and nodes to improve the accuracy of the solution. There are two adaptive mesh generation methods: one is the h-adaptive method which is based on the geometry to refine the mesh. The other adaptive technique is the p-adaptive which is based on the accuracy criterion to automatically increase or decrease the order of the shape function for the selected elements. The capability is applicable for both linear elastic analysis and nonlinear analysis. The capability can be used for lower-order elements, 3-node triangles, 4-node quadrilaterals, 4-node tetrahedrals, and 8-node hexahedral elements or higher order elements. When used in conjunction with the elastic parameter for linear analysis, the mesh is adapted and the analysis repeated until the error criteria is satisfied.

10.5.2.4 Element Birth and Death

If material is added to (or removed from) a system, certain elements in the model may become existent (or nonexistent). The element birth and death options can be used to deactivate or reactivate (as in mining and tunneling), staged construction (as in shored bridge erection), sequential assembly (as in fabrication of layered computer chips), and many other applications in which one can easily identify activated or deactivated elements by their known locations.

To achieve the element death effect, the finite element program does not actually remove the killed elements, instead, it deactivates them by multiplying their stiffness (or conductivity, or other analogous quantity) by a severe reduction factor. This factor is set to 1.0E − 6 by default, but can be given other values. Element loads associated with deactivated elements are zeroed out of the load vector;

however, they still appear in element-load lists. Similarly, mass, damping, specific heat, and other such effects are set to zero for deactivated elements. The mass and energy of deactivated elements are not included in the summations over the model. An element's strain is also set to zero as soon as that element is killed.

In like manner, when elements are born, they are not actually added to the model; they are simply reactivated. To add an element, the element group is deactivated first, and then reactivated at the proper load step. When an element is reactivated, its stiffness, mass, element loads, etc. return to their full original values. Elements are reactivated having no record of strain history. However, initial strain defined as a real constant will not be affected by birth and death operations. Also, unless large-deformation effects are turned on, some element types will be reactivates in their originally geometric configuration (large-deformation effects should be included to obtain meaningful results). Thermal strains are computed for newly activated elements based on the current load step temperature and the reference temperature. Thus, the newborn elements with thermal loads may not be stress-free as intended.

10.5.2.5 Multiphysics Coupling Analysis

A coupled-field analysis is a combination of analyses from different engineering disciplines (physics fields) that interact to solve a global engineering problem; hence, we often refer to a coupled-field analysis as a multiphysics analysis. When the input of one field analysis depends on the results from another analysis, the analyses are coupled.

Some analyses can have one-way coupling. For example, in a thermal stress problem, the temperature field introduces thermal strains in the structural field, but the structural strains generally do not affect the temperature distribution. Thus, there is no need to iterate between the two field solutions. More complicated cases involve two-way coupling. A piezoelectric analysis in a MEMS structure, for example, handles the interaction between the structural and electric fields: it solves for the voltage distribution due to applied displacements, or vice versa. In a fluid-structure interaction problem, the fluid pressure causes the structure to deform, which in turn causes the fluid solution to change. This problem requires iterations between the two physics fields for convergence.

The coupling between the fields can be accomplished by either direct or indirect (load transfer) coupling. Coupling across fields can be complicated because different fields may be solving for different types of analyses during a simulation. For example, in an induction heating problem, a harmonic electromagnetic analysis calculates Joule heating, which is used in a transient thermal analysis to predict a time-dependent temperature solution. The induction heating problem is

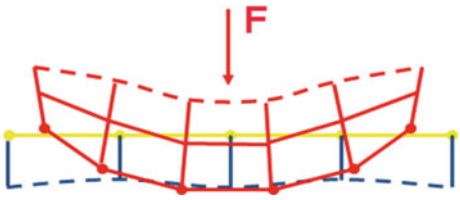


Fig. 10.5 Contact pair with interpenetration

complicated further by the fact that the material properties in both physics simulations depend highly on temperature.

10.5.2.6 Contact Mechanics

When two separate surfaces touch each other such that they become mutually tangent, they are said to be in *contact*. In the common physical sense, surfaces that are in contact have these characteristics:

- They do not interpenetrate.
- They can transmit compressive normal forces and tangential friction forces.
- They often do not transmit tensile normal forces. They are therefore free to separate and move away from each other.

Contact is a *changing-status* nonlinearity. That is, the stiffness of the system depends on the contact status, whether parts are touching or separated. Physical contacting bodies do not interpenetrate. Therefore, the finite element program must establish a relationship between the two surfaces to prevent them from passing through each other in the analysis. Figure 10.5 shows the bad contact model with interpenetration. When the program prevents interpenetration, we say that it *enforces contact compatibility*. Normally, a good finite element software should offer several different *contact algorithms* to enforce compatibility at the contact interface. There are typically three types of algorithms: Augmented Lagrange, Pure Penalty, and Normal Lagrange. Penalty-based methods formulate contact as $[K]\{x\}$, so there is a concept of contact stiffness and some allowable penetration. Normal Lagrange solves contact pressure as a DOF directly, so there is no contact stiffness or penetration, although the solver selection becomes limited because of the unique formulation. Friction describes the tangential behavior between two moving parts. In addition, contact with friction for the tangential or sliding behavior of two contacting bodies is very important in engineering. With friction defined, parts can only slide relative to one another if the tangential force exceeds the product of the normal force and coefficient of friction. Therefore, contact with friction is a function that the advanced finite element should include it and carefully consider it in the modeling and simulation.

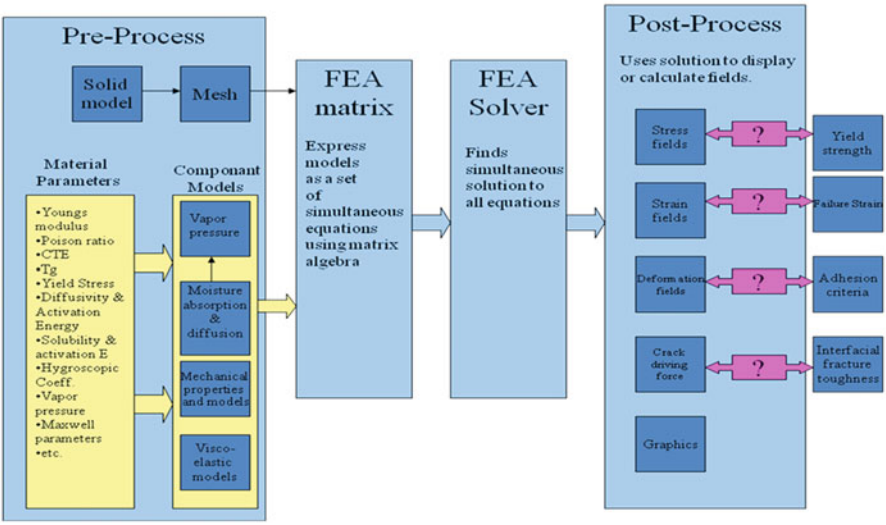


Fig. 10.6 Finite element flowchart for solving the semiconductor packaging

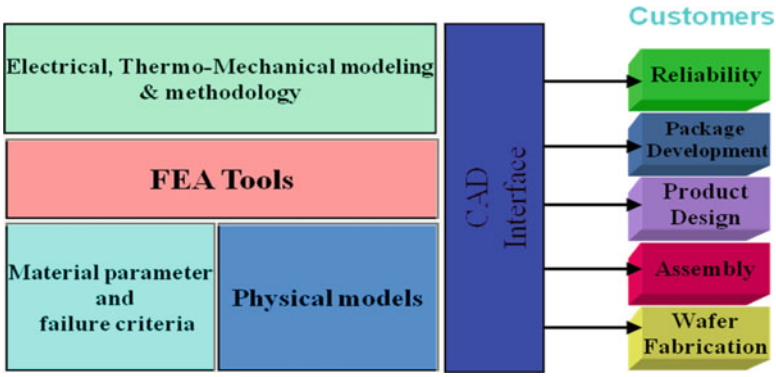


Fig. 10.7 The basic mapping of the modeling and simulation in semiconductor industry

10.5.3 Finite Element Application in Semiconductor Packaging Modeling

Figure 10.6 gives the flowchart of the solving process of the finite element in the fundamental problems in semiconductor packaging.

Figure 10.7 gives the modeling and simulation mapping for the application of finite element to various areas of semiconductor industry. This mapping figure has presented the major functions and roles of the modeling and simulation in semiconductor engineering.

10.6 Modeling Trends in Power Electronic Packaging

The power package development today is becoming increasingly dependent on the rigorous use of proven multiphysics/FEA tools and techniques. Correct use of the modeling tools can definitely save design time and shorten the number of design cycles. The challenge is, can the modeling tool and methodology be ready to support the new trends in the development of new power package technologies? Examples of the challenges include various designs, reliability and assembly modeling which include electromigration simulation; diffusion along the interface of two metal materials; contamination at the interface between lead frame, multiple chips, and EMC; thermal resistance definition in SiP; 3D copper stud bumping and wire bonding simulation, etc.

The greatest challenges in modeling for power packages today are the multiphysics simulations, which couple the electrical, thermal, and mechanical fields, and the assembly process simulation in a multiscale SiP system. The development of highly efficient modeling algorithms for such a SiP system is very critical for the virtual prototyping of new products. In some cases, the SiP might have strong thermomechanical performance but is weak in the electrical area or the SiP has very good electrical performance but is weak in the thermomechanical design. Therefore, it is necessary to determine the best solution using modeling. Package measurements are expensive, time-consuming, and cannot provide all of the required information.

10.6.1 Codesign Automation Simulation

ITRS SiP 2009 white paper [1] describes a future vision of chip-package system codesign: (a) one tool for simultaneous design enabled by a multiuser, cross-functional EDA + system analysis + knowledge-based tool. (b) A wizard-like interface, automatically constructs baseline design for each component based on series of user questions, analysis and an expert system for technology selection and design rules. These ideas cover stress/mechanical modeling, thermal chip-package system and electrical chip-package system. This indicates a modeling trend of the industry is toward package system design automation.

The advance of power package development needs the high efficiency, and short design cycles, in which the FEA use will accelerate the further miniaturization of power electronic components, and accelerate the incorporation of advanced materials and assembly structures. However, most of the power package design engineers, material engineers, test engineers, and the reliability analysis engineers are not familiar with FEA. If they can run designed experiments using FEA for their product optimization in codesigned power package efforts and for material selection, that will really accelerate the power package development. Therefore, to develop the modeling automation system is one trend of the power package

modeling. This system allows people who might not know FEA but wish to do design optimization for their product to run FEA. Engineers just simply input some basic information and set the DOE set, and the system will automatically do the meshing, apply boundary conditions and loads, solve, and automatically output the results. Zhang et al. [6] and Liu [7] have developed the initial modeling automation system for thermal, moisture and linear thermal-mechanical stress analysis. The results have shown great efficiency to save modeling time. Developing the modeling methodology for SiP system needs further to be studied for how to define the thermal resistance for a SiP. A recent investigation of the thermal performance for various power packages has been presented in Fan [8].

10.6.2 Advanced Modeling Methodologies in Power Packaging

One modeling trend of the power package modeling is to develop the advanced methodologies for the current challenges due to the new development of power package in design and assembly. Examples are as follows: as the die size and thickness shrink, die pickup process will become very critical; simulating this pick process is helpful to reduce die cracking [9]. Passivation cracking modeling will help for the metal stacking and layout of passivation layer above the metal [10]. Moisture has a big impact on the power package during wet environmental condition; a systematic modeling and analysis methodology for moisture and vapor pressure have been introduced in Fan [11]. Cu-wire bonding and Cu-stud bumping will induce the failure such as the silicon cratering and BPSG crack under the barrier layer. Development 2D-3D dynamic solution for the wire bonding process can optimize the cu wire bonding parameters [12–14]. Drop test is always interested in and requested by the portable customers. There are a lot of studies toward the drop test modeling [15, 16]. Power WL-CSP will need fully simulation to pass the drop test requirement.

10.6.3 Multiphysics and Multiscale Modeling

During the manufacturing and testing of microsystems, issues of multiphysics and multiscale modeling are involved due to the intrinsic nature of nanomicro scales, and multiphysics behaviors occurring in those processes. Despite the advances made in the current modeling of the structural, thermal, mechanical, and transport properties of materials at the macroscopic level (finite element analysis of complicated structures), there remains tremendous uncertainty about how to predict many properties of interest. For instance, exploiting the tremendous physical and mechanical properties of new nanomaterials by understanding materials at atomic, molecular, and supramolecular levels is useful for designing devices including nanoscale materials and structures. In addition, optical, thermal, electrical, deformation/stress

occur concurrently, which needs coupled-field analysis allowing to determine the combined effects of multiple physical phenomena on a design.

In the development of microsystems such as power electronic packaging, multiphysics effects are inherent and must be addressed absolutely. Microsystems have components with micrometer dimensions. Extensive applications for these devices exist in both commercial and industrial systems. Well-known components such as integrated silicon sensors, power device built in soft substrate, and ultrathin power switch have found to start use in industrial applications.

For such an ultrathin microsystem, there are many multiphysics, one typical example is the electromigration issue which couples electrical, thermal, and mechanical fields. Electromigration in power WL-CSP in both interconnect and solder balls will be a serious challenge as the pitch becomes small due to die shrinks. Modeling of electromigration will help and improve the design of the WL-CSP. Simulation of 3D void generation has been developed in both interconnect and solder bumping level [17]. The further application of the migration simulation method to a package on package (POP) has been studied [18]. Typically, with multiphysics analysis, the exchange of data between the physics fields requires careful coordination, and the different mesh requirements for the various fields, loads, and boundary conditions must be correlated. For all these to function correctly requires a complex feedback loop between the various fields so that the coupled analysis converges to an accurate solution. The predictive FEA simulations more closely represent the real world than simplified assumptions that often neglect accounting for issues that turn out to be critical. Performing multiphysics analysis early in product development enables companies to easily and inexpensively spot and fix problems that can become costly and time-consuming to resolve later. Factoring in the effect of more physics yields more accurate analysis, fewer physical prototypes, a shorter product-development cycle, lower development cost, and a faster time to market and response time to market changes.

Multiscale simulation can be defined as the enabling technology of science and engineering that links phenomena, models, and information between various scales of complex systems. It is recognized that within the scope of materials and structures research, the breadth of length and time scales may range more than 12 orders of magnitude [19]. Different scientific and engineering disciplines for multiscale modeling are involved at each level as shown in Fig. 10.8. The idea of multiscale modeling is straightforward: one computes information at a smaller (finer) scale and passes it to a model at a larger (coarser) scale by leaving out, i.e., coarse-graining, degrees of freedom. From a “bottom-up” perspective, the multiscale approach should consider the intrinsic attributes of the constituent materials for the system of study. The ultimate goal of multiscale modeling is then to predict the macroscopic behavior of an engineering process from first principle, i.e., starting from the quantum scale and passing information into molecular scales and eventually to process scales. In addition, multiscale modeling has the potential to significantly reduce development costs of new nanostructured materials for demanding structural applications by bringing physical and microstructural information into the realm of the design engineer. There are several

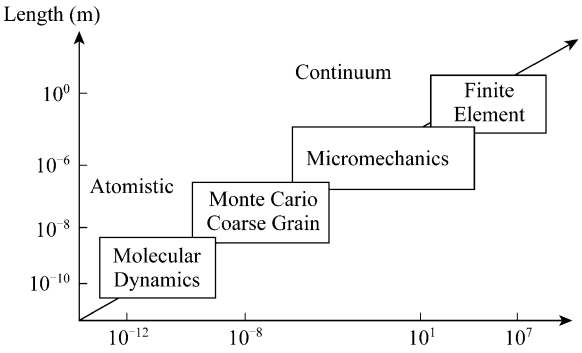


Fig. 10.8 Range of length and time scales of the multiscale modeling [19]

recent studies of the multiscale modeling that have paid attention to ionic polarization layers in polymer electrolytes [20] which could be potentially used for the polymer contamination. Molecular dynamics has been used for the multiscale modeling for moisture, adhesion, delamination between molding compound and metal, and the material properties prediction [21, 22].

10.7 Summary

This chapter first introduces the role of modeling and simulation in power electronic industry. A power electronic packaging from design prototype to final product experiences a lot of assembly processes and extensive reliability testing for extended-life such as those used for automotive electronics, portable power electronics, high power module, etc. The defects in terms of voids, cracks, delaminations, microstructure changes can be induced in any step and may interact and grow in subsequent steps, imposing extreme demands on the fundamental understanding of stressing and physics of failures to improve the design, quality, and reliability. Then, the challenges of modeling tools and methodologies are investigated and discussed, which includes the numerical methods in tools and the next step of development for modeling tools. Then, the modeling requirements in power semiconductor are discussed from power device front-end process, interconnects and passives, circuits modeling to power packaging level. After that, the basic modeling methodologies needed in power packaging are listed, and the advanced modeling techniques are discussed, which includes the basic finite element principals and the advanced finite element methodologies. Finally, the modeling trends in power electronic packagiung are discussed in three directions: (1) Codesign automation simulation, (2) Advance modeling methodologies for the challenges of power electronic packaging, (3) Multiphysics and multiscale simulation.

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Chapter 11
Power Package Thermal and Mechanical Codesign Simulation Automation

Chapter 6 has systematically introduced the thermal management, design, and analysis methods. It is known that the thermal resistance is sensitive to package structure, package material, thermal test board, and ambient conditions. In this chapter, the thermal modeling and simulation and the correlation with test for a regular power chip and a wafer level chip scale power package are presented first. To reduce the design cycle time and solve the thermal and mechanical problems efficiently, a customized tool for power package codesign simulation automation called Automation Simulation System (AutoSim) is developed through finite element software ANSYS® Workbench. With the codesign simulation automation tool, it is easy for users to input necessary data in a friendly and intuitive wizard interface. The whole simulation (including meshing, loading/boundary condition, solving, postprocess, and final report) will be completed automatically and efficiently. This chapter introduces the general methodology of the codesign simulation automation for the IC package.

11.1 Power Package Thermal Modeling and Test Correlation

11.1.1 Background

In the semiconductor industry, thermal management is a key factor that has become important due to the industry trend toward increasingly smaller, faster, and high power devices. While numerical simulation is a powerful tool for thermal management, not only in aiding product engineers for understanding their thermal testing physics, but also in helping package engineers for better design and optimizing their products. Thermal resistance, as an important test parameter, especially for power products, is often used to character the thermal performance of products. JEDEC standard is widely used in semiconductors for the measurement

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of thermal resistance. However, the measurement methodology for power device is different from JEDEC standard; especially the test boards are quite different. This will result in the modeling methodology different for JEDEC standard test based model and power device test based model. In this section, the thermal numerical simulation methodology with finite element method ANSYS is investigated for power application. A 3D power device-D2PAK is employed for modeling with special designed test boards "Mini Pad" and "One Square Inch" board. Thermal resistance is obtained through test and simulation. The correlation between simulation and test is checked to explore a reasonable thermal resistance simulation method.

11.1.2 Thermal Resistance Test Procedure

Thermal resistance is used to characterize a packaged device's thermal performance, which is a measurement ability of a device to dissipate heat while operating in open air without a heat sink.

The thermal resistance θ_{JA} is defined by Sect. 6.1 and it can be rewritten as in the following equation

$$\theta_{JA} = \frac{T_J - T_A}{P_D} \tag{11.1}$$

where

θ_{JA} (°C/W) = Junction-to-ambient thermal resistance of a package
T_J (°C) = Maximum recommended junction temperature
T_A (°C) = Ambient temperature of the application
P_D = Power dissipation of the device

The θ_{JA} testing procedure includes two steps:

(a) Calibration to get calibration factor K
A calibration factor K (which is the slope of the curve in Fig. 11.1) can be defined as

$$K = \frac{1}{\alpha_{SD}} = \frac{T_{J1} - T_{J2}}{V_{SD1} - V_{SD2}} (^\circ\text{C/mV}) \tag{11.2}$$

The purpose of getting calibration factor is to get relationship between V_{SD} and T_J so that T_J can be obtained via V_{SD} in thermal resistance test. Then, place package into oil bath, which provides a steady temperature environment for junction calibration and meanwhile records V_{SD} vs. T_J.

(b) Thermal resistance measurement
Mount the package onto a thermal test board and place it into still air chamber, as shows in Fig. 11.2. Figure 11.3 shows the alternative connection using wires, socket, etc. in the thermal resistance test system.

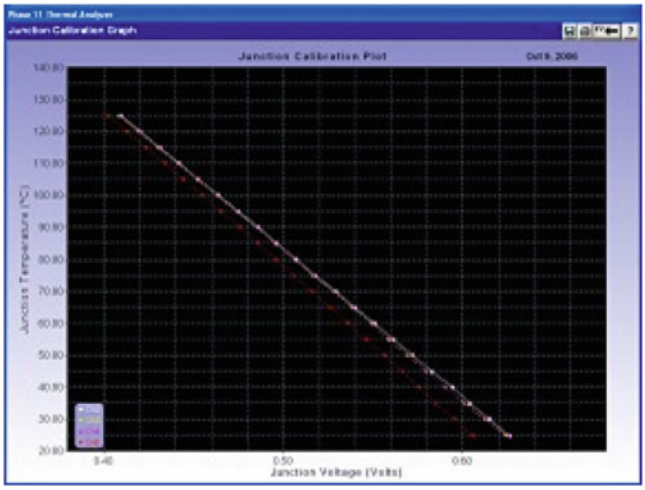


Fig. 11.1 Curve of junction temperature vs. junction voltage

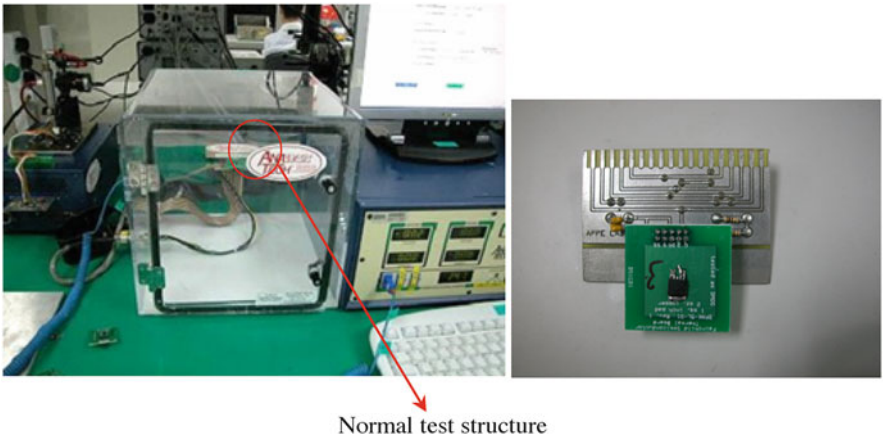


Fig. 11.2 θ_{JA} test equipment

Apply power on die and measure V_{SD}, according to following equation and calculate θ_{JA}.

$$\Delta T_J = K \times \Delta TSP$$

$$\theta_{JA} = (T_{A0} + K\Delta TSP - T_{ASS})/P \tag{11.3}$$

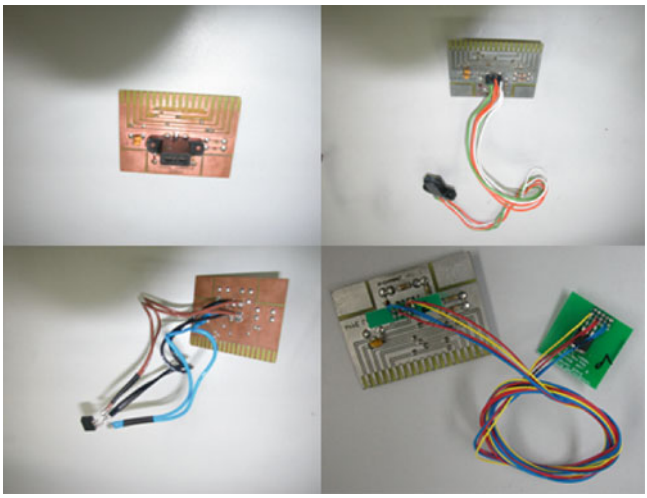


Fig. 11.3 Alternative connection using wires, socket, etc.

Table 11.1 Experimental study of connect fixture function

Legs	Thermal board	Wires	Socket	θ_{JA} (°C/W)
1	No	No	Yes	60.6
2	No	0.2 m, thick	Yes	61.1
3	No	1 m, thick soldering	No	48.9
4	No	0.2 m, thick soldering	No	48.3
5	No	1 m, thin soldering	No	61.9
6	No	0.2 m, thin soldering	No	59.2
7 (Normal)	Mini Pad	No		57.8
8	Mini Pad	1 m thin soldering		51.4
9 (Normal)	One Square Inch	No		32.7
10	One Square Inch	1 m thin soldering		28.9

11.1.3 Influence of Each Factor in Thermal Resistance Test

In order to apply power on the device, an interface board, wires, or socket are necessary to electrical connections for the device. These connection fixtures will unavoidably spread heat into ambient environment. The influence of these factors should be evaluated not only because it is necessary to reduce the unexpected heat loss for getting a reasonable and stable test method but also because it can make the simulation better reflect the actual heat transfer procedure. However, due to the interaction of these factors, it is very hard to find the individual function of each factor, so we designed alternative connection approaches using these fixtures.

The measurement results based on different connect ways for thermal θ_{JA} are summarized in Table 11.1.

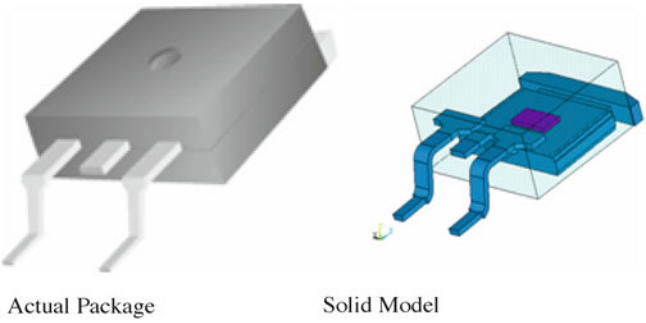


Fig. 11.4 Actual package and its solid model

From Table 11.1, we found the following:

1. Thick wire has more heat spreadability when it is soldering to the lead of package compared to the thin wire.
2. When a socket is used, wires have little influence to the thermal resistance.
3. The normal thermal testing procedure is very reasonable, for this case, the interface board spreads very little heat, even less than the thinner plastic coated wires.

Based on the experimental study, the heat spread by interface board is not significant. So for simplifying the model, we can make the assumption that the effect of interface board is not considered in the modeling.

11.1.4 Package Solid Model

The package studied here is D2PAK, as shown in Fig. 11.4. It consists of die, die attach solder, lead frame, and mold compound. When building the solid model, the bond wires inside the package are neglected for simplicity.

Two types special thermal test boards for power device are investigated. One is "One Square Inch" test board, since one square inch copper layer (about 2 oz thick) covers on the top of the board. Its dimension is 38 $\times$ 38 $\times$ 1.66 mm. Another board is "Mini Pad" test board, since a small pad (about 2 oz thick) whose area is nearly the same as the exposed lead frame at package bottom. Its size is the same as the "One Square Inch" board.

11.1.5 Material Properties and Boundary Conditions

The thermal conductivity parameter for lead frame, die attach, die, mold compound, solder paste, copper trace, and test board is 350, 44, 145, 0.669, 70, 386, and 0.4 W/m K, respectively [1]. In the simulation, materials are assumed as uniform,

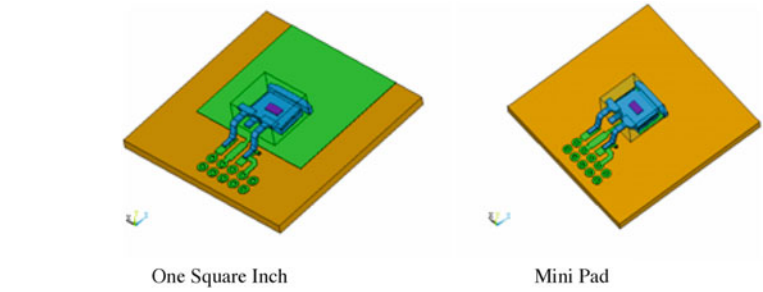


Fig. 11.5 Two types of special designed board for power device

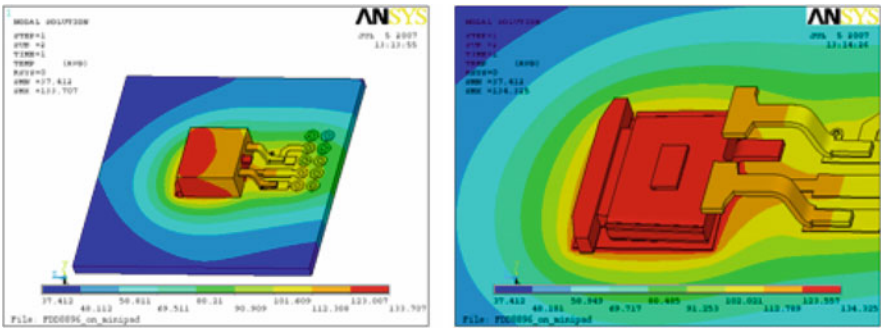


Fig. 11.6 Temperature contour of "Mini Pad" model using empirical heat transfer coefficient "*h*"

and different materials are ideally connected without delamination and voids. In addition, power as a volume load is applied on the die.

Two types of convention boundary conditions are discussed in Fig. 11.5. One is based on the constant empirical film convection coefficient and the other convention boundary is based on temperature-dependent film convection coefficient.

First, constant empirical film convection h is applied. In this case, top of the package is defined as 10 W/m^2 K, the sides and bottom of package/top trace of board as 7.5 W/m^2 K, and rest surfaces of board as 5 W/m^2 K.

Based on above input information, the simulation is run on the "Mini Pad" board, whose temperature contour is shows as Fig. 11.6. Simulation results show that the junction temperature of the die is 134.325°C. Based on (11.1)

$$\theta_{JA} = \frac{T_J - T_A}{P_D} = \frac{134.325 - 25}{1} = 109.3°C/W$$

In order to investigate the relationship of power and θ_{JA} for this load condition, different powers (0.5, 1, 2, 3 W) are applied on the model individually, and draw the curve of θ_{JA} vs. power in Fig. 11.7.

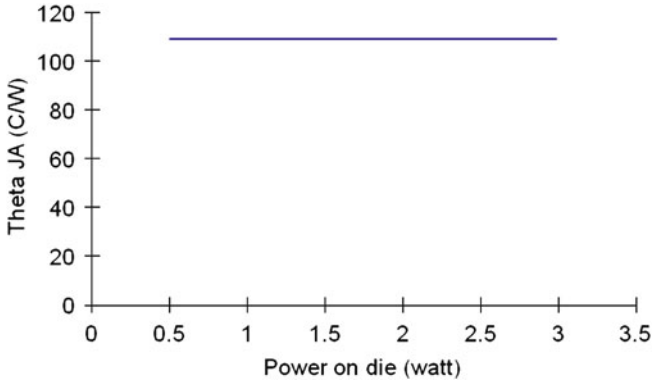


Fig. 11.7 Curve of θ_{JA} vs. power for "Mini Pad" model

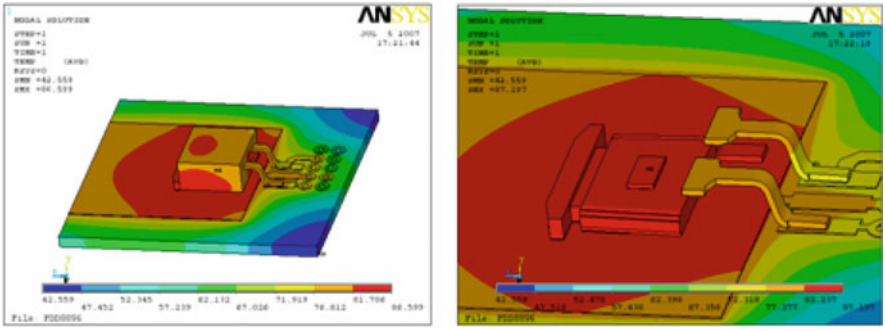


Fig. 11.8 Temperature contour of "One Square Inch" model using empirical heat transfer coefficient "*h*"

The above curve shows that θ_{JA} is independent of the applied power for this case.

In a similar way, we get the temperature contour of "One Square Inch" model, as shown in Fig. 11.8, its θ_{JA} is 62.2°C/W.

The curve of θ_{JA} vs. power is shown in the Fig. 11.9.

Similar conclusion as previous one, θ_{JA} is also independent of power for this case.

Simulation results and the measurement are summarized in Table 11.2. As it shows in the table, simulation results are significantly larger than the measurements.

There are four choices to solve the problem, and make the simulation match the measurement better:

1. Use the experimentally measured heat convection coefficient.
2. Adjust empirical constant film convection by trying lots of simulations and correlate to the measurement.

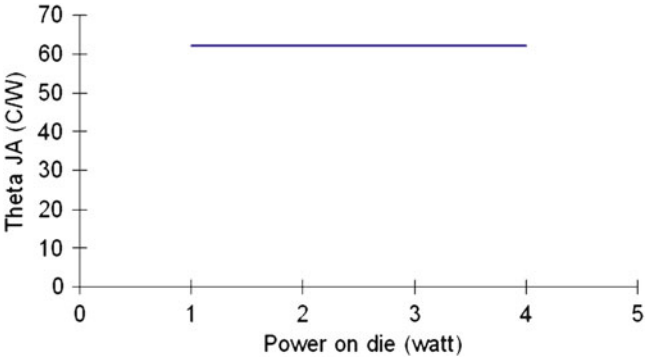


Fig. 11.9 Curve of θ_{JA} vs. power for "One Square Inch" model

Table 11.2 Correlation of simulation result θ_{JA} to the measurement for empirical constant "h"

θ_{JA}	Mini Pad	One Square Inch
Measurement (°C/W)	57.8	32.7
Simulation (°C/W)	109.3	62.2

3. Use Computational Fluid Dynamics (CFD) software.
4. Use empirical film formula to get heat convection coefficient.

As we know that the heat convection transfer coefficient "h" is an experimentally determined parameter whose value depends on all the variables influencing convection such as the surface geometry, the nature of fluid motion, the properties of the fluid, and the bulk fluid velocity [2]. An empirical film formula is developed after correlated with the test data.

$$h_C = Af\left(\frac{T_S - T_A}{P}\right)^n \tag{11.4}$$

where

h_C = Empirical heat convection coefficient (W/in.^{2} °C)
T_S = Surface temperature
T_A = Ambient temperature
P = $WL/[2(L + W)]$ (in.), W = width, L = length (dimensional parameter for horizontal plate)
P = H (in.), H-height (dimensional parameter for vertical plate)
$A = 0.0018 - 0.0025$
$f = 1.22$, $n = 0.35$, vertical plate

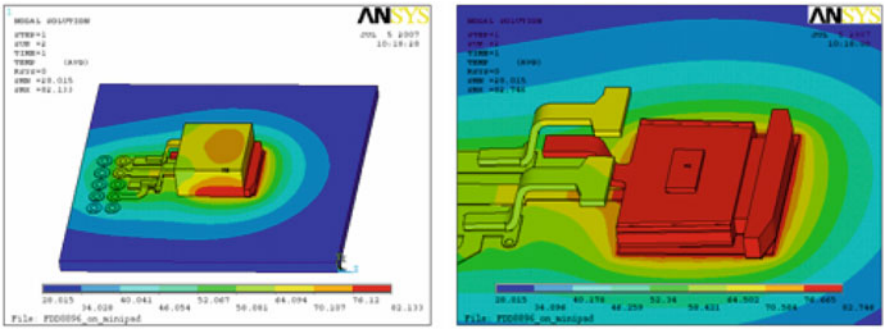


Fig. 11.10 Temperature contour of "Mini Pad" model using temperature-dependent heat transfer coefficient "*h*"

$f = 1.00$, $n = 0.34$, horizontal plate, upper surface
$f = 0.50$, $n = 0.33$, horizontal plate, lower surface

This equation relates the heat transfer coefficient "*h*" to surface temperature, ambient temperature, surface shape, orientation, etc. Use this equation, we developed an ANSYS parametric design language (APDL) code, and got a relationship of "*h*" vs. temperature. Finally apply the nonlinear convection boundary to the surface of the model.

With this method, temperature contour of "Mini Pad" model (power = 1 W) is obtained and as shown in Fig. 11.10.

$$\theta_{JA} = \frac{T_J - T_A}{P_D} = \frac{82.746 - 25}{1} = 57.7^{\circ}\text{C/W}$$

As it was done previously, in order to investigate the relationship of θ_{JA} and power for this load condition, different powers (0.5, 1, 2, 3 W) are applied on the model individually, and got the curve of θ_{JA} vs. powers.

Figure 11.11 shows that θ_{JA} decreases with increased power applied on the device and this can be explained by (11.4), larger power will lead to a high surface temperature of model; furthermore, it will result in a larger "*h*"; therefore, more heat spreads to the ambient environment, and as a result of this, high power results in a lower θ_{JA}.

The same method is applied on "One Square Inch" model, its temperature contour (power = 1 W) shows in Fig. 11.12.

Calculate thermal resistance as follows,

$$\theta_{JA} = \frac{T_J - T_A}{P_D} = \frac{60.11 - 25}{1} = 35.1^{\circ}\text{C/W}$$

And different powers (0.5, 1, 2, 3 W) are applied on the model with One Square Inch board individually. The curve of θ_{JA} vs. power input is shown in Fig. 11.13.

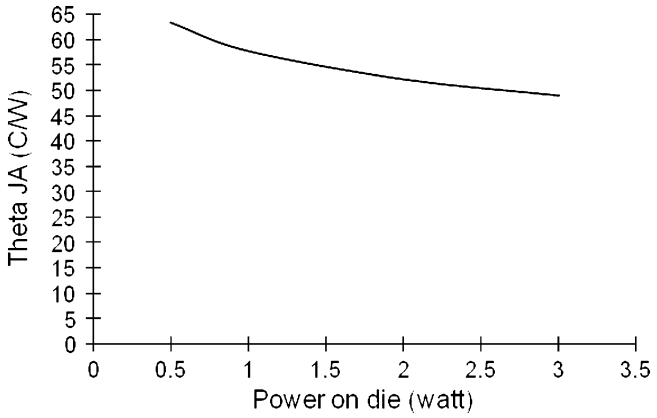


Fig. 11.11 Curve of θ_{JA} vs. power for "Mini Pad" model with temperature-dependent heat transfer coefficient "*h*"

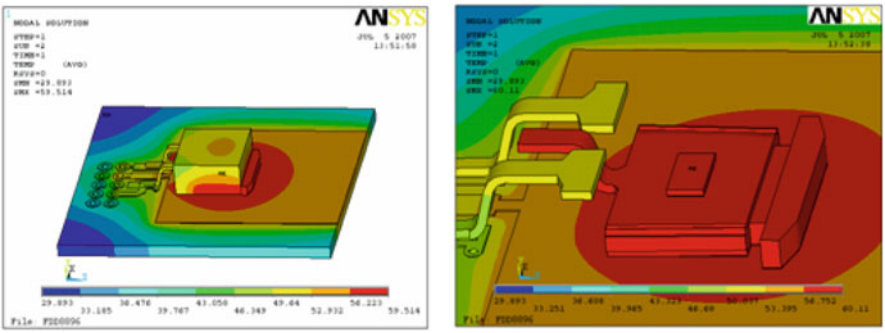


Fig. 11.12 Temperature contour of "One Square Inch" model using temperature-dependent heat transfer coefficient "*h*"



Fig. 11.13 Curve of θ_{JA} vs. power for "One Square Inch" model with temperature-dependent heat transfer coefficient "*h*"

Table 11.3 Correlation of simulation result θ_{JA} to the measurement for temperature-dependent "*h*" with input power 2 W

θ_{JA}	Mini Pad	One Square Inch
Measurement (°C/W)	57.8	32.7
Simulation (°C/W)	52.2	31.8
Variation (%)	9.7	2.8

The simulation results and the measurement data are summarized in Table 11.3, since temperature-dependent heat transfer coefficient "*h*" is applied, the thermal resistance is dependent on the input power.

As shows in the Table 11.3, the variation for each model is within 10% between the test and simulation.

11.1.6 Discussion of the Thermal Simulation and Correlation

With the shrinking of thermal test board from JEDEC size to specially designed power device board size, the empirical heat transfer coefficient "*h*" is not valid anymore to simulate the thermal resistance. While the temperature-dependent heat transfer coefficient "*h*" reflects the impact of many factors such as the shape and the temperature of convection surface to the thermal resistance. Comparison of modeling and measurement results show that this temperature-dependent "*h*" methodology can get very good correlation and the variation is within 10%.

11.2 Wafer Level Power Package Parameter Thermal Simulation

A new type of full thermal parametric model for power wafer level chip scale package (WL-CSP) is developed in this section, which includes parametric WL-CSP and its adaptive parametric JEDEC thermal test board. By employment of the parametric model, package geometry parameters and the trace layout for PCB can easily be changed to meet the requirement of design, so that the influence of all geometry parameters to thermal performance can be investigated fast for the whole series of WL-CSP packages. The entire thermal simulation, including meshing, loading/boundary condition, solving, and postprocessing, is automated with APDL coding. This section introduces the construction of the parametric model for WL-CSP design, and both JEDEC low effective thermal board and high effective thermal conductivity boards with and without thermal vias are included in the model. To study impact of solder ball number, die size, terminal pitch on thermal resistances or parameters, extensive modeling tasks are run and related results are systemically investigated. As verification, a WL-CSP with six balls is actually tested and the results show good agreement between actual measurement and simulation results.

11.2.1 Background for the Power WL-CSP Thermal Analysis

Power WL-CSP becomes more and more popular in semiconductor industry due to its small profile and excellent electrical performance. However, the shrinkage of profile also results in a higher heat concentration, which brings widely concern throughout the industry. As a result of this, to make thermal prediction and its trend in the early design phase is extremely important for a robust design. Therefore, the objective of this section is to develop a full parametric model using commercial software ANSYS, which targets to solve above problems.

The parametric model herein follows JEDEC standards [3, 4], and thermal resistance θ_{JA}, and thermal parameters including ψ_{JB} and ψ_{JC} are taken as objective concerns in this section to characterize thermal performance of WL-CSP. For traditional thermal analysis, when package modeling engineers perform thermal simulation, solid model of thermal board has to be built, and this work takes most of project time, and therefore lengthens project cycle. In addition, although every engineer follows JEDEC, different individual will generate different thermal board due to the tolerance of specified parameters which JEDEC provides (This seems unavoidable for actual manufacturing of thermal board, but can be avoidable for simulation.) and personal understanding of general specification. Comparing with traditional thermal analysis, the thermal parametric model has two outstanding merits.

1. It improves the efficiency of modeling engineers significantly. By employment of the parametric model, modeling engineers don't have to spend much time on understanding of JEDEC standards, also they don't have to take pains to build model and do meshing, what they need do is just to set parameters on demand, and then the entire thermal simulation, including meshing, loading/boundary condition, solving, and postprocessing, will be dealt with and automated by APDL coding.
2. The parametric model can avoid any variation due to unclear or undetailed declaration for JEDEC thermal test board especially for trace layout. This will eliminate the need for the investigator to track the variations and allows focusing on the factors which are of primary concern.

This section introduces the construction of full parametric model for WL-CSP design, and the worst and the best layouts for internal trace are included as extreme cases to evaluate the influence of internal trace layout to thermal resistances or thermal parameters. Both low (1s0p) and high (2s2p, 2s2p with thermal vias) effective thermal conductivity JEDEC boards are included in the model. Then, experiment validated empirical heat convection coefficients are applied to the parametric model, extensive modeling tasks are done to study impact of solder ball number, die size, terminal pitch on thermal resistances or parameters, and related results are systemically investigated as well. As verification, a WL-CSP with six balls will be actually tested finally.

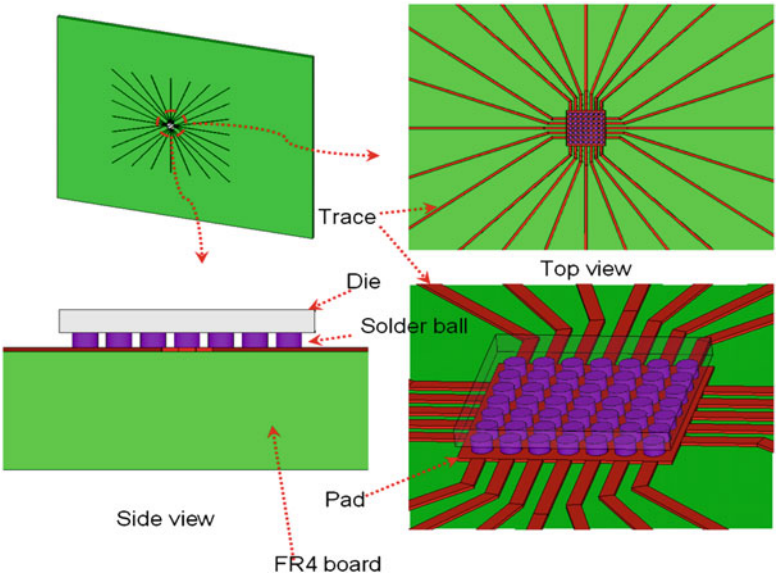


Fig. 11.14 WL-CSP (49 balls) mounted on JEDEC 1s0p thermal test board

11.2.2 Construction of the Parametric Model

As mentioned above, the parametric model consists of package and thermal test board. For a certain package, there are three types of thermal boards existing according to JEDEC standards including 1s0p, 2s2p, and 2s2p with vias. Since 1s0p is a simple case, we begin with that and take 49-ball WL-CSP as an example to introduce how to construct the parametric model.

Figure 11.14 shows the structure of 49-ball WL-CSP, which is mounted on JEDEC 1s0p thermal test board. As shown in Fig. 11.14, the model consists of silicon die, solder balls, copper pads and traces, and FR4 board. The silicon die in the right bottom is set transparent so that the ball array can be shown clearly. All the parameters for the 1s0p parametric model are listed in Table 11.4.

Most parameters in Table 11.4 are easily understood, so they are not explained further. But for some trace-layout-related parameters which may bring confusion to readers, are illustrated in Figs. 11.15 and 11.16.

According to JESD51-9, traces to outer ball row should be flared to perimeter 25 mm from package body, as shown in Fig. 11.15. The distance from package body to perimeter is parameterized as "l_t."

Parameter "l_i" indicates the length of maximum step of traces (see Fig. 11.16): in the case of more balls with finer pitch, the parameter "l_i" should be specified as a bigger value so that the traces will not touch each other to have a better spacing. Parameter "s_{inc}" stands for the length difference between neighboring trace steps; for the same reason, "s_{inc}" also should be defined properly.

Table 11.4 Specified parameters and its description

Parameter	Description	Note
l_{si}	Length of silicon	
w_{si}	Width of silicon	
h_{si}	Height of silicon	
h_{ball}	Height of solder ball	
d_{ball}	Diameter of solder ball	
n_1	Lead number in length of WL-CSP	Need input ($n_1 \geq 2$)
n_2	Lead number in width of WL-CSP	Need input ($n_1 \geq 2$)
p	Pitch	
l_{board}	Length of board	114.5 mm (PKG $\leq$ 40 mm) 139.5 mm (40 $<$ PKG $\leq$ 65 mm) 165.0 mm (65 $<$ PKG $\leq$ 90 mm)
w_{board}	Width of board	101.5 mm (PKG $\leq$ 40 mm) 127.0 mm (40 $<$ PKG $\leq$ 65 mm) 152.5 mm (65 $<$ PKG $\leq$ 90 mm)
h_{board}	Height of board	1.6-h_{trace}
w_{trace}	Width of trace	40% of p for $p > 0.5$ mm 50% of p for $p \leq 0.5$ mm
h_{trace}	Height of trace	70 μm for $p > 0.5$ mm 50 μm for $p \leq 0.5$ mm
l_t	Minimum length of trace	25 mm
s_{inc}	Strep increase of trace	Can be adjusted according to ball number and pitch
l_i	Initial shrinkage length of trace	Can be adjusted according to ball number and pitch

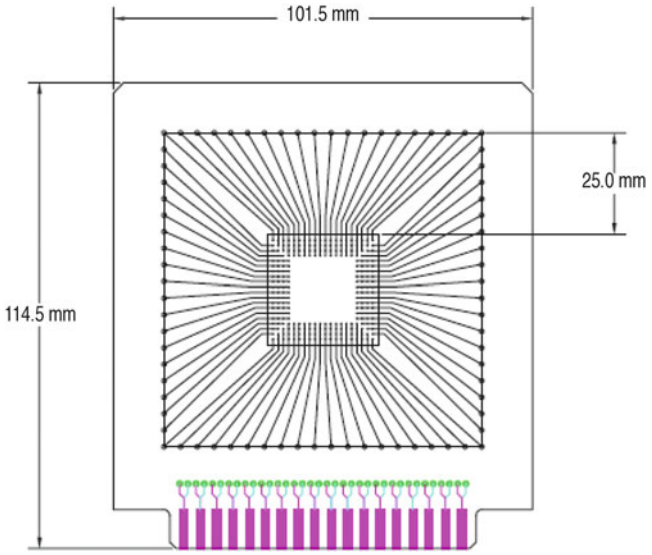


Fig. 11.15 A typical trace layout for JEDEC 1s0p thermal test board

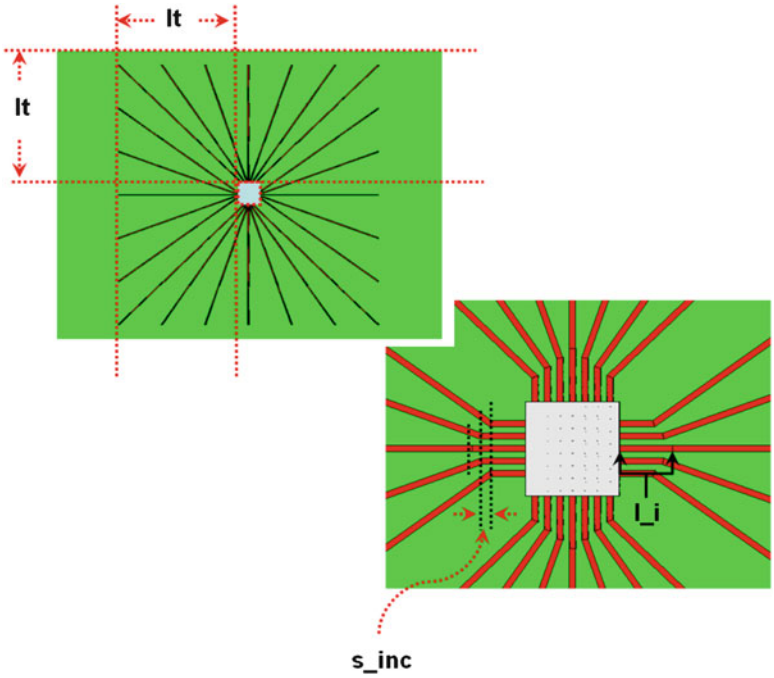


Fig. 11.16 Illustration of trace layout related parameters

One point should be noted that both "l_i" and "s_{inc}" are not specified in JEDEC standards. One advantage of the parametric model herein is: we can define values or rules for specifying above two parameters by ourselves. This leads us to eliminate the variation of models due to the uncontrolled factors.

For the parametric model, the major challenge herein is how to parameterize copper trace of thermal test board. For whichever side of board, the lead number should be either odd or even. For odd case, use a "*do. . ." comment to generate half of right side of traces except central one first, and then reflect along a horizontal symmetry axis, and then followed by central trace generation, by this time, all the right side of traces have already been generated. Finally, reflect all the right side of traces along a vertical symmetry axis, as the results of this, all traces along long side orientation are prepared. While for even case, it is similar to odd case, the difference is that the central trace should not be a special concern (see Fig. 11.17).

After generation of the traces along long side orientation, hide all current traces and use same rule to build traces along short edge orientation. One point should be noted that, the boundary traces (in Fig. 11.17, the trace number is 4, 7, 11, 14 for odd case; and 4, 8, 12, 16 for even case) belong to both neighbor sides, so when we build short side orientation traces, should use "*do,i,1,(n2-1)/2-1" instead of "*do, i,1,(n2-1)/2" for odd case, and use "*do,i,1,n2/2-1" instead of "*do,i,1,n2/2" for even case to avoid trace repeat in the same boundary (see Fig. 11.17).

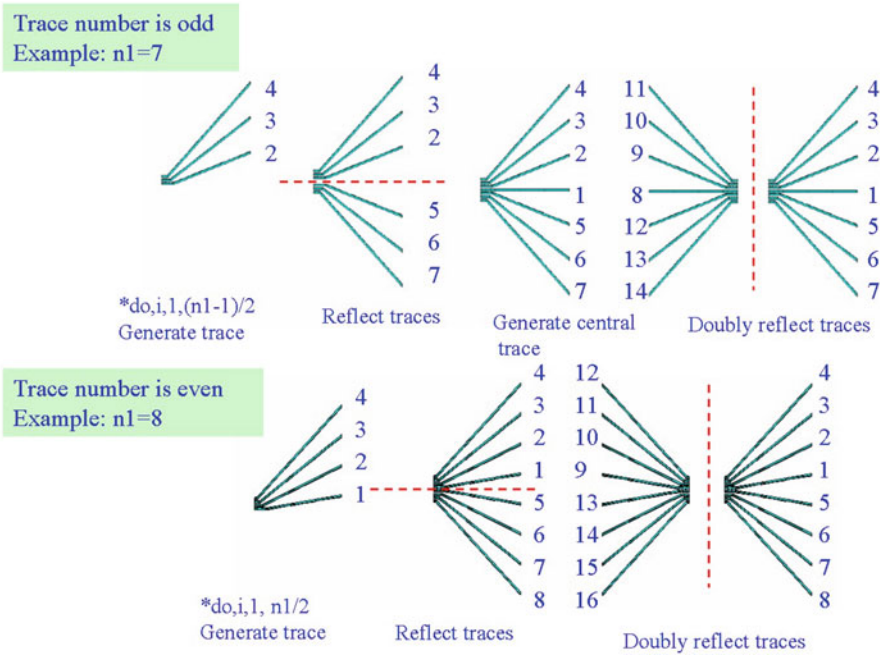


Fig. 11.17 Trace generation flowchart

According to JEDEC, internal pads should be connected to external traces, in order to have a simplified model to improve efficiency, two extreme cases for internal trace layout are designed, which are also used to give the evaluation of internal trace layout to thermal resistances of packages. One is for the best case, which uses a thin block (same thickness with trace, same area with die) to connect all pads, refer to Fig. 11.18a. The other is for the worst case, which only connects outer pads to traces and leave internal pads isolated, see Fig. 11.18b.

Other parts including silicon die, solder ball, and FR4 board are easily parameterized due to its simple geometry. So this part of work is not given in detail.

JEDEC 2s2p thermal board adds bottom signal layer and two buried layers to 1s0p thermal board, while for 2s2p with vias (see Fig. 11.19), one thermal via beneath each ball's pad is designed. These models employ same trace generation methodology and same internal trace design rule. So far, all the three types of thermal boards have been constructed and set-up.

11.2.3 Thermal Automation by Using ANSYS APDL

Whole thermal automation is enabled by using APDL, the main procedure includes the following: (1) Construction of full parametric model, which is already introduced in previous paragraphs. (2) Selection of element type and definition of

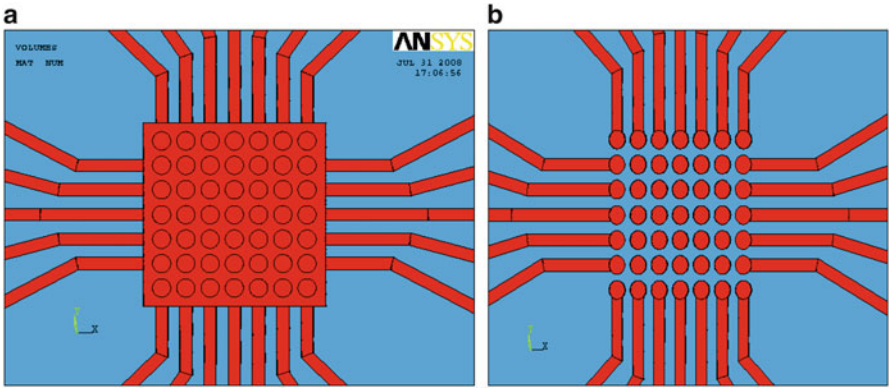


Fig. 11.18 Extreme internal trace layouts. (**a**) The best one. (**b**) The worst one

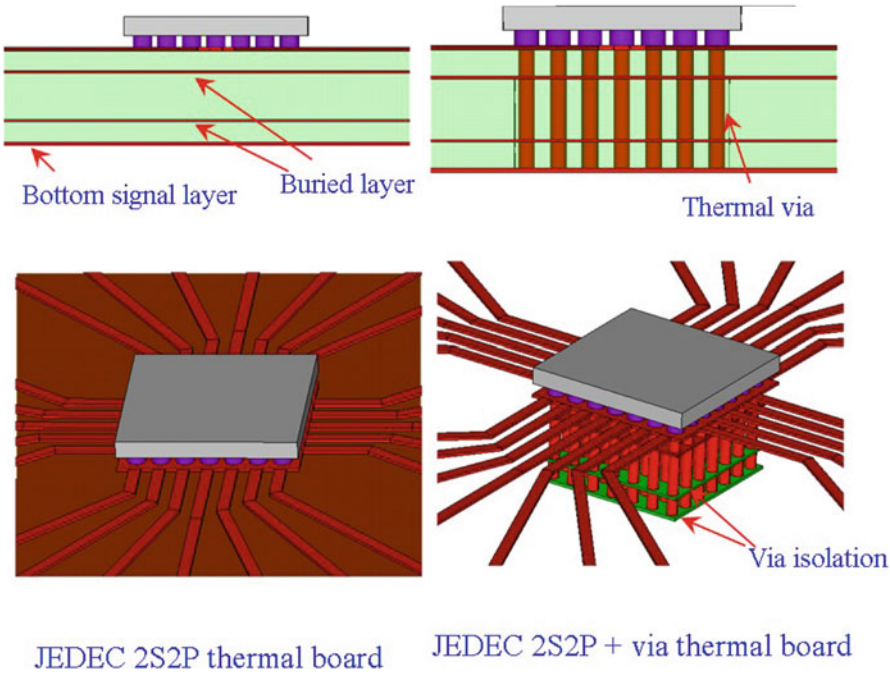


Fig. 11.19 JEDEC high effective board

material properties. (3) Set material ID to volumes by use of entity selection function. (4) Mesh automation by combination of mesh command and entity selection function. (5) Define area components to apply film convection coefficient "*h*" and define volume components to apply heat generation rate. (6) Define arrays to

Table 11.5 Material properties

Material	Thermal conductivity (W/m °C)
Silicon die	145
Solder ball	33
Copper trace and solder	386
FR4	0.4

store component names and its values. (7) Solution setup and use "*do. . ." comment to apply loads or boundary conditions. (8) Results handling and calculation.

The thermal conductivities for all materials are listed in Table 11.5.

11.2.4 Application of the Parametric Model

Thermal performance of WL-CSP under natural convection condition is simulated by use of the parametric model developed here. For a semiconductor device, thermal resistance indicates the steady state temperature rise of the die junction above a given reference for each watt of power (heat) dissipated at the die surface. Its units are °C/W. In addition to these θ thermal resistances, the thermal characterization parameters, denoted by "ψ" can be useful. For a device powered up on an application board, these ψ's provide a correlation between junction temperature and a certain reference temperature. The term "ψ" is used to distinguish these from "θ" thermal resistances, since not all heat is actually flowing between the points of temperature measurement with the ψ's. They are not true thermal resistances for this reason. In this section, thermal resistance θ_{JA} and ψ_{JB} are all used to characterize package performance; they are defined by the following equations:

$$\theta_{JA} = (T_J - T_A)/P$$

$$\psi_{JB} = (T_J - T_B)/P \tag{11.5}$$

where

θ_{JA} = Thermal resistance junction to ambient, °C/W
ψ_{JB} = Thermal parameter junction to board, °C/W
T_J = Die junction temperature, °C
T_A = Ambient temperature, °C
T_B = Board temperature, °C (see Fig. 11.20)

For θ_{JA} evaluation, all the three types of thermal boards are used, while for another thermal parameter ψ_{JB}, 1s0p and 2s2p thermal boards are employed separately. Impact of ball number, die size, and pitch to these thermal resistance and parameters are studied systemically.

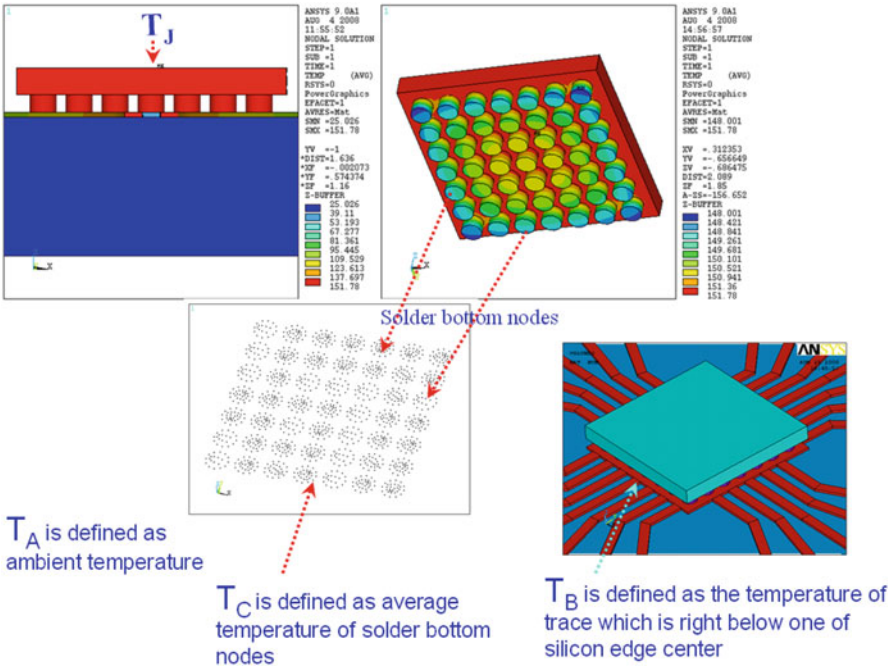


Fig. 11.20 Definition of different temperatures

11.2.5 Thermal Simulation Analysis

11.2.5.1 Impact of Solder Ball Number

In order to investigate the impact of solder ball number to thermal performance of WL-CSP, 3 × 3 mm die size and 0.4 mm pitch are selected, and power is set as 1 W, which applied on the silicon die. And then design ball arrays as 2 × 2, 3 × 3, 4 × 4, 5 × 5, 6 × 6, 7 × 7 separately and input these values to the parametric models including 1s0p, 2s2p, and 2s2p + via thermal test boards. Figure 11.21 gives the temperature distribution of all the WL-CSP packages with the best internal trace design for 1s0p thermal board.

All the results with two types of extreme cases for 1s0p, 2s2p, and 2s2p + via are also summarized in Fig. 11.22. It clearly shows the following:

1. Solder ball number is critical for thermal dissipation. Packages will dissipate heat with higher efficiency through more balls for all three types of boards; therefore, more balls will result in a smaller θ_{JA}. So, if viewed from thermal aspect, it is very important for a certain package to design enough balls to dissipate heat and secure die to work under safe temperature.

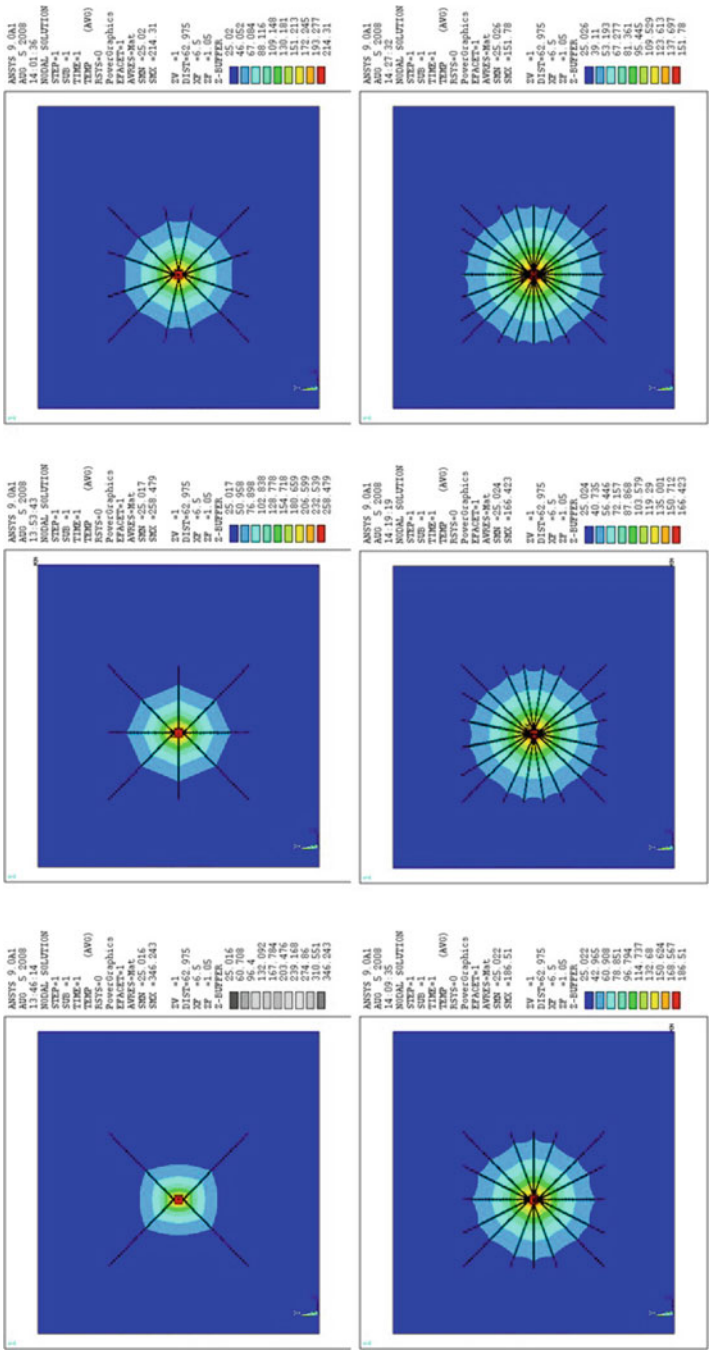


Fig. 11.21 Temperature distribution with different ball array (best internal trace design, 1s0p)

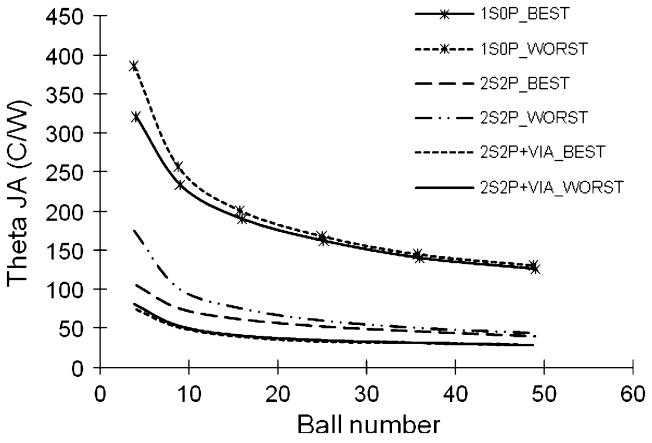


Fig. 11.22 θ_{JA} vs. ball number

2. θ_{JA} curves for 1s0p is far above the ones for 2s2p and 2s2p + via, which means θ_{JA} is really board-dependent; obviously, high effective boards dissipate heat from packages to ambient environment with higher efficiency.
3. The gap between two curves of extreme cases for a certain board reflects the role of internal trace layout design as the function of dissipating heat. Comparison between cases with and without vias tells whether internal trace layout design is invalid or valid for improving heat dissipation, depends on the case if there is design for vertical heat transfer for thermal test board. In the case of thermal vias existing, heat transfers vertically from package to thermal board, for this case, internal trace layout will not work effectively due to its horizontal orientation. So, for customer's application, we should suggest them to concern about internal trace layout for the PCB without effective vertical heat transfer design, especially for the packages with lower ball density.

11.2.5.2 Impact of Die Size

For obtaining impact of die size to thermal performance of WL-CSP, two groups of ball arrays are selected including 2 × 2 and 4 × 4 cases. For 2 × 2 (4 balls) case, designed die size includes 0.85 × 0.85, 1.25 × 1.25, 1.65 × 1.65, 2.05 × 2.05, 2.4 × 2.4, and 3 × 3, while for 4 × 4 (16 balls) case, designed die size includes 1.65 × 1.65, 2.05 × 2.05, 2.4 × 2.4, and 3 × 3. For all these cases, pitch and power keep unchanged, 0.4 mm for pitch and 1 W for power individually. Figure 11.23 gives the temperature distribution of all the cases with the best internal trace design for 2s2p thermal board.

The results for all the cases above are summarized in Fig. 11.23. The curves with six points are for 4-ball cases, and the curves with four points are for 16-ball cases are shown in Fig. 11.24. The conclusion drawn from Fig. 11.24 is listed below:

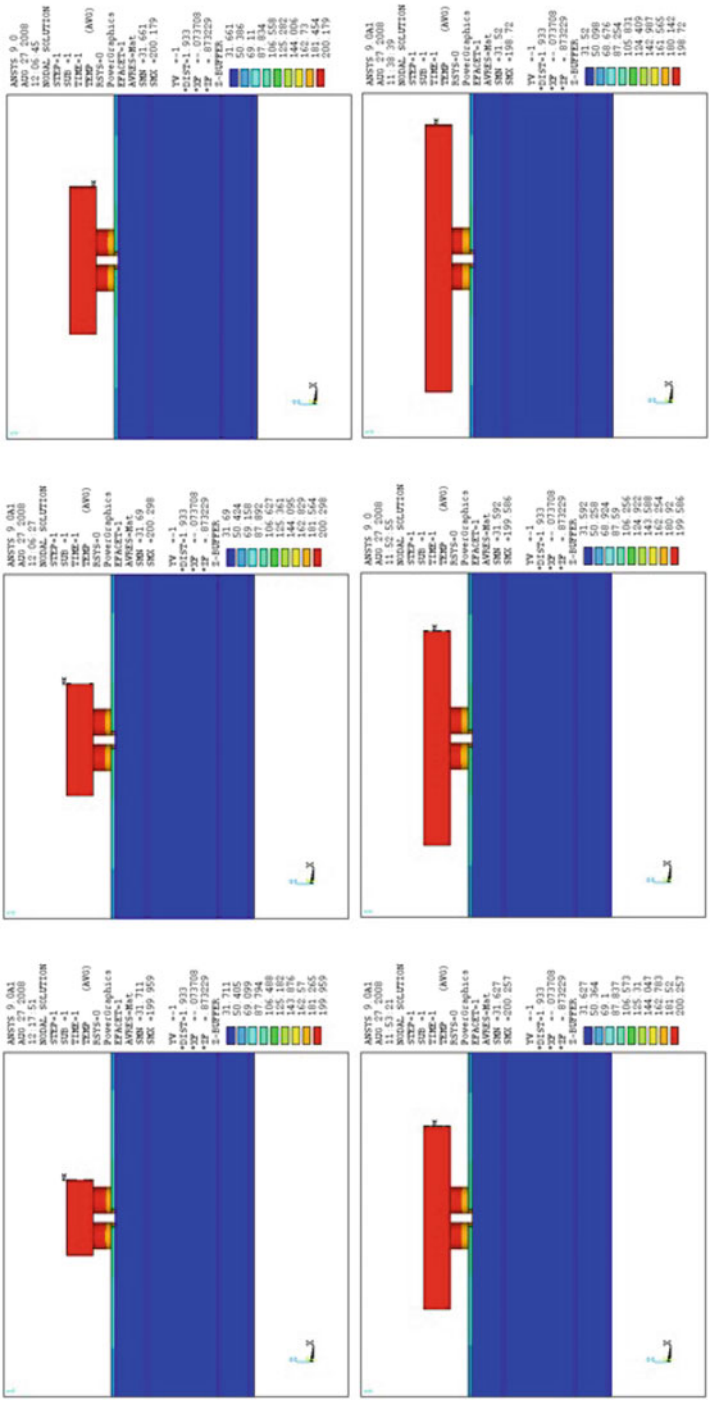


Fig. 11.23 Temperature distribution with different die size (best internal trace design, 2s2p)

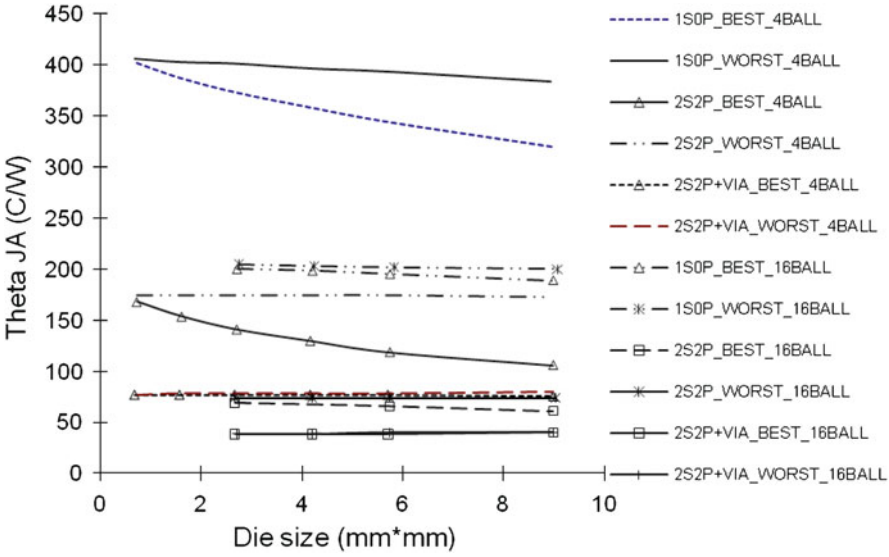


Fig. 11.24 θ_{JA} vs. die size

1. For all the worst internal trace layout designs, the only change is die size; from the curve, we can see that these serials of curves appear flat; this means that increased surface due to the increased die size contributes little to dissipate heat, so θ_{JA} is not sensitive to die size.
2. For the best internal trace layout designs except the cases with vias, θ_{JA} will decrease with increasing die size. Why does this happen? Why is it not same to the cases with the worst internal trace design? If we look back to the construction of the model, we would find that with increasing die size, the thermal test board also changes. Since the copper block right below silicon die has same area to die's, so with increasing die size, the copper block also increases accordingly which enhances heat dissipation; this explains why for this case it seems that θ_{JA} is sensitive to die size.
3. The rules for the role of internal trace layout as the function of dissipating heat, summarized in "5.1 portion" are also consolidated by Fig. 11.24: internal trace layout has very limited impact to θ_{JA} for the thermal test board with thermal vias, and it should be a concern for WL-CSP with bigger size and lower ball density when they are mounted on the board without effective vertical heat transfer path.

11.2.5.3 Impact of Pitch

To evaluate impact of pitch to thermal performance of WL-CSP, five pitch designs including 0.35, 0.4, 0.5, 0.6, and 0.7 mm, with the three types of thermal boards, are prepared. For each experiment, fix die size as 3×3 mm, ball number as 16 (4×4), and power as 1 W. θ_{JA} according to pitch is illustrated in Fig. 11.25.

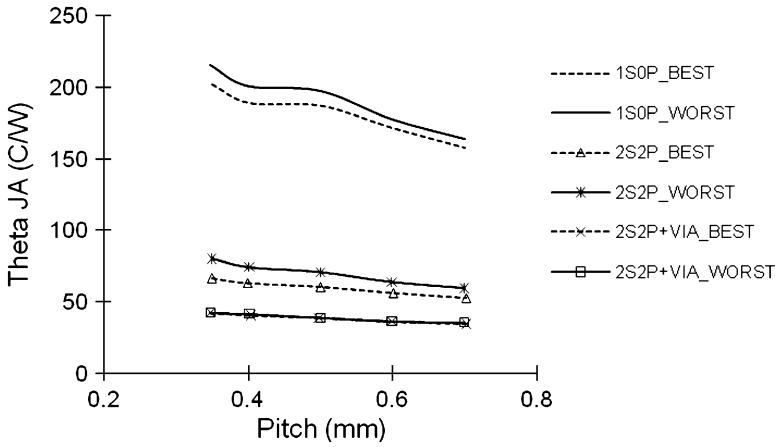


Fig. 11.25 θ_{JA} vs. pitch

Results show that larger pitch has a smaller θ_{JA}, this may be due to two reasons:

1. According to JEDEC standard, larger pitch also needs a wider trace, so this makes PCB dissipate heat with higher efficiency.
2. For all the five designed pitches, larger pitch makes solder ball space more equally, and therefore, it avoids heat crowds and results in a better heat dissipation.

11.2.5.4 Thermal Parameter ψ_{JB}

Thermal parameters ψ_{JB} provides a correlation reference between junction temperature and board temperature. However, because it is not true thermal resistances, the trend of ψ_{JB} is different from θ_{JA} in sometimes, so it seems meaningless to include more study on it. Figure 11.26 shows the trends of ψ_{JB} with best case and worst case as the die size increases, which is quite different from the trend of θ_{JA}.

11.2.5.5 Actual Measurement for a 6-Ball WL-CSP

To correlate simulation result to the actual measurement, actual test is performed on a 6-ball WL-CSP, detailed package, thermal test board, and test apparatus, see Fig. 11.27. This is a 6-ball WL-CSP with 0.65 mm pitch and 1.92 × 1.44 mm die size. Three samples are prepared and tested; according to the results, θ_{JA} falls into the scope from 289 to 309°C/W (see Table 11.6).

Based on the actual construction and dimension of thermal test board, simulations are run to calculate θ_{JA}. The result shows the simulated θ_{JA} is 290°C/W for the

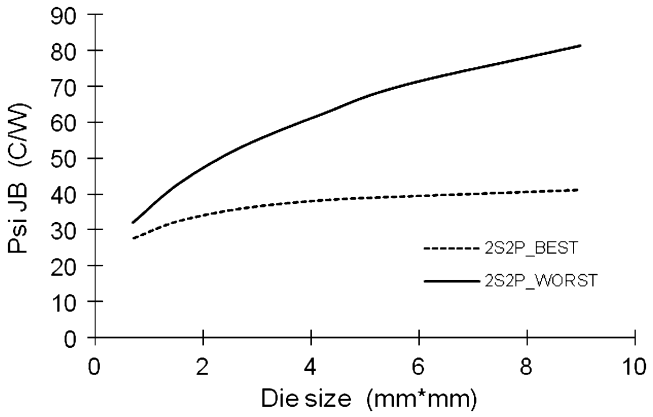


Fig. 11.26 ψ_{JB} vs. die size (4 balls, 0.4 pitch, 1 W, 2s2p)

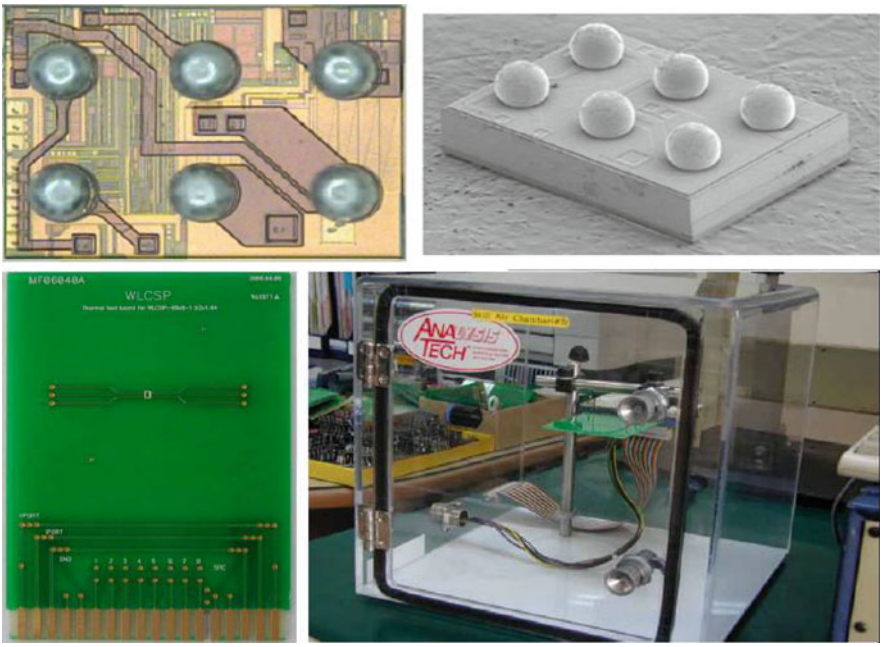


Fig. 11.27 Actual θ_{JA} measurement setup

worst internal trace design and 283°C/W for the best case. Figure 11.28 gives the temperature contour distribution for the worst case. Table 11.7 gives the comparison of the simulated values and the actual measurement. As shown in Table 11.7, variation from simulation to the measurement is about 3.41%, which proves that it fits measurement quite well.

Table 11.6 Actual measurement of 6-ball WL-CSP

Sample 1	Sample 2	Sample 3	Average θ_{JA}
291.18	309.48	289.02	296.56

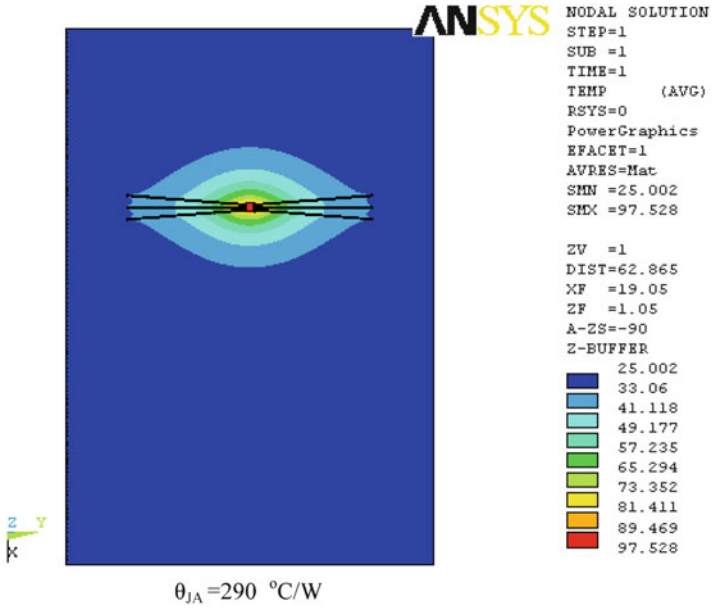


Fig. 11.28 Simulated temperature distribution of 6-ball WL-CSP under 0.25 W power input (1s0p, the worst internal trace layout)

Table 11.7 Simulated θ_{JA} vs. measured θ_{JA} for 6-ball WL-CSP (unit: °C/W)

	Simulation	Measurement
Minimum	283	289
Maximum	290	309
Median or average	286.5 (M)	296.6 (A)
Variation	3.41% off from measurement	

11.2.6 Result Discussion

This section develops a new type of full thermal parametric model for power WL-CSP packages, which includes parametric WL-CSP and its adaptive parametric JEDEC thermal test board. By employment of the parametric model, package geometry parameters can be set freely, and also trace layout for PCB will accordingly change to meet the requirement of package, so that the influence of all geometry parameters to thermal performance can be easily investigated for whole series of WL-CSP packages.

The entire thermal simulation, including meshing, loading/boundary condition, solving, and postprocessing, is automated with ANSYS APDL coding.

Investigation on impact of ball number, die size, and pitch to thermal performance of WL-CSP shows the following: (1) Solder ball number is very critical to thermal performance of WL-CSP; more balls result in a smaller thermal resistance, and therefore, it is important to design proper balls to secure die work under safe temperature. (2) Internal trace layout has significant impact to thermal resistance for boards without effective vertical heat transfer design, so it should be a concern for designing a proper internal trace layout to achieve a better thermal performance, and fully makes of area right below silicon die, especially for the WL-CSP with bigger die size and lower ball density. (3) Equal distribution of balls on silicon die can avoid heat crowds and achieve a better performance for WL-CSP. Correlation of a 6-ball WL-CSP from simulation to measurement also proves the validation of the full thermal parametric model to some extent.

11.3 Package Thermal, Mechanical, Hygroscopic, and Vapor Pressure Codesign Automation Simulation

Modeling and simulation for thermal, mechanical, moisture, and vapor pressure become increasingly vital for codesign of IC package with the rapid increment of packaging density of IC chips, especially for power package. However, in general, IC design engineers and package engineers do not have the skills of performing such simulation and analysis. This result in the lower design efficiency and makes it hard to get the design optimization for the new product. One way of overcoming this problem is to develop a codesign simulation automation tool which can perform the simulation and analysis on package design models automatically. Based on this idea, a customized tool for power package codesign simulation automation called Automation Simulation System (AutoSim) has been developed through finite element software ANSYS Workbench.

11.3.1 Background of the Codesign Automation

With rapid development of microelectronics technology, packaging density of chip has increased quickly and thus very likely to result in higher thermal issues. Overheating and thermal flaws have become the main cause of package quality and reliability. It has been reported that failure rate has near exponential dependence on temperature of electronic component [5]. On the other hand, microelectronic packages are known to absorb moisture when exposed to humid ambient conditions. The presence of moisture in packages induces hygroscopic stress through differential swelling, and induces vapor pressure that is responsible for the eventual popcorn cracking in reflow. Moisture induces the interfacial stresses generated between the die attach and die, die and mold compound, as well as lead

frame and mold compound. This may finally lead to delaminating and package cracking even if the package can pass and withstand the thermal and thermal stress [6–8]. Therefore, thermal, mechanical, moisture, and vapor analysis plays a significant role in development of new generation of IC package design and in the integrity and reliability of microelectronic packaging.

At present, most thermal, mechanical, moisture, and vapor analysis are generally simulated with commercial finite element analysis (FEA) software, which involves complex process of model preprocessing, solution, and postprocessing for individual simulation projects. Researchers are kept to focus on the study of moisture and its related reliability of microelectronic packages [9–11]. Until now, only the high-level professional personnel can perform the simulation by FEA because most IC design engineers, package engineers, assembly process engineers are familiar with their product structure, but poor in modeling and FEA skills.

Obtaining the thermal, mechanical, and moisture simulation results (such as coefficient of thermal expansion (CTE) mismatch stress, hygroscopic stress, and vapor pressure induced stress) is very important to improve the IC package design and reliability for resisting failure [12]. However, most IC package development engineers and reliability engineers may not have the abilities to perform such analysis using FEA. To facilitate the IC package design process and optimize solution, several simulation software programs have been developed to give users convenience in modeling, meshing, or loading. For example, ICEPAK® provides a fully interactive and object-based thermal management software tool. It also expands the ability to handle complex geometry and provide additional flexibility and a higher degree of automation while performing thermal analysis in today's electronics components and systems. PakSi™ is another easy-to-use tool which is developed by Optimal Corporation. It can reduce package modeling and analysis time significantly. Despite these improvements, mistakes can still be easily made by inexperienced users. This includes misrepresenting codesign model boundary conditions, using inappropriate element types, accepting results with an inadequate mesh, and so on. To avoid these incorrect operations, and to assist semiconductor engineers to perform moisture related simulation, it is necessary to develop a fully codesign automated simulation system that has the ability to complete the IC package simulation automatically.

ANSYS Workbench is a new-generation platform used for developing and managing FEA simulations. It not only offers highly integrated engineering simulation platform and bidirectional parametric integration with most available CAD systems but also provides multitiered customization tools to support a variety of development efforts [13]. ANSYS Workbench™ Software Development Kit (SDK) is an open architecture platform that allows customers to develop and integrate application architecture on Workbench environment. Nowadays, Microsoft® Excel® spreadsheet has been widely used in many fields. Especially, Visual Basic® for Application (VBA) expands the capability of Excel to realize many automated and complex tasks. Zhang et al. [14, 15] developed a highly efficient automated simulation system—AutoSim for the thermal analysis in Excel spreadsheet cooperating with ANSYS Workbench. Xia et al. have developed the codesign simulation automation system for the moisture based analysis [16]. A user is only

required to input the basic parameters in Excel interface. Then, the JScript application, which is stored background, will drive and integrate Workbench components automatically to perform the thermal and moisture analysis on packages.

The goal of this section is to expand the AutoSim system to have the capability of thermal, mechanical, and moisture related analysis, including thermal simulation, moisture diffusion analysis, thermal-mechanical stress, hygromechanical stress, and vapor pressure analysis. The AutoSim allows users to select the geometry models from codesigned CAD Library, and then perform various thermal, mechanical, and moisture related analysis automatically. As an example, this customized system has been applied for thermal and moisture diffusion analysis of a Fairchild Molded Leadless Package (MLP) family, and the results are validated using ANSYS-Multiphysics analysis.

11.3.2 Basic Formulations

In Sects. 11.1 and 11.2, we have introduced the definition of the thermal resistance and thermal simulation for power package. Below, we introduce the moisture related theory which includes hygroscopic stress and vapor pressure.

11.3.2.1 Moisture Diffusion and Hygroswelling

Transient moisture diffusion equation is analogous to transient heat conduction equation, and it can be described by Fick's Law as follows:

$$\frac{\partial C}{\partial t} = D\left(\frac{\partial^2 C}{\partial x^2} + \frac{\partial^2 C}{\partial y^2} + \frac{\partial^2 C}{\partial z^2}\right) \tag{11.6}$$

where C is the local moisture concentration, x, y and z are the spatial coordinates, D is the diffusivity which measures the rate of diffusion. However, unlike temperature, the moisture concentration is discontinuous along bimaterial interface. Moisture concentration discontinuity across bimaterial interfaces can be overcome with the use of continuous field variables such as "wetness" [7, 8] w, as follows:

$$w = \frac{C}{C_{\text{sat}}}, \quad 1 \geq w \geq 0 \tag{11.7}$$

where C_{sat} is the saturated moisture concentration. The lower limit $w = 0$ means that material is dry, and the upper limit $w = 1$ means that it is fully saturated with moisture. The (11.1) can also be rewritten as:

$$\frac{\partial w}{\partial t} = D\left(\frac{\partial^2 w}{\partial x^2} + \frac{\partial^2 w}{\partial y^2} + \frac{\partial^2 w}{\partial z^2}\right) \tag{11.8}$$

Table 11.8 Moisture absorption and hygroscopic properties of MLP 6 × 6

Material	D (mm^2/s)	C_{sat} (mg/mm^3)	CME (mm^3/mg)
EMC	4.73e − 7	7.06e − 3	0.222
Die-attach	1.25e − 5	6.20e − 3	0.520

The moisture-thermal analogy using the normalized approach is no longer valid when the saturated moisture concentration is a function of temperature [6, 10–12]. A direct concentration approach (DCA) has been developed to perform moisture diffusion analysis correctly during reflow [12].

Due to CME (Coefficient of Moisture Expansion) mismatch among various materials, the hygroscopic stress is induced. The concept is analogous to the CTE mismatch and the thermomechanical stresses [7–9]. The hygromechanical problem can be solved using the same procedure as thermomechanical solution. It can be described by (11.9) as follows:

$$\varepsilon_h = \beta \cdot C \tag{11.9}$$

where ε_h is the hygrostrain, β is the CME, and $C$is the moisture concentration. The representative values of CME for EMC (Epoxy Mold Compound) and Die attach materials are shown in Table 11.8.

11.3.2.2 Vapor Pressure Model

The moisture exists everywhere in polymer materials in an electronic package after preconditioning. During solder reflow in surface mounting, the temperature of the package body is raised up to 220–260°C. The moisture absorbed in the plastic package becomes vaporized and exerts a pressure on the internal package body. The induced vapor pressure coupled with the thermal stress, hygroscopic stress could result in a failure mechanism often referred to as "popcorn" phenomenon. It is particularly important to analyze the vapor pressure distributions and variations with temperature and moisture concentration.

Most of vapor pressure models that are available in literature assume that the macroscopic delamination or voids exist in packages [10, 11]. Since moisture stays in nanovoids or free-volumes in polymeric materials, a multiscale analysis is needed to develop vapor pressure models. In the following section, a micromechanics based vapor pressure model [10] is introduced. The model has been validated experimentally with many case studies [12]. There are three distinct cases for the vapor pressure evolution from the preconditioning temperature T_0 to the current reflow temperature T [6, 10]. In Case 1, the moisture in the void is in the single vapor phase at T_0, and thus the vapor pressure at T follows the ideal gas law.

When

$$\frac{C_0}{f_0} \leq \rho_g(T_0), \quad P(T) = \frac{C_0 p_g(T_0) T}{\rho_g(T_0) f T_0} \tag{11.10}$$

where P is the pressure, p_g is the saturated vapor pressure and ρ_g is the saturated moisture density.

In Case 2, the moisture is not fully vaporized even at reflow temperature T. The moisture in the void is in the mixed liquid–vapor phase at the temperature from T_0 to T. Thus, the vapor pressure maintains the saturated vapor pressure during the course of the temperature rise.

When

$$\frac{C_0}{f} \geq \rho_g(T), \quad P(T) = p_g(T) \tag{11.11}$$

In Case 3, it is an intermediate case between Cases 1 and 2, where the moisture is in the mixed liquid–vapor phase at a preconditioning temperature T_0, but in the single vapor phase at T. The moisture is fully vaporized at a temperature between preconditioning temperature T_0 and the peak reflow temperature T.

When

$$\begin{cases} \dfrac{C_0}{f_0} > \rho_g(T_0) \\ \dfrac{C_0}{f} < \rho_g(T) \end{cases}, \quad P(T) = p_g(T_1) \frac{T}{T_1} \frac{f(T_1)}{f} \tag{11.12}$$

where T_1 is phase transition temperature at which the moisture can be fully vaporized.

11.3.2.3 Equivalent Coefficient of Thermal Expansion

Thermal conduction is much faster than moisture diffusion. When the external surface is heated to a reflow temperature, the internal package reaches a uniform temperature within a few seconds. Therefore, in the subsequent thermomechanical and vapor pressure models, temperature distribution during reflow can be assumed to be uniform throughout the package body. The temperature load applied is from the stress free reference temperature (usually it selects a curing temperature or a glass transition temperature of the mold compound) to the reflow temperature. For an IC package with EMC, after the moisture absorption, the hygroscopic introduces additional mismatch. The hygroscopic strain can be treated as additional thermal strain, and the same for the vapor pressure which induces additional expansion and

additional mismatch. The vapor pressure induced strain can also be treated as the additional strain.

Assume linear elastic analysis and in the worst case, the vapor pressure and moisture are uniformly distributed. The total linear-elastic strain can be written as [12]

$$\varepsilon_{\mathrm{T}} = \alpha\Delta T + \beta \cdot C + (1 - 2v)p/E \tag{11.13}$$

where ε_{T} is the total linear strain that includes the CTE mismatch strain, hygroscopic strain, and the vapor pressure induced strain, α is the CTE, and ΔT is the temperature changes, v is the Poisson's ratio, E is the modulus, and p is the average vapor pressure. The modulus of mold compound drops a few orders at the reflow temperature; thus, the vapor pressure strain may become as important as thermal or hygroscopic strain in reflow.

The equivalent CTE that integrated thermal CTE, hygroscopic, and vapor pressure can be further expressed as follows:

$$\mathrm{CTE}_{\mathrm{T}} = \alpha + \beta \cdot C/\Delta T + \frac{1 - 2v}{E} p/E/\Delta T \tag{11.14}$$

11.3.3 Development of Automated Codesign Simulation System for Thermal, Mechanical, Moisture, and Vapor Analysis

11.3.3.1 ANSYS Workbench Overview

ANSYS Workbench includes five modules: Design Simulation™, DesignModeler™, CFX-Mesh™, FE Modeler™, and DesignXplorer™. The core of Workbench is the Design Simulation module, which is mainly used for performing structural, thermal, and electromagnetic analyses using the ANSYS solver. DesignModeler is used for creating and modifying CAD geometry to prepare the solid model for using in Design Simulation. CFX-Mesh™ is a mesh generator aimed at producing high-quality meshes for using in CFD simulations. FE Modeler™ supports data transfer from NASTRAN® and ABAQUS® to classic ANSYS. Finally, DesignXplorer™ is used for design optimization. The AutoSim developed in this section is based on Design Simulation and DesignModeler™. Figure 11.29 lists a 3D MLP package model used in AutoSim.

ANSYS workbench is a development platform, which allows the user to carry out various developments through wide range of customization tools. For example, the Simulation Wizard Editor can be used to develop a customized wizard interface. ANSYS Workbench SDK allows the user to develop and integrate applications compatible with the workbench framework and architecture using Application Programming Interfaces (APIs). One of the primary tools in the SDK architecture is the Applet Generator. The Applet Generator is an integrated wizard for Microsoft Visual Studio®, which can produce executable applets using prebuilt Workbench

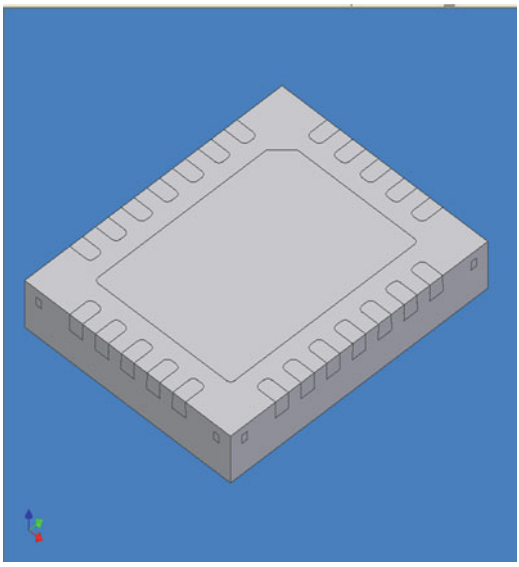


Fig. 11.29 Package model in AutoSim

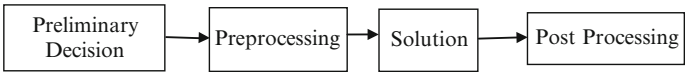


Fig. 11.30 Simulation process in ANSYS Workbench

source code templates. It can also automatically create the customized user interface and finish the applets installation and registration process. In addition to the compiled applications, the Workbench also supports a number of scripting languages including Jscript and VBScript. JScript is recommended as the primary scripting language by ANSYS. Jscript is employed to create the user interface along with HTML and XML. The user can also develop Jscript applications to drive and integrate Workbench components to automate existing processes.

11.3.3.2 General Package Simulation Automated Platform

Generally speaking, every analysis using ANSYS Workbench involves four main steps, as shown the simulation process in Fig. 11.30. As we know, package models from the same family usually have the same or similar structure but different sizes, materials, or number of components. Therefore, a general process can be developed by performing an analysis on all package models from the same family. This general process algorithm can be stored in background and hidden from the user. This algorithm controls material assignment, meshing, loading, and postprocessing.

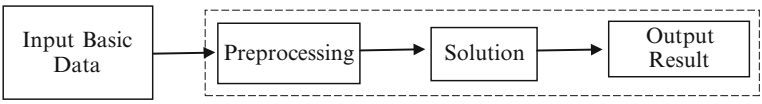


Fig. 11.31 Automated simulation process in AutoSim

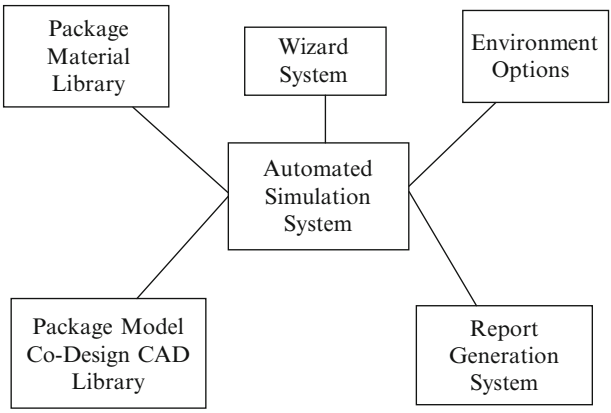


Fig. 11.32 Overall architecture of AutoSim

Figure 11.31 shows the automated simulation process in AutoSim. The user is only required to input the basic data in an intuitive and simple interface and the other steps of preprocessing (meshing, loading and boundary condition), solving, postprocessing, and report will be automatically performed. As we can see, it gives the designers and inexperienced engineers much convenience in performing moisture related analysis. In addition, it ensures the standardization of results.

To build the automated simulation process, the solid model will be developed or loaded first. Usually, a user has to spend much time in building a complex package model using general FEA software during preprocessing. But a CAD model can be directly imported into Workbench because Workbench provides import and bidirectional associated capability with many CAD systems. Additionally, the names of components defined in CAD system will also be imported into Workbench along with the solid model. It is emphasized that the names of components play an important role in distinguishing the components, assigning materials to corresponding components and applying boundary conditions to corresponding components.

Based on the above idea and workbench customization tools, a general automated simulation system (i.e., AutoSim) for thermal stress, moisture diffusion, and hygrothermal stress is developed, which includes five modules: a Package Model Codesign CAD Library, an Executable Wizard System, a Package Material Library, an Environment Options (or Library), and a Report Generation System. The overall architecture of AutoSim is shown in Fig. 11.32.

The Package Model Codesign CAD Library is a core element of AutoSim. First, it is used for storing codesigned CAD models, which provides the user convenience to

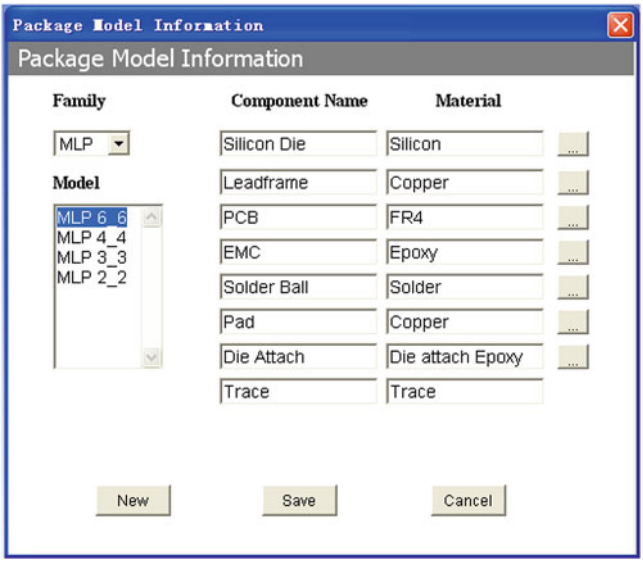


Fig. 11.33 Package CAD model information interface

communicate and select a model for analysis. Second, The Package Model Codesign CAD Library provides a model information interface for the user to manage the models' information, shown in Fig. 11.33. The interface classifies the solid CAD models by package families and requires the user to input models' names and select corresponding materials from Package Material Library. It is noted that the inputted names should be the same as the names defined in CAD software. As we can see, it will be especially convenient when the user wants to compare the results using different materials. The interface also allows the user to add, delete, or modify data. All the information is saved in a database which will be used in analysis process.

Wizard System is another core element of AutoSim, which contains the general procedure of moisture analysis for package models. The Wizard System has a user-friendly interface, it only requires the user to input the basic parameters. An example is to input the title of simulation and user name, load the solid models from Package Model Codesign CAD Library, and input the moisture condition. Because some simulations may be performed on quarter or half package models, the user can select the type of model. The Wizard System will collect all the information that the user inputs and perform the whole moisture simulation automatically according to the predefined procedure in background.

Figure 11.34 shows the general flowchart of AutoSim which is predefined in Wizard System for automated simulation. It builds the connection with other modules and realizes the automation of simulation on package models. The selected CAD model from Package Codesigned Model CAD Library is imported into DesignModeler and applied some operations, such as creating Name Selection (just as grouping geometry items into a component in classic ANSYS), forming

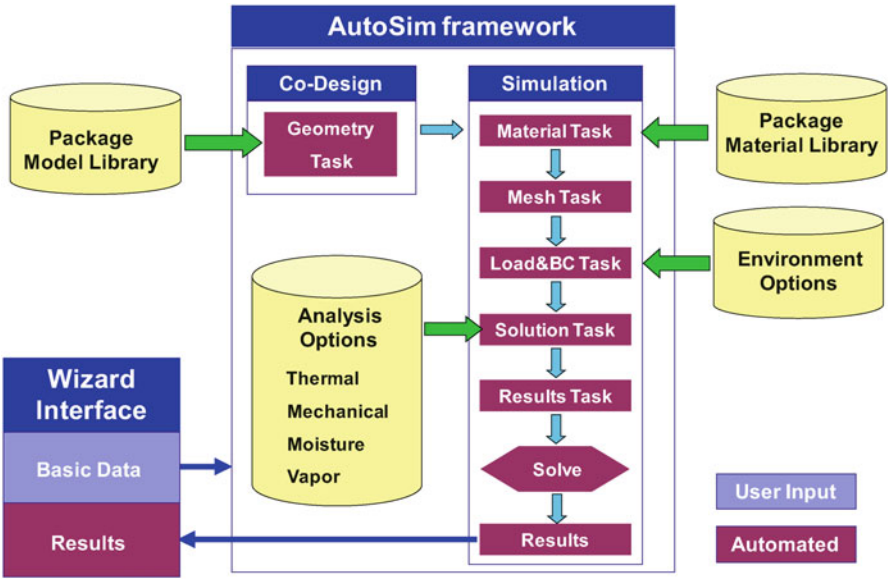


Fig. 11.34 Basic flowchart of AutoSim

new part (just as gluing in classic ANSYS), and so on. In fact, all these operations are prepared for meshing and loading in Design Simulation. Then the model is imported to Design Simulation from DesignModeler. Based on the definition in Package Model Information Interface, every component of model will be assigned to corresponding materials which come from the Package Material Library. An intelligent meshing function is implemented to generate high-quality mesh for highly accurate solutions. The boundary condition (like thermal or moisture) is automatically calculated and is applied to the package outside surface which are saved in Environment Options (or Library). Wizard System is automatically implemented for solving the model and saving the results based on the simulation/analysis option. The results may include contours of temperature and moisture distributions, vapor pressure distribution, thermal-mechanical CTE stress, hygroscopic stress, and various equivalent stresses. It is emphasized that the APDL commands are inserted in the Design Simulation and implementing path operations because these functions have not yet been developed by ANSYS Workbench.

One of the most important steps in simulation automation is to define appropriate material properties for package models to represent actual working conditions. There are various package materials whose parameters vary depending on manufacturing conditions. Furthermore, many material properties are temperature dependent and may require extraction from experimental inputs. For convenience to the user in creating and maintaining package material database, the Package Material Library is built based on Engineering Data Application of ANSYS Workbench.

Environment Options (or library) is the boundary conditions and loads database which is transferred by Wizard System in applying loads. It provides an interface

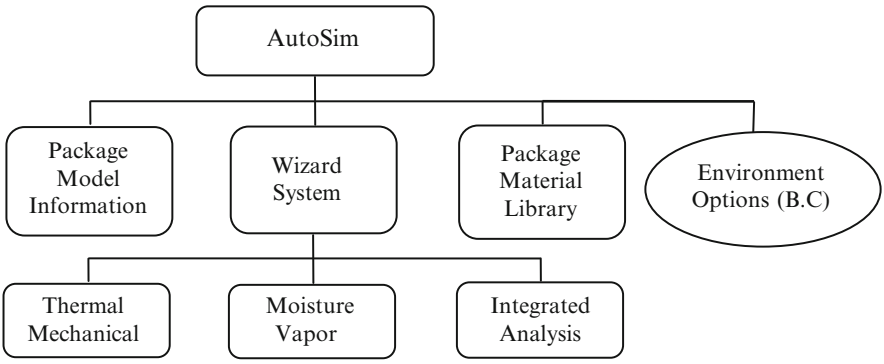


Fig. 11.35 Structure of AutoSim for thermal and moisture related analysis

for people to modify the boundary and loads of different components. It is especially convenient when the user wants to compare the results among different thermal or moisture boundary conditions.

For most engineers and designers, the documentation of analysis report is a very tedious task and time consuming. Therefore, Report Generation System of AutoSim is developed based on Report function of the Design Simulation module. It has the ability to capture engineering information and automatically produce complete engineering documentation in HTML, including words, tables, and color illustrations.

11.3.3.3 Structure of AutoSim in Thermal and Moisture Related Analysis

The above description is a general automation simulation system. Basically it can be applied to any problems. For a high efficient simulation automation system for thermal and moisture related analysis, it can be further developed in three modules: a Package Model Information Library, an Executable Wizard System with Exceed Spreadsheet, a Package Material Library and Environment Option. The user is only required to input basic data in a Wizard interface (an Excel Spreadsheet) and it will link to Workbench and automate the whole steps of moisture and vapor simulation. At last, the simulation results will also export into Wizard interface. Figure 11.35 shows the structure of AutoSim for thermal and moisture simulation.

The Wizard System is composed of three parts, which is used for thermal analysis, moisture analysis, vapor analysis and integrated analysis, respectively. The Wizard System for moisture analysis performs the simulation of moisture diffusions, hygroswelling, and vapor pressure analysis. Other Wizard systems are used to perform the thermal mechanical analysis and the combination analysis which includes the stress analysis of thermal-mechanical; hygromechanical; vapor induced equivalent thermal mismatch and the integrated analysis.

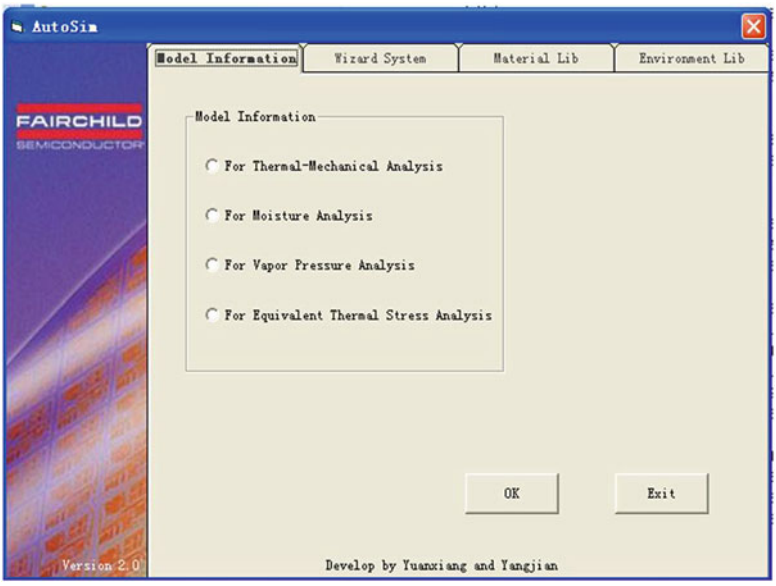


Fig. 11.36 Master interfaces of the AutoSim

Modules of Automated Simulation System

Figure 11.36 lists an interface window of the automated simulation system. At the main menu, there are four major functions: modeling information, wizard system, material library, and the environment library. Each of the function gives the related information for thermal and mechanical, moisture, vapor pressure and equivalent thermal stress.

The Package Model Information Library plays a very important role in the whole process of the analysis automatically. It is the core element of the automation analysis system and provides an interface for user to store and resume CAD models easily. In Fig. 11.9, the example interface shows package model information for equivalent thermal stress analysis. It will automatically show all component names which are defined in CAD software. Then, the user may select corresponding materials for every component from Package Material Library. All the information is saved in a database which will be transferred by Wizard System.

Wizard System is divided into four parts: Wizard System for thermal and CTE Mismatch Stress Analysis, Wizard System for Moisture Diffusion and Hygroswelling Analysis, Wizard System for Vapor Pressure Analysis, and Wizard System for Equivalent Thermal Stress Analysis. All the four parts have similar interfaces as the example in Fig. 11.37. The Wizard System uses Excel Spreadsheet as the user interface which requires the user to input the basic data. An example is to input user name, title of simulation, job name, working directory, and so on.

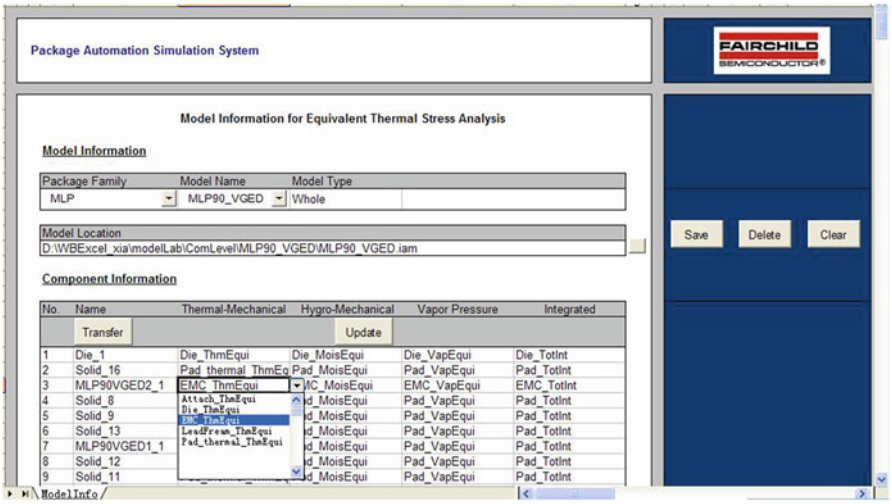


Fig. 11.37 Package model information interface for equivalent thermal stress

The user will also be required to select a model to be simulated, and then the model information stored in Package Model Information Library will be exported into Wizard interface. The Wizard System will collect all the information that the user inputs and perform the whole corresponding simulation automatically according to the predefined procedure in background.

Figure 11.38 gives the data review example of a group thermal coefficient of expansion (CTE) vs. temperature of the material library. Figure 11.39 lists the calculated equivalent CTE for hygroscopic swelling, vapor induced swelling, and the integrated total CTE for a linear analysis in the environment library.

11.3.4 Application of AutoSim

11.3.4.1 Thermal Simulation for an MLP Package

The AutoSim has been applied for the MLP family packages from Fairchild Semiconductor. In the following study, an MLP 6 × 6 quarter model is chosen for analysis, as shown in Fig. 11.40. The package mounted on a JEDEC PCB with equivalent trace is shown in Fig. 11.41. Table 11.9 shows the material properties of MLP 6 × 6 model, and Table 11.10 shows the thermal loads applied in analysis. Through the AutoSim Wizard system, the whole simulation process is highly efficient, and it requires about 10 min from beginning to the end of report for the MLP 6 × 6 package model with about 30,000 elements. While for a normal thermal simulation with postprocess and final report, it will take about 1 day if it is done manually. Figure 11.42 compares the contour of temperature between

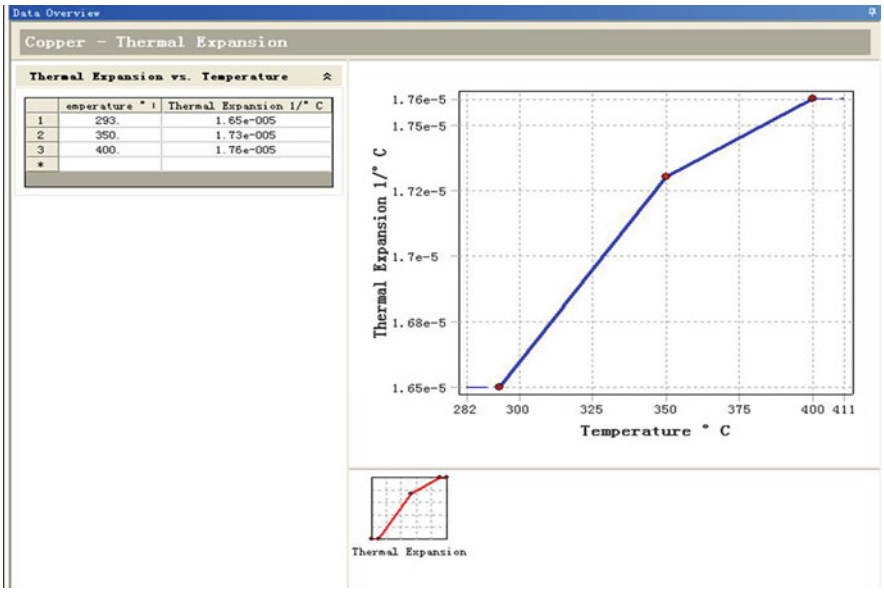


Fig. 11.38 Data review example of material library

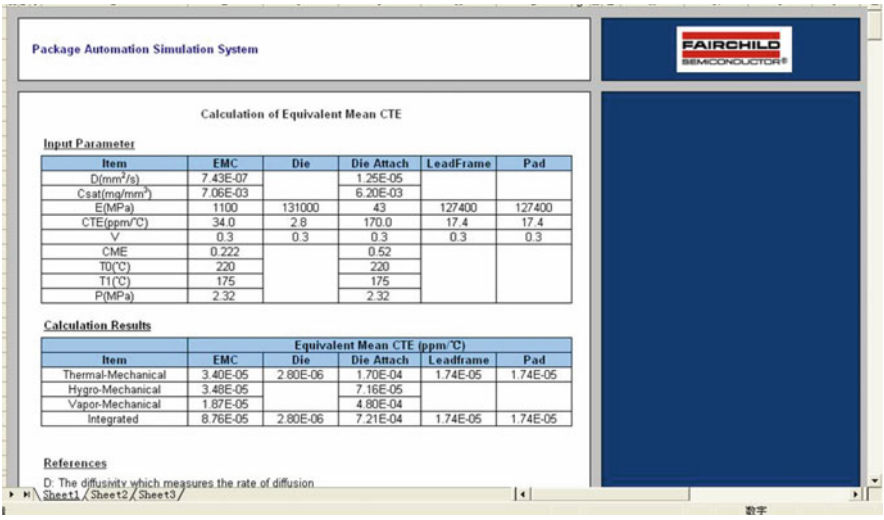


Fig. 11.39 Data review and check of equivalent coefficient of thermal expansion (CTE) of environment library

classic ANSYS and AutoSim. Table 11.11 compares various thermal resistances between ANSYS and AutoSim. It can be found that the results are almost the same. It is within expected tolerances across manufacturing lots.

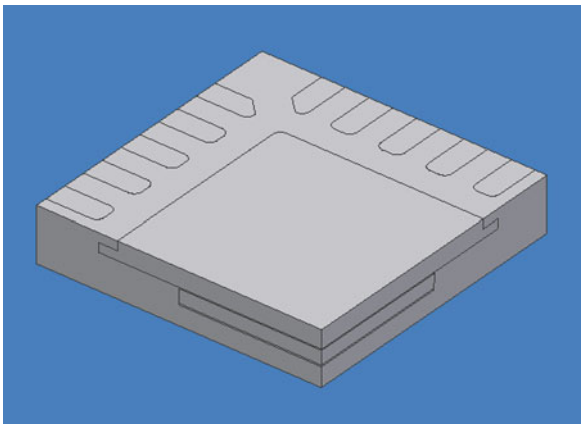


Fig. 11.40 A molded leadless package (MLP) 6 × 6 quarter mode

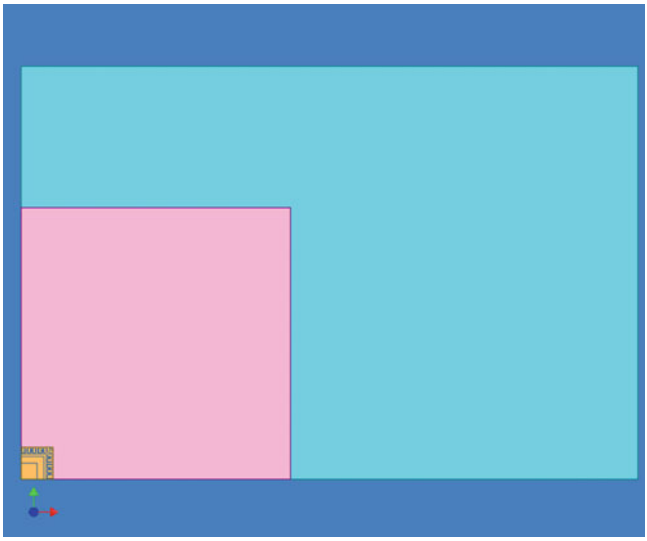


Fig. 11.41 MLP 6 × 6 model mounted on a PCB with equivalent trace

Table 11.9 Material properties of MLP 6 × 6

Material	Thermal conductivity (W/m °C)
Silicon die	145
Mold compound	0.88
Die attach epoxy	3.80
Lead frame	261.0
Pad	0.26
Solder	50.6
Trace	115.8
FR4 of PCB	0.35

Table 11.10 Thermal loads

Item	Content
Power dissipation	0.5 W
Ambient temperature	25°C
Convection	Natural

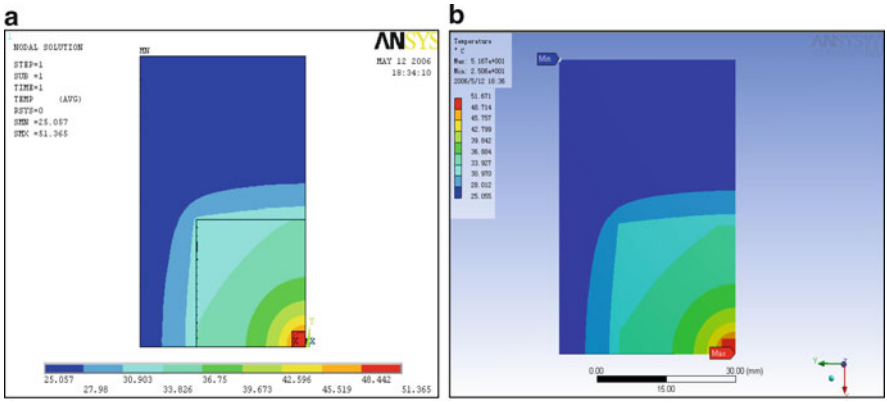


Fig. 11.42 Temperature contour in ANSYS and AutoSim. (**a**) Result in classic ANSYS. (**b**) Result in AutoSim

Table 11.11 Thermal simulation comparison in ANSYS and AutoSim

	T_J (°C)	T_T (°C)	T_C (°C)	θ_{JA} (°C/W)	ψ_{JT} (°C/W)	ψ_{JC} (°C/W)
ANSYS	51.42	51.33	51.23	52.84	0.18	0.38
AutoSim	51.66	51.58	51.48	53.33	0.16	0.37

11.3.4.2 Moisture Diffusion Analysis for an MLP Package

Moisture Diffusion

The moisture properties, i.e., diffusivity and C_{sat}, characterized under 85°C/85% RH, are listed in Table 11.8 [8].

Figure 11.43 shows the comparisons of the moisture wetness distribution between ANSYS-Multiphysics and the AutoSim. From Fig. 11.43, it can be seen that the results agree well with each other. AutoSim is fully automatic to obtain the results.

Figure 11.44 compares the hygroscopic deformation and von Mises stress between ANSYS-Multiphysics and AutoSim. Table 11.12 lists the maximum von Mises stress and the total deformation values of the two methods. Form Fig. 11.44 and Table 11.12, the maximum values at corresponding locations obtained from AutoSim agree with the ANSYS-Multiphysics.

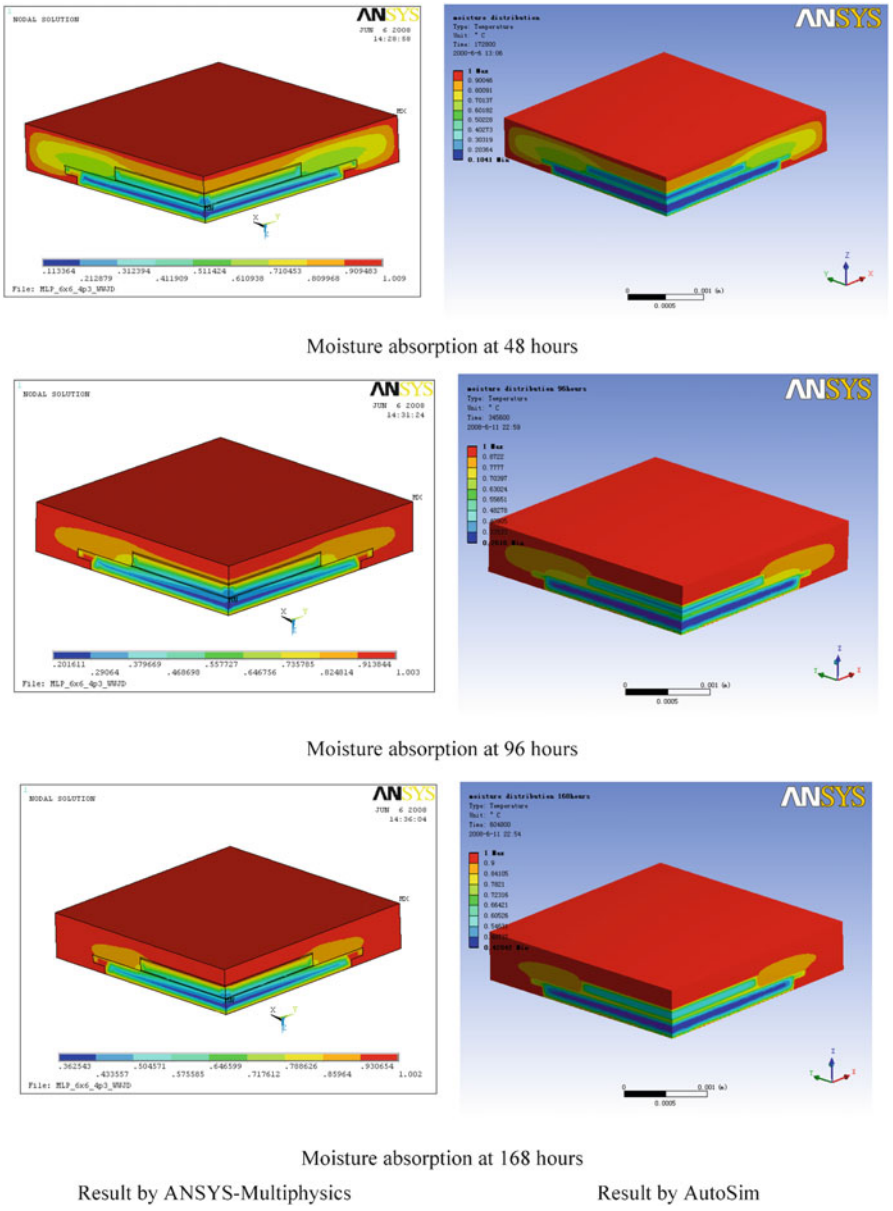
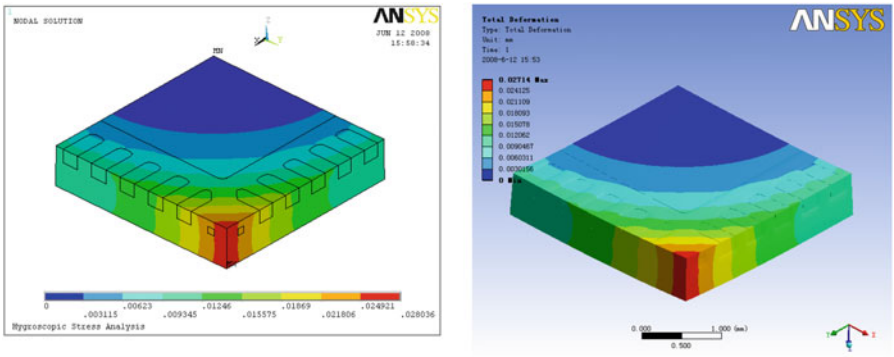


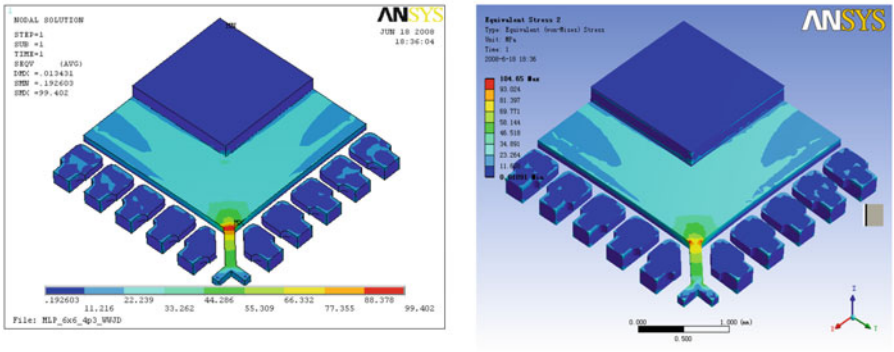
Fig. 11.43 Comparison of moisture distributions between ANSYS-Multiphysics and AutoSim

Vapor Pressure Simulation

Figure 11.45 shows the comparison of the vapor pressure distribution at reflow between the AutoSim and ANSYS-Multiphysics. From Fig. 11.45, we can see that the results match well each other. At reflow temperature 220°C, the saturated vapor



Hygroscopic deformation



Hygroscopic Von Mises stress

Result in ANSYS-Multiphysics Result in AutoSim

Fig. 11.44 Comparison of hygroscopic deformation and von Mises stress

Table 11.12 Hygroscopic stress results by ANSYS-Multiphysics and AutoSim

	Maximum von Mises stress (MPa)	Maximum total deformation (mm)
ANSYS-Multiphysics	99.402	0.02836
AutoSim	104.65	0.02714

pressure is 2.32 MPa. If the moisture is not fully vaporized at reflow, the vapor pressure will maintain the saturated value no matter how much moisture is absorbed.

Integrated Stress Modeling

In the following, the package stress-free temperature is at curing temperature of EMC, which is 175°C. The temperature is raised to a reflow temperature (220°C) is

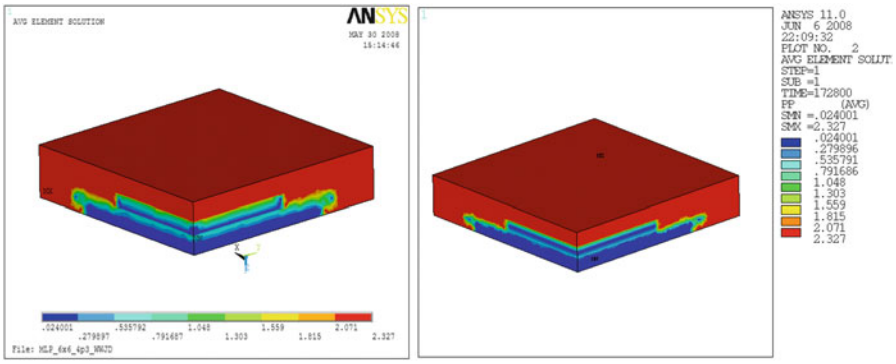


Fig. 11.45 Comparison of vapor pressure distribution at reflow temperature

Table 11.13 Thermomechanical material properties (220°C)

	E (MPa)	CTE (ppm/°C)	*v*
EMC	1,100	34	0.3
Die	131,000	2.8	0.3
Die attach	43	170	0.3
Lead frame	127,400	17.4	0.3
Pad	127,400	17.4	0.3

from 175°C. The thermomechanical material properties used in the modeling are shown in Table 11.13 [8].

Figure 11.46 compares the integrated deformation and von Mises stress induced by hygroscopic and thermal-mechanical loads between the AutoSim and ANSYS-Multiphysics. Table 11.14 lists the maximum hygrothermal-mechanical von Mises stress and total deformation values of the two methods.

The total strains induced by hygroscopic and thermomechanical loads and vapor pressure in mold compound and die attach are listed in Table 11.15. For hygroscopic strain and vapor pressure induced strain, they are converted into the equivalent CTEs with a temperature from curing temperature 175°C to reflow temperature 220°C so that all three modes (hygroscopic, thermal-mechanical, and vapor pressure) can be integrated in an equivalent thermomechanical system. The total equivalent CTE is much larger than any individual contribution. So the thermal, hygroscopic, and vapor pressure induced stresses are integrated, to allow realistic stress analysis for prediction of damage and failure.

Figure 11.47 compares the deformation and stress induced by vapor pressure only. Table 11.16 compares the corresponding maximum values based on the two methods.

Figure 11.48 compares the integrated contours of total deformation and von Mises stress under thermal, hygroscopic and vapor pressure loads between ANSYS-Multiphysics and AutoSim. Table 11.17 compares the integrated total results

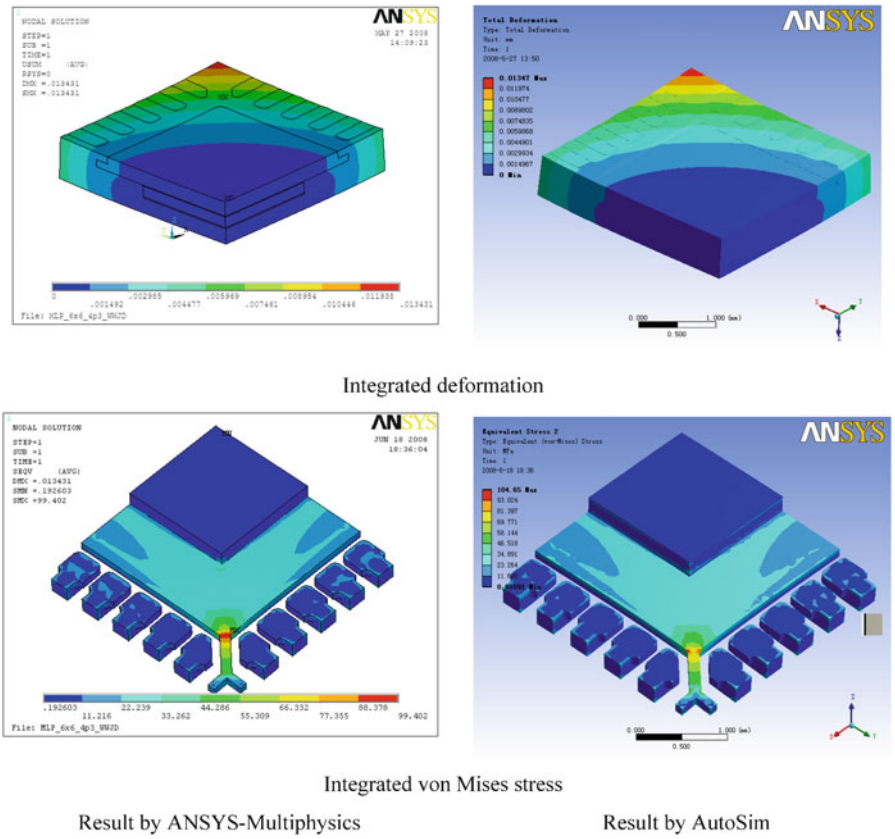


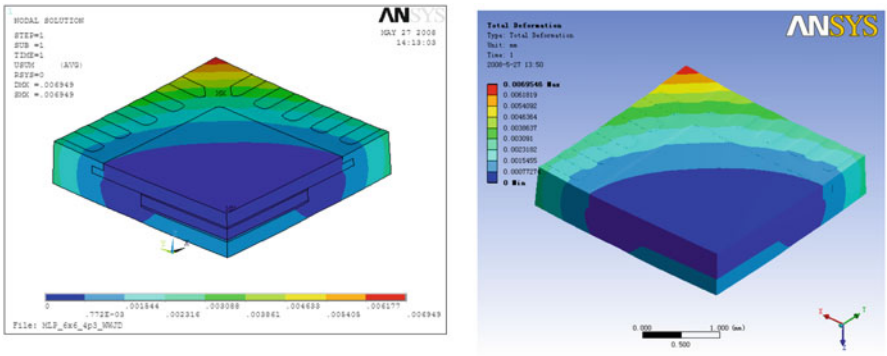
Fig. 11.46 Comparison of integrated hygroscopic and thermal-mechanical deformation and stress

Table 11.14 Integrated hygroscopic and thermal-mechanical results in ANSYS-Multiphysics and AutoSim

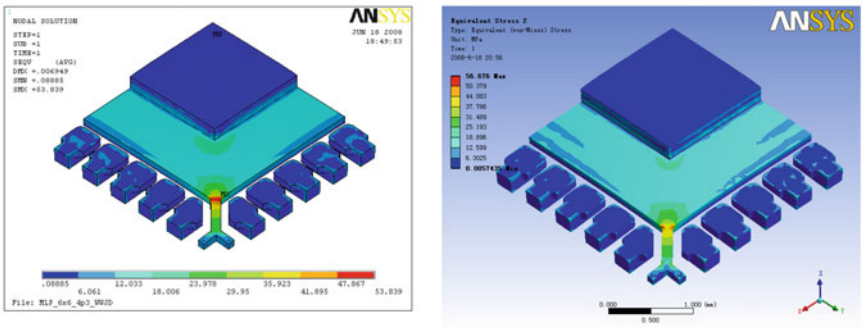
	Maximum von Mises stress (MPa)	Maximum total deformation (mm)
ANSYS-Multiphysics	99.402	0.013431
AutoSim	104.65	0.013470

Table 11.15 Total strain and equivalent CTE in simulation of ANSYS-Multiphysics and AutoSim

	EMC		Die attach	
	Total strain	Equivalent CTE (ppm/°C)	Total strain	Equivalent CTE (ppm/°C)
Thermomechanical	1.53E−03	34	7.65E−03	170
Hygroscopic	1.57E−03	34.8	3.22E−03	71.6
Vapor pressure	8.44E−04	18.7	2.16E−02	480
Integrated (total)	3.94E−03	87.5	3.25E−02	721.6



Vapor pressure induced deformation



Vapor pressure induced von Mises stress

Result by ANSYS-Multiphysics Result by AutoSim

Fig. 11.47 Comparison of vapor pressure induced deformation and stress

Table 11.16 Vapor pressure induced equivalent stress results in ANSYS-Multiphysics and AutoSim

	Maximum von Mises stress (MPa)	Maximum total deformation (mm)
ANSYS-Multiphysics	53.839	0.006949
AutoSim	56.676	0.006954

between ANSYS-Multiphysics and AutoSim. Both total deformation results agree very well.

11.3.4.3 Material Parameter Examination

One advantage of the AutoSim is to run the parameter design of experiment (DoE) very efficiently. Table 11.18 lists 16 legs to study the effect of EMC properties.

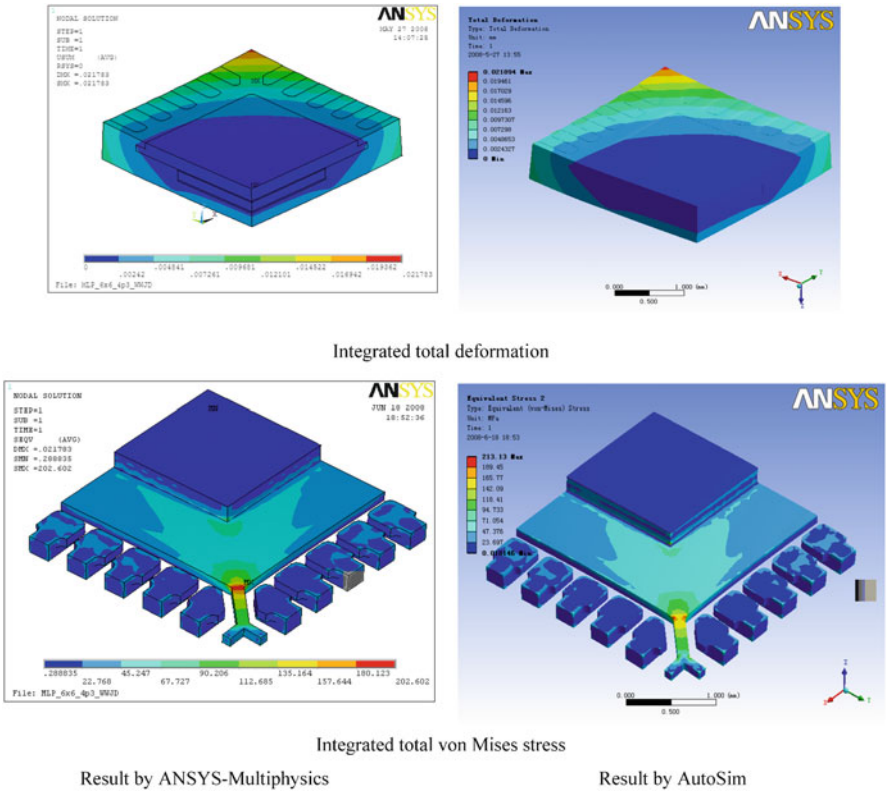


Fig. 11.48 Comparison of integrated deformation and stress induced by hygroscopic, thermal-mechanical, and vapor pressure

Table 11.17 Integrated hygroscopic, thermal-mechanical, and vapor pressure results in ANSYS-Multiphysics and AutoSim

	Maximum von Mises stress (MPa)	Maximum total deformation (mm)
ANSYS-Multiphysics	202.602	0.021783
AutoSim	213.13	0.021894

In addition, die size is also considered as one factor listed in Table 11.18. The purpose of the DoE study is to find out the rank of the legs. Therefore, the simulation results will be used to guide the package design engineers to select the best EMC material in early design phase.

Figure 11.49 gives the integrated von Mises stress DoE results through the moisture simulation automation system. The DoE simulation has given the rank of von Mises stress level in the molding compound at reflow. In each case, the maximum stress appears at the corner interface among the molding compound, die

Table 11.18 Material parameter DoE arrangement

EMC						Die
No.	Leg	T_g	CTE	E (MPa)	Solubility	Die size
1	−−−+−	110	40	500	0.0085	3 × 3 × 0.152
2	−++−+	110	60	800	0.0045	4 × 4 × 0.152
3	−+−++	110	60	500	0.0085	4 × 4 × 0.152
4	+++++	150	60	800	0.0085	4 × 4 × 0.152
5	−+++−	110	60	800	0.0085	3 × 3 × 0.152
6	+−−−−	150	40	500	0.0045	3 × 3 × 0.152
7	−−+−−	110	40	800	0.0045	3 × 3 × 0.152
8	−−−−+	110	40	500	0.0045	4 × 4 × 0.152
9	+−++−	150	40	800	0.0085	3 × 3 × 0.152
10	++−+−	150	60	500	0.0085	3 × 3 × 0.152
11	−+−−−	110	60	500	0.0045	3 × 3 × 0.152
12	−−+++	110	40	800	0.0085	4 × 4 × 0.152
13	+++−−	150	60	800	0.0045	3 × 3 × 0.152
14	++−−+	150	60	500	0.0045	4 × 4 × 0.152
15	+−−++	150	40	500	0.0085	4 × 4 × 0.152
16	+−+−+	150	40	800	0.0045	4 × 4 × 0.152

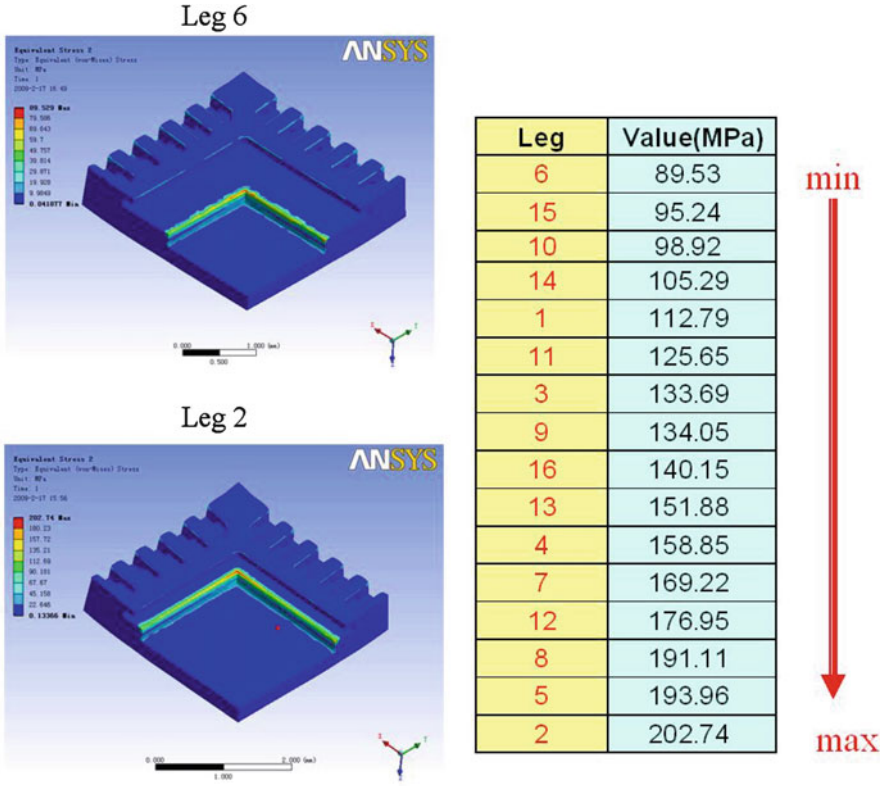


Fig. 11.49 DoE simulation results of integrated von Mises stress

attaching and the die. The Leg 6 with smaller Young's modulus, Higher T_g, smaller CTE, lower solubility, and smaller die size has the lowest von Mises stress, while the Leg 2 with larger Young's modulus, lower T_g, larger CTE, and larger die size gets the highest von Mises stress. This would be helpful information for IC package designer to find the Leg 6 with best material parameters among the 16 DoE legs.

11.4 Summary

This chapter introduces the thermal modeling and its correlation of the power package, the parameter thermal simulation for power WL-CSP, and the development of a codesign automated simulation system, AutoSim, for the analysis of thermal, moisture diffusion, vapor pressure distribution, thermal stress, hygroscopic stress, vapor pressure induced stress, and the integrated equivalent stress for microelectronic package. In the thermal modeling of the power package, it gives the basic methodology for thermal resistance analysis, the empirical heat transfer coefficient and the correlation with the thermal resistance test. The parameter simulation of the WL-CSP gives the automated thermal simulation procedure based on ANSYS APDL code. It includes parametric WL-CSP and its adaptive parametric JEDEC thermal test board. By employment of the parametric model, package geometry parameters can be set freely, and also trace layout for PCB will accordingly change to meet the requirement of package, so that the influence of all geometry parameters to thermal performance can be easily investigated for whole series of WL-CSP packages. The entire thermal simulation, including meshing, loading/boundary condition, solving, and postprocessing, is automated with ANSYS APDL coding. The automated simulation system includes five modules: a Package Model Codesign CAD Library, an Executable Wizard System, a Package Material Library, an Environment Options (or Library), and a Report Generation System. This allows users to select the geometry models from CAD Library in codesign communication, then perform various moisture related analysis automatically. It is especially helpful for engineers who do not know FEA and moisture theories to run the simulation easily by using this system for codesign simulation automation. The automated simulation system has been applied for thermal and moisture diffusion and related stress analysis of an MLP package. A design of experiment (DoE) simulation for EMC material examination has been carried out and discussed by using the AutoSim. The simulated results from the AutoSim agree well with the results by using ANSYS-Multiphysics. It should be noted in some stress simulation case, there is small difference (within 5%) between ANSYS-Multiphysics and the AutoSim due to the possible different meshes, solvers and current limitation of workbench tool itself. However, the methodology developed in this section provides a high-efficiency solution for package designers, reliability and test engineers who do not have modeling and the moisture physics background, to find the optimized result much faster than regular method. This may extremely save the design cycle time and the cost for new package product development.

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Chapter 12
Power Package Electrical and Multiple Physics Simulation

The electrical performance (such as electrical resistance, inductance, and fusing current capability) is a key factor for a power electronic product. Many studies, such as the electrical performance of different devices, effect of assembly reflow process on electrical properties and the resistance of a solder joint, have been done to improve a product's electrical performance [1–4]. In recent years, the investigation has been started for the electrical conductivity under the mechanical deformation of a device [5]. Package design optimization for electrical performance of a power module by using finite element analysis (FEA) [6] has also been presented. Studying the impact of the defect on package electrical performance, especially for the parasitic effect, is very important. It can help to understand the potential root causes and failure mechanisms, as well as to ensure that the electrical performance meets the requirement of product by optimizing the package design and assembly process.

12.1 Power Package Electrical Simulation

This section introduces the power electrical packaging modeling for extracting the self and mutual inductance, resistance and capacitor from a 3D model of an IC package using ANSYS® Multiphysics. Results are to be used to generate an electrical model of the package for use in SPICE simulation.

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12.1.1 Extracting the Inductance and Resistance

12.1.1.1 Theory Background

At alternating current (AC), the characteristic impedance can be represented by the real component "resistance" and imaginary component "reactance" [1]

$$Z_0 = R + jX \tag{12.1}$$

where R and X can be described using AC voltages and currents

$$R = \frac{V_{\text{real}} \cdot I_{\text{real}} + V_{\text{imag}} \cdot I_{\text{imag}}}{I_{\text{real}}^2 + I_{\text{imag}}^2} \tag{12.2}$$

$$X = \frac{V_{\text{imag}} \cdot I_{\text{real}} - V_{\text{real}} \cdot I_{\text{imag}}}{I_{\text{real}}^2 + I_{\text{imag}}^2} \tag{12.3}$$

Inductance can be derived from reactance as long as the frequency is known

$$L = \frac{X_{\text{L}}}{2\pi f} \tag{12.4}$$

Mutual reactance can be solved by

$$X_{ab} = \frac{V_{b_{\text{imag}}} \cdot I_{a_{\text{real}}} - V_{b_{\text{real}}} \cdot I_{a_{\text{imag}}}}{I_{a_{\text{real}}}^2 + I_{a_{\text{imag}}}^2} \tag{12.5}$$

Mutual inductance can be obtained from mutual reactance

$$L_{ab} = \frac{X_{ab}}{2\pi f} \tag{12.6}$$

Coupling factors can be derived based on the self and mutual inductance

$$K_{ij} = \frac{L_{ij}}{\sqrt{L_{ii} \cdot L_{jj}}} \tag{12.7}$$

Note: if $K_{ij} < 10\%$, the mutual inductance L_{ij} could be neglected.

12.1.1.2 Simulation Procedure

The unit of power electrical simulation is base d: MKS system. A detailed drawing of a power package should include lead frame and bond wires. DAP, EMC (epoxy mold compound), die, and die attach layer can be omitted for simplicity

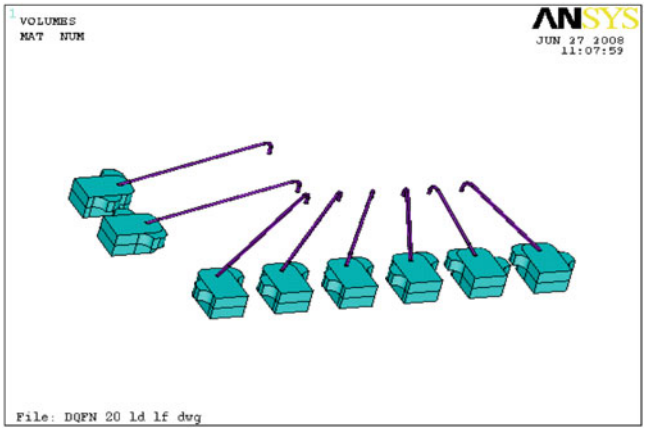


Fig. 12.1 A symmetric model of pin and wires layout of DQFN

without losing much accuracy. The CAD geometry structural dimensions must be accurate in every detail. Check the drawing to insure that there is no tiny dimensional errors from the CAD import. All the components in the package system must be in perfect connection without initial defects. For the material data requirements, it includes resistivity and relative permeability. The 3D Element is selected with Solid97: 3D 8-node magnetic solid and infin111: 3D infinite boundary element. In the following simulation procedure, we use a power package DQFN with 20 leads as an example.

1. Define the element type
2. Define the material property data
3. Define the harmonic analysis: ANTYPE, 3
4. Generate/import the solid model of the package
   For low pin count power package, the full model would be the best solution. However, for high ping count package, it is necessary to take the advantage of symmetry to simplify model and save time. In this case only eight pins and eight bond wires are built for the solid model due to the symmetry, as shown in Fig. 12.1. The relative permeability of lead frame, EMC, air and infinite boundary has the same value "1." So the DAP, die, die attach, and EMC can be replaced by air. The resistance, R_i, self-inductance L_{ii}, mutual inductance $L_{i,i+1}$ and $L_{i,i+2}$ are variable required to calculate.

   The total L/R of pin and bond wire in the simulation of this section can be considered as the sum of L/R of pin and L/R of bond wire. Therefore, another method to extract the L/R is to calculate the L/R of pin and bond wire individually and then sum them up. For extraction of L/R of pins, the solid model only consists of the pins and no bond wires. For extraction of L/R of bond wires, it can be estimated using some experienced and simplified formula.

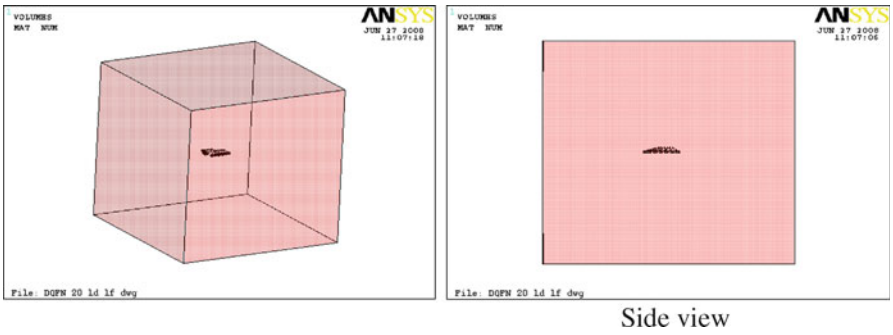


Fig. 12.2 The air volume around the conductors and insulators in package

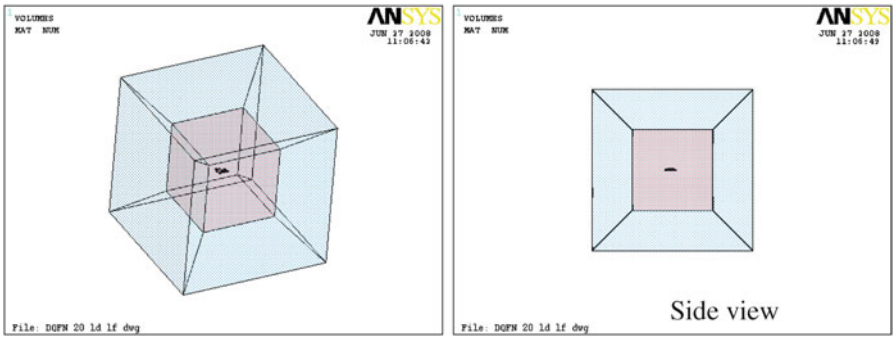


Fig. 12.3 Infinite boundary

5. Add air volume around conductors and insulators
   The "air" volume refers to any nonconductive material having a relative permeability of "1." This can include the package mold compound, substrate, underfill, die, and air. The length, width, and height of the air volume should be 3–5 times greater than the length, width, and height of the package as shown in Fig. 12.2. This will allow room for the mesh to transition from swept brick to tetrahedral.
6. Add infinite boundary to external surfaces of air using mitered volumes
   Around the air volume, there is an external dimension of the infinite boundary which should be 2 times the air volume (see Fig. 12.3).
7. Create a mesh
   Try to mesh the conductors with hex/wedge shapes using the sweep operation. If the geometry of the conductors will not allow for this a free tetrahedral mesh can be used. The meshing for the conductors and air volume is shown in Fig. 12.4.

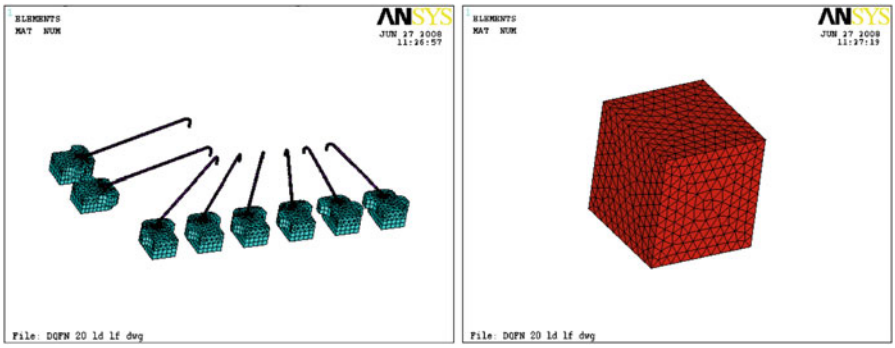


Fig. 12.4 Meshing for conductors and air volume

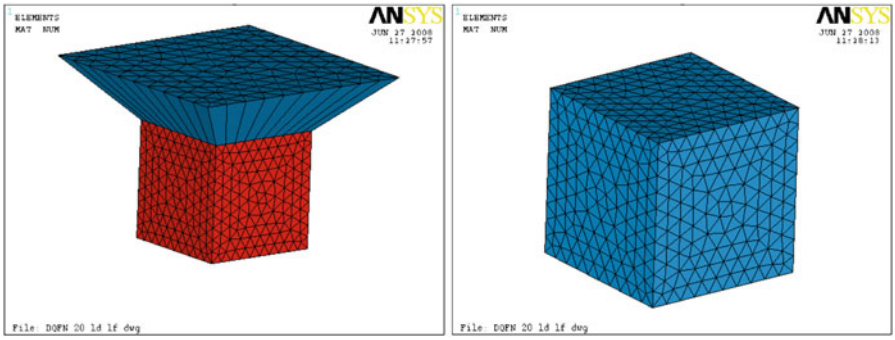


Fig. 12.5 Meshing for infinite boundary

For each of the six mitered infinite boundary volumes, generate the mesh by extruding a prism mesh from the air volume. For infinite boundary, only one layer of elements is required. See the meshing result in Fig. 12.5.

8. Apply the electrical boundary condition
   Apply the 0 V loads to one end of conductors. Loads can be applied to areas or nodes at the wire ends that locate at the die surface as shown in Fig. 12.6. Couple the opposite ends of the conductor (leads) with volt degree of freedom (DOF), in which the current load can be applied. The coupled set number should coincide with the package pin number, see Fig. 12.7.
9. Apply the infinite boundary flags to the six exterior areas
   The infinite boundary flags to the six exterior areas are set as in Fig. 12.8.
10. Set frequency for analysis
    Extraction can be performed at various frequencies including performing a frequency "sweep" to extract *R* and/or *L* vs. frequency. By default the analysis frequency has been set to 1 Hz to extract the static inductance and resistance. For high frequency analysis, it can be set to 1 MHz or higher.

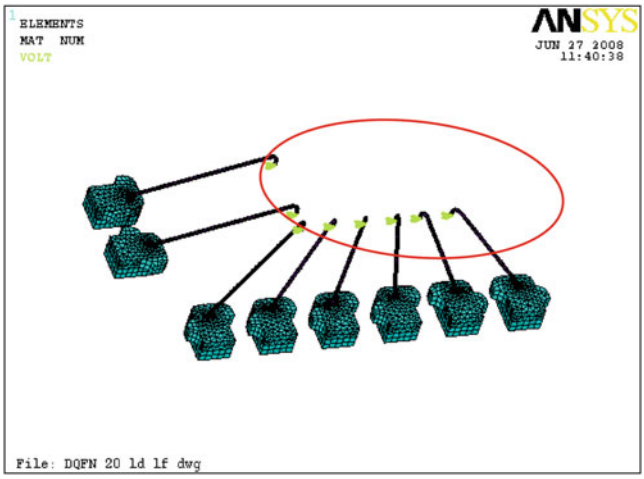


Fig. 12.6 Apply the 0 V loads on one end of conductor

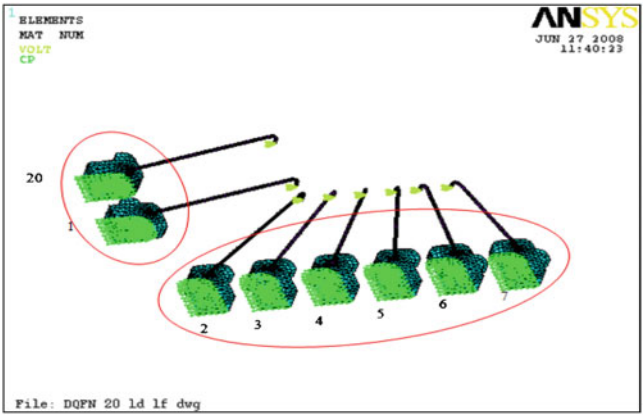


Fig. 12.7 Couple the other end of the conductor with volt DOF

11. Run the simulation and review the result
    Simulation may be run through the interface of the ANSYS software or may be run through a macro that assigns the current load, run the magnetic solution, and perform the inductance and resistance calculation. The after the simulation is finished, check the result. In ANSYS, you can run *STAT to show the result.

    Sometimes we may get negative mutual inductance. The negative values are valid and just mean that the current in the path is flowing in opposite directions. When we build the Spice model each of the inductors has a pin#1 and pin#2. The polarity of the inductors, when there is a negative coupling factor, should be reversed.

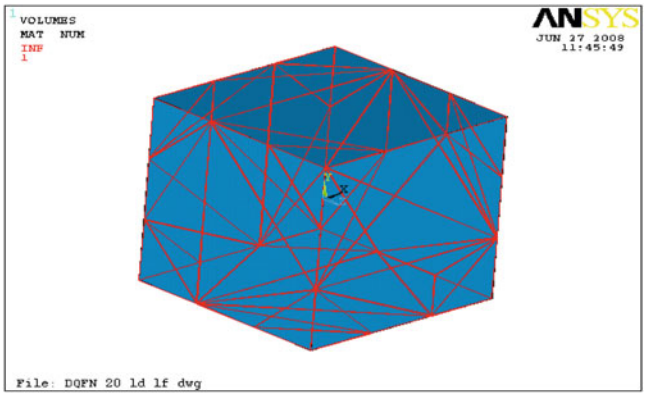


Fig. 12.8 Infinite boundary flags on six exterior surfaces

Table 12.1 Checklist of simulation for the inductance and resistance

Inductance and resistance extraction checklist
Obtain detailed drawing with all required dimensions
Obtain permeability and resistivity of materials
Define element type
Drawing imported/generated in ANSYS with no errors
All drawing and material property units converted to MKS
Conduct proper Booleans operation to all the volumes
Conductors checked and optimized for meshing
"Air" volume added
Infinite boundary volumes added
Element and material attributes assigned to all volumes
Conductors meshed with no errors
0 V applied to one terminal of each conductor
Opposite terminal of each conductor coupled with volt DOF
Air volume meshed with no errors
Mesh extruded to infinite boundary volumes with no errors

12.1.1.3 Checklist of the Simulation

To make sure following the correct procedure, a checklist is shown in Table 12.1.

12.1.1.4 Skin Effect

The skin effect is the tendency of an AC to distribute itself within a conductor so that the current density near the surface of the conductor is greater than that at its core. That is, the electric current tends to flow at the "skin" of the conductor. The skin effect causes the effective resistance of the conductor to increase with the frequency of the current. Skin effect is due to eddy currents set up by the AC

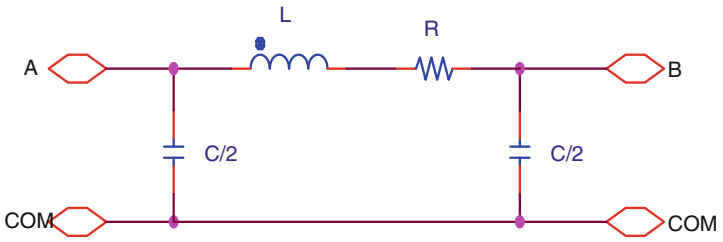


Fig. 12.9 CLC circuit element

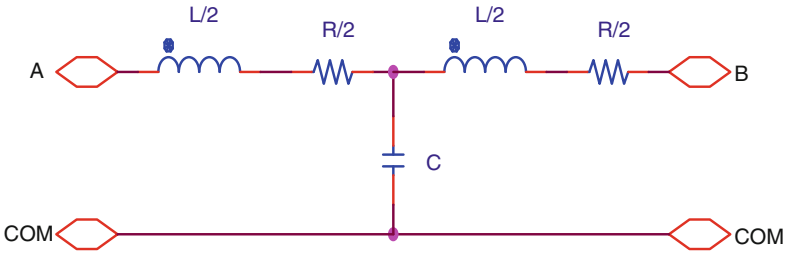


Fig. 12.10 LCL circuit element

current. The skin effect has practical consequences in the design of radio-frequency and microwave circuits and to some extent in AC electrical power transmission and distribution systems. Also, it is of considerable importance when designing discharge tube circuits.

If the analysis is to be performed at high frequency, the skin depth of the conductors must be considered prior to meshing. To properly model the skin effect, the maximum element spacing should be equal to or less than one half of the skin depth.

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \tag{12.8}$$

δ = skin depth in meters, ρ = resistivity in Ωm, f = frequency in Hertz, and μ = absolute permeability in Henries/meter, $\mu = \mu_0 \cdot \mu_r$, μ_0 is the permeability of free space ($4\pi \times 10^{-7}$ N/A2) and μ_r is the relative permeability.

12.1.1.5 Spectre Netlist Generation

The extracted inductance, resistance, and capacitance will be used to generate the Spice model including a Spectre netlist and a Cadence symbol.

When modeling a conductor there are two common structures that are used. They are referred to as LCL and CLC. We use the CLC structure because it results in fewer total components in the netlist (see Figs. 12.9 and 12.10).

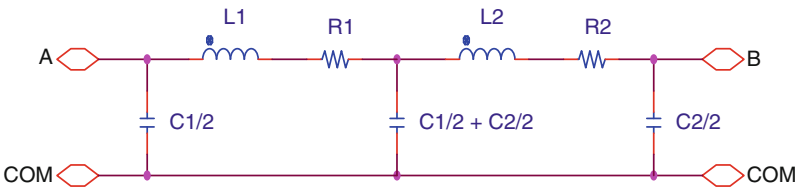


Fig. 12.11 Two CLC circuit element

For high frequency modeling we can divide a conductor into several CLC elements as shown in Fig. 12.11 for two CLC elements. Sometimes the elements are the same and sometimes they will change as the characteristic impedance of the conductor changes with respect to the propagation velocity of the signal.

12.1.2 Methodology for Extracting Capacitance

A capacitor is a device for storing charge. It is usually made up of two plates separated by a thin insulating material known as the dielectric. The capacitance is a measure of the amount of charge a capacitor can store; this is determined by the capacitor geometry and by the kind of dielectric between the plates. For a parallel plate capacitor made up of two plates of area A and separated by a distance d, and dielectric material with dielectric constant k, the capacitance is given by $C = k\varepsilon_0 A/d$, where ε_0 is free space permittivity.

12.1.2.1 Simulation Procedure

To extract capacitance, an h-method electrostatic analysis will be used. The CMATRIX command will be used to solve the analysis and extract the lumped capacitance matrix. The unit used in this section is uMKS (capacitance in pF, length in μm). A detailed drawing of the package includes leads, DAP, and EMC. Bond wires, die and die attach layer can be omitted for simplicity without losing much accuracy. The CAD geometry structural dimensions must be accurate in every detail. Check the drawing to insure that there is no tiny dimensional errors from the CAD import. All the components in the PKG system must be in perfect connection without initial defects. Material data requirements: Dielectric constant k, i.e., the relative permittivity of all the materials is needed. The 3D element is selected to be: Solid122: 3D 20-Node Electrostatic Solid, Solid123: 3D 10-Node Tetrahedral Electrostatic Solid and the Infin111: 3D infinite boundary element. The simulation procedure uses the DQFN 20L package as an example for extracting the capacitance.

1. Define the element type
2. Set the electromagnetic units to microns and picofarads
3. Define the material property data

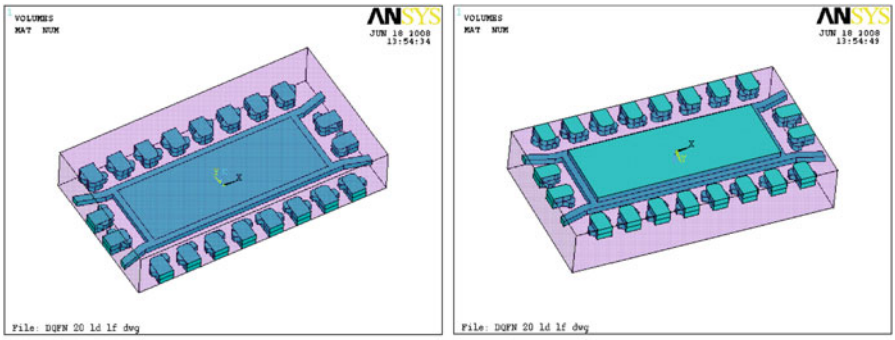


Fig. 12.12 The 3D model for capacitor

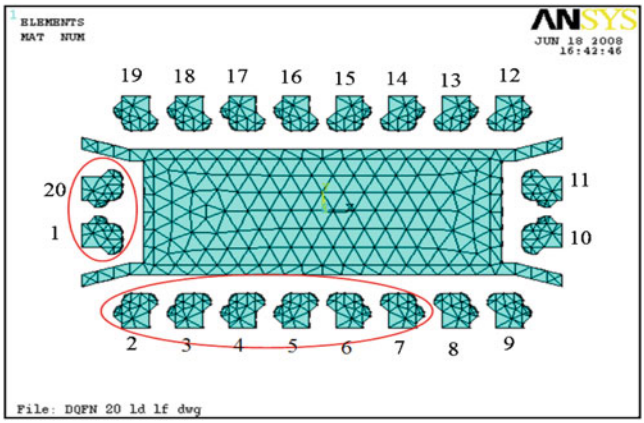


Fig. 12.13 Symmetry of the model

4. Generate/import the solid model of the package
   The 3D model is shown in Fig. 12.12. Take advantage of symmetry to simplify model, see Fig. 12.13. The self capacitance is C_{ii}, mutual capacitance is $C_{i,i+1}$ and $C_{i,i+2}$.
5. Generate the test board
   The test board locates below the bottom of the package leads with a thickness of 152 μm (JEDEC EIA/JEP 126) as shown in Fig. 12.14.
6. Add air volume around conductors and insulators
   The length, width, and height of the air volume should be 3–5 times greater than the length, width, and height of the package (see Fig. 12.15).
7. Add infinite boundary to external surfaces of air using mitered volumes
   External dimensions of the infinite boundary should be two times greater than the air volume, see Fig. 12.16.

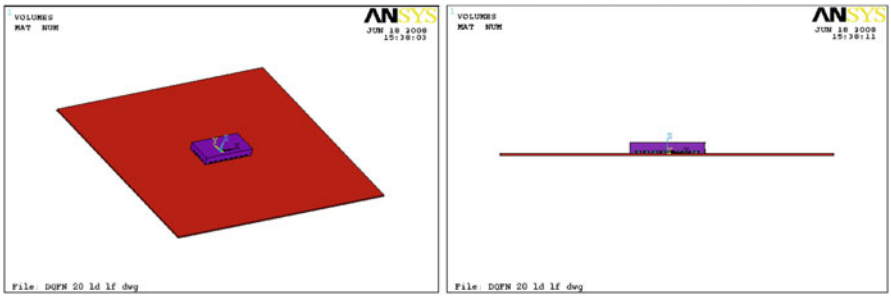


Fig. 12.14 The test board locates below the bottom of the package leads with a thickness of 152 μm (JEDEC EIA/JEP 126)

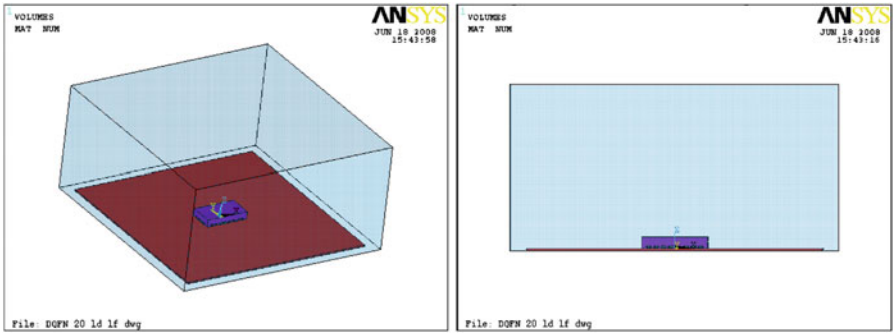


Fig. 12.15 Add air volume around the conductors and insulators of the package

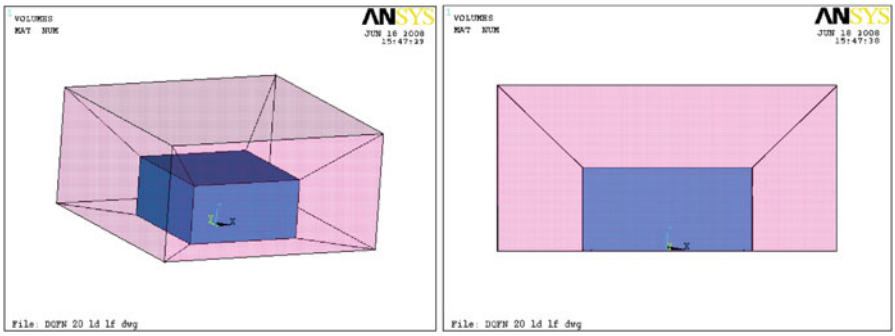


Fig. 12.16 Infinite boundary around the external surfaces of air volume

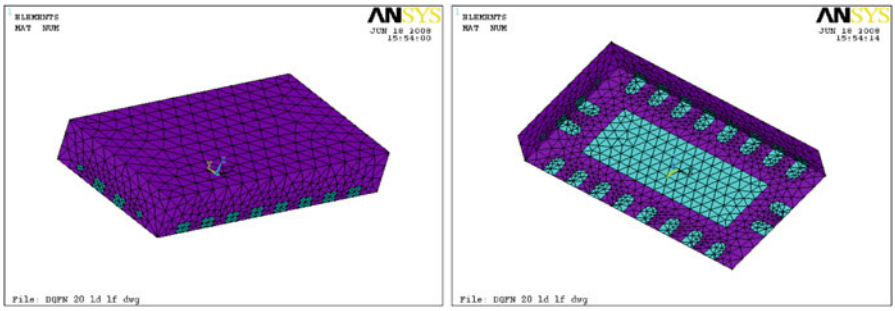


Fig. 12.17 Package mesh for capacitor model

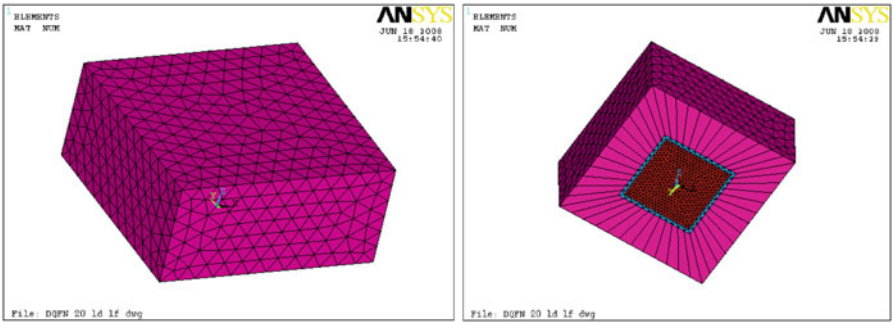


Fig. 12.18 Infinite boundary mesh for capacitor

8. Mesh generation
   Use free tet mesh for all volume except infinite boundary (Fig. 12.17) and a sweep mesh with hex/wedge for the infinite boundary (Fig. 12.18). There is no need to mesh the conductors. But we usually do mesh them because this helps when defining the components. For infinite boundary, only one layer of elements is required.
9. Create components from the conductors
   Select all of the elements associated with that volume and select the nodes associated with the elements using the EXT (external) option in ANSYS. Create a component using the NODE option with the name "cond1." Repeat for each pin and use the package pin# with the "cond" prefix as the component name in each case, as shown in Fig. 12.19.

   For the ground plane, select the nodes attached to the bottom surface area of the PCB and those external nodes of DAP, create a component using those nodes. This component must be assigned the greatest value (an example is

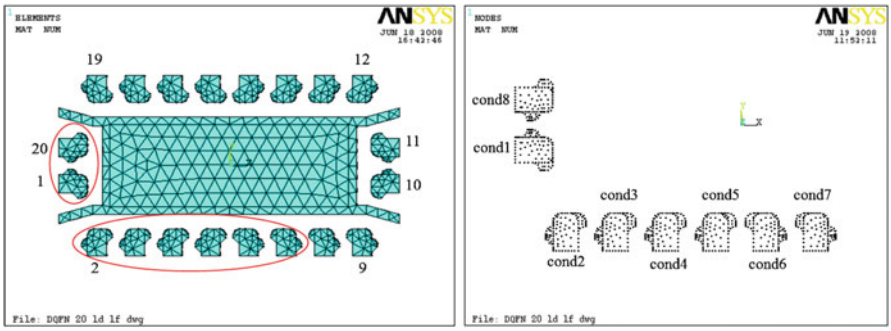


Fig. 12.19 Create the components

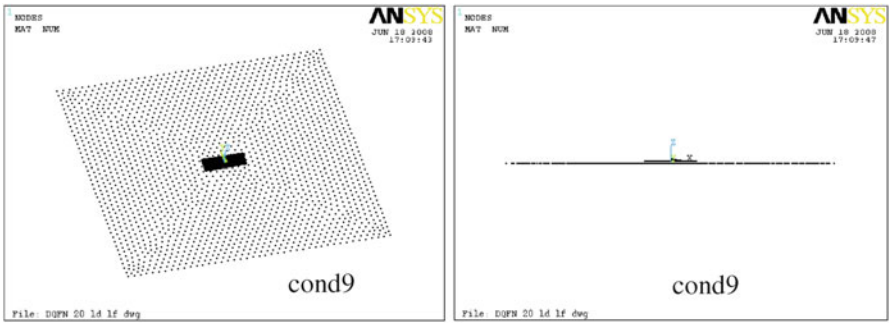


Fig. 12.20 Ground plane setting

"cond9" if there are eight pins defined as components) as shown in Fig. 12.20. *In other cases, if the DAP is floating, the external nodes of DAP cannot be defined as ground.*

Because the package model is symmetric, it is not necessary to calculate the self capacitance and mutual capacitance of all the 20 pins. In order to calculate the self capacitance C_{ii}, and mutual capacitance $C_{i,i+1}$ and $C_{i,i+2}$, the external nodes of eight pins (i.e., Pin1–7 and Pin20) are defined as components (cond1–8). The ground plane, which includes the nodes of the bottom area of test board and DAP, is defined as component "cond9" as shown in the above figures. The other pins are not defined as components, but they cannot be neglected when building the solid model.

10. Apply the infinite surface boundary condition to the five exterior areas (the sixth exterior area is the ground plane)
Figure 12.21 shows the boundary layout.

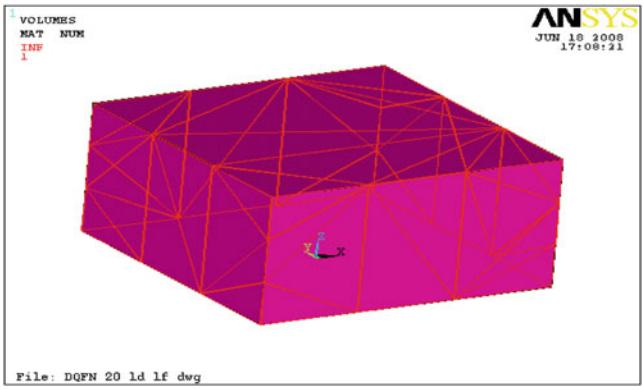


Fig. 12.21 The infinite surface boundary condition

11. Run the analysis and check the results

For ANSYS, use the following commends to run it.

cmatrix,symfac,'condname',numcond,grndkey

symfac: geometric symmetry factor. Defaults to 1.0

Condname: conductor name

Grndkey = 0 if ground is one of the components or 1 if ground is at infinity

Numcond: total number of components.

The example is:

```
/SOLU
CMATRIX,1,'cond',9,0
```

Results of the analysis will be written to a file named cmatrix.txt in the ANSYS working directory as a capacitance matrix in two formats, "Ground" and "Lumped."

12.1.2.2 Checklist

The Checklist is shown in Table 12.2 for capacitor simulation.

12.1.2.3 Remark for Ground and Lumped Capacitance

Finite element simulation can readily compute and extract a "Ground" capacitance matrix of capacitance values that relate the charge on one conductor with the conductor's voltage drop (to ground). A three-conductor system (one conductor is

Table 12.2 The checklist for the capacitor simulation

Capacitance modeling checklist
Select the proper analysis type: Preferences > Electromagnetics > Electric
Units of free space permittivity match dimensional units
Permittivity of material(s)
Detailed drawing with dimensions
Meshing completed without error/warning
Component associated with each conductor
Apply infinite surface boundary condition
Internal elements cleared from all conductor volumes
Solution completed without error/warning
Add lumped capacitance values to package model parameter file

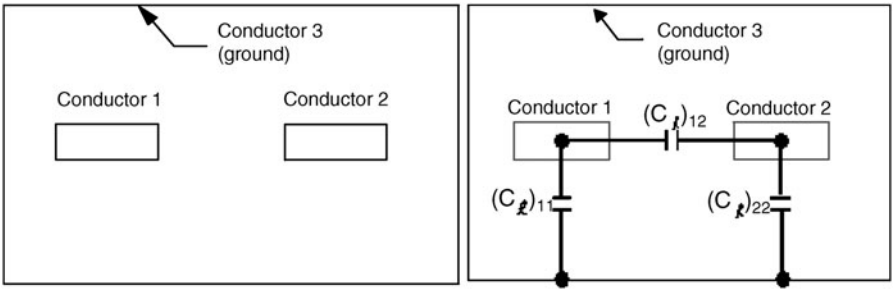


Fig. 12.22 A three conductor system

ground) shown in Fig. 12.22 is used to illustrate the ground and lumped capacitance matrix. The following two equations relate charges on electrodes 1 and 2, Q_1 and Q_2, with the voltage drops for the electrodes, U_1 and U_2:

$$\begin{aligned} Q_1 &= (C_g)_{11}(U_1) + (C_g)_{12}(U_2) \\ Q_2 &= (C_g)_{12}(U_1) + (C_g)_{22}(U_2) \end{aligned} \tag{12.9}$$

where C_g represents the matrix of ground capacitances.

The *CMATRIX* command macro in ANSYS can convert the ground capacitance matrix to a lumped capacitance matrix, which is typically used in a circuit simulator such as Spice. The lumped capacitances between the conductors are illustrated in Fig. 12.22. The following two equations then relate the charges with the voltage drops:

$$\begin{aligned} Q_1 &= (C_l)_{11}(U_1) + (C_l)_{12}(U_1 - U_2) \\ Q_2 &= (C_l)_{12}(U_1 - U_2) + (C_l)_{22}(U_2) \end{aligned} \tag{12.10}$$

where C_l represents the matrix of lumped capacitances.

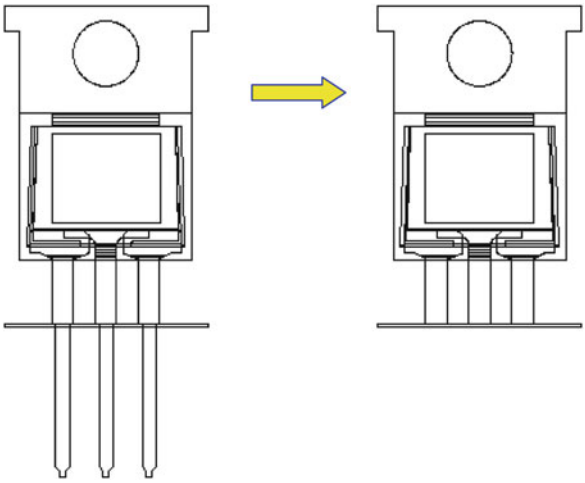


Fig. 12.23 The DIP type package

12.1.2.4 Remark for Capacitance Extraction for Through-Hole Leaded Packages

For the DIP (dual inline package), SiP (single inline package), PGA (pin grid array) packages, etc., the solid model could be simplified. Figure 12.23 shows the model simplification taking TO220 as an example. The air volume and infinite boundary follow the same rule as described for DQFN package. And the procedures are also same.

12.2 Defect Impact on Power Package Electrical Performance

This section will discuss the impact of wire bonding-related defects and the die attach solder voids for the electrical resistance, inductance and fusing current capability of the power packages. The major work in this section consists of two parts. One is the impact of wire bonding-related defects on the electrical performance of the power package. The other is the impact of die attach (DA) solder void. Both electrical and coupled thermal electrical simulations are conducted to study the wire bonding-related defects and DA solder voids of different levels.

12.2.1 Background

The common power package defects include die attach solder crack/voids, wire bonding crack and delamination between lead frame and EMC. During the die attach process voids can form in solder paste between die and the lead frame dap. In

the wire bonding process, the interface between bond wire and pad may not be fully bonded. The wire bonding defects induced during the wire bonding process are usually characterized as the outer edge of the interface is bonded while the center of the interface may not be bonded well. Another typical wire bonding-related defect is bond lifting/delamination between the bond wire and silicon die/lead frame. In addition, the cratering is also a big concern under the bond pad. The poor adhesive strength between lead frame and EMC may induce delamination in next step assembly process such as the trim and form process. The further process, such as reflow in precondition, may induce delamination due to moisture and the CTE mismatch between lead frame and EMC. However, this section will only focus on the modeling and simulation for the electrical performance of a package with and without typical wire bonding and die attach defects.

The modeling methodologies for electrical resistance, inductance (RL) and fusing current capability of the power package are developed based on the finite element code ANSYS. The self and mutual inductance as well as resistance are extracted from a 3D model of the power package using ANSYS/Multiphysics. The fusing current capability is simulated through coupled thermal and electrical simulations. Modeling result can be used for packaging design optimization and the assembly process optimization. It can further be used to generate the SPICE model to conduct circuit modeling. Investigation of the assembly defect impact is very useful for IC designers to understand the electrical performance with various defects. It is also helpful for the package engineers, reliability engineers and the assembly engineers to understand how the defects induced in assembly process will impact the performance of a product so that they can make improvement to meet the requirements of the products. The major modeling work in this section consists of two parts. One is the impact of wire bonding related defects on the electrical performance of the power package, the other is the impact of die attach (DA) solder void.

12.2.2 Resistance, Inductance and the Fusing Current

Methodology to extract resistance and inductance with FEA has been discussed in Sect. 12.1. In the package current capability analysis, the fusing current test is generally used to determine the maximum current capability of a certain package. The test setup is shown in Fig. 12.24 for a DPAK package. An external heat sink is attached to the package bottom during the test [7].

The coupled thermal and electrical simulation is conducted for the fusing current analysis. The FEA model is shown in Fig. 12.25 with a DAPK as an example. The silicon die is assumed as bulk silicon, and its electrical resistivity is determined based on its dimension and $R_{DS(ON)}$. A 0-V voltage is applied to the source lead, and the current is applied to the drain pad. The bottom surface of the package is assumed to be 298 K, which simulates the ideal boundary condition for external heat sink. A transient simulation within 5 min is conducted, and the max temperature of the source wire is compared with the melting temperature of Al (933.5 K) to judge if the wire will be fused or not.

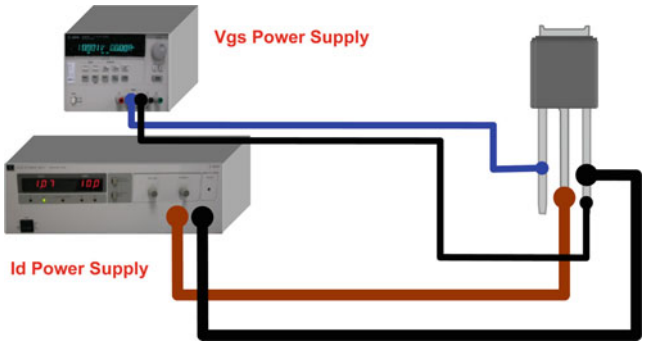


Fig. 12.24 Test setup for fusing current capability

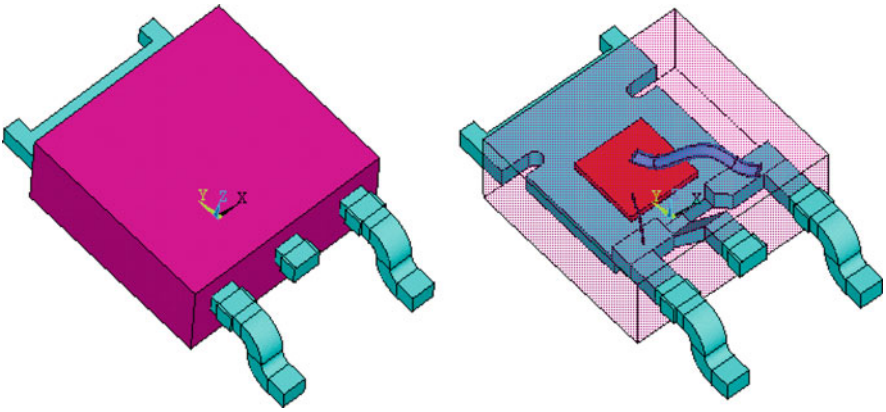


Fig. 12.25 FEA model of DPAK

12.2.3 Impact of Wire Bonding Related Defect

The impact of wire bonding defect is studied by using a typical power package DPAK with size 9.9 × 6.54 mm^2, which is shown in Fig. 12.25. Al wires (15 mil source wire and 2 mil gate wire) are bonded to make connection between the silicon die and the *I/O* leads. The major Al wire bonding related defects includes wedge bond lifting, heel crack, mid-span wire break, bond-to-bond shorting, wire-to-wire shorting, and cratering, etc. Wedge bond lifting means detachment or nonsticking of the wedge bond from the silicon die, bonding post, or lead finger. This may result from contamination on the bond pad or lead finger, incorrect parameter settings, instability of the die or lead frame during bonding, bond pad or lead finger corrosion, etc. Heel crack means breakage of the wire at the heel of the Al wedge bond, which is caused by incorrect wire bond parameter settings, incorrect wire looping, lead finger-to-package delamination, excessive wire sweeping during molding process, etc. In this study, wedge bond lifting from the silicon die and heel crack at the first bond of source wire are investigated.

Table 12.3 Extracted *R*/*L* of a perfect DPAK model

Frequency	Pin#	L_{ii} (nH)	L_{ij} (nH)	R (mΩ)
1 Hz	Source	4.366	0.762	0.96
	Gate	4.735	0.762	34.5
1 KHz	Source	4.366	0.762	0.96
	Gate	4.735	0.762	34.5
1 MHz	Source	3.521	0.551	3.61
	Gate	4.031	0.551	36.7

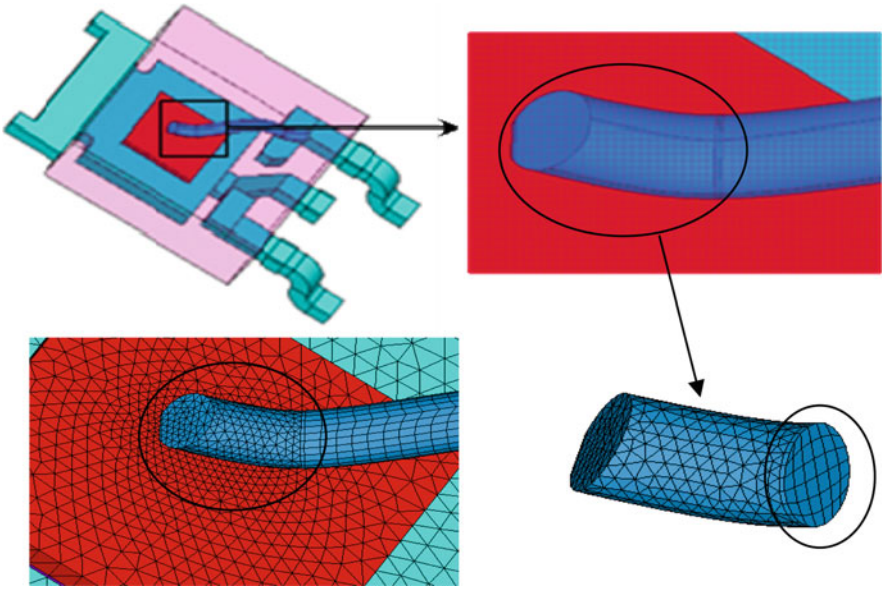


Fig. 12.26 Heel crack location of the first bond of source wire

12.2.3.1 Impact of Heel Crack

According to the methodology introduced in the previous section, the resistance and inductance of the perfect model are extracted, and the simulation results are listed in Table 12.3 for a perfect DPAK model without defects. It can be seen that with the increase of the AC frequency to 1 MHz the inductance of the source wire, gate wire, as well as the mutual inductance between them decreases. However, the resistance of both source wire and gate wire increases. This may be caused by the skin effect with high frequency.

Assumed the heel crack location of the first bond of source wire is illustrated in Fig. 12.26. A very thin layer is cut around the wedge bond heel area. The heel crack is simulated by deleting part of the elements in the layer, e.g., half elements in the layer are deleted to simulate 50% heel crack. This may not have much influence on the simulation accuracy as long as the cut layer is thin enough. According to the

Table 12.4 Extracted *R*/*L* of the model with 25% heel crack

Frequency	Pin#	L_{ii} (nH)	L_{ij} (nH)	R (mΩ)
1 Hz	Source	4.366	0.761	0.97
	Gate	4.735	0.761	34.5
1 KHz	Source	4.366	0.761	0.97
	Gate	4.735	0.761	34.5
1 MHz	Source	3.522	0.550	3.61
	Gate	4.031	0.550	36.7

Table 12.5 Extracted *R*/*L* of the model with 50% heel crack

Frequency	Pin#	L_{ii} (nH)	L_{ij} (nH)	R (mΩ)
1 Hz	Source	4.402	0.765	1.00
	Gate	4.735	0.765	34.5
1 KHz	Source	4.402	0.765	1.00
	Gate	4.735	0.765	34.5
1 MHz	Source	3.555	0.553	3.66
	Gate	4.032	0.553	36.7

specification, the heel crack area should not exceed 25% of the cross section of the bond wire. In this study, 25 and 50% heel crack of source wire are considered to study the heel crack impact.

The extracted resistance and inductance of the package with 25 and 50% heel crack of source wire are illustrated in Tables 12.4 and 12.5, respectively. The extracted resistance and inductance keep almost the same even if the source wire has 25% heel crack. When the heel crack propagates to 50%, the inductance and resistance of both source wire and gate wire have very small increase. This indicates that the heel crack of source wire has very little impact on the resistance and inductance of the DPAK package.

The fusing current analysis for the perfect model is conducted with a 50 A current applied to the drain pad. Through the coupled thermal and electrical simulation, the temperature distribution of the package is obtained as shown in Fig. 12.27. With the current of 50 A, the max temperature of the Al wire reaches 662 K, which is below the melting temperature of Al (933.5 K). Therefore, more simulations are conducted by applying higher drain currents with all the other conditions fixed. In this way, the fusing current of the perfect package is obtained, which is around 66 A (the cross point of temperature curve and the melting temperature dot line, as shown in Fig. 12.28).

The impact of source wire heel crack on the fusing current capability of the package is studied using the same methodology. The simulations results for 25 and 50% heel cracks are obtained by applying a drain current of 50 A. It seems that the max current density does not change much with 25% heel crack of source wire and it has an increase of about 15% with 50% heel crack of source wire. However, the maximum temperature of the Al wire induced by the drain current increases less than 1 K even with 50% heel crack of source wire. This indicates that the heel crack of source wire has very little impact on the fusing current capability of the package.

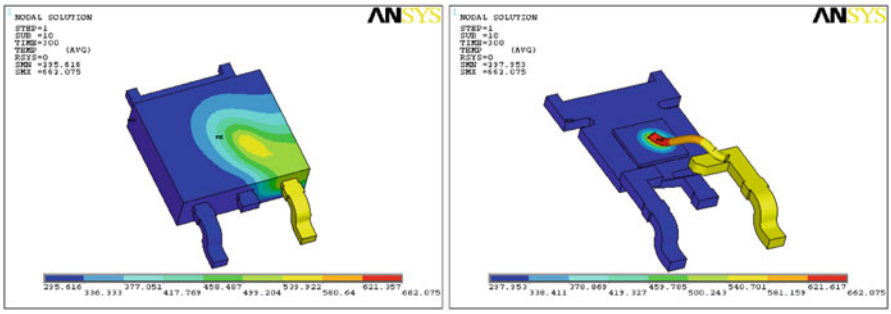


Fig. 12.27 Temperature distribution of the perfect model

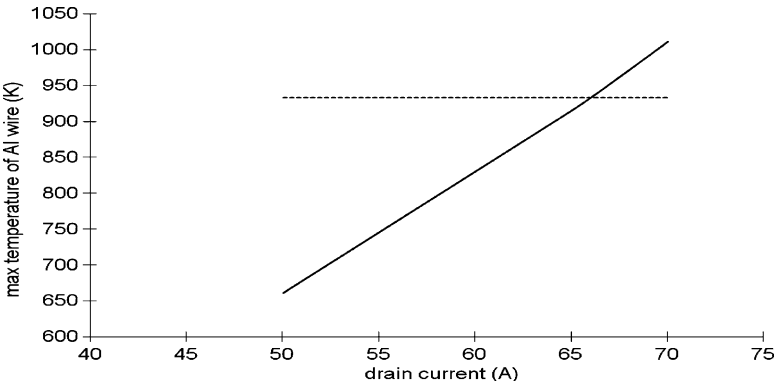


Fig. 12.28 The max temp of Al wire vs. applied drain current for perfect package model

12.2.3.2 Impact of Bond Lifting

The FEA model of the package and the Al bond wire with the enlarged wedge bond figure are shown in Fig. 12.29.

Two types of wedge bond defect are studied as shown in Fig. 12.30. One represents the delamination between the wedge bond and the silicon die (type A), the other is induced during the wire bonding process (type B), which usually characterizes as the outer edge of the interface is bonded while the center of the interface is not bonded well. Similar as the wedge bond heel crack simulation, part of the elements in the very thin layer of the wedge bond are deleted to simulate the bond lifting effect. According to the specification, the bond lifting area should not exceed 50% of the whole bond area. In this study, 50 and 75% bond lifting of the first bond of source wire are considered to study the bond lifting impact.

Through the electrical simulation, it is found that the two types of wedge bond defect generate quite close resistance and inductance values of the package. The detailed simulation results are listed in Tables 12.6 and 12.7 with 50% bond lifting and 75% bond lifting, respectively. Comparing with the simulation results from the

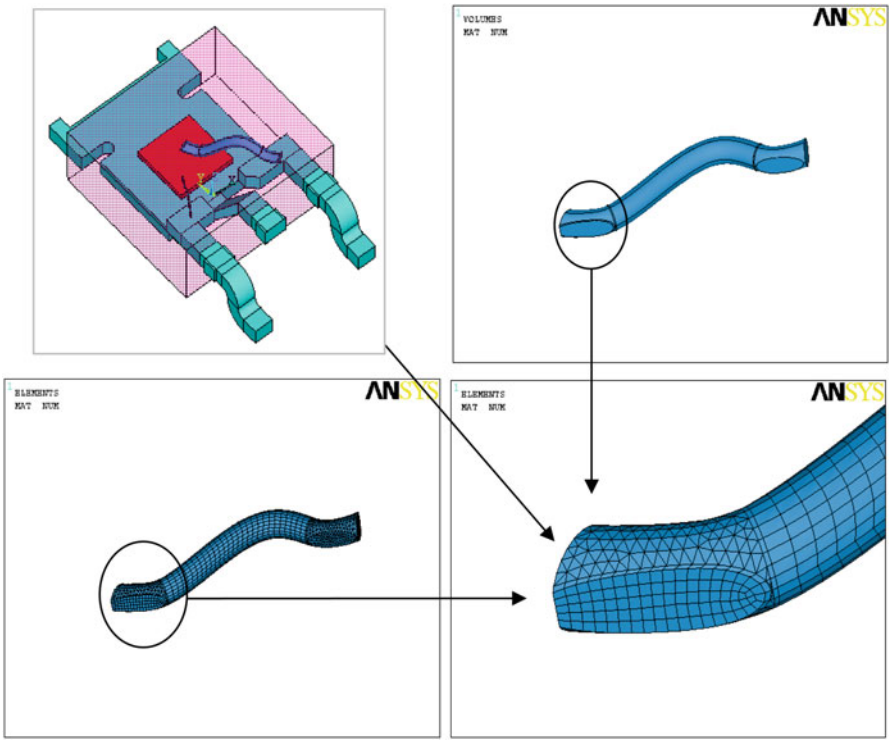


Fig. 12.29 FEA model of Al wedge bond

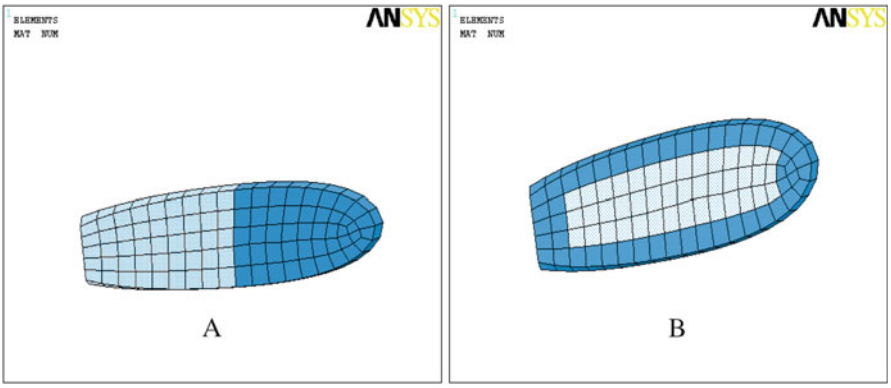


Fig. 12.30 FEA model simulating 50% bond lifting

Table 12.6 Extracted *R*/*L* of the model with 50% bond lifting

Frequency	Pin#	L_{ii} (nH)	L_{ij} (nH)	R (mΩ)
1 Hz	Source	4.338	0.757	0.97
	Gate	4.735	0.757	34.5
1 KHz	Source	4.338	0.757	0.97
	Gate	4.735	0.757	34.5
1 MHz	Source	3.569	0.576	3.67
	Gate	4.053	0.576	36.7

Table 12.7 Extracted *R*/*L* of the model with 75% bond lifting

Frequency	Pin#	L_{ii} (nH)	L_{ij} (nH)	R (mΩ)
1 Hz	Source	4.355	0.760	0.96
	Gate	4.735	0.760	34.5
1 KHz	Source	4.355	0.760	0.96
	Gate	4.735	0.760	34.5
1 MHz	Source	3.546	0.565	3.64
	Gate	4.044	0.565	36.7

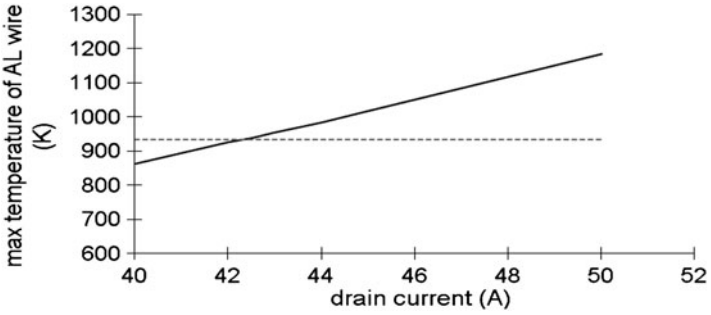


Fig. 12.31 The max temp of Al wire vs. applied drain current for the package model with 50% bond lifting (type A)

perfect model, the extracted resistance and inductance have very small changes. This indicates that both the resistance and inductance of the DPAK package are not sensitive to the wedge bonding lifting defect.

The temperature distribution and current density vector are obtained by doing the fusing current simulation using coupled thermal and electrical method. The fusing current capability of the package model with two types of wedge bond lifting defects (see Fig. 12.30) is studied. The simulation results of the package model with 50% bond defect of type A are illustrated in Fig. 12.31. The max temperature of the Al wire increases to 1,184 from 662 K of the perfect model when the same drain pad current (50 A) is applied. The max current density also increases with the max value located at the bond defect area. The fusing current of the model with 50% bond defect of type A decreases rapidly to around 42.5 from 66 A. The fusing current 42.5 A is determined by the cross point between the temperature curve and the melting temperature dot line.

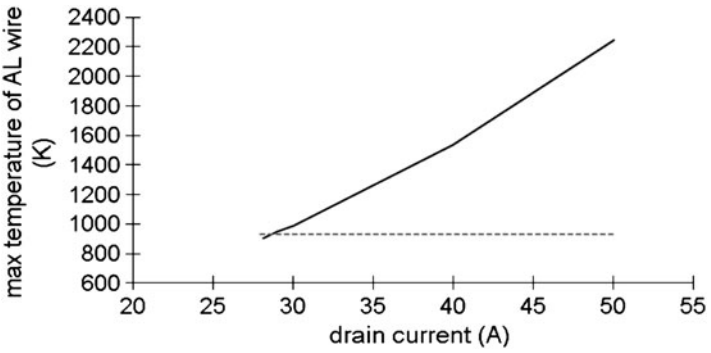


Fig. 12.32 The max temp of Al wire vs. applied drain current for the package model with 75% bond lifting (type A)

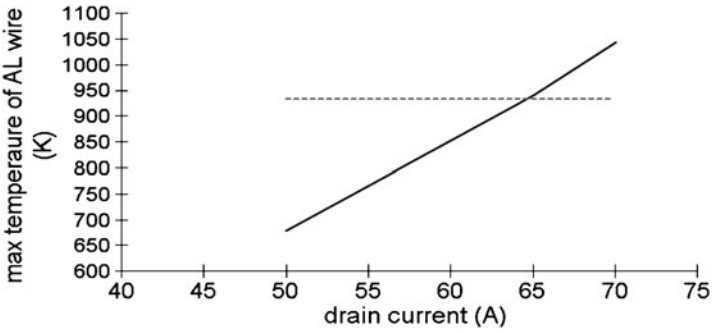


Fig. 12.33 The max temp of Al wire vs. applied drain current for the package model with 50% bond lifting (type B)

Figure 12.32 shows the simulation results of the package model with 75% bond defect of type A. It can be seen that both the max temperature and the max current density are increased significantly as compared with the perfect model and 50% bond defect of type A model. The fusing current of the model further decreases to around 28.5 A (the cross point between temperature curve and the melting temperature of the Al dot line). It can be concluded that the bond defect of type A has quite big impact on the fusing current capability of the package. Therefore, this type of defect, which corresponds to the delamination between the wedge bond and silicon die, should be carefully controlled during the assembly process.

The simulation results of the package model with bond defect of type B are illustrated in Figs. 12.33 and 12.34. Both 50 and 75% bond defect are studied for the fusing current capability of the package model. The fusing current of the model with 50% bond defect is around 64.5 A, and it decreases to around 58 A with the bond defect increasing to 75%. It can be seen that this type of bond defect induced during wire bonding process could endure higher fusing current compared with the

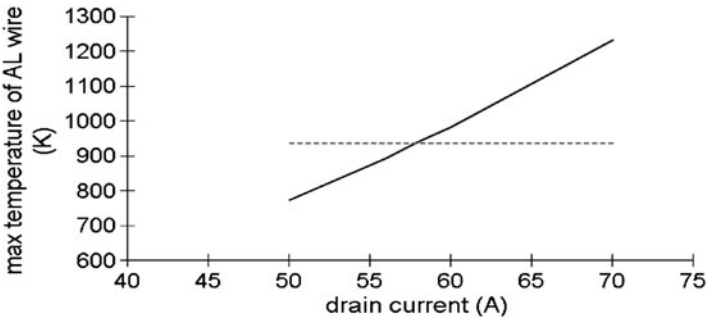


Fig. 12.34 The max temp of Al wire vs. applied drain current for the package model with 75% bond lifting (type B)

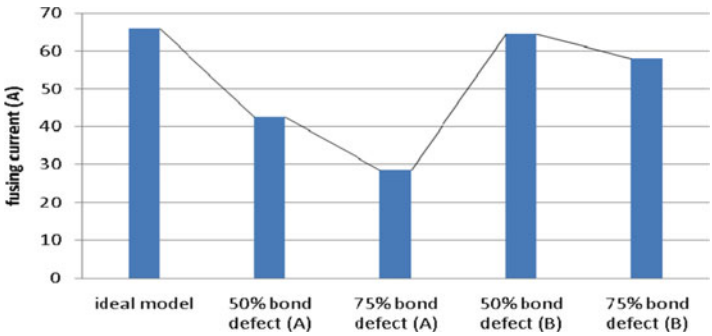


Fig. 12.35 Comparison of the fusing current capability of the perfect model and the models with bond defects

delamination-type bond defect. The comparison of the fusing current capability of the perfect model and the models with bond defects is shown in Fig. 12.35. The bond defect of type A has much larger impact on the fusing current capability than the bond defect of type B.

12.2.4 Impact of Die Attach Solder Void

In this section, we select a power package QFN5×6 mm for the study of the impact of die attach solder paste void on the electrical performance. This package has eight leads with 1.27 mm lead pitch. There are three source leads, one gate lead and four drain leads. The die attach solder material is 88Pb10Sn2Ag. The power package uses Al bond wires as the interconnection between the MOSFET die and the leads, in which the gate wire is 5 mil and the source wires are 8 mil single stitched for the source pad. Figure 12.36 is the model and mesh of QFN5×6.

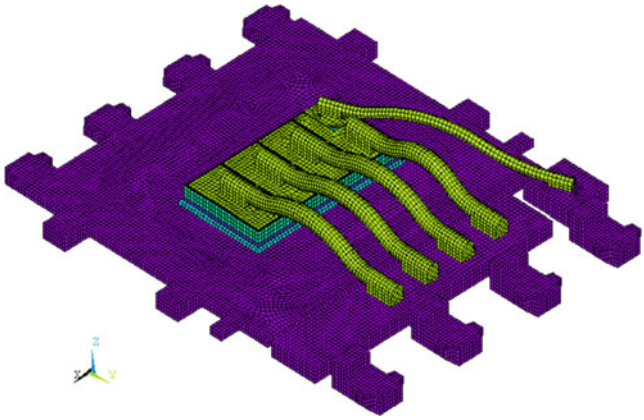


Fig. 12.36 A QFN5×6 mm model

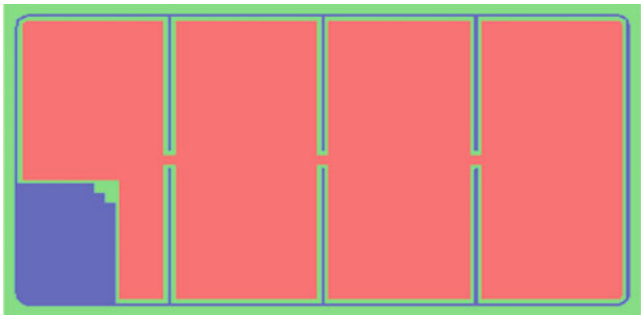


Fig. 12.37 The MOSFET die of QFN5×6

The die size is 2.36 × 1.27 × 0.2 mm^2, its surface layout is shown in Fig. 12.37.

The setting up for electrical modeling is shown in Fig. 12.38 with elements for insulator (blue area) which includes the nonconductive material such as the mold compound, die substrate, and the air, and elements for infinite (red area). The die attach voids are assumed to be individual voids at the center area each source units, and there is no void below the gate area. Figure 12.39 shows the die attach with different void levels. The simulation for this example is in 0.5 MHz.

Figure 12.40 gives the electrical potential and current density distributions. Figure 12.41 gives the magnetic potential and field distributions.

Table 12.8 gives the resistance and inductance of the QFN5×6 package with different void levels. From Table 12.8 we can see that the source resistance increases 141% as the voids increase 45%. The source self-inductance has slightly increased, while the mutual inductance has reduced a little bit when the die attach voids increase.

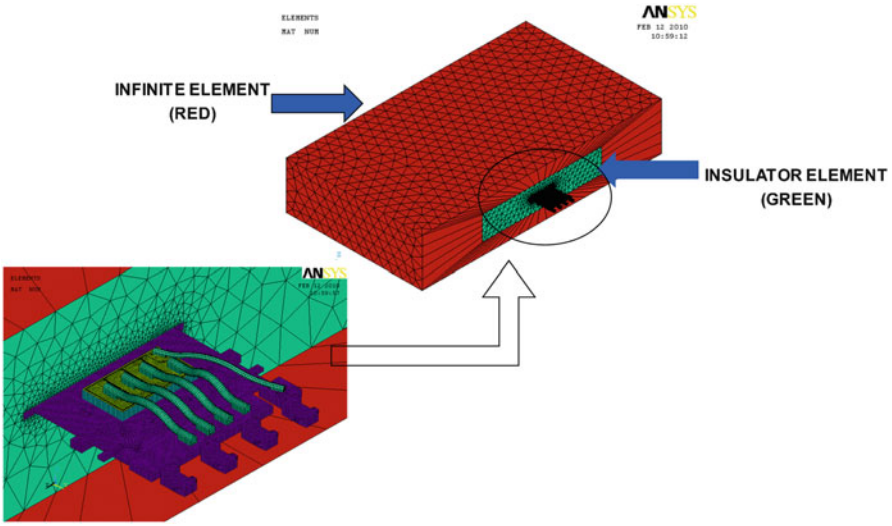


Fig. 12.38 The electrical modeling setup for QFN5×6

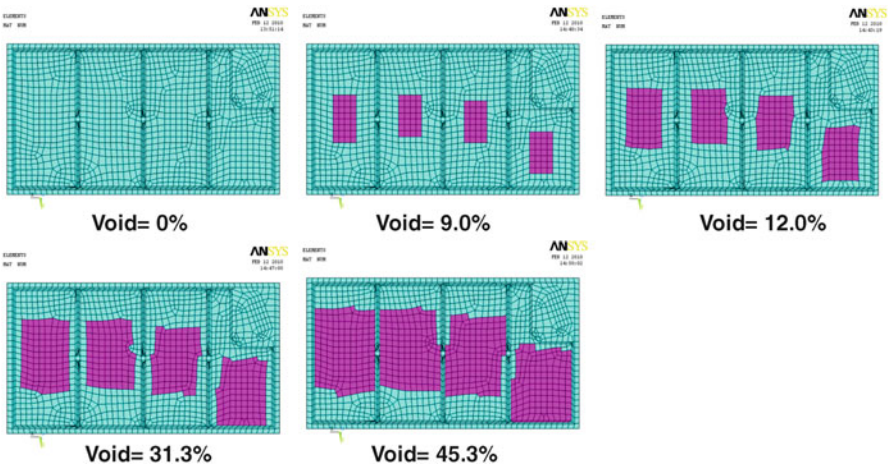


Fig. 12.39 Models of die attach void with different level

12.2.5 Discussion and Conclusions

This section studies the impact of defects on electrical performance of power packages with two types of defects—wire bonding defect (wedge crack and bonding lift) and the die attach voids. The first is the impact of wire bonding related defects on the resistance, inductance and fusing current capability of a DPAK power package. The second is the impact of the die attach (die bonding) voids on the resistance and

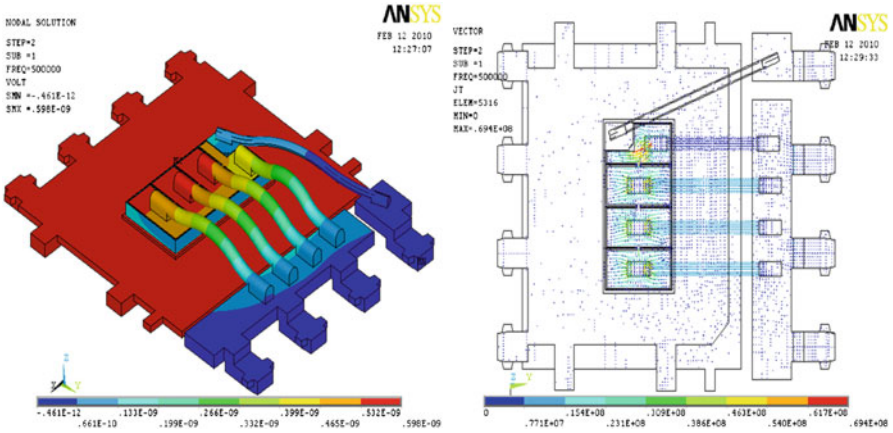


Fig. 12.40 Electric potential and current density distribution

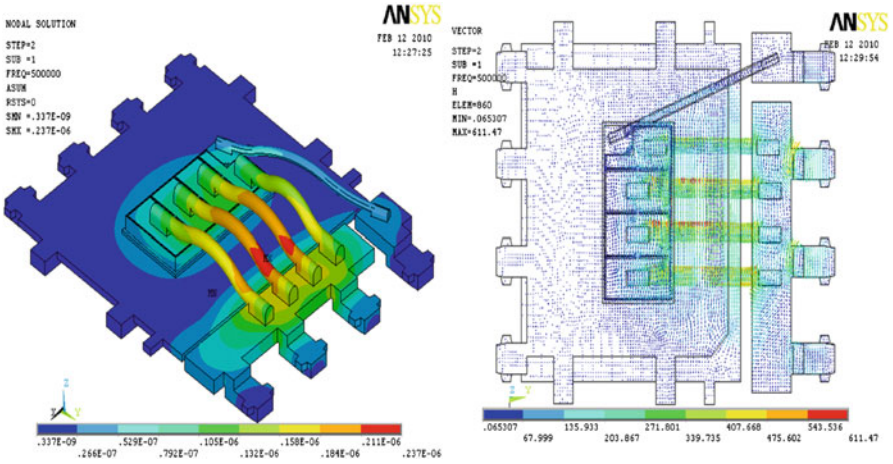


Fig. 12.41 Magnetic potential and field distribution

Table 12.8 Electrical simulation for resistance and the inductance for QFN5×6 package

	Resistance (mΩ)				
Void (%)	Gate	Source	Lgg (nH)	Lss (nH)	Lgs (nH)
0	1037.75	5.995	1.88	0.552	0.134
9	1037.75	6.147 (102.5%)	1.88	0.553	0.134
12	1037.75	6.472 (108.0%)	1.88	0.554	0.134
31.3	1037.75	7.114 (118.7%)	1.88	0.556	0.133
45.3	1037.75	8.474 (141.4%)	1.88	0.563	0.132

inductance of a QFN5×6 power package. The electrical simulations are performed to extract the resistance and inductance of the package at different frequency levels. The fusing current analysis is conducted by using coupled thermal electrical simulations for the wire bonding defects.

According to the simulation results, it is found that the electrical resistance and inductance of the package are not sensitive to the wire bond defects. However, the wire bond defects may induce significant impact on the fusing current capability of the package. For die attach voids, the inductance of the package seems not sensitive to the die attach void defect while the electrical resistance have been affected significantly. That is, as the defect area increases, the package fusing capability will be significantly reduced due to wire bonding defect, while the electrical resistance will increase significantly due to the die attach voids.

12.3 Power UIL/UIS Test and Simulation

In power packages, the DC test for $R_{DS(ON)}$, AC test for various parameters, test for fusing current capability, and unclamped inductive load (UIL) or unclamped inductive switching (UIS) test, are important and critical for assurance of the robust product performance, quality, and reliability. The fusing current capability test tries to simulate which case has the highest fusing current capability. The fusing current is generally used to determine the maximum current capability of a certain package. An UIL represents an extreme electrical stress condition since the energy stored in the inductor during the on-state is dumped directly into the device when it is turned off. The device UIL capability rating is also termed as "ruggedness," which is a scale of how much power the body diode can handle before it is destroyed. During the assembly process, some modifications might be made to achieve high machine throughput without affecting much electrical performance. However, this must be carefully investigated. In this section the layout of wire bond is thoroughly investigated by experimental work and FEA modeling. The initial design has three 8 mil source wires bonded on three pads of the die. Two evaluation cases using two 12 mil source wires bonded on two different pads are studied and compared with the control case. Both current fusing test and UIL test are simulated by FEA. It is indicated that the FEA simulation results have good correlation with the experimental results.

12.3.1 Background

The electrical tests such as DC test for $R_{DS(ON)}$, AC test for various parameters, test for fusing current capability, and UIL or UIS test for power packages are all critical in power electronics. The on-state resistance ($R_{DS(ON)}$) of a power MOSFET is made up of several components: substrate resistance, drift region resistance, "JFET" component-resistance, accumulation resistance, channel resistance, source diffusion resistance, and sum of bond wire resistance, the contact resistance

between the source and drain metallization and the silicon, metallization, and lead frame contributions. At high voltage loading, the $R_{DS(ON)}$ is dominated by epi resistance and JFET component. At lower voltage loading, the $R_{DS(ON)}$, is dominated by the channel resistance and the contributions from the metal to semiconductor contact, metallization, bond wires, and lead frame. The substrate contribution becomes more significant for lower breakdown voltage devices [8].

An UIL represents an extreme stressful condition since the energy stored on the inductor during the on-state is dumped directly into the device when it is turned-off. UIL/UIS testing verifies device ruggedness as seen in real world applications since power MOSFETs are used extensively in driving inductive loads such as motors, solenoid, relays, filters (e.g., synchronous buck converter), etc. Applications needing UIL capability include buck converters, flyback converters, automotive fuel injectors, etc. Heat-related failure mechanisms of UIL testing have two modes: passive mode and active mode. Passive mode does not require bipolar action. It is simply caused by current density getting high enough (to critical temperature). Active mode gives lower ruggedness (and UIL rating) than passive mode [9–11].

During the assembly process, some modifications might be made to achieve high machine throughput without affecting the electrical performance. Replacing three 8 mil source wires by two 12 mil source wires will increase the bonding efficiency and machine throughput. However, careful characterization must be made to confirm the robustness of the two 12 mil source wires package. In the following sections, three 8 mil source wires and two 12 mil source wires of power package I-PAK are investigated through the DC test, the AC test, the fusing current test, and the UIL test. Both experimental work and FEA modeling are conducted in this study.

12.3.2 DC Test

A DC test is used for the electrical verification on semiconductor products to determine its capability on a steady-state (or low frequency) operation. $R_{DS(ON)}$, in particular is one of the most important DC tests. This parameter is used to check the total on-state resistance of a product and dictates the power dissipation of a part for a given constant current (I_D). When conducting current as a switch, the conduction power losses are:

$$P_{\text{conduction}} = \{I_D(\text{RMS})\}^2 \times R_{DS(ON)} \tag{12.11}$$

A change in the wire length or diameter will have significant effect on the $R_{DS(ON)}$ for a particular device. Looking into the formula of a conductor resistance,

$$R = \rho \frac{l}{A} \tag{12.12}$$

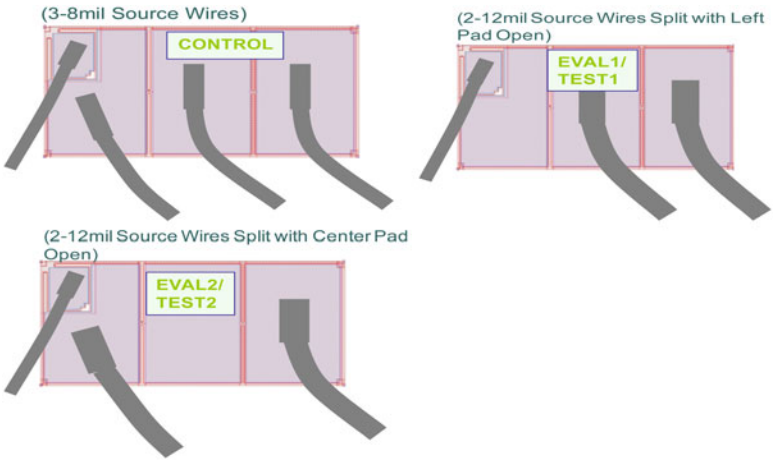


Fig. 12.42 Three types of split test samples

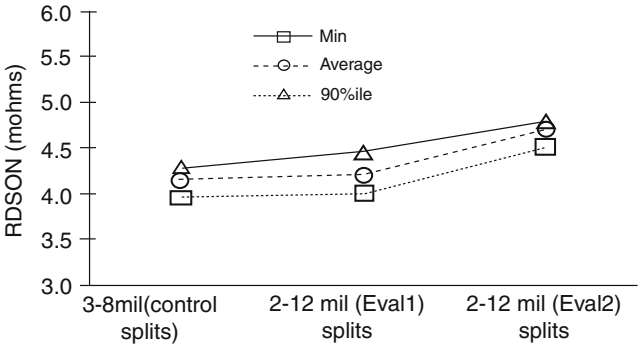


Fig. 12.43 FT $R_{DS(ON)}$ comparison between the three assembly splits

where ρ is the resistivity, l is the length, and A is the cross-sectional area. It can be noticed that with the Area ("A") variable on the bottom of the fraction, the resistance value decreases as the conductor area increases. More conductors connected in parallel also decrease its overall resistance.

Three splits of samples are manufactured and tested. One is used for a control split in which the three 8 mil source wires are bonded on the three source pads. Another two splits are used for evaluation. They are defined as Eval 1 and Eval 2 with two 12 mil source wires are bonded as shown in Fig. 12.42.

The test results of $R_{DS(ON)}$ for the control split (3–8 mil source wires) and two evaluation splits (2–12 mil source wires) are illustrated in Fig. 12.43 and Table 12.9. It can be seen that no significant $R_{DS(ON)}$ difference for Eval 1 and control split. However, Eval 2 shows significant $R_{DS(ON)}$ shift of 0.4–0.5 mΩ or 8–10% increase from 3–8 to 2–12 mil wires.

Table 12.9 $R_{DS(ON)}$ statistical comparison between the three assembly splits

	3–8 mil (control split)		2–12 mil (Eval 1)		2–12 mil (Eval 2)	
	$R_{DS(ON)1}$ (mΩ)	$R_{DS(ON)2}$ (mΩ)	$R_{DS(ON)1}$ (mΩ)	$R_{DS(ON)2}$ (mΩ)	$R_{DS(ON)1}$ (mΩ)	$R_{DS(ON)2}$ (mΩ)
Test condition	$V_{GS} = 4.5$ V/ $I_D = 33$ A	$V_{GS} = 10$ V/ $I_D = 35$ A	$V_{GS} = 4.5$ V/ $I_D = 33$ A	$V_{GS} = 10$ V/ $I_D = 35$ A	$V_{GS} = 4.5$ V/ $I_D = 33$ A	$V_{GS} = 10$ V/ $I_D = 35$ A
FT limit	7.84	5.59	7.84	5.59	7.84	5.59
Min	5.22	3.96	5.51	4.00	5.79	4.53
10%ile	5.28	4.02	5.57	4.09	5.90	4.63
25%ile	5.33	4.07	5.61	4.11	5.93	4.66
Median	5.41	4.14	5.64	4.15	5.97	4.69
Average	5.49	4.18	5.75	4.22	5.99	4.71
75%ile	5.54	4.25	5.71	4.26	6.01	4.72
90%ile	5.63	4.34	5.91	4.47	6.07	4.80
95%ile	5.85	4.44	6.36	4.64	6.13	4.88
99.3%ile	7.64	4.78	8.22	5.00	6.80	5.18
Max	8.64	5.54	8.82	5.14	7.75	5.40
Std	0.37	0.16	0.40	0.19	0.14	0.10
N = samples	1,101	1,101	1,088	1,088	538	538

12.3.3 AC Test

AC test is the electrical verification for a semiconductor product at high frequency operations. Some of the most common AC parameters used for semiconductor devices are: switching tests, capacitance, gate charge, and Trr/Qrr.

The AC test results of switching characteristics are listed in Table 12.10 for the control and Eval 1 splits. No significant difference can be seen from it.

12.3.4 Fusing Current Test

1. Experimental work
   This test is to simulate which split type of samples has the highest fusing current capability. The fusing current is generally used to determine the maximum current capability of a certain package. The test setup is shown in Fig. 12.24. An external heat sink is attached to the package bottom.

   Five samples with 3–8 mil source wires (from control split) and five samples with 2–12 mil source wires (from Eval 1 split) are tested. V_{GS} power supply of 10 V is applied. All ten samples reached 48 A constant current for 5 min without breaking down. This suggests the continuous current capability for both the 2–12 mil wire and 3–8 mil wire are higher than 48 A at steady state condition. No higher current was tested due to test equipment limitations.

2. FEA modeling
   The simplified FEA model is shown in Fig. 12.44, in which gate wire is neglected, die is assumed as bulk silicon, and its electrical resistivity is determined based on its dimension and the $R_{DS(ON)}$. The loading and boundary condition are set with the same power as in the experiment tests (Gate: volt = 10 V; Drain: current = 50 A; Source: volt = 0 V). The bottom surface of the package is assumed to be 298 K, which is the ideal condition for external heat sink.

   The coupled thermal and electrical simulations are conducted by the FE code ANSYS®. After 5 min, the max temperature of source wires is quite close for all the three cases. The max value is 430 K, which is far below the melting temperature of Al (933.5 K). This agrees with the test results.

   In order to obtain the maximum current capability of the package, more simulations with increasing drain current are conducted for three 8 mil wire case. The simulation results are listed in Table 12.11. It shows that the Al bond wire temperature reaches its melting temperature when the drain current increases to around 110 A. In experimental testing, the current might be lower because the external heat sink might not work as the ideal condition. This can be correlated when the new test equipment with higher current capability is on board.

Table 12.10 AC statistical comparison between the 2–12 and 3–8 mil Al source wires

Device FDU8796		Final data sheet spec.				2–12 mil Al bond wire					3–8 mil Al bond wire					Unit (except for CPK)
Item	Test condition	Min	Typ	Max	Unit	Min	Avg	Typ	Max	Stdev	Min	Avg	Typ	Max	Stdev	
Ciss	V_{DS} = 13 V,	/	1,960	2,610	pF	1931.8	2040.297	2052.5	2124.6	68.17	1888.32	2051.2	2081.43	2122.64	87.932	pF
Coss	V_{GS} = 0 V,	/	455	605	pF	498.13	519.8947	514.5	543.05	19.5	484.765	519.8	518.366	553.845	27.501	pF
Crss	f = 1 MHZ	/	315	475	pF	342.85	363.0596	359.9	386.64	18.46	327.731	363.38	361.407	395.317	25.631	pF
RG		/	1.1	/	Ω	1.107	1.1393	1.1335	1.199	0.029	1.106	1.1338	1.1205	1.213	0.037	Ω
Td(on)	V_{DD} = 13 V,	/	10	20	ns	11	12.32	12.4	13.5	0.855	10.6	12.63	12.75	13.5	0.835	ns
Tr	I_D = 35 A,	/	24	39	ns	35.2	43.61	42.7	61.1	8.049	34.7	43.08	41.1	54.6	7.003	ns
Td(off)	V_{GS} = 10 V,	/	99	158	ns	110	111.8	112	113	1.033	109	113.4	113.5	117	2.459	ns
Tf	R_G = 20Ω	/	57	91	ns	74.2	78.69	79	82.3	2.518	68	79.18	80.6	82.7	4.58	ns
Qg(s)	V_{DD} = 13 V,	/	19	27	nC	21.06	22.11	22.07	23.28	0.806	20.39	22.17	22.2	23.25	1.007	nC
Qg(D)	I_D = 35 A, I_G	/	37	52	nC	38.41	40.39	40.5	42.05	1.32	37.62	40.52	40.82	42.28	1.675	nC
Qgs	$_{(REF)}$ = 1.0 mA	/	6	/	nC	5.52	6.07	6.09	6.54	0.379	5.27	6.05	6.19	6.47	0.442	nC
Qgd		/	6	/	nC	7.99	9.13	9.02	10.12	0.69	8.39	9.26	9.2	10.15	0.601	nC
Vsd	Isd = 35 A	/	0.9	1.25	V	0.87	0.89	0.89	0.9	0.006	0.88	0.89	0.89	0.9	0.006	V
vsd	Isd = 15 A	/	0.8	1		0.8	0.81	0.81	0.82	0.005	0.8	0.81	0.81	0.82	0.004	V
Trr	Isd = 56 A, disd/	/	30	45	ns	27.92	28.43	28.5	28.92	0.367	27.25	28.5	28.71	29.25	0.673	ns
Qrr	dt = 100 A/μs	/	23	35	nC	18.5	19.43	19.45	20.1	0.583	17.5	19.6	19.9	20.5	0.942	nC

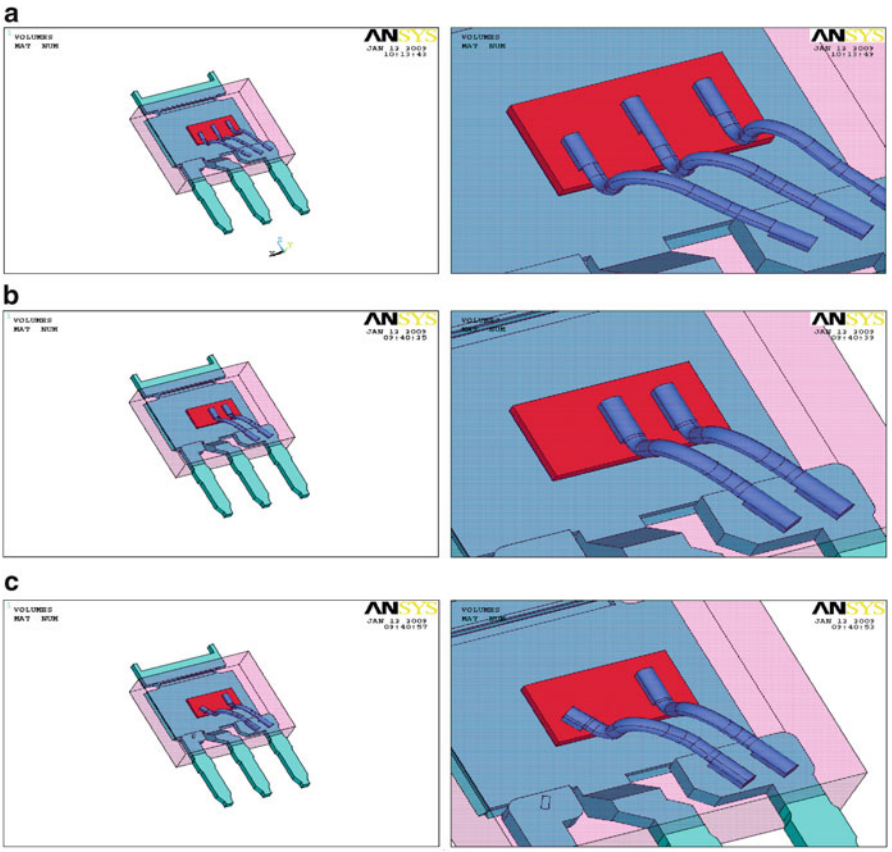


Fig. 12.44 Simplified FEA model of the package for three tests: (**a**) control case, (**b**) Eval 1, (**c**) Eval 2

Table 12.11 Simulation results with different drain currents

I_D (A)	T (K)
50	430
110	945
115	1,002
120	1,065

12.3.5 UIL Test

The simplified inductive switching test circuit for MOSFET is shown in Fig. 12.45. In the UIL test, the MOSFET is turned on and the drain current is ramped to a desired value. Then, the MOSFET is turned off and the magnetic field from the inductor collapses, causing the current to reverse and the body diode of the device under test undergoes avalanche breakdown. Figure 12.46 shows the circuit

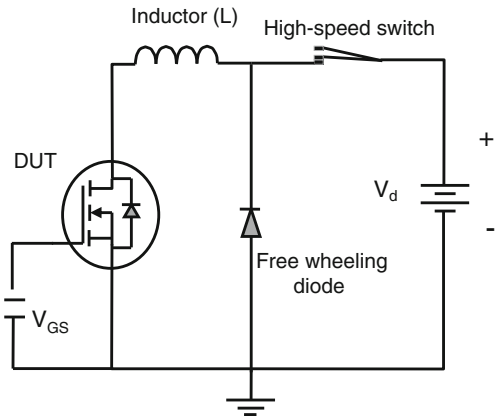


Fig. 12.45 Simplified inductive switching test circuit for MOSFET

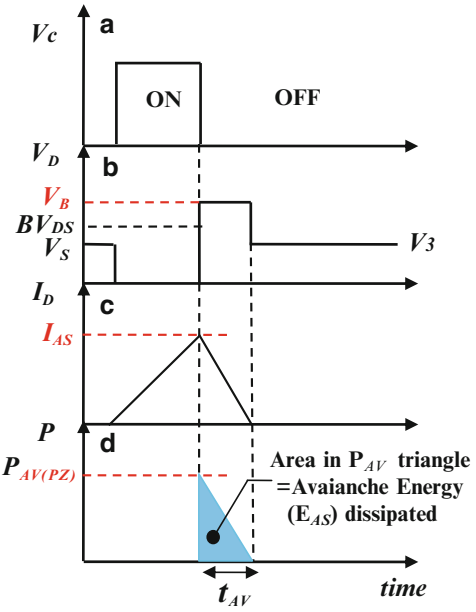


Fig. 12.46 Single pulse UIS waveform

waveform, and the dissipated avalanche energy which exactly equals to the area in the blue triangle (Fig. 12.46d) [11].

1. Experimental work
   A standard UIL characterization procedure at 25°C is conducted. A repetitive pulse to failure (RPF) test with fixed inductance value of 0.1, 0.3, 1, and 3 mH is performed to determine the device threshold to failure. The sample size is three

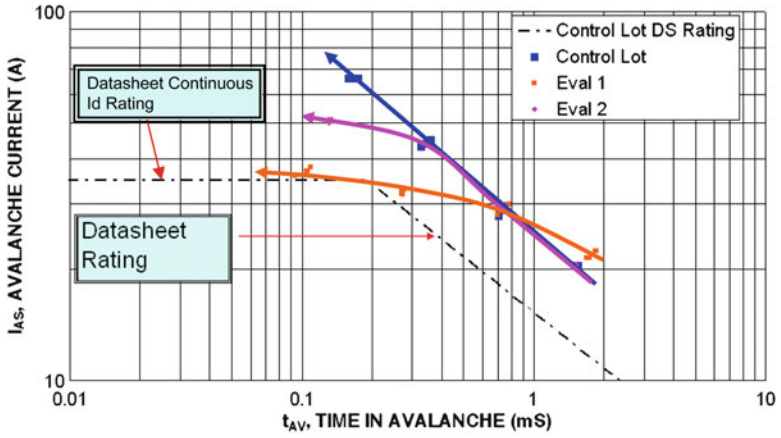


Fig. 12.47 Avalanche current (I_{as}) vs. avalanche time (T_{av})

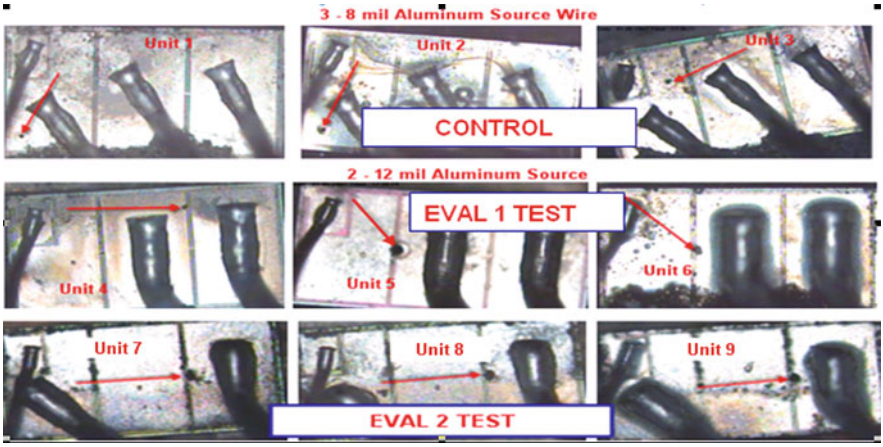


Fig. 12.48 FA decap (actual photo) for UIL failures after characterization

units per inductor per split. The characterization result is shown in Fig. 12.47. For control split the avalanche current (I_{as}) vs. avalanche time (T_{av}) plot shows a very linear function when plotted on a log–log scale. This should be the ideal behavior for a good product. Eval 1 and Eval 2 seem to saturate at higher current level ratings.

The samples were sent for decapsulation to check if there is a pattern for the hotspot location. The actual photos are shown in Fig. 12.48. All three units for the 3–8 mil wire samples (control split) have the hotspot located at the source pad at random location. The 2–12 mil wire sample units (for Eval 1 and Eval 2) however show consistent burned location around the gate bus. This might be caused by current crowding, which generates concentrated heat in these areas.

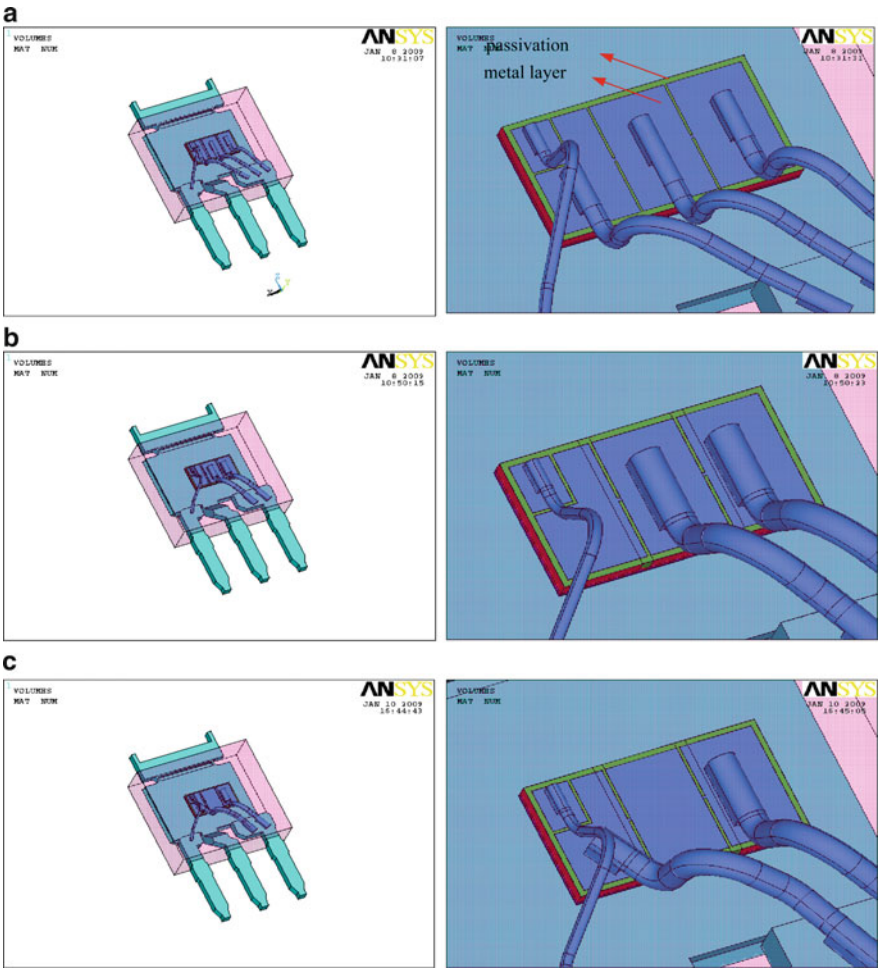


Fig. 12.49 FEA model for UIL simulation: (**a**) control, (**b**) Eval 1, (**c**) Eval 2

2. FEA modeling
   The simplified FEA model is shown in Fig. 12.49. The top metal layer, passivation, and bulk silicon are included in the model of the die. The equivalent electrical resistivity of the die is determined based on the drain voltage and current from the characterization test. The boundary condition is to apply the volt 0 V on gate and source, and to apply the volt 40 V on the drain.

   The coupled thermal and electrical simulations are conducted for the three cases. From the current density vector drawing Fig. 12.50, it can be seen that for Eval 1 (Fig. 12.50b) the max current density locates at the gate bus disconnection area between the source pad without bond wire and its neighbor source pad. For Eval 2 (Fig. 12.50c), the current density has high values at the gate bus

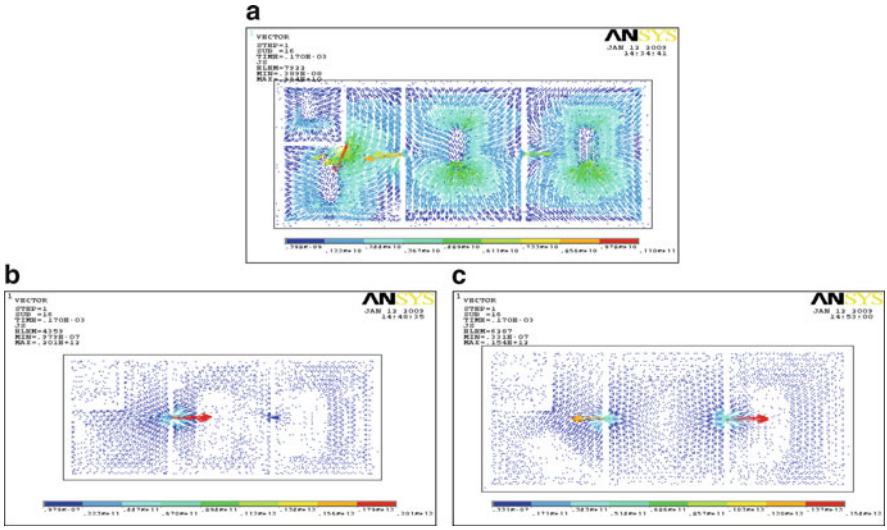


Fig. 12.50 Current density vector drawing of die: (**a**) control, (**b**) Eval 1, (**c**) Eval 2

disconnection area between the middle source pad (without bond wire) and its left and right neighbor source pad. The max value occurs at the right side because the left source pad is smaller compared with the right source pad.

The temperature distribution is illustrated in Fig. 12.51. For control case (Fig. 12.51a), the max temperature locates at the left source pad, and a large area has relatively high temperature value. For Eval 1 and Eval 2 (Fig. 12.51b, c), the max temperature has the same location as the max current density. This indicates that the high current density in the die causes the hot spot. These simulation results correlate well with the characterization tests in the previous section.

12.3.6 Discussion and Conclusion

The evaluation and characterization of I-PAK with two 12 mil source wires are conducted and compared with the same package using three 8 mil source wires. Both experimental work and FEA modeling are investigated. The simulation results have good correlation with the experimental test results. Through DC test, no significant $R_{DS(ON)}$ difference is observed for Eval 1 and control split. The AC test results of switching characteristics also have no significant difference between control case and two evaluation cases. The current fusing capability of packages with three different bond wire designs is also quite close. However, in UIL test, all three units for the three 8 mil wire samples (control split) have the hot spot located at the source pad at random location. But the two 12 mil wire sample units (for Eval 1

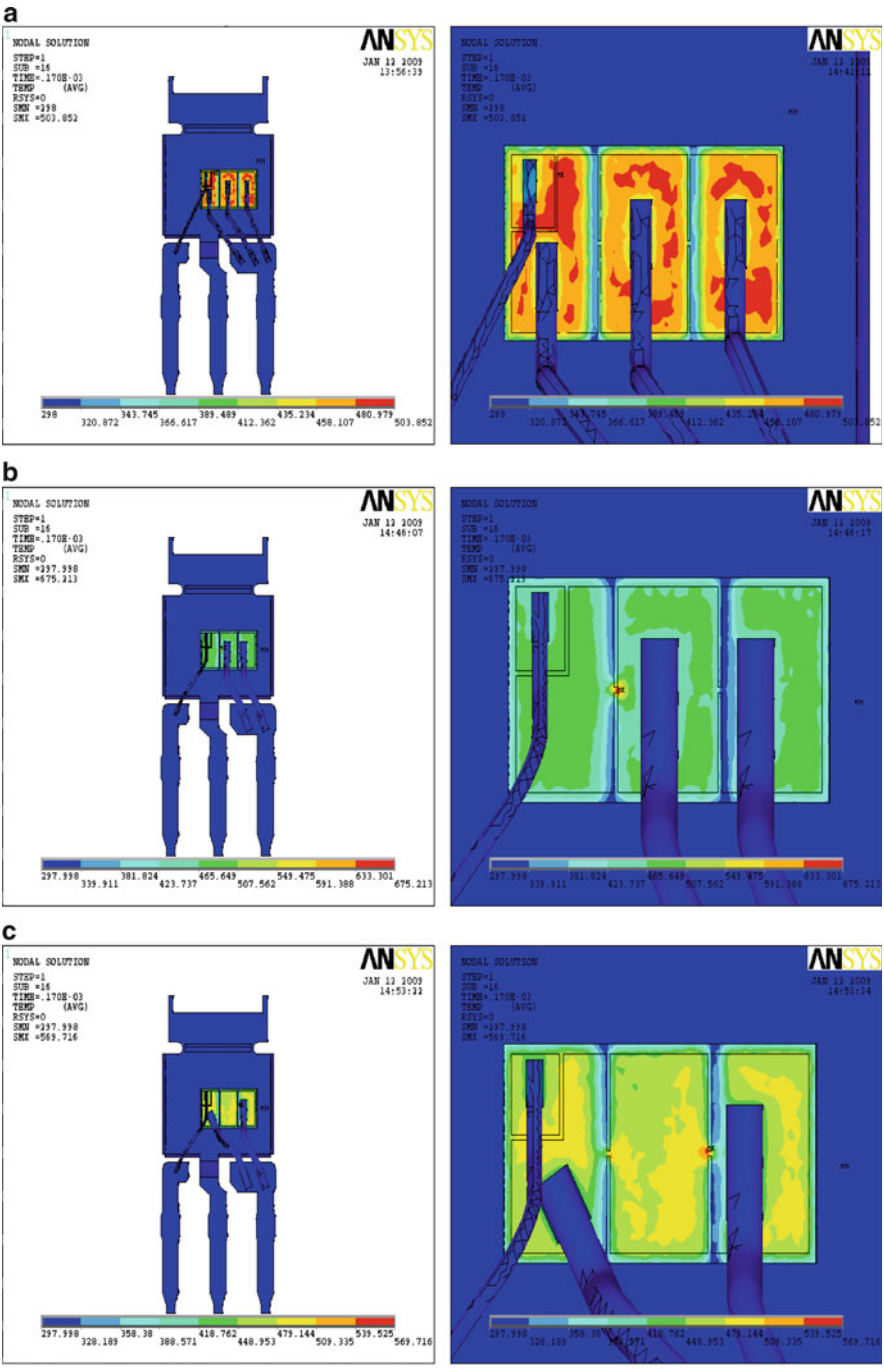


Fig. 12.51 Temperature distribution: (**a**) control, Max temp: 504 K, (**b**) Eval 1, Max temp: 675 K, (**c**) Eval 2, Max temp: 570 K

and Eval 2) show consistent burned location around the gate bus, which is the week point of the package. Through this study, it can be concluded:

1. Decreasing the number of source wires for any reason for a certain source pad layout is not advisable unless careful characterization is made.
2. For certain die layout, leaving a source pad open without any wire would create current crowding on the small area of the source pad separated by the gate bus runners near that pad. This current crowding creates a localized heating effect that affects the UIL performance.

12.4 Electromigration Simulation for Power WL-CSP

12.4.1 Background

Electromigration (EM) is a phenomenon of mass transport in metallization structures when the metallization is stressed with high electrical current density. This mechanism was reported in early work by Huntington and Grone [12], Blech and Meieran [13], and Black [14]. As the electronics industry continues to push for higher performance and miniaturization, the demands of higher current densities increases. This may cause electromigration failures, not only in IC interconnects but also in solder bumps of IC packages, especially in power wafer level packages, see the typical theoretical and experimental studies in solder joints by Tu and his coworkers [15, 16], Ho and his group [17], Basaran and his coworkers [18]. In recent years, there have been a lot of efforts attempting to predict the electromigration failure and to evaluate the electromigration lifetime through modeling. Dalleau et al. [20] developed the finite element model for electromigration in interconnects with mass continuity equation, which considers three mechanisms including the electromigration, the thermomigration, and the stress-migration. Later, Basaran and Lin [19] developed the damage mechanics for electromigration in solder joints and interconnects, which is governed by the vacancy conservation equation and is equivalent to mass conservation equation. Many other researchers also studied the atomic flux divergence (AFD) method based on finite element models [21–24]. However, the accuracy of the AFD method is always an issue. Tan et al. found that the conventional AFD formulation is not accurate in the predicting void nucleation site in a very thin film structure [23]. In fact, due to the coupled multiphysics character of EM and the challenges to get the divergence of stress and atomic flux gradients, it is extremely difficult to predict the exact location of EM induced void nucleation and to simulate the subsequent void evolution in an arbitrary interconnect segment and a solder joint in a wafer level chip scale package (WL-CSP).

This section proposes a new prediction method for electromigration induced void generation and time to failure (TTF) of solder bumps in a WL-CSP. The methodology is developed based on discretized weighted residual method (WRM)

in a user-defined FEA framework to solve the local electromigration mass continuity equation with the variable of atomic density. The local iteration procedure of the electromigration governing equation for the atomic concentration redistribution and its time step scheme are developed and discussed. Then, the local solution of atomic concentration is incorporated in the multiphysics environment for electrical, thermal and stress in both submodel and global model. Both the submodel and the global model FEA algorithms based on the multiphysics platform of ANSYS are developed to combine all the coupled fields and the information from the local atomic concentration finite element solution by WRM. Since the new method takes the advantage of solving the variable of atomic concentration, it avoids directly solving the divergences of the atomic flux, which includes the atomic concentration gradient items and is very hard and challenging to get the solution by traditional method. Furthermore, the new method considers the EM, atomic density gradient migration (ADGM), stress migration (SM) and thermal migration (TM), while the traditional electromigration modeling method only considers the EM, TM and SM. It neglects the effect of atomic concentration gradient which results in the traditional method loses the information of atomic density gradient (ADG), that will induce larger error in electromigration modeling, especially in predicting the TTF life. Our past electromigration study for a solder joint in a flip-CSP by the traditional AFD method [24] showed that, as compared to the measured mean time to failure (MTTF) test result, there is larger difference between the traditional prediction method and measurement.

In this section, we investigate the impact of the ADG on the atomic concentration distribution (including the effects of EM, ADGM, SM and TM) of solder bumps in a WL-CSP. The comparison of results with and without considering the ADG is fully presented and discussed. The results show that the effect of ADG on the atomic concentration is significant and it cannot be neglected. The TTF life of solder bump is simulated. The comparison to the MTTF is presented and discussed. The new FEM method developed in this section which includes all the ADG formulations, has demonstrated reasonable predicted TTF result.

12.4.2 Electromigration Formulation

Electromigration is a diffusion process which is controlled by the mass continuity (balance) equation. The time dependent evolution equation of a local atomic density in a solder bump can be written as

$$\nabla \cdot \vec{q} + \frac{\partial c}{\partial t} = 0 \tag{12.13}$$

where c is the normalized atomic density $c = C/C_0$, C is the atomic density and C_0 is the initial (equilibrium state) atomic density in the absence of a stress field, t is the time; $\vec{q}$ is the total normalized atomic flux vector.

Assuming that the driving forces of an atomic flux are electrical field forces (electron wind), thermal gradient, stress gradient, and ADG, respectively, the normalized atomic flux is given by [22].

$$\begin{aligned}\vec{q} &= \vec{q}_{Em} + \vec{q}_{\mathbf{T}h} + \vec{q}_S + \vec{q}_C \\ &= \frac{cD}{kT} Z^* e\rho\vec{j} - \frac{cD}{kT} Q^* \frac{\nabla T}{T} + \frac{cD}{kT}\Omega\nabla\sigma_m - D\nabla c \\ &= c \cdot F(T, \sigma_m, \vec{j}, \ldots) - D\nabla c \end{aligned} \tag{12.14}$$

where

$$F(T, \sigma_m, \vec{j}, \ldots) = \frac{D}{kT}\left(Z^* e\rho\vec{j} - Q^* \frac{\nabla T}{T} + \Omega\nabla\sigma_m\right) \tag{12.15}$$

where k is Boltzmann's constant; e is the electronic charge; Z^* is the effective charge which is determined experimentally; T is the absolute temperature, ρ is the resistivity which is calculated as $\rho = \rho_0(1 + \alpha(T - T_0))$, α is the temperature coefficient of the metallic material; D is the diffusivity, $D = D_0 \exp(-(E_a/kT))$, E_a is the activation energy, D_0 is the thermally activated diffusion coefficient; $\vec{j}$ is the current density vector; Q^* is the heat of transport; Ω is the atomic volume; σ_m is the local hydrostatic stress.

For the EM evolution equation (12.13) on any enclosed domain V with the corresponding boundary Γ, the atomic flux boundary conditions (BC) of a metal interconnects or a solder bump system can be expressed as

$$\vec{q} \cdot \vec{n} = q_0 \quad \text{on } \Gamma \tag{12.16}$$

For blocking boundary condition,

$$q_0 = 0 \quad \text{on } \Gamma \tag{12.17}$$

At the initial time, the normalized atomic density for all nodes is assumed to be

$$c_0 = 1 \tag{12.18}$$

The above equations and boundary conditions constitute the boundary value problem that governs the atomic transport during EM. This boundary value problem must be solved accurately in order to adequately describe the continuous atom redistribution and to capture the realistic kinetics of void nucleation and growth as a function of the interconnect architecture, segment geometry, material properties, and stress conditions.

12.4.3 EM Evolution Simulation

12.4.3.1 Atomic Density Redistribution Algorithm

In general, the atom redistribution, caused by various EM driving forces, tends to bring the atomic system to quasi-equilibrium (steady state). Depending on the particular UBM interconnect and solder bump geometry, material properties and applied electrical current, voids may be nucleated somewhere in the interface of UBM and solder joint. The nucleated void affects current density, temperature, and mechanical stress distributions around the void; hence, it changes the local atomic fluxes in the void vicinity and leads to further void evolution on solder joint.

In the finite element method, we seek an approximation solution for equation (12.13) to develop a new local simulation algorithm for the local atomic density in a solder joint system. The first step is to multiply the time dependent EM evolution equation with a weighted residual function w and integrate over the enclosed domain V based on the vector identity by applying the Gauss–Ostrogradsky divergence theorem to the product of the scalar function w and the atomic flux vector field $\vec{q}$.

$$\int_V w(\nabla \cdot \vec{q} + \dot{c})\, \mathrm{d}V = \int_V w\dot{c}\, \mathrm{d}V + \int_V w \cdot \nabla \cdot \vec{q}\, \mathrm{d}V$$

$$= \int_V w\dot{c}\, \mathrm{d}V - \int_V \frac{\partial w}{\partial \vec{n}} \cdot \vec{q}\, \mathrm{d}V + \int_\Gamma w \cdot (\vec{q} \cdot \vec{n})\, \mathrm{d}\Gamma = 0 \quad (12.19)$$

Equation (12.19) can be further written as,

$$\int_V w\dot{c}\, \mathrm{d}V - \int_V \frac{\partial w}{\partial \vec{n}} \cdot \vec{q}\, \mathrm{d}V = -\int_\Gamma w \cdot q_0\, \mathrm{d}\Gamma \quad (12.20)$$

Next, assume that $c = \sum_{j=1}^{n} \psi_j c^j$, $\dot{c} = \sum_{j=1}^{n} \psi_j \dot{c}^j$ and $w = \psi_i$ (for Galerkin Method), where ψ_i is the shape function of the element. After element discretization, the matrix form of (12.20) can be generated as

$$[M]\{\dot{c}\} + [K]\{c\} = \{F\} \quad (12.21)$$

where the matrix $[M]$ is independent of time, and $[K]$ will remain constant in an incremental step where we consider the current density $\vec{j}$ and the local hydrostatic stress σ_m are not varied (i.e., both are constants) in the current incremental step.

The most commonly used local iteration scheme for solving the above equation is the α-family of approximation method in which a weighted average of the time derivatives at two consecutive time steps is approximated by linear interpolation of the values of the variable at two steps:

$$(1-\alpha)\dot{c}_{t_i} + \alpha\dot{c}_{t_{i+1}} = \frac{c_{t_{i+1}} - c_{t_i}}{\Delta t}, \quad 0 \le \alpha \le 1 \quad (12.22)$$

From (12.21 and 12.22), it yields

$$([M] + \alpha\Delta t[K])\{c_{t_{i+1}}\} = ([M] - (1-\alpha)\Delta t[K])\{c_{t_i}\} + \{\bar{F}_{i,i+1}\} \tag{12.23}$$

where

$$\{\bar{F}_{i,i+1}\} = \{\bar{F}_{i,i+1}\} = (1-\alpha)\Delta t\{\bar{F}_{t_i}\} + \alpha\Delta t[M]\{\bar{F}_{t_{i+1}}\} \tag{12.24}$$

In this work, $\alpha = 0.5$ is used. Such method is called the Crank–Nicolson scheme which is stable and has the accuracy order of $O((\Delta t)^2)$. Thus, the normalized atomic density c in the $(i + 1)$th step can be obtained based on equation (12.23) in terms of the corresponding value in the ith step.

12.4.3.2 Simulation Algorithm of EM Induced Void Evolution

Electromigration is a phenomenon of mass transport in metallization structures when the metallization is stressed with high electrical current density. The damage induced by electromigration appears as voids and hillocks. The growth of voids in interconnects ultimately results in electrical discontinuity. Lifetime and failure location in an interconnect structure can be predicted by means of numerical simulation of the process of void incubation, initiation and growth. The changes in current density and temperature distribution due to void growth should be taken into account in simulation.

In this section, an indirect coupled analysis based on ANSYS is studied. The indirect coupled method and its flowchart may be found in our previous works [24].

The computation procedure of EM void evolution based on atomic density redistribution simulation algorithm and ANSYS multiphysics coupled analysis is shown in Fig. 12.52. The modeling flowchart consists of the simulation for an incubation period (a) and a void growth period (b). In the simulation for the incubation period, at first, the initial distributions of current density and temperature in the structure are obtained by the 3D finite element method analysis based on the ANSYS platform. Then, the atomic density redistribution in the considered solder bump is solved based on (12.22 and 12.23) with a user-defined FORTRAN code. The data exchange between the ANSYS and FORTRAN codes is developed with ANSYS program design language (APDL) and the system batch language in Windows or Unix to transfer the data.

Assume that there is a critical normalized atomic density for void initiation, $c^*_{\min}$, and for hillock initiation, $c^*_{\max}$. When the normalized atomic density c is less than or equal to $c^*_{\min}$ ($c \le c^*_{\min}$), a void will appear [21]. Conversely, when the normalized atomic density c is greater than or equal to $c^*_{\max}$ ($c \ge c^*_{\max}$), a hillock will be generated. For the solder material, a criterion for void generation is selected to be $c^*_{\min} = 0.85$. The work in this section can show the location of hillock, but it has not yet considered the formation of a hillock. In the simulation procedure of the void

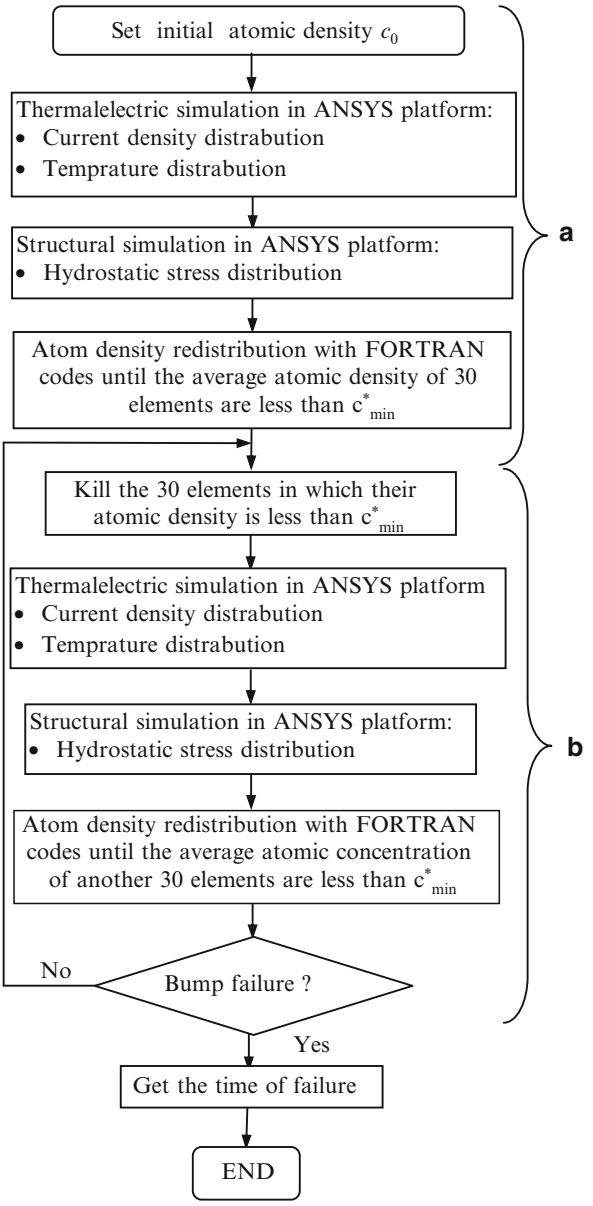


Fig. 12.52 Flow chart of EM failure simulation: (**a**) incubation period for void formation (**b**) growth period for void propagation

growth period, once the average atomic density value of the elements are less than the critical atomic density for void initiation c^*_{min}, the corresponding elements will be killed ("element death") and the structure need to be reconstructed. To achieve the "element death" effect, ANSYS do not actually remove "killed" elements.

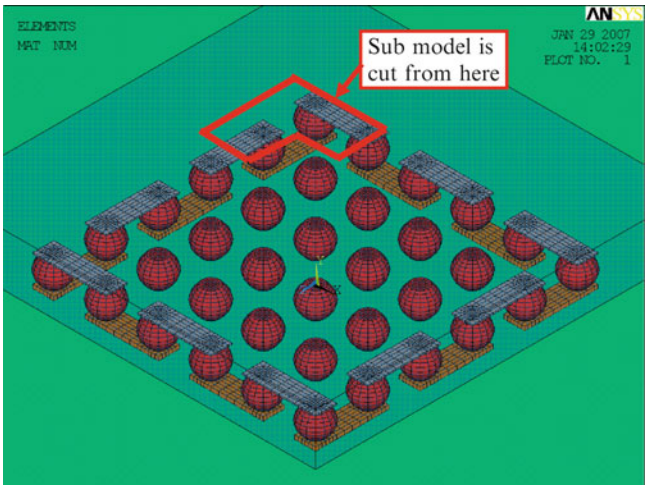


Fig. 12.53 WL-CSP package model

Instead, it deactivates them by reducing the element material attribute, such as the elastic modulus and resistivity, by a factor of 1.0E−6.

In the semiconductor industry for a WL-CSP bump failure criterion, a 15% increment in electrical resistance of the bump is usually considered EM failure. This criterion is used in this work to get the final TTF.

12.4.4 Numerical Examples

To correlate the new simulation methodology with the experimental data, a WL-CSP package from refs. [17, 29] is considered, which has 36 solder bumps with 500 μm pitch. The exterior 20 solder bumps are assumed to connect with each other in a daisy chain as shown in Fig. 12.53. The UBM on the silicon die side is the equivalent material parameters (Al/NI(V)/Cu) layer. The diameter of the solder joints is around 300 μm and the height is about 200 μm. The solder joints are encapsulated in the underfill between the silicon die and PCB.

A global WL-CSP with PCB is modeled using relative coarse mesh and a submodel is built with refined mesh as shown in Figs. 12.53 and 12.54, respectively.

Figure 12.55 shows the electron flow for the thermal-electric coupled field quarter model with 1.7 A current. The free convention boundary condition is applied with 17 W/m^2 °C film coefficient and 50°C ambient temperature.

Electromigration test is conducted in the WL-CSP package which uses both eutectic 63Sn37Pb and 95SnAg4.5Cu0.5 solder joints. The basic material parameters are selected from refs. [24–27] as listed in Table 12.12. The electromigration parameters of 63Sn37Pb and 95SnAg4.5Cu0.5 solder bump are selected from refs. [28–31] as shown in Table 12.13.

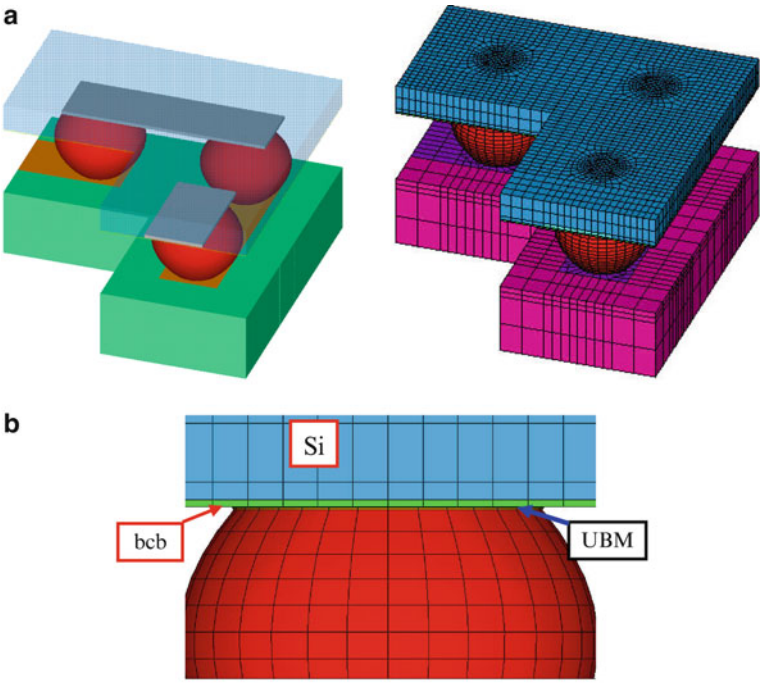


Fig. 12.54 Submodel of CSP package. (**a**) View of the *top right* of the model, (**b**) local view

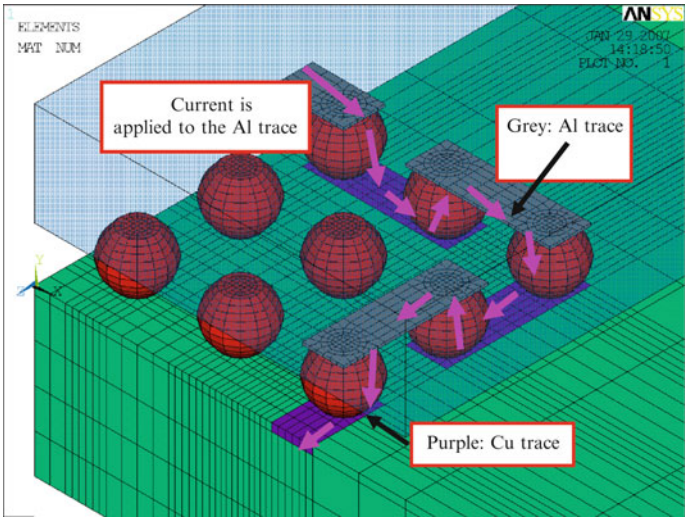


Fig. 12.55 Electron flow in a global model

Table 12.12 Material properties for numerical model

Material	Density (kg/m^3)	Specific heat (J/kg/K)	Elastic modulus (GPa)	Poisson's ratio
63Sn37Pb	8,420	150	30.8	0.4
SnAgCu	7,390	219	26.2	0.35
Al	2,710	902.1	69	0.33
Cu	8,900	385.2	127.7	0.31
Ni	8,900	443.8	200	0.31
BCB	1,050	2,180	2.9	0.34
Die	2,300	/	131	0.3
			25.4 (x, z), 11 (y)	0.39 (xy, yz)
PCB	1,900	/	4.971 (GXY, GYZ)	0.11 (xz)
			11.453 (GXZ)	

Material	CTE (1/K)	Thermal conductivity (W/m K)	Electrical resistivity (Ωm)
63Sn37Pb	24E−6	50	15.5E−8 (1 + 3E−3ΔT)
SnAgCu	23E−6	57.26	13.3E−8 (1 + 2.8E−3ΔT)
Al	23E−6	240	2.61E−8 (1 + 4.2E−3ΔT)
Cu	17.1E−6	393	1.58E−8 (1 + 4.3E−3ΔT)
Ni	13.4E−6	91	6.32E−7
BCB	52E−6	0.29	1E17
Die	2.8E−6	150	4.4
PCB	16E−6 (X, Z) 84E−6 (Y)	1.7	1E10

Table 12.13 EM parameters of SnPb and SnAgCu

Symbol	SnPb	SnAgCu
E_a (ev)	1	0.98
Z*	−33	−23
D_0 (m^2/s)	3.138E−05	4.1E−5
Q* (ev)	0.0094	0.0094
Ω (m^3/atom)	2.48E−29	2.71E−29
ρ (Ωm)	See Table 12.1	See Table 12.1

12.4.4.1 Multiphysics Coupled Simulation

A multiphysics simulation which includes electrical, thermal, and structure couple analysis is conducted firstly. Figure 12.56 shows the temperature gradient distribution of the viscoplastic SnPb and SnAgCu solder bump at corner under 1.7 A in a submodel. The maximum temperature gradient is 161.4 K/cm for SnAgCu and 193.4 K/cm for SnPb solder materials. While the criterion for thermal migration is 1,000 K/cm [32], therefore, both Pb and Pb free solder materials will not have the thermal migration. Figure 12.57 shows the current density distribution of the viscoplastic SnPb and SnAgCu solder bump under 1.7 A of a submodel. Figure 12.58 shows the hydrostatic stress distribution of the viscoplastic SnPb and SnAgCu corner solder bump under 1.7 A. The results show that the tensile stress of Pb solder bump is larger than the Pb-free solder at the edge of high current

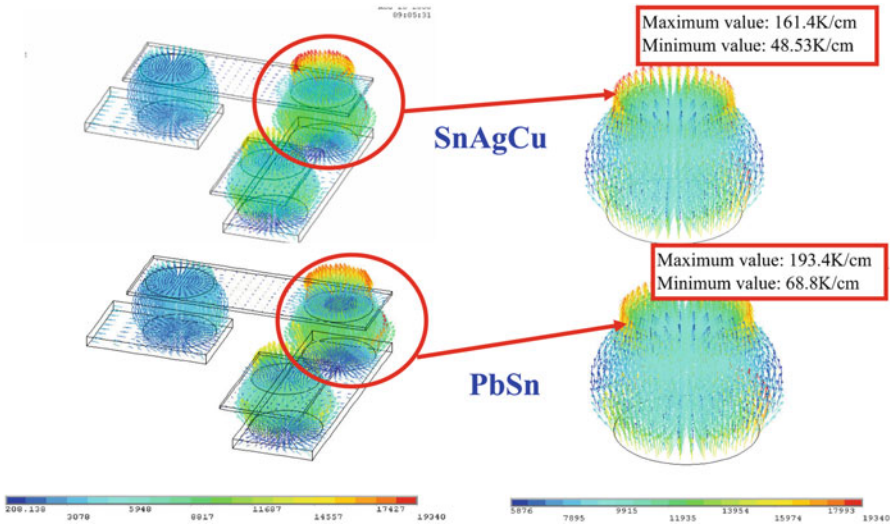


Fig. 12.56 Temperature gradient distribution of SnPb and SnAgCu corner solder bump under 1.7 A

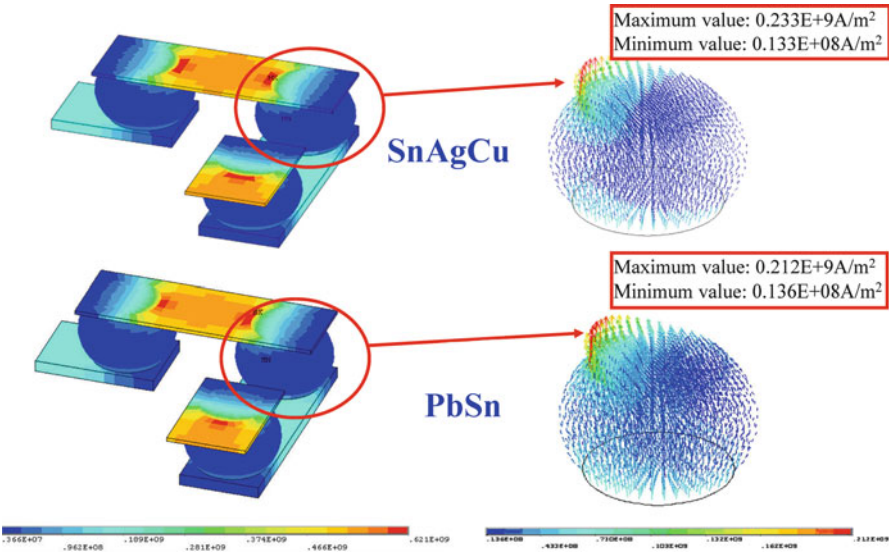


Fig. 12.57 Current density distribution of SnPb and SnAgCu corner solder bump under 1.7 A

density area. While the compressive stress of Pb-free solder bump is larger than the Pb material at the edge of the same section but opposite side. The later TTF simulation results will show that the TTF of Pb-free material is longer than the Pb material. This might indirectly indicate that the tensile stress will play the role to speed up the TTF, while the compressive stress will contribute to the longer TTF.

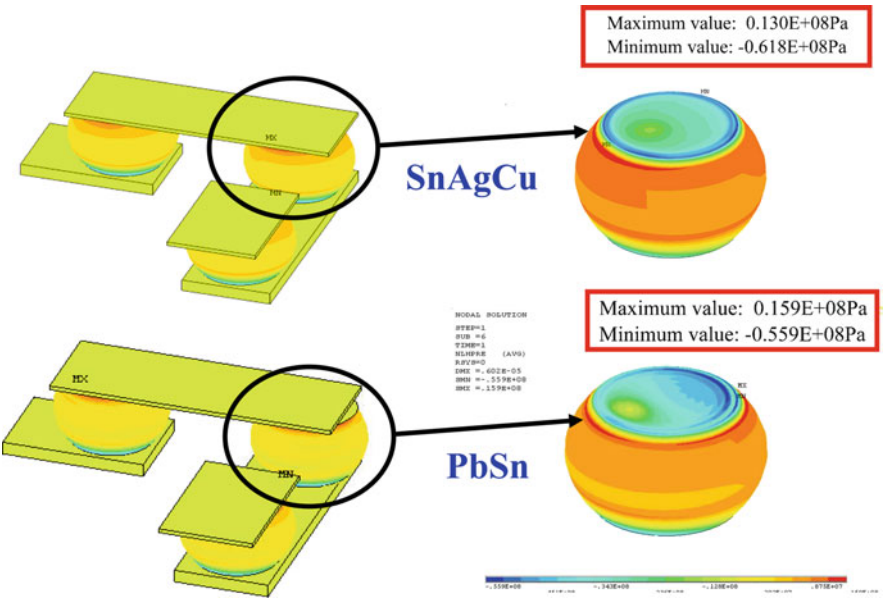


Fig. 12.58 Hydrostatic stress distribution of SnPb and SnAgCu corner solder bump under 1.7 A

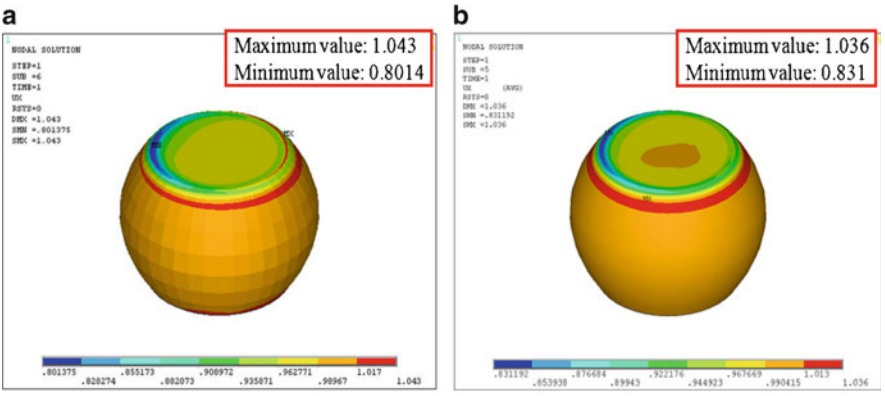


Fig. 12.59 Normalized atomic density distribution of the corner bump under 1.7 A at 3.5E + 5 s. (**a**) PbSn solder bump, (**b**) SnAgCu solder bump

Figure 12.59 shows the normalized atomic density distribution under 1.7 A at 3.5E5 s for the corner bump for both Pb and Pb-free materials. From Fig. 12.59, we can easily found the voids will begin to form at the interface between the UBM and the solder bump at the blue area because the atomic density has satisfied the voids generation criterion. The maximum atomic density of Pb-free solder material is larger than the Pb solder material. This means that the void in Pb solder material will be generated first because it will be faster to reach the void generation criterion.

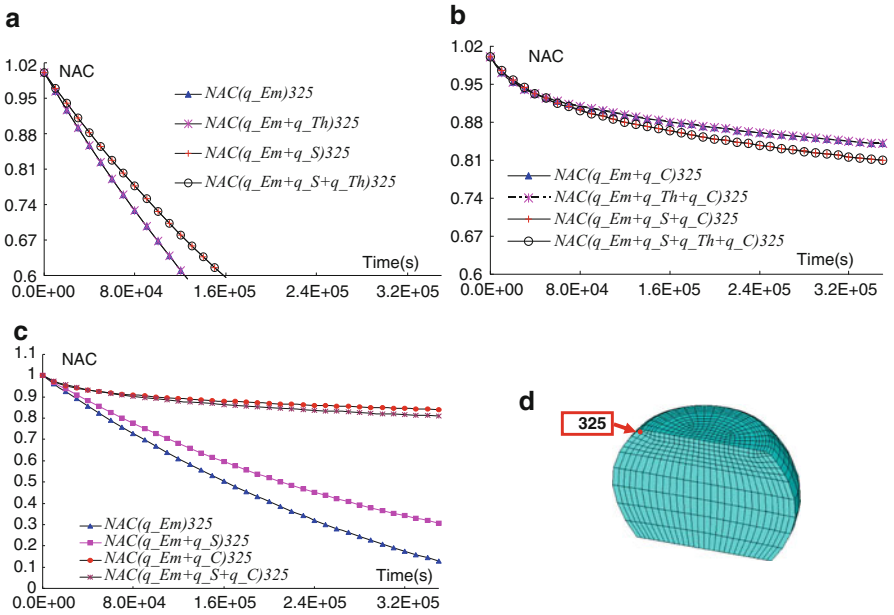


Fig. 12.60 Comparison of normalized atomic concentration (NAC) or density distribution with and without considering $\vec{q}_C$ at a examined node of the cross section of the corner solder bump. (**a**) Atomic density vs. time at node 325 without $\vec{q}_C$. (**b**) Atomic density vs. time at 325 with $\vec{q}_C$. (**c**) Comparison of atomic density with and without $\vec{q}_C$. (**d**) Examined node at the cross section of solder bump

To study the impact of EM with and without considering the ADG $\vec{q}_C$, we examined the normalized atomic density redistribution in a node (number 325) of solder bump cross section. Figure 12.60 shows the comparison of normalized atomic density distribution with and without considering $\vec{q}_C$ in a SnPb solder bump, where the examined node 325 is listed in Fig. 12.60d. Figure 12.60a gives the atomic density of node 325 varies as time without considering the ADG item. It can be seen that, without considering the ADG $\vec{q}_C$, the normalized atomic density decreases rapidly. The pure temperature gradient migration seems very small, almost no impact on the atomic density curve, while the stress gradient has significant impact on the atomic density curve. In Fig. 12.60b with consideration of $\vec{q}_C$, the normalized atomic density varies slowly with the time and it will reach a saturation value. Figure 12.60c combines the two cases with and without considering the ADG item. From Fig. 12.60c, it can be seen that the atomic density will be retarded due to the effect of ADG item $\vec{q}_C$ in the time-dependent EM evolution. This will delay the void generation and growth, and make the actual TTF be longer. Therefore, using the time-dependent EM evolution equation without considering $\vec{q}_C$ will underestimate the EM failure of the solder bumps. From Fig. 12.60c it may further observe that the impact rank order of the void generation is: EM $>$ ADGM $>$ SM $>$ TM.

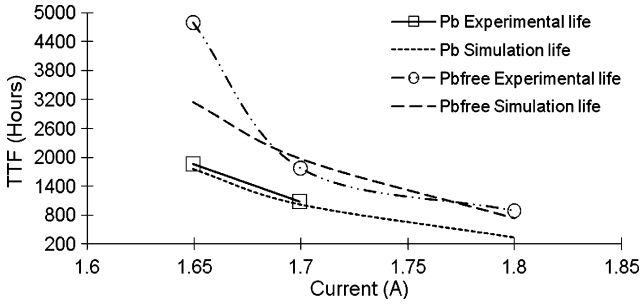


Fig. 12.61 TTF comparison between simulation and test result in ref. [29]

12.4.4.2 Simulation for Voids and TTF

Based on the modeling algorithm of EM induced void evolution (see Sect. 12.4.3.2), the voids and TTF of the solder bump of solder joint in a WL-CSP structure under high current density are simulated [33]. A comparison of the simulated results for TTF and the previous experimental test results obtained in ref. [29] is presented in Fig. 12.61. The results show that the two solder bump materials (Pb and Pb-free), both simulated TTF data agree well with the tested MTTF. There is some difference in the current of 1.65 A for the Pb-free material, and this might be either due to the modeling setting up and selected parameters need to be further validated or the error of the test system. From Fig. 12.61, it may clearly be seen that the Pb-free solder bump has the longer TTF than Pb solder material.

Figure 12.62 shows void shape and location comparison between simulation and test. From Fig. 12.62, we can see the void by simulation appears at the solder bump adjacent the UBM layer which is similar to the void and failure mode shown in the test [29].

Figure 12.63 gives the impact of UBM thicknesses with Pb and Pb-free solder materials. As the thickness increases, the TTF of solder bump increases. Again Fig. 12.63 has shown the TTF of Pb-free bump is higher than the Pb bump material.

Figure 12.64 gives the TTF with different rim angles of UBM for SnAgCu and SnPb. The simulation results show that the UBM geometry has a significant impact on the solder bump void growth and TTF. The 75° rim angle of UBM gets the longest the solder bump TTF, the 0° and the 90° rim angles of UBM are the poor structures to withstand the failure.

12.4.5 Discussion

A new predicted numerical simulation method for void generation and TTF in electromigration is developed in this section. The method has been implemented in the commercial software ANSYS Multiphysics in combined with a user defined

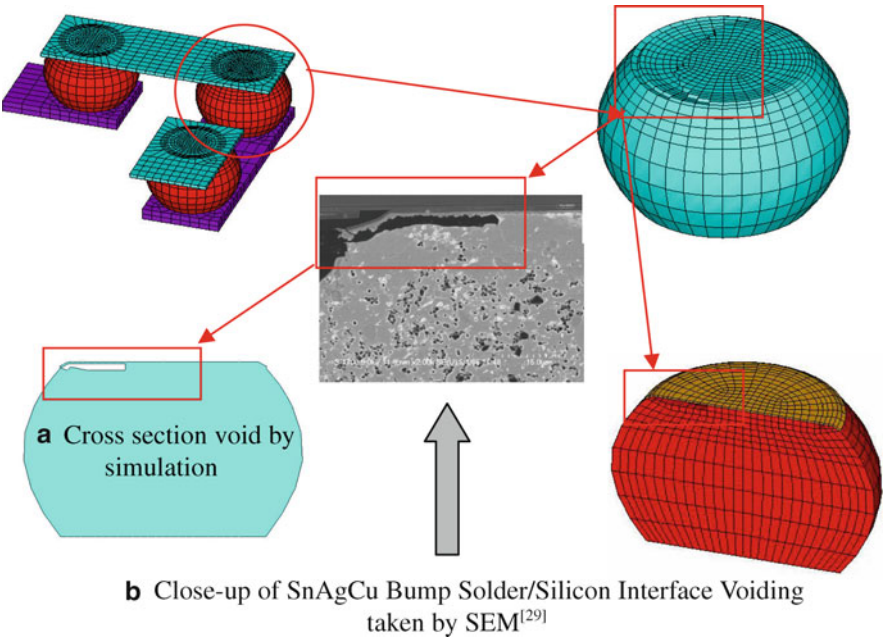


Fig. 12.62 Voids formation between simulation and test. (**a**) Cross section void by simulation. (**b**) Close-up of SnAgCu bump solder–silicon interface voiding taken by SEM [29]

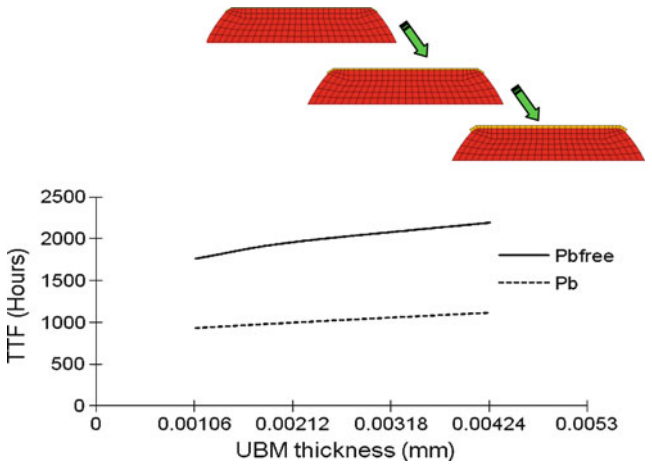


Fig. 12.63 TTF with different UBM thickness for SnAgCu and Pb materials

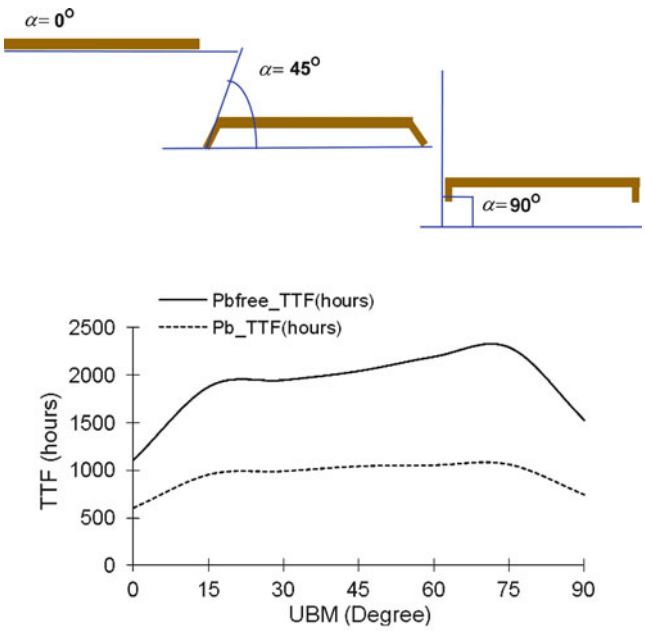


Fig. 12.64 Impact of Pb-free and Pb materials for TTF with different rim angles of UBM

FORTRAN code that computes the atomic density redistribution through a weighted residual finite element algorithm. The method is capable of calculating current density, joule heating, atomic density, and stress in the solder bump system of a WL-CSP. The atomic density distribution result can give the integrated effect of four types of migrations (EM, ADGM, SM, and TM) and the individual contribution of each item. It has been shown that the significant impact of the ADG, however, was often not considered in the past. Without consideration of the ADG, the TTF will be underestimated. The simulation further indicates that the impact on atomic density by pure temperature gradient is very small while the impact on atomic density by stress gradient is significant. The impact rank order on the void generation is EM > ADGM > SM > TM. Comparison of the TTF by the new predication method and the measured MTTF by previous studies has obtained good agreement.

The simulation results further show that the UBM geometry and bump shapes have significant impact on the solder bump void growth and the TTF. In the UBM geometry design, the 75° rim angle of UBM gets the longest solder bump TTF. A thicker UBM produces the longer bump TTF.

Note that in this section, there are challenges that need to be considered in the future work: We do not model the hillock formation; The simulation also does not include the dissolution of intermetallic compound (IMC) between UBM and solder material.

12.5 Summary

This chapter first introduces the electrical modeling methodologies of the power package for the extracting the self and mutual inductance, resistance, and the capacitors based on 3D models; the results are to be used to generate an electrical model of the package for use in spice simulation. Then, this chapter shows the defect impact on power package electrical performance, which includes impact of wire bonding-related defects and the die attach solder voids for the electrical resistance, inductance, and fusing current capability of the power packages. The electrical simulations are performed to extract the resistance and inductance of the package at different frequency levels. The fusing current analysis is conducted by using coupled thermal electrical simulations for the wire bonding defects. After that, this chapter discusses the UIL/UIS test and simulation. In power packages, the DC and AC test, the UIL or UIS test are important and critical for assurance of the robust product performance, quality, and reliability. Different MOSFET die top layer layouts and bond wires are analyzed and discussed through the fusing current test, UIL test, and electrical-thermal coupling simulation. Finally, the multiple physics modeling for electromigration in a power WL-CSP is given, which includes a new prediction method for electromigration induced void generation of solder bumps in a power WL-CSP. The methodology is developed based on discretized WRM in a user-defined FEA framework to solve the local electromigration governing equation with the variable of atomic concentration. The local solution of atomic concentration is incorporated in the multiphysics environment for electrical, thermal and stress in both submodel and global model. The new method takes the advantage of solving the variable of atomic density, and it avoids directly solving the divergences of the atomic flux, which includes the ADG items and is very hard and challenging to get the solution by traditional method. Comparison of the atomic density distributions with and without considering the ADG for representative nodes is investigated. The simulation results for voids and TTF are discussed and correlated with previous test results. The impact of parameters of UBM on the void generation and TTF is presented finally.

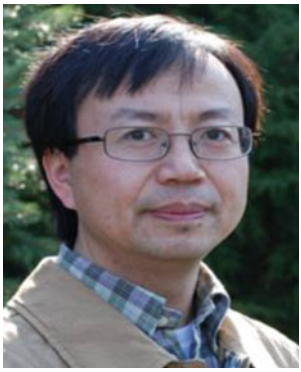
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