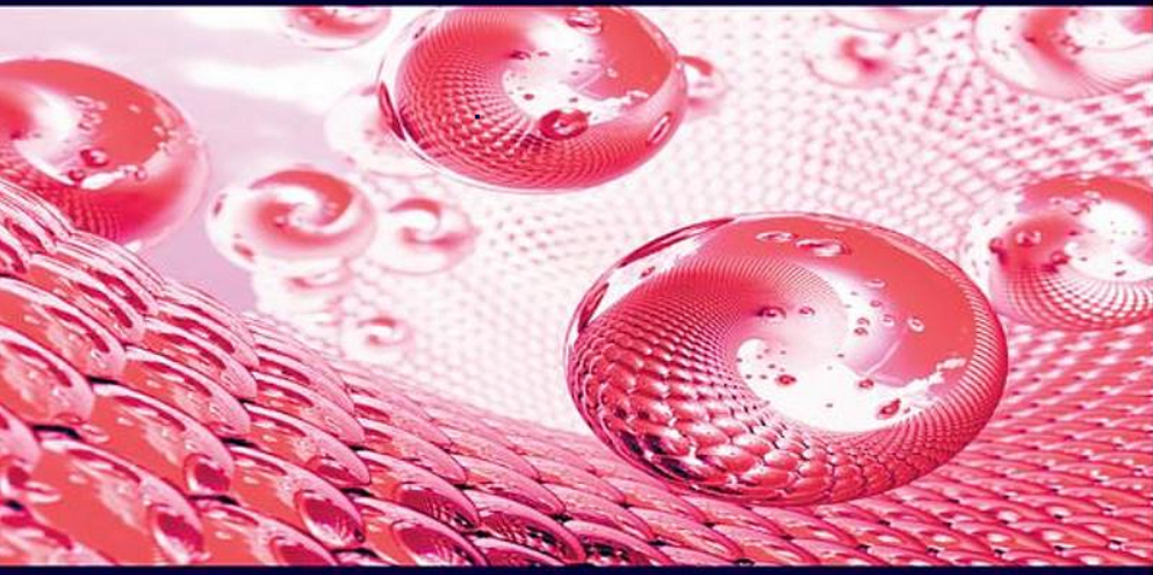
NANOSCIENCE AND NANOTECHNOLOGY SERIES



Beyond-CMOS Nanodevices 2

Edited by
Francis Balestra

ISTE

WILEY

Beyond-CMOS Nanodevices 2

Series Editor
Mireille Mouis

Beyond-CMOS Nanodevices 2

Edited by

Francis Balestra

ISTE

WILEY

First published 2014 in Great Britain and the United States by ISTE Ltd and John Wiley & Sons, Inc.

ISTE Ltd
27-37 St George's Road
London SW19 4EU
UK

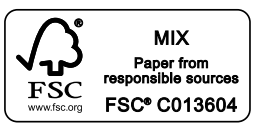
www.iste.co.uk

John Wiley & Sons, Inc.
111 River Street
Hoboken, NJ 07030
USA

www.wiley.com

Library of Congress Control Number: 2014935738

British Library Cataloguing-in-Publication Data
A CIP record for this book is available from the British Library
ISBN 978-1-84821-655-6



Printed and bound in Great Britain by CPI Group (UK) Ltd., Croydon, Surrey CR0 4YY

Contents

Acknowledgments

We would like to thank all the Partners of the FP7 Nanosil and Nanofunction Networks of Excellence supported by the European Commission and the Members of the European Sinano Institute (www.sinano.eu) for their contributions to these research activities, and Pascale Caulier (Sinano) for her contribution to the realization of this book and “Beyond-CMOS Nanodevices 1”.

General Introduction

Microelectronics, based on complementary metal–oxide semiconductor (CMOS) technology, is the essential hardware enabler for electronic product and service innovation in key growth markets, such as communications, computing, consumer electronics, automotives, avionics, automated manufacturing, health and the environment. The global semiconductor industry underpins 16% of the world's total economy and is growing every year. The worldwide market for electronic products is estimated to be more than $1,800 billion, and the related electronics services market more than $6,500 billion. These product and service markets are made possible by a $310 billion market for semiconductor components and an associated $90 billion market for semiconductor equipment and materials. The new era of nanoelectronics, which started at the beginning of the current millennium with the smallest patterns in state-of-the-art silicon-based devices below 100 nm, is making an exponential increase in system complexity and functionality possible.

Nanoelectronics allows the development of smart electronic systems by switching, storing, monitoring, receiving and transmitting information. In respect to its societal relevance, the ubiquitous nanoelectronics is also closely linked to the notion of ambient intelligence, which is a vision of the future where people are surrounded by intelligent intuitive interfaces that are embedded in all kinds of objects and an environment that is capable of recognizing and responding to the presence of different individuals in a seamless way.

Since the invention of the transistor in 1947 at Bell Labs, followed by the first silicon transistor in 1954 and the concept of integrated circuits in 1958

at Texas Instruments, progress in the field of microelectronics has been tremendous, which has revolutionized society. In these last 50 years, dramatic advances have been achieved in the packing density of transistors. This has resulted in the density of transistors on an integrated chip (IC) doubling every two years (Moore's law) since the 1970s. At the beginning of the 1970s, the first microprocessor had only about 2,000 transistors (10 μm gate length), the world's first two-billion transistor processor was reported in 2008 in 65 nm CMOS technology.

The same trend can be observed for memories. The dynamic random access memory (DRAM) capacity has been raised from 1 kb in 1970 to several Gb at present. Several billion transistor static random access memory (SRAM) chips have also been realized. For nonvolatile memories, 256 Gb have been demonstrated. This increase in transistor count and memory capacity has led to increased processing power, measured now in thousands of millions of instructions per second (MIPS).

Moore's law also means decreasing cost per function, the transistor price has dropped at an average rate of about 1.5 per year (about 108 since the beginning of the semiconductor industry).

However, according to the International Technology Roadmap for Semiconductors and ENIAC Strategic Research Agenda, there are big challenges to overcome in order to continue progressing in the same direction.

The minimum critical feature size of the elementary nanoelectronic devices (physical gate length of the transistors) will drop into the sub-decananometer range in the next decade. In the sub-10 nm range, "beyond-CMOS" devices, based on nanowires, nanodots, carbon electronics or other nanodevices, will certainly play an important role and could be integrated onto CMOS platforms in order to pursue integration down to nanometer structures. Silicon (Si) will remain the main semiconductor material for the foreseeable future, but the required performance improvements for the end of the roadmap for high performance, low and ultra-low power applications will lead to a substantial enlargement of the number of new materials, technologies, device and circuit architectures.

Therefore, new generations of Nanoelectronic ICs present increasingly formidable multidisciplinary challenges at the most fundamental level (novel materials, new physical phenomena, ultimate technological processes, novel design techniques, etc.).

In this timeframe, performance will also derive from heterogeneity, referring to the increasing diversity of functions integrated onto CMOS platforms as envisaged in the "More than Moore (MtM)" approach.

This book, and the related book *Beyond-CMOS Nanodevices 1* (Volume 1), also published by ISTE and Wiley offer a comprehensive review of the state-of-the-art in innovative Beyond-CMOS nanodevices for developing novel functionalities, logic and memories dedicated to researchers, engineers and students.

Volume 1 particularly focuses on the interest of nanostructures and nanodevices (nanowires, small slope switches, 2D layers, nanostructured materials, etc.) for advanced MtM (RF, nanosensors, energy harvesters, on-chip electronic cooling, etc.). This book focuses on beyond-CMOS logic and memory applications.

MtM functions allow the world of digital computing and data storage to interact with the real world. MtM devices typically provide conversion of non-digital as well as non-electronic information, such as mechanical, thermal, acoustic, chemical, optical and biomedical functions, to digital data and vice versa. Clearly MtM technologies and products provide essential functional enrichment to the digital CMOS-based mainstream semiconductors. MtM has become one of the major innovation drivers for a very broad spectrum of societally relevant applications.

There has been increased interest recently for using nanoscale beyond-CMOS devices in the More Moore and MtM domains:

– miniaturization remains a major enabler for price reduction, functionality multiplication and integration with electronics;

– the CMOS technology is facing dramatic challenges for future low power, high performance and memory applications;

– nanoscale beyond-CMOS structures can improve devices' intrinsic performance and enable new functionalities.

Nanotechnologies will also offer powerful ways to bring added value, in terms of cost, reproducibility, sensitivity, automation, analysis and new functionality in healthcare applications such as *in vitro* diagnostics or drug delivery, as well as in environment control (water, air, soil), agriculture and food, transport monitoring, ambient intelligence, defense or homeland

security. A wide range of sensor types will be required, such as biochemical sensors, sensors for liquid and gas spectroscopy.

As a very good example, nanowires have received much attention from the R&D community as components for electrical circuits based on CMOS compatible processes. Although the R&D activities for nanowires were initiated to address the future need of IC technologies beyond the physical limits of CMOS, more and more R&D activity nowadays is devoted to using nanowires to create innovative MtM products.

Other fields in which nanostructured materials and nanodevices could be of great interest are in the domain of energy-autonomous systems using energy harvesting, for wireless sensor networks, *in situ* monitoring for mobile systems, body-area networks, biomedical devices or mobile electronics; these systems will become very important in the future for the development of "green/sustainable" applications.

The integration of many different types of devices will be needed – for example, bio-sensors, nanoelectro mechanical structure (NEMS) devices, nanocomponents for logic and memory, energy scavenging systems and RF interfaces, for the development of these future nanoelectronics systems.

This book, and Volume 1, are thus reviewing innovative nanoscale structures that can improve performance and/or enable new functionalities in future terascale ICs and nanosystems. The convergence of More Moore and beyond-CMOS, on one hand, and the merging of MtM and beyond-CMOS, on the other hand, have been extensively studied in scientific literature these last years. The two books are offering a detailed overview of the most recent advances in these fields which have gained strong momentum for many applications.

In the MtM field, very sensitive nanosensors for biological and chemical products, mechanical, solar, thermoelectric energy harvesters, localized cooling on a chip with management of heat transfer using nanostructures and high performance, small size, low cost RF passive components using nanodevices or nanostructured materials are highlighted.

In order to develop future autonomous nanosystems, which will be needed for many applications of high industrial and societal relevance (monitoring of health and environment, internet of things, etc.), the main

challenges are the development of CMOS-compatible technologies and using mainly "green" materials, the reduction of the energy consumption of sensors, computing and RF communication, together with the increase in the energy harvested from the environment.

This book, and Volume 1, have been written by scientists from universities and research centers, strongly involved in teaching and research programs related to nanoelectronic devices and circuits. Because of their expertise and international commitment, they are very well informed on the state-of-the-art of the physics and technologies and the evolution of nanoelectronic materials, components, circuits and systems.

Part 1, Volume 1, reviews the nanosensing field, including Si nanowire: biochemical sensors, fabrication of nanowires, functionalization techniques, sensitivity, integration of SiNWs with CMOS, and portable system for real-time impedimetric measurements on nanowires biosensors.

Part 2, Volume 1, outlines new materials, nanodevices and technologies for energy harvesting, dedicated to vibrational energy harvesting (piezoelectric and electromagnetic energy transducers), thermal energy harvesting (thermal transport at nanoscale, porous silicon for thermal insulation on silicon wafers, spin dependent thermoelectric effects, composites of thermal shape memory alloy and piezoelectric materials), Nanowire based solar cells, and smart energy management and conversion (power management solutions for energy harvesting devices, sub-mW energy storage solutions).

Part 3, Volume 1, highlights on-chip electronic cooling, including silicon based cooling elements (Schottky barrier junctions, strained silicon Schottky barrier mK coolers, silicon mK coolers with an oxide barrier, silicon cold electron bolometer, integration of detector and electronics), thermal isolation through nanostructuring (lattice cooling by physical nanostructuring, porous silicon platforms, crystalline membrane platforms) and tunnel junction electronic coolers.

Part 4, Volume 1, addresses new materials, nanodevices and technologies for RF applications, devoted to substrate technologies for silicon-integrated RF and mm-wave passives, metal nanolines and antennas for RF and

mm-wave applications, and nanostructured magnetic materials (nano-composite materials, nanomodulated continuous films) for high frequency applications.

This volume gives an overview of beyond-CMOS nanodevices for logic and memories applications, including small slope switches (tunnel field effect transistor (FET), ferroelectric gate FET, NEMS), nanowires (ultimate CMOS, ultimate memories with new solutions offered by nanowire technologies in terms of charge storage and resistive change types), 2D layers and devices for More Moore and MtM (graphene and other 2D materials).

Francis BALESTRA
April 2014

Introduction to Volume 2: Silicon Nanowire Bio-Chemical Sensors

Volume 2 gives an overview of beyond complementary metal oxide semiconductor (CMOS) nanodevices for logic and memories applications, including small slope switches (Tunnel field effect transistor (FET), Ferroelectric (Fe) gate FET and Nano-Electro-Mechanical-Structures (NEMS)), Nanowires (NWs) (Ultimate CMOS, NanoCMOS Ultimate Memories) and two-dimensional (2D) layers and devices for More Moore and More-than-Moore (graphene and other 2D materials).

Chapter 1, Volume 2 addresses the dramatic challenges associated with accelerated energy consumption and heating, and the move from a constant field toward a near constant voltage scaling. Indeed, in 2005, the increase in microprocessor frequency abruptly ceased, but the integration level continued to increase and parallel processors were proposed. Thus, today we are facing dramatic challenges dealing with the limits of energy consumption (static + dynamic) and heat removal, inducing fundamental trade-offs for the future integrated circuits (ICs). The researches on ultimate reduction of computation dissipation are strongly needed for the development of future high-performance terascale integration and autonomous (nano) systems. The introduction reviews the main challenges, limits and possible solutions for strongly reducing the energy per binary switching. Several paths are possible: the adiabatic logic using a slow clock, logic stochastic resonance, feedback-controlled dynamic gate, nanoelectromechanical switches or conventional logic with a reduction in the stored energy, therefore, a

---

Introduction written by Francis BALESTRA.

decrease of device capacitance C (device integration) or applied bias V_{dd}, which seem to be the most promising for future ICs.

Indeed, the reduction of the stored energy in conventional logic can be done with a strong reduction in V_{dd} using new physics and/or devices with sub-60 mV/dec subthreshold swing S, in particular with the main following concepts: energy filtering (Tunnel FET, with metal-oxide-semiconductor (MOS)-NW-CNT or graphene, using band-to-band tunneling to filter energy distribution of electrons in the source, or NW FET with superlattice (e.g. InGaAs-InAlAs) hetererostructure in the source), internal voltage step-up (Ferroelectric gate FET, inducing a negative capacitance to amplify the change in channel potential induced by the gate), NEMS, or Impact Ionization MOS devices.

We will focus here on the best ones, Tunnel FETs, Fe FETs and NEMS, which could lead to ultrashort channel devices with a strong reduction of the applied bias, together with very good performance and reliability.

Chapter 2, Volume 2 will be devoted to Silicon-based NW metal-oxide-semiconductor field effect transistors (MOSFETs), which are recognized as one of the most promising candidates to extend Moore's law into nanoelectronics era. Both the top–down and the bottom–up approaches are widely studied for the fabrication of NW MOSFET transistors. We will give some highlights of silicon NW MOSFET both in terms of fabrication challenges based on top-down approach, which is probably today the most commonly investigated option by the microelectronic industry and in terms of quantum simulation and electrical characterization issues.

Moreover, semiconductor memories are electronic data storage devices based on MOS technology. There are various types of semiconductor memories that can be grouped into two basic categories: (1) volatile memory that requires power to retain the data content such as Dynamic Random-Access Memory (DRAM) and Static Random-Access Memory (SRAM) and (2) non-volatile memory (NVM), which is able to retain stored information even without power such as floating-gate memory. We will focus on the new solutions for NVM technologies offered by NW technologies in terms of both charge storage and resistive change types.

Chapter 3, Volume 2 will review the current status of graphene and other 2D transistors as potential supplement to silicon CMOS technology, for

More Moore and More-Than-Moore applications. An overview of graphene manufacturing and metrology methods is followed by a discussion of macroscopic and nanoribbon graphene FETs. Graphene FETs are shown to be of interest for analog radio frequency applications. Recent discoveries of non-classic switching mechanisms or tunneling-based devices may eventually lead to a cointegration of graphene into silicon technology.

Chapter 4, Volume 2 gives an overview of the use of NEMS for small slope switches. NEMS-based technology may be considered as a long term solution for ultralow power electronics. This chapter investigates the nanorelay principles, the logic operation being performed by the control of a movable structure. The switch is composed of an actuation mechanism and a mechanical contact. Four mechanisms are considered for actuation: the electrostatic actuation, the piezoelectrical actuation, the magnetic actuation and the thermal actuation. The technology challenges for NEMS computing are also addressed. Two challenges are identified: the low voltage operation in order to reduce the active power and the reliability of electrical contacts. Finally, the NEMS-based architectures, conventional and adiabatic, are discussed.

1

Small Slope Switches

1.1. Introduction

Power dissipation in switching devices is considered today as the most important roadblock for future nanoelectronic circuits and systems [SAK 04]. The complementary metal-oxide-semiconductor (CMOS) power consumption consists of two contributions: the dynamic and the static leakage components. In the past, the power increase was due to the different scaling factors for the voltage supply and the device geometry being essentially dominated by the dynamic power. Added to the dynamic power, there is an additional power component, the subthreshold leakage, which starts to dominate for advanced technology nodes and practically limits the supply voltage of modern integrated chip (IC) to a lower limit of 0.5 V. As the technology nodes scale, we have to use a lower supply voltage and, as the threshold voltages are reduced, the leakage or off current, I_{off}, becomes dominant because the subthreshold swing, S, of a *metal-oxide-semiconductor field-effect transistor* (MOSFET) is unscalable and tied to the thermal value of 60 mV/decade at room temperature [GOP 05]. This refers to the gate voltage required to change the drain current by one order of magnitude when the transistor is operated in subthreshold and is defined by

$$\text{SS} = \frac{\partial V_g}{\partial(\log I_d)} = \underbrace{\frac{\partial V_g}{\partial \psi_s}}_{\text{m}} \underbrace{\frac{\partial \Psi_s}{\partial(\log I_D)}}_{\text{n}} = \left(1 + \frac{C_{\text{d}}}{C_{\text{ox}}}\right)\frac{kT}{q}\ln 10 \qquad [1.1]$$

Chapter written by Adrian M. IONESCU, Francis BALESTRA, Kathy BOUCART, Giovanni SALVATORE and Alexandru RUSU.

Beyond-CMOS Nanodevices 2, First Edition. Edited by Francis Balestra.

where Ψ_S is the surface potential, V_g is the gate voltage, kT/q is the thermal voltage and C_d and C_{ox} are the depletion and the oxide capacitance, respectively. The subthreshold leakage problem cannot be solved by any advanced engineering if we rely on the MOSFET principle. Various device solutions have been proposed to reduce the m and n factors of equation [1.1] below their fundamental thermal limits of 1 and $\ln 10 kT/q$, respectively. Here, subthermal is what we call the values of the subthreshold swing less than kT/q ln10 (e.g. less than 60 mV/dec at room temperature, $T = 300$ K). A subthermal subthreshold swing by reducing the n factor involves the modification of the conduction or carrier injection mechanism; impact ionization [CHE 08] and quantum mechanical band-to-band tunneling (BTBT) mechanism have been proposed [BOU 09a, QUI 78] as major solutions. Recently, tunnel field effect transistor (FETs) [QUI 78, BAN 87, TAK 88, BAB 92] exploiting BTBT have emerged as candidates for ultralow standby power switches. However, one major drawback of tunnel FETs is their intrinsically low on-current capability, which is in best case one-to-two order of magnitude less compared to silicon nano-CMOS.

Another solution to lower S is to reduce below 1 the body factor, m, in equation [1.1]. This can be achieved by using the recently proposed negative capacitance effect [RED 95, KOG 96, HAN 00] or by using electromechanical gates [AYD 04] (with a movable electrode) where instability points between electrical and mechanical forces are used to define infinitely abrupt transitions between off and on states in micro/nanoelectromechanical (M/NEM) relays.

1.2. Tunnel FETs[1]

Compared to other steep slope devices, tunnel FETs seem today the most promising abrupt switches; they do not suffer from the reliability problems such as the impact ionization abrupt switches, I-MOS and the nanoelectromechanical (NEM) relays. Moreover, in both I-MOS and NEM relay, the voltage scaling below 1 V is extremely challenging, being limited not only by the device engineering but also by their fundamental physics.

The basic design of tunnel FET is a gated p-i-n diode where the band-to-band tunneling takes place between the intrinsic and p+ regions, for n-type

1 Section written by Kathy BOUCART, Adrian M. IONESCU and Francis BALESTRA.

devices (see Figure 1.1). To operate tunnel FET devices, the p-i-n diode is reverse-biased (for the energy band simulations reported in Figure 1.1, the source is grounded and positive voltages are applied to the drain and to the gate). With a zero gate voltage, the width of the energy barrier between the intrinsic region and the p+ region is wide (larger than 10 nm, one approximate minimum usually adopted for defining the limit of a significant tunneling probability), and the device is in the OFF-state. As the positive gate voltage increases, the bands in the intrinsic region are pushed down in energy, narrowing the tunneling barrier and allowing tunneling current to flow.

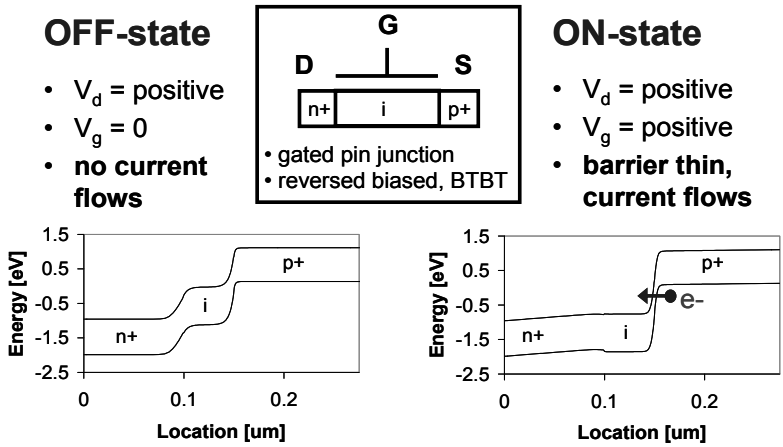


Figure 1.1. *Principle of tunnel FET and corresponding energy band diagrams in OFF and ON states with their control by the gate voltage*

The tunnel MOSFET offers an appealing concept for a substantial lowering of the energy dissipated in a switching device by replacing the thermionic emission of charge carriers over a barrier to enter the MOSFET channel with a tunneling process. If the tunneling process is made sufficiently effective, tunnel FETs can ultimately yield an effective cooling of the injecting source contact through a band-pass filter action that enables steep inverse subthreshold slopes over many orders of magnitude, thus providing low values of the average subthreshold swing, SS_{avg}.

Some of the first-tunnel FETs were proposed in 1978 followed by a small number of subsequent publications dealing with silicon and III–V surface tunnel transistors. Since approximately 2000, the field has been rapidly

evolving and, recently, tunnel FETs have attracted an increasing amount of interest due to their potential ability to enable switching with an inverse subthreshold slope steeper than 60 mV/dec. The following list of categories shows the most important contributions to the field and the present state-of-the-art of tunnel FETs.

First, realizations of interband tunneling transistors.– Quinn *et al.* at Brown University [QUI 78], were the first to propose the gated p-i-n structure of a Tunnel FET in 1978, and suggested the usefulness of this device for spectroscopy. Banerjee *et al.* [BAN 87] studied the behavior of a three-terminal silicon tunnel device, and Takeda *et al.* [TAK 88] showed the lack of VT roll-off when scaling. Baba fabricated tunnel FETs, which he called surface tunnel transistors in III–V materials [BAB 92]. In 1995, Reddick and Amaratunga published measured characteristics of silicon surface tunnel transistors [RED 95]. In 1997, Koga and Toriumi proposed a post-CMOS three-terminal forward-biased silicon tunneling device [KOG 96]. In 2000, Hansch *et al.* reported experimental results from a reverse-biased vertical silicon tunneling transistor made with MBE with a highly-doped boron delta-layer and noted the saturation behavior in the ID-VG characteristics [HAN 00]. Aydin *et al.* fabricated Lateral Interband Tunneling Transistors on silicon-on-insulator (SOI) in 2004 [AYD 04]. These devices were like tunnel FETs with no intrinsic region and the gate over a p-n junction, aiming to reduce gate capacitance and therefore increase speed. As a particular feature, the authors claim that there should be no current saturation for these devices.

Tunnel FETs in the Si/SiGe material system.– In 2004, Bhuwalka *et al.* published the first of many articles about their vertical tunnel FET on silicon with a SiGe delta layer, grown by MBE [BHU 04]. The SiGe replaced the silicon delta layer already used by Hansch, and, in theory, the smaller bandgap reduces the tunnel barrier width and increases tunneling current in the on-state as well as lowering the subthreshold swing. In 2006, the same group proposed a lateral tunnel FET on SiGe-on-insulator, and showed through simulation that on-current would increase with the percentage of Ge in the SiGe [BHU 06].

In 2007, Boucart and Ionescu showed the first comprehensive numerical simulations of Si tunnel FETs with a high-k gate dielectric and double-gate structure [BOU 07a]. The better capacitive control of the tunnel junction improves both the on-current and the subthreshold swing. The same authors

also presented a method of threshold voltage extraction for tunnel FETs that has a physical basis (related to the saturation of the energy tunneling barrier), demonstrated a second threshold voltage in relation to the drain [BOU 07b], and showed that tunnel FETs have the potential for high gain at low applied voltages. The second threshold voltage was shown to be caused by drain-induced-barrier-thinning due to the p-i-n structure of tunnel FETs.

In 2008, Nayfeh *et al.* simulated and measured tunnel FETs with a strained SiGe channel layer and the drain on the n-type silicon substrate. Significantly improved device characteristics were obtained with increasing Ge content [NAY 09]. Also, in 2008, first experimental tunnel FETs in strained Ge [KRI 08] were demonstrated by Krishnamohan *et al.* that exhibited a point slope, i.e. an inverse subthreshold slope in a small-gate voltage range, of 50 mV/dec. In addition, Mayer *et al.* from CEA-LETI showed experimental results for silicon-, germanium- and SiGe-on-insulator and demonstrated an inverse subthreshold slope of 42 mV/dec in ultrathin body (UTB) SOI tunnel FETs for p-channel operation (Figure 1.2(a)) [MAY 08]. Using silicon-germanium on insulator (SGOI) and GOI TFETs, strong improvements of the driving current, between several hundreds and thousands, are obtained compared with SOI transistors (Figure 1.2(b)). I_{off} is very low but I_{on} is only of the order of several μA/μm for the best GOI TFETs [MAY 08].

Verhulst, *et al.* at IMEC studied the optimization of nanowire tunnel FETs by changing the source material to Ge [VER 08a]. The band discontinuity between Si and Ge leads to a significantly enlarged BTBT probability.

Boucart *et al.* from Ecole Polytechnique Fédérale de Lausanne (EPFL), in Switzerland, proposed a silicon-only tunnel FET with a lateral strain profile to decrease the bandgap at the tunnel junction and therefore improve device characteristics [BOU 09b]. Moselund *et al.* from IBM Zurich presented tunnel FETs on *in-situ* doped VLS grown silicon nanowires with different gate dielectric material [MOS 09]. Fully-depleted Ge tunnel FETs were investigated by Zhang *et al.*, first using simulations [ZHA 09]. More recently, experimental demonstrations of a heterostructure design for tunnel field effect transistors with two low-direct bandgap group IV compounds, GeSn and highly tensely strained Ge in combination with ternary SiGeSn alloy by Wirths *et al.,* have pushed forward the performance of these devices [WIR 13].

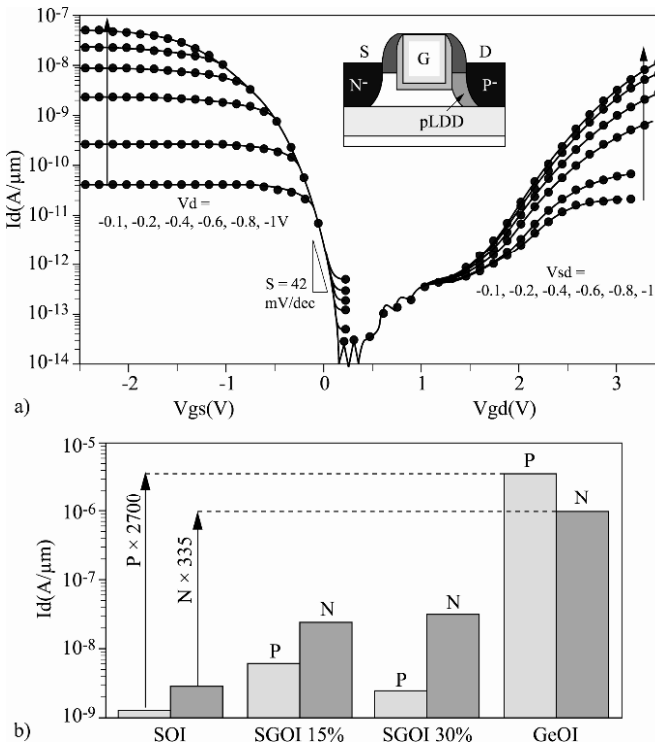


Figure 1.2. *a) Transfer $I_d(V_g)$ characteristics of 100 nm gate length n- and p-channel TFETs (t_{si} = 20 nm). b) I_{on} of 400 nm Lg SOI, SGOI and GOI n- and p-TFETs (t_{SiGe} = 20 nm, t_{Ge} = 60 nm, V_d = ±0.8 V, V_g = ±2 V)*

III–V and III–V hetero-junction tunnel FETs.– There are basically two different approaches for III/V based devices. The first approach is similar to the SiGe tunnel FETs, where the source consists of an SiGe alloy to decrease the effective bandgap and provide higher on-currents compared to an all-silicon tunnel FET. However, an SiGe-based source is only a solution for the n-type tunnel FET as pointed out by Verhulst *et al* [VER 08b]. For a p-type tunnel FET a device with III/V source was proposed enabling the realization of inverters etc. Suitable materials for such p-type tunnel FETs are, for instance, InAs and InxGa1-xAs, where the latter would be easier to fabricate due to the smaller lattice mismatch. InAs, having a smaller bandgap, would on the other hand bring higher on-currents. The main advantage of this type of tunnel FET is that both polarities can be implemented on silicon and would be CMOS compatible.

Several groups have investigated all III/V tunnel FETs by simulation in two main configurations. The simplest structure consists of a p-i-n structure in the same III/V material such as InAs [MOO 08, ZHA 08, LUI 09]. If doping profiles can be controlled, the authors report a better performance than both Si- and Ge-based tunnel FETs at low supply voltages (<0.5 V). Furthermore, both Ge and InAs based tunnel FETs show clear advantages in energy-delay-product and switching delay as VDD is scaled toward 0.25 V.

In 2009, Knoch investigated the use of III–V heterojunctions for tunnel FETs since they offer the possibility of studying the impact of staggered to broken band line-ups [KNO 09]. It was found that a broken band line-up yields an inverse subthreshold slope close to 60 mV/dec and a staggered line-up is beneficial for steep slope III–V devices.

For very short gate lengths Gate-All-Around InAs TFETs, small wire diameters are needed, down to 5 nm or below, in order to obtain a good subthreshold swing (Figure 1.3) [CON 11].

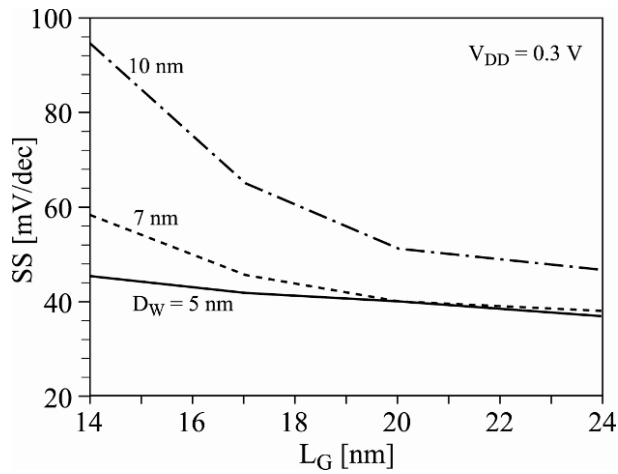


Figure 1.3. *Subthreshold swing versus gate length for GAA InAs nanowire TFETs for various wire diameters obtained by quantum simulation*

High performances, with I_{on} up to 1 mA/µm at low V_d, have been demonstrated by quantum transport simulation on strained InAs NW TFET (Figure 1.4), the best result being shown for a biaxial strain [CON 11].

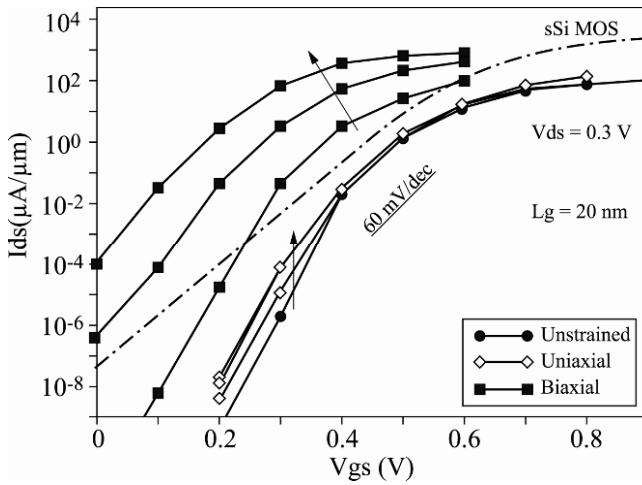


Figure 1.4. *20 nm gate length InAs NW TFET with 5 nm diameter and different strains obtained by quantum simulations*

However, the on-current improvements can be frustrated by the degradation of the swing in the presence of traps. Both traps and surface roughness can also be a relevant source of device variability for tunnel FETs [CON 12].

Tunnel FETs based on alternative materials.– The bandgap engineering exploiting other 1D and 2D materials attracted interest for alternative implementations of tunnel FETs. Employing a dual-gate carbon nanotube tunnel FET Appenzeller *et al.* demonstrated BTBT with an S = 40 mV/dec [APP 04]. The same group showed in another work, that in an optimized carbon nanotube tunnel FETs an S = 10 mV/dec would be possible [APP 05]. In 2006, Zhang from Stanford demonstrated an experimental carbon nanotube p-i-n tunnel transistor exhibiting a minimum inverse subthreshold slope of 25 mV/dec [ZHA 06]. In 2009, Koswatta *et al.* at Purdue University showed a comparison of tunnel FET and MOSFET performance, based on devices built on carbon nanotubes [KOS 09]. Poli *et al.* studied the ultimate scaling limits of carbon nanotube tunnel FETs [POL 08].

A comprehensive review of fabricated tunnel FETs and their experimental characteristics has been proposed by Seabaugh [SEA 10], concluding that their main promise is in their ability to provide higher drive

current than the MOSFET as supply voltages approach 0.1 V. His overview of experimental characteristics for p- and n-type tunnel FETs are reproduced in Figures 1.5(a) and (b), which also compared tunnel FETs with I-MOS switches. It has been concluded that a lot of progress in provided high on currents and steep subthreshold swings over many decades is still expected.

In addition to logic circuits, the application of TFETs in static random access memory (SRAM) has been reported [CHE 13]. SRAMs designs with CMOS and TFET technology using different transistor numbers (6T, 7T and 8T) were compared in terms of switching behavior, output characteristics and stability. An improvement of 700-fold leakage reduction was demonstrated using TFET over CMOS technology in silicon TFET SRAM [SIN 10].

Further attractive applications of TFETs are in analog integrated circuits such as ultralow-power voltage controlled oscillators or voltage references [MAL 12, FUL 08].

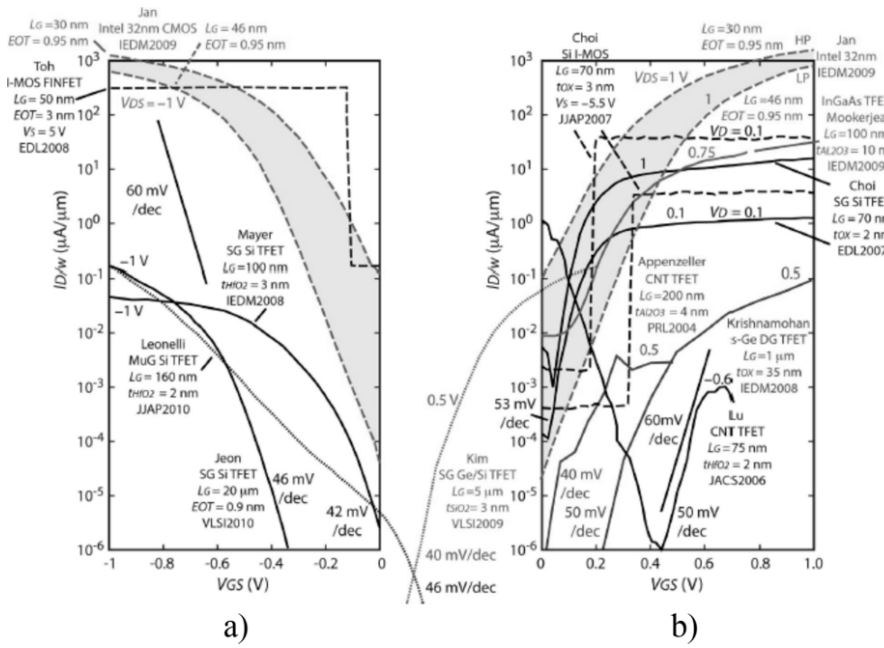


Figure 1.5. *Experimental Tunnel FET characteristics for a) p-type and b) n-type, as collected by Seabaugh [SEA 10] and their comparison with data on I-MOS switches (©2010 IEEE). For a color version of the figure, see www.iste.co.uk/balestra/nanodevices2.zip*

1.3. Ferroelectric gate FET[2]

Exploiting the ferroelectric polarization in the gate stack to control the inversion charge of a FET channel provides a uniquely compact one-transistor device with an active gate stack; to date many studies have been reported concerning memory applications. Sallahuddin *et al.* [SAL 08a] have proposed using ferroelectrics in order to exploit their unique nonlinear energy dependence on polarization to provide a negative capacitance effect. However, the difficulty in demonstrating the principle of negative capacitance experimentally is related to the fact that the exploited instability should be controlled (stabilized) by an in-series positive capacitance and, for defining an abrupt transition from off-to-on state, place the stabilized negative capacitance region in the subthreshold operation of the MOSFETs. First attempts to experimentally demonstrate such a ferroelectric abrupt switch (Fe-FET) were reported by Salvatore *et al.* [SAL 08b] and Rusu *et al.* [RUS 10]; the last report in particular can by far be considered the first experimental result of a sub-thermal swing at room temperature. A key advantage of the Fe-FET is that, in contrast to tunnel FETs, its on-current is as high as the one of a conventional MOSFET. In this chapter, we focus on the characteristics of metal-ferroelectric-metal-oxide-semiconductor structures recently reported by the EPFL group [SAL 08b, RUS 10] based on a complete set of experiments exploiting the internal metal contact.

Figure 1.6(a) depicts a three-dimensional (3D) view of the Fe-FET under investigation, exhibiting such a negative capacitance effect: it consists of a conventional silicon p-type MOSFET (made in a n-type well laterally isolated by Shallow-Trench-Isolation (STI) filled with silicon dioxide to minimize the leakage sources), with a 50 nm layer of P(VDF-TrFE) (70–30%) ferroelectric copolymer integrated in the gate stack. The poly(vinylidene fluoride/trifluoroethylene), P(VDF-TrFE), is a wide-bandgap semicrystalline polymer that was selected for our investigations because of its low temperature processing (annealing temperature less than 180°C), possibility to spin-coat very thin film on full wafers, low-leakage current and excellent ferroelectric properties in sub-100 nm layers [NAB 05]. At a VDF:TrFE ratio of about 70:30, this copolymer is ferroelectric [BRA 06] A particularity of this device is the 50 nm thin metal layer (AlSi) sandwiched between the ferroelectric and SiO_2, with a double

2 Section written by Adrian M. IONESCU, Giovanni SALVATORE and Alexandru RUSU.

role: (1) to act as a floating equipotential metal plane between the ferroelectric and the intrinsic MOS transistor gate and exploit in such a structure the negative susceptibility of multi-domain films governed by the electrostatic according to previous results of Bratkovsky [BRA 06] concerning ferroelectrics sandwiched between metal electrodes and, (2) to enable direct measurements on the internal voltage potential, V_{int}, by probing the potential of the internal metal layer with a high-impedance voltmeter (therefore investigate ferroelectric polarization in all regimes of operation).

From equation [1.1], the device design condition for achieving a sub-thermal swing is expressed in terms of the amplification of the surface potential, dΨS/dVg, or in terms of the body factor, *m*

$$0 < m = \left[\frac{d\Psi_S}{dV_g}\right]^{-1} = \left[\frac{d\Psi_S}{dV_{\text{int}}}\frac{dV_{\text{int}}}{dV_g}\right]^{-1} = \frac{1}{G}\left[\frac{d\Psi_S}{dV_{\text{int}}}\right]^{-1} = \\ = 1 + \frac{C_d(V_g)}{\dfrac{C_{ox}C_{ferro}(V_{ferro})}{C_{ox} + C_{ferro}(V_{ferro})}} < 1 \qquad [1.2]$$

where $G = dV_{int}/dV_g$ is the internal voltage gain, directly accessible by measurement in our Fe-FET structure with internal metal contact. If the ferroelectric capacitance is assumed negative, $C_{ferro} < 0$, and with $V_{ferro} = V_g - V_{int}$ the key design conditions for sub-thermal subthreshold swing due to a stabilized negative capacitance by in series C_{ox} and C_d, are

$$C_{MOS} = \frac{C_{ox}C_d(V_{\text{int}})}{C_{ox} + C_d(V_{\text{int}})} < -C_{ferro}(V_{ferro}) < C_{ox} \qquad [1.3]$$

Conditions [1.3] are difficult to simultaneously fulfill in practice because of the dependence of both C_d and C_{ferro} on the internal voltages and, for our device, also because of the process variability of the ferroelectric thickness. Fulfilling the conditions [1.3] in a limited range of gate voltage (subthreshold) operations of the Fe-FET results in hysteretic I_d–V_g characteristics with sub-thermal transitions limited to the regions where the internal voltage gain is achieved.

The negative capacitance condition can be written as function of the polarization, *P*, and the gain, *G*

$$C_{ferro} = \frac{dP}{dV_{ferro}} = \frac{dP}{d(V_g - V_{\text{int}})} = \frac{dP}{dV_{\text{int}}} \frac{G}{1-G} < 0 \qquad [1.4]$$

Therefore, an internal voltage amplification, $G > 1$, is directly linked to the existence of the negative capacitance effect, Figure 1.6(b)

Figure 1.6(c) shows a high-resolution TEM of the fabricated Au/P(VDF-TrFe)/AlSi/SiO_2 gate stack. Figure 1.6(d) is an AFM image of the deposited polymer layer showing a variability of the P(VDF-TrFE) topography in the order of 20 nm and an average thickness of 50 nm. The Fe-FETs reported here, have been designed so that their C_{ox}, C_{ferro} and C_{MOS} could verify conditions [1.3]..

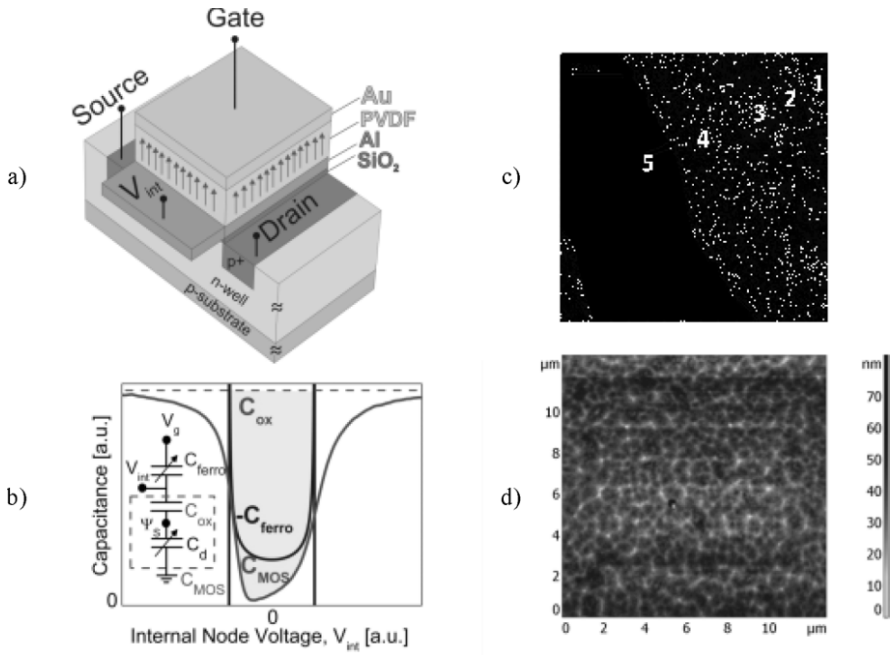


Figure 1.6. *a) Cross-section of the fabricated p-type metal-ferroelectric-metal-oxide semiconductor field effect transistor with internal gate contact, V_{int}, within an n-well and with STI isolation. b) Qualitative depiction of the conditions to be fulfilled by the gate stack capacitances for a sub-thermal subthreshold swing: CMOS < -C_{ferro} < C_{ox}, and illustration of the capacitive divider of the gate stack. c) TEM cross sectional image of the fabricated device: 1 = silicon substrate, 2 = silicon dioxide, 3 = aluminum, 4 = PVDF-TrFE, 5 = gold. The thickness variability of the PVDF-TrFe layer is clearly visible. d) AFM topography of the ferroelectric layer: the average thickness is ~50 nm while the variability is in the order of 20 nm. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices2.zip*

Figure 1.7(a) reports the I_d–V_g characteristics of the intrinsic MOSFET (with the gate bias directly applied on the internal contact, V_{int}) and the Fe-FET (with the gate bias applied on the top Au contact, V_g, and with the internal contact being left floating). As expected, the ferroelectric induces a voltage-controlled hysteresis in the current–voltage characteristics. Surprisingly, even if equivalent-oxide-thickness (EOT) of the Fe-FET using the full gate stack is significantly larger, the subthreshold swings in the "up" and "down" directions (indicated by arrows in Figure 1.7(a)) are not degraded in Figure 1.7(b). We observe that in the "down" direction, the swing of the Fe-FET is at the thermal limit of 60 mV/decade (this is the lowest ever reported/achieved thermal swing in a bulk silicon FET). Figure 1.7(c) reports the butterfly *C*–*V* characteristics, which are the typical signature of a ferroelectric gate stack, compared to the non-hysteretic quasi-static *C*–*V* characteristics of the internal transistor (using only SiO_2 as gate dielectric) measured on the same Fe-FET device. This figure shows an excellent correlation between the regions where the minimum of the subthreshold swings is observed and the low values of the gate stack capacitance, where the negative capacitance is fulfilled. Despite the noisy quasi-static *C*–*V*, in systematic experiments we observe some reversed peaks or locally flat values of the capacitance.

Figure 1.8 reports the unique experimental investigation enabled by the internal metal contact: the characteristics of the Fe-FET are measured while the V_{int} contact is probed with a high-impedance voltmeter configuration. A typical hysteretic dependence V_{int}–V_g is reported in Figure 1.8(a). Figure 1.8(b) shows that the highest peaks of the internal voltage gain, $G = dV_{int}/dV_g > 1$ are perfectly correlated with the minimum swing, which is lower compared to that of the intrinsic transistor (~80 mV/dec).

This is clear proof of the negative capacitance effect. The V_{int}–V_g plot permits the extraction of the ferroelectric polarization loop, *P*, versus the voltage drop on the ferroelectric, V_{ferro}, based on the following simple relation derived by the application of the Gauss law at the ferroelectric-SiO_2 interface

$$P = \left[\frac{(V_{int} - \Psi_S) k_{ox}}{t_{ox}} - \frac{V_g - V_{int}}{t_{Fe}} \right] \times \varepsilon_0 \qquad [1.5]$$

where Ψ_S is the MOSFET surface potential, k_{ox} is the relative permittivity of the SiO_2, ε_0 is the vacuum permittivity, and t_{ox} and t_{Fe} are the thicknesses of

oxide and ferroelectric layers, respectively. The surface potential $\Psi_S(V_{int})$ is calculated according to the full-analytical equation of a conventional MOSFET[11] from depletion to strong inversion. Figure 1.8(c) reports the resulting experimental minor loops, P–V_{ferro}.

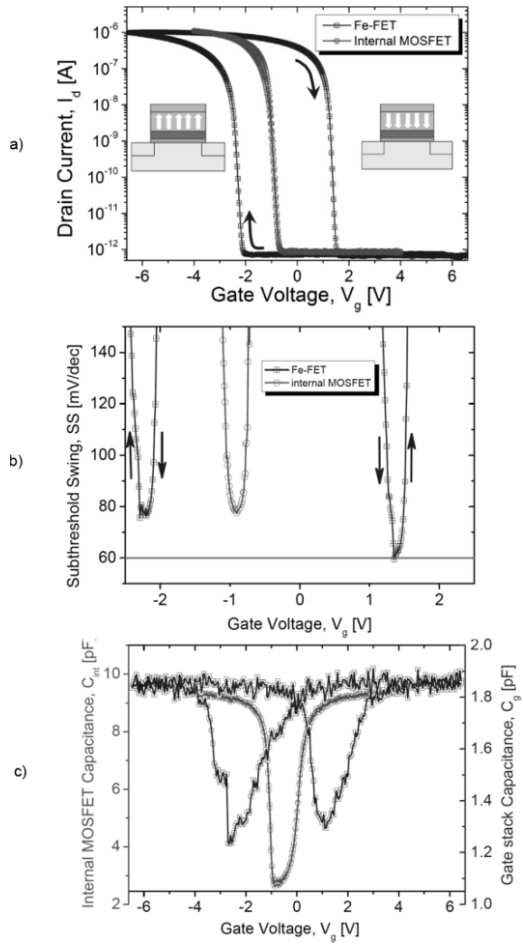


Figure 1.7. *a) Drain current, Id, versus gate voltage, Vg, characteristics of the Fe-FET (hysteretic) with metal-ferroelectric-metal-SiO_2 gate stack and of the internal MOSFET (non-hysteretic) using SiO_2 as gate dielectric, for V_d = 50 mV. The channel dimensions are: length = 50 μm and width = 20 μm. b) Calculated point subthreshold swings, SS, of the Fe-FET based on experimental data c) Quasi-static capacitances of the internal MOSFET, C_{int}, (circles) and of the ferroelectric gate stack, C_g, (squares) measured on the same device. All the measurements are performed with the internal metal contact floating (not connected). For a color version of the figure, see www.iste.co.uk/balestra/nanodevices2.zip*

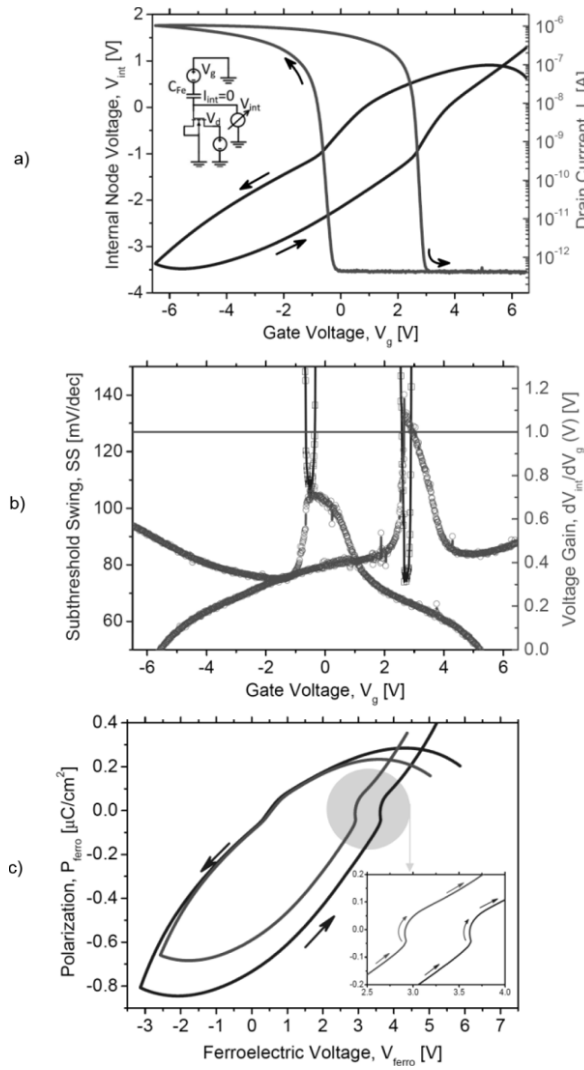


Figure 1.8. *a) Drain current versus gate voltage experiment and corresponding hysteretic internal voltage, Vint, (inset: experimental setup for test conditions, with internal contact connected to a high impedance voltmeter). The hysteretic Vint has a change of slope in the off to on transitions (weak inversion) of the Fe-FET. b) Corresponding subthreshold swings (squares), SS, and internal voltage gain (circles), dVint/dVg. The region of highest internal voltage gain peaks (dVint/dVg ~1.1) corresponds to the lowest SS ~72 mV/decade. Note that when probing the internal contact the Fe-FET subthreshold swing is slightly degraded compared with the case when Vint is left floating and the characteristics shifted to the right (as showed in the supplementary material). c) Polarization versus ferroelectric voltage minor loops showing a clear S-shape region in the voltage range where the internal voltage gain is maximum. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices2.zip*

Another experimental proof of the negative capacitance is the S-shape of P–V_{ferro} or the negative slope of the polarization versus voltage drop on the ferroelectric layer ($dP/dV_{ferro} < 0$) that confirms equation [1.5]. The inset of Figure 1.8(c) clearly demonstrates that such a region is achieved in the Fe-FET device in the sweep-down of the V_g (corresponding to the region where SS is lowered compared to the reference transistor). As the minor loop is not symmetrical, a similar condition is not achieved in the sweep-up of the V_g for the same device. In the corresponding S-shape region, G value is maximal (peak) and larger than 1. Due to the non-uniformity of PVDF-TrFe layer, the negative capacitance condition is not identically achieved in all the devices.

An important property of negative capacitance in Fe-FET concerns the influence of the temperature of the internal voltage amplification, G, and the S-shape region of ferroelectric polarization that is requirement for sub-thermal subthreshold swings. According to the Landau–Devonshire theory of ferroelectrics [TAG 03, GIN 01], the Helmholtz free energy, F, can be truncated with respect to the macroscopic polarization, P according to

$$F = \frac{1}{2}\alpha(T)P^2 + \frac{1}{4}\beta P^4 + \frac{1}{6}\gamma P^6 - EP \qquad [1.6]$$

where E is the electric field and α coefficient is a linear function of temperature, vanishing at the Curie temperature T_0

$$\alpha = \frac{1}{\varepsilon_0}\frac{T - T_0}{C_{CW}} \qquad [1.7]$$

where C_{CW} denoting the Curie–Weiss constant. Parameters β and γ are independent of the temperature. Note that α is positive in the paraelectric phase and negative in the ferroelectric phase.

Figure 1.9 qualitatively shows that only below the Curie temperature ($T < T_0$), when the first term of expression [1.6] is non-zero, does the free energy have a local maximum that conditions the negative capacitance effect. When approaching T_0, the P^2 term of expression [1.6] is reduced and the negative capacitance effect weakens and eventually disappears at T_0, as the unstable equilibrium region in the energy–charge dependence (local maximum) will disappear [SAL 10]. The corresponding slope of electric field versus polarization, dE/dP is negative (S-shape) in the region of

negative capacitance for $T < T_0$ and when the P^2 term cancels out in equation [1.6], dE/dP becomes positive for $T > T_0$.

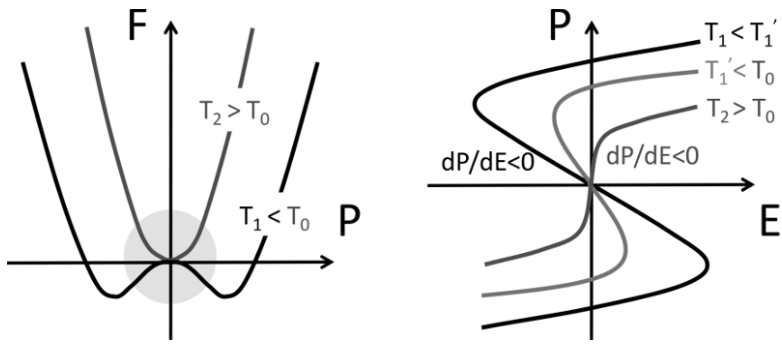


Figure 1.9. *a) Effect of temperature on the Helmholtz free energy, F. b) Effect of temperature on the S-shape P–E characteristics. T_0 is the Curie temperature: for $T < T_0$ the material is in the ferroelectric phase. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices2.zip*

In summary, the polarization S-shape, and therefore, the negative capacitance effect, could vanish by increasing the temperature while the capacitance of the ferroelectric gate stack increases, in agreement with Laudau–Devonshire theory of ferroelectrics. This means that any practical negative ferroelectric gate stack should be designed with a Curie temperature higher than the device operation point in integrated circuits (>100°C).

1.4. Bibliography

[APP 04] APPENZELLER J., LIN Y.-M., KNOCH J., *et al.*, "Band-to-band tunneling in carbon nanotube field-effect transistors", *Phys. Rev. Lett.*, vol. 93, no. 19, 2004.

[APP 05] APPENZELLER J., *et al.*, *IEEE Trans. Electron Dev.*, vol. 52, no. 12, pp. 2568–2576, 2005.

[AYD 04] AYDIN C., *et al.*, *Appl. Phys. Lett.*, vol. 84, no. 10, pp. 1780–1782, 2004.

[BAB 92] BABA T., *Jpn. J. Appl. Phys.*, vol. 31, pp. L455–L457, 1992.

[BAN 87] BANERJEE S., *et al.*, *IEEE Elec. Dev. Lett.*, vol. EDL-8, pp. 347–349, 1987.

[BHU 04] BHUWALKA K., *et al*., *Jap. J. of Appl. Phys.*, vol. 43, no. 7A, pp. 4073–4078, 2004.

[BHU 06] BHUWALKA K., *et al*., *Jap. J. Appl. Phys.*, vol. 45, no. 4B, pp. 3106–3109, 2006.

[BOU 07a] BOUCART K., IONESCU A.M., *IEEE Trans. on Elec. Dev.*, vol. 54, no. 7, pp. 1725–1733, 2007.

[BOU 07b] BOUCART K., IONESCU A.M., *ESSDERC 2007*, Munich, Germany, pp. 299–302, 11–13 Sept. 2007.

[BOU 09a] BOUCART K., IONESCU A.M., *Proceedings of ESSDERC*, Athens, Greece, 2009.

[BOU 09b] BOUCART K., *et al., IEEE Elec. Dev. Lett.*, vol. 30, no. 6, pp. 656–658, 2009.

[BRA 06] BRATKOVSKY A.M., LEVANYUK A.P., "Depolarizing field and 'real' hysteresis loops in nanometer-scale ferroelectric films", *Applied Physics Letters*, vol. 89, 2006.

[CHE 08] CHEN F., KAM H., MARKOVIC D., *et al*., *ICCAD 2008*, pp. 750–757, 10–13 November 2008.

[CHE 13] CHEN Y.N., *et al*., *IEEE Transactions on Electron Devices*, vol. 60, pp. 1092–1098, 2013.

[CON 11] CONZATTI F., PALA M.G., ESSENI D., *et al*., "A simulation study of strain induced performance enhancements in InAs nanowire Tunnel-FETs", *Proc. IEDM*, p. 95, 2011

[CON 12] CONZATTI F., PALA M.G., ESSENI D., "Surface-roughness-induced variability in nanowire InAs tunnel FETs", *IEEE Electron Device Letters*, vol. 33, pp. 806–808, 2012.

[FUL 08] FULDE M., *et al., Proc. IEEE INEC*, pp. 579–584, 2008.

[GIN 01] GINZBURG V.L., *Physics-Uspekhi*, vol. 44, no. 10, pp. 1037–1043, 2001.

[GOP 05] GOPALAKRISHNAN K., GRIFFIN P.B., PLUMMER J.D., *IEEE Transactions on Electron Devices*, vol. 52, no. 1, pp. 69–76, January 2005.

[HAN 00] HANSCH W., *et al., Thin Solid Films*, vol. 369, pp. 387–389, 2000.

[KNO 09] KNOCH J., *Symp. VLSI Technol. System Appl., Technical Digest*, 2009.

[KOG 96] KOGA J., TORIUMI A., *Appl. Phys. Lett.*, vol. 69, no. 10, pp. 1435–1437, 1996.

[KOS 09] KOSWATTA S.O., *et al., IEEE Trans. on Elec. Dev.*, vol. 56, no. 3, pp. 456–465, 2009.

[KRI 08] KRISHNAMOHAN T., *et al., IEDM*, pp. 947–949, 2008.

[LUI 09] LUISIER M., KLIMECK G., *IEEE Electron Device Letters*, vol. 30, p. 602, 2009.

[MAL 12] MALLIK A., "Tunnel Field-Effect Transistors for Analog/Mixed-Signal System-on-Chip Applications", *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 888–894, 2012.

[MAY 08] MAYER F., *et al*., *IEDM 2008*, pp. 163–166, 2008.

[MOO 08] MOOKERJEA S., *et al., Proc. Device Res. Conf.*, June 2008.

[MOS 09] MOSELUND K., *et al*., *Proceedings of ESSDERC 2009*, Athens, Greece, pp. 14–18, September 2009.

[NAB 05] NABER R.C.G., TANASE C., BLOM P.W.M., *et al*., "High-performance solution-processed polymer ferroelectric field-effect transistors", *Nature Materials*, vol. 4, p. 243, 2005.

[NAY 09] NAYFEH O.M., *et al., IEEE Trans. on Elec. Dev.*, vol. 56, no. 10, pp. 2264–2269, 2009.

[POL 08] POLI S., *et al., IEEE Trans. Electron Dev.*, vol. 55, p. 313, 2008.

[QUI 78] QUINN J., *et al*., *Surface Science*, vol. 73, pp. 190–196, 1978.

[RED 95] REDDICK W., AMARATUNGA G., *Appl. Phys. Lett.*, vol. 67, no. 4, pp. 494–496, 1995.

[RUS 10] RUSU A.A., SALVATORE G.A., JIMENEZ D., *et al*., "Metal-ferroelectric-meta-oxide-semiconductor field effect transistor with sub-60mV/decade subthreshold swing and internal voltage amplification", *IEDM Tech. Dig.*, pp. 16.3.1–16.3.4, 2010.

[SAK 04] SAKURAI T., "Perspectives of low power VLSI's", *IEICE Trans. Electron.*, vol. E87-C, pp. 429–436, April 2004.

[SAL 08a] SALAHUDDIN S., DATTA S., "Use of negative capacitance to provide voltage amplification for low power nanoscale devices", *Nanoletters*, vol. 8, no. 2, pp. 405—410, 2008.

[SAL 08b] SALVATORE G.A., BOUVET D., IONESCU A.M., "Demonstration of subthrehold swing smaller than 60mV/decade in Fe-FET with P(VDF-TrFE)/SiO2 gate stack", *2008 IEDM Tech. Dig., Electron Devices Meeting*, pp. 1–4, 2008.

[SAL 10] SALVATORE G.A., LATTANZIO L., BOUVET D. *et al*., "Ferroelectric transistors with improved characteristics at high temperature", *Applied Physics Letters*, vol. 97, no. 5, p. 053503, 2010.

[SEA 10] SEABAUGH A.C., "Low-voltage tunnel transistors for beyond CMOS logic", *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2095–2110, December 2010.

[SIN 10] SINGH J.*, et al*., *Proc. Asia S. Pacif. Design Automat. Conf.*, pp. 181–186, 2010.

[TAG 03] TAGANTSEV A.K., SHERMAN V.O., ASTAFIE K.F., *et al., Ferroelectric Materials for Microwave Tunable Applications*, vol. 11, pp. 5–66, 2003.

[TAK 88] TAKEDA E., *et al*., *IEDM 1988*, pp. 402–405.

[VER 08a] VERHULST A., *et al., J. Appl. Phys*, pp. 064514-1–10, 2008.

[VER 08b] VERHULST A.S. *et al.,* "Electron device letters", *IEEE*, vol. 29, no. 12, pp. 1398–1401, 2008.

[WIR 13] WIRTHS S., *et al*., "Band engineering and growth of tensile strained Ge/(Si)GeSn heterostructures for tunnel field effect transistors", *Appl. Phys. Lett.*, vol. 102, p. 192103, 2013.

[ZHA 06] ZHANG G., *et al*., *Internat. Electron Dev. Meet., Technical Digest*, pp. 431–434, 2006.

[ZHA 08] ZHANG Q., SEABAUGH A., *Proc. Device Res. Conf.*, pp.73–74, June 2008.

[ZHA 09] ZHANG Q., *et al., Solid-State Electron.*, vol. 53, no. 1, pp. 30–35, 2009.

2

Nanowire Devices

2.1. Introduction

Silicon-based nanowire (SiNW) metal-oxide-semiconductor field effect transistors (MOSFETs) are recognized as one of the most promising candidates to extend Moore's law into the nanoelectronics era. Both the top-down and bottom-up approaches are widely studied for the fabrication of NW MOSFET transistors. For the bottom-up approach, the vapor-liquid-solid (VLS) mechanism is the most commonly used route for making semiconductor NWs. The VLS mechanism uses metallic clusters as the nucleation site. If significant progress has been made in realizing NW with VLS growth, there are still a number of outstanding issues associated with the integration of bottom-up grown semiconductor NWs into conventional integrated circuit, design and processing [HOB 12]. The potential metal-contamination presents a major concern for complementary metal–oxide semiconductor (CMOS) technology and the alignment techniques required for large-scale semiconductor device processing is not completely controlled. The top-down approach combines lithographic steps and anisotropic etching processes or deposition to produce semiconductor NWs. This type of processing offers advantages compared to bottom-up synthesis techniques in terms of better yields, availability of mature technology and manufacturing techniques provided by the semiconductor industry for many years. Section 2.2 will give some examples of silicon NW MOSFET both in terms of fabrication challenges based on the top-down approach, which is probably (today) the option most commonly investigated

Chapter written by Gérard GHIBAUDO, Sylvain BARRAUD, Mikaël CASSÉ, Xin Peng WANG, Guo Qiang LO, Dim-Lee KWONG, Marco PALA and Zheng FANG.

Beyond-CMOS Nanodevices 2, First Edition. Edited by Francis Balestra.

by the microelectronic industry [BAN 10, SAI 12] as well as in terms of quantum simulation and electrical characterization issues.

Besides, semiconductor memories are electronic data storage devices based on metal-oxide-semiconductor (MOS) technology. There are various types of semiconductor memories that can be grouped into two basic categories: (1) volatile memory that requires power to retain the data content such as Dynamic Random-Access Memory (DRAM) and Static Random-Access Memory (SRAM) and (2) non-volatile memory (NVM), which is able to retain stored information even without power such as floating-gate memory. In section 2.3, we will focus on the new solutions for NVM technologies offered by NW technologies in terms of both charge storage and resistive change types.

2.2. NW for logic CMOS devices[1]

2.2.1. *NW fabrication and technology*

2.2.1.1. *NW fabrication process*

Silicon-on-insulator (SOI) wafers with 12-nm thick Si layer and 145 nm buried oxide were used as the starting substrate. The SOI substrate is patterned to create silicon NW by using a MESA isolation technique. The stack used to pattern the NWs consisted of a bottom antireflective coating (BARC) layer and a deep ultra-violet (DUV) resist. An ArF laser with an emission wavelength of 193 nm is used. The thickness of the photoresist is adapted to have a proper aspect ratio at the end of trimming. The active zone (i.e. NW feature) etching is carried out using the trimmed resist/BARC as a mask. Obviously, the final line width of NWs is mainly determined by the amount of trimmed resist. The HBr plasma curing process is performed in order to harden the 193 nm ArF resist for a better etching resistance. The BARC opening is done using CF_4 chemistry. It is used in order to ensure vertical resist/BARC profile and correct line width roughness. Moreover, as this sequence consumes a lot of photoresist, the thickness of the BARC layer is well suited to minimize the resist budget during the process.

The BARC/resist trimming process is performed just before the main etch to selectively pattern the silicon on buried oxide. Trimming resist is

1 Section written by Sylvain BARRAUD.

performed to achieve NW structures as small as 7 nm in width using HBr/O_2 plasma. Figure 2.1 shows different NW patterns. Singlefin and multifin (×50) structures are achieved after etching. If small dimensions (sub-10 nm width) are demonstrated, it is not possible to create dense active features by using only 193 nm lithography because of its optical limitations. Consequently, several approaches have been developed in order to reach ITRS predictions [ITR 12], such as extreme ultraviolet (UV) [SUG 12], block-copolymer [ORI 11], e-beam lithography [SUN 13] and spacer patterning approach [CHO 02, BAR 12b]. Regarding the technical issues that remain to be solved for each approach, the spacer patterning technology is one of the most promising solutions [CHO 02, MUK 08]. This approach includes at least three steps: lithography, spacer deposition, spacer and silicon etching to divide the active pitch of the first lithography by a factor 2. E-beam lithography can be used to create the "mandrel" patterns that support the spacers.

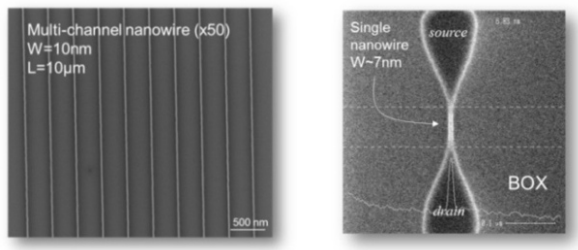


Figure 2.1. *Scanning electron microscopy (SEM) images of multifin and singlefin nanowire after etching (mesa isolation with 145 nm BOX). Nanowire width down to 7 nm is demonstrated*

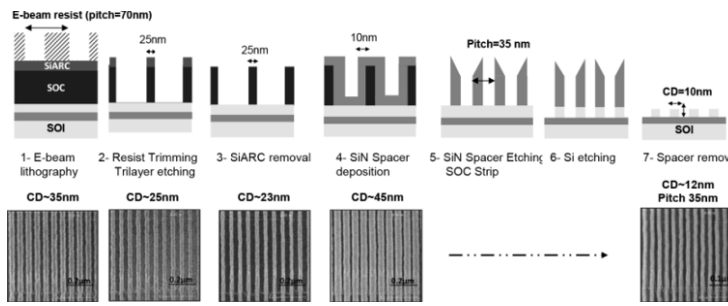


Figure 2.2. *Process flow of spacer patterning module. E-beam lithography with trilayer stack, resist trimming, trilayer etching, Si-Arc removal, spacer deposition, spacer etching, SOC stripping, Si etching and spacer removal*

A typical integration flow for spacer patterning device fabrication is illustrated in Figure 2.2 [BAR 12b]. The e-beam initial pitch is 70 nm, its critical dimension (CD) has to be reduced to 25 nm by a trimming step to reach the final 35 nm fin pitch. Initially developed and demonstrated for FinFET devices on SOI substrate [YAM 11], the spacer patterning has recently been applied for NW [BAR 12b]. Figure 2.2 shows the CD for each process step. Si fin pattern with a CD~10 nm and a fin pitch of 35 nm is demonstrated. After surface cleaning, the high-κ/metal gate stack is deposited: 1.9 nm chemical vapor deposition (CVD) HfSiON with 5 nm TiN metal gate is deposited by atomic layer deposition (ALD) and 50 nm polysilicon layer. As for the active patterning, 193 nm lithography is used with a resist trimming in order to etch the gate length down to 8 nm (Figure 2.3).

A transmission electron microscopy (TEM) cross-section of a NW transistor with L_G = 8 nm and W_{NW} = 7 nm is shown in Figure 2.3. The Si thickness (NW height: H_{NW}) under the HfSiON/TiN gate is 11.5 nm.

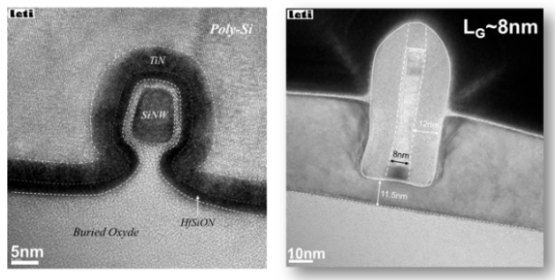


Figure 2.3. *Cross-sectional TEM images: a) 7 nm nanowire width and b) 8 nm gate length*

Recent demonstrations of multigate transistors (MugFET), namely gate-all-around (GAA) [TAC 10, LI 09, KIM 08], Omega-Gate [JIA 09, YAN 02, JAH 05, BUR 10], and TG [SAI 10] have been reported. Obviously, there will be a compromise between the improvement in the electrostatic of MuGFET devices and the fabrication complexity of making gates on all sides of the wire.

If the GAA structure is expected to be the ideal geometry that maximizes electrostatic gate control, it also requires a more complicated fabrication process. An alternative solution for maximizing electrostatic confinement

while minimizing the manufacturing complexity is to use Ω-shaped gate NW. The only difference between TG and omega-gate technology is the hydrogen (H_2) anneal used to round the NW. Hydrogen annealing is a common *in-situ* surface treatment that can be intentionally used for profile transformation by rounding sharp corners [DOR 07]. After Hf-last wet cleaning, the NWs are annealed for 2 min in hydrogen at 750°C. The resulting structures have been observed in cross-sectional high resolution transmission electron microscopy (HRTEM) (Figure 2.4). The hydrogen annealing is used for various reasons: (1) smoothening [DOR 07] and realigning the NW sidewalls to the crystal planes and (2) reshaping the NW cross-section [YAN 04].

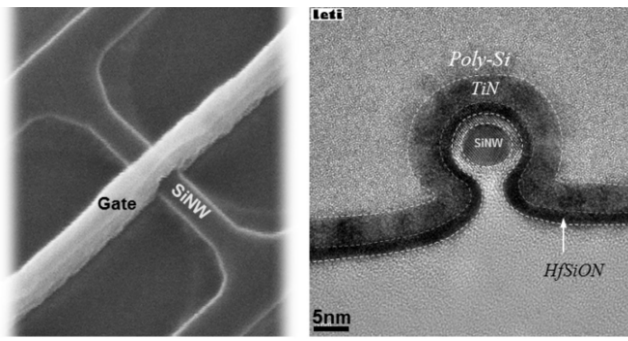


Figure 2.4. *SEM (left) and cross-sectional TEM (right) images of omega-shaped-gate nanowire MOSFETs with 8 nm diameter [BAR 12a]*

After gate etching, a SiN layer (thickness 10 nm) was deposited and etched to form a first offset spacer on the sidewalls of the gate. 18 nm thick Si raised source/drain (S/D) were selectively grown at 750°C, 20 Torr, for the Si reference transistors prior to the (S/D) extension implantation and activation annealing in order to reduce access resistance. If NW-based transistors with excellent immunity to short-channel–effects have already been fabricated [BAR 12a, COQ 12a, SAI 12, BAN 10], strain-induced performance enhancement in short-channel NW will be crucial for the 10 nm technology node and below. Then, embedded SiGe S/D integration previously demonstrated on bulk [UEN 05, MIT 10, PAC 09] and fully depleted silicon-on-insulator (FDSOI) [ZHA 06, CHE 09a, ROY 11] P-type MOSFETs need to be investigated for NW MOSFET architecture. For SiGe S/D, two 650°C schemes can be used: (1) a straightforward selective epitaxy growth (SEG) of *in-situ* boron-doped $Si_{0.7}Ge_{0.3}$:B raised S/D

([B] = 2×10^{20} cm^{-3}) or (2) the *in-situ* HCl + GeH_4 etching of a few nm of Si followed by the SEG of $Si_{0.7}Ge_{0.3}$:B for the formation of recessed S/D. A TEM cross-section of a TG transistor with L_G = 13 nm and W_{NW} = 11 nm is shown in Figure 2.5 [BAR 13].

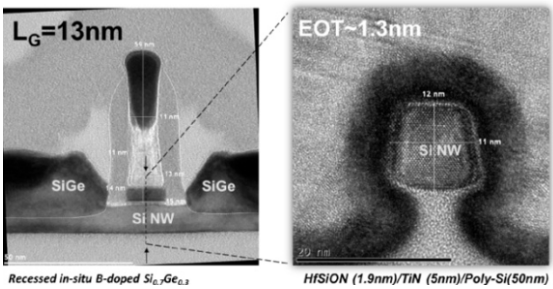


Figure 2.5. *Cross-sectional TEM images of omega-shaped-gate nanowire MOSFETs with SiGe raised source/drain. The nanowire width is 11 nm (right) and the gate length is 13 nm (left)*

Then, a second offset spacer consisting of tetraethyl orthosilicate (TEOS) liner and nitride spacer was formed prior to S/D implantations, activation spike anneal and silicidation (with formation of NiPtSi silicide) for lower contact resistance. Finally, tungsten contact and standard Cu back end are used. Figure 2.6 shows an energy dispersive X-ray analysis of TG NW transistor with the composition of the different chemical species of semiconductor and silicide.

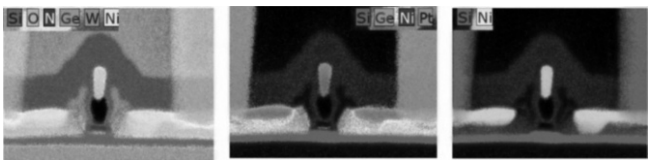


Figure 2.6. *Energy Dispersive X-ray (EDX) analysis of tri-gate nanowire transistor with SiGe source/drain showing the chemical composition of MOSFET devices with NiPt silicide. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

Other top-down technological solutions based on 3D stacked NWs have been proposed to achieve NW densities. The 3D stacked NW process uses the silicon-on-nothing approach [JUR 00]. Starting from a SOI substrate, a (Si/SiGe) superlattice is grown by reduced pressure-chemical vapor

deposition (RP-CVD) [HAR 09]. The superlattices were anisotropically etched in order to pattern fins, as previously discussed. SiGe is then selectively removed from between the Si NW using pure CF_4 in a remote plasma, high pressure and low microwave power tool [BOR 04]. The crystalline structure remains intact after etching [ERN 06]. Figure 2.7 shows the epitaxial growth of Si/SiGe superlattice and stacked NWs after removing the SiGe layer.

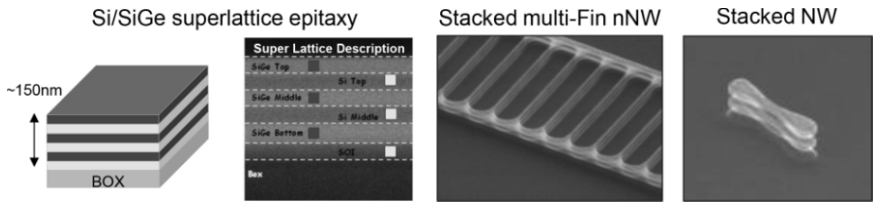


Figure 2.7. *Epitaxial growth of Si/SiGe superlattice and stacked nanowires after removing the SiGe layer*

After removing the SiGe layer, innovative through-Si 3D lithography for ultimate self-aligned GAA NW transistors is proposed [COQ 13b]. E-beam lithography using hydrogen silsesquioxane (HSQ), $H_8Si_8O_{12}$) resist can be used to form self-aligned cavities and finally GAA devices. HSQ is known to be an inorganic material composed of cage-like monomers that turn into cross-linked polymers upon exposure or baking. Unexposed structures are soluble in classical developers such as extra methyl ammonium hydroxide (TMAH). Thanks to its excellent gap-filling properties, HSQ can be spin-coated above and below the Si membrane (Figure 2.8) [COQ 13b].

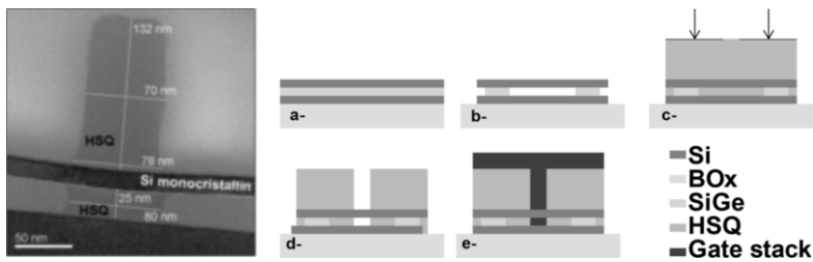


Figure 2.8. *HSQ pattern exposed above/below Si membrane (left). HSQ exposition is possible through Si without impacting Si crystallinity [COQ 13b]. HSQ-based integration steps to create a transistor with self-aligned gates (right). For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

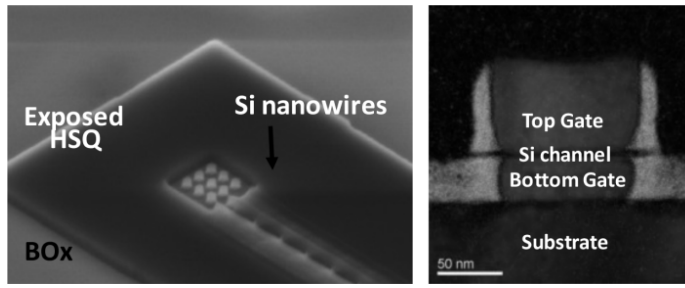


Figure 2.9. *Tilted SEM view of final HSQ pattern over Si nanowire (left) and TEM cross-section showing self-aligned gates with identical top and bottom dimension (right). For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

Figure 2.9(a) and (b) shows the HSQ pattern over 50-channels Si NW with a trench width of 40 nm, and the very good self-alignment of top and bottom gate obtained, respectively. These properties allow the formation of a self-aligned HSQ trench structure around a silicon membrane. This trench can then be filled with a gate material to create a self-aligned multigate transistor, without altering the future Si conduction channel. After poly-Si filing of the patterns, dry etch step is used as planarization to remove the excess gate materials on top of the HSQ. The latter is then removed with wet HF cleaning and nitride spacers are fabricated (light gray region of Figure 2.9).

In the next section, basic electrical characterization of TG and omega-gate NW transistors is summarized.

2.2.1.2. *Performance evaluation*

As explained previously, there is every reason to believe that the downscaling of MOSFET will continue if multigate devices are proposed to keep good short-channel effects (SCEs) with steep subthreshold slopes. Figure 2.10 shows the saturated subthreshold slope SS_{SAT} (extracted at V_{DS} = 0.9V) versus the NW width W_{NW} and the drain induced barrier lowering (DIBL) as a function of the gate length L_G for N- and P-FET TG NWs.

DIBL as small as 82 mV/V has been achieved for H_{NW} = 11 nm, W_{NW} = 12 nm and L_G = 10 nm. A reduction of the subthreshold slope is also observed when reducing the NW width with SS_{SAT}≈75 mV/dec at L_G = 20 nm.

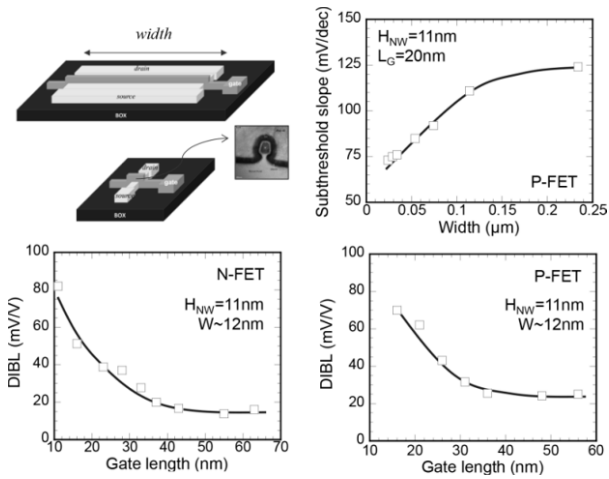


Figure 2.10. *Electrostatics in nanowire field-effect-transistors showing excellent immunity to short-channel-effects down to 10 nm gate length*

Long-channel mobility has been extracted as a function of the NW width in Figure 2.11 ($N_{inv}=10^{13}$ cm^{-2}). Turning from 10 μm wide devices toward 10 nm wide TG NW MOSFETs, the electron mobility tends to decrease (−35%) while the hole mobility is improved (+40%). This behavior is well explained by the combination of the top and sidewall channel conduction and the surface orientation dependence of the mobility [CHE 10].

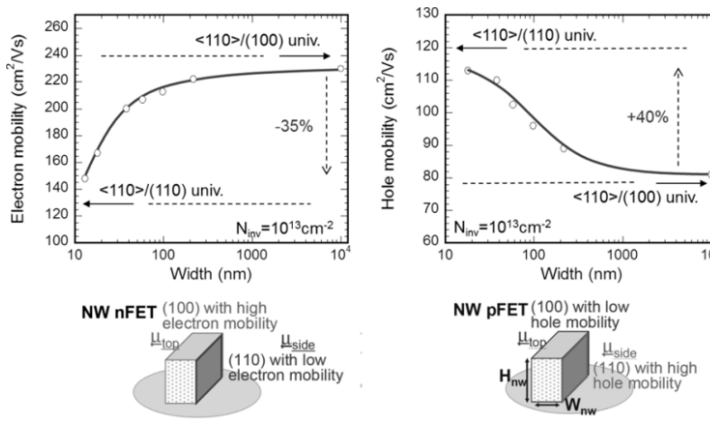


Figure 2.11. *Carrier mobility of tri-gate nanowire as a function of the nanowire width. The mobility is extracted at $N_{inv}=10^{13}$ cm^{-2} along the <110>/(100) direction*

If aggressively scaled NW transistors with good SCEs have been processed, strain-induced performance enhancement in short-channel NWs still need to be proven and deeply understood to improve performance. Several key challenges remain in order to achieve high performance in MuGFET devices. In particular, the lower electron mobility on (110) lateral channels compared to conventional (100) top channel may be an issue. The most common way for mobility enhancement is stress engineering, widely used for high-performance logic applications. As a result, strained-Si NW FETs, combining the benefits of enhanced mobility with excellent electrostatics, are seriously envisaged as a leading solution for the future technology nodes [COQ 13, BAR 13]. The performance (I_{OFF}-I_{SAT}) of ultrascaled strained-Si N-FET NW scaled down to L_G = 10 nm is reported in Figure 2.12a. About +50% I_{SAT} improvement is obtained at I_{OFF} = 10 nA/µm. The saturation current (I_{SAT}) versus the threshold voltage V_{TSAT} is shown in Figure 2.12(b) for short channel(s) SOI NW (L_G=25 nm). Under uniaxial tensile strain, V_{TSAT} is reduced and the I_{SAT} current improvement is almost by a factor of 2.

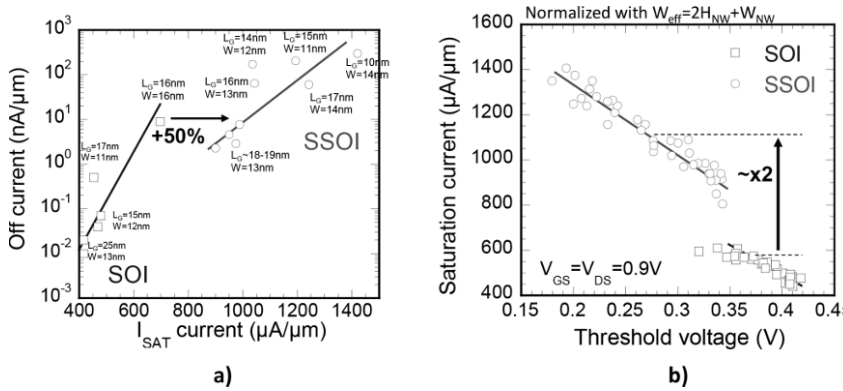


Figure 2.12. *a) Performance (I_{OFF}-I_{SAT}) of (strained)-SOI NW with L_G down to 10 nm. An I_{SAT} improvement of +50% is achieved at I_{OFF}=10 nA/µm; b) I_{SAT} versus V_{TSAT} for multi-fin (strained)-SOI NW (W_{NW}=20 nm, L_G=25 nm). Under uniaxial tensile strain, V_{TSAT} is reduced and the I_{SAT} current improvement reaches almost ×2*

$I_{DS}(V_{GS})$ and $I_{DS}(V_{DS})$ curves of 10 nm gate length strained-SOI NW are plotted in Figure 2.13 showing excellent electrostatic control and performance. These results demonstrate the high efficiency of strained-SOI substrates to enhance short-channel transport in N-FET NWs.

For P-FET, embedded SiGe S/D integration has previously been demonstrated on bulk and FDSOI MOSFETs. However, few results are available for NWs [LI 07].

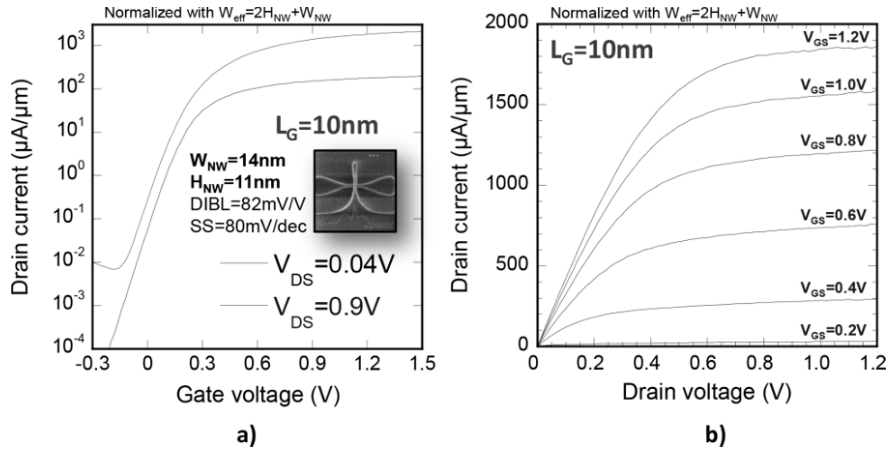


Figure 2.13. *a) $I_{DS}(V_{GS})$ and b) $I_{DS}(V_{DS})$ characteristics of omega-gate strained-SOI NW transistor. Excellent immunity to short-channel-effects (DIBL=82 mV/V) and good performance (I_{SAT}=1420 µA/µm) are achieved*

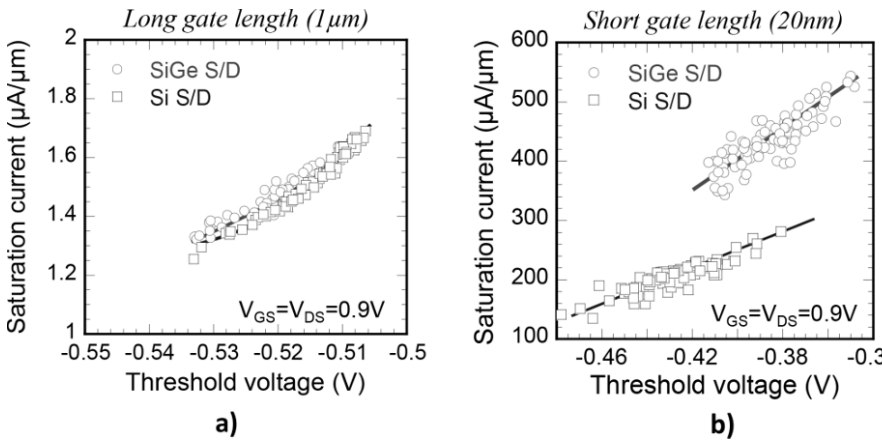


Figure 2.14. *a) I_{SAT} versus V_{TSAT} of P-FET multifin SOI NWs. For W_{NW}=25 nm and L_G=25 nm, the in-situ HCl + GeH_4 etching and $Si_{0.7}Ge_{0.3}$:B selective epitaxial growth (650°C, 20 Torr) yields the best performance*

Figure 2.14 compares the performance of P-FET NW with and without SiGeS/D. The saturated threshold voltage is extracted by using the constant current method at 100 nA × W/L_G with $W = 2 \times H_{NW} + W_{NW}$. The relevance of using SiGe:B S/D comes from: (1) the carrier mobility enhancement induced by the uniaxial compressive strain in the channel and (2) the improvement of access resistance induced by the SiGe layer and the high boron (B) doping levels. For long gate lengths (Figure 2.14(a)), the compressive strain effect diminishes in the channel and the impact of S/D resistances becomes negligible. No I_{SAT} improvement is achieved. For short gate lengths, SiGe:B S/D improves I_{SAT} compared to Si S/D (Figure 2.14b). The combination of *in-situ* HCl etching with the SEG of B-doped $Si_{0.7}Ge_{0.3}$ improves electrical performance and slightly reduces V_{TSAT}. The increase of uniaxial compressive strain in the channel coming from the use of recessed S/D SiGe stressors may be a promising option for SOI NW technology.

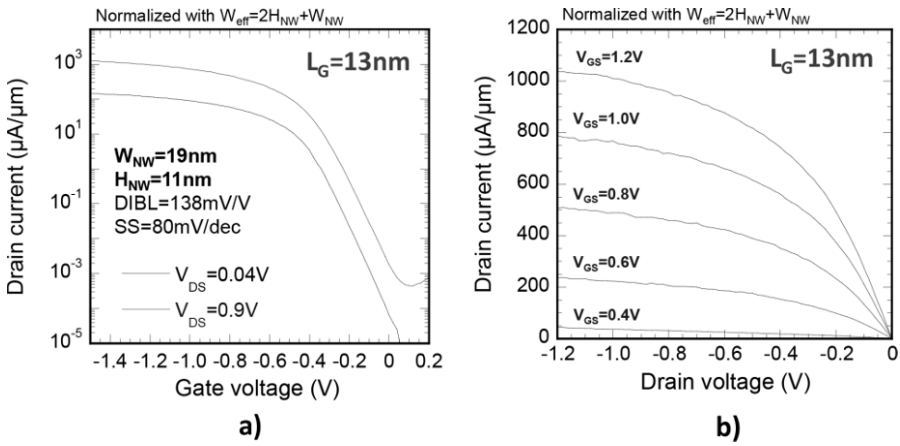


Figure 2.15. *a) $I_{DS}(V_{GS})$ and b) $I_{DS}(V_{DS})$ characteristics of P-FET NW transistor with recessed-SiGe source/drain*

$I_{DS}(V_{GS})$ and $I_{DS}(V_{DS})$ curves of 13 nm gate length P-FET NW with $Si_{0.7}Ge_{0.3}$:B S/D are plotted in Figure 2.15. A saturation current I_{SAT} = 610 µA/µm is achieved with a low I_{OFF} current (1.8 nA/µm). The NW width is also expected to have a large impact on performance due to the change of mobility in <110> NWs. By reducing the NW width, a large mobility improvement induced by a significant increase of subband curvature and hole velocity is expected [NEO 10]. The efficiency of recessed

S/D SiGe:B stressors for narrow channel transistors is well illustrated in Figure 2.16(a). The results show a major improvement of the saturation current, from +40% for wide planar transistors up to +100% for narrow NW transistors. The high efficiency of uniaxial compressive strain in <110> NWs has been explained with the atomistic tight-binding approach [NIQ 12]. Compressive strain strengthens the light subbands of the highest valence subbands, pushing heavy hole subbands down. This leads to a higher average hole velocity and induces an improvement of the saturation current (×2) along the <110> direction. In Figure 2.16(b), the saturation current enhancement is shown as a function of the epitaxial SiGe:B film thickness. The saturation current is extracted at $|V_{GS}-V_T| = 0.65$ V and $L_G = 25$ nm. The performance of P-FET NW is enhanced as the SiGe:B S/D becomes thicker (13 nm–20 nm), from +50% up to +70% due to an increase of compressive strain [LIO 08, LI 06].

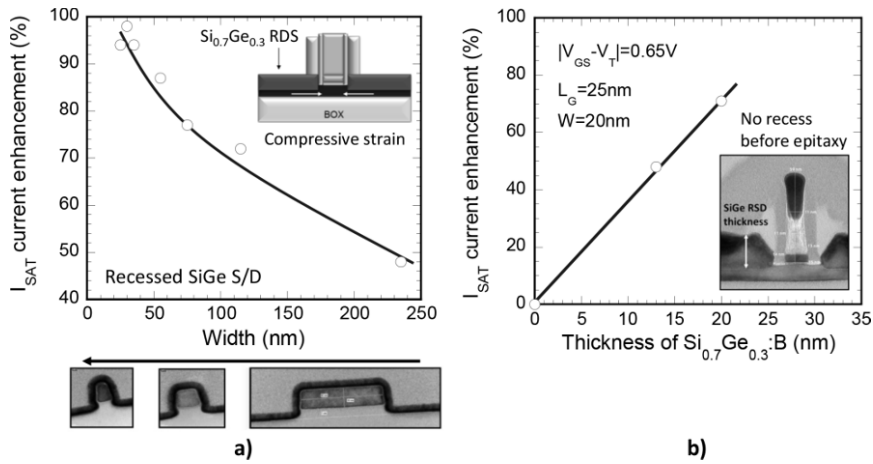


Figure 2.16. *a) I_{SAT} current enhancement of P-FET multi-fin NW induced by SiGe:B S/D (+100% for narrow NW versus +40% for wide planar FET); b) as thickness of SiGe:B S/D increases, performance of P-FET SOI NWs is enhanced from +50% to +70%*

2.2.2. *Quantum simulation of NWs* [2]

Advancements in miniaturization techniques have allowed the microelectronics industry to fabricate MOS transistors with gate lengths of a

2 Section written by Marco PALA.

few nanometers. As promising candidates to replace bulk MOSFETs, great research effort has been devoted to the development of strongly confined structures such as NWs due to their optimal electrostatic control of the channel region suppressing SCEs and increasing the Ion/Ioff ratio.

2.2.2.1. *Model*

Quantum effects arising from lateral confinement or phase coherence cannot be neglected in short-length NWs and have to be accounted for by means of a full-quantum transport approach. For this purpose, coherent- and dissipative-quantum transport simulations can be realized by solving the self-consistent 3D Poisson and Schrödinger equations within the non-equilibrium Green's function (NEGF) formalism.

Depending on the system, different kinds of Hamiltonians can be exploited to simulate the transport properties of the considered NWs. Here, we present simulations of silicon NWs according to the effective-mass approximation [POL 08, BUR 09], and InAs NWs according to the eight band k·p Hamiltonian proposed in [BAH 90], which describes the valence and conduction bands at the Γ point and accounts for the spin–orbit interaction. If the 3D Hamiltonian is directly discretized in real space, i.e. by using the finite-difference method on a 3D grid where $r_{ijk} = (x_i, y_j, z_k)$ is the generic discretization point, then we obtain a block tridiagonal matrix with submatrices $H_{RS}(x_i, x_j)$, where i identifies the x_i section of the NW. Each $H_{RS}(x_i, x_j)$ has rank $N_b N_y N_z$, with N_b being the number of bands of the k·p Hamiltonian and N_y and N_z being the number of discretization points along the y- and z-directions, respectively. In order to reduce the computational effort arising from the manipulation of matrices of such dimensions, we exploited the theoretically equivalent coupled-mode-space formulation [POL 08, SHI 09, CON 12a]. With this approach, the rank of the diagonal and off-diagonal blocks of the Hamiltonian can be reduced by means of the unitary transformation $H_{MS}(x_i, x_j) = U(x_i)\dagger H_{RS}(x_i, x_j)U(x_j)$, with $j = i$, $(i - 1)$ or $(i + 1)$, where $U(x_i) = (\chi_1(x_i) \cdots \chi_M(x_i))$ is the rectangular unitary matrix composed of the M eigenvectors of the two-dimensional (2D) Schrödinger problem at the ith device section. Eigenvalues $E_m(x_i)$ and wave functions $\chi_m(x_i)$ are referred to as the modes of section x_i, and the number of the modes retained in each section (M) sets the rank of submatrices $H_{MS}(x_i, x_j)$ of the mode-space Hamiltonian [POL 08, CON 12a]. Since the carrier transport is mainly governed by the modes with eigen-energies close to the

conduction- and valence-band edges, a very good approximation of the transport properties of our devices can be achieved with some tens of modes at most. The mode-space retarded Green function $G^{R,MS}$, lesser than $G^{<,MS}$ and greater than $G^{>,MS}$ Green functions were then computed via a recursive algorithm based on the Dyson equation [FER 97]; the self-energies of the contacts were obtained with the iterative scheme of [SAN 84]. The strain was included in our simulations of InAs NWs by adding the strain interaction matrix to the k·p Hamiltonian [BAH 90], with the deformation potentials taken from [FIS 91, LEN 08]. As for Si NWs, the uniaxial strain was described according to the analytical expressions for the conduction-band edges and effective masses reported in [UNG 07].

In the case of non-null phonon scattering, the kinetic equations for the retarded and lesser than Green functions are nonlinearly coupled and need to be self-consistently solved. Here, the lesser than self-energies for phonon scattering are expressed within the self-consistent Born approximation $\Sigma^{<(>)} = D^{<(>)}\ G^{<(>)}$, where $D^{<(>)}$ is proportional to the Green function of the unperturbed phonon bath [ROG 09]. More precisely, the mode-space lesser than self-energy for acoustic phonons and for the *n*th mode reads:

$$\Sigma_{ac}^{<,n,n}\left(x_i,x_i;E\right)=\frac{D_{ac}^2 k_B T}{\rho v_s^2}\sum_m I^{m,n}\left(x_i,x_i\right)G^{<,m,m}\left(x_i,x_i;E\right) \qquad [2.1]$$

where $I^{m,n}(x_i, x_j)$ is the usual form factor, ρ is the material density, v_s is the sound velocity, T is the temperature and D_{ac} is the acoustic deformation potential. The lesser than self-energy for dispersionless optical phonons is expressed as:

$$\Sigma_{opt}^{<,n,n}\left(x_i,x_i;E\right)=\frac{\hbar D_{opt}^2}{2\rho\omega_j}\sum_m I^{m,n}\left(x_i,x_i\right)G^{<,m,m}\left(x_i,x_i;E\pm\hbar\omega_j\right)\left[N_j+\tfrac{1}{2}\pm\tfrac{1}{2}\right] \qquad [2.2]$$

where ω_j is the frequency of the j^{th} optical branch, D_{opt} is the optical deformation potential and N_j is the equilibrium phonon density given by the Bose statistics. Polar-optical-phonon (POP) scattering was also included in InAs device simulations due to its relevance in III–V compounds. However, although this is a non-local mechanism, it was accounted for by means of a local self-energy similar to equation [2.2] with an effective deformation potential D_{pop} and phonon frequency ω_{pop}. This approximation was adopted

to circumvent the numerical difficulties of implementing non-local self-energies, which would prevent the use of the recursive algorithms used to handle 3D quantum transport problems [LUI 09].

Surface roughness (SR) was introduced by means of a geometrical description of spatial fluctuations at the $Si\text{-}SiO_2$ interfaces [POL 08], [BUR 09]. Random fluctuations $\Delta(r)$ are generated according to an exponential autocorrelation function:

$$\langle \Delta(r')\Delta(r'-r)\rangle = \Delta_m^2 \exp\left(-\sqrt{2}r / L_m\right) \quad [2.3]$$

where Δ_m is the root mean square (RMS) of the fluctuation and L_m is the correlation length [GOO 85].

The extraction of the effective mobility μ_{eff} is performed in the linear transport regime (typically V_{DS} = 5 mV) following the method presented in [POL 08]. The evaluation of the effective mobility for such short-channel devices accounts for the non-local effect of the apparent or ballistic mobility component arising from contact resistance and linearly depending on the channel length. In order to isolate a purely scattering-limited mobility, we adopt a Mathiessen rule [SHU 02, POL 09a, GNA 10] to decompose the effective mobility μ_{eff} as:

$$\mu_{SR(PH)} = \left(\mu_{eff}^{-1} - \mu_{bal}^{-1}\right)^{-1}, \quad [2.4]$$

where μ_{bal} is the ballistic component and $\mu_{SR(PH)}$ is the SR (PH)-limited mobility.

2.2.2.2. *Comparison of transport properties of Si NWs and double-gate MOSFETs in the presence of SR*

Although ballistic electrons are expected to play an important role in the electrical performance of ultrashort devices, spatial fluctuations arising from different sources of scattering such as doping pockets [LUS 05], random impurities [HUE 07], remote Coulomb scattering [ESS 03, POL 09b] and SR at the interfaces [WAN 05, BUR 09, CRE 11, CON 12b] can significantly affect the source-to-drain transport.

Due to the strong confinement along the transverse directions, SR generates important variability effects on the electrical characteristics and electron mobility reduction. One main effect induced by SR is to introduce

spatial fluctuations of the effective potential seen by electrons along the transport direction, which can result in sizeable device variability. Here, we address the impact of dimensionality on electron transport in the presence of SR, which takes place via one-dimensional (1D) and 2D subbands for the NWs and planar double-gate (DG) structures, respectively. We present a comparative study on the effect of the SR on NW and DG transistors with thin lateral sizes by analyzing their drain current and SR-limited mobility [CRE 11].

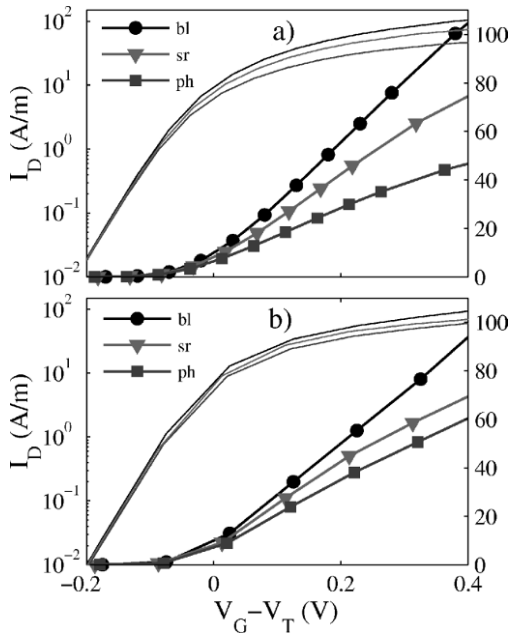


Figure 2.17. *Drain-current as a function of (VG − VT) for silicon (a) NW and (b) DG FETs with a channel thickness of T = 3 nm. From top to bottom the I-V curves correspond to a device with no scattering (bl), to one with surface roughness scattering (sr) and to one with phonon scattering (ph). V_{DS}=5 mV, L_G=20 nm, EOT=1 nm*

Here, we simulated planar DG and rectangular NW FETs with channel thickness T = 3 nm and gate length L_G = 20 nm. We assumed an SR described by equation [2.3] with an RMS value of Δ_m = 0.2 nm and a correlation length of L_m = 1 nm. This corresponds to high-quality surface

samples, being real devices possibly characterized by larger spatial fluctuations. We remark that the two kinds of devices have different electrostatics since the NWs are confined along two spatial directions whereas the DGs are confined only along one direction, as well as a different transport dimensionality since electrons propagate through 1D and 2D subbands in NW and DG structures, respectively. An example of drain current as a function of the gate overdrive ($V_G - V_T$) for both NWs and DGs with a specific realization of the SR is shown in Figure 2.17. Currents and electron densities are normalized with respect to the effective width $W_{eff} = 4W_{NW} = 4T$ for NWs and $W_{eff} = 2WDG$ for DGs. This choice assures a similar dependence on the gate overdrive of the transfer characteristics of the two geometries under study.

The effect of the SR on the current is qualitatively known from previous results in the literature [BUR 09]. It consists in a positive threshold-voltage shift ΔV_T and a current reduction at large overdrives. However, due to the larger fluctuations of the first subband of the unprimed valley induced by the rough interfaces, ΔV_T turns out to be larger in NWs than in DGs. This can be explained by considering that the ratio between the first subband fluctuation of the NW and the DG at the first order in the thickness fluctuation ΔT can be approximated as $\Delta E_{NW}/\Delta E_{DG} \approx 1 + m_l/m_t$, where m_l and m_t are the longitudinal and transverse Si effective masses. The threshold voltage of the ballistic device was extracted from the linearization of the output characteristics at high overdrive, whereas ΔV_T of devices with roughness was estimated by considering the voltage shift necessary to match the output characteristics in the subthreshold-voltage regime. A statistical study of ΔV_T for the most interesting case of thin devices (T = 3 nm) is presented in Figure 2.18. We evaluated threshold voltage shifts of 100 different SR realizations and observed larger mean value and broader dispersion for NW transistors than for DG transistors. In particular, we report a mean value $<\Delta V_T> = 47$ mV and a standard deviation of 14 mV for NWs, and $<\Delta V_T> = 16$ mV and a standard deviation of 7 mV for DGs. As a result, thin NW devices are much more sensitive to SR-induced variability of the threshold voltage, whereas the drain current at large overdrive is similarly reduced in quasi-1D and in quasi-2D nanostructures. Moreover, we notice that, for the chosen values of roughness parameters, phonon (PH) scattering is more efficient than SR scattering in suppressing the drain current at high overdrive. This is particularly relevant in the case of NWs thanks to the increased efficiency of el–ph interaction as far as the quantum confinement increases.

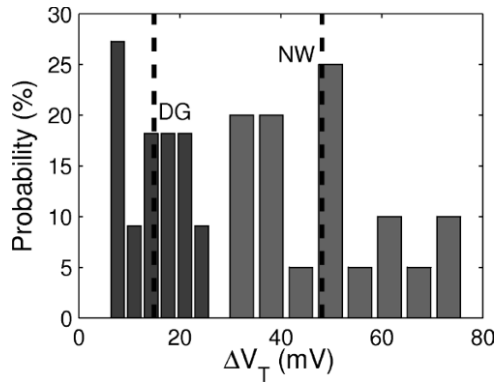


Figure 2.18. *Variation of the threshold-voltage shift for (left) DG and (right) NW devices with a channel thickness of T = 3 nm. Statistics collected over 100 different roughness realizations. SR parameters are Δm = 0.2 nm and Lm = 1.0 nm. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

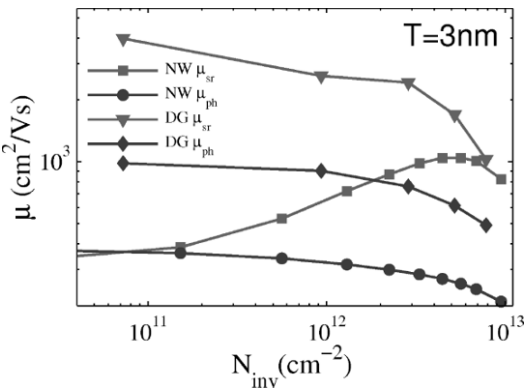


Figure 2.19. *SR- and PH-limited mobilities as a function of the inversion density Ninv for silicon NW and DG FETs with a channel thickness of T = 3 nm*

Mobility curves conclude the analysis on the SR effect on transport properties of 1D and 2D structures. Figure 2.19 shows results for SR-limited mobilities extracted according to equation [2.4]. We observe that μ_{PH} is always smaller than μ_{SR}. This confirms that, for the SR parameters used in these simulations, the main limiting scattering mechanism is still the el–ph interaction [POL 09a]. A remarkable difference in the μ_{SR} dependence on N_{inv} between the quasi-1D and 2D structures is shown in Figure 2.19, where the mobility of the thin NW increases with the electron density in the weak

inversion regime. This is a consequence of enhanced localization phenomena [POL 09], which strongly reduce the SR mobility at low overdrives. Localization effects are less relevant in DG devices due to their quasi-2D nature that allows electrons to circumvent potential obstacles induced by the SR by using alternative current paths. As the overdrive increases and localizations become less probable, μ_{SR} presents similar values for the DG and NW FETs.

2.2.2.3. *Interfacial traps in InAs NW FETs*

Semiconductor NWs based on III-V materials such as InAs have recently attracted a lot of interest for their outstanding transport properties, thanks to the low density of states and high electron mobility and the reduced SCEs with respect to the planar case guaranteed by the TG or the GAA configurations. Moreover, the InAs NW is a very attractive channel material/device architecture combination for tunnel-FETs due to the small bandgap and the possibility to further boost the on-current, ion, using staggered or broken bandgap heterojunctions [KNO 10] or strain engineering [CON 11, CON 12a]. Such devices could reduce the inverse subthreshold slope (SS) with respect to MOSFETs and thus allow for an aggressive V_{DD} scaling. However, given the relatively large density of interface states in III-V FETs [PAS 10, LIN 11], the degradation of the SS in both tunnel-FETs and MOSFETs due to interface states is a serious concern for the realization of efficient nanodevices.

The effect of traps in NWs can be accounted for within a full-quantum approach based on the model presented in [PAL 12, PAL 13], where traps were inserted by superimposing cubic potential wells $V_t(r,r_t)$ to the conduction band profile $E_C(\mathbf{r})$ with $V_t(\mathbf{r}, \mathbf{r}_t) = -V_{depth}$ if $(\mathbf{r}-\mathbf{r}_t) \in C_t$ and $V_t(\mathbf{r}, \mathbf{r}_t) = 0$ otherwise, with C_t being a cube with a 1 nm^3 volume. The traps are placed at the InAs-oxide interface. The depth V_{depth} of the quantum well can be used to modify the trap energy level.

Figures 2.20 and 2.21 show an example of the local density of states (LDOS) for an InAs NW MOSFET and a tunnel-FET, respectively, in the presence of randomly distributed traps in the channel region. In fact, the NEGF simulations neatly show the LDOS in the gaps corresponding to the traps. Traps at different lateral and longitudinal positions produce localized zero-dimensional (0D) electrically active states with different trap energy levels, even if the barrier potential depth V_{depth} is the same for all

traps. This occurs because the actual energy resolved LDOS is the result of the self-consistent solutions of the Poisson and the transport equations [ESS 13].

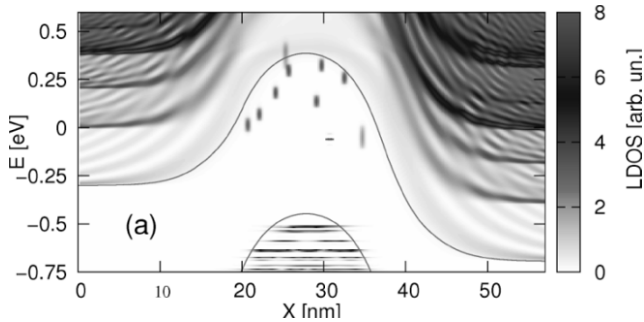


Figure 2.20. *Example of energy-resolved LDOS of a nanowire InAs MOSFET in the presence of interfacial traps with density $D_T = 2 \times 10^{12} cm^{-2}$. The LDOS produced by the traps are clearly visible at different positions along the x-axis and at different energies. $V_{GS} = -0.1V$ and $V_{DS} = 0.4V$ (off-state). For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

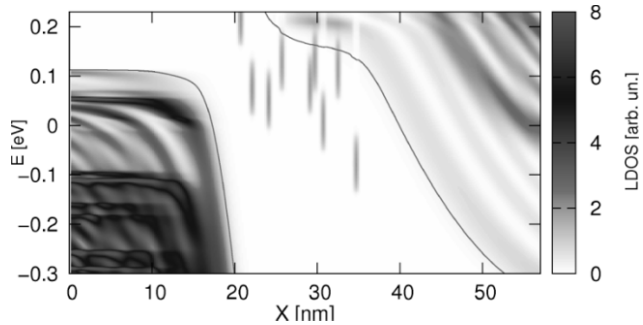


Figure 2.21. *Example of energy-resolved LDOS of an InAs Tunnel-FET in the presence of randomly distributed interface traps in the channel region (20nm <x< 37nm) with density $D_T = 2x10^{12} cm^{-2}$. The LDOS produced by the traps are clearly visible at different positions along the x-axis and at different energies. $V_{GS} = -0.1V$ and $V_{DS} = 0.4V$ (off-state), For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

This approach to trap modeling [PAL 13] has the advantage of accounting for the discrete nature of traps, and of providing 0D electrically active states, which can both modify the device electrostatics and play a direct role in the carrier transport.

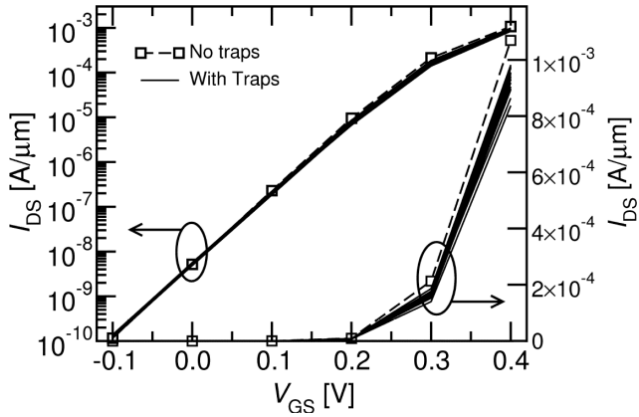


Figure 2.22. *Drain current versus gate voltage characteristics for an InAs MOSFET at V_{DS} = 0.4 V and for about 20 realizations of a spatially random distribution of traps. Trap areal density $D_T = 2 \times 10^{12}$ cm^{-2}, $E_{T,FB} = -149$ meV, EOT = 0.7 nm*

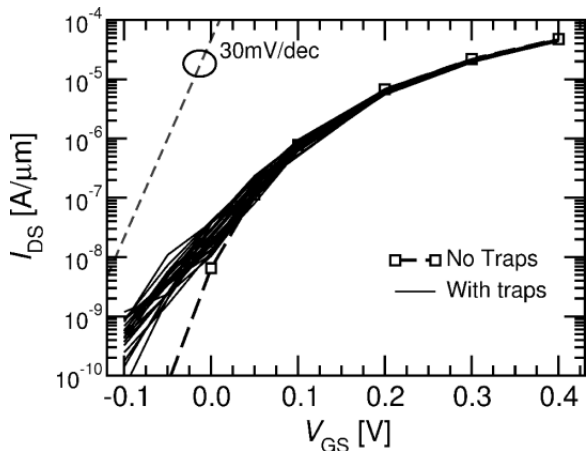


Figure 2.23. *Drain current versus gate voltage characteristics for an InAs Tunnel- FET at V_{DS} = 0.4 V and for about 20 realizations of a spatially random distribution of traps. Trap areal density $D_T = 2 \times 10^{12}$ cm^{-2}, $E_{T,FB} = -149$ meV, EOT = 0.7 nm*

The investigation of the impact of traps in InAs NW MOSFETs and tunnel-FETs was first carried out by considering the same device structure. We considered an (100) InAs NW with a gate length of 17 nm and a cross-section of 5 × 5 nm^2. Figure 2.22 illustrates the IV curves for about 20

realizations of InAs MOSFETs. The comparison with Figure 2.23 immediately reveals that the impact of traps is much smaller in MOSFETs than in tunnel-FETs. In particular, the influence of traps on the subthreshold slope is modest and the different realizations show a sizeable difference only at large V_{GS}. A closer analysis shows that traps affect the IV curves of the MOSFETs mainly by modifying the device electrostatics, and thus inducing an I_{DS} reduction compared to the device with no traps. In particular, the traps also result in subband fluctuations at the virtual source and along the channel, which are known to degrade the I_{on} by increasing the channel reflection coefficient [BUR 09]. Figure 2.23 shows the IV curves for about 20 realizations of InAs tunnel-FETs. As can be seen, the traps have a large effect on the I_{DS} characteristics in the subthreshold region and we verified that the largest I_{off} degradation arises from traps located close to the center of the channel (see Figure 2.21). Here the traps act as stepping stones for the tunneling from the source valence band to the channel conduction band and thus shorten the dominant tunneling distance. The influence of the traps becomes progressively smaller with larger V_{GS} and the impact on the ion is almost negligible. This means that the traps do not appreciably affect the I_{DS} of the tunnel-FETs when the gate bias induced band-bending is large enough. The results in Figure 2.23 show that the impact of traps in tunnel-FETs mainly stems from the enhancement of the band-to-band tunneling, i.e. from a direct involvement of the trap in the transport from the valence band in the source to the conduction band in the channel. The effect of the negative charge in the traps is instead quite modest, which results in a change of the subband profiles with respect to the device with no traps. Moreover, such an effect on the subband profiles implies a reduction of I_{DS} with respect to the case with no traps.

Figures 2.24 and 2.25 show the IV for different random patterns of interface states for MOSFETs and tunnel-FET, so that a statistical analysis for off-current, subthreshold slope and on-current can be carried out. As can be seen in Figure 2.24 the traps determine a significant variability of SS and I_{off} in tunnel-FETs, and both figures of merit are remarkably deteriorated compared to the device with no traps [ESS 13]. The impact of traps on the corresponding figures for MOSFETs is instead much smaller. Figure 2.25 illustrates the I_{off} versus I_{on} graph and it can be seen that in tunnel-FETs the large trap induced variations of I_{off} correspond to a very limited I_{on} variability, which is consistent with Figure 2.23, whereas the trap induced variability in MOSFETs is very small for both I_{off} and I_{on}. The results in

Figures 2.24 and 2.25 underline that, as already pointed out in [CON 12b], the device variability may be critical in tunnel-FETs, because of the inherent sensitivity of tunneling to bandgap fluctuations induced by changes in the device's geometrical features and to defects that may act as stepping stones for the band-to-band tunneling process.

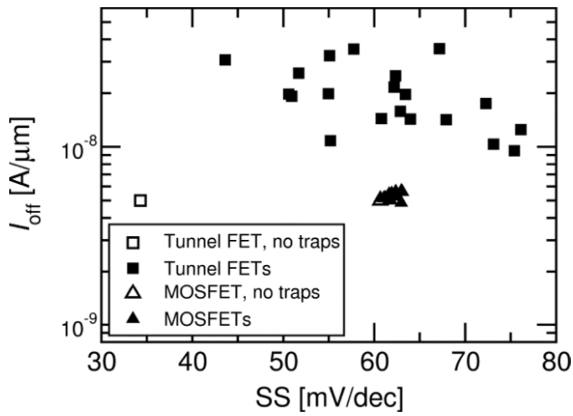


Figure 2.24. *I_{off} (i.e. I_{DS} for $V_{GS} = 0$, $V_{DS} = V_{DD} = 0.4V$) versus SS (averaged for I_{DS} between 1nA/µm and 100 nA/µm) for about 20 realizations of InAs tunnel-FET and InAs MOSFET with a spatially random distribution of traps with $D_T = 2 \times 10^{12}$ cm^{-2}, $E_{T,FB} = -149$meV, EOT = 0.7 nm*

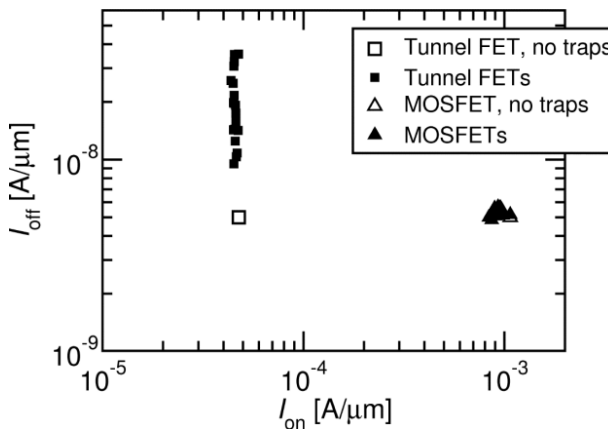


Figure 2.25. *I_{off} versus I_{on} (i.e. I_{DS} for $V_{GS} = V_{DS} = V_{DD} = 0.4$ V) for about 20 realizations of InAs Tunnel-FET and InAs MOSFET with a spatially random distribution of traps. Trap areal density $D_T = 2 \times 10^{12}$ cm^{-2}, $E_{T,FB} = -149$ meV, EOT = 0.7 nm*

2.2.3. *Electrical characterization of NWs*[3]

2.2.3.1. *Electronic transport evaluation*

2.2.3.1.1. Mobility results by CV-split: effect of channel width

The transport properties of Si NW transistors depends on the NW width (W_{top}) as shown by mobility measurements performed on long channel N- and P- NW FETs with a rectangular cross-section [CHE 08, COQ 12a] (Figure 2.26). The devices have been fabricated using the top-down approach by optical lithography followed by a resist trimming process, starting from an (100) unstrained and strained SOI (SOI and sSOI) wafers [COQ 12a]. In Figure 2.26(a) and (c), the effective mobility as a function of inversion carrier density N_{inv} is measured as the device is turned from wide (W_{top} = 10 µm) to NW architecture down to W_{top} = 10nm, for NWs with a (110) channel orientation. For the NMOS case, the effective mobility of unstrained NWs is degraded compared to wide FET, while the hole mobility is improved, especially in high N_{inv} region in PMOS. Depending on the channel orientation, the sidewall surfaces of the NW FETs fabricated on a standard (001) silicon wafer may result in either (110) or (100) inversion layers. For (110) channels, the sidewall corresponds to (110) surfaces. The conduction in strong inversions can mainly be described by the independent contribution of the (100) top surface and the (110) sidewall surface for NWs, and the surface orientation dependence of the mobility [UCH 06, CHE 08, SAI 10]. Electron mobility is higher for a (100) Si inversion surface than a (110) Si surface, while hole mobility exhibits the opposite behavior, with hole mobility improvement for (110) inversion surface. As the width is narrowed the vertical (110) oriented sidewalls play an increasing role in carrier transport, following the additivity of mobility expressed as [COQ 12b, KOY 13a]:

$$\mu_{NW} = \mu_{top}^{(100)}\left[W_{top}/\left(2H_{NW}+W_{top}\right)\right] + \mu_{sidewall}^{(110)}\left[H_{NW}/\left(2H_{NW}+W_{top}\right)\right] \qquad [2.5]$$

This leads to a 44% mobility loss for electron mobility as W_{top} is reduced down to 10 nm on data of Figure 2.26(a), while hole mobility is improved by 35% for W_{top} = 10 nm. The sidewall contribution can be extracted from NWs mobility data, using equation [2.5], and with the reliable assumption that $\mu_{top}^{(100)}$ is given by the 10 µm wide mobility. The

3 Section written by Mikaël CASSÉ and Gérard GHIBAUDO.

obtained sidewall mobility $\mu_{sidewall}$ is in very good agreement with the electron and hole mobility measured on (110) reference wafer (Figure 2.26(d)), thus demonstrating the validity of equation [2.5] in strong inversion.

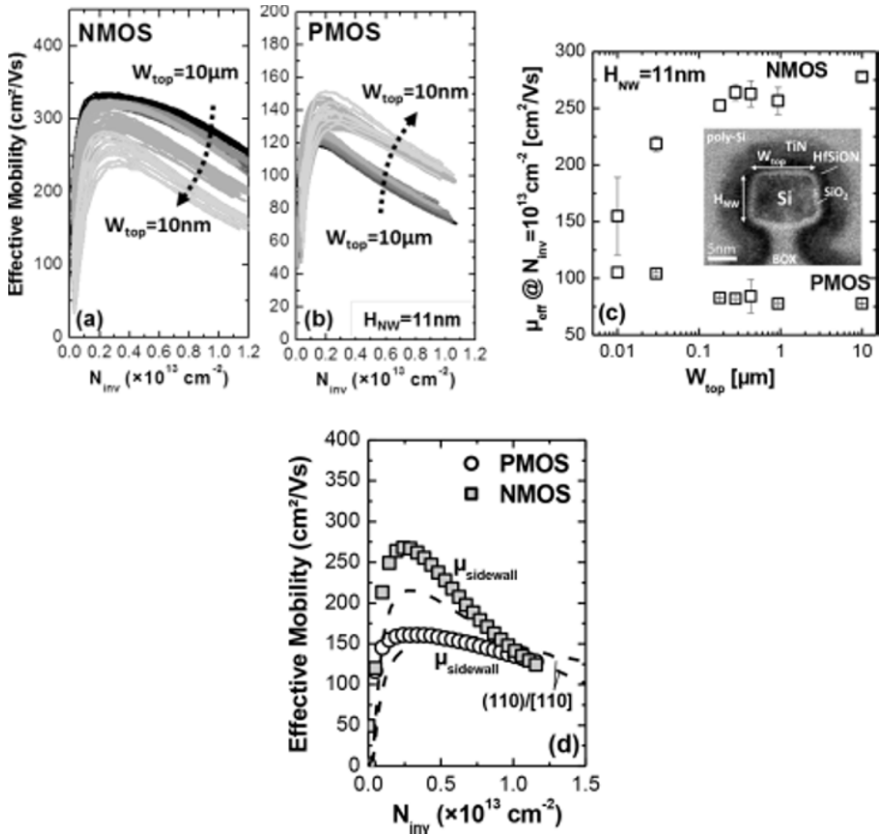


Figure 2.26. *Effective mobility measured as a function of inversion carrier density in SOI devices with varying widths from wide (W_{top} = 10 µm) to NW (W_{top} = 10nm) devices: a) NMOS; b) PMOS (L_g = 10 µm) [COQ 12a]; c) effective electron and hole mobility extracted at $N_{inv} = 10^{13}cm^{-2}$ as a function of W_{top}; d) extraction of the sidewall mobility $\mu_{sidewall}$ in NMOS and PMOS NW MOSFET using equation [2.5] (symbols, W_{top} = 18 nm), compared with (110)/[110] planar references (dotted lines): the sidewall mobility is governed by the (110) inversion surface properties*

2.2.3.1.2. Strain effect in NWs

The addition of a uniaxial strain is efficient to change the transport properties of NW devices (Figure 2.27) [TEZ 07, FAN 07, HAS 08, CAS 13], and can be exploited in order to improve, in particular, the electron mobility. A uniaxial tensile strain can be implemented in NWs, by starting from strained SOI (sSOI) wafers with an initial biaxial tensile stress [XIO 06, HAS 08, COQ 12, BAR 13]. After etching, the biaxial strain relaxes toward a uniaxial tensile strain along the channel direction of the NW, due to lateral strain relaxation [HAS 08, COQ 12]. Thus, strained NWs can be fabricated with uniaxial stress well above 1 GPa.

In Figure 2.27, electron mobility enhancement is obtained in NMOS strained Si (sSi) NWs that overcomes the electron mobility loss inherent to unstrained Si NWs with (110) sidewalls. For PMOS, the hole mobility is degraded by a uniaxial tensile stress along the channel, especially for a (100) inversion surface [SUN 07]. In (110) surface the better mobility in the unstrained case is counterbalanced by the detrimental effect of the uniaxial tensile strain. As a result, as the width is decreased the total hole mobility in sSi NWs is no more improved as compared to wide transistors, and remains roughly constant with W_{top} variation (Figure 2.27(b)).

The effect of the strain on transport properties in NWs can be more deeply understood by considering the band structure modification of Si NWs under mechanical stress [NIQ 12]. For NMOS NWs, a uniaxial tensile strain favors the proportion of electrons with the lowest effective mass and suppresses intervalley scattering. These two mechanisms contribute to enhance the electron mobility in strained NWs. The strain also has a significant effect on the transport effective mass of Δ_z valleys – i.e. in the lowest energy twofold degenerate subband – in (110)-oriented Si NWs. In particular a shear stress breaks the symmetry of the transverse mass of the Δ_z valleys, leading to the decrease of the transport effective mass for tensile strain ($\varepsilon_{\parallel} > 0$). The decrease of effective mass enhances the average velocity of the carriers, reduces intersubband scattering and therefore increases the mobility. For PMOS, the confinement of Si NWs tends to promote light hole (LH) bands in (110) directions. A compressive strain strengthens the LH character of the highest valence subbands, pushing heavy hole (HH) subbands downward. This leads to a large increase in mobility. However, a tensile strain brings HH subbands back up, which degrades the total hole mobility.

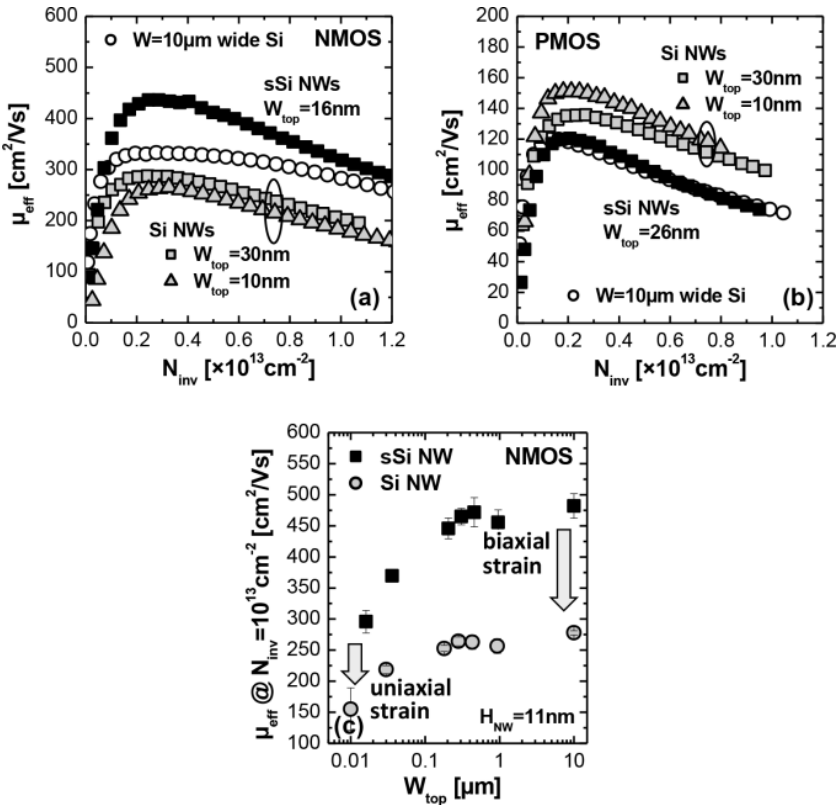


Figure 2.27. *a) NMOS and (b) PMOS effective mobility measured as a function of inversion carrier density N_{inv} by CV-split (L_g=10 µm) for unstrained and uniaxially strained (~1.4G Pa tensile strain along the (110) channel) SOI Tri-Gate (TG) NWs. Wide planar SOI reference (W=10 µm) is also given for comparison. Electron mobility enhancement and hole mobility decreasing is observed for strained NWs; c) electron mobility extracted at $N_{inv}=10^{13}$ cm^{-2} as a function of W_{top} for SOI and sSOI devices, showing enhancement for wide devices (due to biaxial tensile stress) down to NWs (due to uniaxial tensile stress)*

2.2.3.1.3. Piezoresistance measurement

The piezoresistive (PR) coefficients evaluate the mobility change $\Delta\mu/\mu$ due to a uniaxial stress applied perpendicularly (π_T) or longitudinally (π_L) to the channel direction. This set of coefficients provides an additional insight on the potentiality of strain in complex architecture like multigate NWs [SHI 06, CAS 12]. These coefficients are also used in technology computer aided design (TCAD) models to project the scalability of 3D architectures [NAI 13]. The PR coefficients can be measured using a four point bending

system [ROC 09] on 10 µm long devices to avoid the influence of access resistance. An external tensile uniaxial stress has been applied from 0 to 200 MPa longitudinally or perpendicularly to the (110)-channel direction to allow the extraction of the longitudinal π_L and transversal π_T. The PR coefficient is extracted by measuring the change of mobility $\Delta\mu/\mu$ with the applied stress σ, using:

$$\frac{\Delta\mu}{\mu} = -\pi_{L,T}\sigma \qquad [2.6]$$

The sign of $\pi_{L,T}$ denotes an increase or a decrease of mobility with a compressive ($\sigma < 0$) or a tensile ($\sigma > 0$) stress.

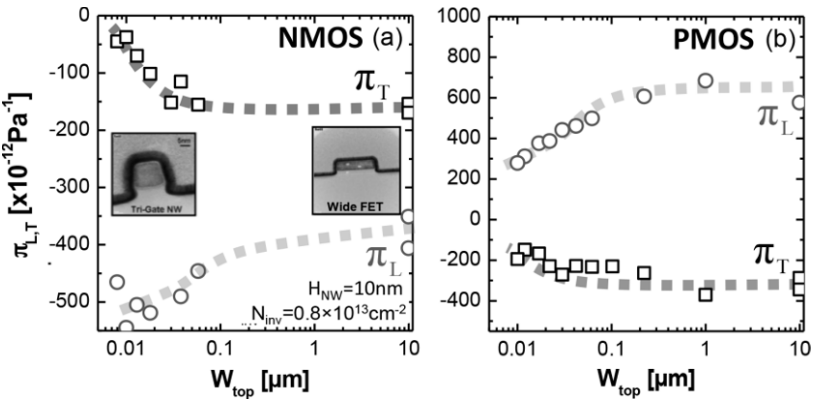


Figure 2.28. *Longitudinal and transversal piezoresistance coefficients as a function of the device width W_{top}: a) NMOS and b) PMOS (L_g=10 µm) [CAS 13]. A change in the effect of strain on transport properties is evidenced below a critical width W_{crit}≈60nm*

Figure 2.28 shows the evolution of π_T and π_L measured on long channel devices as the device width is narrowed from 10 µm down to 10 nm. A change in all the PR values is clearly observed on both NMOS and PMOS below a critical width W_{crit}≈60 nm. Below this value the strain effect on transport properties is affected by the dimensions of the channel, due to confinement and/or surface effects. The most striking feature is an increase of π_L by ~35% for NMOS with respect to wide devices. This result highlights the strong interest of a uniaxial tensile strain to enhance the

electron mobility in NWs. However, the transversal coefficient π_T decreases from 175×10^{-12} Pa^{-1} down to 0. The effect of stress on transport completely disappears for a stress applied perpendicularly to the channel direction. For PMOS, both π_L and π_T decrease in Si NWs with respect to wide devices. In particular, the longitudinal coefficient π_L is strongly reduced by ≈60%, down to $\pi_L = 280 \times 10^{-12}$ Pa^{-1} for 10 nm wide NW. However, this value, different from 0, indicates that a compressive stress should still be effective to enhance hole mobility in PMOS NWs.

2.2.3.2. *Interface quality assessment*

In multigate (MG) transistors (like Trigate (TG), Ω-Gate and GAA NW FETs), the interface between the oxide and the channel can play a determinant role on the electrical characteristics, through the SR or the interface traps, and due to specific process steps used to fabricate them [TAC 09]. In addition, the quality of the thermal SiO_2 in conventional SiO_2/polysilicon MOSFETs is rather well controlled, the introduction of new materials in the gate stack (such as high-k oxides, metallic gate and nitrided oxide) has a strong impact on the quality and their electrical characteristics [GAR 08].

2.2.3.2.1. Spectroscopic charge pumping

The interface quality of 3D architectures made on SOI can be characterized by an adapted charge pumping (CP) technique, using specific P-*i*-N structures (Figure 2.29) [ELE 88, VAN 91, CAS 10]. In this spectroscopic CP technique, a trapezoidal voltage pulse is applied to the transistor gate (Figure 2.29(a)) that alternatively fills the interface traps with electrons and holes, thereby causing a recombination current, I_{CP}, to flow in the P+ and N+ regions of the gated diode [ELE 88]. By varying the base level V_{base} from accumulation to inversion, with a constant amplitude ΔV_g greater than the value of the bandgap (ΔV_g = 1.3 eV is used here), the measured I_{CP} has a typical "hat" shape. The maximum of the two-level CP current can be expressed as [BRU 69, GRO 84]:

$$I_{CP} = qfA \int_{E_{em,h}}^{E_{em,e}} D_{it}(E)\, dE \qquad [2.7]$$

where A is the gate area and q the electron charge. The integration is done between the hole and the electron emission levels $E_{em,h}$ and $E_{em,e}$. Those energy levels are given by:

$$E_{em,h} = E_i + k_B T \ln\left(v_{th} n_i \sigma_p \frac{|V_{fb} - V_t|}{\Delta V_g} t_r \right) \quad [2.8]$$

$$E_{em,e} = E_i - k_B T \ln\left(v_{th} n_i \sigma_n \frac{|V_{fb} - V_t|}{\Delta V_g} t_f \right) \quad [2.9]$$

where E_i is the intrinsic Fermi level, V_{fb} the flat-band voltage, V_t the threshold voltage, k_B the Boltzmann constant, v_{th} the thermal velocity of carriers, n_i the intrinsic carrier density and $\sigma_{n,p}$ the capture cross-section of electrons or holes (see inset of Figure 2.29(b)). Equation [2.7] shows a linear relation between I_{CP} and frequency f. This simple relation allows the measurement of the mean value $\overline{D_{it}}$ integrated over the bandgap by sweeping the frequency of the pulsed signal $\overline{D_{it}} = 1/(qA\Delta E_{em} dI_{CP}/df)$. According to equations [2.8] and [2.9], the emission levels can be modulated by varying either the fall or rise time, or the temperature. In particular, varying t_r while keeping t_f constant, and vice versa, allows us to extract the D_{it} energy profile in the forbidden bandgap [GRO 84, VAN 91] using:

$$D_{it}(E_{em}) = \frac{1}{qAfk_B T} \frac{dI_{CP}}{d \ln t_{r,f}} \quad [2.10]$$

where $t_{r,f}$ is the rise or fall time depending on the energy range scanned within the bandgap. Finally, changing the temperature allows us to scan a broader range of energy. Low temperatures down to 25 K thus give access to the energy distribution close to the conduction and the valence band of Si in a typical ±(0.58–0.3) eV energy range (Figure 2.29(b))[4]. The value of the capture cross-section $\sigma_{n,p}$ is difficult to determine experimentally. However, an error on this parameter only results in a shift in the energy axis (limited to 120 meV for $\sigma_{n,p} = 10^{-15}$–10^{-17} cm^2) and does not change the results in a significant way. In the case of CMOS technology, a constant value equal to 10^{-16} cm^2 is a physically acceptable value [GRO 84, VAN 91]. Due to the derivative used in equation [2.10], and for the small geometries of the

4 Notice that the energy bandgap of the Si increases at low temperature, reaching 1.17 eV at 25 K.

measured devices, the measurement sensitivity of this spectroscopic CP technique is around 10^{11} eV^{-1} cm^{-2}.

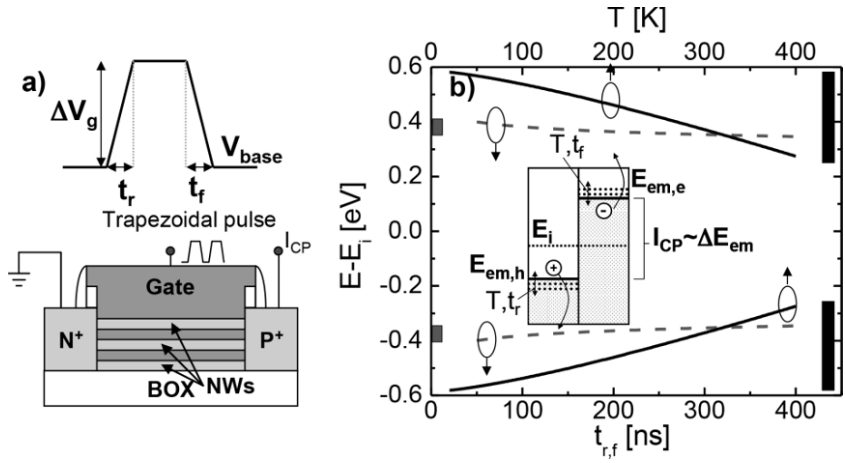


Figure 2.29. *a) Schematics of the experimental setup used for CP; a trapezoidal pulse is applied to the gate and CP current is measured on the P+ contact; b) energy range scanned by temperature modulation from 20 to 400 K (bold line) or by rise/fall time modulation (dashed line), as calculated from equations [2.8] for Si. Inset: Schematics of the physical mechanism involved during CP measurements. The electron and hole emission levels E_{em} can be scanned by changing temperature T and/or the rise or fall time $t_{r/f}$*

Figure 2.30 shows the energy profile of D_{it} measured for Si NW transistors with a rectangular and a circular cross-section, using the spectroscopic CP technique [TAC 09, CAS 10]. 3D-stacked Si NW transistors matrices were fabricated by an epitaxial growth of an $Si/Si_{0.8}Ge_{0.2}$ superlattice on (001) oriented SOI substrates and isotropic removal of SiGe layers [TAC 09]. The Si NW transistors have either a rectangular (W = 20 nm × H_{NW} = 15 nm) or a circular cross-section (diameter d = 25 nm). Circular cross-sectional shaped silicon NWs are formed by an additional H_2 annealing at 750°C for two minutes before the gate deposition. A uniformly surrounding gate stack has been fabricated with an SiO_2-like interfacial layer (t_{IL}≈1.5–2 nm), 3 nm thick HfO_2 dielectric and a 10 nm TiN metal gate layer. The resulting equivalent oxide thickness (EOT) is 2.6 nm. The channels of the NWs are oriented along the (110) direction. The NWs are vertically

stacked on three levels, and horizontally arrayed leading to a total of 150 parallel wires. Wide planar (100) SOI MOSFETs, with 10 nm silicon film thickness, and with the same high-k/metal gate stack were used as a reference.

The energy profiles reveal an asymmetry between the upper part (Figure 2.30(a)) and the lower part (Figure 2.30(b)) of the Si bandgap. In the upper part of the bandgap, the trap density is much higher than in the lower part of the bandgap, due to dangling bonds (Pb-centers) [SCH 07], combined with N-generated defects [GAR 08, CAS 11]. The latter generally induce a peak density in the upper part of the bandgap, visible for the planar reference. For both rectangular and circular NWs, the energy profile $D_{it}(E)$ is modified compared to references as follows: (1) less asymmetry is observed between the upper part and the lower part of the bandgap and (2) a higher mean density D_{it} is measured (up to five times more for circular NWs). The lower asymmetry could indicate the different nature of defects for NWs. This difference could result from the lower impact of *N* diffusion in NWs, due to a thicker interfacial oxide (1.5–2 nm), compared to planar devices (1 nm). More Pb-centers could also be present in Si NW transistors. Indeed, more dangling bonds are generally measured on (110) plane, i.e. the orientation of the sidewalls in the case of rectangular shape (110)-Si NWs [SCH 07, MAE 04]. The circular NWs exhibit the highest D_{it}, roughly two times larger than rectangular NWs. This high value occurs despite the H_2 annealing, which is known to passivate some defects such as dangling bonds [REE 88]. This latter result highlights the sensitivity of the interface quality to the technological process (in this case the etching of the sacrificial SiGe layers).

These defects have an influence on the transport properties. Earlier works have shown that interface traps at the Si/SiO_2 interface are acceptor-like in the upper half and donor-like in the lower half of the Si bandgap [GRA 66, SCH 07]. For NMOS, in strong inversion the Fermi level E_F lies above the intrinsic Fermi level E_i. All the traps below E_F are filled with electrons so that those between E_i and E_F are negatively charged (occupied acceptors) whereas those below E_i are neutral (occupied donors). These negative charges can in turn induce an additional Coulomb scattering with carriers flowing in the channel [CAS 10].

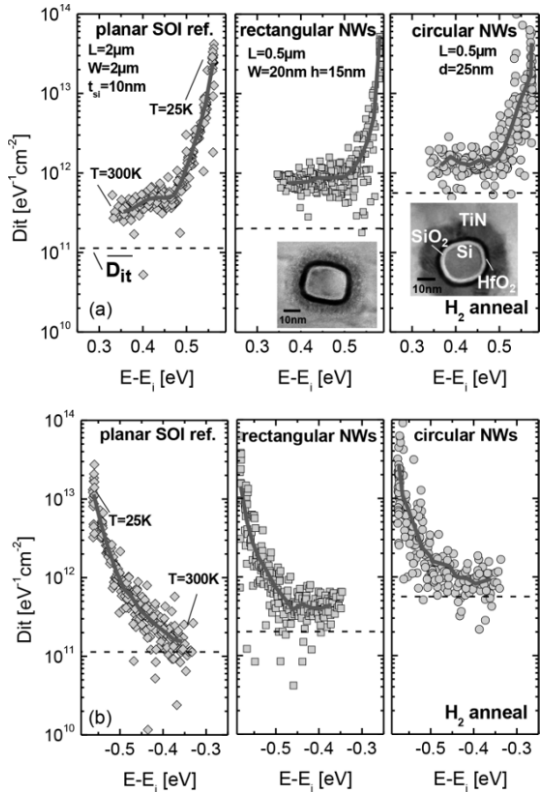


Figure 2.30. *Energy distribution of interface traps (symbols) for circular, rectangular and planar SOI devices with the same gate stack (3 nm HfO_2 ALD/10 nm TiN CVD): a) upper half part of the bandgap and b) lower half part of the Si bandgap [CAS 10]. The profile is obtained by scanning the temperature from 300 K down to 25 K by 25 K steps. The bold line represents the mean value of $D_{it}(E)$. The dashed line is the directly measured mean value of interface trap density, $D_{it,}$ over the full energy range at 300 K which evidences the lower density of interface traps in the middle of the gap. Insets: cross-sectional TEM images of the vertically stacked Si NWs (3 levels-NWs) with a rectangular and circular cross-section. For color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

2.2.3.2.2. Low frequency noise measurements

It is commonly accepted that low frequency (LF) noise measurements can be employed as characterization tools for the quality or reliability of MOS devices. Indeed, as recalled below, the LF noise can provide unique information about the slow oxide border trap density. This feature has often been exploited for the assessment of the oxide quality after various technological/electrical treatments such as nitridation [JAY 89, MOR 96],

stressing under uniform [MAE 85, SIM 93] or hot carrier injections [FAN 86] and irradiation [MEI 90]. With the advent of NW MOSFETs, it becomes a promising tool for interface characterization, since LF noise is enhanced as the devices are scaled.

In the classical carrier number fluctuation approach, the fluctuations in the drain current stem from the fluctuations of the inversion charge nearby the Si-SiO_2 interface, arising from variations in the interfacial oxide charge after dynamic trapping/detrapping of free carriers into slow oxide border traps. These interface charge fluctuations δQ_{it} can be equivalently equated to a flat band voltage variation $\delta V_{fb} = -\delta Q_{it}/(WLC_{ox})$. Moreover, in a more detailed analysis one should also take into account the supplementary mobility change $\delta\mu_{eff}$ due to the modulation of the scattering rate induced by the interface charge fluctuations. The normalized drain current and input gate voltage noise $S_{Vg} = S_{Id}/g_m^2$ for strong inversion read [GHI 91]:

$$S_{Id}/I_d^2 = \left(1 + \alpha\mu_{eff} C_{ox} I_d / g_m\right)^2 \left(\frac{g_m}{I_d}\right)^2 S_{Vfb} \qquad [2.11]$$

and

$$S_{Vg} = S_{Vfb}\left[1 + \alpha\mu_0 C_{ox}(V_g - V_t)\right]^2 \qquad [2.12]$$

where g_m is the transconductance, μ_{eff} is the effective mobility, α is the Coulomb scattering coefficient ($\approx 10^4$ Vs/C for electrons and 10^5 Vs/C for holes) for equation [2.11]. For equation [2.12], μ_0 is the low field mobility, C_{ox} is the gate oxide capacitance, V_t is the threshold voltage, $S_{Vfb} = S_{Qit}/(WLC_{ox}^2)$ with S_{Qit} ($C^2/Hz/cm^2$) being the interface charge spectral density per unit area, W being the device width and L being the device length.

The spectral density of the oxide interface charge essentially depends upon the physical trapping mechanisms into the oxide. For a tunneling process, the trapping probability decreases exponentially with oxide depth x, so that the flat band voltage spectral density takes the form [CHR 68, MCW 57],

$$S_{Vfb} = \frac{q^2 kT\lambda N_t}{WLC_{ox}^2 f^\gamma} \qquad [2.13]$$

where f is the frequency, γ is a characteristic exponent close to 1, λ is the tunnel attenuation distance (≈0.1nm), kT is the thermal energy and N_t is the volumetric oxide trap density (/eV/cm^3).

For a thermally activated trapping process [DUT 81], the trapping probability decreases exponentially with the cross-section activation energy E_a, so that the flat band voltage spectral density reads [SUR 88]:

$$S_{Vfb} = \frac{q^2 k^2 T^2 N_{it}}{WLC_{ox}^2 f^{\gamma} \Delta E_a} \qquad [2.14]$$

where ΔE_a is the amplitude of the activation energy dispersion and N_{it} is the oxide trap surface state density (/eV/cm^2). In both trapping mechanisms, the $1/f$ nature of the spectrum stems from the uniform distribution in log scale of the involved time constants [VAN 79].

A generic procedure for the diagnosis of the excess LF noise sources in a MOS transistor can be drawn from the above analyses [GHI 91]. The normalized drain current noise versus drain current characteristics in log-log scale can first be inspected for comparison with equation [2.11]. If the normalized drain current spectral density varies with drain current as the transconductance to drain current ratio squared, one can likely conclude that carrier number fluctuations dominate. Furthermore, if the associated input gate voltage noise shows a parabolic dependence with gate voltage at strong inversion, correlated mobility fluctuations might be involved ($\alpha >> 1$ in equation [2.12]).

Figure 2.31 gives typical examples of $S_{Id}/I_d^2(I_d)$ characteristics for 0.18 μm CMOS devices and which illustrate the very good correlation between the normalized drain current noise and the transconductance to drain current ratio squared from weak to strong inversion. Therefore, in this case, it can be inferred that carrier number fluctuations are the main LF noise source. This behavior is representative of modern N and P channel devices ($L < 0.35$ μm) in which both device types operate in surface mode due to the dual polygate material. In contrast, for 0.35 μm technology, it was found that P-type transistors obey the Hooge mobility model due to the buried architecture of the channel with N^+ Si polygate [GHI 94]. Therefore, in general, for surface mode operated MOSFETs, the LF noise is found to result from carrier number fluctuations whereas, for volume mode operated

devices, Hooge mobility fluctuations should contribute more. However, in P MOSFETs with SiGe buried channel, the LF noise is found to be governed by carrier number fluctuations at high drain currents, while at lower values, Hooge mobility fluctuations could appear [GHI 02]. This is due to the fact that the surface potential fluctuations due to the trapping/detrapping of holes from the surface channel indirectly generate fluctuations in the SiGe buried channel carrier population, and, in turn, in the corresponding drain current [GHI 02].

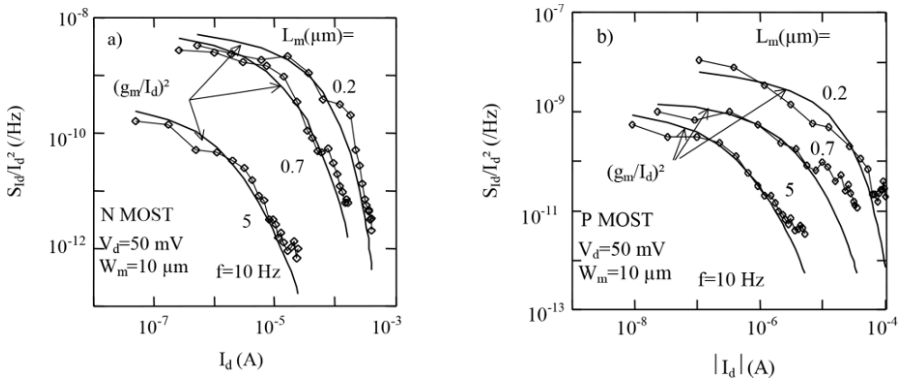


Figure 2.31. *Variation of normalized drain current noise versus drain current for a) N channel and b) P channel devices from 0.18µm CMOS technologies [BOU 98]*

MG architectures are very attractive candidates for future MOSFET technology nodes, due to their good electrostatic integrity, immunity against SCE and drain induced barrier lowering [FER 11]. However, the controlled quality of multiple interfaces could be a serious issue in these 3D devices. The interfacial surfaces with different crystallographic orientation may contribute to the total electrostatic characteristics. Low-frequency noise (LFN) measurement is an efficient diagnostic tool to evaluate the electrical properties of these complex interfaces [ZHU 09, WEI 09, BEN 09, BAE 11, FEN 11, LEE 12, THE 12, LEE 13, JAN 10, JAN 11, KOY 13b]. Therefore, the understanding of these LFN characteristics in MG devices with aggressively shrunk dimensions in all regions of the FET operation is important. Generally, LFN spectra contain $1/f$ and Lorentzian ($1/f^2$) components that are mainly dominated by charge traps in the gate oxide. Concerning $1/f$ noise, the origin in MG devices has been attributed to carrier number fluctuations with correlated mobility fluctuations (CNF + CMF) [JAN 10, JAN 11, KOY 13b].

The LF noise has been investigated in c-strained and un-strained 3D stacked Si0.8Ge0.2 core-shell NW p-MOS devices with different gate lengths [JAN 10]. To this aim, 3D stacked SiGe NW p-MOS transistors with high-k/metal gate stacks were fabricated. SOI (001) wafer and tensile-strained (1.3GPa) SOI (001) wafer were used for c-strained SiGe NWs and un-strained SiGe NWs, respectively. $Si/Si_{0.8}Ge_{0.2}$ superlattices were epitaxially grown on the wafers by reduced pressure – chemical vapor deposition. A 2 nm thick Si capping layer was grown at 650°C on the liberated SiGe NWs to achieve higher mobility. Then, an HfO_2 (3 nm)/TiN (10 nm)/polySi gate stack was deposited on NWs. Figure 2.32 shows a typical cross sectional TEM image of 3D-stacked SiGe NWs with high-k/metal gate stacks.

As it is shown in Figure 2.33, the overall pattern of normalized drain current noise varied according to the $(g_m/I_d)^2$ characteristic of the transistor and not as according to the reciprocal of the drain current. This clearly suggests that the LF noise in such SiGe NW does stem from CNF (equation [2.11]). The corresponding trap density (N_t) was extracted from the flat-band voltage fluctuations (S_{Vfb}) using equation [2.13] and found in the range of 4×10^{18} to 6×10^{19} $cm^{-3}eV^{-1}$ for both devices [JAN 10]. The extracted N_t values are comparable to those obtained in high-*k* MOS planar devices, both of which are 10–50 times larger than in bulk silicon MOSFETs with SiO_2 gate oxide. It should also be noted that, at high drain current, the normalized current noise decreases less drastically than $(g_m/I_d)^2$ due to the presence of additional correlated mobility fluctuations (see equation [2.11]). In the case of the un-strained SiGe NWs, N_t is 3–4 times larger in the short channel than in long devices, whereas for c-strained SiGe NWs, it is slightly reduced [JAN 10].

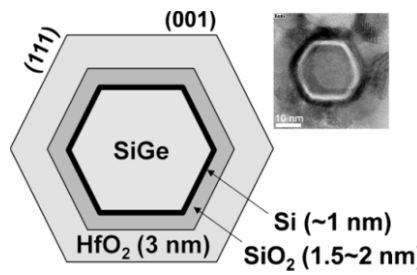


Figure 2.32. *1 Schematic and a corresponding TEM image of core-shell NW structures with Si cap and SiGe core [JAN 10]*

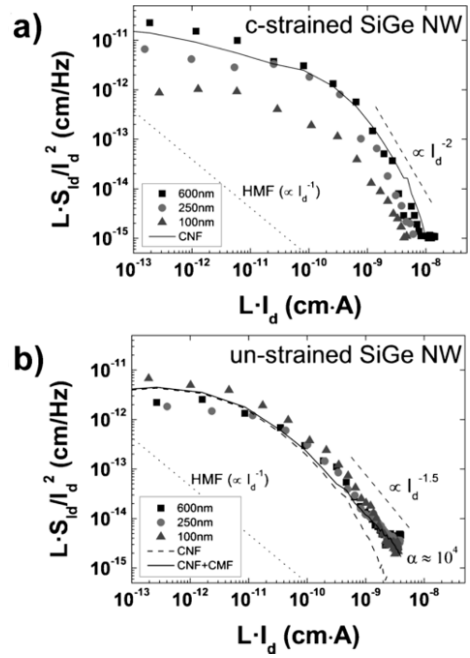


Figure 2.33. *Noise normalized by the drain current and the channel length of a) c-strained SiGe NWs and b) un-strained SiGe NWs at V_{ds} = 50 mV and f = 20 Hz. Black lines are fitting curves for each 600 nm device [JAN 10]*

The LF noise has also been measured in trigate (TG) SiNWs fabricated using the top-down approach by optical lithography followed by a resist trimming process [KOY 13b]. The NWs with a (110)-oriented channel were fabricated on an undoped (100) SOI wafer with 11 nm Si thickness (thus constituting the sidewall height H (Figure 2.34) and 145 nm thick buried oxide. These MOSFETs have high-k/metal gate stack consisted of 2.3 nm CVD HfSiON, 5 nm ALD TiN covered with 50 nm poly-Si. The total EOT is 1.25 nm for both reference wide devices and TGNW FETs. N-type FET structures with top widths W_{top} from 10 µm (wide FET) down to 10 nm, and with a single channel or 50 channels in parallel (1ch- and 50ch-TGNWs) were studied. For TGNW FETs, the total effective width is given by $W_{tot} = N_{ch} \times (W_{top} + 2H)$, where N_{ch} is the number of channels (1 or 50).

Figure 2.35 shows typical S_{Id}/I_d^2-I_d characteristics normalized by channel area parameters (W_{tot} and L_g) for all device structures. LFN data for wide FET and 50ch-devices with W_{top} from 180 nm to 10 nm are almost merging,

indicating that LFN behavior has a simple W_{tot} dependence. Moreover, this also exhibits that there is no large contribution of surface orientation difference between (100) top and (110) sidewall surfaces to LFN in TGNW devices. These findings are in good agreement with reports on bulk wide FETs fabricated on (100) and (110) Si oriented wafers. However, the LFN data for some 1ch-NW samples does not coincide with the general trend. This specific noise level behavior could be attributed to the sample-to-sample LFN variability effect reinforced in ultrascaled devices, and not observed in 50ch-NWs, where it is largely reduced by an averaging process [KOY 13b].

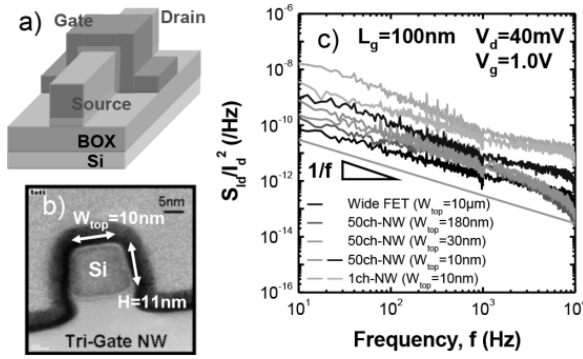


Figure 2.34. *a) Schematic view, b) cross-sectional TEM image of the channel for TGNW FET and c) frequency dependence of the normalized drain current noise S_{Id}/I_d^2 for all devices in linear and strong inversion regions [KOY 13b]. For color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

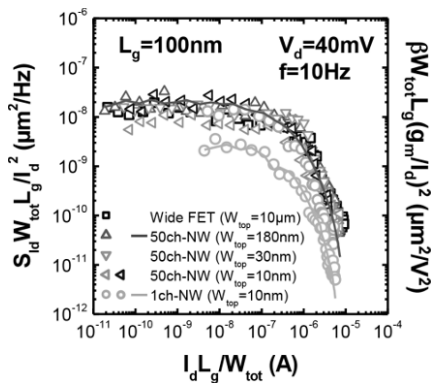


Figure 2.35. *Normalized S_{Id}/I_d^2 (symbols) and $(g_m/I_d)^2$ (lines) characteristics vs I_d normalized by channel area parameters (W_{tot} and L_g) in all wide, 50ch- and 1ch-TGNW FETs [KOY 13b]*

Figure 2.36 shows the typical variation of oxide trap density N_t extracted using equation [2.11] and [2.13] as a function of the effective NW width [KOY 13b]. The trap density is slightly deceasing for small gate width, which is likely due to SCEs and falls in a range close to 10^{18}/eVcm^3, which is the standard value for such high-k metal gate stacks. In Figure 2.37, the evolution with W_{tot} of the corresponding Coulomb scattering parameter, $\alpha_{sc}\mu_{eff}$, controlling the CMF mechanism are reported. It takes values in agreement with those generally found for bulk silicon MOSFETs [ION 12]. Both N_t and $\alpha_{sc}\mu_{eff}$ values are close to those obtained in state-of-the-art planar MOS devices, which reveals that such aggressively scaled silicon or SiGe NWs have nevertheless a well-optimized interface quality.

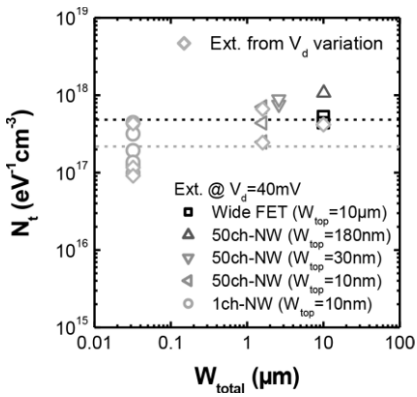


Figure 2.36. *Gate oxide trap density N_t as a function of the W_{tot} [KOY 13b]*

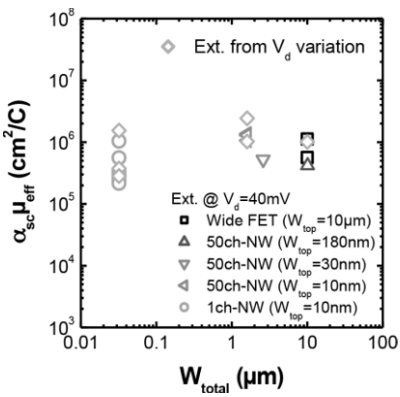


Figure 2.37. *Coulomb scattering parameter $\alpha_{sc}\mu_{eff}$ as a function of the total effective channel width W_{tot} [KOY 13b]*

2.3. Nano-CMOS ultimate memories[5]

2.3.1. *Overview of memory*

Aggressive scaling of semiconductor memory cells and the dramatic increase in memory array size demand a highly scalable cell structure with low cost and low power consumption. Until now, the floating-gate technology, including both NOR and NAND flash memories, has been sufficient for NVM developments because of the scalability of memory cell-size and the corresponding reduction in production cost [ITR 06]. However, this conventional memory scaling strategy is expected to face technical and physical limitations in the near future [LU 13]. This can be reasoned from the following three aspects using NAND flash memory as an example, as illustrated in Figure 2.38:

– geometric limitations imposed by gate coupling ratio (GCR) and tunneling oxide thickness;

– wordline-to-wordline (WL-to-WL) interference for scaling beyond 20 nm technology node;

– Fewer available electrons being stored in the cell to reliably represent program state.

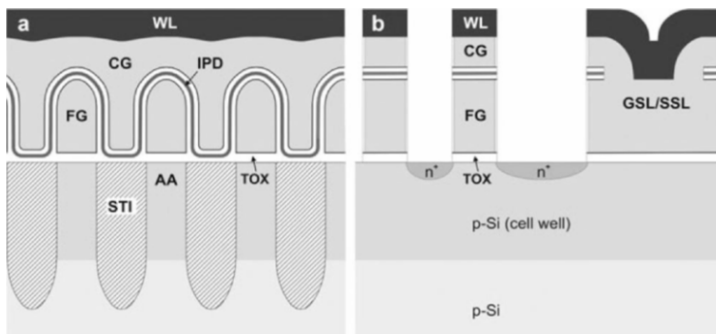


Figure 2.38. *Schematic cross-section of a floating-gate cell in a a) word-line (WL) direction and b) bit-line (BL) direction [MIC 13]*

In order to overcome the impending scaling limitations, two solutions have been proposed (as shown in Figure 2.39): (1) to develop evolutive

5 Section written by Zheng FANG, Xin Peng WANG, Guo Qiang LO and Dim-Lee KWONG.

charge-based NVM technologies such as realizing 3D (dimensional) flash memory cells from 2D structures; and (2) to exploit new, emerging memory concepts that show larger room and better potential in scalability. Owing to the unique advantages, NW technology has been a topic of interest in both evolutionary and disruptive solutions.

In the next section, we will review the current status of NW technology in the applications for NVM development.

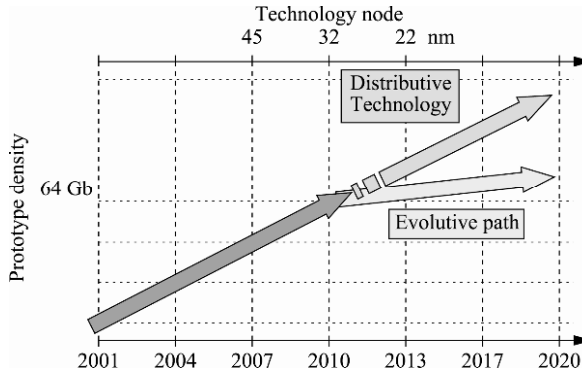


Figure 2.39. *Two solutions of NVM scaling beyond 22 nm nodes: along either disruptive or evolutive path [IMS 10]*

2.3.2. *NW application in the evolutive solution path*

From the viewpoint of evolutive NVM cell structures development, various multi-gate architectures including double-gate, tri-gate, Π-gate, Ω-gate and gate-all-around (GAA) [HIS 98, DOY 03, PAR 01, YAN 02, COL 90] have been extensively studied in pushing NVM scaling further in the technology roadmap. Compared to planar cells, the multi-gated structures exhibit improved GCR, as well as enhanced electrostatic control and immunity to short channel effects (SCE). As these architectures usually employ fin, cylinder or arch-shaped active profile along with multi-gate control, it provides additional suppression of SCE with low subthreshold slope (SS), drain induced barrier lowering DIBL and reduced threshold voltage (V_{th}) roll-off. Besides device architecture, different gate stacks have also been explored for charge trapping type memory, such as (SONOS) Silicon-Oxide-Nitride-Oxide-Silicon, which has superior scaling capability as it is immune to the capacitive-coupling issue and enables the adoption of

thin gate stacks for better electrostatic control [LEE 02]. In SONOS memory, electrons are stored in the discrete trapping sites in the nitride layer and high program speed can be achieved while maintaining good retention. However, SONOS memory also has its own problem such as slow de-trapping rate [WHI 00]. Moreover, the 2D scaling of SONOS is similarly limited by the small number of electrons when the volume of charge storage node becomes small.

Among all multi-gate concepts, the GAA vertical NW field effect transistor (FET) is recognized as one of the strongest potential candidates to advance the CMOS technology towards extreme miniaturization limits, due to its optimal electrostatic control [END 03]. Also, owing to the cylindrical geometry and the inverse logarithmic dependence of the insulator capacitance on the oxide thickness, the gate length in these devices can be scaled further with channel diameter (for instance, close to 10 nm scale) without reducing the gate dielectric physical thickness. Therefore, GAA cylindrical-shaped vertical NW devices represent the most suitable architecture for SONOS-type NVM applications.

Vertical silicon nanowire (SiNW) SONOS memory for ultra-high density application was reported by Chen *et al.* in 2009 [CHE 09b] in which the fabrication process flow and characterization of GAA SONOS Flash memory were presented and a highly scaled SiNW with diameter down to 50 nm was achieved using CMOS compatible technology. Figure 2.40 illustrates the process flow of SiNW SONOS memory fabrication. It is noted that the devices exhibited well-behaved memory characteristics, in terms of P/E (programming/erasing) window, retention and endurance. As such, it was considered the key building block to realize 3D multilevel memory technology.

Shortly after, Sun *et al.* demonstrated multibit programmable SiNW SONOS memory using a similar approach [SUN 10]. The memory devices realized on highly scaled squarish SiNW, down to 20 nm in diagonal (as shown in Figure 2.41), showed much improved P/E speed and window along with good retention and endurance characteristics when compared to those with a large dimension. Detailed P/E characteristics of 20 nm devices as well as a comparison of P/E speed, retention and endurance with 50 nm devices are presented in Figure 2.42, wherein the P/E window is expected to be further improved with optimized gate stacks.

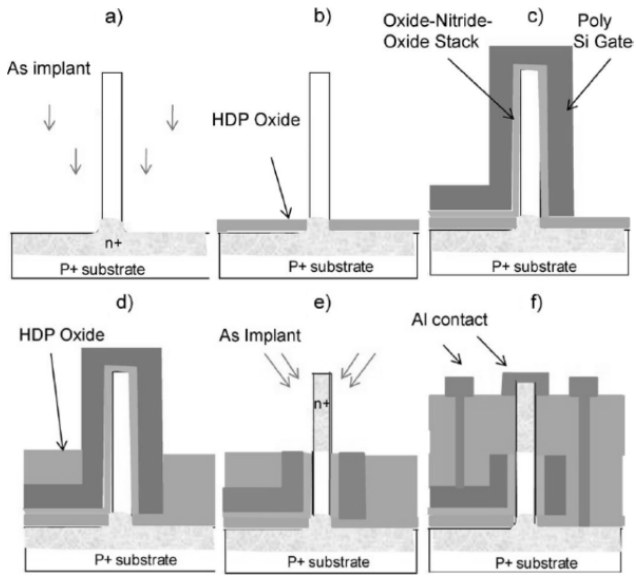


Figure 2.40. *Schematic process flow of the vertical SiNW SONOS Flash memory fabrication: a) vertical SiNW formation and As implantation to form the source; b) high density plasma (HDP) isolation oxide formation; c) oxide–nitride–oxide (ONO) stack deposition followed by poly-Si gate deposition and then gate definition; d) another HDP isolation oxide to define the gate length; e) poly-Si gate and ONO stack etch back to form the desired gate length, and As implantation to form the drain; (f) Final metal contact formation [CHE 09b]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

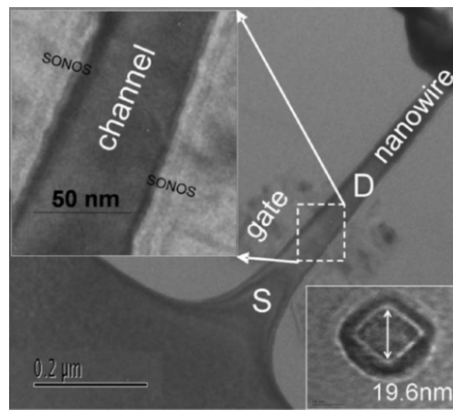


Figure 2.41. *Transmission electron microscopy (TEM) images of vertical SiNW memory with gate length of ~150 nm, SONOS stack of $SiO_2/Si_3N_4/SiO_2$ ~4.5/5/5 nm and SiNW diameter of 50 nm. Inset at bottom right corner shows the planar TEM image of SiNW device with a diameter of 20 nm [SUN 10]*

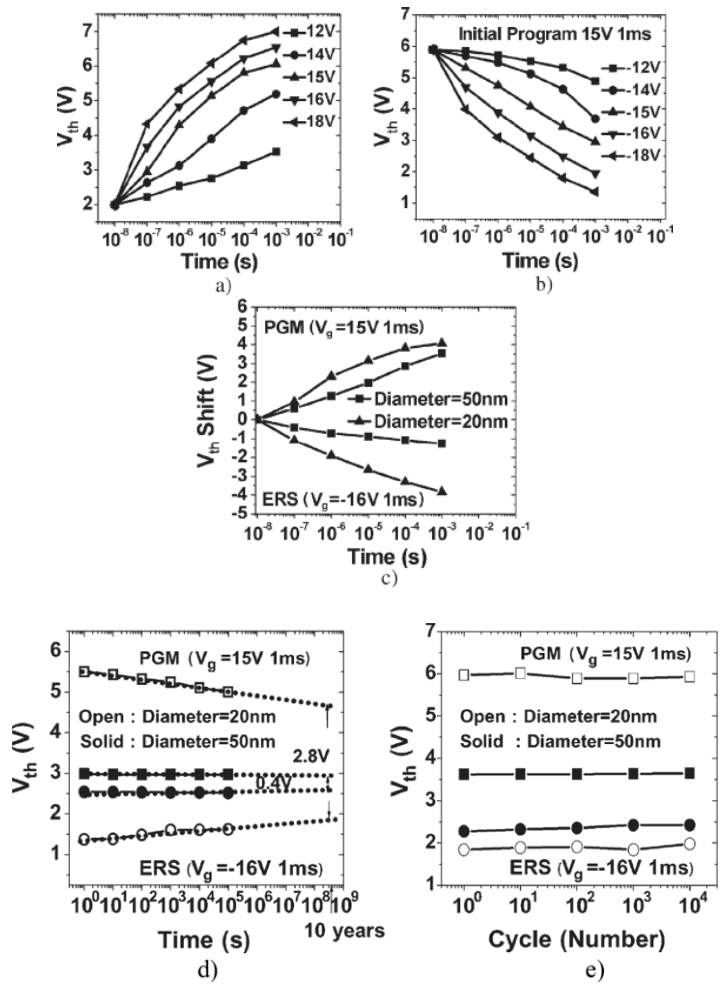


Figure 2.42. *a) Programming and b) erasing characteristic of vertical SiNW SONOS memory (gate length ≈ 150 nm and diameter = 20 nm). c) Comparison of the P/E characteristics, d) retention, and e) endurance of devices with diameters of 50 nm and 20 nm [SUN 10]*

The improvement came from the concentrated e-field near the silicon channel when the SiNW diameter was scaled to the value that was comparable to oxide–nitride–oxide (ONO) stack layer thickness, as described by Sun *et al*. In addition to that, the e-field could be further enhanced at the corners of the squarish NW due to smaller radius of curvature [SUN 10], to give a much concentrated e-field in the tunnel oxide

and a corresponding reduced value in the block oxide. For charge trapping devices working under Fowler–Nordheim (FN) tunneling mechanism, the tunneling current is related to the e-field in an exponential way, thus the large tunneling current in the ultra scaled squarish device is expected to improve the programming speed. Other than that, the weakened e-field in the blocking oxide reduces the leakage current from the trapping layer to the poly-Si control gate, which further improves the programming speed. Similarly, the smaller dimension also contributes positively to the erasing process.

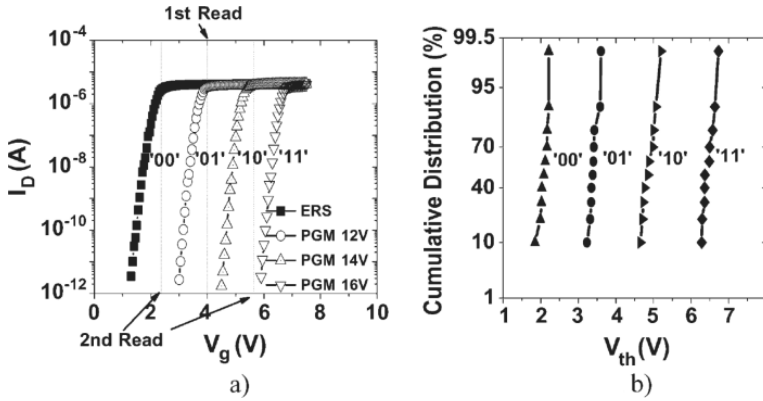


Figure 2.43. *Vertical SiNW (with dimension of 20 nm): a) multibit programming with different gate biases for 1 ms. b) Cumulative distribution of multibit programmed V_{th} with gate biases of 12 V, 14 V, and 16 V for 1 ms for randomly selected ten devices [SUN 10]*

Benefiting from the sufficiently large memory window and good gate control, ultra scaled SiNW devices with diameter of 20 nm also exhibit multibit programming capabilities as shown in Figure 2.43. Devices are programmed under the various gate voltages of 12 V, 14 V and 16 V for 1 ms: during the first read operation, “00” and “01” states can be distinguished from “10” and “11”; after that “00” from “01” and “10” from “11” at 2.4 V and 5.8 V, respectively. In Figure 2.43(b), cumulative V_{th} is plotted for 10 random selected devices, showing excellent distributions.

Furthermore, Sun *et al.* [SUN 11] presented a NAND memory string based on 2-level stacked junction-less (JL) GAA SONOS cells fabricated on vertical SiNW platform, achieving $6F^2/2$ footprint at International Electron Devices Meeting (IEDM) 2011 and the corresponding fabrication process of the stacked architecture is shown in Figure 2.44.

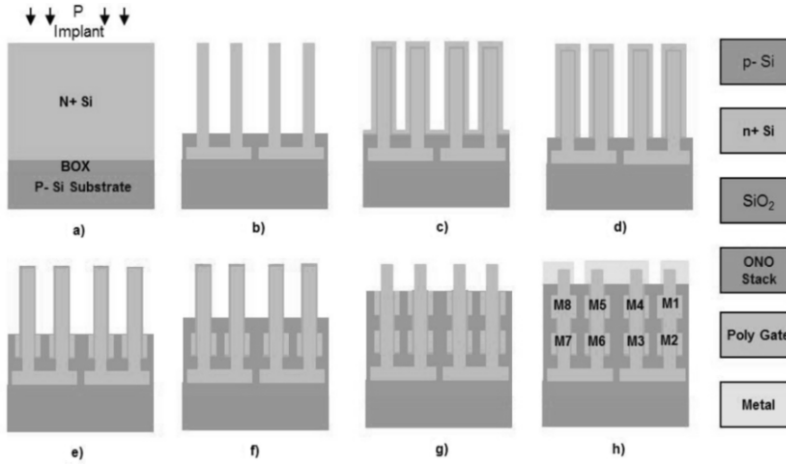


Figure 2.44. *Process integration flow for NAND string of eight junction-less SONOS memory cells (M1-M8) on four vertical SiNWs: a) bulk implant and annealing; b) vertical SiNW formation and HDP isolation; c) 1st level gate stack deposition; d) 1st level gate pad definition; e) tip poly removal; f) HDP oxide isolation; g) 2nd level gate pad definition and tip poly-ONO removal; h) metallization. M1 to M8 are 8 cells on 4 wires [SUN 11]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

Figure 2.45 is the cross-sectional TEM image of 2-level stacked JL SONOS memory cell. The vertical stacked structure improves device density and absence of junctions reduces process complexity, making this kind of device one step closer to the real product in terms of cost.

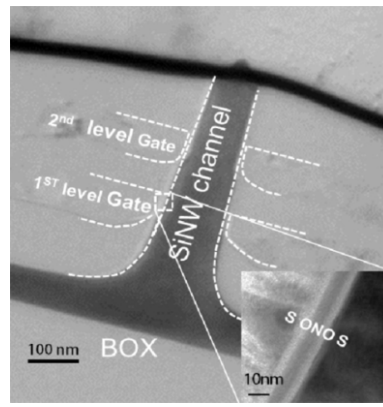


Figure 2.45. *Cross-sectional TEM image of 2-level stacked JL GAA SONOS memory cell with SiNW diameter of ≈120 nm and gate length of ~100 nm. Inset shows the ONO stack using here of oxide/nitride/oxide at 5/7/7 nm [SUN 11]*

The P/E characteristics of the top- and bottom-level cells are quite similar, as illustrated in Figure 2.46 that shows a memory window of 3.4 V when P/E time of 10 ms is used at +15 V and –18 V, respectively. In addition, similar to devices presented in Figure 2.43, multibit programming can also be achieved in the current stacked cells with proper P/E conditions [SUN 11].

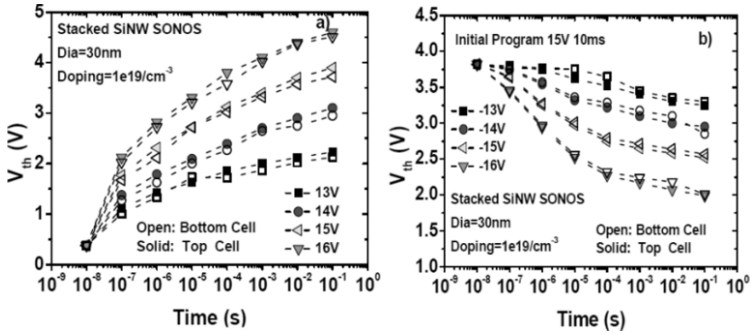


Figure 2.46. *a) Programming and b) erasing characteristics of stacked JL SONOS memory cell with SiNW diameter of 30 nm. Open and solid symbols represent bottom-level and top-level cell in the stack respectively [SUN 11]*

2.3.3. *NW technology along the disruptive solution path*

As another solution path, several emerging NVM technologies are under exploration, such as PCRAM [OVS 68], STT-MRAM [CHU 10] and resistive random-access memory (RRAM) [BAE 05]. Among them, RRAM has attracted considerable attention for the potential as the next generation NVM. RRAM based on the working principle of electrical bias induced resistance change was first reported in the 1960s [HIC 62], while the current wave of resistive switching for memory exploration started in the late 1990s with efforts spearheaded by Asamitsu *et al.* [ASA 97], Kozicki *et al.* [KOZ 99] and Beck *et al.* [BEC 00].

The RRAM cell has a simple metal–insulator–metal (MIM) structure. Two metal electrode materials might be the same or different for top and bottom electrodes. The switching layers between the electrodes may vary from a large range of material choices. At present, various transitional metal oxides (TMO) have been explored as switching layer candidates for their simple compositions, CMOS compatibility and reported outstanding performances [LEE 08].

In order to realize high density memory array, crosstalk between adjacent cells should be avoided by adapting one selection device with one resistor. The RRAM cell in one-transistor one-resistor (1T1R) configuration has been implemented with a planar transistor, as previously reported [LEE 08, YUA 09]. However, the minimum footprint for planar 1T1R cells is $6F^2$, in which F stands for the minimum feature size. In 2010, RRAM cells integrated with 3D vertical bipolar junction transistor (BJT) was demonstrated to have $4F^2$ footprint [CHI 10]. It was the first attempt to use transistors as selective devices with $4F^2$ density, whereas BJT has a high leakage current and may also increase process complexity if implemented along with CMOS logic circuit. Compared to that approach, a more direct method to achieve $4F^2$ density is to integrate the RRAM cell with GAA vertical nanopillar (VNP) transistor, of which the cell size is $4F^2$ [KWO 12]. GAA VNP transistors exploit the unique advantages of NW GAA architecture, which has been demonstrated as a feasible option for 15 nm and beyond technology nodes with sub-10 nm channel length devices by both simulations and experiments [GNA 06, JIA 08]. Such demonstration was first reported by Wang *et al.* with HfO_x based RRAM stack in IEDM 2012 [WAN 12], as shown in Figure 2.47.

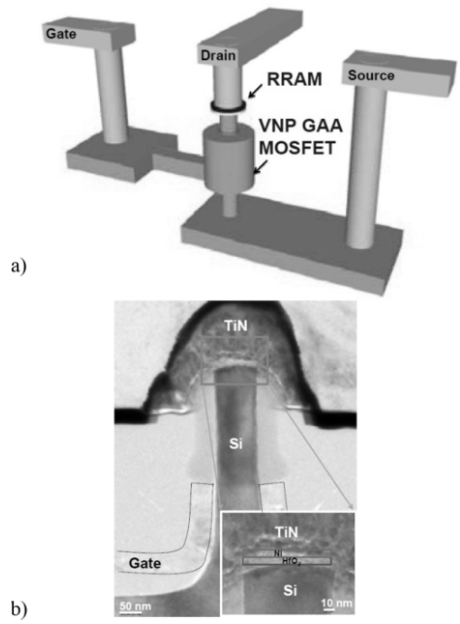


Figure 2.47. *a) Schematic illustration of GAA VNP integrated 1T1R architecture with RRAM stack build directly on top of Si NP. b) Cross-sectional TEM image of 1T1R memory cell with HfO_x based RRAM stack [WAN 12]*

The fabrication process flow of such integration before RRAM stacking is rather similar to that of the SiNW transistor or the SiNW SONOS NVM memory cell. It requires only one additional mask layer to add RRAM stack on top of the VNP transistor (shown in Figure 2.48**)**, where the bottom electrode can be self-aligned to the VNP transistor drain/source. Other than 1T1R single device, a small array of 4 × 4 size was also demonstrated. Scanning electron microscope (SEM) images of major steps during fabrication are shown in Figure 2.49 for both a single device and a 4 × 4 array.

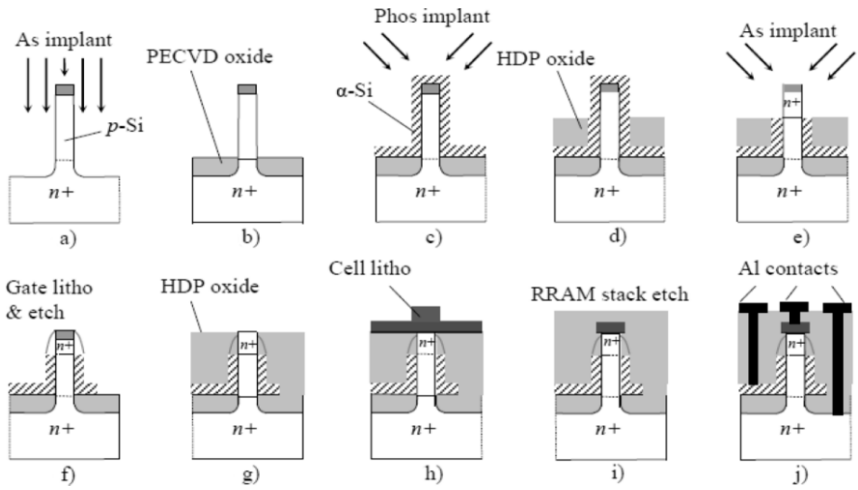


Figure 2.48. *Fabrication process flow of the vertical nanopillar 1T1R memory cell: a) Si nanopillar formation with nitride hard mask etching, trimming with oxidation for a smaller diameter and source implantation doping; b) plasma enhanced chemical vapor deposition (PECVD) isolation oxide; c) gate oxide growth and amorphous Si (α-Si) gate deposition and implantation; d) HDP isolation oxide deposition and etch back to expose Si nanopillar; e) excess gate α-Si removal and As drain implantation; f) spacer formation and oxide strip, followed by α-Si gate patterning; g) HDP oxide deposition and CMP to expose and remove hard mask; h) RRAM memory cell deposition and patterning after second nitride spacer formed on nanopillar tip sidewall; i) pre-metal dielectric (PMD) oxide deposition for passivation; j) metallization with Al metal pad [FAN 13]*

GAA VNP control transistor without RRAM integration shows good I_d–V_g characteristics with a threshold voltage of –0.57 V, DIBL ≈27 mV/V and a subthreshold swing of only 66 mV/decade at 300 K as shown in Figure 2.50(a). Saturation drive current scales with pillar diameter as shown in Figure 2.50(b).

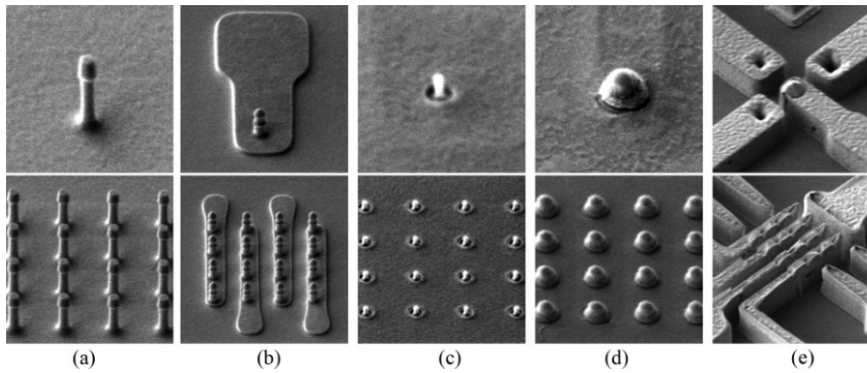


Figure 2.49. *SEM images of major steps of single device (upper part) and 4 × 4 array (lower part) during fabrication process: a) Si nanopillar formation with nitride hard mask on top; b) α-Si gate pad formed after thermally grown gate oxide; c) nanopillar transistor drain exposed for memory cell integration; d) oxide based RRAM cell deposited and patterned after isolation spacer formation: e) metallization and patterning [FAN 13]*

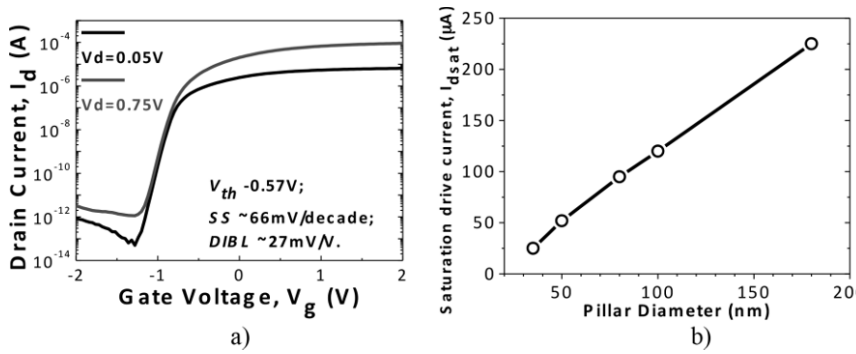


Figure 2.50. *a) Excellent I_d–V_g characteristics of the control transistor without RRAM integration, subthreshold swing of 66 mV/dec and DIBL of 27 mV/V have been extracted from measurement; b) saturation drive current (I_{dsat}) for vertical nanopillar control transistor with pillar diameter from 180 nm down to ~40 nm, which is the size of the bottom electrode for RRAM cell after integration. Drain current values are collected under same gate voltage of 1.5 V for all transistors [FAN 13]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

After adding an RRAM stack on top of the VNP transistor, the current output characteristics were not affected, as shown in Figure 2.51. It is observed that both *I–V* curves are similar, suggesting minimal impact of functionality of vertical transistor with subsequent RRAM cell integration.

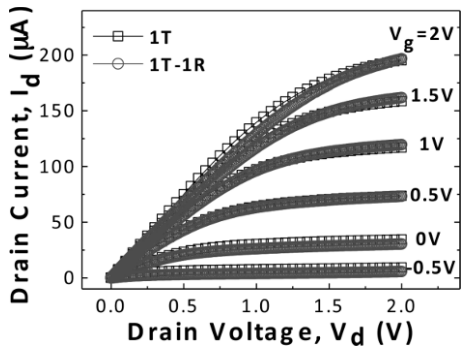


Figure 2.51. *Output (I_d–V_d) characteristics of control transistor and 1T1R with electrically broken RRAM cell. Similar curves suggest minimum impact on transistor's performance with the RRAM cell incorporation [FAN 13]*

The fabricated 1T1R memory cells exhibit three modes of resistive switching behaviors, namely ultra low current switching before forming, as well as unipolar and bipolar switching after forming. This electrical forming process refers to the very first electrical bias to initiate the resistive switching phenomenon as required in many RRAM cells [WAS 07]. Figure 2.52(a) shows the current–voltage characteristics of pre-forming ultralow current switching of 100 cycles and resistance distribution is plotted in Figure 2.52(b) with a memory window of >10 times. Stable room temperature retention is measured in Figure 2.52(c) and projected to 10 years without severe degradations.

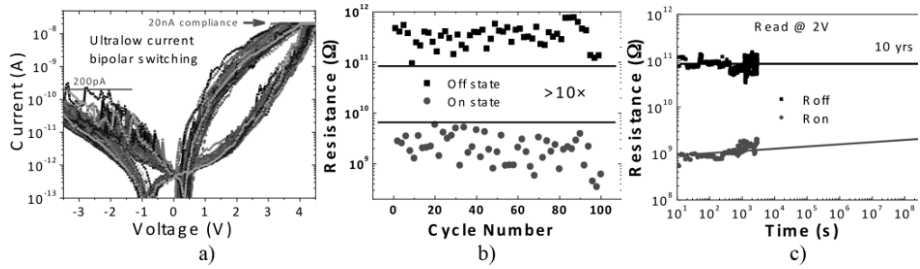


Figure 2.52. *a) I–V characteristics of ultralow current switching before forming. b) Resistance distribution of 100 consecutive DC cycles in pre-forming ultralow current resistive switching. c) Room temperature retention over a few thousands seconds without obvious degradation and projection to 10 years [FAN 13]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

Such low current bipolar switching is possibly due to oxygen ion movement in HfO_x layer, according to Fang *et al*. [FAN 13]. Prior to the high voltage forming process, a thin layer of SiO_2 exists between the nanopillar transistor tip and the HfO_x switching layer, which limits the current levels. When a positive voltage is applied to the transistor drain (Ni/TiN electrode), negatively-charged oxygen ions in HfO_x tend to be attracted toward the Ni layer, which results in a more oxygen deficient oxide and higher conductance of the stack. While for the reset process, the reverse movement of oxygen ions recovers the resistance of the memory cell.

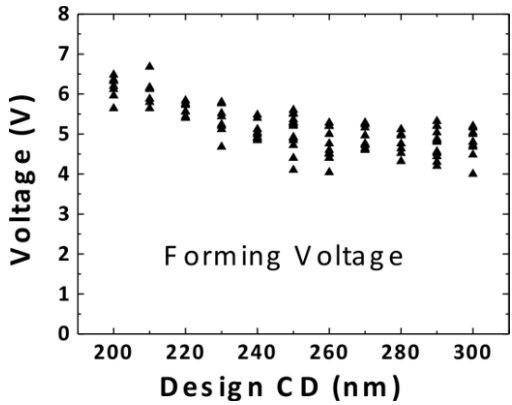


Figure 2.53. *Forming voltage versus nanopillar design CD plot. An increasing forming voltage with decreasing pillar design CD or equivalently device area can be seen [FAN 13]*

Other than pre-forming ultra low current switching, such integrated cells also show normal unipolar and bipolar switching behaviors after a proper forming process of around 5–6 V. Figure 2.53 summarizes the forming voltage distribution versus the transistor pillar diameter design CD. It is seen here that forming voltage decreases with enlarging CD, which is equivalent to the bottom electrode area of the RRAM device. Of note, the actual pillar diameter here is much smaller than its design CD as photoresist trimming and oxidation pillar trimming techniques are employed to reduce transistor channel diameters.

Figure 2.54 depicts the typical unipolar switching *I–V* characteristics and statistical distribution of operation voltages as well as on/off resistance. Compact distribution of V_{set} and V_{reset} is achieved with the average value of ~0.78 V/~2.38 V and standard deviation of ~0.30 V/~0.27 V, respectively. A

memory window of ~10^3 is maintained in all cycles measured without obvious degradations, especially for on resistance which is nearly a constant value.

Voltage polarity dependent bipolar resistive switching is also observed in VNP transistor integrated RRAM cells as shown in Figure 2.55(a). To get statistical resistive switching data, 100 DC cycles were measured and summarized from 10 devices and plotted in Figures 3.55(b) and (c). Similarly very tight distribution of on resistance was achieved and the memory windows of two orders were maintained for all devices, with an average set/reset voltages of ≈2.50 V/–1.08 V and a standard deviation of only ~0.37 V/0.32 V.

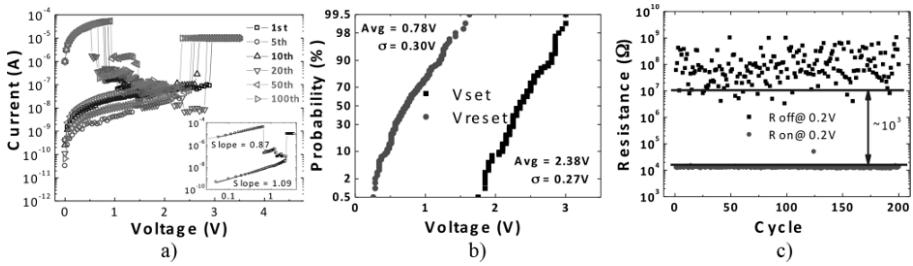


Figure 2.54. *a) Typical unipolar resistive switching I–V characteristics, inset shows the I–V fitting of on/off states in log–log scale. Statistical distribution of b) operation voltage and (c) on/off resistance from 200 DC cycles [FAN 13]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

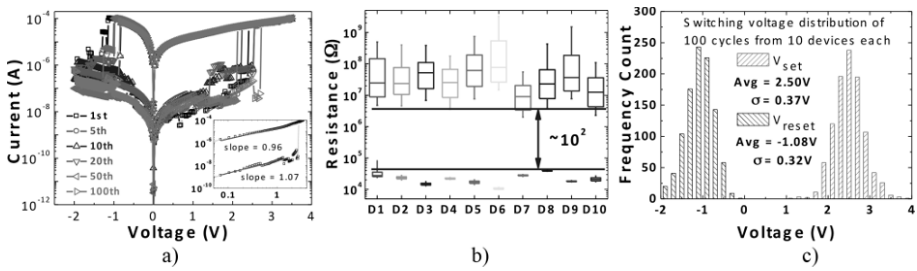


Figure 2.55. *a) Typical bipolar resistive switching I–V characteristics, and inset shows the I–V fitting of on/off states in log–log scale. Statistical distributions of b) on/off resistances and c) operation voltages of 100 DC cycles from 10 randomly selected devices each [FAN 13]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

It is observed in Figure 2.50(b) that nanopillar transistor saturation current increases with increasing pillar diameter, while a similar trend is also observed here in 1T1R integration. Figure 2.56 plots the RRAM reset current versus the nanopillar design CD in both unipolar and bipolar switching modes. It is seen that the reset current decreases as the nanopillar transistor design CD decreases. This suggests that the saturation drive current of the transistor also contributes in reducing the damage during a set process, since this saturation current is roughly the maximum current that can pass through the transistor and the RRAM cell.

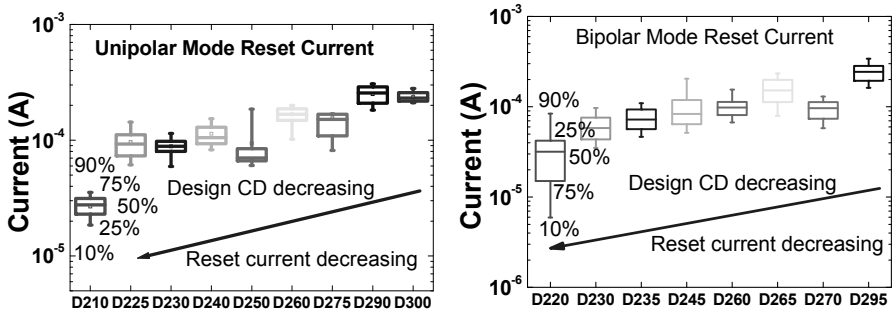


Figure 2.56. *Reset current in a) unipolar and b) bipolar switching plots versus nanopillar transistor diameter, showing a decreasing trend of current amplitude with decreasing design diameter. In this box chart plot, upper and lower whisker indicate 90% and 10%, upper and lower of rectangular box indicate 75% and 25% and the middle line indicate 50% percentage distribution respectively [FAN 13]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

Endurance and speed were also tested under AC conditions, in which a satisfactory endurance for a bipolar switching mode was obtained under voltage pulses for $>10^5$ without window degradations (shown in Figure 2.57). It was also demonstrated that the pulse width could be further shortened to 50 ns, a boundary condition for the setup available for that work.

Despite the SiNW-based transistor showing great potential to replace traditional planar structured memory cells, there are still tremendous challenges to overcome before the new concept is ready for mass production.

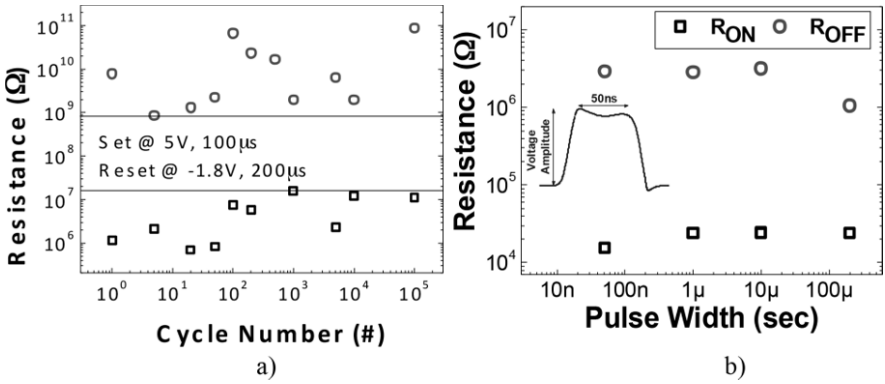


Figure 2.57. *a) Endurance properties of 1T1R cell in bipolar switching mode under voltage pulses, without window degradation after 10^5 cycles; b) Switching speed test down to 50 ns, a boundary condition for the setup (inset) [WAN 12]*

Firstly, the challenge of large device variations in threshold voltage and in on-current needs to be addressed [SIN 08]. This challenge is mainly attributed to the variety of NW shapes, sizes, diameters, roughness and variations in interface quality. Tight process control is needed to overcome this problem. Secondly, there is the challenge of tuning the threshold voltage. Due to the very limited volume of the channel body, doping of the channel for V_{th} adjustment is not feasible. Possible solutions rely only on the tuning of the gate electrode work function and the geometry of the NW. Lastly, a challenge uniquely inherent to vertical NW transistors, is the asymmetry between source and drain resistance, as well as in the channel diameter if the profile is not well controlled. Proper circuit design solutions may be sought to address the issues arising from these asymmetries.

2.4. Conclusions

This chapter has first summarized the major challenges encountered in the fabrication, electrical characterization and quantum transport simulation of SiNWs intended for end of the road map logic CMOS devices. In the second part, it has illustrated the new solutions offered by NW technologies for nonvolatile memory technologies both in terms of charge storage and resistive change types.

2.5. Acknowledgments

This work has been partially supported by several projects such as the FP7 NanoFunction Network of Excellence (no. 257573), the FP7 SQWIRE project (no. 257111), the A*STAR/Singapore TSRP "Future Data Center Technologies/NVM based on Integration of PCRAM and RRAM cells with ultra scaled vertical Si nanowire devices" (112-172-0016).

2.6. Bibliography

[ASA 97] ASAMITSU A., TOMIOKA Y., KUWAHARA H., *et al.*, "Current switching of resistive states in magnetoresistive manganites", *Nature*, vol. 388, pp. 50–52, 1997.

[BAH 90] BAHDER T.B., "Eight-band k · p model of strained zinc-blende crystals", *Phys. Rev. B*, vol. 41, pp. 11992–12 001, 1990.

[BAE 05] BAEK I.G., KIM D.C., LEE M.J., *et al.*, "Multi-layer cross-point binary oxide resistive memory (OxRRAM) for post-NAND storage application", *IEEE International Electron Device Meeting Technical Digest*, pp. 750–753, 2005.

[BAE 11] BAEK R.-H., BAEK C.-K., CHOI H.-S., *et al.*, "Characterization and modeling of 1/f noise in Si-nanowire FETs: effects of cylindrical geometry and different processing of oxides", *IEEE Trans. Nanotechnol.*, vol. 10, pp. 417–423, 2011.

[BAN 10] BANGSARUNTIP S., MAJUMDAR A., COHEN G.M., *et al.*, "Gate-all-around silicon nanowire 25-stage CMOS ring oscillators with diameter down to 3 nm", *Symp. on VLSI Technology*, pp. 21–22, 2010.

[BAR 12a] BARRAUD S., COQUAND R., CASSÉ M., *et al.*, "Performance of omega-shaped-gate silicon nanowire MOSFET with diameter down to 8nm", *IEEE Electron Dev. Lett.*, vol. 33, pp. 1526–1528, 2012.

[BAR 12b] BARNOLA S., PIMENTA-BARROS P., DESVOIVRES L., *et al.*, "Spacer patterning for Trigate SOI devices", *AVS 59th Annual International Symp. and Exhibition*, 2012.

[BAR 13] BARRAUD S., COQUAND R., MAFFINI-ALVARO V., *et al.*, "Scaling of omega-gate SOI nanowire N- and P-FET down to 10nm gate length: size- and orientation-dependent strain effects", *VLSI Tech. Dig.*, pp. 24–25, 2013.

[BEC 00] BECK A., BEDNORZ J.G., GERBER C., *et al.*, "Reproducible switching effect in thin oxide films for memory applications", *Applied Physics Letters*, vol. 77, pp. 139–141, 2000.

[BEN 09] BENNAMANE K., BOUTCHACHA T., GHIBAUDO G., *et al*., "DC and low frequency noise characterization of FinFET devices", *Solid-State Electron.*, vol. 53, pp. 1263–1267, October 2009.

[BOU 98] BOUTCHACHA T., GHIBAUDO G., "Low frequency noise characterization of 0.18 mu m Si CMOS transistors", *Physica Status Solidi-A.*, vol. 167, p. 261, 1998.

[BOR 04] BOREL S., ARVET C., BILDE J., *et al*., "Isotropic etching of SiGe alloys with high selectivity to similar materials", *Microelectronic. Eng.*, vol. 73, pp. 301–305, 2004.

[BUR 09] BURAN C., PALA M., BESCOND M., *et al*., "Three dimensional real-space simulation of surface roughness in silicon nanowire FETs", *IEEE Trans. Electron Devices*, vol. 56, pp. 2186–2192, October 2009.

[BUR 10] BURCHHART T., ZEINER C., HYUN Y.J., *et al*., "High performance Ω-gated Ge nanowire MOSFET with quasi-metallic source/drain contacts", *Nanotechnology*, vol. 21, pp. 435704–435708, 2010.

[BRU 69] BRUGLER J., JESPERS P., "Charge pumping in MOS devices", *IEEE Trans. Electron Devices*, vol. 16, p. 297, 1969.

[CAS 10] CASSÉ M., TACHI K., THIELE S., *et al*., "Spectroscopic charge pumping in Si nanowire transistors with a high-k/metal gate", *Appl. Phys. Lett.*, vol. 96, p. 123506, 2010.

[CAS 11] CASSÉ M., GARROS X., WEBER O., *et al*., "A study of N-induced traps due to a nitrided gate in high-k/metal gate nMOSFETs and their impact on electron mobility", *Solid-State Electronics*, vol. 65–66, pp. 139–145, 2011.

[CAS 12] CASSÉ M., BARRAUD S., LE ROYER C., *et al*., "Study of piezoresistive properties of advanced CMOS transistors: thin film SOI, SiGe/SOI, unstrained and strained Tri-Gate Nanowires", *IEDM Tech. Dig.*, p.637, 2012.

[CAS 13] CASSÉ M., BARRAUD S., COQUAND R., *et al*., "Strain enhanced performance of Si-Nanowire FETS", *ECS Transactions*, vol. 53, pp.125–136, 2013.

[CHE 08] CHEN J., SARAYA T., SHIMIZU K.K.M., *et al*., "Experimental study of mobility in [110]- and [100]-directed multiple silicon nanowire GAA MOSFETs on (100) SOI", *VLSI Symp. Tech. Dig.*, pp. 32–33, 2008.

[CHE 09a] CHENG K., KHAKIFIROOZ A., KULKARNI P., *et al*., "Extremely thin SOI (ETSOI) CMOS with record low variability for low power system-on-chip applications", *IEDM Tech. Dig.*, pp. 49–52, 2009.

[CHE 09b] CHEN M., YU H.Y., SINGH N., *et al*., "Vertical-Si-nanowire SONOS memory for ultrahigh-density application", *IEEE Electron Device Lett.*, vol. 30, pp. 879–881, 2009.

[CHE 10] CHEN J., SARAYA T., HIRAMOTO T., "Mobility enhancement over universal mobility in (100) silicon nanowire gate-all-around MOSFETs with width and height of less than 10 range", *VLSI Tech. Dig.*, pp. 175–176, 2010.

[CHI 10] CHING-HUA W., YI-HUNG T., KAI-CHUN L., *et al*., "Three-dimensional $4F^2$ ReRAM cell with CMOS logic compatible process", *IEEE International Electron Device Meeting Technical Digest*, pp. 29.6.1–29.6.4, 2010.

[CHO 02] CHOI Y.-K., KING T.-J, HU C., "A spacer patterning technology for nanoscale CMOS", *IEEE Trans. Electron Dev.*, vol. 49, pp. 436–441, 2002.

[CHR 68] CHRISTENSSON S., LUNDSTROM I., SVENSSON C., "Low frequency noise in MOS transistors–I Theory", *Sol State Electron*, vol. 11, p. 797, 1968.

[CHU 10] CHUNG S., RHO K.-M., KIM S.-D., *et al*., "Fully integrated 54nm STT-RAM with the smallest bit cell dimension for high density memory application", *IEEE International Electron Device Meeting Technical Digest*, pp. 304–307, 2010.

[COL 90] COLINGE J.P., GAO M.H., ROMANO-RODRIGUEZ A, *et al*., "Silicon-on-insulator gate-all-around device", *IEEE International Electron Device Meeting Technical Digest*, pp. 595–598, 1990.

[CON 11] CONZATTI F., PALA M., ESSENI D., *et al*., "A simulation study of strain induced performance enhancements in InAs nanowire tunnel-FETs", *IEEE IEDM Tech. Dig.*, pp. 5.2.1–5.2.4, December 2011.

[CON 12a] CONZATTI F., PALA M., ESSENI D., *et al*., "Strain-induced performance improvements in InAs nanowire tunnel FETs", *Electron Devices, IEEE Transactions on Electron Devices*, vol. 59, pp. 2085–2092, 2012.

[CON 12b] CONZATTI F., PALA M., ESSENI D., "Surface-roughness-induced variability in nanowire InAs tunnel FETs", *IEEE Electron Device Letters*, vol. 33, pp. 806–808, 2012.

[COQ 12a] COQUAND R., CASSÉ M., BARRAUD S., *et al*., "Strain-induced performance enhancement of tri-gate and omega-gate nanowire FETs scaled down to 10nm Width", *Symp. VLSI Technology*, p. 13, 2012.

[COQ 12b] COQUAND R., BARRAUD S., CASSÉ M., *et al*., "Scaling of high-k/metal-gate Trigate SOI nanowire transistors down to 10nm width", *Proc. Int. Conf. on Ultimate Integration on Silicon ULIS*, p. 37, 2012.

[COQ 13a] COQUAND R., CASSÉ M., BARRAUD S., *et al*., "Strain-induced performance enhancement of trigate and omega-gate nanowire FETs scaled down to 10-nm width", *IEEE Trans. Electron Dev.*, vol. 60, pp. 727–732, 2013.

[COQ 13b] COQUAND R., MONFRAY S., PRADELLES J., *et al*., "On the optimization of e-beam lithography using hydrogen silsesquioxane (HSQ) for innovative self-aligned CMOS process", *ECS Trans.*, vol. 53, pp. 177–184, 2013.

[CRE 11] CRESTI A., PALA M., POLI S., *et al*., "A comparative study of surface-roughness-induced variability in silicon nanowire and double-gate FETs", *IEEE Trans. Electron Devices*, vol. 58, pp. 2274–2281, 2011.

[DOR 07] DORNEL E., ERNST T., BARBÉ J.C., *et al*., "Hydrogen annealing of arrays of planar and vertically stacked Si nanowires", *Appl. Phys. Letters*, vol. 91, pp. 233502–233504, 2007.

[DOY 03] DOYLE B.S., DATTA S., DOCZY M., *et al*., "High performance fully-depleted tri-gate CMOS transistors", *IEEE Electron Device Lett.*, vol. 24, pp. 263–265, 2003.

[DUT 81] DUTTA P., HORN P., "Low-frequency fluctuations in solids: 1/f noise", *Rev. Mod. Phys.*, vol. 53, pp. 497–516, 1981.

[ELE 88] ELEWA T., HADDARA H., CRISTOLOVEANU S., *et al*., "Charge pumping in silicon on insulator structures using gated P-I-N diodes", *J. Phys. Colloq*., vol. 49 (C4), p. 137, 1988.

[END 03] ENDOH T., KINOSHITA K., TANIGAMI T., *et al*., "Novel ultrahigh-density flash memory with a stacked-surrounding gate transistor (S-SGT) structured cell", *IEEE Trans. on Electron Device*, vol. 50, pp. 945–951, 2003.

[ERN 06] ERNST T., DUPRÉ C., ISHEDEN C., *et al*., "Novel 3D integration process for highly scalable nano-beam stacked-channels GAA (NBG) FinFETs with HfO_2/TiN gate stack", *Electron Devices Meeting (IEDM)*, pp.997–1000, 2006.

[ESS 03] ESSENI D., ABRAMO A., "Modeling of electron mobility degradation by remote coulomb scattering in ultrathin oxide MOSFETs", *IEEE Transactions on Electron Devices*, vol. 50, pp. 1665–1674, 2003.

[ESS 13] ESSENI D., PALA M., "Interface traps in InAs nanowire tunnel-FETs and MOSFETs - Part II: comparative analysis and traps induced variability", *IEEE Transactions on Electron Devices*, vol. 60, pp. 2802–2807, 2013.

[FAN 86] FANG Z., CRISTOLOVEANU S., CHOVET A., "Analysis of hot-carrier-induced aging from 1/f noise in short-channel MOSFET's", *IEEE Electron Device Letters*, vol. 7, pp. 371–373, 1986.

[FAN 07] FANG W.W., SINGH N., BERA L.K., *et al.*, "Vertically stacked SiGe nanowire array channel CMOS transistors", *IEEE Elec. Dev. Lett.*, vol. 28, p. 211, 2007.

[FAN 13] FANG Z., WANG X.P., LI X., *et al.*, "Fully CMOS-Compatible 1T1R integration of vertical nanopillar GAA transistor and oxide-based RRAM cell for high-density nonvolatile memory application", *IEEE Trans. on Electron Device*, vol. 60, pp. 1108–1113, 2013.

[FEN 11] FENG W., HETTIARACHCHI R., LEE Y., *et al.*, "Fundamental origin of excellent low-noise property in 3D Si-MOSFETs - Impact of charge-centroid in the channel due to quantum effect on 1/f noise", *IEDM Tech. Dig.*, pp. 630–633, 2011.

[FER 11] FERAIN I., COLINGE C.A., COLINGE J.-P., "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors", *Nature*, vol. 479, pp. 310–316, 2011.

[FER 97] FERRY D.K., GOODNICK S.M., *Transport in Nanostructures*, Cambridge University Press, Cambridge, UK, 1997.

[FIS 91] FISCHETTI M.V., "Monte Carlo simulation of transport in technologically significant semiconductors of the diamond and zinc-blende structures–Part I: Homogeneous transport", *IEEE Trans. Electron Devices*, vol. 38, pp. 634–649, 1991.

[GAR 08] GARROS X., CASSÉ M., REIMBOLD G., *et al.*, "Guidelines to improve mobility performances and BTI reliability of advanced high-k/metal gate stacks", *Symp. VLSI Technology*, 2008.

[GHI 91] GHIBAUDO G., ROUX O., NGUYEN-DUC C., *et al.*, "Improved analysis of low frequency noise in field-effect MOS transistors", *Phys. Stat. Sol. (a)*, vol. 124, p. 571, 1991.

[GHI 94] GHIBAUDO G., ROUX DIT BUISSON O., "Low frequency fluctuations in scaled down Silicon CMOS devices. Status and trends", *Proc. ESSDERC*, vol. 94, p. 693, 1994.

[GHI 02] GHIBAUDO G., CHROBOCZEK J., "On the Origin of LF Noise in Si/Ge Channel MOSFET's", *Sol. State Electron.*, vol. 46, p. 393, 2002.

[GNA 06] GNANI E., REGGIANI S., RUDAN M., *et al.*, "Design considerations and comparative investigation of ultra-thin SOI, double-gate and cylindrical nanowire FETs", *European Solid-State Device Research Conference*, pp. 371–374, 2006.

[GNA 10] GNANI E., GNUDI A., REGGIANI S., *et al.*, "Effective mobility in nanowire FETs under quasi-ballistic conditions", *IEEE Trans. Electron Devices*, vol. 57, pp. 336–344, 2010.

[GOO 85] GOODNICK S.M., FERRY D.K., WILMSEN C.W., *et al*., "Surface roughness at the Si(100)-SiO2 interface", *Physical Review B*, vol. 32, no. 8171, 1985.

[GRO 84] GROESENEKEN G., MAES H., BELTRAN N., *et al.*, "A reliable approach to charge-pumping measurements in MOS transistors", *IEEE Trans. Electron Devices*, vol. 31, p. 42, 1984.

[GRA 66] GRAY P.V., BROWN D.M., "Density of SiO_2-Si interface states", *Appl. Phys. Lett.*, vol.8, p. 31, 1966.

[HAR 09] HARTMANN J.M., PAPON A.M., BARNES J.P., *et al.*, "Growth kinetics of SiGe/Si superlattices on bulk and silicon-on-insulator substrates for multi-channel devices", *J. Cryst. Growth*, vol. 311, pp. 3152–3157, 2009.

[HAS 08] HASHEMI P., GOMEZ1 L., CANONICO M., *et al.*, "Electron transport in gate-all-around uniaxial tensile Strained-Si Nanowire n-MOSFETs", *IEDM Tech. Dig.*, p. 865, 2008.

[HIC 62] HICKMOTT T.W., "Low-frequency negative resistance in thin anodic oxide films", *Journal of Applied Physics*, vol. 33, pp. 2669–2682, 1962.

[HIS 98] HISAMOTO D., LEE W.-C., KEDZIERSKI J., *et al.*, "A folded-channel MOSFET for deep-sub-tenth micron era", *IEEE International Electron Device Meeting Technical Digest*, pp. 1032–1034, 1998.

[HOB 12] HOBBS R.G., PETKOV N., HOLMES J.D., "Semiconductor nanowire fabrication by bottom-up and top-down paradigms", *Chem. Mater.*, vol. 24, pp. 1975–1991, 2012.

[HUE 07] HUET K., SAINT-MARTIN J., BOURNEL A., *et al.*, "Monte Carlo study of apparent mobility reduction in nano-MOSFETs", *Proc. ESSDERC Conf.*, pp. 382–385, 2007.

[IMS 10] Innovative Mass Storage Technologies (IMST) white book, October 2010.

[ION 12] IOANNIDIS E.G., DIMITRIADIS C.A., HAENDLER S., *et al.*, "Improved analysis and modeling of low-frequency noise in nanoscale MOSFETs", *Solid-State Electron.*, vol. 76, pp. 54–59, 2012.

[ITR 06] "ITRS 2006 Update", International Technology Roadmap for Semiconductors, 2006.

[ITR 12] International Technology Roadmap for Semiconductors (2012), 2012, available at http://www.itrs.net/.

[JAH 05] JAHAN C., FAYNOT O., CASSÉ M., *et al.*, "ΩFETs transistors with TiN metal gate and HfO_2 down to 10nm", *VLSI Tech. Dig.*, pp. 112–113, 2005.

[JAN 10] JANG D., LEE J.W., TACHI K., *et al.*, "Low-frequency noise in strained SiGe core-shell nanowire p-channel field effect transistors", *Applied Physics Letters*, vol. 97, p. 073505, 2010.

[JAN 11] JANG D., LEE J.W., LEE C.-W., *et al.*, "Low-frequency noise in junctionless multi-gate transistors", *Applied Physics Letters*, vol. 98, p. 133502, 2011.

[JAY 89] JAYARAMAN R., SODINI C., "A 1/f noise technique to extract the oxide trap density near the conduction band edge of silicon", *IEEE Trans. Electron Devices*, vol. 36, p. 1773, 1989.

[JIA 08] JIANG Y., LIOW T.Y., SINGH N., *et al.*, "Performance breakthrough in 8 nm gate length Gate-All-Around nanowire transistors using metallic nanowire contacts", *Symp. on VLSI Tech.*, pp. 34–35, 2008.

[JIA 09] JIANG Y., SINGH N., LOW T.Y., *et al.*, "Omega-Gate p-MOSFET with nanowirelike SiGe/Si Core/Shell channel", *IEEE Electron Device Lett.*, vol. 30, pp. 392–394, 2009.

[JUR 00] JURCZAK M., SKOTNICKI T., PAOLI M., *et al.*, "Silicon-on-nothing (SON) – an innovative process for advanced CMOS", *IEEE Trans. Electron Dev.*, vol. 47, pp. 2179–2187, 2000.

[KIM 08] KIM D.-W., LI M., YEO K.-H., *et al.*, "Twin Silicon nanowire FET (TSNWFET) on SOI With 8nm Silicon Nanowires and 25nm Surrounding TiN Gate", *IEEE International SOI Conference*, pp. 117–118, 2008.

[KOY 13a] KOYAMA M., CASSÉ M., COQUAND R., *et al.*, "Study of carrier transport in strained and unstrained SOI tri-gate and omega-gate silicon nanowire MOSFETs", *Solid-State Electron.*, vol. 84, pp. 46–52, 2013.

[KOY 13b] KOYAMA M., CASSÉ M., COQUAND R., *et al.*, "Study of low-frequency noise in SOI Tri-gate Silicon Nanowire MOSFETs", *Proc. Int. Conf. on Noie and Fluctuations, ICNF'13*, Montpellier, France, June 2013.

[KOZ 99] KOZICKI M.N., YUN M., HILT L., *et al.*, "Applications of programmable resistance changes in metal-doped chalcogenides", *Pennington NJ USA: Electrochem. Soc*, vol. 99–13, pp. 298-309, 1999.

[KNO 10] KNOCH J., APPENZELLER J., "Modeling of high-performance p-type IIIV heterojunction tunnel FETs", *IEEE Electron Device Letters*, vol. 31, pp. 305–307, 2010.

[KWO 12] KWONG D.-L., LI X., SUN Y., *et al.*, "Vertical silicon nanowire platform for low power electronics and clean energy applications", *Journal of Nanotechnology*, vol. 2012, p. 21, 2012.

[LEE 02] LEE J.D., HUR S.H., CHOI J.D., "Effects of floating-gate interference on NAND flash memory cell operation", *IEEE Electron Device Lett.*, vol. 23, pp. 264–266, 2002.

[LEE 08] LEE H.Y., CHEN P.S., WU T.Y., *et al.*, "Low power and high speed bipolar switching with a thin reactive ti buffer layer in robust HfO_2 based RRAM", *IEEE International Electron Device Meeting Technical Digest*, pp. 297–300, 2008.

[LEE 12] LEE S.-H., BAEK C.-K., PARK S., *et al.*, "Characterization of channel-diameter-dependent low-frequency noise in silicon nanowire field-effect transistors", *IEEE Electron Device Lett.*, vol. 33, pp. 1348–1350, 2012.

[LEE 13] LEE J.W., CHO M.J., SIMOEN E., *et al.*, "1/f noise analysis of replacement metal gate bulk p-type fin field effect transistor", *Appl. Phys. Lett.*, vol. 102, p. 073503, February 2013.

[LEN 08] LENZI M., PALESTRI P., GNANI E., *et al.*, "Investigation of the transport properties of silicon nanowires using deterministic and Monte Carlo approaches to the solution of the Boltzmann transport equation", *IEEE Trans. Electron Devices*, vol. 55, pp. 2086–2096, 2008.

[LI 06] LI M., SUK S.D., YEO K.H., *et al.*, "Investigation of Nanowire Orientation and embedded Si1-xGex source/drain influence on twin silicon nano-wire field effect transistor (TSNWFET)", *8th International Conference on Solid-State and Integrated Circuit Technology*, pp. 78–80, 2006.

[LI 07] LI M., HWAN K., YEOH Y.Y., *et al.*, "Experimental Investigation on Superior PMOS performance of uniaxial strained <110> silicon nanowire channel by embedded sige source/drain", *IEDM Tech. Dig.*, pp. 899–902, 2007.

[LI 09] LI M., YEO K.H., SUK S.D., *et al.*, "Sub-10nm gate-all-around CMOS nanowire transistors on bulk si substrate", *VLSI Tech. Dig.*, pp. 94–96, 2009.

[LIN 11] LIN L., ROBERTSON J., "Defect states at III-V semiconductor oxide interfaces", *Applied Physics Letters*, vol. 98, p. 082903, 2011.

[LIO 08] LIOW T.-Y., TAN K.-M., LEE R.T.P., *et al.*, "Germanium source and drain stressors for ultra-thin-body and nanowire field-effect transistors", *IEEE Electron Device Lett.*, vol. 29, pp. 808–810, 2008.

[LU 13] LU C.Y., HSIEH K.Y., LIU R., "Future challenges of flash memory technologies", *Microelectronic Engineering,* vol. 86, pp. 283–286, 2009.

[LUI 09] LUISIER M., KLIMECK G., "Atomistic full-band simulations of silicon nanowire transistors: effects of electron–phonon scattering", *Phys. Rev. B*, vol. 80, pp. 155 430-1–155 430-11, 2009.

[LUS 05] LUSAKOWSKI J., KNAP W., MEZIANI Y., *et al.*, "Ballistic and pocket limitations of mobility in nanometer Si metal–oxide semiconductor field-effect transistors", *Appl. Phys. Lett.*, vol. 87, pp. 053507–1, 2005.

[MAE 85] MAES H., USMANI S., GROESENEKEN G., "Correlation between 1/f noise and interface state density at the Fermi level in field-effect transistors", *J. Appl. Phys.*, vol. 57, p. 4811, 1985.

[MAE 04] MAEDA S., CHOI J.-A., YANG J.-H., *et al.*, "Negative bias temperature instability in triple gate transistors", *International Reliability Physics Symposium Proceedings*, pp. 8–12, 2004.

[MCW 57] MCWHORTER A., "1/f noise and germanium surface properties" *In Semiconductor Surf. Phys*., Univ. of Pennsylvania Press, Philadelphia, p. 207, 1957.

[MEI 90] MEISENHEIMER T.M., FLEETWOOD D.M., "Effect of radiation-induced charge on 1/f noise in MOS devices", *IEEE TNS*, vol. 37, p. 1696, 1990.

[MIC 13] MICHELONI R., MARELLI A., ESHGHI K., *Inside solid state drives (SSDs)*, Springer, 2013.

[MIT 10] MITARD J., WITTERS L., ENEMAN G., *et al.*, "85nm-Wide 1.5mA/µm-I_{ON} IFQW SiGe-pFET: raised vs embedded $Si_{0.75}Ge_{0.25}$ S/D benchmarking and in-depth hole transport study", *VLSI Tech. Dig.*, pp. 163–164, 2010.

[MOR 96] MORFOULI P., GHIBAUDO G., OUISSE T., *et al.*, "Low frequency noise characterization of N and P MOSFET's with ultrathin oxynitride gate films", *IEEE Electron Device letters*, vol. 17, p. 395, 1996.

[MUK 08] MUKAI H., SHIOBARA E., TAKAHASHI S., *et al.*, "A study of CD budget in spacer patterning technology", *Proc. SPIE, Optical Microlithography*, vol. 6924, p. 692406, 2008.

[NAI 13] NAINANI A., GUPTA S., MOROZ V., *et al.*, "Is strain engineering scalable in FinFET era?: teaching the old dog some new tricks", *IEDM Tech. Dig.*, p. 427, 2013.

[NEO 10] NEOPHYTOU N., KOSINA H., "Large enhancement in hole velocity and mobility in p-Type [100] and [111] silicon nanowires by cross section scaling: an atomistic analysis", *Nano Lett.*, vol. 10, pp. 4913–4919, 2010.

[NIQ 12] NIQUET Y.-M., DELERUE C., KRZEMINSKI C., "Effects of strain on the carrier mobility in silicon nanowires", *Nano Lett.*, vol. 12, pp. 3545–3550, 2012.

[ORI 11] ORIA L., RUIZ DE LUZURIAGA A., CHEVALIER X., *et al.*, "Guided self-assembly of block-copolymer for CMOS technology: a comparative study between grapho-epitaxy and surface chemical modification", *Proc. SPIE, Alternative Lithographic Technologies III*, 79700P, 2011.

[OVS 68] OVSHINSKY S.R., "Reversible electrical switching phenomena in disordered structures", *Physical Review Letters*, vol. 21, pp. 1450–1453, 1968.

[PAC 09] PACKAN P., AKBAR S., ARMSTRONG M., *et al.*, "High performance 32nm logic technology featuring 2nd generation high-k+metal gate transistors", *IEDM Tech. Dig.*, 2009.

[PAL 12] PALA M., ESSENI D., CONZATTI F., "Impact of interface traps on the IV curves of InAs Tunnel-FETs and MOSFETs: a full quantum study", *IEEE IEDM Technical Digest*, pp. 6.6.1–6.6.4, 2012.

[PAL 13] PALA M., ESSENI D., "Interface traps in InAs nanowire Tunnel-FETs and MOSFETs - Part I: Model description and single trap analysis in Tunnel-FETs", *IEEE Transactions on Electron Devices*, vol. 60, pp. 2795–2801, 2013.

[PAR 01] PARK J.-T., COLINGE J.-P., DIAZ C.H., "Pi-gate SOI MOSFET", *IEEE Electron Device Lett.*, vol. 22, pp. 405–405, 2001.

[PAS 10] PASSLACK M., DROOPAD R., BRAMMERTZ G., "Suitability study of oxide/gallium arsenide interfaces for MOSFET applications," *Electron Devices, IEEE Transactions on*, vol. 57, pp. 2944–2956, 2010.

[POL 08] POLI S., PALA M., POIROUX T., *et al.*, "Size dependence of surface-roughness-limited mobility in silicon-nanowire FETs", *IEEE Trans. Electron Devices*, vol. 55, pp. 2968–2976, 2008.

[POL 09a] POLI S., PALA M., "Channel-length dependence of low-field mobility in silicon-nanowire FETs", *IEEE Electron Device Lett.*, vol. 30, pp. 1212–1214, 2009.

[POL 09b] POLI S., PALA M.G., POIROUX T., "Full quantum treatment of remote Coulomb scattering in silicon nanowire FETs", *IEEE Trans. Electron Devices*, vol. 56, pp. 1191–1198, 2009.

[REE 88] REED M.L., PLUMMER J.D., "Chemistry of Si-SiO_2 interface trap annealing", *J. Appl. Phys.*, vol. 63, p. 5776, 1988.

[ROC 09] ROCHETTE F., CASSÉ M., MOUIS M., *et al.*, "Piezoresistance effect of strained and unstrained fully-depleted silicon-on-insulator MOSFETs integrating a HfO2/TiN gate stack", *Solid-State Electron.*, vol. 53, pp. 392–396, 2009.

[ROG 09] ROGDAKIS K., POLI S., BANO E., *et al.*, "Phonon-and surface-roughness-limited mobility of gate-all-around 3C-SiC and Si nanowire FETs", *Nanotechnology*, vol. 20, p. 295202, 2009.

[ROY 11] LE ROYER C., VILLALON A., CASSE M., *et al.*, "First demonstration of ultrathin body c-SiGe channel FDSOI pMOSFETs combined with SiGe(:B) RSD: drastic improvement of electrostatics (Vth, p tuning, DIBL) and transport (μ0, Isat) properties down to 23nm gate length", *IEDM Tech. Dig.*, pp. 16.5.1–16.5.4, 2011.

[SAI 10] SAITOH M., NAKABAYASHI Y., ITOKAWA H., *et al.*, "Short-channel performance and mobility analysis of <110>- and <100>-oriented tri-gate nanowire MOSFETs with raised source/drain extensions", *VLSI Symp. Tech. Dig.*, pp. 169–170, 2010.

[SAI 12] SAITOH M., NAKABAYASHI Y., OTA K., *et al.*, "Performance improvement by stress memorization technique in trigate silicon nanowire MOSFETs", *IEEE Electron Dev. Lett.*, vol. 33, pp. 8–10, 2012.

[SAN 84] SANCHO M.P.L., SANCHO J.M.L., RUBIO J., "Quick iterative scheme for the calculation of transfer matrices: Application toMo (100)", *J. Phys. F, Met. Phys.*, vol. 14, pp. 1205–1215, 1984.

[SCH 07] SCHRODER D.K., "Negative bias temperature instability: what do we understand?", *Microelectron. Reliab.*, vol. 47, p. 841, 2007.

[SHI 06] SHIN K., XIONG W., CHO C.-Y., *et al.*, "Study of bending-induced strain effects on MuGFET performance", *IEEE Electron Dev. Lett.*, vol. 27, p. 671, 2006.

[SHI 09] SHIN M., "Full-quantum simulation of hole transport and band-to-band tunneling in nanowires using the k · p method", *J. Appl. Phys.*, vol. 106, pp. 054505–1, 2009.

[SHU 02] SHUR M.S., "Low ballistic mobility in submicron HEMTs", *IEEE Electron Device Lett.*, vol. 23, pp. 511–513, 2002.

[SIM 93] SIMOEN E., DIERICKX B., CLAEYS C., "Hot-Carrier degradation of the Random Telegraph Signal amplitude in submicrometer Si MOSTs", *Appl. Phys.*, vol. A57, p. 283, 1993.

[SIN 08] SINGH N., BUDDHARAJU K.D., MANHAS S.K., *et al.*, "Si, SiGe nanowire devices by top-down technology and their applications", *IEEE Trans. on Electron Device*, vol. 55, pp. 3107–3118, 2008.

[SUG 12] SUGI R., SHIMIZU M., KIMURA T., "Development of EUV Resist for 16nm Half Pitch", *J. of Photopolymer Science and Technology*, vol. 25, pp. 603–607, 2012.

[SUN 07] SUN G., THOMPSON S.E., NISHIDA T., "Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors", *J. Appl. Phys.*, vol. 101, p. 104503, 2007.

[SUN 10] SUN Y., YU H.Y., SINGH N., *et al.*, "Multibit programmable flash memory realized on vertical si nanowire channel", *IEEE Electron Device Lett.*, vol. 31, pp. 390–392, 2010.

[SUN 11] SUN Y., YU H.Y., SINGH N., *et al.*, "Demonstration of memory string with stacked junction-less SONOS realized on vertical silicon nanowire", *IEEE International Electron Device Meeting Technical Digest*, pp. 223–226, 2011.

[SUN 13] SUN M.-C., KIM G., LEE J.H., *et al.*, "Patterning of Si nanowire array with electron beam lithography for sub-22nm Si nanoelectronics technology", *Microelectronic Enginnering*, 2013.

[SUR 88] SURYA C., HSIANG T., "A thermal activation model for hbox1f#x03B3 noise in Si-MOSFETs", *Sol. State Electron*, vol. 31, p. 959, 1988.

[TAC 09] TACHI K., CASSE M., JANG D., *et al.*, "Relationship between mobility and high-k interface properties in advanced Si and SiGe nanowires", *IEDM Tech. Dig.*, p. 313, 2009.

[TAC 10] TACHI K., CASSÉ M., BARRAUD S., *et al.*, "Experimental study on carrier transport limiting phenomena in 10nm width nanowire CMOS transistors," *IEDM Tech. Dig.*, pp. 94–95, 2010.

[TEZ 07] TEZUKA T., TOYODA E., NAKAHARAI S., *et al.*," Observation of mobility enhancement in strained Si and SiGe tri-gate MOSFETs with multi-nanowire channels trimmed by hydrogen thermal etching", *IEDM Tech Dig.*, p .887, 2007.

[THE 12] THEODOROU C.G., FASARAKIS N., HOFFMAN T., *et al.*, "Flicker noise in n-channel nanoscale tri-gate fin-shaped field-effect transistors", *Appl. Phys. Lett.*, vol. 101, p. 243512, 2012.

[UEN 05] UENO T., RHEE H.S., LEE S.H., *et al.*, "Dramatically enhanced performance of recessed SiGe source-drain PMOS by in-situ etch and regrowth technique (InSERT)", *VLSI Tech. Dig.*, pp. 24–25, 2005.

[UCH 06] UCHIDA K., KINOSHITA A., SAITOH M., "Carrier transport in (110) nMOSFETs: subband structures, non-parabolicity, mobility characteristics, and uniaxial stress engineering", *IEDM Tech. Dig.*, 2006.

[UNG 07] UNGERSBOECK E., DHAR S., KARLOWATZ G., *et al.*, "The effect of general strain on the band structure and electron mobility of silicon", *IEEE Trans. Electron Devices*, vol. 54, pp. 2183–2190, 2007.

[VAN 79] VAN DER ZIEL A., "Flicker noise in electronic devices", *Advances in Electronics and Electron Physics*, vol. 49, p. 225, 1979.

[VAN 91] VAN DEN BOSCH G., GROESENEKEN G, HEREMANS P., *et al.*, "Spectroscopic charge pumping: a new procedure for measuring interface trap distributions on MOS transistors", *IEEE Trans. Electron Devices*, vol. 38, p. 1820, 1991.

[VUR 01] VURGAFTMAN I., MEYER J.R., RAM-MOHAN L.R., "Band parameters for III–V compound semiconductors and their alloys", *J. Appl. Phys.*, vol. 89, pp. 5815–5875, 2001.

[WAN 05] WANG J., POLIZZI E., GOSH A., *et al.*, "Theoretical investigation of surface roughness scattering in silicon nanowire transistors", *Appl. Phys. Lett.*, vol. 87, pp. 043101-1–043101-3, 2005.

[WAN 10] WANG L., YU E., TAUR Y., *et al.*, "Design of tunneling field effect transistors based on staggered heterojunctions for ultralow-power applications", *Electron Device Letters, IEEE*, vol. 31, pp. 431–433, 2010.

[WAN 12] WANG X.P., FANG Z., LI X., *et al.*, "Highly compact 1T-1R architecture ($4F^2$ footprint) involving fully CMOS compatible vertical GAA nano-pillar transistors and oxide-based RRAM cells exhibiting excellent NVM properties and ultra-low power operation", *IEEE International Electron Device Meeting Technical Digest*, pp. 493–496, 2012.

[WAS 07] WASER R., AONO M., "Nanoionics-based resistive switching memories", *Nature Materials*, vol. 6, pp. 833–840, 2007.

[WEI 09] WEI C., XIONG Y.-Z., ZHOU X., *et al.*, "Investigation of low-frequency noise in silicon nanowire MOSFETs in the subthreshold region", *IEEE Electron Device Lett.*, vol. 30, pp. 668–671, 2009.

[WHI 00] WHITE M.H., ADAMS D.A., BU J., "On the go with SONOS", *IEEE Circuits and Devices*, vol. 16, pp. 22–31, 2000.

[XIO 06] XIONG W., RINN CLEAVELIN C., KOHLI P., *et al.*, "Impact of strained-silicon-on-insulator (sSOI) substrate on FinFET mobility", *IEEE Electron Device Lett.*, vol.27, p. 612, 2006.

[YAM 11] YAMASHITA T., BARKER V.S., STANDAERT T., *et al.*, "Sub-25nm FinFET with advanced fin formation and short channel effect engineering", *Symp. on VLSI Technology*, pp. 14–15, 2011.

[YAN 02] YANG F.L., CHEN H.-Y., CHEN F.-C., *et al.*, "25nm CMOS Omega FETs", *IEDM Tech. Dig.*, pp. 255–258, 2002.

[YAN 04] YANG F.-L., LEE S.-H., CHEN H.-Y., *et al.*, "5nm-gate nanowire Finfet", *VLSI Tech. Dig.*, pp. 196–197, 2004.

[YUA 09] YUAN HENG T., CHIA-EN H., KUO C.H., *et al.*, "High density and ultra small cell size of Contact ReRAM (CR-RAM) in 90nm CMOS logic technology and circuits", *IEEE International Electron Device Meeting Technical Digest*, pp. 5.6.1–5.6.4, 2009.

[ZHA 06] ZHANG D., WHITE T., NGUYEN B.-Y., "Embedded Source/Drain SiGe Stressor Devices on SOI: Integrations, Performance, and Analyses", *IEEE Trans. Electron Devices*, vol. 53, pp. 3020–3024, 2006.

[ZHU 09] ZHUGE J., WANG R., HUANG R., *et al.*, "Investigation of low-frequency noise in silicon nanowire MOSFETs", *IEEE Electron Device Lett.*, vol. 30, pp. 57–60, 2009.

3

Graphene and 2D Layer Devices for More Moore and More-than-Moore Applications

This chapter reviews the current status of graphene transistors as a potential supplement to silicon complementary metal-oxide-semiconductor (CMOS) technology for More Moore and More-than-Moore applications. A short overview of graphene manufacturing and metrology methods is followed by an introduction of macroscopic graphene field effect transistors (FETs). The absence of an energy bandgap is shown to result in severe shortcomings for logic applications.

Possibilities to engineer a bandgap in graphene FETs, including quantum confinement in graphene nanoribbons (GNRs) and electrically or substrate, induced asymmetry in double and multilayer graphene are discussed. Graphene FETs are shown to be of interest for analog radio frequency applications. Finally, novel switching mechanisms in graphene transistors are briefly introduced which could lead to future memory devices.

3.1. Introduction

Graphene has attracted enormous research interest since its experimental discovery in 2004 [NOV 04, BER 04]. It consists of carbon atoms arranged in a two-dimensional (2D) honeycomb crystal lattice with a bond length of 1.42 Å [HAR 89]. A schematic of a single-graphene layer is shown in Figure 3.1(a), including "armchair" and "zigzag" edges, named after their characteristic appearance on the atomic scale.

Chapter written by Max C. LEMME.

Beyond-CMOS Nanodevices 2, First Edition. Edited by Francis Balestra.

The carbon atoms in the graphene lattice are sp2 hybridized and three of the four valence electrons participate in the bonds to their next neighbors (σ-bonds Figure 3.1(b)). The fourth π-electron orbital is oriented perpendicular to the sheet and delocalized (Figure 3.1(b)). The graphene lattice is made up of two equivalent carbon sublattices A and B, which lead to crystal symmetry. As a result, the charge carriers can be described by the Dirac equation [GEI 07], i.e. the band structure of graphene exhibits a linear dispersion relation for charge carriers, with momentum k proportional to energy E. Finally, the energy bands associated with the sublattices intersect at zero energy E resulting in a semi-metal with no bandgap (Eg = 0 eV). A schematic of the band structure in the vicinity of $k = 0$ including the Fermi level EF is shown in Figure 3.1(c).

Charge carriers in graphene possess a very small effective mass [NOV 05a], and hence graphene shows extremely attractive material properties relevant to electronic devices. These include: carrier mobilities up to 15,000 cm^2/Vs for graphene on SiO_2 [NOV 05a], 27,000 cm^2/Vs for epitaxial graphene [BER 06] and 200,000 cm^2/Vs for suspended graphene [BOL 08, MOR 08, Du 08]. In addition, high current carrying capability exceeding 1×10^8 A/cm^2 [MOS 07], high thermal conductivity [BAL 08, GHO 08], high transparency [BLA 08] and mechanical stability [BOO 08] have been reported. While similar promising properties have been reported for carbon nanotubes (CNTs), the fact that graphene sheets can be processed with conventional CMOS-technology is potentially a huge advantage over CNTs. Despite the enthusiasm over the discovery of graphene, however, research is still at an early stage. In this review we therefore discuss the potential of graphene for electronic applications based on experimental data available to date. A short introduction to standard graphene fabrication and detection methods is followed by an overview of the state-of-the-art in graphene metal-oxide-semiconductor field-effect transistors (MOSFETs). We then briefly discuss graphene transistors for high-frequency operation and present various non-classic graphene switches.

3.2. Graphene

3.2.1. *Graphene fabrication*

There are currently three established fabrication methods for graphene: mechanical exfoliation, epitaxial growth from silicon carbide (SiC)

substrates and chemical vapor deposition of hydrocarbons on reactive nickel or transition-metal-carbide surfaces.

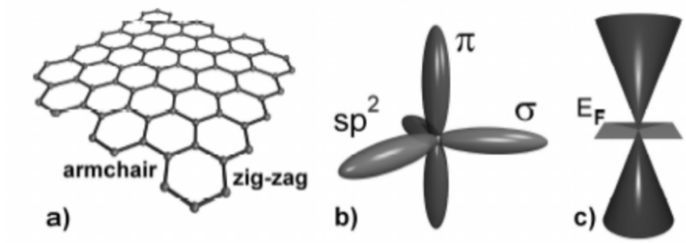


Figure 3.1. *a) Schematic of a graphene crystallite with characteristic armchair and zigzag edges. b) Schematic of electron σ- and π-orbitals of one carbon atom in graphene. c) Band diagram of graphene at k = 0*

3.2.1.1. *Exfoliation*

Novoselov *et al.* have introduced a manual cleaving process of graphite, frequently called "mechanical exfoliation", to obtain single and few-layer graphene [NOV 04, GEI 07]. This process makes use of adhesive tape to pull graphene films off a graphite crystal. These are then thinned down by further strips of tape and finally rubbed against appropriate surfaces like silicon dioxide on silicon, which leaves randomly sized and distributed flakes on the surface. When observed through an optical microscope, single and few-layer graphene flakes add to the optical path compared to the bare wafer. If a proper thickness of silicon dioxide is chosen, the resultant visible contrast is sufficient to identify even single graphene layers [NI 07, BLA 07, ABE 07, CAS 07]. Figure 3.2(a) shows the result of a contrast simulation of a single graphene layer on SiO_2. In this simulation, the contrast is plotted for a range of wavelengths and SiO_2 thicknesses. In the visible range, SiO_2 films of ~90 nm and ~300 nm result in high contrast and have hence been widely used as substrates. This pragmatic, low-cost method has enabled researchers to conduct a wide variety of fundamental physics and engineering experiments, even though it cannot be considered a controlled process in terms of industrial exploitation. An example of typical graphene flakes on an oxidized silicon wafer is shown in Figure 3.2(b). While a trained person can distinguish single- from few-layer grapheme, with high fidelity, using the

"naked eye", Raman spectroscopy has become the method of choice when it comes to scientific proof of single layers [FER 06, FER 07, GRA 07, WAN 08a]. Both G and 2D Raman peaks at around 1,580 cm-1 and 2,700 cm-1 change in shape, position and intensity with the number of graphene layers. This is demonstrated in Figure 3.1(c), where Raman spectra for single- and few-layer graphene, as well as, graphite are plotted. Note that the spectra have been separated for ease of viewing by moving them along the *y*-axes. The baseline intensity is identical for each measurement.

3.2.1.2. *Epitaxial graphene form silicon carbide*

Berger and de Heer have pioneered an epitaxial approach for fabricating graphene from SiC substrates [BER 04, BER 06, DE 07]. During the process, silicon is thermally desorbed at temperatures between 1,250°C and 1,450°C. This process can surely be classified as more controllable and industrially relevant when compared to mechanical cleaving. In fact, it has been shown that graphene transistors can be manufactured from epitaxial graphene on a wafer scale [KED 08]. Similar to exfoliated graphene, it has been demonstrated that single epitaxial graphene layers can be identified by Raman spectroscopy [ROH 08]. In addition, Raman spectroscopy revealed that these layers are compressively strained [ROH 08, NI 08]. A major disadvantage of epitaxial graphene is the extremely high cost of production type SiC wafers, their limited size compared to silicon wafers, and the high processing temperatures above current CMOS limits. With these advantages and disadvantages, it remains to be seen whether epitaxial graphene will find its way into future nanoelectronics applications.

3.2.1.3. *Chemical vapor deposition*

A promising large-area deposition method is currently explored in the form of chemical vapor deposition (CVD) on metallic surfaces like nickel [OBR 07, YU 08, REI 09, KIM 09], ruthenium [SUT 08] and others (see references in [COR 08]). These CVD approaches rely on dissolving carbon into the metal substrates and then forcing it to precipitate out by cooling. Another approach is to grow graphene films directly on iridium [COR 08, NDI 08] or copper [LI 09]. Several methods of transferring the CVD graphene films onto relevant substrates have been suggested, including the use of disposable PMMA or PDMS films. After transfer, Raman spectroscopy has been used to verify single layers, and even devices have been fabricated with typical graphene properties [YU 08, KIM 09, LI 09].

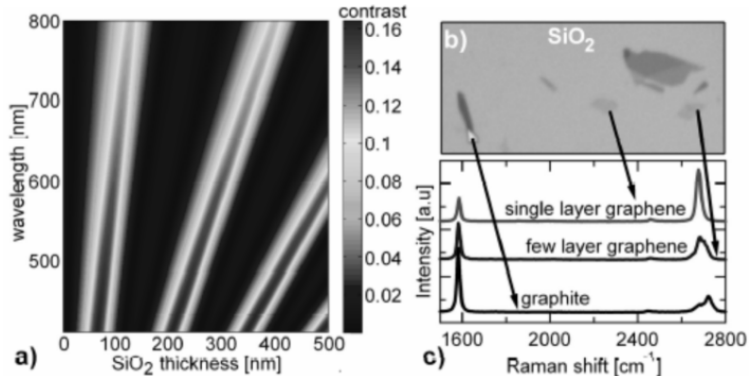


Figure 3.2. *a) Contrast simulation of single layer graphene on a silicon dioxide film on silicon. Blue represents areas of no contrast, whereas red represents the maximum contrast. b) Optical micrograph of macroscopic graphene crystallites of various thicknesses on an SiO_2/ Si substrate. c) Raman spectra of three representative flakes of single- and few-layer graphene and graphite. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

3.2.2. *Macroscopic graphene field effect transistors*

The most straightforward device application of graphene may seem to be as a replacement channel material for silicon MOSFETs. Figure 3.3(a) shows a schematic of such a graphene FET, including a top gate electrode, gate dielectric and source and drain metal contacts. Figure 3.3(b) shows a top-view optical micrograph of a macroscopic graphene FET on silicon dioxide. The fabrication of graphene FETs follows standard silicon process technology once the graphene is deposited and identified. This includes the use of photo- or e-beam lithography, reactive ion etching and thin-film deposition for the gate insulators and contacts. Details of typical fabrication processes are described in references [LEM 07b, ECH 07, WIL 07].

The transfer characteristics (here: drain current I_d vs. back gate voltage V_{bg}) of a typical graphene transistor is shown in Figure 3.4(a). It reveals a major drawback of macroscopic graphene MOSFETs: the absence of an energy bandgap (E_g = 0 eV) severely limits the current modulation in the graphene FET and, in addition, leads to ambipolar behavior. In fact, the best current modulation reported to date has been about 30, measured at cryogenic temperatures [NOV 04]. Furthermore, in conjunction with randomly distributed oxide charges the zero-bandgap leads to a finite minimum charge density even without any applied gate voltage [MAR 08].

Consequently, macroscopic graphene transistors conduct substantial current even at their point of minimum conductance (also referred to as Dirac point or charge neutrality point), preventing their application as a silicon MOSFET replacement in future CMOS-type logic circuits.

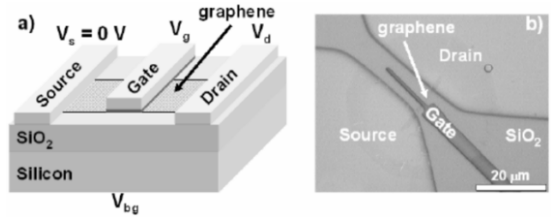


Figure 3.3. *a) Schematic cross-section, and b) optical top-view micrograph of a graphene field effect transistor (image modified and reproduced with permission from ECS transactions, 11(6) (2007) [LEM 07a]. Copyright 2007, The Electrochemical Society)*

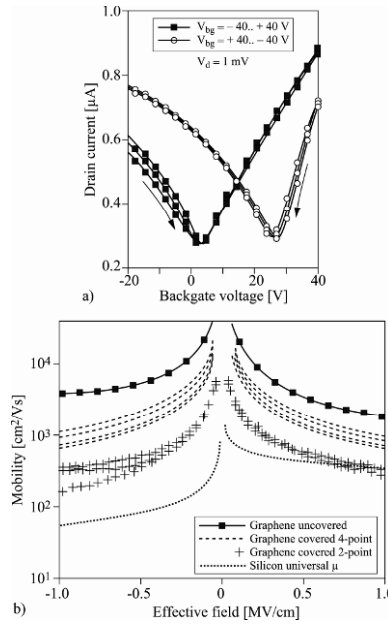


Figure 3.4. *a) Drain current versus back gate voltage of a graphene FET. Changing the sweep direction results in considerable hysteresis of ΔV = 22 V. b) Mobility versus electric field in graphene FETs. Covering graphene with a gate insulator leads to mobility reduction. Contacts have a considerable influence on graphene FETs. Universal mobility of silicon included as reference (after Takagi [TAK 94]) (graph modified and reproduced with permission from ECS Transactions, 11(6) (2007) [LEM 07a]. Copyright 2007, The Electrochemical Society)*

Figure 3.4(a) further shows hysteresis as the gate voltage is swept from negative to positive direction and vice versa. This typical behavior occurs despite measuring in vacuum conditions ($P = 5 \times 10^{-3}$ mbar) and is a strong indicator of charge traps near the graphene/insulator interface. While suspended graphene measured in ultra-high vacuum conditions has been shown to have mobilities exceeding 200,000 cm^2/Vs, realistic graphene FETs are limited in performance by substrates and top gates. Nonetheless, the carrier mobilities in top-gated devices exceed those of silicon and are typically in the order of several hundred to a thousand cm^2/Vs, even though not all graphene/insulator interfaces have been optimized yet [LEM 07a, WIL 07, LEM 08, LIN 09]. Figure 3.4(b) shows electron and hole mobilities extracted from several top gated devices, both in 2-point and by 4-point probe configuration..

3.2.3. *Graphene nanoribbon transistors*

A potential method to create a bandgap in graphene is to cut it into narrow ribbons of less than a few tens of nanometers (GNRs). However, GNRs must be divided into two sub-types as indicated in Figure 3.1: armchair and zigzag edge terminated ribbons. Both types of GNR may be semiconducting or semimetallic. In armchair ribbons, the transition from 2D graphene to 1D GNRs leads to quantum confinement and a bandgap that is roughly inversely proportional to the nanoribbon width ($E_g \sim 1/W$) according to simulations [NAK 96, BAR 06]. The precise value of the bandgap is further predicted to depend on the number N of carbon atoms across the ribbon [NAK 96, BAR 06, SON 06, OBR 06]. This is demonstrated in Figure 3.5(a), where the simulated density of states (DOS) versus energy for three different hydrogen-terminated armchair GNRs with $N = 11$, 12 and 13 atoms across the GNR width is shown [YAN 99] (see section 3.5 regarding simulation services). While the GNR with $N = 11$ is semimetallic, the ribbons with 12 and 13 atoms are semiconducting (generally armchair ribbons are semimetallic at $N = 3m - 1$, where m is an integer [FUJ 96]). In hydrogen-terminated zigzag GNRs, however, the situation is more complicated. It has been predicted by Nakada *et al.* that localized edge states near the Fermi level lead to semimetallic behavior, regardless of the number of carbon atoms [NAK 96]. On the other hand, Son *et al.* have calculated *ab initio* that edge magnetization causes a staggered sublattice potential on the graphene lattice that induces a bandgap [SON 06]. Finally, GNRs with other chiral orientations have been considered, including a mix of edges along a

ribbon, adding to the complexity of this option [HUA 07, YAN 07, KAN 07, HOD 07, KUD 08, YOO 07, SOL 07]. In summary, the simulated results for any form of GNRs should be regarded with care, as they typically share an optimistic assumption of well-controlled termination of dangling bonds. In reality, however, there is very likely a great variety of chemical groups terminating the edge atoms of a single graphene nanoribbon. The first detailed discussion has recently been published to address these issues [CER 08], but it is probably reasonable to consider the nature of "real life" zig-zag GNRs as an open question at this point in time. The predicted presence of a bandgap in specific GNRs has been experimentally confirmed. The first evidence was reported by Han *et al.* [HAN 07] and Chen *et al.* [CHE 07], where GNRs were structured by e-beam lithography and etched in oxygen plasma with minimum widths of ~20 nm. The bandgaps of these GNRs where in the range of ~30 meV and resulted in field effect transistors with *I*on/*I*off ratios of about 3 orders of magnitude at low temperatures (1.7 – 4 K), reduced to a ratio of ~10 at room temperature. These investigations support theoretical predictions that sub-10 nm GNRs are required for true field effect transistor action at room temperature. More importantly, the experiments revealed a bandgap regardless of the chiral orientation of the GNRs [HAN 07]. This latter result was attributed to a strong influence of edge states, which dominates the chirality dependency of the band structure. To date, two examples of sub-10 nm GNRs have been shown experimentally. Ponomarenko *et al.* have fabricated GNRs with a minimum width of about 1 nm and a bandgap of about 500 meV using e-beam lithography and repeated, careful over-etching [PON 08]. The resulting transistors consequently switched off at room temperature to "no measurable conductance". An alternative fabrication process for GNRs has been presented by Li *et al.* [LI 08]. Here, graphene ribbons were a solution derived from graphite by thermal exfoliation, sonification and centrifugation. The resulting solution was dispersed onto substrates and GNRs were identified with an atomic force microscope (AFM). The resulting devices exhibited well-behaved transistor action at room temperature with *I*on/*I*off ratios of more than 106 [LI 08, WAN 08b]. Finally, unzipping of carbon nanotubes by etching or sputtering has been experimentally shown to result in GNRs [KOS 09, JIA 09]. Interestingly, all GNR transistors in these studies were semiconducting, even though both armchair and zig-zag orientations were believed to be present. The experimental *I*on/*I*off ratios that have been reported to date are summarized in Figure 3.5(b). While they clearly support theoretical predictions and show promise for graphene

nanoribbon electronics, they also show an urgent need for further research in this field: statistical data is obviously scarce and the discrepancies between theory and experiment have to be addressed. The necessity of controllable sub-10 nm feature sizes and great uncertainties in chirality control as well as edge state definition remain tremendous challenges toward future industrial applicability. To this end, a recently developed technique, helium ion beam microscopy, has been shown to have potential for precise nanopatterning of graphene [LEM 09, BEL 09].

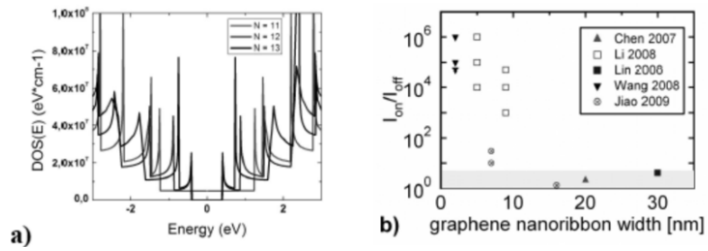


Figure 3.5. *a) Simulated density of states (DOS) versus energy of hydrogen terminated armchair graphene nanoribbons (GNRs) for various numbers of electrons N across the ribbon [NOV 04]. b) Experimental Ion/Ioff ratios versus GNR width taken from literature. None of the GNRs reported thus far has shown metallic behavior. The lower colored part of the graph indicates Ion/Ioff values of typical macroscopic graphene FETs. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

3.2.4. *Bilayer graphene and substrate effects*

A viable approach to obtain a bandgap in graphene is to break its symmetry. McCann proposed that macroscopic double- or bilayer graphene films would display a bandgap if a transverse electric field was applied to them to cause layer asymmetry [MCC 06]. His calculations predict a roughly linear dependence of the bandgap on the carrier density n, with each 1012 cm^{-2} adding about 10 meV to the gap. This prediction was experimentally confirmed by Ohta *et al.* on bilayer graphene films on SiC through angle-resolved photoemission spectroscopy (ARPES) [OHT 06]. In their work, they used potassium doping to modify the carrier density in the graphene, which lead to changes in the electronic bandgap. Oostinga *et al.* took this approach a step further by applying an electrostatic field through a top gate electrode. Their bilayer graphene device showed a bandgap in the range of a few meV, demonstrated with low-temperature measurements at 4 K [OOS 08].

A related concept has been demonstrated by Zhou *et al.*, who report a much more significant bandgap in single-layer graphene on SiC of 260 meV, again obtained by ARPES measurements [ZHO 07]. As the number of graphene layers increases, the bandgap was found to decrease. Here, the gap is attributed to a broken A, B sublattice symmetry in the graphene, caused by a buffer layer between the SiC crystal and the graphene [VAR 07]. While this approach seems to indicate the feasibility of macroscopic graphene transistors with high *I*on/*I*off ratios at room temperature, to date there have been no experimental reports of such devices on single-layer graphene on SiC. Even an extensive study by Kedzierski *et al.* [KED 08], who investigated a statistically relevant number of several hundreds of graphene transistors on SiC, did not reveal a considerable bandgap in any of the devices. While mobility values exceeding those of silicon transistors were achieved, all devices showed typical "zero-gap" graphene characteristics similar to Figure 3.3(c). In summary, electrically induced bandgaps in bilayer graphene have been observed, but their small absolute value prevents an application in room temperature field effect transistors. While a larger substrate induced bandgap has been observed by ARPES for single-layer graphene on SiC, this result remains to be confirmed in an actual electronic device.

3.2.5. *RF transistors*

The discussed lack of a bandgap at room temperature in macroscopic graphene FETs makes them unsuitable for logic applications. For radio-frequency (RF) analog applications, on the other hand, a high on–off ratio is desirable but not mandatory. Instead, the most important aspect for good RF performance is a FET channel with excellent carrier transport properties (high mobility and maximum velocity) [SCH 07] combined with a small-scale length, which improves strongly as the channel material thickness is reduced [FRA 98]. As graphene fulfils these requirements, graphene RF FETs have recently been investigated, made from exfoliated [LIN 09, MER 08], epitaxial [MOO 09] and CVD graphene. The reported cut-off frequencies are plotted as a function of gate lengths in Figure 3.6 for a *number* of publications in literature. The maximum cut-off frequencies reported exceed 300 GHz for sub-100 nm gate lengths, and the results are almost independent of the graphene fabrication method. This is a good sign for CVD graphene, which is the most likely candidate for future mass production.

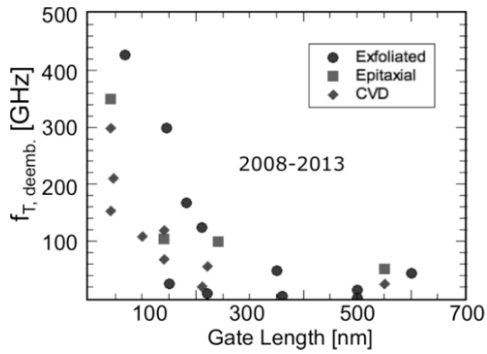


Figure 3.6. *Summary of published graphene RF transistor cut-off frequencies*

3.2.6. *Alternative graphene switches*

A number of concepts for (non-volatile) graphene switches have emerged that operate on mechanisms other than the classic semiconductor field effect. Even though a thorough review is beyond the scope of this chapter, they are briefly introduced in this section.

The first concept is graphene/graphene-oxide (GO) Schottky barrier MOSFETs [WU 08], where semiconducting GO acts as the transistor channel. Another approach suggests atomic-scale graphene switches that are based on creating nanoscale gaps by electric fields in graphene films [STA 08]. These physical gaps are reversibly opened and closed by breaking and reforming the carbon atomic chains in the graphene. Chemical surface modification strongly affects the electronic band structure of graphene [BOU 08]. We reversibly modified the drain current electrostatically in a graphene FET similar to Figure 3.3(a) by controlled chemisorption [ECH 08]. Ferroelectric gating has been shown to electrostatically dope graphene and change the drain currents in a non-volatile way [ZHE 09]. While these early concepts are far from mature, they, nevertheless, demonstrate the potential of graphene for nanoelectronics applications that might not be anticipated today.

Vertical devices have received considerable attention lately. One such candidate, a graphene-based hot electron transistor has been proposed conceptually [MEH 12] and later demonstrated in experiments [VAZ 13]: a graphene sheet is sandwiched between two insulators, with metals or doped semiconductors on both sides (see Figure 3.7(a)). Carrier transport is vertical

and happens by way of quantum mechanical tunneling. In such a device, the base contact is made up of graphene (hence Graphene Base Transistor, GBT), because the combination of high electrical conductivity and extreme thinness of the material leads to high transmission of charge carriers: the graphene transition time is expected to be much lower than for metals, which need to be thicker. When a voltage is applied to the graphene base, the current can be modulated by several orders of magnitude (Figure 3.7(b)). This happens because the graphene base potential modulates the tunneling barrier between the emitter and the base. Above a certain threshold, charge carriers may tunnel via the Fowler – Nordheim mechanism and reach the collector by ballistic transport (Figure 3.7(c)).

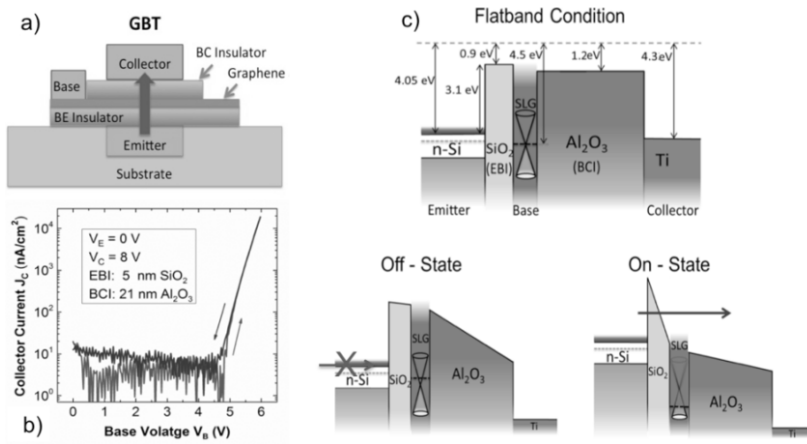


Figure 3.7. *a) Schematic of a vertical hot electron transistor with a base made of graphene (Graphene Base Transistor, GBT). b) Transfer characteristics of a GBT. c) Band structure of a GBT with SiO_2 and Al_2O_3 barriers in the flat band condition, the off-state and the on-state [VAZ 13]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices2.zip*

3.3. 2D materials beyond graphene

Encouraged by the scientific excitement surrounding the discovery of graphene, researchers began to consider other isolated 2D materials early on [NOV 05b]. These 2D materials may behave like insulators (e.g. hexagonal boron nitride, h-BN) or semiconductors, such as transition metal dichalcogenides (TMDs) molybdenum disulfide (MoS2) or tungsten diselenide (WSe). Like graphite, these materials have been known for quite some time, but it was only recently that they have been isolated in single-

layer form and manufactured into solid-state devices. As with graphene and graphite, these 2D crystals change their properties compared to their bulk counterparts. MoS2, for example, is an indirect semiconductor with a bandgap of approximately 1.2 eV in bulk form, but changes to a direct semiconductor with a bandgap of 1.8 eV when isolated in a single layer. This has been confirmed in experiments with field effect transistors made with MoS2 (and other) channels [RAD 11]. The charge carrier mobility in MoS2 transistors can theoretically reach values of about 400 cm^2/Vs and is thus lower than that of state-of-the-art silicon devices. On the other hand, the ultimate thinness of the material means that the scale length λ should be lower than in silicon transistors, translating to improved gate length scalability compared silicon or even silicon on insulator transistors. In addition, the carrier mobility of ultrathin SOI devices is typically reduced to several 10 cm^2/Vs due to surface roughness scattering. Thus, nanoscale TMD-based transistors may yet have an advantage over their silicon counterparts. In fact, MoS2 has been used to fabricate simple integrated circuits such as NAND gates, static random access memory and ring oscillators [WAN 12], and recently, the scaling behavior of MoS2 transistors has been investigated in detail [LIU 12]. While first experiments were carried out on exfoliated TMDs, there is trend toward experiments on CVD MoS2, in analogy to graphene research [ZHA 12]. Despite these advances in experimental device research, all 2D materials are far from being manufacturable, and substantial research is required in this field.

3.4. Conclusions

The potential of graphene-based field effect transistors to supplement or substitute existing silicon CMOS technology has been assessed. While macroscopic graphene transistors are not suitable for logic application due to the lack of an energy bandgap, graphene RF transistors seem promising and feasible. GNRs, on the other hand, show extreme promise as a straightforward CMOS compatible approach, but their extreme sensitivity on an atomic level to both geometric and edge termination variations may well render their application impossible. Recent discoveries of non-classic switching mechanisms or tunneling-based devices may eventually lead to a cointegration of graphene into silicon technology, even though details of manufacturability and variability are far from clear today. In addition to these device related issues, a major roadblock for the application of graphene is the unavailability of a large area, CMOS compatible deposition technique.

However, chemical vapor deposition is maturing and carries potential for future manufacturing. Finally, other 2D materials such as the semiconductor molybdenum disulfide may fill gaps, where graphene fails to deliver solutions. Experiments on the device level are promising, accompanied by first successful demonstrations of methods for large area deposition of these materials. An ultimate vision would be devices and circuits made up entirely of 2D material stacks and placed on arbitrary substrates, including flexible polymers, clothes.

3.5. Acknowledgments

M.C. Lemme gratefully acknowledges support from the European Commission through an ERC Starting Grant (InteGraDe, No. 307311) and a collaboration project (GRADE, No. 317839), as well as the German Research Foundation (DFG, LE 2440/1-1). Simulation services for results presented here were provided by the Network for Computational Nanotechnology (NCN) at nanoHUB.org.

3.6. Bibliography

[ABE 07] ABERGEL D.S.L., RUSSELL A., FAL'KO V.I., "Visibility of graphene flakes on a dielectric substrate", *Applied Physics Letters*, vol. 91, no. 6, pp. 063125–3, 2007.

[BAL 08] BALANDIN A.A., GHOSH S., BAO W., *et al.*, "Superior thermal conductivity of single-layer graphene", *Nano Letters*, vol. 8, no. 3, pp. 902–907, 2008.

[BAR 06] BARONE V., HOD O., SCUSERIA G.E., "Electronic structure and stability of semiconducting graphene nanoribbons", *Nano Letters*, vol. 6, no. 12, pp. 2748–2754, 2006.

[BEL 09] BELL D.C., LEMME M.C., STERN L.A., *et al.*, "Precision cutting and patterning of graphene with helium ions", *Nanotechnology*, vol. 20, no. 45, p. 455301, 2009.

[BER 04] BERGER C., SONG Z.M., LI T.B., *et al.*, "Ultrathin epitaxial graphite: 2D electron gas properties and a route toward graphene-based nanoelectronics", *Journal of Physical Chemistry B*, vol. 108, no. 52, pp. 19912–19916, 2004.

[BER 06] BERGER C., SONG Z.M, LI X.B., *et al.*, "Electronic confinement and coherence in patterned epitaxial graphene", *Science*, vol. 312, no. 5777, pp. 1191–1196, 2006.

[BLA 07] BLAKE P., HILL E.W., NETO A.H.C., *et al.*, "Making graphene visible", *Applied Physics Letters*, vol. 91, no. 6, pp. 063124–3, 2007.

[BLA 08] BLAKE P., BRIMICOMBE P.D., NAIR R.R., *et al.*, "Graphene-based liquid crystal device", *Nano Letters*, vol. 8, no. 6, pp. 1704–1708, 2008.

[BOL 08] BOLOTIN K.I., SIKES K.J., JIANG Z., *et al.*, "Ultrahigh electron mobility in suspended graphene", *Solid State Communications*, vol. 146, no. 9–10, pp. 351–355, 2008.

[BOO 08] BOOTH T.J., BLAKE P., NAIR R.R., *et al.*, "Macroscopic graphene membranes and their extraordinary stiffness", *Nano Letters*, vol. 8, no. 8, pp. 2442–2446, 2008.

[BOU 08] BOUKHVALOV D.W., KATSNELSON M.I., "Tuning the gap in bilayer graphene using chemical functionalization: density functional calculations", *Physical Review B (Condensed Matter and Materials Physics)*, vol. 78, no. 8, pp. 085413–5, 2008.

[CAS 07] CASIRAGHI C., HARTSCHUH A., LIDORIKIS E., *et al.*, "Rayleigh imaging of graphene and graphene layers", *Nano Letters*, vol. 7, no. 9, pp. 2711–2717, 2007.

[CER 08] CERVANTES-SODI F., CSANYI G., PISCANEC S., *et al.*, "Edge-functionalized and substitutionally doped graphene nanoribbons: electronic and spin properties", *Physical Review B (Condensed Matter and Materials Physics)*, vol. 77, no. 16, pp. 165427–13, 2008.

[CHE 07] CHEN Z., LIN Y.-M., ROOKS M.J., *et al.*, "Graphene nano-ribbon electronics", *Physical Review E: Low-Dimensional Systems and Nanostructures*, vol. 40, no. 2, pp. 228–232, 2007.

[COR 08] CORAUX J., N`DIAYE A.T., BUSSE C., *et al.*, "Structural coherency of graphene on Ir(111)", *Nano Letters*, vol. 8, no. 2, pp. 565–570, 2008.

[DE 07] DE HEER W.A., BERGER C., WU X., *et al.*, "Epitaxial graphene", *Solid State Communications*, vol. 143, no. 1–2, pp. 92–100, 2007.

[DU 08] DU X., SKACHKO I., BARKER A., *et al.*, "Approaching ballistic transport in suspended graphene", *Nat Nano*, vol. 3, no. 8, pp. 491–495, 2008.

[ECH 07] ECHTERMEYER T.J., LEMME M.C., BOLTEN J., *et al.*, "Graphene field-effect devices", *European Physical Journal- Special Topics*, vol. 148, pp. 19–26, 2007.

[ECH 08] ECHTERMEYER T.J., LEMME M.C., BAUS M., *et al.*, "Nonvolatile switching in graphene field-effect devices", *Electron Device Letters*, *IEEE*, vol. 29, no. 8, pp. 952–954, 2008.

[FER 06] FERRARI A.C., "Raman spectrum of graphene and graphene layers", *Physical Review Letters*, vol. 97, no. 18, pp. 187401–4, 2006.

[FER 07] FERRARI A.C., "Raman spectroscopy of graphene and graphite: disorder, electron-phonon coupling, doping and nonadiabatic effects", *Solid State Communications*, vol. 143, no. 1–2, pp. 47–57, 2007.

[FRA 98] FRANK D.J., TAUR Y., WONG H.S.P., "Generalized scale length for two-dimensional effects in MOSFETs", *Electron Device Letters*, *IEEE*, vol. 19, no. 10, pp. 385–387, 1998.

[FUJ 96] FUJITA M., WAKABAYASHI K., NAKADA K., *et al.*, "Peculiar localized state at zigzag graphite edge", *Journal of Physical Society of Japan*, vol. 65, no. 7, pp. 1920–1923, 1996.

[GEI 07] GEIM A.K., NOVOSELOV K.S., "The rise of graphene", *Nature Materials*, vol. 6, no. 3, pp. 183–191, 2007.

[GHO 08] GHOSH S., CALIZO I., TEWELDEBRHAN D., *et al.*, "Extremely high thermal conductivity of graphene: prospects for thermal management applications in nanoelectronic circuits", *Applied Physics Letters*, vol. 92, no. 15, pp. 151911–3, 2008.

[GRA 07] GRAF D., MOLITOR F., ENSSLIN K., *et al.*, "Spatially resolved Raman spectroscopy of single- and few-layer graphene", *Nano Letters*, vol. 7, no. 2, pp. 238–242, 2007.

[HAN 07] HAN M.Y., OZYILMAZ B., ZHANG Y., *et al.*, "Energy band-gap engineering of graphene nanoribbons", *Physical Review Letters*, vol. 98, no. 20, pp. 206805–4, 2007.

[HAR 89] HARRISON W.A. (ed.), *Electronic Structure and Properties of Solids: The Physics of the Chemical Bond*, Dover Publications, 1989.

[HOD 07] HOD O., BARONE V., PERALTA J.E., *et al.*, "Enhanced half-metallicity in edge-oxidized zigzag graphene nanoribbons", *Nano Letters*, vol. 7, no. 8, pp. 2295–2299, 2007.

[HUA 07] HUANG B., YAN Q., ZHOU G., *et al.*, "Making a field effect transistor on a single graphene nanoribbon by selective doping", *Applied Physics Letters*, vol. 91, no. 25, pp. 253122–3, 2007.

[JIA 09] JIAO L., ZHANG L., WANG X., *et al.*, "Narrow graphene nanoribbons from carbon nanotubes", *Nature*, vol. 458, no. 7240, pp. 877–880, 2009.

[KAN 07] KAN E.-J., LI Z., YANG J., *et al.*, "Will zigzag graphene nanoribbon turn to half metal under electric field?", *Applied Physics Letters*, vol. 91, no. 24, pp. 243116–3, 2007.

[KED 08] KEDZIERSKI J., PEI-LAN H., HEALEY P., *et al.*, "Epitaxial graphene transistors on SiC substrates", *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 2078–2085, 2008.

[KIM 09] KIM K.S., ZHAO Y., JANG H., *et al.*, "Large-scale pattern growth of graphene films for stretchable transparent electrodes", *Nature*, vol. 457, no. 7230, pp. 706–710, 2009.

[KOS 09] KOSYNKIN D.V., HIGGINBOTHAM A.L., SINITSKII A., *et al.*, "Longitudinal unzipping of carbon nanotubes to form graphene nanoribbons", *Nature*, vol. 458, no. 7240, pp. 872–876, 2009.

[KUD 08] KUDIN K.N., "Zigzag graphene nanoribbons with saturated edges", *ACS Nano*, vol. 2, no. 3, pp. 516–522, 2008.

[LEM 07a] LEMME M.C., ECHTERMEYER T., BAUS M., *et al.*, "Towards graphene field effect transistors", *ECS Transactions*, vol. 11, no. 6, pp. 413–419, 2007.

[LEM 07b] LEMME M.C., ECHTERMEYER T.J., BAUS M., *et al.*, "A graphene field-effect device", *Electron Device Letters*, *IEEE*, vol. 28, no. 4, pp. 282–284, 2007.

[LEM 08] LEMME M.C., ECHTERMEYER T.J., BAUS M., *et al.*, "Mobility in graphene double gate field effect transistors", *Solid-State Electronics*, vol. 52, no. 4, pp. 514–518, 2008.

[LEM 09] LEMME M.C., BELL D.C., WILLIAMS J.R., *et al.*, "Etching of graphene devices with a helium ion beam", *ACS Nano*, vol. 3, no. 9, pp. 2674–2676, 2009.

[LI 08] LI X., WANG X., ZHANG L., *et al.*, "Chemically derived, ultrasmooth graphene nanoribbon semiconductors", *Science*, vol. 319, no. 5867, pp. 1229–1232, 2008.

[LI 09] LI X., CAI W., AN J., *et al.*, "Large-area synthesis of high-quality and uniform graphene films on copper foils", *Science*, vol. 324, no. 5932, pp. 1312–1314, 2009.

[LIN 09] LIN Y.-M., JENKINS K.A., VALDES-GARCIA A., *et al.*, "Operation of graphene transistors at gigahertz frequencies", *Nano Letters*, vol. 9, no. 1, pp. 422–426, 2009.

[LIU 12] LIU H., NEAL A.T., YE P.D., "Channel length scaling of MoS2 MOSFETs", *ACS Nano*, vol. 6, no. 10, pp. 8563–8569, 2012.

[MAR 08] MARTIN J., AKERMAN N., ULBRICHT G., *et al.*, "Observation of electron-hole puddles in graphene using a scanning single-electron transistor", *Nature Physics*, vol. 4, no. 2, pp. 144–148, 2008.

[MCC 06] MCCANN E., "Asymmetry gap in the electronic band structure of bilayer graphene", *Physical Review B (Condensed Matter and Materials Physics)*, vol. 74, no. 16, pp. 161403–161404, 2006.

[MEH 12] MEHR W., SCHEYTT J.C., DABROWSKI J., *et al.*, "Vertical graphene base transistor", *Electron Device Letters*, *IEEE*, vol. 33, no. 5, pp. 691–693, 2012.

[MER 08] MERIC I., BAKLITSKAYA N., KIM P., *et al.*, "RF performance of top-gated, zero-bandgap graphene field-effect transistors", *Electron Devices Meeting*, *2008. IEDM 2008. IEEE International*, 2008.

[MOO 09] MOON J.S., CURTIS D., HU M., *et al.*, "Epitaxial-graphene RF field-effect transistors on Si-face 6H-SiC substrates", *Electron Device Letters*, *IEEE*, vol. 30, no. 6, pp. 650–652, 2009.

[MOR 08] MOROZOV S.V., NOVOSELOV K.S., KATSNELSON M.I., *et al.*, "Giant intrinsic carrier mobilities in graphene and its bilayer", *Physical Review Letters*, vol. 100, no. 1, pp. 016602–4, 2008.

[MOS 07] MOSER J., BARREIRO A., BACHTOLD A., "Current-induced cleaning of graphene", *Applied Physics Letters*, vol. 91, no. 16, pp. 163513–3, 2007.

[NAK 96] NAKADA K., FUJITA M., DRESSELHAUS G., *et al.*, "Edge state in graphene ribbons: nanometer size effect and edge shape dependence", *Physical Review B*, vol. 54, no. 24, p. 17954, 1996.

[NDI 08] N'DIAYE A.T., CORAUX J., PLASA T.N., *et al.*, "Structure of epitaxial graphene on Ir(111)", *New Journal of Physics*, vol. 10, no. 4, p. 043033, 2008.

[NI 07] NI Z.H., WANG H.M., KASIM J., *et al.*, "Graphene thickness determination using reflection and contrast spectroscopy", *Nano Letters*, vol. 7, no. 9, pp. 2758–2763, 2007.

[NI 08] NI Z.H., CHEN W., FAN X.F. , *et al.*, "Raman spectroscopy of epitaxial graphene on a SiC substrate", *Physical Review B (Condensed Matter and Materials Physics)*, vol. 77, no. 11, pp. 115416–6, 2008.

[NOV 04] NOVOSELOV K.S., GEIM A.K., MOROZOV S.V., *et al.*, "Electric field effect in atomically thin carbon films", *Science*, vol. 306, no. 5696, pp. 666–669, 2004.

[NOV 05a] NOVOSELOV K.S., GEIM A.K., MOROZOV S.V., *et al.*, "Two-dimensional gas of massless Dirac fermions in graphene", *Nature*, vol. 438, no. 7065, pp. 197–200, 2005.

[NOV 05b] NOVOSELOV K.S., JIANG D., SCHEDIN F., *et al.*, "Two-dimensional atomic chrystals", *Proceedings of the National Academy of Sciences*, vol. 102, no. 30, pp. 10451–10453, 2005.

[OBR 06] OBRADOVIC B., KOTLYAR R., HEINZ F., *et al.*, "Analysis of graphene nanoribbons as a channel material for field effect transistors", *Applied Physics Letters*, vol. 88, no. 14, pp. 142102–3., 2006

[OBR 07] A.N. OBRAZTSOV, E.A. OBRAZTSOVA, A.V. TYURNINA., *et al.*, "Chemical vapor deposition of thin graphite films of nanometer thickness", *Carbon*, vol. 45, no. 10, pp. 2017–2021, 2007.

[OHT 06] T. OHTA, A. BOSTWICK, T. SEYLLER., *et al.*, "Controlling the electronic structure of bilayer graphene", *Science*, vol. 313, no. 5789, pp. 951–954, 2006.

[OOS 08] J.B. OOSTINGA, H.B. HEERSCHE, X. LIU., *et al.*, "Gate-induced insulating state in bilayer graphene devices", *Nat Mater*, vol. 7, no. 2, pp. 151–157, 2008.

[PON 08] PONOMARENKO L.A., SCHEDIN F., KATSNELSON M.I., *et al.*, "Chaotic dirac villiard in graphene quantum dots", Science, vol. 320, no. 5874, pp. 356–358, 2008.

[RAD 11] RADISAVLJEVIC B, RADENOVIC A, BRIVIO J., *et al.*, "Single-layer MoS2 transistors", *Nature Nanotechnology*, vol. 6, pp. 147–150, 2011.

[REI 09] A. REINA, X. JIA, J. HO., *et al.*, "Large area, few-layer graphene films on arbitrary substrates by chemical vapor deposition", *Nano Letters*, vol. 9, no. 1, pp. 30–35, 2009.

[ROH 08] J. ROHRL, M. HUNDHAUSEN, K.V. EMTSEV., *et al.*, "Raman spectra of epitaxial graphene on SiC(0001)", *Applied Physics Letters*, vol. 92, no. 20, pp. 201918–3, 2008.

[SCH 07] SCHWIERZ F., LIOU J.J., "RF transistors: recent developments and roadmap toward terahertz applications", *Solid-State Electronics*, vol. 51, no. 8, pp. 1079–1091, 2007.

[SOL 07] SOLS F., GUINEA F., NETO A.H.C., "Coulomb blockade in graphene nanoribbons", *Physical Review Letters*, vol. 99, no. 16, pp. 166803–4, 2007.

[SON 06] SON Y.-W., COHEN M.L., LOUIE S.G., "Energy gaps in graphene nanoribbons", *Physical Review Letters*, vol. 97, no. 21, pp. 216803–4, 2006.

[STA 08] STANDLEY B., BAO W., ZHANG H., *et al.*, "Graphene-based atomic-scale switches", *Nano Letters*, vol. 8, no. 10, pp. 3345–3349, 2008.

[SUT 08] SUTTER P.W., FLEGE J.-I., SUTTER E.A., "Epitaxial graphene on ruthenium", *Nat Mater*, vol. 7, no. 5, pp. 406–411, 2008.

[TAK 94] TAKAGI S., TORIUMI A., IWASE M., *et al.*, "On the universality of inversion layer mobility in Si MOSFET's: part I: effects of substrate impurity concentration", *Electron Devices*, *IEEE Transactions on*, vol. 41, no. 12, pp. 2357–2362, 1994.

[VAR 07] VARCHON F., FENG R., HASS J., LI X., *et al.*, "Electronic structure of epitaxial graphene layers on SiC: effect of the substrate", *Physical Review Letters*, vol. 99, no. 12, pp. 126805–4, 2007.

[VAZ 13] VAZIRI S., LUPINA G., HENKEL C., "A graphene-based hot electron transistor", *Nano Letters*, vol. 13, no. 4, pp. 1435–1439, 2013.

[WAN 08a] WANG Y.Y., NI Z.H., SHEN Z.X., *et al.*, "Interference enhancement of Raman signal of graphene", *Applied Physics Letters*, vol. 92, no. 4, pp. 043121–3, 2008.

[WAN 08b] WANG X., OUYANG Y., LI X., *et al.*, "Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors", *Physical Review Letters*, vol. 100, no. 20, pp. 206803–4, 2008.

[WAN 12] WANG H., YU L., LEE Y.-H., *et al.*, "Integrated circuits based on bilayer MoS2 transistors", *Nano Letters*, vol. 12, no. 9, pp. 4674–4680, 2012.

[WIL 07] WILLIAMS J.R., DICARLO L., MARCUS C.M., "Quantum hall effect in a gate-controlled p-n junction of graphene", *Science*, vol. 317, no. 5838, pp. 638–641, 2007.

[WU 08] SPRINKLE X. WU, LI M., X., *et al.*, "Epitaxial-graphene/graphene-oxide junction: an essential step towards epitaxial graphene electronics", *Physical Review Letters*, vol. 101, no. 2, pp. 026801–4, 2008.

[YAN 99] YANG L., ANANTRAM M.P., HAN J., *et al.*, "Band-gap change of carbon nanotubes: effect of small uniaxial and torsional strain", Physical Review B, vol. 60, no. 19, p. 13874, 1999.

[YAN 07] YAN Q., HUANG B., YU J., *et al.*, "Intrinsic current-voltage characteristics of graphene nanoribbon transistors and effect of edge doping", *Nano Letters*, vol. 7, no. 6, pp. 1469–1473, 2007.

[YOO 07] YOON Y., GUO J., "Effect of edge roughness in graphene nanoribbon transistors", *Applied Physics Letters*, vol. 91, no. 7, pp. 073103–3, 2007.

[YU 08] YU Q., LIAN J., SIRIPONGLERT S., *et al.*, "Graphene segregated on Ni surfaces and transferred to insulators", *Applied Physics Letters*, vol. 93, no. 11, pp. 113103–3, 2008.

[ZHA 12] ZHAN Y., LIU Z., NAJMAEI S., *et al.*, "Large-area vapor-phase growth and characterization of MoS2 atomic layers on a SiO_2 substrate", *Small*, vol. 8, no. 7, pp. 966–971, 2012.

[ZHE 09] ZHENG Y., NI G.-X., TOH C.-T., *et al.*, "Gate-controlled nonvolatile graphene-ferroelectric memory", *Applied Physics Letters*, vol. 94, no. 16, pp. 163505–3, 2009.

[ZHO 07] ZHOU S. Y., GWEON G. H., FEDOROV A. V., *et al.*, "Substrate-induced bandgap opening in epitaxial graphene", *Nat Mater*, vol. 6, no. 10, pp. 770–775, 2007.

4

Nanoelectromechanical Switches

4.1. Context

Today, all the digital integrated circuits use complementary metal-oxide-semiconductor (CMOS) technology. The success of the CMOS technology semiconductor industry is based on scaling of the MOS transistor allowing cost decrease and performance improvement. However, as number of transistors increase on a chip exponentially, the leakage power due to subthreshold currents and tunnel currents also increases. It is difficult to reduce the supply voltage below 1 V, and in the end the increase of leakage and active power is not compatible with the future needs of the information and communication applications, especially if we consider the constraints of the Internet of Things. These considerations explain why researchers are now interested in new devices offering lower leakage power. Tunnel field effect transistors (TFET) and nano-electromechanical systems (NEMS) appear to be the most promising future components.

The use of mechanical devices for computing is very old technology. The first mechanical machine is attributed to the French physicist Blaise Pascal, who built an adding system. In 1834, the British engineer Charles Babbage fabricated the first mechanically programmable machine. In 1835, John Henry invented the electromechanical relay and the second half of the 19th Century was the most active period for the development of mechanical computing. However, these calculators were limited in performance, expensive and consumed a lot of power.

Chapter written by Hervé FANET.

Beyond-CMOS Nanodevices 2, First Edition. Edited by Francis Balestra.

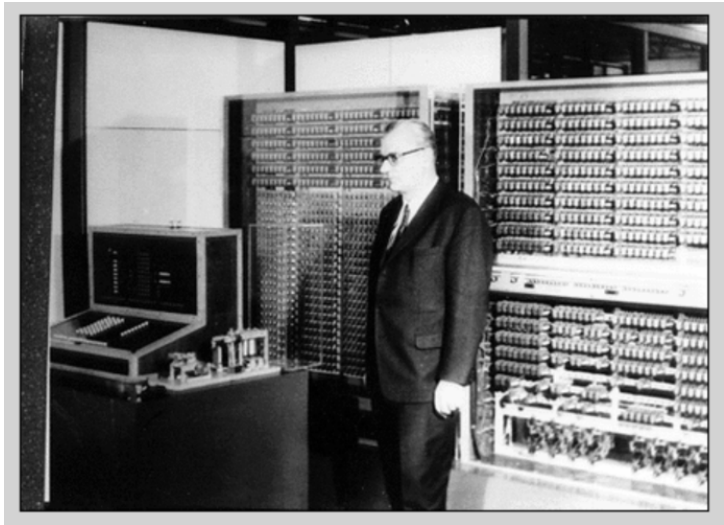


Figure 4.1. *The electromechanical calculator of Konrad Zuse (1941), 2,600 relays, 22 bit*

The invention of triode in 1906 and the development of the semiconductor transistor from 1947 led to the end of electromechanical technology for computing applications. Is this an opportunity to resurrect mechanical computing today? The recent development of nano-electrical mechanical systems (NEMS) for sensing applications proved it is possible to produce extremely small-sized components (comparable with scaled transistors) with a good reliability. However, it is necessary to demonstrate that this technology will be able to satisfy constraints of the electronic industry (speed, power dissipation and cost). Some interesting demonstrators have recently been implemented in Berkeley, Stanford and KAIST, but low-voltage operation and contact reliability issues appear very challenging.

4.2. Nanorelay principles

Logic operation is performed by the control of a movable structure. The switch comprises an actuation mechanism and a mechanical contact. Four mechanisms are investigated for actuation: the electrostatic actuation, the piezoelectrical actuation, the magnetic actuation and the thermal actuation.

4.2.1. *The electrostatic actuation*

The electrostatic actuation is the most popular since switch fabrication is simple and power performances are of interest. The principle is to use the attractive electrostatic force between two electrodes [POT 10]. Figure 4.2 describes the switching operations.

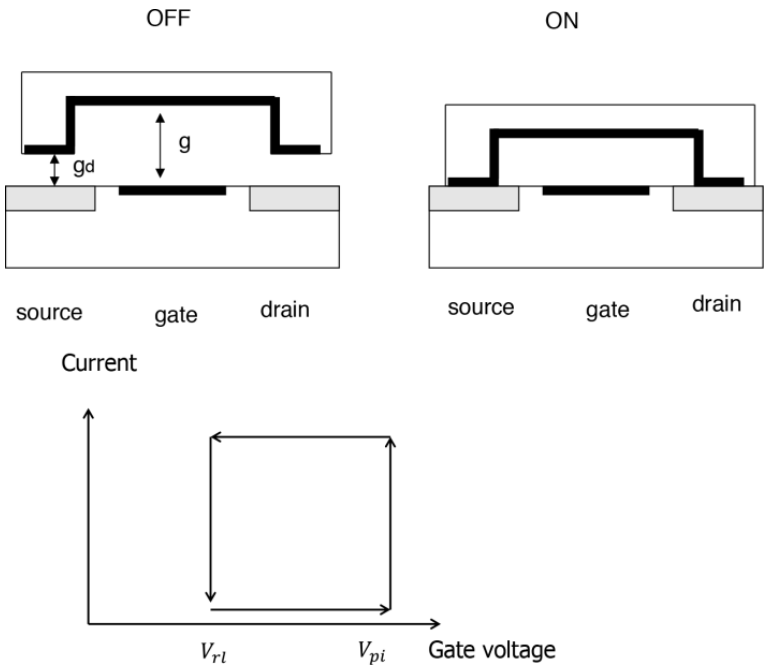


Figure 4.2. *Basic electrostatically mechanical switch*

The current flows from the source to the drain if the actuation voltage applied onto the gate is high enough to establish the mechanical contact between the movable beam and the gate. Figure 4.2 shows the variation of the current with the gate voltage. As the gate voltage is increased above the pull-in voltage Vpi, the contact is established and the current flows. As the gate voltage is decreased below the release voltage V_{rl}, the contact is broken and no current flows. This mechanism explains why the leakage current is negligible. The hysteretic behavior of the switch (the release voltage is lower than the pull-in voltage) is due to the surface adhesion force. It is

important to note the difference between the actuation gap *g* and the contact gap *gd*. The analysis given in section 4.3 will demonstrate that the optimal ratio between *g* and *gd* is 3/2.

Different switch architectures are studied: the three-terminal switch (3T) and the four-terminal switch (4T). The movable structure is a beam or a membrane and sometimes a second control electrode is used. Various designs have been reported: the actuated structure can move vertically or laterally and many contact materials have been investigated (gold, tungsten, titanium nitride, ruthenium and silicon carbide).

For system design considerations, it is generally more interesting to separate the actuation circuit and the conduction path.

4.2.2. *The piezoelectrical actuation*

The inverse piezoelectric effect is the deformation of a dielectric material upon application of an electrical field. The most popular materials are PZT, AlN and ZnO. PZT is the most efficient. Recently, feasibility of low-voltage piezoelectric microrelays has been demonstrated [ZAG 13]. Despite there only being a few researchers working with piezoelectric effect for nanorelay applications today, some theoretical considerations seem to prove the interest of this solution for low-voltage implementations [KLA 04].

4.2.3. *The magnetic actuation*

Researchers noted that interaction between ferromagnetic materials and actuators can be used for switch implementation. An alternative solution is to use the deformation of a thin film with the magnetostriction effect. However, magnetic actuators do not appear to provide a sufficiently energy-efficient technology compared to electrostatic and piezoelectric solutions.

4.2.4. *The thermal actuation*

Thermal actuators use different materials having different thermal expansion coefficients. Simplicity of fabrication made this solution attractive, but a large amount of power is necessary for actuation and this solution seems not compatible with electronic applications.

4.3. Electrostatic nanorelay modeling and optimization

We have to distinguish the dynamic modeling and the quasi-static modeling, generally used for circuit properties estimation.

4.3.1. *Dynamic modeling*

This section summarizes publications of Vitaly Leus and David Elata [LEU 08]. For simplicity we consider a simple parallel-plates structure. However analysis is difficult since equations are nonlinear.

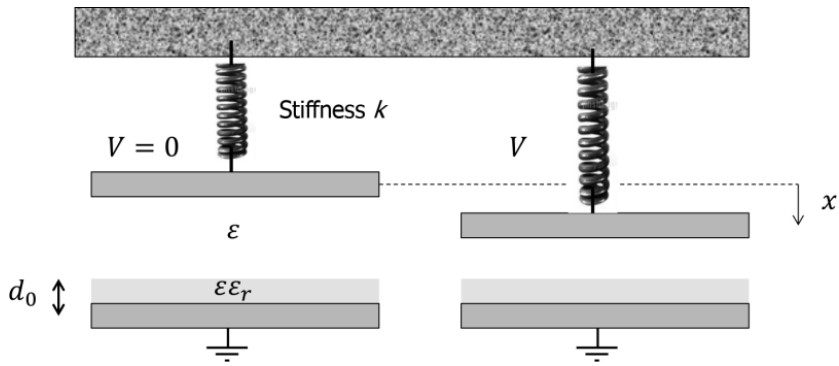


Figure 4.3. *The parallel-plate actuator*

It is necessary to introduce a thin-insulator layer into the model to avoid infinite capacitance, if electrodes were to be in contact. In practical switches, the difference between the actuation gap and the contact gap made this hypothesis unnecessary. The coefficient k is the stiffness of the movable structure and m and A are, respectively, the mass and the area of this structure. The parameter g is the gap without applied voltage V and $\mathcal{E}$ is the permittivity of free space.

The Hamiltonian of the system is given by

$$H = \frac{1}{2}m\dot{x}^2 + \frac{1}{2}kx^2 - \frac{\varepsilon A V^2}{2\left(\frac{d_0}{\varepsilon_r} + g - x\right)^2}$$

The three terms are the kinetic energy, the elastic potential and the electrostatic energy.

It is easy to introduce normalized variables defined by

$$\tilde{x} = \frac{x}{g} \quad \gamma = \frac{d_0}{g\varepsilon_\gamma} \quad \tilde{H} = \frac{H}{kg^2}$$

$$\tilde{V}^2 = \frac{\varepsilon A}{kg^3} \quad \tilde{t} = t\sqrt{\frac{k}{m}}$$

If damping is negligible, the Hamiltonian is unchanged and

$$\frac{1}{2}\tilde{x}^2 + \frac{1}{2}\tilde{x}^2 - \frac{1}{2}\frac{\tilde{x}}{(\gamma+1-\tilde{x})(\gamma+1)} = 0 \qquad [4.1]$$

The motion equation is

$$\tilde{x} = -\frac{\partial \tilde{H}}{\partial \tilde{x}} = -\tilde{x} + \frac{1}{2}\frac{\tilde{V}^2}{(\gamma+1-\tilde{x})^2}$$

If a step function voltage is applied, this equation can be integrated twice to find the position x.

Solution with $\gamma = 0$ is shown in Figure 4.4 depending on the voltage amplitude. The parameter *n* indicates the difference between the applied voltage and the dynamic pull-in voltage. Below a critical value $\tilde{V}_{Dpi}$ the dynamic response is periodic. For voltages above this critical value, the response is non-periodic and the movable electrode converges to an unstable equilibrium. This value is the dynamic pull-in voltage.

The voltage $\tilde{V}_{Dpi}$ is 0.5 when $\gamma = 0$.

If γ is different of 0, these critical values are

$$\tilde{V}_{Dpi} = \frac{1}{2}(1+\gamma)^{\frac{3}{2}} \qquad \tilde{x}_{Dpi} = \frac{1}{2}(1+\gamma)$$

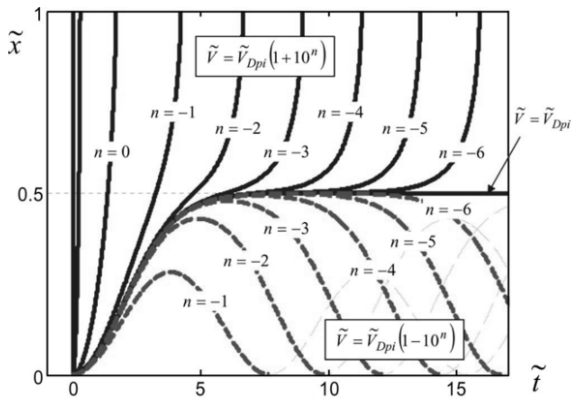


Figure 4.4. *The dynamic response of the electrostatic switch*

Equation [4.1] allows us to calculate the time when the stagnation state is reached for the first time for a periodic response.

$$\tilde{t}_s = \int_{\tilde{x}=0}^{\tilde{x}=\tilde{x}_s} \frac{d\tilde{x}}{\sqrt[2]{\frac{\tilde{x}\tilde{V}^2}{(\gamma+1-\tilde{x})(\gamma+1)} - \tilde{x}^2}}$$

For a non-periodic response, the switching time defined as the time for the first contact of the electrodes is given by

$$\tilde{t}_c = \int_{\tilde{x}=0}^{\tilde{x}=1} \frac{d\tilde{x}}{\sqrt[2]{\frac{\tilde{x}\tilde{V}^2}{(\gamma+1-\tilde{x})(\gamma+1)} - \tilde{x}^2}}$$

These relations can be simplified if the applied voltage is slightly below or above the dynamic pull-in voltage.

$$\tilde{V} = \tilde{V}_{Dpi}\left(1 \mp \delta\right)$$

$$\tilde{t}_s \approx \frac{\pi}{2} + \frac{3}{2}\ln(2) - \frac{1}{2}\ln(\delta)$$

$$\tilde{t}_s \approx 3\ln(2) - \ln(\delta)$$

These relations may be used for approximation of the switching time.

4.3.2. *Quasi-static modeling*

This analysis summarizes the published paper [KAM 11]: design, optimization and scaling of microelectromechanical (MEM) relays for ultra-low power digital logic. This analysis has been developed for the MEM switches designed in Berkeley, but many results are applicable for other devices.

The quasi-static analysis considers the forces being in equilibrium. During actuation, the spring force varies linearly with the displacement of the movable electrode while the electric force is inversely quadratic in gate displacement. The critical displacement at which the spring and the electrical forces are equal is one third of the gap g. If the total displacement gd is larger than this critical distance, the applied voltage causes the movable electrode to accelerate toward the contact electrode. It is easy to prove that the optimal applied voltage is larger than the static pull-in voltage defined by

$$V_{pi} = \sqrt[2]{\frac{8}{27}\frac{kg^3}{\varepsilon A}} \qquad [4.2]$$

where A is the actuation area and g is the actuation gap. The coefficient k is the stiffness of the spring.

For a beam (length L, width W and thickness h), it is possible to have an approximation of k

$$\frac{1}{k} \approx \left(\gamma_f \frac{EWh^3}{L^3}\right)^{-1} + \left(\gamma_t \frac{GWh^3}{L}\right)^{-1}$$

where γ_f and γ_t are, respectively, flexural and torsional constants ($3.7 \cdot 10^{10}$ m^{-2} and $1.3 \cdot 10^{10}$ m^{-2}), E is Young's modulus and G the shear modulus.

If F_A is the adhesion force (typically 0.1 μN), the V_{rl} voltage is

$$V_{rl} + \sqrt[2]{\frac{2(kg_d - F_A)(g - g_d)^2}{\varepsilon A}} \qquad [4.3]$$

For an NEMS-based circuit, energy and delay are traded off by adjusting all the design parameters: the voltage V_{dd}, the actuation gap *g*, the actuation area, the spring length *L*. This analysis considers the actuation gap g_d being given from technology constraints. It is clear that this parameter has to be chosen to be as low as possible in order to reduce the switching delay. The first step is to obtain analytical expressions for the relay delay and the dissipated energy in a commutation considering a chain of N relays actuated with N inputs at the same time.

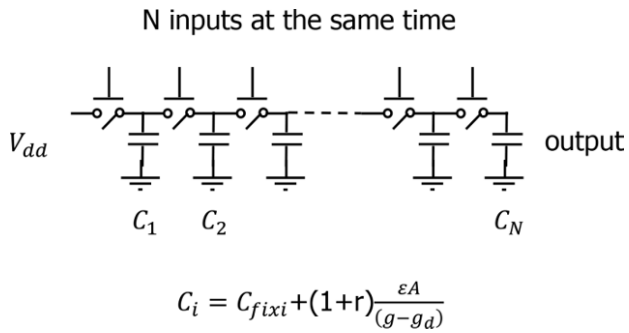


Figure 4.5. *optimization of a chain of N nanorelays*

The model considers the load capacitance as the sum of the relay capacitance $\frac{\varepsilon A}{(g-g_d)}(1+r)$ and the fixed Capacitance C_{fixi} of interconnection. The coefficient *r* indicates the input capacitance area is larger than the actuation area. Now we have to write the delay t_c and the dissipated energy E_d. An approximate expression of the delay is:

$$t_c = \sqrt[2]{\frac{m_2}{k}}\sqrt[2]{\frac{g_d}{g}}\frac{V_{pi}}{V_{dd}} \qquad [4.4]$$

An improved expression is

$$t_c = \delta\sqrt[2]{\frac{m}{k}}\left(\frac{g_d}{g}\right)^{\gamma}\left(\frac{V_{dd}}{V_{pi}}-\theta\right)^{-\beta} \qquad [4.5]$$

The constants δ, γ, θ and β are adjusted parameters depending on the quality factor of the movable electrode.

$$\delta \approx 2 \quad \gamma \approx 0.35 \quad \theta \approx 0.8 \quad \beta \approx 0.7$$

The dissipated energy depends on the value at the end of switching and of the average activity factor $\propto$.

$$\mathrm{E}=\sum_{i=1}^{i=N} \alpha \left(\frac{\varepsilon \mathrm{A}}{(g-g_d)}(1+r) \right) V_{dd}^2 \qquad [4.6]$$

The problem we have to solve is to minimize E for a given delay. The Lagrange optimization method allows us to write the following equations

$$\frac{\dfrac{\partial t_c}{\partial V_{dd}}}{\dfrac{\partial E}{\partial V_{dd}}} = \frac{\dfrac{\partial t_c}{\partial A}}{\dfrac{\partial E}{\partial A}} = \frac{\dfrac{\partial t_c}{\partial g}}{\dfrac{\partial E}{\partial g}} = \frac{\dfrac{\partial t_c}{\partial L}}{\dfrac{\partial E}{\partial L}} \qquad [4.7]$$

One other method should be to minimize the product delay-energy, but the universality of the Lagrangian method allows us to obtain interesting conclusions. Solving equations [4.7], we obtain g_{opt}

$$\frac{g_d}{g_{opt}} \cong \frac{2+3c_{norm}}{3+3c_{norm}}$$

where

$$C_{norm} = \frac{\dfrac{\sum C_{fixi}}{N(1+r)}}{\left(\dfrac{\in A}{g-g_d} \right)}$$

If the fixed capacitance is negligible, we simply obtain $\dfrac{g_d}{g_{opt}} \cong \dfrac{2}{3}$

We also obtain V_{ddopt}

$$\frac{\beta V_{ddopt}}{\left(V_{ddopt}-\theta V_{pi}\right)}=\frac{\left(2\gamma-1+\frac{1}{\sigma}-2\gamma\frac{g_d}{g_{opt}}\right)}{\left(2+\frac{1}{\sigma}-3\frac{g_d}{g_{opt}}\right)}\approx 1.2-1.3$$

where $\sigma=\frac{\left(\frac{k}{L}\right)}{\frac{dk}{dL}}$ is assumed constant roughly -1.4.

We obtain A_{opt} from C_{normopt} and the optimal size of the switch.

$$C_{normopt}=\frac{\sigma-1+V_{norm}}{\left(1-V_{norm}\right)\left(1-\sigma\right)}$$

where $V_{norm}=\frac{\beta V_{ddopt}}{\left(V_{ddopt}-\theta V_{pi}\right)}$

4.4. Technological challenges for NEMS computing

Two challenges are generally identified: low voltage operation in order to reduce the active power and the reliability of electrical contacts.

4.4.1. *Low voltage operation*

The analysis developed in the previous section has demonstrated that the optimal operating voltage is slightly larger than the pull-in voltage. The question is now to define conditions to get low pull-in voltages. Table 4.1 shows variation of the pull-in voltage with the length and the gap of the movable beam [DAD 11].

	Length (nm)	Gap(nm)	Thickness(nm)	Width(nm)
Node 100	1,000	100	100	100
Node 50	500	50	50	50
Node 25	250	25	25	25
Node 12	125	12	12	12
Node 6	60	6	6	6

Table 4.1. *Impact of scaling on the pull-in voltage*

	Length (nm)	Pull-in Voltage (V)
Node 100	1,000	25
Node 50	500	12
Node 25	250	5
Node 12	125	3
Node 6	60	1.5

Table 4.1. *Impact of scaling on the pull-in voltage* (*Continued)*

To overcome the need for high-voltage, researchers are attempting to reduce the physical dimensions of the devices. Relation [4.2] allows us to calculate the gap for scaled device operating below 1V. Actuation gaps around 10 nm are mandatory. Industrial processing techniques have not achieved this performance and the impact of scaling on other electrical properties is not perfectly known today. However, it is possible to predict an important increase of the contact resistance, a more important effect of the surface forces and a possible degradation of reliability. One of the most interesting results for low-power operation (0.5 V) has been published in *Nature Materials* in 2013 [LEE 13].

4.4.2. *Reliability of contact technology*

Surface forces play an important role in increasing the probability of failure. The first negative effect is the probability of "stiction". The movable part of the device is unable to return to the initial position, because capillary and Van der Waals forces are significant compared to elastic restoring force or applied reset electrostatic force. The second negative effect is the increase with the scaling of the contact resistance. Due to surface roughness, the contact is made at a finite number of points. When two asperities are in contact, they deform and form a circular contact. Some researchers consider each metal-to-metal contact spot as being described by a model combining the Maxwell resistance and the Sharvin resistance. Other researchers consider the conduction mechanism as being a tunnel effect through the thin oxide between the two metals. Table 4.2 [DAD 11] compares different metals in terms of conductance, reliability and useful lifetime.

To conclude, it seems difficult to have, simultaneously, a usable contact resistance (less than 1 MΩ) and an acceptable endurance. This trade-off is maybe the most important challenge for the future of NEMS-based computing technology.

	Hardness (GPa)	Resistivity (μΩ.cm)	Archard's wear constant (10–4)
Ag	1.5	1.6	2.2
Al	1.3	2.8	4
Au	1	2.2	5
Cu	1.3	1.7	1.5
Pt	5.4	10	0.2
Rh	10	4.3	0.03
Ru	15	7	0.01
Tt	2.8	40	2.5
W	4.1	5.3	0.4

Table 4.2. *Comparison of metal elements for switching application*

4.5. NEMS-based architectures

4.5.1. *Conventional architectures*

Due to the high switching delay, it is necessary to develop electronic architectures different of CMOS gate implementations. Conventional architectures are described in [POT 10] and give preliminary results for a 1 micron lithographic process (the gap is around 100 nm). The basic inverter is shown in Figure 4.6.

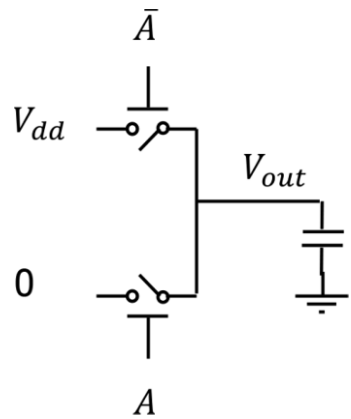


Figure 4.6. *The relay-based inverter*

Despite the relative low pull-in voltage, this gate is a low-frequency circuit, because the mechanical delay varies between 10 and 50 µs. If we use a scaled technology (90 nm-like) we can expect a mechanical delay between 20 and 100 ns. The imbalance between electrical and mechanical delays suggests that nanorelay-based circuits should be optimized by arranging many relays to switch simultaneously. Concerning energy performances, a benchmark between a CMOS Sklansky adder and an MEM relay adder indicates an advantage of a factor 10 for the relay technology [POT 10].

4.5.2. *Adiabatic architectures*

NEMS technology is interesting not only for ultra-low leakage properties, but also for active power reduction [FAN 11, HOU 13]. This is true if the adiabatic principle is used for logic gate implementation. Adiabatic logic circuits were introduced as a possible means to achieve ultra-low power circuits by taking advantage of the adiabatic charging principle (the adiabatic charging principle states that if the voltage in a circuit changes more slowly than the electric time constant of the circuit, then resistive losses are reduced). However, while the adiabatic charging principle affords a possibly unlimited energy–performance trade-off, the fact is that CMOS-based adiabatic circuits suffer from non-adiabatic residues and leakage loss components that deteriorate their performance. On the other hand, electrostatic nanoelectromechanical (NEM) switches have already been suggested and demonstrated for use in classical logic circuits. NEM switches offer the advantage of zero-leakage current and therefore zero static power dissipation, which is an appealing property for low-power-low-performance circuits. However, these switches require high operating voltages and suffer from low switching speeds when compared to metal-oxide-semiconductor field-effect transistors (MOSFETs). These factors constitute serious obstacles to replace CMOS circuits by NEMS relays for low-power solution. Nonetheless, NEM switches are ideal candidates to replace classical CMOS elements in adiabatic logic circuits, where the zero-leakage current experienced in NEM switches allows the efficient operation of NEM-based adiabatic logic circuits at low frequencies without any static dissipation penalties, and at the same time the use of adiabatic charging makes it possible to offset the high-energy dissipation that accompanies the voltages required to operate the nanoelectromechanical relays. For the first

time, in 2011, new NEM-based architectures were proposed for ultra-low power applications [FAN 11]. Figure 4.7 depicts a NEMS-based adiabatic inverter.

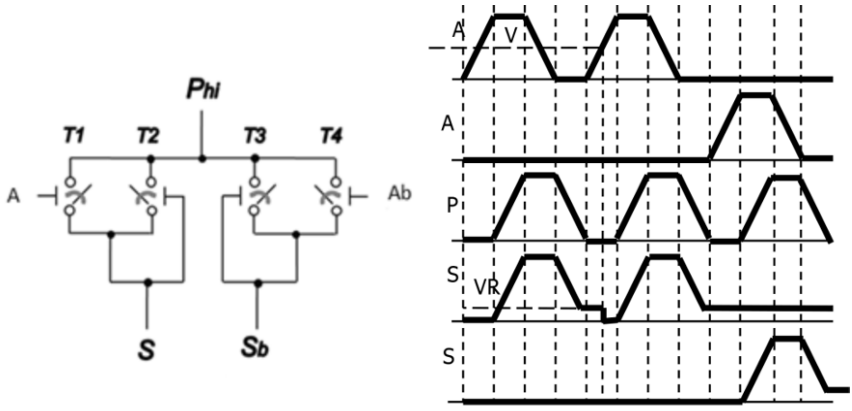


Figure 4.7. *An adiabatic NEMS-based inverter*

It is very easy to calculate the energy dissipation of this gate during a period of 4T (*T* is the duration of the ramp, *C* is the capacitance at the output node and *R* is the resistance of the switch in conductive mode), in the following form:

$$E = 2\frac{RC}{T}C \cdot Vdd^2 + \frac{1}{2}C \cdot V_{RL}^2$$

In Figure 4.7, the supplementary non-adiabatic dissipation appears when the output *S* is in reset. It abruptly switches from VRL to 0. Contrarily to the CMOS solution, it is now possible to reduce the non-adiabatic dissipation $C \cdot V_{RL}^2$ by lowering the release voltage V_{RL} of the nanorelay without negative impact on the leakage current, because the leakage is negligible.

4.6. Conclusions

Considering leakage power aspects and active power dissipation, NEMS-based technology may be considered as a long-term solution for ultra-low

power electronics. However, serious technological challenges have to be overcome in order to obtain simultaneously acceptable contact resistances and a reasonable reliability.

4.7. Bibliography

[DAD 11] DADGOUR H. *et al.*, "Impact of scaling on the performances and reliability of metal-contacts in NEMS devices", *Reliability Physics Symposium,* 2011.

[FAN 11] FANET H., Circuit logique à faible consommation et circuit intégré comportant au moins un tel circuit logique, Patent no 11 56670, 22nd July 2011.

[HOU 13] HOURI S., VALENTIAN A. FANET H., "Comparing CMOS-based and NEMS-based adiabatic logic circuits", *Lecture Notes in Computer Science*, vol. 7948, pp. 36–45, 2013.

[KAM 11] KAM H., *et al.*, "Design, optimization and scaling of MEM relays for ultra-low power digital logic", *IEEE Transactions on Electron Devices*, vol. 58, no. 1, January 2011.

[KLA 04] KLAASSE G., *et al.*, "Piezoelectric versus electrostatic actuation for a capacitive RF-MEMS switch", *2004 Conference on MEMS, MOEMS and Micromachining*, Strasbourg, France, April 29–30, 2004.

[LEE 13] LEE J.O., *et al.*, *Nature Nanotechnology*, vol. 8, pp. 36–40, 2013.

[LEU 08] LEUS V., ELATA D., "On the dynamic response of electrostatic MEMS switches", *Journal of Microelectromechanical Systems*, vol. 17, no. 1, February 2008

[POT 10] POTT V., *et al.*, *Proceedings of the IEEE*, vol. 98, no. 12, December 2010.

[ZAG 13] ZAGHLOUL U., PIAZZA G., "10–25 nm Piezoelectric nano-actuators and NEMS switches for millivolt computational logic", *International Conference on MEMS 2013*, Taipei, January 20–24, 2013.

List of Authors

Francis BALESTRA
IMEP-LAHC/Sinano Institute
(Grenoble INP-Minatec/CNRS)
Grenoble
France

Kathy BOUCART
Ecole Polytechnique Fédérale de
Lausanne
Switzerland

Sylvain BARRAUD
CEA-LETI
Grenoble
France

Mikaël CASSÉ
CEA-LETI
Grenoble
France

Hervé FANET
CEA-LETI
Grenoble
France

Zheng FANG
IME/A*STAR Singapore
Singapore

Gérard GHIBAUDO
CNRS/IMEP-LAHC
Grenoble
France

Adrian M. IONESCU
Nanolab
Ecole Polytechnique Fédérale de
Lausanne
Switzerland

Dim-Lee KWONG
IME/A*STAR Singapore
Singapore

Max C. LEMME
Department of Electrical Engineering
and Computer Science
University of Siegen
Germany

Guo Qiang LO
IME/A*STAR
Singapore

Marco PALA
CNRS/IMEP-LAHC
Grenoble
France

Beyond-CMOS Nanodevices 2, First Edition. Edited by Francis Balestra.

Alexandru RUSU
Ecole Polytechnique Fédérale de Lausanne
Switzerland

Giovanni SALVATORE
Swiss Federal Institute of Technology
Zurich
Switzerland

Xin Peng WANG
IME/A*STAR Singapore
Singapore

Index

Beyond-CMOS Nanodevices 2, First Edition. Edited by Francis Balestra.