Advances in electrothermal simulation of solid-state devices and circuits using commercial CAD tools

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Abstract
This contribution presents the new capabilities of a recently developed simulation tool devoted to the electrothermal analysis of solid-state devices and circuits. The code exploits an effective analytical approach to describe the 3-D thermal process and is based on a commercial circuit simulator to consistently solve the electrical and thermal networks. The proposed versions rely on a more effective strategy to automatically build the electrothermal schematic starting from the original circuit. Moreover, additional device models provided with thermal node have been made available. Finally, transient analyses are allowed through the construction of equivalent RC networks.

1. Introduction

Nowadays, due to the technology trends directed toward enhanced integration capability and higher speed, solid-state multifinger transistors [1] as well as integrated analog circuits [2] are increasingly affected by electrothermal effects. As a consequence, various electrothermal simulation programs have been developed to optimize the device/circuit design in order to achieve an improved thermal ruggedness. Conveniently, some tools adopted in the IC CAD arena, e.g., ADS from Agilent [3], present newly developed BJT/HBT models provided with an additional terminal, namely, a thermal node, and include a default value for the self-heating thermal resistance. In such programs, the temperature increase above ambient can be evaluated from the dissipated power and considered, in turn, as a supplementary input that modifies the temperature-dependent parameters. Therefore, the temperature actually represents a variable (*not* a parameter) that is computed during the simulation run and self-heating effects are accounted for. However, mutual thermal interactions between active devices integrated on the same chip are not described, which may lead to unavoidable simulation inaccuracy, especially when the heat generating regions are located in close proximity. Besides, other embedded active/passive components (as e.g., resistances, diodes, and FETs) are not equipped with a thermal node.

In order to overcome the aforementioned limitations, we have conceived and developed an electrothermal simulation tool based on the solving engine of the commercial software ADS. A first version of the code has been successfully adopted for analyzing the thermal behavior of multifinger GaAs HBTs as well as of basic analog electronics blocks [4].

Enhanced versions have been subsequently employed to investigate the thermal interactions in multicellular power BJTs [5] and identify the optimum layout of multifinger SiGe HBTs [6].
This communication is organized as follows. Some details about the tool, with particular emphasis on the added features, are given in Section 2. It is shown that a novel effective procedure is employed to automatically generate the circuit that accounts for the electrothermal feedback (EF). Besides, the approach adopted to enable transient analyses is discussed. Lastly, in Section 3, various simulation results are provided to illustrate the software capability. Conclusions are drawn in Section 4.

2. The tool

The program is subdivided into three basic blocks, i.e., a pre-processing routine, a main core, and a post-processing code (see Fig. 1).

The pre-processing stage involves two steps.

1. First, the self-heating and mutual thermal resistances are evaluated from the layout file associated to the circuit under analysis through the closed-form analytical formulations proposed in [7]. Such a process is fully automated. Moreover, the adoption of an analytical approach allows avoiding troublesome discretization issues that arise when dealing with numerical techniques. On the other hand, when analyzing domains characterized by complex geometries, in which an analytical description of the thermal process is difficult (or even impossible) to be obtained, the thermal resistance matrix can be directly provided by the user. In such cases, a preliminary numerical/experimental extraction of the thermal resistance values is required.
2. Second, an additional component including the thermal resistance matrix is generated and automatically connected to the active devices of the original ADS circuit. Such a block is treated by ADS as an embedded element and is exploited to handle the EF. In particular, it calculates the temperature increase above ambient of each device (treated as a voltage) starting from the powers dissipated by all components included in the circuit (reviewed as currents) during the electrothermal simulation run. A novel circuit accounting for the EF is therefore created, which can be solved by the main core via the native ADS engine.

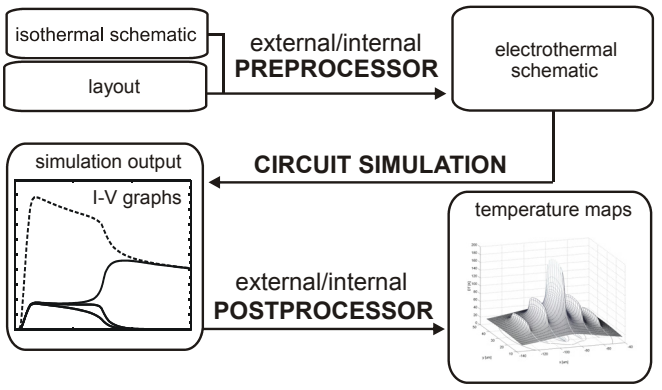

Fig. 1. Schematic *block diagram* of the proposed ADS-based electrothermal simulation tool.

Various features have been added with respect to the former program versions:

a. A novel straightforward strategy has been developed for creating the EF circuit, which can be described as follows. If the embedded transistor models equipped with a thermal node (i.e., Mextram 504, HiCUM, and VBIC) are present in the analyzed circuit, they are automatically replaced by new device instances (made available in the program libraries), which provide the dissipated power P_D at an additional output terminal, namely, a "dissipated power" node. The evaluation procedure of the dissipated power can be described as follows. As far as the standard thermal-node models are concerned, when the self-heating flag is enabled, the temperature increase above ambient is evaluated as the voltage drop across the "intrinsic" thermal resistance (treated as an electrical one) that conducts the dissipated power (treated as a current). As shown in Fig. 2, in the new instances, the internal thermal resistance is automatically deactivated (i.e., it is set to an open); this allows accessing the intrinsically evaluated dissipated power through a current-controlled current source (CCCS). As a consequence, the dissipated power is made available to become an input of the ET feedback block. It is noteworthy that in former program versions the dissipated power of each transistor was evaluated as the product $I_C \cdot V_{CE}$ [4], [6], which limits the program applicability to circuits operated under dc conditions.

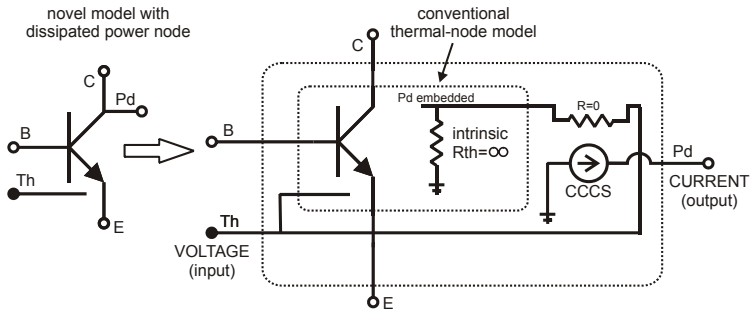

Fig. 2. Representation of the novel embedded transistor model with thermal node and equipped with a circuit for providing the dissipated power as an output. The temperature increase above ambient is calculated by the EF block (see Fig. 3) and provided to the transistor as an input.

b. The whole pre-processing stage is typically demanded to an external code. This solution allows for high flexibility when applied to other commercial circuit simulators (as e.g., ELDO, SABER, and SPICE). In addition, a novel program version has been developed, in which the pre-processing routine – written in Application Extension Language (AEL) – is completely embedded within the ADS environment. This eliminates the need for an additional external code and results in increased manageability and speed. However, such a version can be only used on ADS-based platforms.

c. Various strategies for generating the EF block have been pursued, such as the Verilog-A behavioral language [4], [6], which well lends itself to the analytical description of components, and Symbolically Defined Devices (SDD) [5], which are ADS-embedded multi-port elements, whose current/voltages inputs and outputs (and their derivatives) can be suitably related by user-defined equations. In addition, it is also possible to resort to networks employing only standard SPICE components. It is

noteworthy that, due to the introduction of the novel device models, such a block is not required to evaluate the dissipated power any longer as in previous software versions [4], [6]. Lastly, the EF block allows accounting for nonlinear thermal effects through the Kirchhoff transform.

d. The new pre-processor versions allow enabling transient analyses as follows. First, starting from the layout file, the actual thermal impedances are numerically evaluated as a function of time according to the approach described in [8]. Subsequently, an external routine is adopted to synthesize a lumped thermal network suitable to accurately describe the thermal impedance behavior vs. time. Finally, the attained thermal network is automatically included into the EF block. Currently, algorithms are sought to suitably reduce the component count of the thermal equivalent circuit without affecting the simulation accuracy.

e. Besides the enriched versions of the embedded thermal-node transistor models, other custom dc electrothermal models for active/passive components (e.g., resistances, diodes, power and conventional MOS, BJTs, and HBTs) have been conceived, developed, and made available in the library. To this purpose, both the Verilog-A and SDD approaches have been employed.

The resulting electrothermal schematic where the new devices (i.e., those with dissipated-power node) and the EF component lie (see Fig. 3, where a 5-finger bipolar transistor is represented) is then solved by the main core via the native ADS engine in order to exploit its fast and robust convergence algorithms.

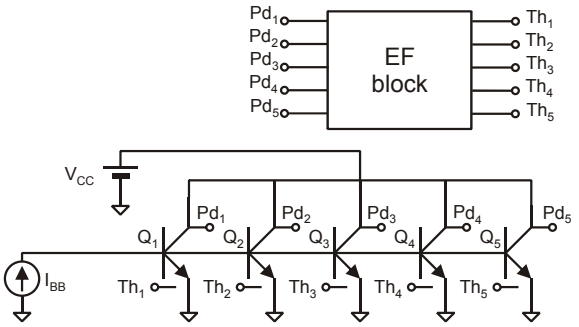

Fig. 3. Electrothermal schematic of a 5-finger bipolar transistor. Every finger is described through the new instances. The block handling the electrothermal feedback is also shown.

Lastly, a post-processing code (either external or embedded by AEL) is adopted for handling the simulation results (e.g., storing data in files) and for evaluating the temperature maps under assigned bias conditions over a chosen grid.

The possible future improvements can be summarized as follows:

- Novel analytical thermal models are being developed to seamlessly evaluate the thermal resistances associated to complex domains (e.g., trenched devices, SOI structures). Such models will be shortly available in the pre-processing routine.
- The effects of package and surface metallizations will be empirically included by introducing related thermal resistances.

3. Simulation results

As a first application, the behavior of a GaAs-based HBT was analyzed. The structure is composed by 3 individual sub-transistors characterized by a horseshoe shaped InGaP emitter with a GaAs/InGaAs contact and area amounting to 56 μm^2. The self-heating and mutual thermal resistances were preventively evaluated through both numerical FEM simulations and dc measurement techniques. The obtained values – which were found to be almost identical – were subsequently included into the EF component. The transistor model parameters were calibrated on the basis of isothermal measurements of I–V characteristics performed at various thermo-chuck temperatures. As can be seen in Fig. 4, excellent agreement is obtained between experimental and simulated results: both the negative differential resistance (NDR) region and the unwanted *collapse of current gain* are accurately described by the tool.

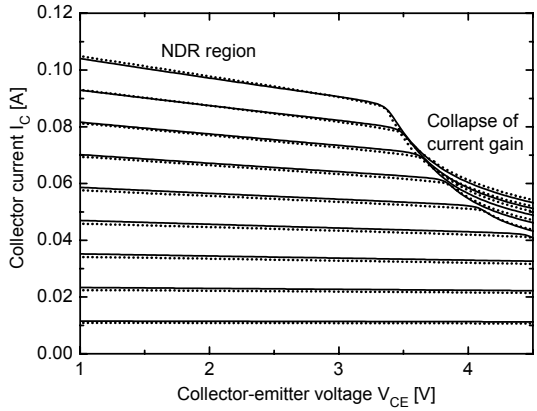

Fig. 4. Nonisothermal output characteristics of a GaAs-based 3-emitter HBT: comparison between simulated (solid lines) and experimental (dotted) results. The base current I_B spans from 0.1 to 0.9 mA.

Afterward, a different GaAs-based HBT composed of 3 sub-transistors, each of them provided with 2 rectangular 2×14 μm^2 emitters, was thoroughly analyzed. The spacing between the centers of the individual sub-transistors is equal to 72 μm. In this case, the thermal resistance matrix was automatically evaluated from the layout. The nonisothermal I_C–V_{CE} characteristic at $I_B = 1.8$ mA was simulated by the proposed tool (see inset in Fig. 5a). Figs. 5a and 5b detail the temperature field over the top surface of the device under test for $V_{CE} = 1.20$ V (point A in the inset) and 3.75 V (point B), respectively. As can be seen, for $V_{CE} = 1.20$ V, the temperature distribution is rather uniform (i.e., the peak values over the single sub-transistors are approximately identical), while being noticeably uneven for $V_{CE} = 3.75$ V, that is, beyond the occurrence of the collapse of current gain.
The beneficial effect of an increased thermal coupling between sub-transistors as well as of ballasting emitter resistors was then investigated through nonisothermal simulations. Fig. 6 plainly shows that reducing the spacing between sub-transistors centers moves the onset locus of the collapse to the right, which results in an enhanced thermal ruggedness. In a similar fashion, Fig. 7 illustrates that the safe operating area of the HBT under analysis markedly enlarges by connecting identical ballasting resistors to the emitters of the 3 sub-transistors.

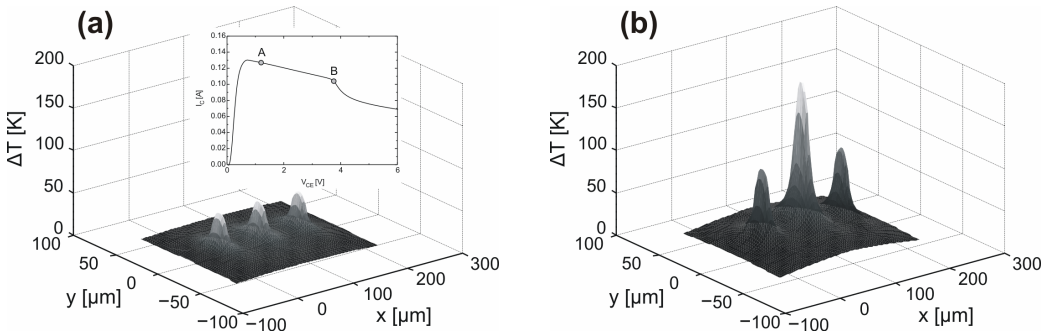

Fig. 5. Top surface temperature fields as obtained by the ADS-based code for a GaAs HBT composed of 3 sub-transistors at V_{CE} = 1.20 V (a) and 3.75 V (b).

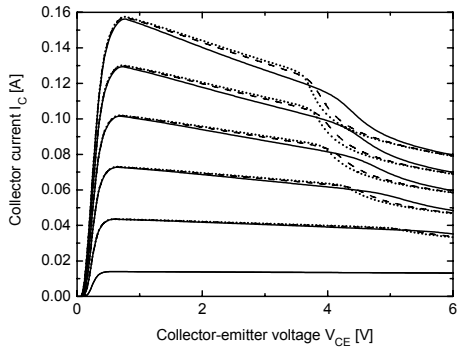

Fig. 6. Nonisothermal I_C–V_{CE} characteristics at various I_B values as obtained by the ADS-based code for different distances between the centers of the individual transistors, i.e., 24 μm (solid lines), 48 μm (dashed), and 72 μm (dotted).

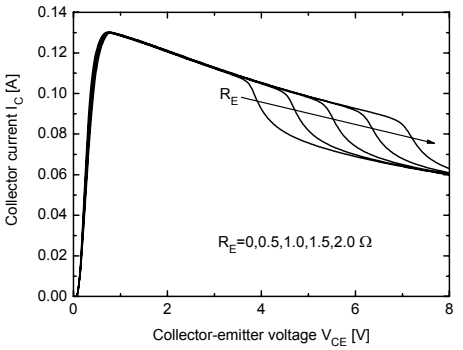

Fig. 7. Nonisothermal I_C–V_{CE} characteristic at I_B = 1.8 mA for various ballasting (identical) resistors tied to the emitters of the sub-transistors.

The proposed code has also allowed for an extensive electrothermal analysis of some basic analog building blocks, such as current mirrors and differential pairs.

Fig. 8 shows the simulated output current vs. voltage of a current mirror fabricated in a bipolar silicon-on-glass technology [9] for various mutual thermal resistances between reference transistor Q_1 and output transistor Q_2. It can be plainly observed that (1) a thermal instability occurs, which manifests itself as a *flyback* behavior under current-controlled conditions; (2) the flyback locus moves to the right by increasing the thermal coupling between devices Q_1 and Q_2, i.e., by reducing the spacing between them.

Fig. 9 depicts the simulated collector current of transistor Q_1 vs. input voltage V_{IN} in a differential pair as obtained by sweeping V_{IN} from negative to positive values for various supply voltages. As theoretically explained in [10], differential pairs may exhibit a thermally-induced instability phenomenon, which results in a distortion in the I–V characteristics with respect to the *classical* expected behavior (dashed line) under isothermal (at T = 300 K) conditions. An inspection of the nonisothermal curves (solid lines) clarifies that such a distortion enhances (i.e., transistor Q_1 turns on with growing voltage delay) by increasing V_{CC}, which strengthens the EF.

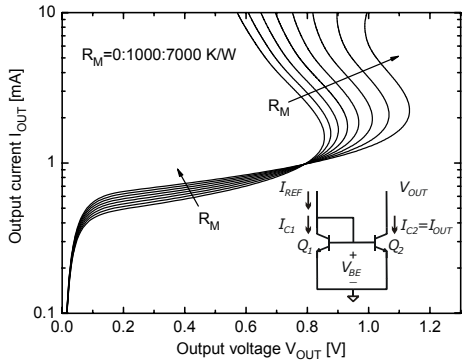

Fig. 8. Nonisothermal output current I_{OUT} vs. voltage V_{OUT} curves for various mutual thermal resistances between the individual transistors Q_1 and Q_2. The reference current I_{REF} is equal to 1.0 mA. The self-heating thermal resistance of the single devices amounts to 17500 K/W. The current mirror scheme is reported in the inset.

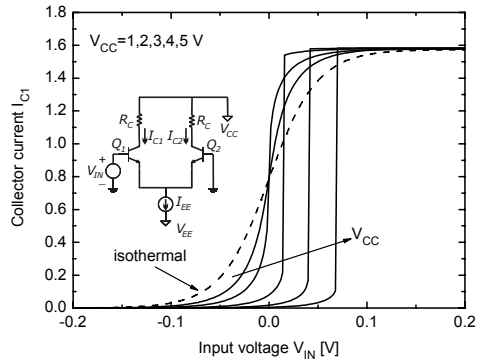

Fig. 9**.** Nonisothermal collector current I_{C1} vs. input voltage V_{IN} for various values of supply voltage V_{CC} (solid lines). Also represented is the isothermal at T = 300 K curve (dashed). The self-heating thermal resistance of the individual transistors and the mutual resistance between them are equal to 17500 and 2000 K/W, respectively; I_{EE} = 1.6 mA, R_C = 120 Ω. The differential pair scheme is reported in the inset.

Finally, a transient analysis has been performed on an individual GaAs HBT biased at I_B =0.6 mA by applying a V_{CE} = 2 V step at t = 0. At the early transient stage, the device works at ambient temperature (point 1 in Fig. 10a), and then moves to the steady-state condition (point 2). The evolution of both current and temperature is shown in Fig. 10b. As can be seen, the current reduces with increasing temperature due to the negative temperature coefficient of the current gain.

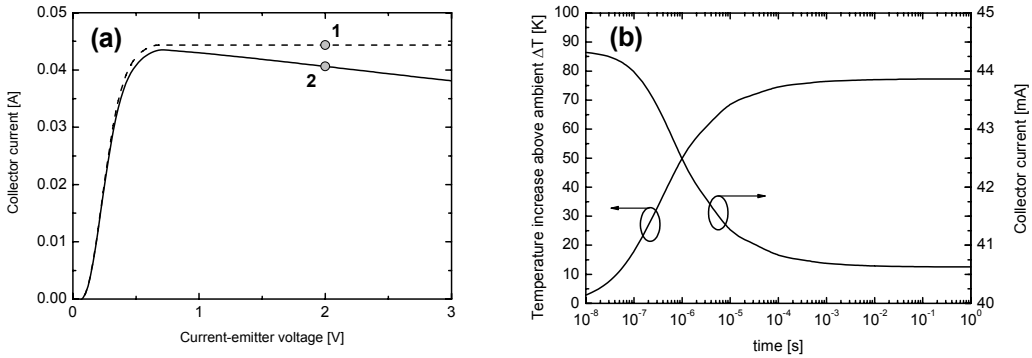

Fig. 10. Isothermal (at T = 300 K) (dashed line) and steady-state nonisothermal (solid) output characteristics for a single-finger HBT at I_B = 0.6 mA. The transient analysis is performed by applying a V_{CE} = 2 V step at t = 0, so that the operating point moves from point 1 to point 2 (a). Temperature increase over ambient and collector current vs. time (b).

4. Conclusions

We have discussed some novel features implemented in an electrothermal simulation tool based on the fully automated employment of the commercial circuit simulator ADS. The new program versions exploit an elegant and effective procedure to create the electrothermal schematic starting from the standard circuit, which also allows extending the software applicability to ac and transient simulations. New custom dc electrothermal models have been developed and made available in the program libraries. Transient analyses are enabled through the adoption of thermal equivalent RC networks, which are properly determined at the pre-processing stage. It has been shown that the proposed simulation strategy can be successfully applied to the design optimization of multicellular/multifinger transistors as well as of integrated analog circuits.

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