ON Semiconductor

Compte Rendu de la réunion du Comité d'Entreprise du 23 mars 2015

La composition de l'assemblée était la suivante :

Représentants de la Direction	
Yolande De Busschop, Présidente	Sophie Baquié, Administration Ressources Humaines
Carolina De Landsheer, Directrice des Ressources Humaines EMEA	Pascal Aigouy, Collaborateur de la Présidente (excusé)
Bertrand Clou, Design center manager	Joël Turchi, Ingénieur d'applications PG
Représentants du Personnel	
Titulaires	**Suppléants**
Bernard Clarysse, Trésorier	Aurore Weiss, Trésorier adjoint
Carl Van Baelen	Fabien Foulon
Olivier Martinez, Secrétaire	Philippe Andre
Pascal Tournier, Secrétaire adjoint (excusé)	Thierry Sutto
Thierry Viard	Julie Athanassiadis
Délégués Syndicaux	
Bernard Clarysse, CFE-CGC	Myriam Combes, CFDT

Ordre du jour :

1- Approbation du compte-rendu de la réunion du CE du 26 mars 2015
2- Politique de recherche et développement de l'entreprise – Information et Consultation
3- Recours aux conventions de forfait modalités de suivi de la charge de travail - information et consultation

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Approbation du compte-rendu de la réunion du CE du 26 février 2015

Le compte-rendu est approuvé à l'unanimité.

Politique de recherche et développement technologique de l'entreprise – Information et consultation

Bertrand C. présente les activités design et test de la BU PI.

2014 a été marqué par des améliorations techniques concernant les dc-dc et les PMICs. De nouvelles architectures ont été développées :

- IP Buck avec architecture ACOT.
- IP Boost avec 1 brevet déposé.
- IP Buck Boost avec 2 brevet déposés.

Concernant les PMICs, une progression a été faite avec le développement du SCY6992 (gestion de la charge sans fil des téléphones, tablettes, …). C'est le plus gros produit développé depuis le début par le centre de design de Toulouse. On est en avance de phase sur le marché avec ce produit. De plus Qualcomm a fait une annonce sur le marché officialisant le partenariat avec ON Semiconductor concernant le « wireless charging ».

Concernant la technologie, un partenariat se met en place avec Tower. Le NCP3901 (premier produit développé dans cette technologie) a été reçu et les premiers retours du client sont positifs.

Suite à une question du CE concernant le partage des produits entre Gresham et Tower, Bertrand Clou répond que les produits dits « haute tension » dans le marché du portable seront fabriqués chez Tower.. La fabrication des autres produits standards 5V devrait se poursuivre à Gresham.

Concernant l'équipe test et l'amélioration de la testabilité de nos produits, une équipe comprenant des ingénieurs test, des ingénieurs de conception et des ingénieurs de caractérisation a été mise en place pour revoir et améliorer les méthodes de test des régulateurs à découpage. Ce travail de recherche et de développement de nouvelles techniques est toujours en cours.

Le centre de design de Toulouse développe aussi des chargeurs de batterie pour la BU PI. Cette activité va être renforcée pour comprendre 3 ingénieurs de conception. Il faudrait aussi plus d'ingénieurs d'application lors de l'évaluation de ces produits.

Concernant les IP développées en avance de phase, l'impact sur le test des produits dérivés de ces IP et la disponibilité des ressources de test doit être anticipé. La nouvelle

organisation des équipes design et test devrait accélérer la qualification des nouvelles IP.

Les objectifs du centre de design sont d'être un centre de design d'excellence en power management et d'être un centre de design de référence en power interface. Actuellement nous sommes au niveau de la compétition voire mieux sur le premier point, mais en retard sur le second.

Concernant le nouveau marché du wearable, l'objectif actuel est de faire un test chip avec les blocs faible courant de consommation correspondant. On va aussi s'appuyer sur notre partenariat avec Qualcomm pour définir un chargeur de batterie pour ce marché « wearable ».

3 produits importants doivent être finalisés cette année pour améliorer nos ventes : NCP6356B, NCP6868 et NCP6878. Il faut aussi finaliser le NCP1871 et reprendre le NCP1864.

La stratégie de test est liée au SCY6992. Une évaluation comparative de nouveaux testeurs est en cours au niveau de la corporation (ETS 800 vs Teradyne MicroFlex vs Advantest T2000). Les produits sont de plus en plus gros et nécessitent des testeurs avec davantage de ressources.

Les élus font aussi remarquer l'inadéquation des ressources de l'équipe application en comparaison de la complexité grandissante des produits que l'on doit développer, et du support grandissant demandé par les clients.

Joël Turchi, en l'absence de Christophe Basso, nous présente les activités R&D de l'équipe application PG à Toulouse.

Après nous avoir présenté l'équipe et l'organigramme de la business unit PG, Joël souligne que l'activité de ce service est tirée par l'initiative « green power » qui vise à réduire le plus possible la consommation d'énergie en veille des équipements, l'amélioration de la régulation primaire avec la suppression de l'opto-coupleur qui permet de réduire le coût de la solution finale, et la résolution de problèmes analytiques. L'équipe se positionne aussi sur le marché de l'éclairage à LED.

Le CE demande quelle est la projection de l'équipe application PG à Toulouse pour les 5 ans avenir ? (développement de l'activité et croissance de l'équipe en ligne avec la stratégie de la BU PG). Christophe Basso répondra à cette question lors du prochain CE.

L'avis du CE concernant la politique de recherche et développement sera rendu lors du prochain CE.

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Recours aux conventions de forfait modalités de suivi de la charge de travail - information et consultation

La présentation est disponible en annexe.
Sophie Baquié rappelle les règles du forfait jours et des modalités de suivi de la charge de travail. Un entretien doit avoir lieu en milieu d'année entre le salarié et le manager. Un rappel va être fait aux managers car celui-ci doit être séparé de l'entretien de début d'année sur les performances du salarié.

A l'unanimité le CE rend un avis favorable.

Toulouse le 26 mars 2015,

Yolande De Busschop — Présidente

Olivier Martinez — Secrétaire

ON Semiconductor®

Tlse Design Team Goals 2015

Content

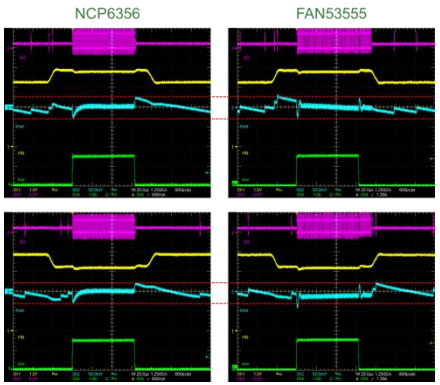
- 2014 Highlights & Lowlights
- 2015 Goals headlines
- Test Strategy for PI

Back to 2014 Performance …

Design Highlights

New DCDC converter architectures

- Several outstanding innovations in Buck Boost field
  - Hyst Boost topology combining ripple & error amp (D. Romeo).
  - Ripple based control Buck-Boost architecture (D. Romeo).
  - Negative charge-pump over driving non switching power Fets, in Buck or Boost architecture (B. Le Men, S. Ramond).
- New ACOT with ripple emulator Buck IP enabling equivalent or slightly better performances than FAN53555!
- Start extend ACOT architecture to new applications
  - Multi-phase for high power hungry ARM processors.
  - Wearable applications to compete with ultra low Iq TI part

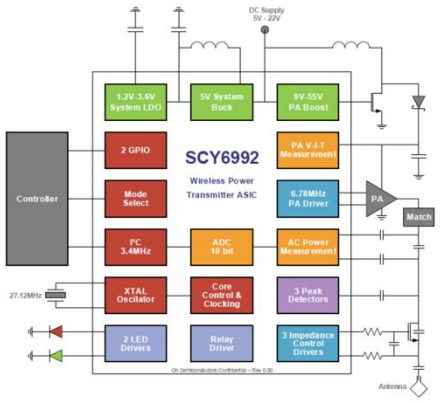


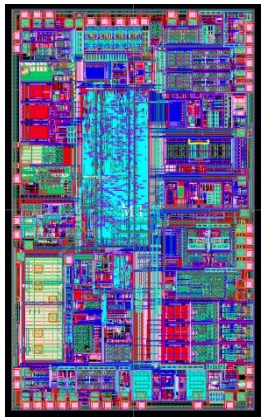
Line and Load Transient vs FAN53555 0.01A to 1.5A


Ripple based control Buck-Boost architecture

High integrated Power Management IC

- SCY6992 is the biggest mixed signal integrated circuit done by the team so far!
  - Die size = 7.92mm2
  - ~200.000 devices & ~1300 nets @ top level
  - Digital content: 11.5kGates (0.84mm²)
  - ~130 top verification benches as compare to 30 for usual mini PMIC.
- New step to prove BU ability to develop complex integrated power management ICs.
- Increase our IPs portfolio: crystal oscillator, AC power measurement, Peak detector ...



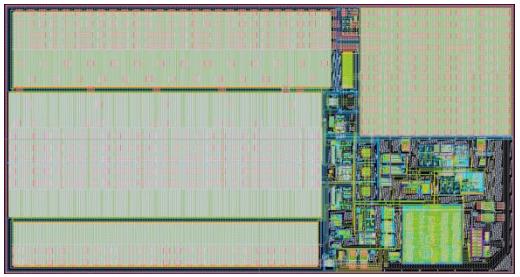


Other Technical Highlights

Very Good Progress on TOWER technology

- Tower process enables improvement of HV products (thx to low Ron & scalable power devices) => suitable for SBC &OVP ICs
  - NCP3901: power stage is 3.1mm2 vs 7.0mm2 in ONC25 with 30V devices. **It's more than half the power size saved!**
  - NCP392 product cost is 20% lower (7,5 cents vs 9 in ONC25BCD)
- Technical Training done by Julien to guide team using this process
- New rules to reduce space between WTN and substrate contact
- Design flow validated on NCP1864, NCP6904 & NCP3901
- Now need to confirm technology performance with silicon.
- Should also help fix Gresham capacity limitation.

► Just received 1st NCP3901 silicon & got positive feedback from Qualcomm

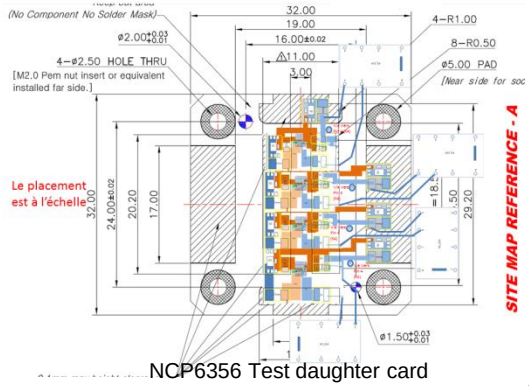


NCP3901: CSP 4x7- 1.65x3.1mm

Great team work on Manufacturing Test of DCDCs & PMICs

- Refund test hardware & method to satisfy all the manufacturing constraints & critical aspects of new DCDC IPs: timely measure of IC Iq & leakage current; multi site & close loop test to optimize test time & coverage, while controlling PCB noise & spikes
- Cross functional team: Patrick, Stephane, Boris, Mickael, (test), Aude, Serge (Cz) Henrique, Dominique (Design).

► Not yet closed … To be continued …



NCP6356 Test daughter card

Team Highlights

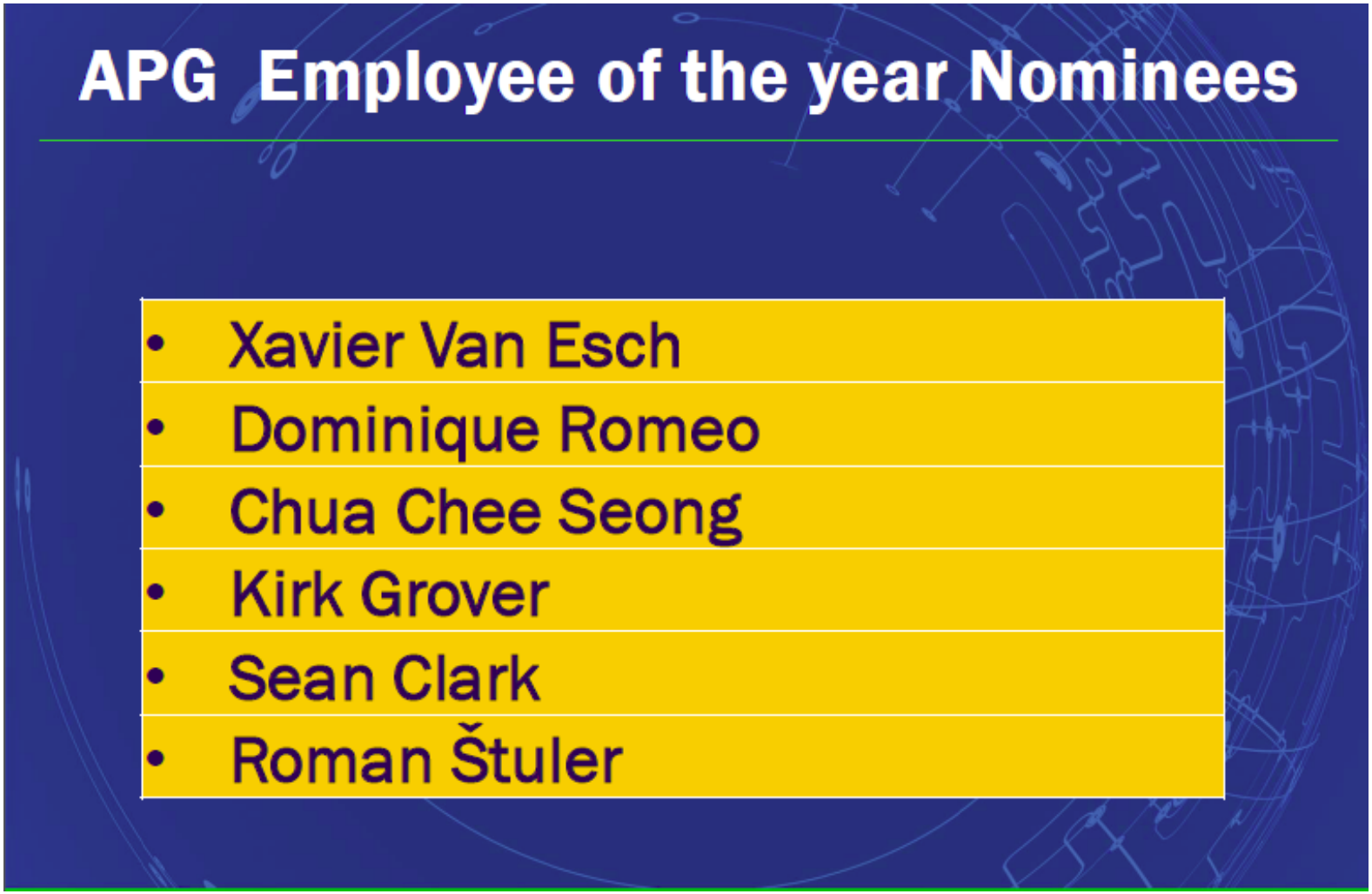
Sucessful rotations inside BU Team

- Julie A. (Characterization engineering).
- Anissa K. (Analog Design).

Perfect integration of new employees

- Boris D. (Test engineering).
- Marion D. (Physical Design).
- Amokrane M (PhD Buck-Boost).
- Emile M. (Physical Design).
- Jonathan M. (Digital Design).

Employee of the Year Nominee



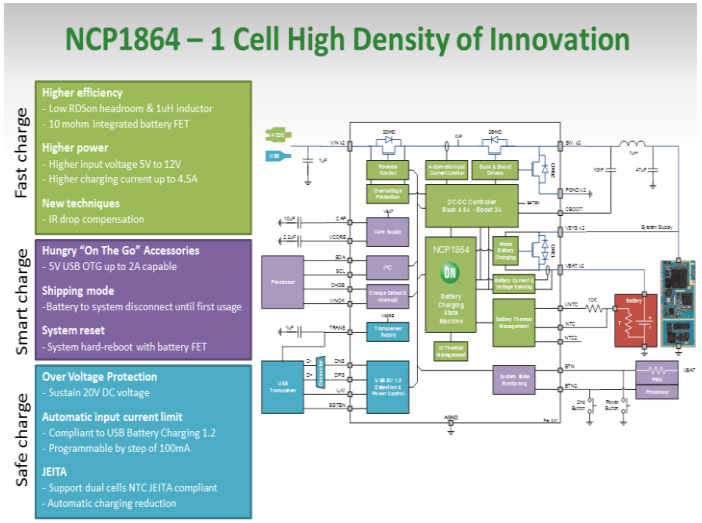
Execution Lowlights

Switching Battery Charger

- NCP1871 not qualified in 2014 as initially targeted.
- NCP1864 (Austin): 6 month delay on the TO plan!

► These are certainly our most complex ICs, so …
- Re-enforce team with 3 designers
- Take all lessons learned from previous projects, to improve overall execution from Definition, Design, Evaluation … to Qualification.

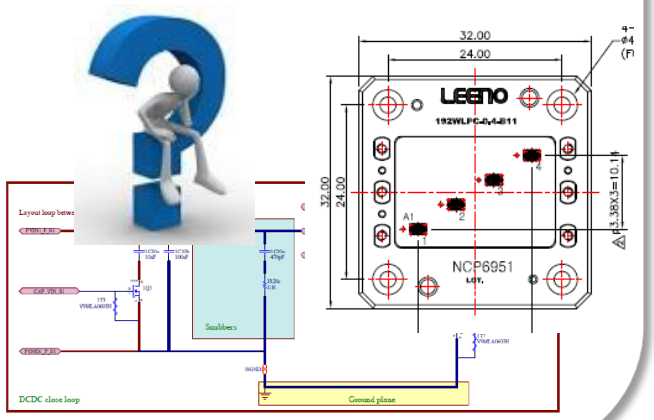
► Good basis for roadmaps: dual inputs SBC



Advance development is not a design matter only

- All new advanced development should be anticipated as well on test engineering side (ex: NCP6868, NCP6951)
- Also on SCY6992 project with several new IPs (crystal oscillator, AC power measurement, Peak detector …) it is mandatory to anticipate test resources early in development process.

► Better design/test team organization & additional test resources will help accelerate new IP qualification.



Business Highlights

Bz success on ARM core Bucks with Qualcomm references design

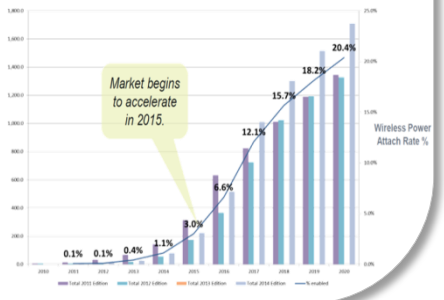
- **NCP6335:** total sales is 11M$ in one year!
- **NCP6343:** NCP6343 is a high volume new product that is ramping up
- Expect Story to continue with **NCP6336/6336B** and then **NCP6353 …**

Switching Battery Chargers

- NCP185x revenues represented more than 5M$ in 2013.
- The NCP1854 is now released and approved at several Chinese manufacturers
- NCP1855 is going to be promoted.
- **NCP1864** will consolidate our position at MTK.
- New IPs as Flash, Fuel Gauge or rectifier will open new opportunities

Prepare road for success after 2015 with Wireless charging

- Receiver solutions: **SCY1751** and **NCP3901**
- Power Transmitter solution: **SCY6692** (power, measurements & control IC)
- Opportunities to extend design outside Qualcomm: NCP3901 @ MTK
- Need to propose general market devices

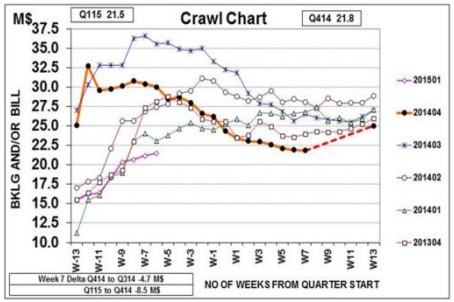


Business Lowlights

Year Business results are below expectations

- Meet $103.5M of revenues, which is under the 112M$ targeted.
- Samsung business falls from about 20%
- Q4 has been very difficult (@ $22M). It is our lowest quarter since Q1 2013.

► Focus on selling what we have and promiting what we are going to release on the short term: NCP6868/78, NCP6353, NCP3901 etc



Computing Market

- Load switch not yet largely adopted by the market except the 451A @ Stringer.
- No contact anymore with Intel for NVDC Battery Charger and no real traction on the market (especially in Taiwan).

PMIC : Difficulties to find the perfect fit to engage outside Qualcomm

- The 2015 Kinect program on which the SCY6941 was supposed to be used has been stopped.
- NCP6904: Stringer decided not to proceed but may come back with silicon?
- Samsung/LG: No design in with NCP6915 & NCP6915B
- Got several opportunities that were not suitable: planning, system knowledge

2015 Goals Headlines …

Executing to higher standards of excellence

Why such quest for continuous improvement?

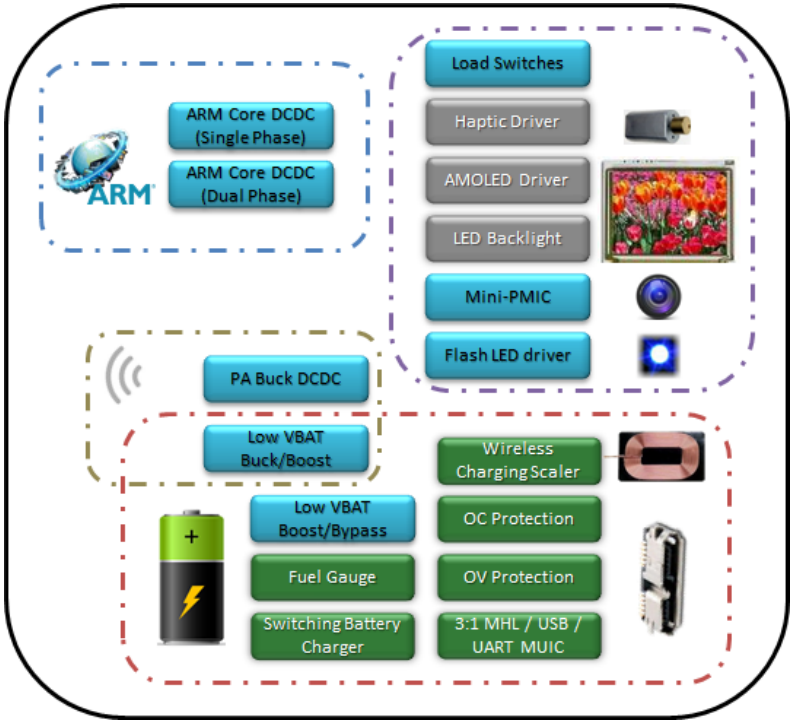
- Strong competition on integration & performances must be taken up …
- While still meeting key business drivers : time-to-market, ↘cost & ↗quality.

4 key axes to go the Next Step

- Keep re-enforce global team **expertise** in **Power & Battery management**
  - Continue grow Design technical expertise & leadership in our areas of focus.
  - Develop "systems and IPs aware" approach for Layout, Dig, Verif, CZ & Test.
- Develop **Quality Mindset Culture**.
  - Prevention is better than cure: the later things are corrected the higher the cost is.
  - Deploy best practices & lessons learned improving our work flows.
- **Flawless execution** from product definition to production ramp up
  - Drive all new IC, hardware & software developments while hard thinking Reuse.
  - Take time to do it right rather than taking it to do it twice.
  - Engage/biased to solve recurring problems or roadblock issues
- Take both **Team & individuals** to the next level
  - Take all benefits of new organization to improve synergy between functions.
  - Foster individuals development & career progression to meet Team objectives.

Design Goals headlines

- *Design center of excellence in Power Management.*

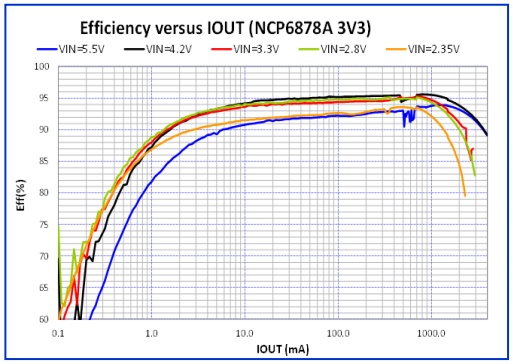


- *Design Center of reference for Power Interface functions*

Design Goals headlines 1/2

Design center of excellence in Power Management

- Develop best in class DCDC converters (be ahead competition).
  - Primary focus must be on NCP6353/56, NCP6868, NCP6878
  - Consolidate expertise in ripple base architecture.
  - Extend know-how to Multiphase Buck converter.
  - Master tradeoffs to reduce EMI generated by SPS.
- Develop key Power Mgt IPs for Wearable applications.
  - Flexible & modular IP to enable easiest reuse on PMIC.
  - Target directly IPs at least at the level of our main competitors
- Master mixed signal/ higher Integration challenges
  - Demonstrate with SCY6992 our ability for higher integration
    - Target final pass TO by early May
    - Test package ready on time for sampling & ATE CZ
  - Take lessons learned of all integration issues (Design, Layout)
  - Anticipate challenges of wearable design
  - Then result mixed signal integration guidelines & methodology.



NCP6878 efficiency

Top Wireless DCDCs ICs

NCP6353 – 3.0 A, 2.4 MHz DCDC with I²C and DVS

NCP6356B – 5.0 A, 2.4 MHz DCDC with I²C and DVS

Value Proposition

NCP6356B is a low cost step-down converter ideally suited for wireless application supplying processors / memory that demands high power at low voltages. Dynamic Voltage Scaling through I²C programming. It could also work as "transient load helper".

Unique Features

- 2.5 V to 5.5 V input voltage
- Up to 5.0 A Output Current
- DVS support through I²C
- Selectable Current Limit
- I²C acces in off mode
- 4 Level Thermal Warnings
- Best in class Transient / Ripple

Benefits

- Latest battery technology support
- Optimized processor power
- Facilitate inductor selection
- Optimized efficiency
- Preprogramming at low power
- Precise temperature control
- LPDDR4 memory support

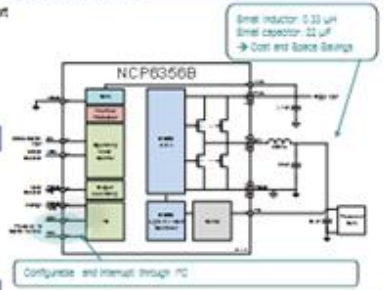
Other Features

- Fixed output voltage from 0.6 V to 1.4 V with 6.25 mV steps
- Low Quiescent Current thanks to PFM mode
- 1 µA Shutdown Current
- 100% maximum duty cycle DCDC
- Soft Start to Limit Inrush Current
- Current Limitation to Protect Against Short Circuit
- Thermal Protection

Market & Applications

Battery powered devices, Portable devices, Mobile phones, Entertainment, Standard 5V rail powered devices

Application Data



Ordering & Package Information

1.62 x 2.02 mm CSP20, pitch 0.4mm
Samples 3/20/2015 MP 4/27/2015

NCP6868 – Boost DC-DC Converter with By-Pass

Value Proposition — Compatible to FAN48632

The NCP6868 is a synchronous boost converter. It is designed primarily to boost new generation Low-Voltage Li-Ion Batteries (silicon anode-based) embedded into cell and smart phones. The objective is to maintain a minimum output voltage even in the case for which the battery voltage is below the system minimum. The device features a Boost mode coupled with a Bypass mode. It is capable to drive a load up to 2.5A, operates at a frequency of 2.5 MHz in Continuous Conduction Mode (CCM).

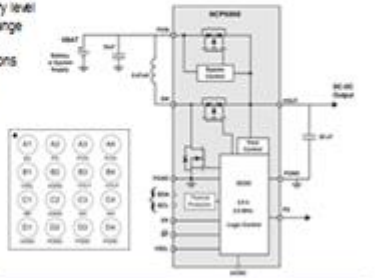
Unique Features

- 2.35 V to 5.5 V input voltage
- Bypass operation when Vin close to Vout
- few ext components & 0.47µH inductor
- High Efficiency up to 96%

Benefits

- Handles low voltage battery level
- Smooth and automatic change
- Ideal for tiny space
- Ideal for portable applications

Application Data



Other Features

- Output current up to 2.5A continuous (Vin = 2.6V, Vout = 3.5V)
- Fixed Output voltage from 3.0 V up to 5.3 V
- Active Discharge path when disabling
- Forced bypass option through /BP pin
- Low Quiescent Current
- Voltage Control pin (VSEL) to adjust Vout
- Soft Start to Limit Inrush Current
- Current Limitation to Protect Against Short Circuit
- Thermal Limit Protection
- 0.4 mm pitch WLCSP-16 package

Market & Applications

- Cell phone, smart phone, Portable devices
- Boost for Low-voltage Lithium-Ion (Li-Ion) Batteries

Ordering & Package Information

Samples Available Now MP 5/10/2015
Pin to pin compatible to FAN48632

NCP6878 – Configurable 2.5A/2.0A Buck/Boost Converter

Value Proposition

The NCP6878 is a synchronous buck/boost converter designed for addressing new Low Li-Ion Batteries embedded in smart phones or tablets. The transition between the different modes of operating is done automatically and seamlessly. It is able to drive a load up to 2.5A DC in buck mode and 2.0A DC on boost mode and provides excellent efficiency. An I²C serial control can also be enabled for configuring the output voltage.

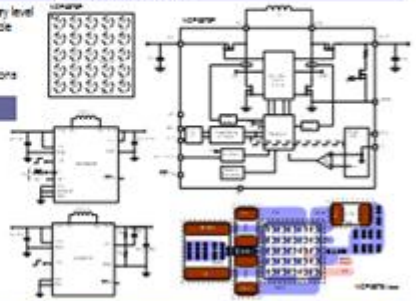
Unique Features

- 2.35 V to 5.5 V input voltage
- Automatic change between buck and boost modes
- few ext components & 0.47µH inductor
- High Efficiency up to 96%

Benefits

- Handles low voltage battery level
- Smooth and seamless mode transitions
- Ideal for tiny space
- Ideal for portable applications

Application Data



Other Features

- Output current up to 2.5Adc in buck (PVin ≥ 3.5V, Vout = 3.3V)
- Output current up to 2.0Adc in boost (PVin ≥ 2.8 V, Vout = 3.3V)
- 3 Versions: Fixed V_{OUT} (NCP6878Vxxx), I²C Programmable V_{OUT} from 2.85 V up to 5.3V (NCP6878P) & Adjustable V_{OUT} (NCP6878A)
- Low Quiescent Current
- Voltage Control pin (VSEL) to adjust Vout
- Hard Reset pin (/RC) & INT / PG pin (/INT/PG)
- Soft Start to Limit Inrush Current
- Current Limitation to Protect Against Short Circuit
- Thermal Limit Protection
- Small 2.02 x 2.02 mm² / 0.4 mm pitch CSP package (WLCSP-25)

Market & Applications

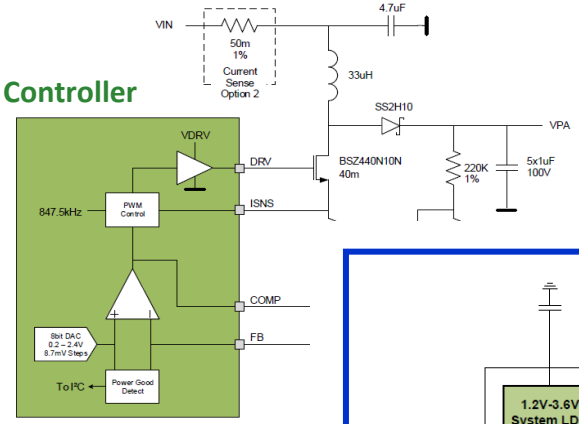
- Buck or Boost for Low-voltage Li-Ion Batteries
- Tablet, Phablet • Smart and Cell Phones • 3G / 4G RF PA

Ordering Information — In Development

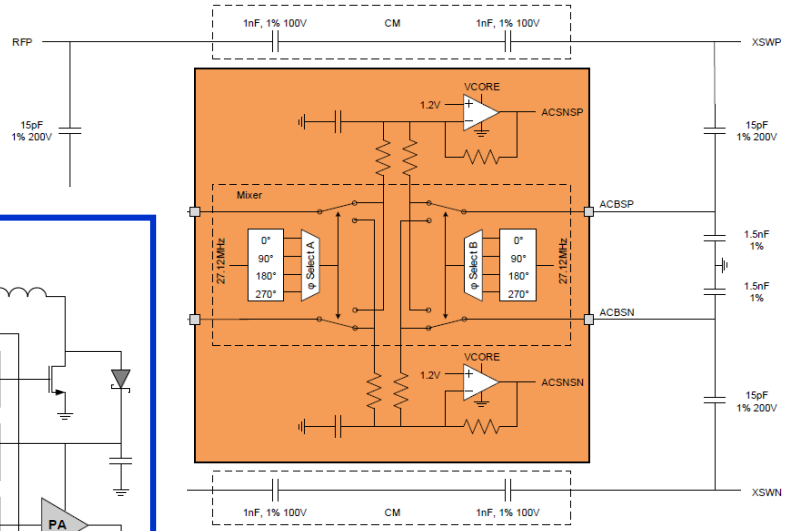
- NCP6878P FCCT1G: I²C version w/ Programmable Vout
- NCP6878V330 FCCT1G / NCP6878Vxxx FCCT1G : Fixed Vout
- NCP6878A FCCT1G: Adjustable Output Voltage

TX Wireless Charging IPs

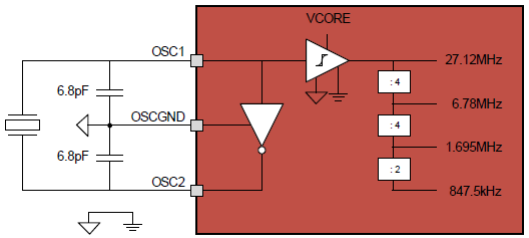
PA Boost Controller

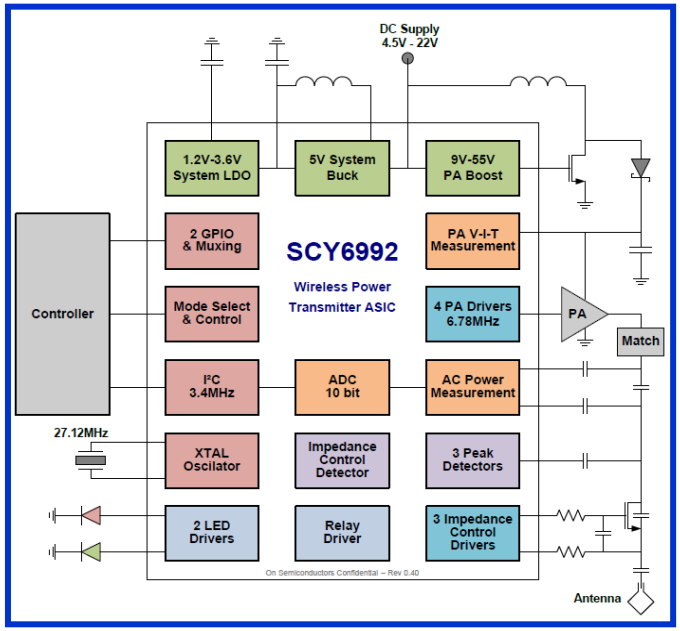


AC Power Measurement

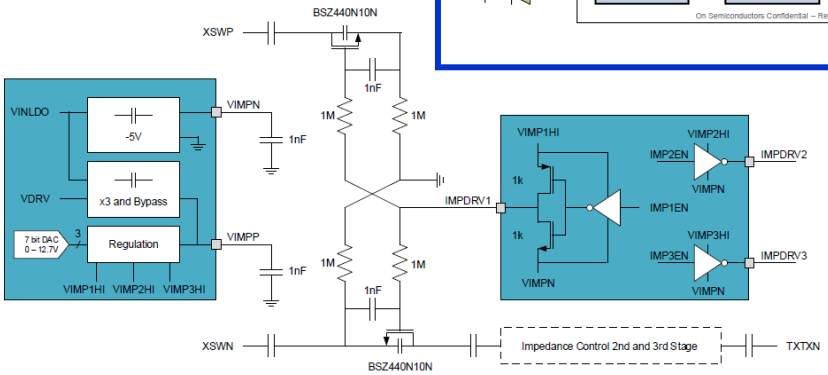


27. 12 MHz Crystal Oscillator

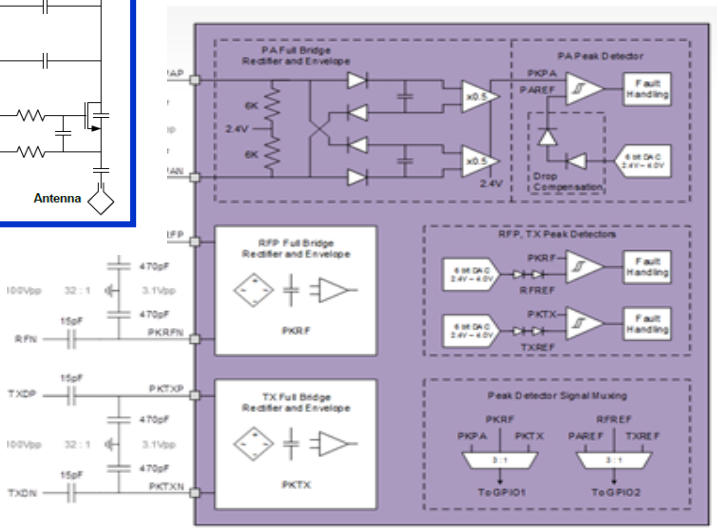




Impedance Control Drivers



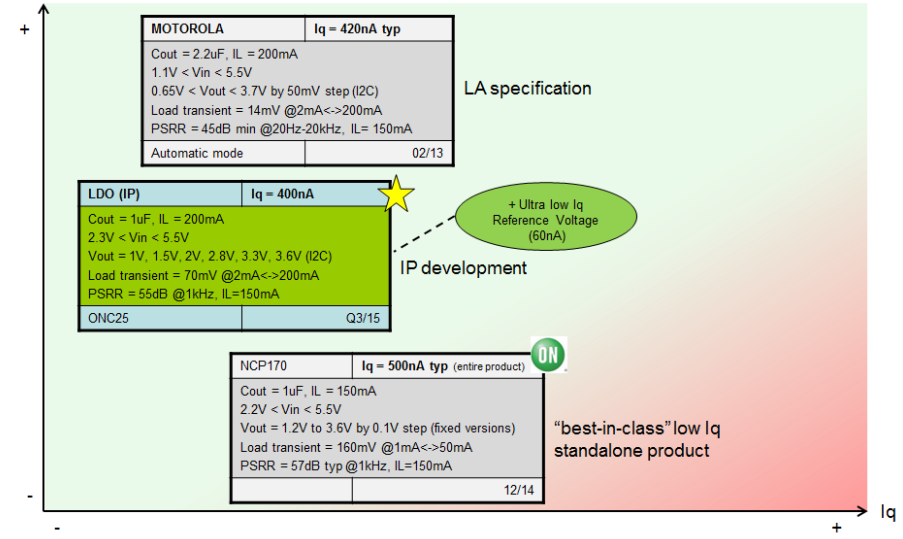
Peak detectors



Wearable IPs

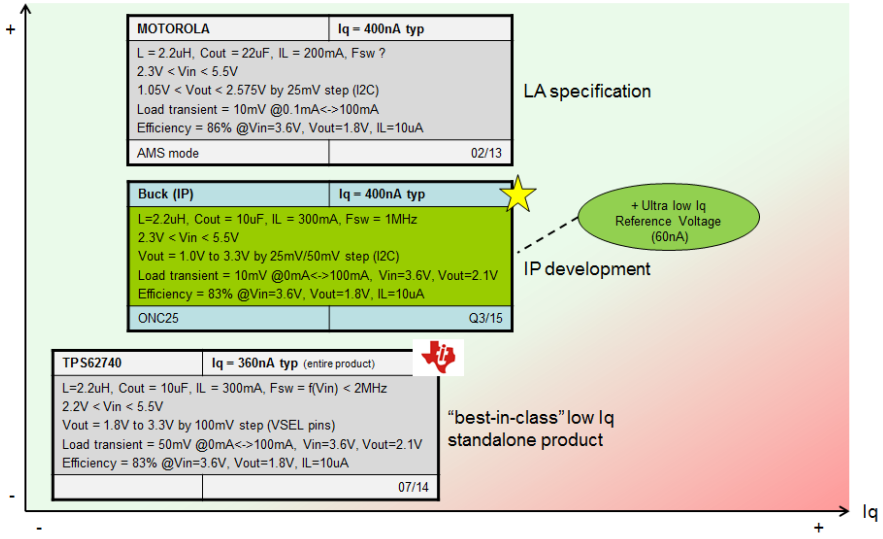
Ultra-low Iq LDO

Performances
(Cout, IL, load transient, PSRR)



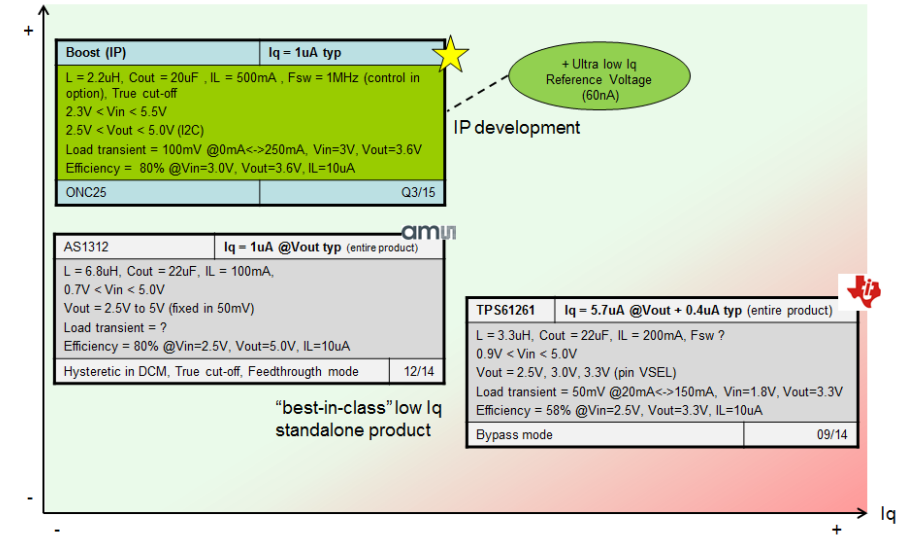
Ultra-low Iq Buck

(L, Cout, IL, load transient, efficiency)



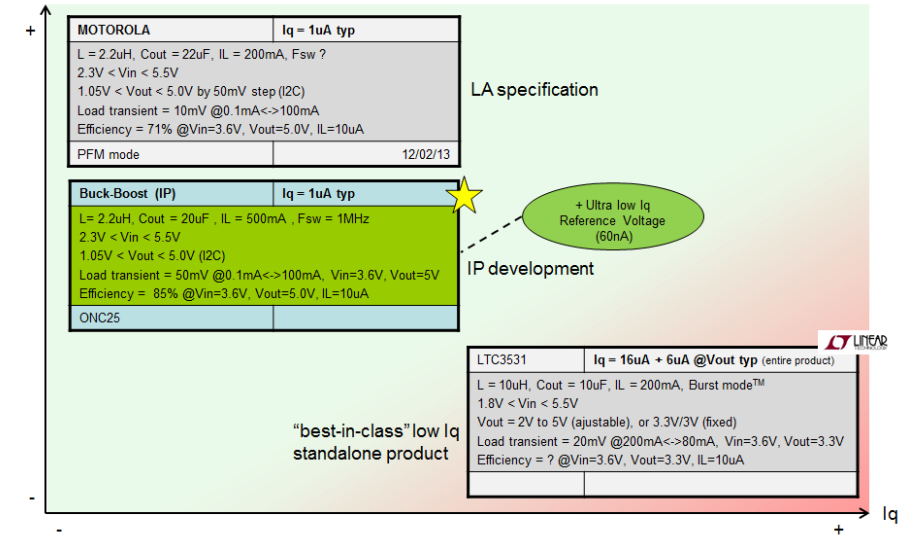
Ultra-low Iq Boost

Performances
(L, Cout, IL, load transient, efficiency)



Ultra-low Iq Buck-Boost

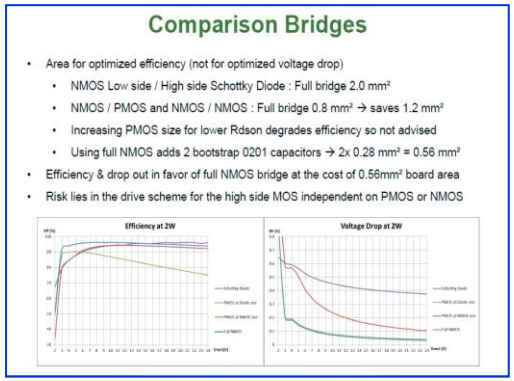
Performances
(L, Cout, IL, load transient, efficiency)



Design Goals headlines 2/2

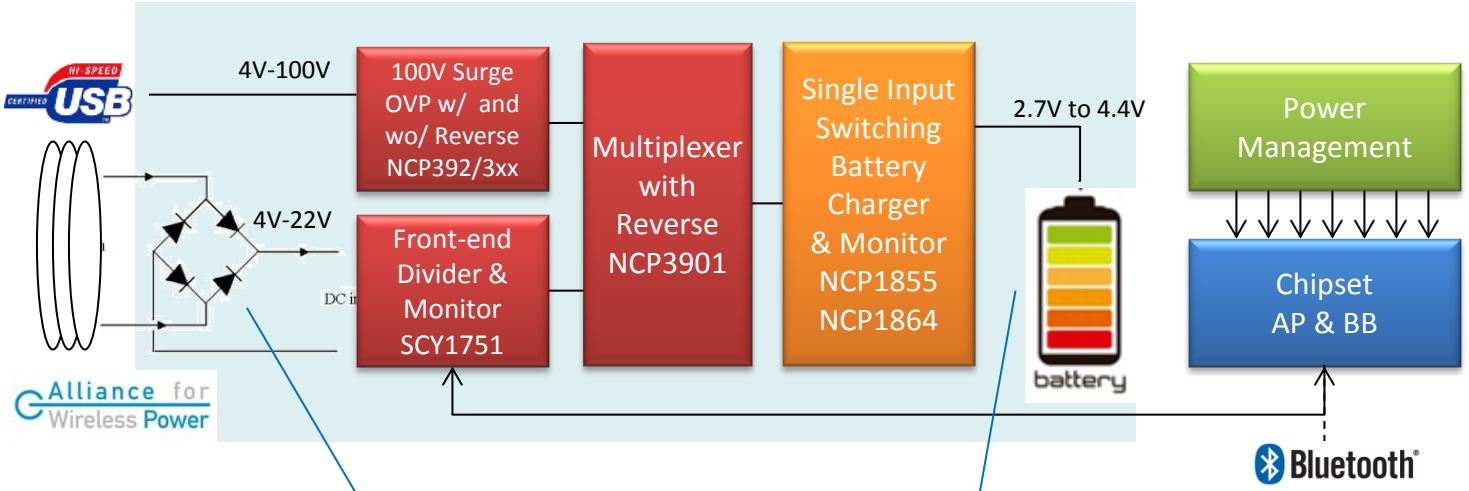
Design Center of reference for Power Interface functions

- Focus on project execution to accelerate new products introduction
  - Switching Battery Chargers: NCP1871/72, NCP1864/65, NCP1841
    - Close NC1871 as soon as possible
    - Be prepared to take ownership of NCP1864
  - De-risk SBC strategy with OVP, MUX, CHGPMP
    - OVP, MUX: NCP3901, NCP392 Tower …
    - CHG PUMP: NCP1764
- Continue Grow IP portfolio to enable new opportunities
  - Prepare wireless charging support integration in SBC.
  - Develop active rectifier to get all RX Wireless charging IP blocks.
  - Support Fuel Gauge architecture study & definition.
  - OVP with OCP feature to support USB PD Type C interface.

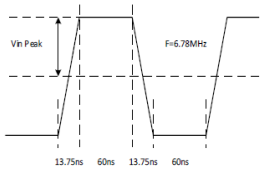


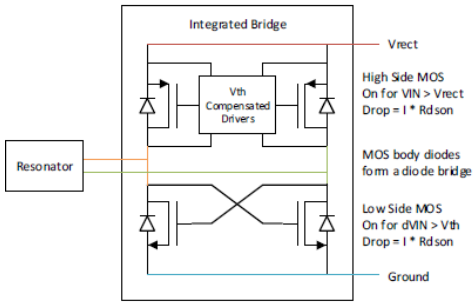
Feasibility Analysis NCP1841

RX Wireless Charging IPs

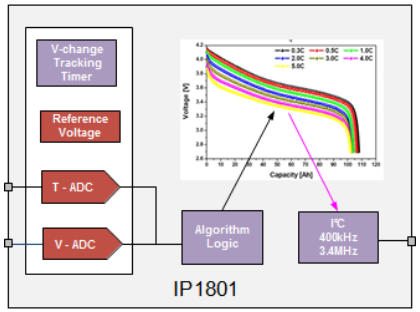


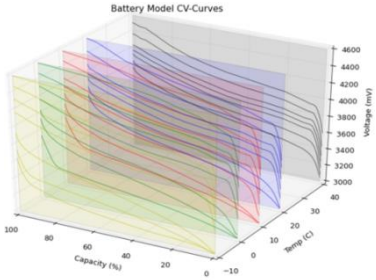
Integrated Bridge rectifier





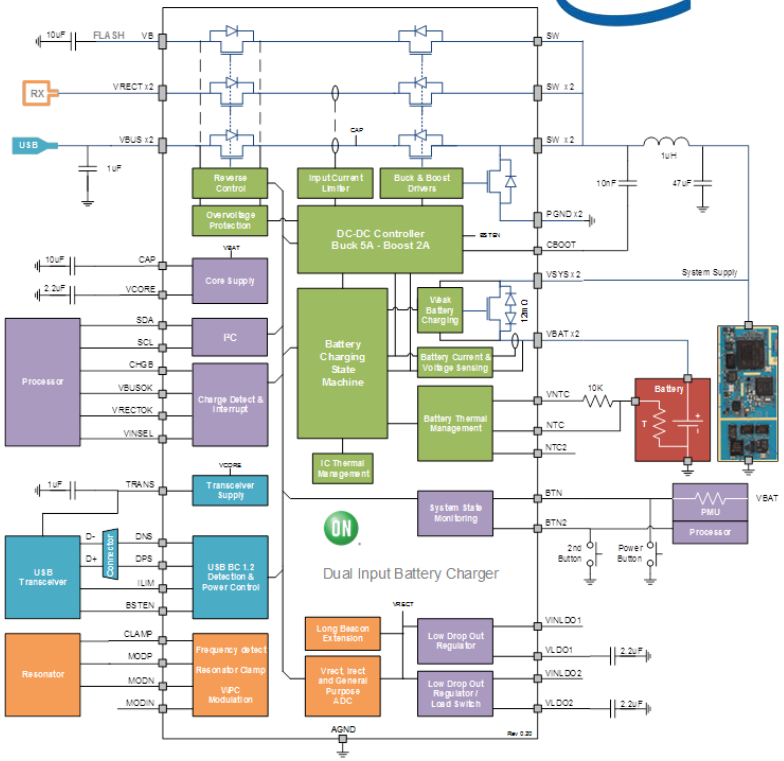
Fuel Gauge



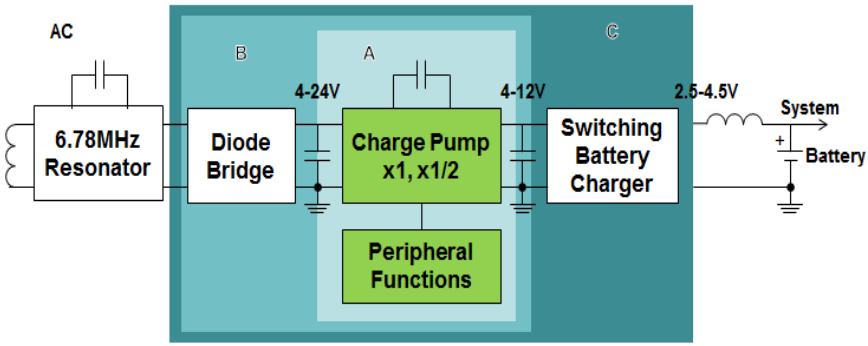


Charging IPs integration

NCP1865



NCP1841



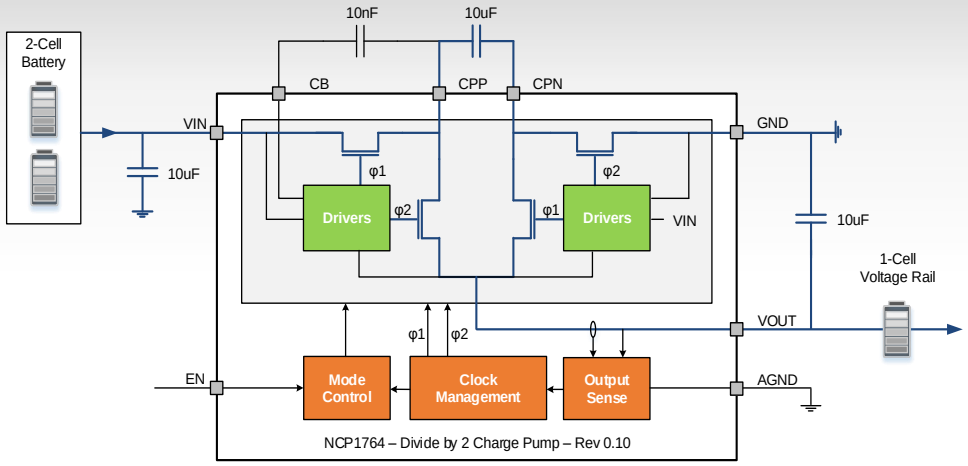
Wearable applications

- A4WP 2W max
- Battery <350mAh
- Form factor : Small, thin, curved

Smartphone or Tablet applications

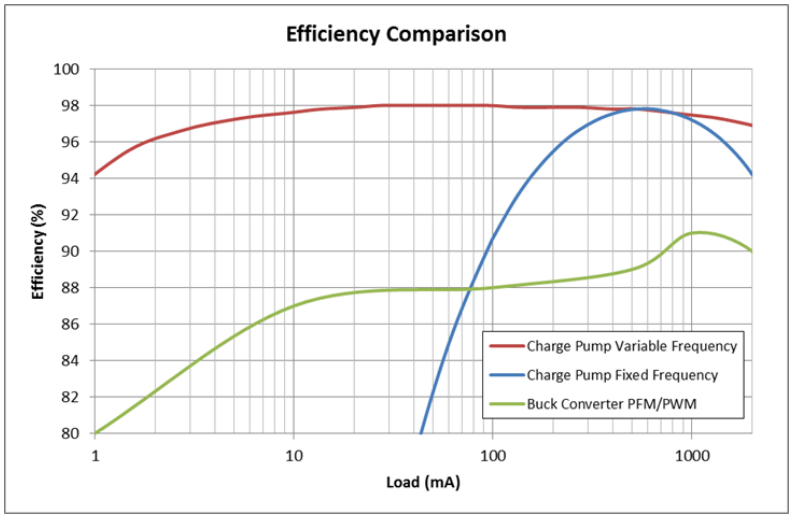
- Dual Input Battery Charger : USB Type C & A4WP
- OTG output for Camera Flash
- 1S Battery 4Ah

Charge Pump IPs



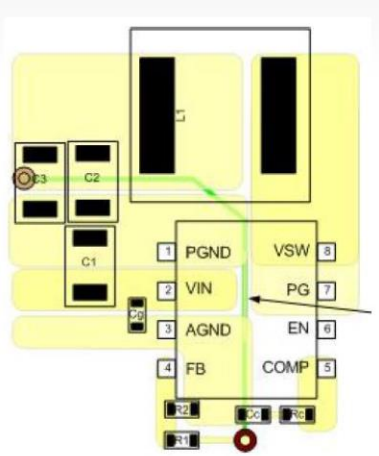
Divide by 2 Charge Pump with Adaptive Frequency

- "Closed Loop" Charge Pump:
  - ➔ Sensing of the C_{FLY} ripple voltage to control the switching frequency
  - ➔ increase the efficiency at light load.
- 4A output current capability
- Tile operation to double the output capability



NCP1764 (CP DIV2)
Area = 16 mm^2
Height < 1 mm^2

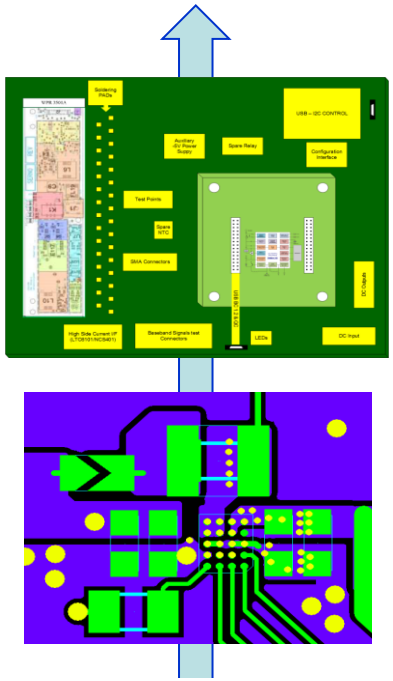
NCP3170 (Buck Converter)
Area = 70 mm^2
Height ~ 2 mm^2



Develop “System & IP” awareness

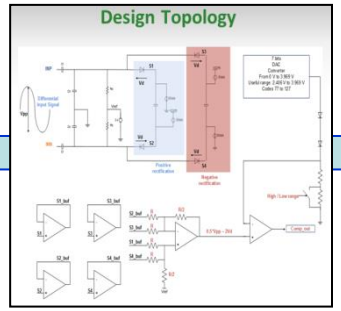
Power Management functions is our Core expertise

- **All is about the function itself**. Knowing the functions is determinant to learn how to draw, simulate, use and test it.
- Don’t need to know all the details of internal mechanism, but product cannot be approached simply as a « black-box »!
- When test it, don’t be sentimental: do your best to make the product failing!



Need also to learn about what is outside the box

- Designers to understand hardware constraints, measurement capabilities ...
- System & application: Verification vs validation - are we building the product right or are we building the right product?



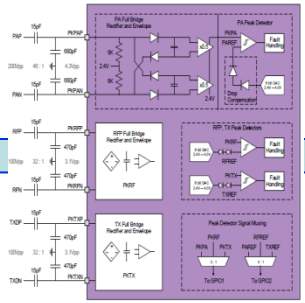
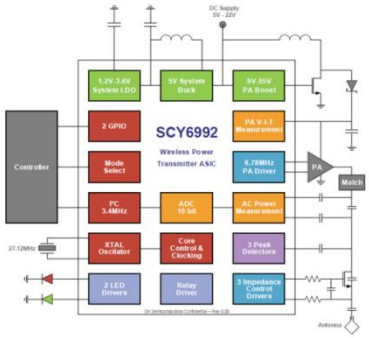
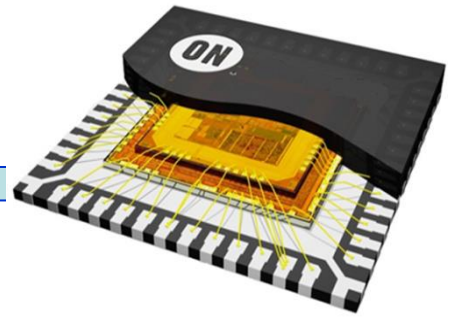


Figure 24: Peak Detectors





Principles of Design for Reuse

Planning for reuse at all stages of the NPD process

- **Reuse does not concern a specific deliverable** (usually refer to IP block, RTL, or physical design, but this is also relevant for simulation or cz benches, test hardware & software, and can also be applied to a methodology).

The six compass points of Design for Reuse

- **Abstraction :** it means concentrating on the essentials while temporarily ignoring the unimportant details
  - Tow down method is a natural way to approach a complex design task
  - Helps achieve modularity, increase quality, reliability and maintainability.
- **Modularity:** improve modularity , in turn increase the reusability of the cell
  - Design the functions interface thinking them likely to be used or slightly modified for derivative
  - Develop adaptive, reconfigurable approaches that allow single development with multiple, user-modifiable uses.
- **Optimization vs Flexibility:** set the right balance with all elements in mind
  - Anticipate roadmap evolutions or product derivatives while not overkill your first product (time, size).
  - Compromise between the most universal and versatile solution and the one that provides the most differentiation
  - Ideally Parameterization provides the best way of customizing while generalizing the reuse (ex: Memory compiler)
- **Legibility:** schematic, RTL or test codes must be designed thinking "Clarity and Understandability "
  - Complex design, code should be appropriately split into elementary cells/procedures
  - Documentation should be self contained (self explanatory names in code or schematics, comments inside …).
- **Simplicity:** The principle of simplicity is best captured by adage, "less is more."
  - « Simple can be harder than complex: you have to work hard to get your thinking clean to make it simple » S. Jobs.
- **Common Flow:** Reuse is moreover efficient as all designs use a consistent methodology based on standard tools.

Quality

New actions to Catch issues as Early as Possible

- Better **anticipate potential issue** during design phase
  - Systematically set architecture reviews for new IP development, prior full transistor level design.
  - Refresh Design & Layout Checklists based on all recent lessons learned (add a new DFT checklist).
  - Digital Designer to translate all requirements from design/app into a block specification or Design memo.
- Top Level Verification & Pre-silicon Validation
  - One ownership for both Functional & DFT validation
  - Ease Top verification for design community (connect modules, I2C interface, automatic vams0 or sch0 view)
- **CZ engineer** takes the **ownership for HTOL** development , to define the much relevant stressed conditions (DCDCs in close loop), in order to **catch earlier as possible any reliability issues (TDDB/HCI)**.

Increase our Fault coverage on new products

- Design for Test to **improve final test coverage**
  - Test Analog functions in closed loop to get best test coverage; it's also the most cost-effective approach.
  - DFT Eng. to identify methods to improve test coverage & test time, while not impacting IC performance & size.
  - Have a clear picture of our scan fault coverage and evaluate opportunities to improve it.
- IC characterization focused on **specification coverage** and **new IPs**
  - Coordinate IC characterization plan (CZ & ATE test plan) with the core team
  - Develop new benches to support RF IPs evaluation (Peak Detector , AC Power Measurement and PA driver)
  - Continue to grow the test library of AC measurements (Peak Current, PSRR & Noise)

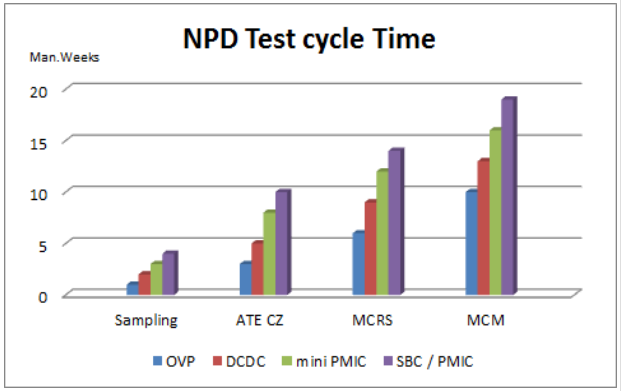
New Methodology or Procedures

- Set a formal **methodology** to achieve **top level routing** for best in class IP integration.
- Write with application team an internal **IEC test procedure** based on IEC61000-4-2 standard.

NPD Test Cycle Time

What are the key milsestones & targets?

- Hardware & Program to **sample customer** with 1st silicon
- **ATE CZ**: Full test coverage for tri temp CZ , ESD, latch-up & HTOL
- **MCRS & MCM Final test package** release for production (gage, spike check, correlation, checklist completed , qualification report …).
- Target ESD material ready from pass1.0
- Target run HTOL tests on pass1.x samples, prior production pass.



How to achieve this Pull-in? … With a strong Team work!

- Test Engineer assigned earlier in the development process of new IPs or ICs
- **Design Leader** to provide earlier **Design For Test document** to enable test package development
  - Standardize the document format to ease test program coding.
  - DFT engineer & Test team to deploy trim tables to designers
- **Digital/Verification team** to Develop a standard design flow to generate **plug and play Scan patterns**
- **Test hardware development** continuous improvement
  - Designed based on record of Lessons learned , with also in mind the product line roadmap
  - CZ engineer drives HTOL development looking for minimum Test HW & SW rework from production package.
- **Test software development** driven by three decisive elements
  - Test code legibility and flexibility to enable maintainability in production & quick product derivative
  - Test program architecture done to anticipate, at best , the later on test time optimization
  - ATE Characterization focused on key parameters and test limits definition for test time optimization
- **UF2000 prober** utilization to get qualification data for test package release and ease production ramp up

Individuals making a Team

Organization changes

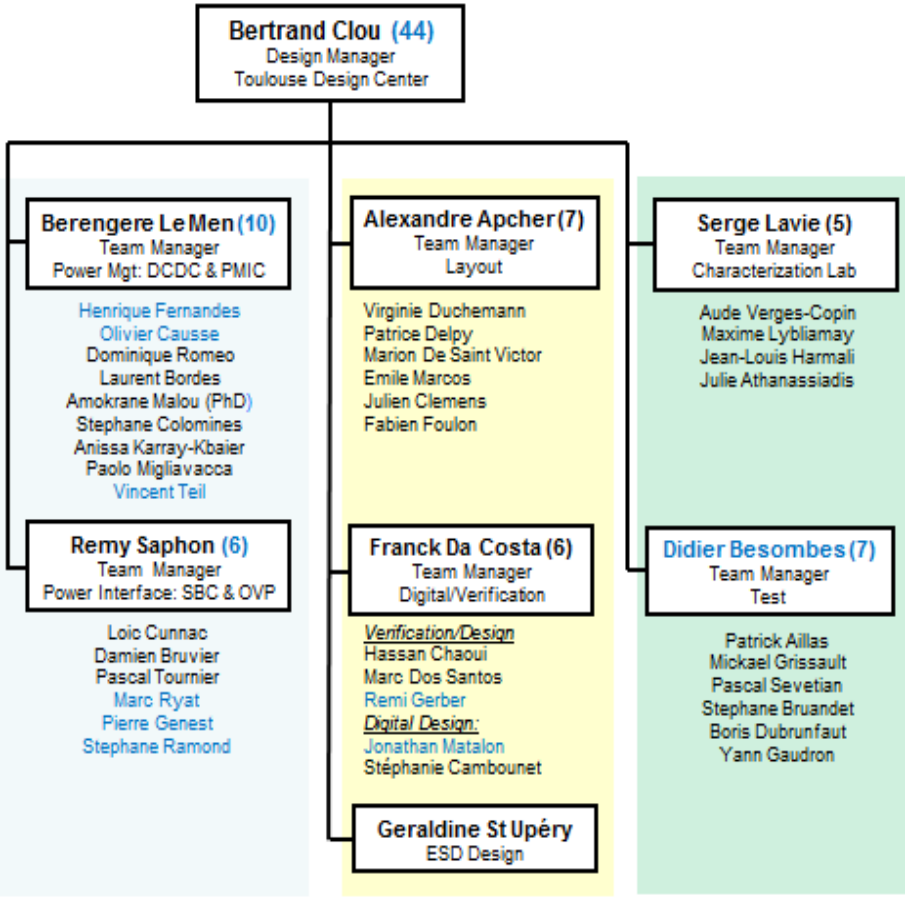
- To support this move forward excellence
- To enable best people development

People engagement

- Set SMART goals to enable career development
- Develop leadership (Thought, Result & People).
- Demonstrate a positive, “can-do” attitude, to improve situation no matter what it is.
- Be open minded to others opinion and support facts based decision.

Keep Team Spirit

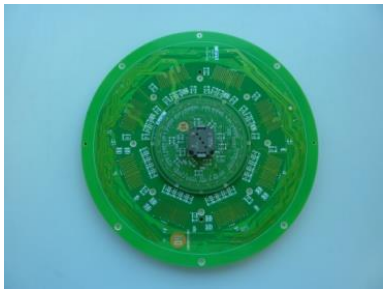
- Improve synergy between all functions: “We all win when we support each other”.
- What we can achieve as a team can far exceed what we can do as individuals.
- Effective & open team communication is essential for team efficiency & success.
- Re-enforce collaboration with Limerick

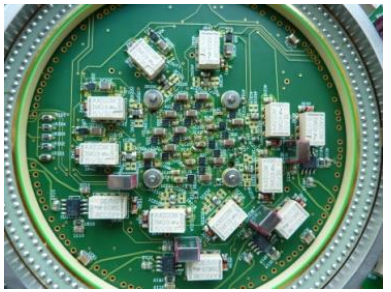


What Tester for New Products ?

Tester Strategy for PI 1/2

Today Toulouse Test equipment





2 Eagle ETS364

- CSP probe configuration (Majority of Projects)
  - Test package development and qualification for CSP Probe in Seremban
  - Challenging multisite probe cards development for swiching devices
- OSPI Final Test configuration (SCY6992)
  - Prototype test package development for Final Test in OSPI
  - Advantages: Hard docking capability to the PROBER or Handler
- Limitations:
  - Not adapted to ICs > 56 pins for multisite (ex: SCY6992).
  - Need to add a QHSU card to enable test of AC functions (AC accuracy?)

1 Eagle ETS88 Tester

- Seremban Final Test configuration
  - For Low pin count devices with ISMECA Turret handler
  - Test package development for NCP1871
- Limitations :
  - Soft docking with the Handler, very small load board,
  - Difficult to use for switching devices

1 UF2000 Prober

- To ease test package qualification & production ramp-up
  - Trim debug, gage study, data collection for qualification

Tester Strategy for PI 2/2

High Pin count ICs & AC functions (1-30 MHz range) require new test capabilities … 3 alternatives :

ETS800
with QHSU

- (-) QHSU on ETS800 ?
- (-) QHSU accuracy is not specified for AC level.
- (+) Lower risk for learning from ETS364 to ETS800
- (+) ETS800 Lower cost vs T2000 (765 k$)

microFLEX
with VHFAC

- (+) OK with VHFAC instrument
- (-) 19 testers in FT but only 1 tester available in Q3 and beyond
- (-) Test cost > ETS364 , depending on loading
- (-) Need Teradyne support for conversion

Advantest T2000
with GPWGD

- (+) New supplier
- (+) should be OK with GPWGD, tbc
- (-) Testers availability in FT?
- (-) Higher cost (950 k$)
- (-) need Advantest support for the conversion
- (-) Learning for eng. development

Questions and Answers

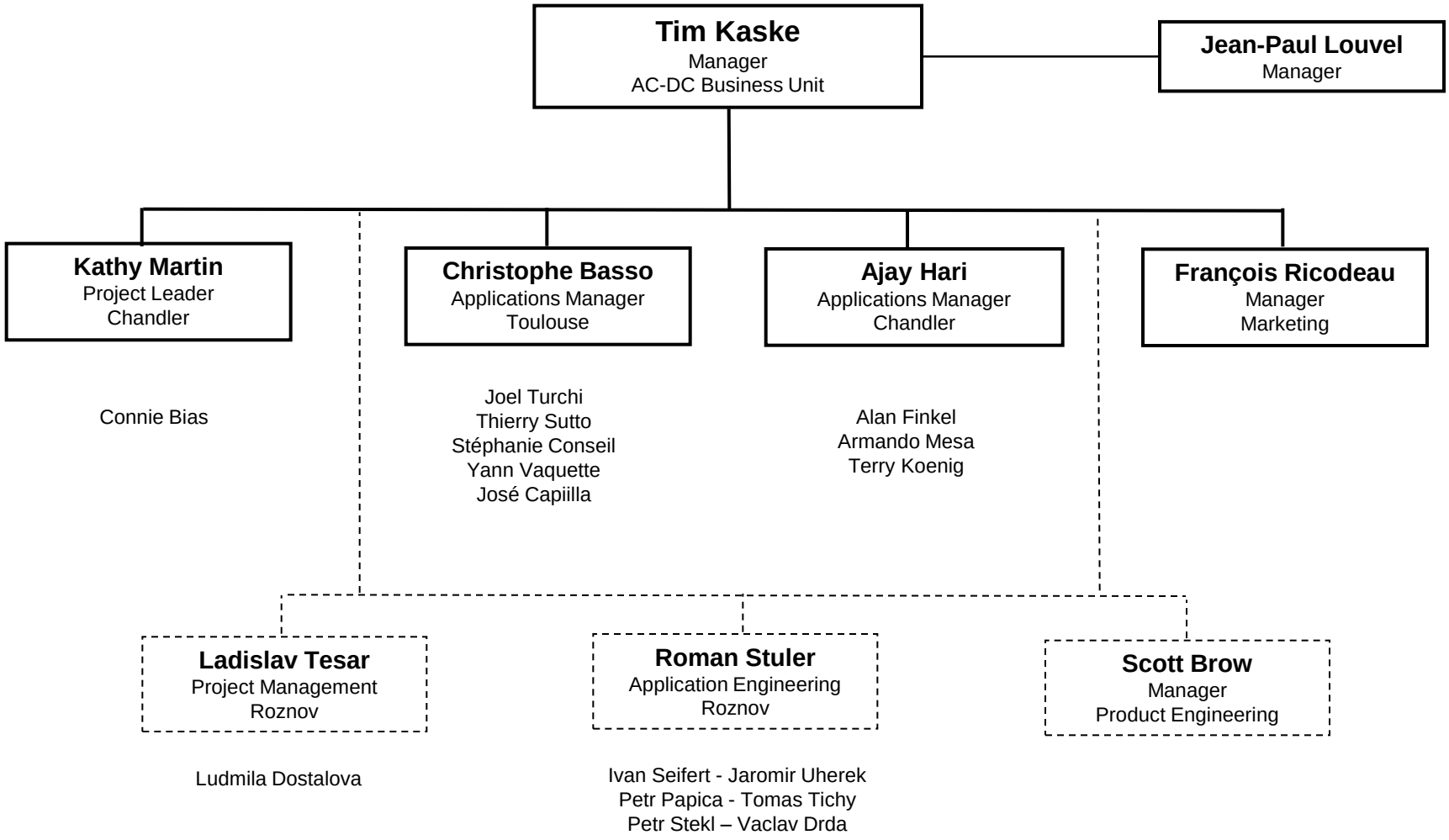
ON Semiconductor®

Ac-dc Toulouse Application Team

Ac-dc Team Members

- Joël Turchi – app. eng. PFCs, analytical studies
- Thierry Sutto – app. eng. half-bridges, primary-side regulators
- Stéphanie Cannenterre – app. eng. modeling, analytical studies
- José Capilla – app. eng. stability, analytical studies
- Yann Vaquette – app. eng. switching converters
- Christophe Basso – manager
- Jean-Paul Louvel – system architect TV (Tim Kaske)
- Marc Barboni – product line marketing (F. Ricodeau)

Ac-dc Organization Chart



Skills

❑ **New product concepts:**

✓ Power supply control: PFC control laws, resonance, quasi-resonance etc.

✓ Analytical analysis of problems, equations-based studies

✓ IP generation, numerous patents from 2008 to 2015

✓ Distinguished Innovators level II (J. Turchi, C. Basso)

❑ **Customer support**:

✓ small-signal, average modeling, SPICE model generation

✓ articles and papers presentations (PET-US, APEC/IEEE, PCIM…)

❑ **Seminar organization**:

✓ lot of training sessions, internal and external (1 hour to 8 hours sessions).

For IEEE-related conferences, APEC 2009/10/11/12/13/14 in the US

❑ **Copernican approach!** ⟶ 

✓ specifications are written here, dispatched worldwide (US, Czech R.)

Patents

- **2008-2015**

✓ ONS01196, C. Basso, J-P. Louvel: “TL431 bias current suppression”
✓ ONS01525, J. Turchi, "6-pin PFC without aux winding"
✓ ONS01444, S. Cannenterre, J. Turchi: "Primary CC PFC"
✓ ONS01320, J-P. Louvel: "High voltage Pre-Regulator"
✓ ONS013884, J. Turchi: "Optoless CC flyback conv."
✓ ONS01449, S. Cannenterre: "Automatic prop. delay compensation"
✓ ONS01383, J-P. Louvel: "OFF mode & Feedback combined SMPS"
✓ ONS01383, J-P. Louvel: "High Efficiency DSS"
✓ ONS01430, J-P. Louvel: "Automatic Eco mode detector"
✓ ONS01158, J. Turchi: "Interleaved clock"
✓ ONS01194, J. Turchi: "Brown-Out solution"
✓ ONS01220, J. Turchi: "Current Limit for Interleaved Converter"
✓ ONS01333, J. Turchi: "CCFF Modulation Strategy for PFC"

Recent Circuit Introductions

- NCP1365: primary-side controller for cell-phone and USB chargers
- NCL30082/83: optoless constant-current LED drivers
- NCP107x: high-voltage switchers in VHVIC 3
- NCL30085/86/87/88: PF-controlled constant current controllers for SSL
- NCP1565: high performance active clamp dc-dc for Huawei
- NCP1611/1612: new CCFF power factor controllers
- DAP029: new QR controller for Delta
- NCP1255 and DAP versions, peak power controllers
- DAP013 CA/H, 7 different successful versions

Products Sales TLS (2013-2015)

- DAP017 – NCP1605: 4 M$
- SCY99104 – NCP1250: 8M$
- NCP1252: 1.2 M$
- DAP018: 1.6 M$
- DAP013 - NCP1336: 1 M$
- NCP5104/5106/5181: 1.5 M$

All-in-one open-frame

Notebook adapters

ATX power supplies

USB chargers

LCD TVs

Involvement in Green Power Initiative

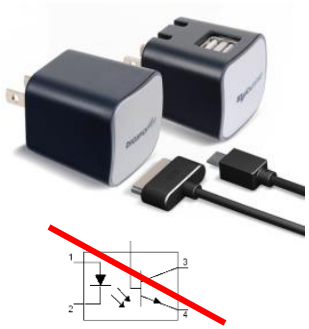
- Power consumption reduction necessity is present at design stage.
- Communication of ON Semiconductor performance via articles, papers.
- Involved in international conferences (APEC in the US, PCIM Germany)
- Companies like Apple challenge us to reduce the consumption further
- From 70 mW a few years back, they now want 10 mW

P_{noload} = 10 mW

- Toulouse members have worked on original solutions to meet 10 mW
- Several patents have been filed

Involvement in Primary Regulation

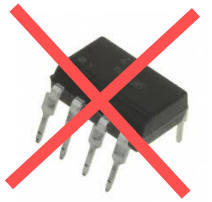
- The bulk of adapters market is now made of 10-20 W applications
- These adapters feed tablets and other portable devices
- Cost pressure implies the optocoupler suppression
- A new technique has been developed in Toulouse



- Toulouse members have worked on original solutions
- Joint development with Roznov colleagues (application and design)
- Challenges are numerous, standby power, efficiency etc.
- Potential customers are Samsung, Apple, Asus, RFTech etc.

Involvement in Solid-State Lighting

- LEDs-based lighting solutions are flooding the market
- Solutions still use an optocoupler to maintain the output current constant
- ON Semiconductor Toulouse has patented a novel optoless solution
- Solution addresses mass market production for CC applications



optocoupler

Constant current

- Several patents have been filed for this project
- Power Factor correction is now being added

Analytical Analysis, Trainings

- Analytical analysis of complex circuits
  - Problems solving for customers
  - Equation-based small-signal compensation
  - Power stage transfer function derivations

$$\frac{V_{out}(s)}{D(s)} = F_0 \frac{1+\frac{s}{s_{zF}}}{1+\frac{s}{\omega_{0F}Q_F}+\left(\frac{s}{\omega_{0F}}\right)^2} N \left(V_{in} - D_0 r_{on1} M_0 \frac{sC_{clp}}{1+\frac{s}{\omega_{0M}Q_M}+\left(\frac{s}{\omega_{0M}}\right)^2} \right)$$

Active-clamp forward converter transfer function

- International trainings to ON locations, Brno, Phoenix, Piestany, Oudenaarde, Limerick etc.
- Technical days at Huawei, Delta, (Renault, Valeo – cross BU trainings)

The Market Reality

- power market segment is wide, a few watts to 1 kW or so
- low-power designs gain in complexity (optoless, power factor, efficiency)
- vast majority of customers do not have the analytical knowledge:
  - they need extensive technical documentation to help for the design
- a lot of customers require design assistance and turnkey solutions
- in some cases, competitor circuits are close to ours, performance wise
  - the difference is made via the available documentation and support
  - typical example: LiteON asking us an analysis that hp, Dell or Apple require
  - difficult to combine fast-paced new product introduction and market care!
- A lot of small players who copy our circuits: Leadtrend, ONBright, GreenForest. Price is severely brought down.

FORFAIT EN JOURS ET SUIVI DE LA CHARGE DE TRAVAIL

I - Rappel des règles du Forfait jours

- Tous les collaborateurs cadres des sociétés ON Semiconductor France SAS et ON Semiconductor SAS sont en forfaits jours (213 jours par an) en raison de leur autonomie dans leur activité professionnelle.

- Le document auto-déclaratif qui doit être signé par le collaborateur et le Manager permet de s'assurer du respect du nombre de jours travaillés.

- Les collaborateurs disposent de 13 jours de RTT par an à prendre par trimestre.

  Un contrôle régulier est effectué par le Département des Ressources Humaines (kiosque RH) pour s'assurer que ces jours soient pris.

  A défaut un report et une planification sont effectués avec validation du Manager .

- Le collaborateur en forfait jours reste soumis aux règles du repos quotidien de 11 heures et du repos hebdomadaire de 35 heures

  (24 heures + 11 heures).

FORFAIT EN JOURS ET SUIVI DE LA CHARGE DE TRAVAIL

II – Le suivi de la charge de travail :

A – Entretien individuel avec chaque salarié ayant une convention de forfait en jours et son Manager.

Au vu des résultats des actions RPS menées l'entretien qui était semestriel depuis 2011 est annuel depuis 2014.

L'entretien porte essentiellement sur :

=> *la charge de travail du salarié*

=> *l'organisation du travail dans l'entreprise*

=> *l'articulation entre l'activité professionnelle et la vie personnelle et familiale*

=> *la rémunération du salarié*

L'entretien est formalisé par écrit dans le formulaire ci-dessous .

	Niveau de satisfaction (1-2-3-4)*			Oui -Non	Commentaires si Non	Oui -Non	Détails
Charge de travail (importance, répartition, évolution, impact des périodes de vacances)							
Organisation du travail dans l'entreprise et le service							
Articulation entre la vie professionnelle et la vie personnelle et familiale							
Rémunération (en lien avec le poste occupé, les responsabilités, le temps de travail)							
Autres thèmes abordés dans l'entretien (à préciser)							
conclusions :							
Nom et signature du collaborateur			**Nom et signature du Manager :**				

* niveau de satisfaction
1 -très satisfaisant
2- satisfaisant
3- insatisfaisant
4- problème soulevés

FORFAIT EN JOURS ET SUIVI DE LA CHARGE DE TRAVAIL

- B – Analyse des résultats de l'entretien et suivi :

- Les entretiens permettent de suivre l'évolution positive ou négative sur les différents thèmes. Le formulaire qui prévoit une note de satisfaction de 1 à 4 attribuée par le collaborateur est un indicateur objectif qui permet de mesurer de manière précise les résultats.

- les résultats sont analysés par le service des Ressources Humaines et si des problèmes sont détectés un suivi individuel est mis en place et un plan d'action est mis en œuvre (les notes 4 font systématiquement l'objet d'un suivi).

FORFAIT JOURS ET SUIVI DE LA CHARGE DE TRAVAIL

III – Un renforcement des garanties

Une jurisprudence qui tend à se confirmer considère que les mesures de contrôle du forfait jours doivent être de nature à garantir que l'amplitude et la charge du travail restent raisonnables et assurent une bonne répartition dans le temps du travail de l'intéressé, et donc à protéger la sécurité et la santé du travailleur.

L'accord de branche de la Métallurgie sur les forfaits jours qui est applicable à notre société a été reconnu valide par la cour de cassation.

On peut constater que de plus en plus de sociétés contrôlent effectivement les amplitudes de travail par un dispositif d'enregistrement du temps de présence ou un système auto déclaratif afin de disposer d'éléments objectifs.

FORFAIT JOURS ET SUIVI DE LA CHARGE DE TRAVAIL

La société a jusqu'à ce jour privilégié l'autonomie des collaborateurs dans la gestion de leur activité et le dialogue entre le Manager et le collaborateur pour garantir une charge de travail raisonnable.

Une note de rappel des règles et des procédures à suivre a été communiquée au mois de janvier 2015 à tous les collaborateurs afin de sensibiliser les collaborateurs et les Managers à l'importance du respect de ces règles et assurer une charge de travail raisonnable et une bonne répartition de la charge de travail dans le temps.

Un renforcement des obligations de l'employeur en ce qui concerne les garanties n'est pas encore d'actualité mais pourrait se dégager des jurisprudences à venir.