

# VoltageStorm PE V4.0.0 Data Requirements

## High Level Requirements

Design can be given in DEF format, GDS format or a mix of DEF & GDS formats.

Standard cell primitives should ideally be given in LEF.

IO's, memories and other IP should ideally be given in LEF and GDS (can handle GDS only)

## Layout Data Requirements

Design Data can be given in several formats and combinations of:

- 1) DEF(s) – design can be provided as a single DEF or multiple hierarchical DEF's
  - Does not need to be LVS/DRC clean
- 2) GDS of the design
  - VDD/VSS at least should be LVS/DRC clean for predictable results
  - Several GDS files can be given – must have consistent layer maps
- 3) Mix of DEF(s) & GDS files
  - VDD/VSS in the GDS should be LVS/DRC clean for predictable results
  - Example: GDS of RDL layer for flip-chip is available in GDS only
  - Example: GDS of finished block with ECO's not present in DEF
  - GDS layer mapping of design
  - DEF comments:
    - DEF layout as opposed to logic
    - Use “auDefOut” within Apollo environment
    - Can also use “auNDOApi” api routines to customize output from within Apollo environment

Library (Primitive) Data:

- LEF of the technology – wire widths and via rules
- Standard cell library/primitive cells – LEF only
- IO primitives – LEF and GDS
- Memories – LEF and GDS
- Other IP blocks – LEF and GDS
- Block DEF - LEF interface of each P&R block
- LEF comments:
  - Use “getClash” within Apollo environment if LEF's not already available
  - Can also use “auNLOApi” api routines to customize output from within Apollo environment
  - LEF describes how an entity (primitive or hierarchical block) interfaces with the next level up
- Additional when GDS supplied:
  - Assura/Dracula/Hercules/Calibre run-set that describes the GDS layer map, layer connectivity and transistor forming layers
  - List of all device types present in layout
  - GDS layer mapping – gds of libraries can sometimes be different to the mappings used in the design – need both.
- What if LEF of a primitive is not available?
  - Need the GDS of the primitive plus:
    - What layer(s) are text labels on?
    - Any special port geometries?

## Circuit Data Requirements

- Power/ground pad locations

- To insert voltage sources at the correct pin locations, require the X and Y coordinates (in um) and the layer name of each of the power/gnd pins (name, x, y, layer)
- Remember to include the power/gnd supplies for the pad ring
- Spice model cards for transistors
- Nominal voltage and total power consumption
- Limit for IR drop on (Power and Ground)
- For PowerMeter:
  - Synopsys .lib file for the library/primitive cells
  - DSPF/SPEF of block(s)
  - Overall frequency
  - Clock root names and their respective frequencies
  - Additionally/optionally:
    - SDC (Synopsys Design Constraint file) – provides clock information
    - Low Frequency and high frequency signals – activity factor
    - Activity factors:
      - all inputs
      - all signals (switches off propagation algorithm)
      - TCF – Cadence toggle file format
    - VCD:
      - primary inputs
      - all signals (switches off propagation algorithm)
    - Input slews
      - can generate from CeltIC NDC
      - we provide a .tcl script to dump out slews from PT
    - Power information on blocks, specific IP's

## ***Process Data***

- Layout Scale factor to be applied to the drawn data during extraction
- Layout Bias information for each layer to be applied to the drawn data during extraction
  - Metal biasing that will be imposed on the drawn data (in addition to any scaling)
  - WEE effects handled automatically
  - Use of layout scale and layout bias usually only required when using “generic rules” which require re-targeting to different processes
- Name of exact process: (e.g. TSMC 0.13um Low-k 1P8M).
- We already have many technology files already created for TSMC (access TSMC web-site), UMC (access UMC web-site), IBM and CSM. If you can't find the technology file we can see if we have it at Cadence.
- If using an internal process or technology file not available please refer to the following document “Process Models – Requirements”.

## ***Electrical parameters (for Electromigration Analysis of Power and Signals)***

- Please refer to the document “EM Models – Requirements”

## ***Computing Resources***

- Host id for evaluation license.
- If using Sun: 5 UltraSparcs, 256MB, 1GB swap, Solaris 2.6 or better. One machine should have a minimum 1GB main memory, and 4GB swap. For designs larger than 15 million transistors, require a Solaris 2.8 machine using 64bits. Should have large memory ( $\geq 4GB$ ) and large swap ( $>10GB$ ).
- If using HP: 5, 256MB, 1GB swap, HP-UX 10.20 or better. One machine should have a minimum 1GB main memory, and 4GB swap. For designs larger than 15 million transistors, require a HP-UX 11.00 machine using 64bits. Should have large memory ( $\geq 4GB$ ) and large swap ( $>10GB$ ).

- Can automatically handle a mix of the Sun and HP machines.
- 10GB file system, fully NFS'd
- Home directory must be cross-mounted on all machines.

Filename: VSPE - Requirements.doc  
Directory: X:\vstorm  
Template: C:\Documents and Settings\Administrator\Application  
Data\Microsoft\Templates\Normal.dot  
Title: LAYOUT DATA  
Subject:  
Author: Preferred Customer  
Keywords:  
Comments:  
Creation Date: 8/28/2002 5:59 PM  
Change Number: 21  
Last Saved On: 10/7/2003 2:31 AM  
Last Saved By: Tom Taylor  
Total Editing Time: 2,774 Minutes  
Last Printed On: 8/19/2004 5:35 PM  
As of Last Complete Printing  
Number of Pages: 3  
Number of Words: 709 (approx.)  
Number of Characters: 4,042 (approx.)