Répondre Répondre à tous Transférer | Fermer | Aide

⚠ Les pièces jointes peuvent contenir des virus risquant d'endommager votre ordinateur. Elles peuvent aussi ne pas s'afficher correctement.

De: Alexandre Apcher
Date: mar. 15/03/2011 15:27
À: Patrice Delpy
Cc:
Objet :
Pièces jointes : Appraisal2011_Patrice Delpy.pdf(149Ko)

Afficher sous forme de page Web

A imprimer et a signer

Alex

Répondre Répondre à tous Transférer | Fermer | Aide

De: Alexandre Apcher Date: mar. 08/02/2011 11:36
À: Anissa Karray-Kbaier; Aurore Masson; Virginie Duchemann; Patrice Delpy; Fabien Foulon; Julien Clemens
Cc: Bertrand Clou; Berengere Le Men
Objet : FW: Marsk order checks
Pièces jointes :

Afficher sous forme de page Web

Tous,

Suite a l'erreur de commande de masques sur le NCP2815 (il a été commandé sur GBOM le V3 alors qu'il fallait commander le V4 ce qui rend le produit non fonctionnel) je vous demande a tous **une extrême rigueur et concentration lorsque nous COMMANDONS les masques dans GBOM**.

N'hésitez pas vérifier 2 fois ou a faire vérifier la cohérence de la GBOM et du gds.

Pour les tweaks (c'est le cas pour le 2815) les Stream compare demande une rigueur et une concentration absolue pour bien noter les niveaux modifies.

Des actions sont en cours en Gresham pour améliorer leur flow de traitement des GDS afin que ce genre d'erreur ne se reproduisent plus.

Merci a tous pour votre vigilance a ce sujet.

Alexandre

From: Robert Muller
Sent: Monday, February 07, 2011 8:16 PM
To: Bertrand Clou
Cc: David Price; Alexandre Apcher; Berengere Le Men; Myriam Combes; John Jensen
Subject: RE: Marsk order checks

Hello Bertrand,

Its normal practice for us to run XOR to double check the order against the previous revision. We have in the past notified designers they have missed changed layers, but I somehow missed this on these two parts. Both G0B014B and G0B014C Y07K had the same incorrect via layer specified in the order. I discussed this with my management and we're looking at automating the xor check in our tapeout flow, making it mandatory. Automation for initial releases, which compares gds layers vs layers in order, is currently being worked on.

Regards,

Robert

From: Bertrand Clou
Sent: Monday, February 07, 2011 9:59 AM
To: Robert Muller
Cc: David Price; Alexandre Apcher; Berengere Le Men; Myriam Combes
Subject: Marsk order checks

Hello Robert,

We have just received the last metal tweak version of the NCP2815 audio IC and it is not functional at all.

This is due to an error we made during the mask order in GBOM : the Via3 layer which is actually not modified has been ordered in place of via4 layer which has been modified and finally not ordered. Wafers have been then processed with old version of Via4 layer, creating a short circuit.

In order to not repeat same story in the future, just because of a typo, would it be possible to add some cross-checks on your side?

- Full layer pass: check layers between gds delivered and layers ordered in GBOM

- Metal tweak pass: run gds compare between gds delivered and previous one to re-validate the mask order

Thanks to let us know what do you think.

Best regards,

Bertrand

Répondre Répondre à tous Transférer Fermer Aide

De:	Michael Tedeschi	Date: lun. 08/08/2011 22:35
À:	David Price; Alexandre Apcher; John Jensen; Michael Schlicht; Robert Muller	
Cc:	Catherine Goyon; Patrice Delpy; Miroslav Hora; Verne Hornback; Warren Thompson; Jake Wright; Sangmok Lee; Edward Zanella; Tomas Pecenka; Dan Hegsted; Wayne Heavey; Santosh Menon; Tracy Myers	
Objet :	RE: GAN18505.1 - unusual PC-Test data	
Pièces jointes :		

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Hi David,

Sorry for late reply.

I looked at the file “test_chip.drc.summary” include with the job and noticed the PAHOLE_OS_ANYLAYER_DE_EDGESEAL check was not executed.

```
RULECHECK co_ew_de_edgeseal ................................ TOTAL Result Count = 0
RULECHECK pa_mw_de_edgeseal ................................ TOTAL Result Count = 0
RULECHECK pahole_os_anylayer_de_edgeseal ................... NOT EXECUTED
RULECHECK text_outside_chipsize ............................ TOTAL Result Count = 0
RULECHECK layers_outside_chipsize .......................... TOTAL Result Count = 0
```

I then loaded the GDS in CALIBRE and using the SET CHECKS option from the CALIBRE GUI enabled the check and ran DRC. I did get the following flag:

```
Check pahole_os_anylayer_de_edgeseal   559
  Cell A_test_chip_top                 559
```

So it appears this check is OFF by default and needs to be enabled.

I am not sure why the default is OFF and need to consult with Mirek when he returns from vacation to get the history on this. I suspect this check was flagging during cell level runs and there was a ticket/request to default the check to OFF which I don’t think is the right decision since we rely on this check to ensure the EDGESEAL is exists and no data extends past the edge seal.

The DRC check selection GUI in CALIBRE is limited in capability but recently some new capability has been added to CALIBRE which will enable the PDK team to present designers with a more descriptive Menu for presenting and setting DRC checks based on GROUPS. Ed’s team is testing this capability and working on a proposal for implementation which we will run by you, the mask prep team, and some BU reps for review.

We believe this new capability will make it easier/more reliable for designers to select checks between desired block and top level checks (ex: DFMR, IO, density, etc) which should avoid this issue. (ticket # 52892, 72978)

I will initiate a ticket to track defaulting this specific check since it does not fall into one of the generic GROUPS for ONC25 and will also initiate a ticket to check and implement this for ONC18 as well.

In the mean time, we will initiate a design alert notifying designers to be sure they enable this check for tape out.

John Jenson: Is this something we can do for GRS incoming checks till new methodology is in place? I looked through the CALIBRE deck and this appears to be only check that is defaulting to OFF besides known DMFR, IO, and COVERAGE group checks.

// Unselect section

```
// ticket 52892; TAPEOUT_CHECKS might be default setting in future.

// Current #IFDEF implementation is for MAtrin Kejhar for testing purposes.

#IFDEF $TAPEOUT_CHECKS YES

DRC UNSELECT CHECK dfmr ?_un_mincoverage

#ELSE

DRC UNSELECT CHECK dfmr                          (this is DMFR group checks)

DRC UNSELECT CHECK io                            (this is IO group checks)

DRC UNSELECT CHECK coverage                      (this is COVERAGE group checks)

DRC UNSELECT CHECK pahole_os_anylayer_de_edgeseal    (this is EDGESEAL individual check)

#ENDIF
```

Best Regards,

mt

From: David Price
Sent: Monday, August 08, 2011 10:46 AM
To: Alexandre Apcher; John Jensen; Michael Schlicht; Robert Muller
Cc: Catherine Goyon; Patrice Delpy; Miroslav Hora; Michael Tedeschi; Verne Hornback
Subject: RE: GAN18505.1 - unusual PC-Test data

Mike,

Please advise why this design is not getting flagged for missing edgeseal.

David Price

From: Alexandre Apcher
Sent: Monday, August 08, 2011 6:39 AM
To: David Price; John Jensen; Michael Schlicht; Robert Muller
Cc: Catherine Goyon; Patrice Delpy
Subject: RE: GAN18505.1 - unusual PC-Test data

Hello all,

To complete Patrice ‘s mail please find in attachment 3 snapshots of the calibre DRC.

You can get all DRC files by onsend :

> Hello,
> Your file test_chip.tar has been successfully transferred to the ONSend server.
> It can be retrieved using the keyword: uhmk4589x
>
> Thank you for using the ONSend tool.
>
> For help, type:
> unix> onsend -h
>
> For web access see: ONSend
>
> Thanks,

ONSend admin
Th. Bordignon © ONSemiconductor 2008-2010

Best Regards

Alexandre

From: Patrice Delpy
Sent: Friday, August 05, 2011 11:45 AM
To: Miroslav Hora; David Price; John Jensen; Michael Schlicht; Robert Muller
Cc: Alan Massaro; Kim Johnson; Kass Giusti; Agajan Suwhanov; Dan Hegsted; Verne Hornback; Ken Fuchs; Michael Tedeschi; Alexandre Apcher; Catherine Goyon
Subject: RE: GAN18505.1 - unusual PC-Test data

David,

There is no edgeseal in circuit. I don't know the reason but the structure has been forgotten or deleted in layout.

The PC –Test electrical monitors are shorted with a internal guard ring.

The Topcell DRC / LVS do not verify the edgeseal instantiation , 0 errors in our case (DK onc25_5_8p3).
Since it was a testchip, the visual check was quickly done.

Apologize.

Regards,

Patrice

From: Miroslav Hora
Sent: Friday, August 05, 2011 9:16 AM
To: David Price; John Jensen; Michael Schlicht; Robert Muller
Cc: Alan Massaro; Kim Johnson; Kass Giusti; Agajan Suwhanov; Dan Hegsted; Verne Hornback; Ken Fuchs; Michael Tedeschi; Patrice Delpy; Alexandre Apcher; Catherine Goyon
Subject: RE: GAN18505.1 - unusual PC-Test data

David,

You are correct. The rule check:

- whether the edgeseal is placed in layout
- whether any layer is outside of edgeseal

Regards,

Mirek

From: David Price
Sent: Thursday, August 04, 2011 10:42 PM
To: John Jensen; Michael Schlicht; Robert Muller
Cc: Alan Massaro; Kim Johnson; Kass Giusti; Agajan Suwhanov; Dan Hegsted; Verne Hornback; Ken Fuchs; Michael Tedeschi; Miroslav Hora; Patrice Delpy; Alexandre Apcher; Catherine Goyon
Subject: RE: GAN18505.1 - unusual PC-Test data

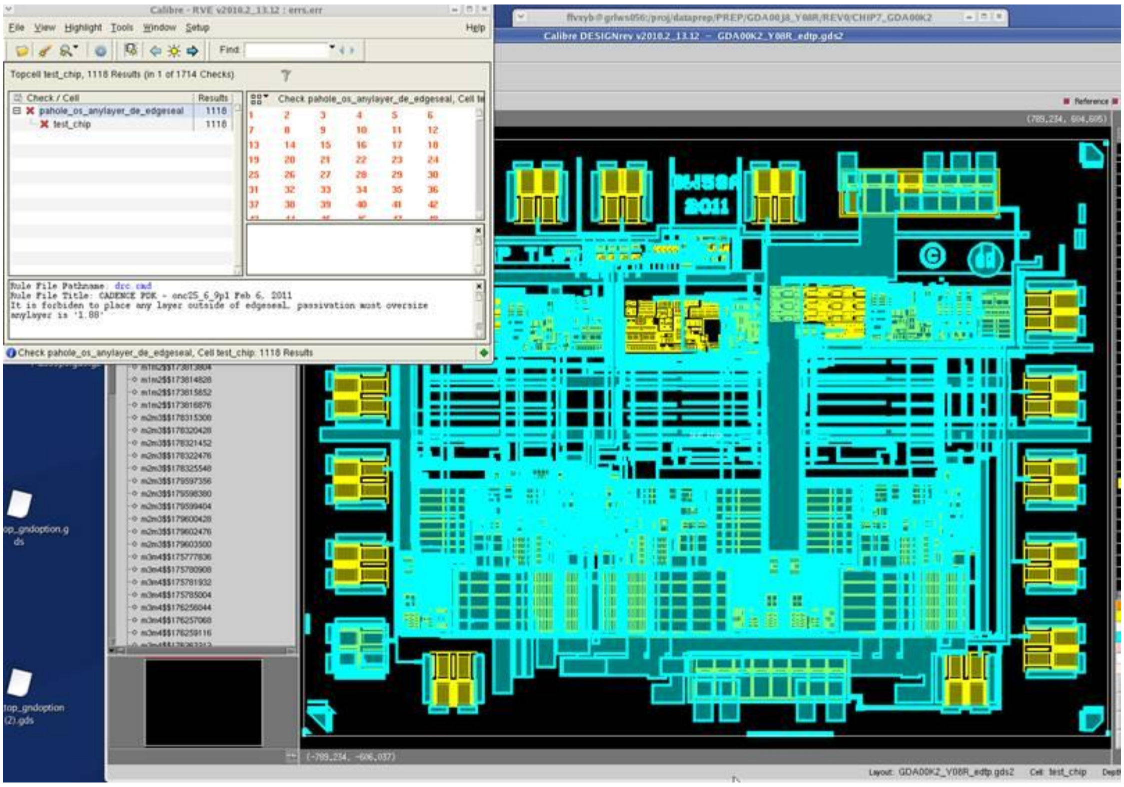
Mirek,

The DRC check below is intended to verify that ONC25 edgeseal exists, correct? If not, we need to create a check to verify that edgeseal is part of a product.

Patrice,

Can you explain the reasoning for using a non-standard edgeseal on NCP2815_Test chip 1 GDA00K2 Y08R? What was created is shorting the production PC-Test electrical monitors.

David Price



Topcell test_chip, 1118 Results (in 1 of 1714 Checks)

Check / Cell	Results
pahole_os_anylayer_de_edgeseal	1118
test_chip	1118

```
Rule File Pathname: drc.cmd
Rule File Title: CADENCE PDK - onc25_6_9p1 Feb 6, 2011
It is forbiden to place any layer outside of edgeseal. passivation must oversize
anylayer is '1.88'
```

Check pahole_os_anylayer_de_edgeseal, Cell test_chip: 1118 Results

From: John Jensen
Sent: Thursday, August 04, 2011 12:20 PM
To: Michael Schlicht; Robert Muller
Cc: Alan Massaro; Kim Johnson; Kass Giusti; Agajan Suwhanov; Dan Hegsted; Verne Hornback; David Price; Ken Fuchs
Subject: RE: GAN18505.1 - unusual PC-Test data

Mike,

The problem that you are seeing is the Y08R chip seems to have an edge seal that is not standard. When the process integration group had the PC-Test structures created they created them at 80 microns wide. The metal layers are allowed to run out to this width. They were depending on the die seal structure not to create shorts to the metal layers of the PC-Test structures. In the design kit seal ring the passivation defines the extent of the chip and the metal layers are a couple of microns in from there. In the case below the metal layers run all the way out to the extent of the chip.

When we run either a double wide scribe or an LVR type layout we assume the PC-Test structures are 85 microns wide not 80 so we do not produce shorts.

John

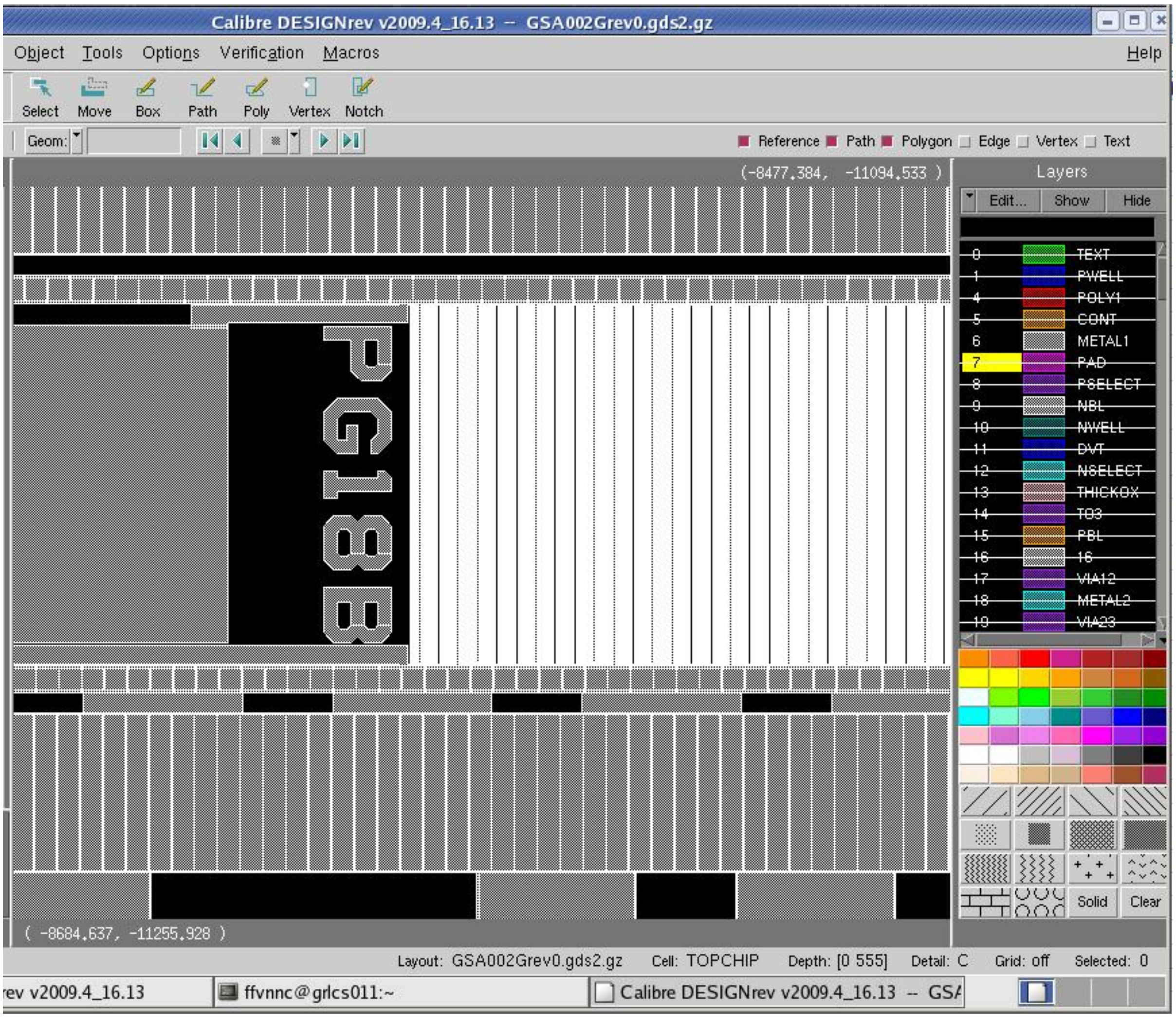
From: Michael Schlicht
Sent: Thursday, August 04, 2011 11:46 AM
To: John Jensen; Robert Muller
Cc: Alan Massaro; Kim Johnson; Kass Giusti; Agajan Suwhanov
Subject: RE: GAN18505.1 - unusual PC-Test data

Hello,

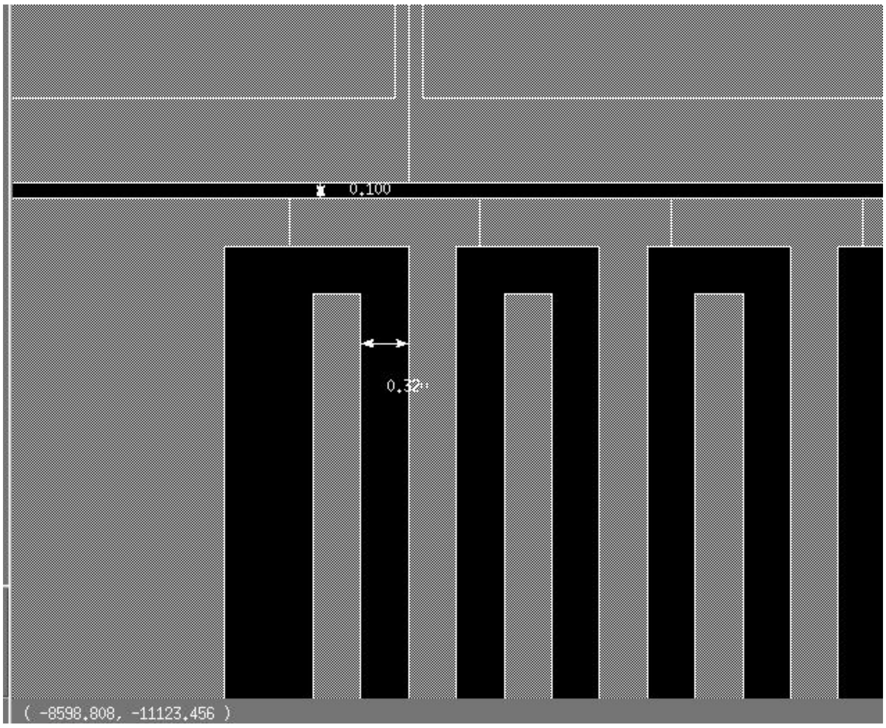
We seem to have a layout issue, with the placement of scribe line PCM structures in the Y08R reticle set. Y08R lots are failing all metal bridging & continuity tests, which are pad groups 18 & 19.

Reviewing the gds data shows sub-DR spacing alongside the m1comb (Metal 1 bridging) structure. The comb structure is fine (0.32um space) but alongside there is a 0.1um space.

Mike



Layout: GSA002Grev0.gds2.gz Cell: TOPCHIP Depth: [0 555] Detail: C Grid: off Selected: 0



From: Kim Johnson
Sent: Thursday, August 04, 2011 11:17 AM
To: Kass Giusti
Cc: Michael Schlicht; Alan Massaro
Subject: RE: GAN18505.1 - unusual PC-Test data

Kass,

Since this lot (wafers) failed M1B at M1 and EOL PC-Test (most likely different testers/probe card), the failure mode repeat and are real from a test perspective. It is odd that all of the metal bridging structures show railed leakage values. All of the continuity resistance tests are also shorted yielding railed results (to within the resolution of the tester). I think a review of the GDS for this product is in order.

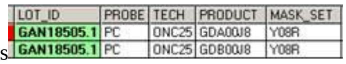
I can't comment more about these failures other than the above at this time. Let me know what you (or the team) finds out regarding these "failures"…

Best regards,

Kim

From: Kass Giusti
Sent: Thursday, August 04, 2011 10:58 AM
To: Kim Johnson
Cc: Michael Schlicht; Alan Massaro
Subject: GAN18505.1 - unusual PC-Test data

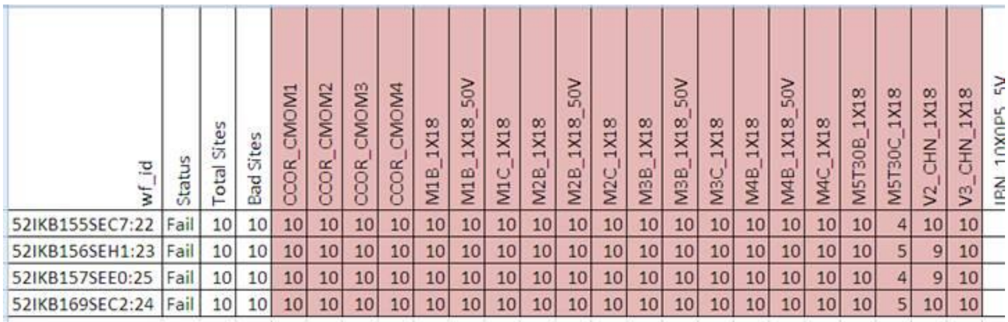
Hey Kim: I'm trying to figure out what's going on here. This lot is . We've not run this flavor of Y08R that I can see. The lot failed for M1C and M1B at Met1 and was sent on by Agajan.



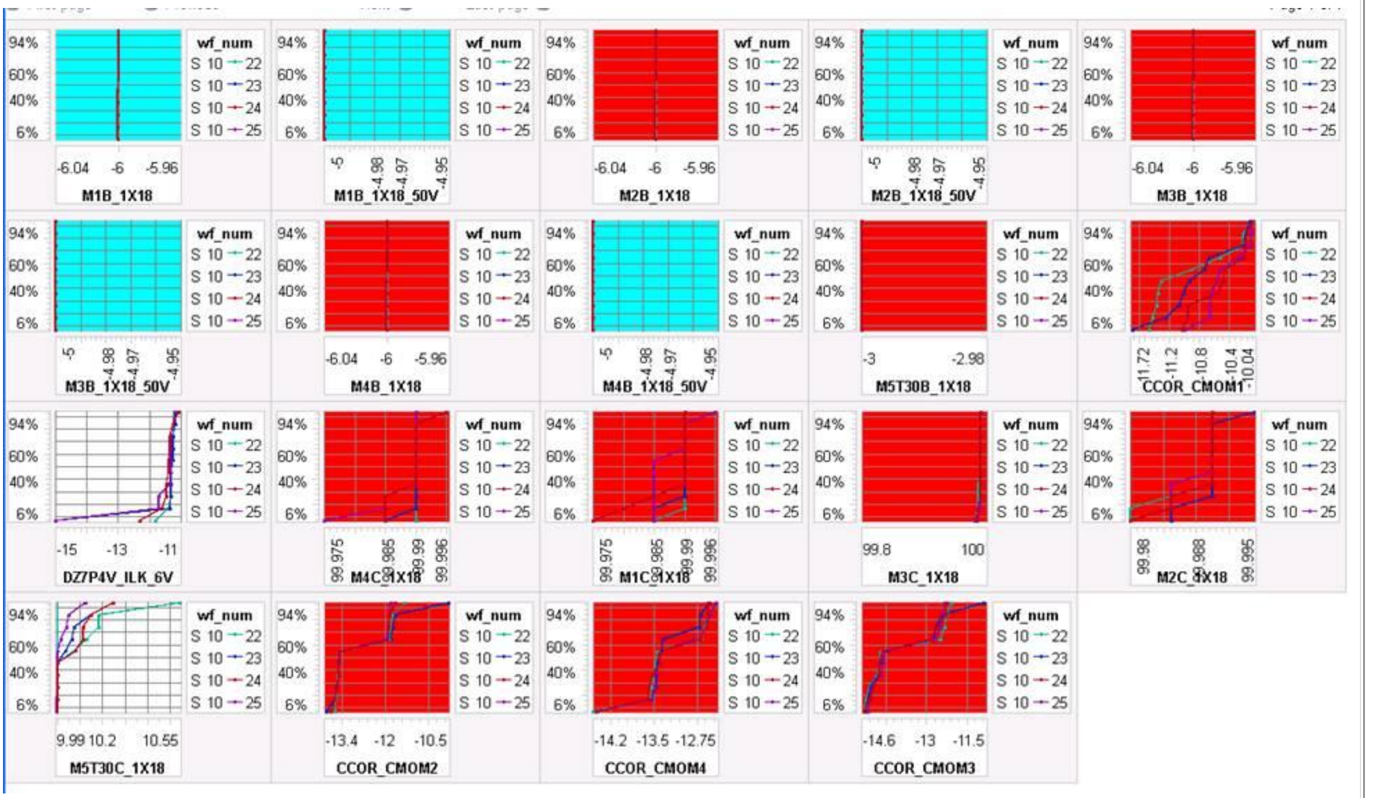
LOT_ID	PROBE	TECH	PRODUCT	MASK_SET
GAN18505.1	PC	ONC25	GDA00J8	Y08R
GAN18505.1	PC	ONC25	GDB00J8	Y08R

This is both std and rework. The only parameter that didn't have more fails with the rework map was M5T30C.

Can you shine any light on these for me? If we truly were bridged, the FE would have the same catastrophic fails – and it doesn't.



wf_id	Status	Total Sites	Bad Sites	CCOR_CMOM1	CCOR_CMOM2	CCOR_CMOM3	CCOR_CMOM4	M1B_1X18	M1B_1X18_50V	M1C_1X18	M2B_1X18	M2B_1X18_50V	M2C_1X18	M3B_1X18	M3B_1X18_50V	M3C_1X18	M4B_1X18	M4B_1X18_50V	M4C_1X18	M5T30B_1X18	M5T30C_1X18	V2_CHN_1X18	V3_CHN_1X18	IRN 10X0P5 5V
52IKB155SEC7:22	Fail	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	4	10	10	
52IKB156SEH1:23	Fail	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	5	9	10	
52IKB157SEE0:25	Fail	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	4	9	10	
52IKB169SEC2:24	Fail	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	5	10	10	



Kass Giusti

Device Engineering Technician

503-618-4265

✓ Accepter ? Provisoire ✗ Refuser | Calendrier... | | Fermer | Aide

De: Alexandre Apcher Date: mar. 15/03/2011 14:50

Requis: Patrice Delpy

Facultatif:

Ressources:

Objet : FW: RDL Issue

Emplacement : edison

Date: mardi 15 mars 2011 de 16:30 à 18:00

Pièces jointes :

Afficher sous forme de page Web

When: Tuesday, March 15, 2011 4:30 PM-6:00 PM (GMT+01:00) Amsterdam, Berlin, Bern, Rome, Stockholm, Vienna.

Where: edison

Note: The GMT offset above does not reflect daylight saving time adjustments.

~~*~*~*~*~*~*~*~*

-----Original Appointment-----
From: Alexandre Apcher
Sent: Monday, March 14, 2011 11:40 AM
To: ROOM FRTL1 EDISON; Vincent Teil; Stephane Colomines; Remy Saphon; Laurent Bordes; Bertrand Clou; Julien Clemens; Aurore Masson; Virginie Duchemann; Berengere Le Men
Cc: Geraldine Saint Upery
Subject: RDL Issue
When: Tuesday, March 15, 2011 4:30 PM-6:00 PM (GMT+01:00) Amsterdam, Berlin, Bern, Rome, Stockholm, Vienna.
Where: edison

Suite aux recents problemes de RDL (short entre PAD/ probleme de slot sous les PADs/ erreur dans le ball out due a la redistribution)

Petit point sur les outils&nethodes necessaires a une verification pertinente et fiable pour ne plus reproduire ce genre d'erreurs

Merci

Alexandre

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De: Berengere Le Men Date: lun. 18/04/2011 14:09
À: Marc Ryat; Catherine Goyon; Patrice Delpy; Alexandre Apcher
Cc:
Objet : RE: NCP2815 test chip
Pièces jointes :

Afficher sous forme de page Web

C’est le mask set bw58a, si je ne me trompe pas.

A+.

Berengere.

From: Marc Ryat
Sent: Monday, April 18, 2011 1:24 PM
To: Catherine Goyon; Berengere Le Men; Patrice Delpy; Alexandre Apcher
Subject: RE: NCP2815 test chip

j’ai oublie. Si quelqu’un sait, j’aimerais savoir.

Marc

From: Catherine Goyon
Sent: Monday, April 18, 2011 1:22 PM
To: Berengere Le Men; Marc Ryat; Patrice Delpy; Alexandre Apcher
Subject: NCP2815 test chip

Pouvez vous me rappeler quel était le nom de la test chip 2815 ?

Merci

Best regards,

Catherine Goyon

Program manager

Low Voltage Power Management New Product Development

ON Semiconductor France SAS

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BP 53512

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Tel : (33) (0)5 34 61 11 12 - **Cell** : 06 82 68 65 40 / 33 6 82 68 65 40

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