

**ECE 511
Analog Electronics**

Term Project

Fully Differential CMOS Amplifier

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Introduction

In this project, a fully differential CMOS operational amplifier was designed with Cadence 2005 using a 0.18 μ m GPDK process. The supply voltage is a 1.8 V source with no variation. The op-amp was specified to meet several specifications over process variations that include slow-slow, slow-fast, fast-slow, and fast-fast for pmos and nmos transistors. A folded cascode stage with an nmos driven common source amplifier output stage was used that met all the specifications except for the settling time. Process corner simulations showed a dramatic decrease in performance, including a catastrophic failure for the slow-slow corner. This paper discusses the design approach, frequency response and time domain simulation results, rejection ratio performance for common mode and power supply, and closes with a retrospective look at lessons learned and ways to improve the operational amplifier design.

Specifications Summary

Parameter	Specifications	Nominal Compliance	Marginal Worst Case	Absolute Worst Case
Corner	-	NN	SF	SS
LF Gain	80 dB	98.32 dB	79.84 dB	-0.197 dB
0dB BW*	160 MHz	235.03 MHz	141.1 MHz	N/A
Phase Margin*	55°	79.19°	82.5°	N/A
Settling Time*	10 ns	63.13 ns	160.12 ns	N/A
Output Swing	± 0.6 V	± 0.84	± 0.81	N/A
CMRR	> 50 dB	189.1 dB	189.59 dB	189.10 dB
PSRR	> 50 dB	170.27 dB	178.1 dB	170.27 dB
Supply Voltage	+1.8 V	-	-	-
Technology	0.18 μ m CMOS	-	-	-

Table 1 – Specifications summary. (*with 4pF load)

Design Approach

Topology – Fully Differential Folded Cascode with Common Source Output Stage Configuration

The first configuration implemented was a pmos differential pair with nmos load with a tail current source with each leg of the differential pair driving an nmos driven common source amplifier. Extensive theoretical design analysis did not translate into simulation success, and much difficulty was encountered in biasing the circuit properly. The second and final approach was a folded cascode first stage with pmos differential pair input driving an nmos driven common source with pmos load output stage. The slew rate of the op-amp in this case is proportional to the overdrive of the input stage, and for a given bias current a pmos will provide a greater overdrive.¹ For a common mode input, the current in the tail is split evenly between the two legs of the differential pair. This halved tail current is summed with the current through the pmos load (P3,P3a,P4,P4a) of the cascode stage and should equal the drain current of the bottom nmos (N11-12) transistors. The pmos load current was arbitrarily set to 100 μ A and the bottom nmos transistors were designed to provide 400 μ A of drain current. As a result, 300 μ A would flow in each leg of the differential pair thus requiring a 600 μ A tail current source. For matched pmos load transistors, this mandated the W/L ratio for the tail source to be six times the W/L of the pmos load, for the same bias voltage.

The specifications required an output swing of ± 0.6 V for each output, which translates to a 1.2 V_{p-p} single-ended output. To achieve this output swing, the common mode output voltage was designed to be 0.9 V, so the output could swing up to 1.5 V and down to 0.3 V. The folded cascode stage was designed to also have a common mode output voltage of 0.9 V. To achieve this headroom, the total overdrive voltages for the bottom two nmos and the top two nmos were designed to be 0.3 V, respectively. The common-source output stage was added later, and was also designed to have a common mode output voltage of 0.9 V. Fine tuning of the W/L ratios and the common mode input level (set to 0.699 V) was needed to precisely set the 0.9 V voltage.

¹ Johns & Martin. Analog Integrated Circuit Design. Wiley & Sons, Canada. © 1997. pgs. 228-231.

Nominal simulations were run for the folded cascode stage and showed a gain of 75 dB. The addition of the common source output stage increased the nominal gain to 98 dB and extended the bandwidth, uncompensated, to above 250 MHz.

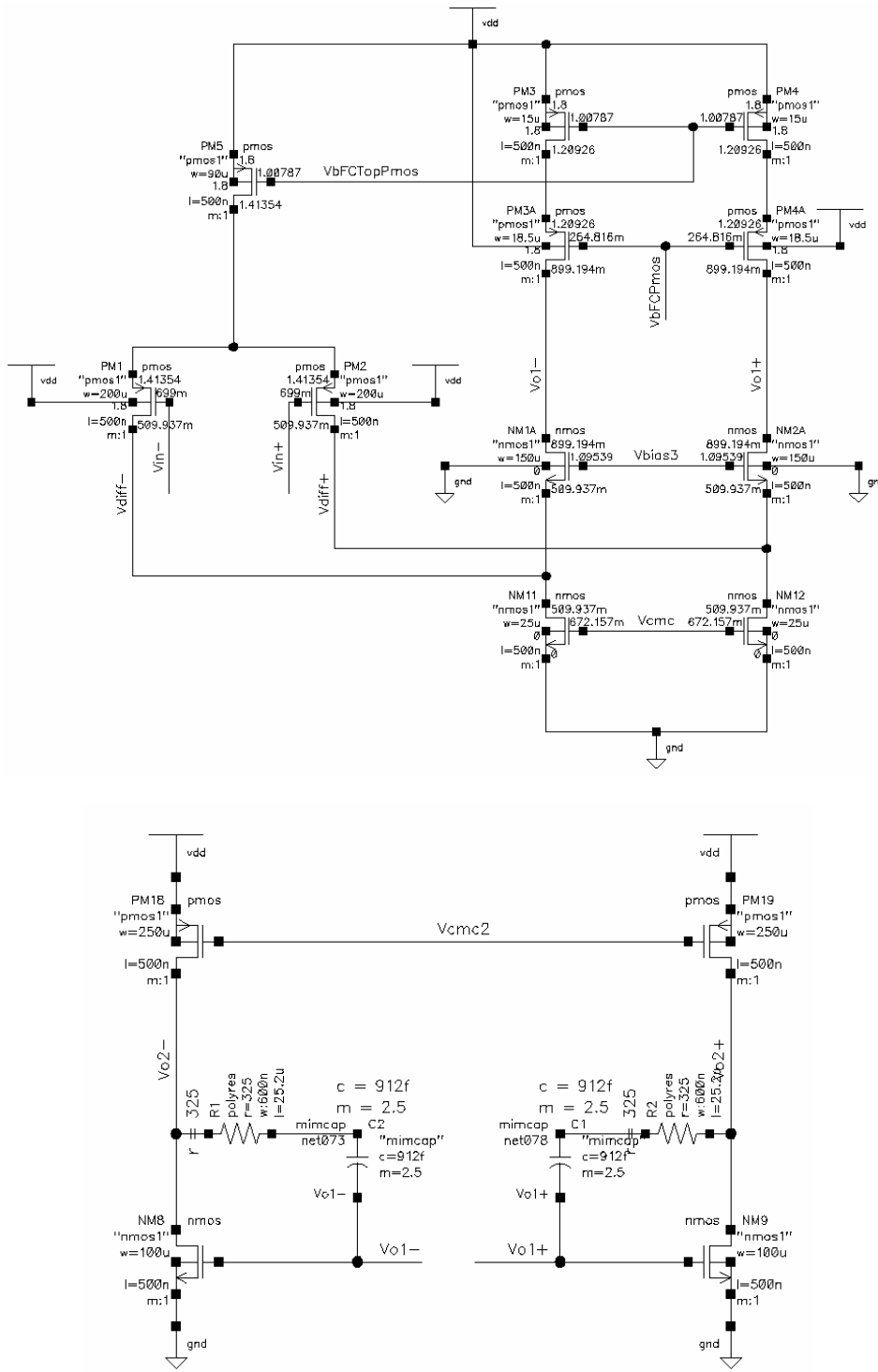


Figure 1 – Folded Cascode Input and Common Source Output Stage, Sizes. 4pF load not shown.

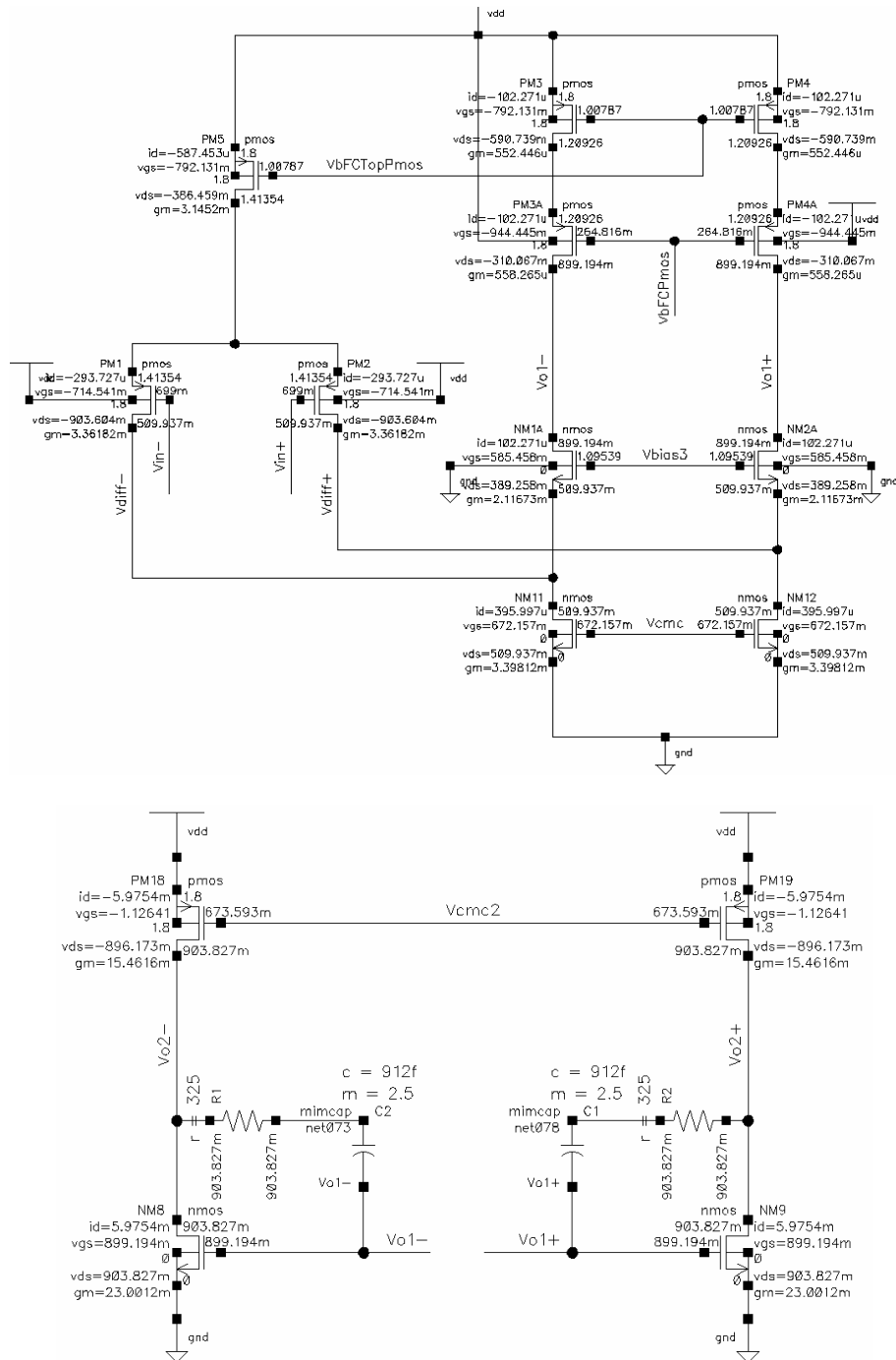


Figure 2 – Folded Cascode Input and Common Source Output Stage, DC operation points. 4pF load not shown.

Common Mode Feedback Circuits

Common mode feedback circuits were used to regulate the common mode outputs for the first and second stages. The dual differential pair sense amp configuration was used, with a diode connected nmos tail supplying the common mode control voltage to the bottom nmos transistors on the folded cascode. With P12-15 transistors matched, the current summed through N6 is proportional to the difference between the output voltages V_{o+} and V_{o-} and a desired common mode voltage, V_{CM} , set externally by a bias circuit. The common mode control voltage, V_{CMC} , is used to bias the N11-12 transistors at the bottom of the folded cascode stage.

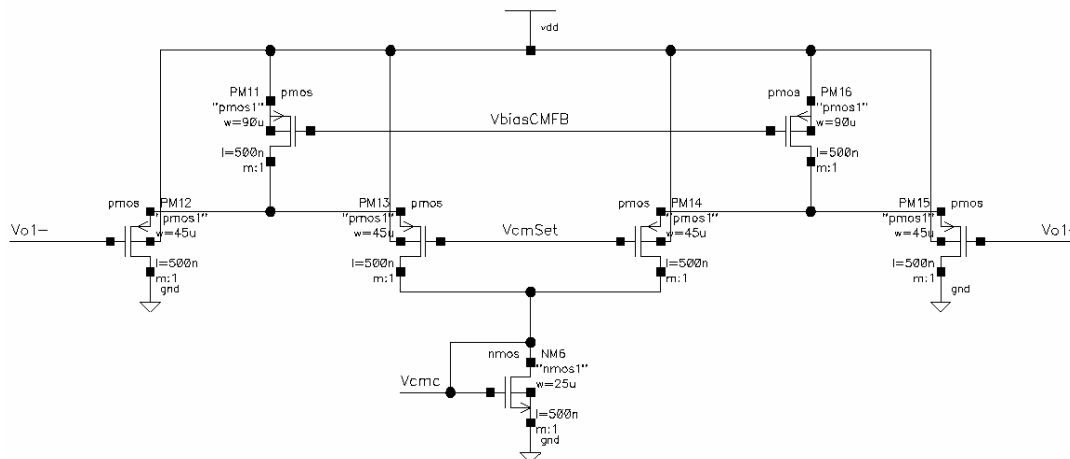


Figure 3 – Common Mode Feedback Circuit, Sizes

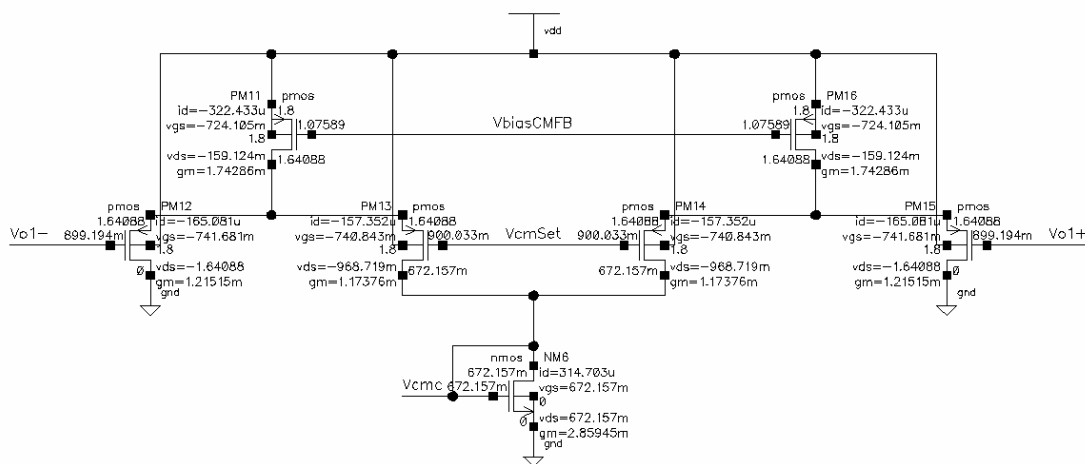


Figure 4 – Common Mode Feedback Circuit, DC operation points.

An identical common mode feedback circuit was used to provide CMFB for the output stage. Due to constraints and the need to eliminate an additional bias voltage generation, the bias for the pmos load was set to the same as before, approximately 0.672 V.

Compensation

The output of the second stage, $Vo2+$ and $Vo2-$, was compensated by a capacitor and resistor in series back to the output of the first stage, $Vo1+$ and $Vo1-$. The capacitor has the most notable effect on the frequency response. It shifts the dominant p_1 pole to the left and thus reduces the unity gain bandwidth slightly. The benefit can be seen in the phase margin. By increasing the distance between the dominant and non-dominant poles, the op-amp is able to achieve a constant phase margin for a wider bandwidth in the middle of its frequency response. Using the metal capacitor contained in the design kit the compensation capacitor, C_C , was arbitrarily set at $2.5 \cdot 912 \text{ fF} = 2.28 \text{ pF}$. Previous experience with compensation capacitors led to this judgment. Parametric analysis was used to identify the optimal compensation resistor, R_C , that would offset the decrease in phase caused by the non-dominant pole that lies just beyond the unity-gain frequency. For high values of R_C , the phase margin would begin to peak slightly near the unity-gain frequency. While this results in a higher phase margin in this narrow range of frequencies, it is undesirable because slight variations in the bandwidth can cause the opamp to quickly slide into instability. An R_C value of 325Ω was found to provide optimal results.

Bias Circuits

In the initial design, ideal voltage and current sources were used for biasing. The folded cascode has three bias voltages to set the currents in the cascode part, and the common mode feedback circuits require two bias voltages, one to set the current course and another precise bias voltage for the desired V_{CM} .

Once an acceptable nominal frequency response was attained², the ideal sources were substituted using a bias circuit network. A self-biasing V_T reference topology was used², with a 1k Ω poly resistor connected in series with an nmos to draw current from V_{DD} . The W/L ratios of the NM13-14 & PM27-28 transistors were set to keep all four transistors in saturation. Nmos and pmos transistors in a current mirror configuration (with a complementary diode connected loads) connected to N13 and P27, respectively, are used to generate the bias voltages by adjusting the W/L ratios.

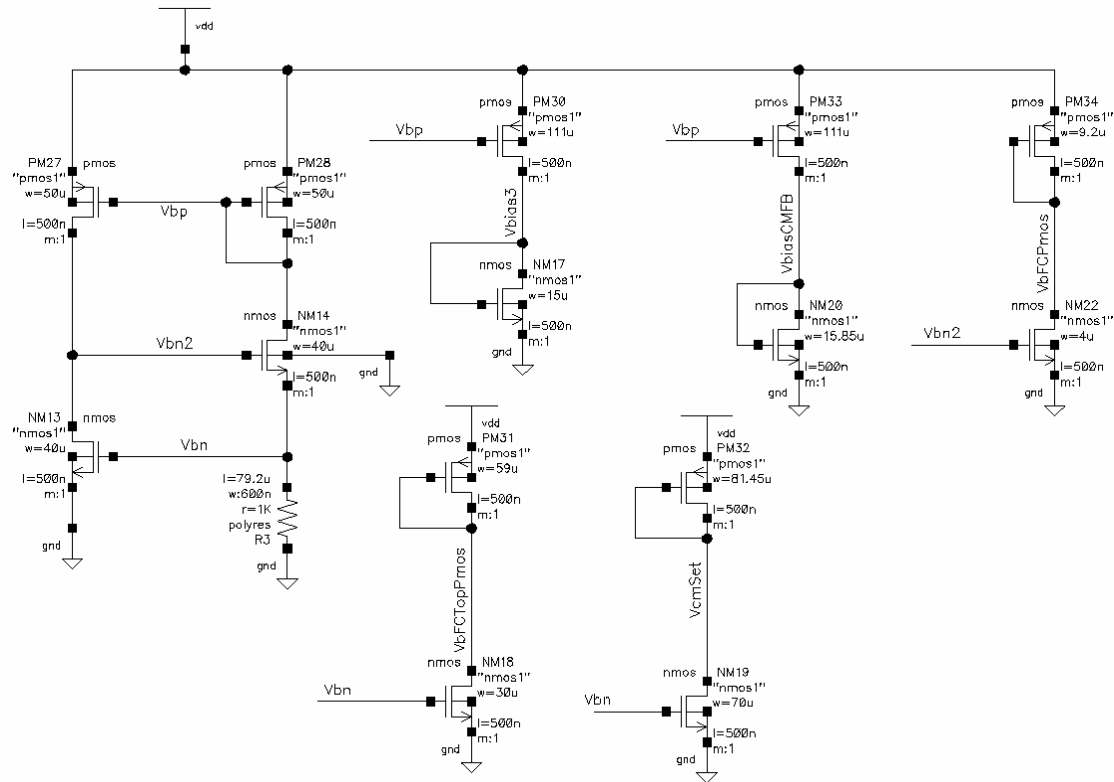


Figure 5 – Self-biasing V_T reference bias circuit, Sizes

² Gray Hurst Lewis Meyer, Analysis and Design of Integrated Analog Circuits, 4th edition. Wiley & Sons, New York:NY. © 2001. pg. 311.

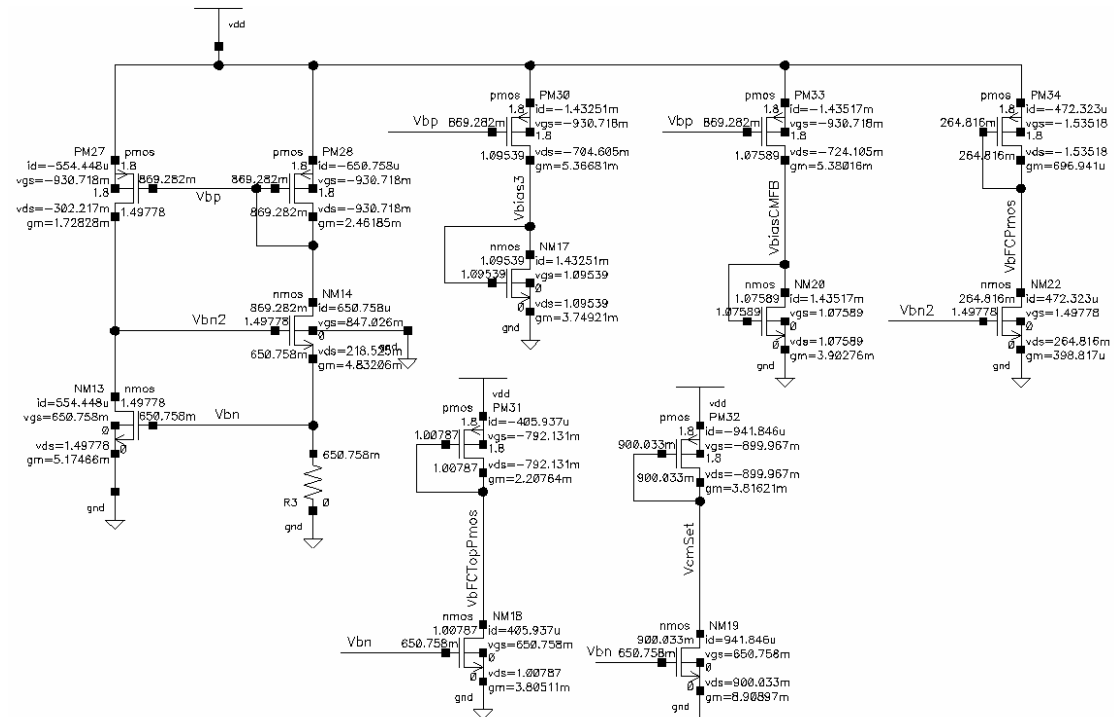


Figure 6 – Self-biasing V_T reference bias circuit, DC operating points.

Simulation Results

Frequency Response

The important frequency response related specifications are low frequency gain, the unity-gain bandwidth, and the phase margin. The gain and phase frequency response for the nominal process case demonstrated a low frequency gain of 98.32 dB, a unity-gain bandwidth of 235.03 MHz, and a phase margin of 79.19°. These surpass the specifications by 23%, 32%, and 44% respectively.

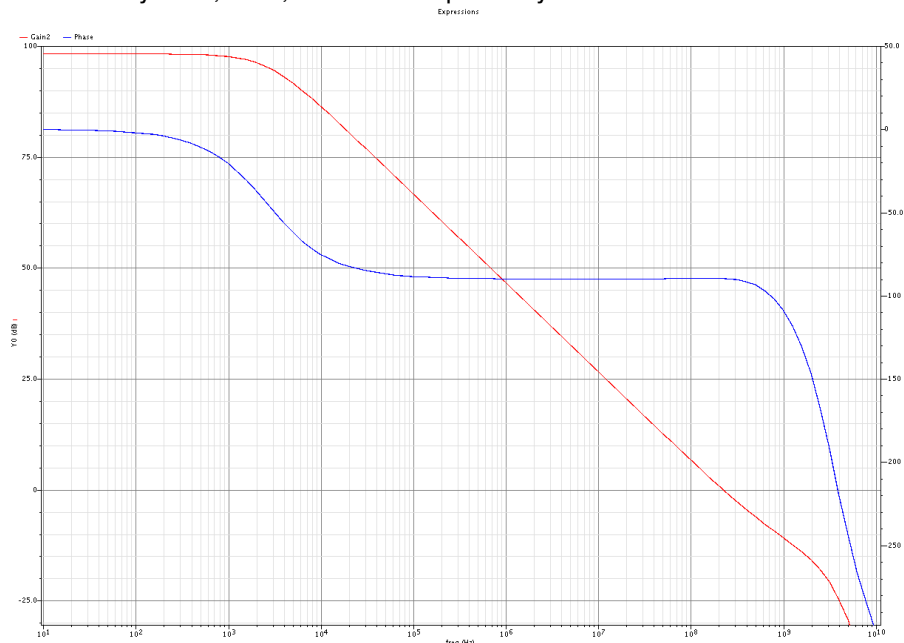


Figure 7 – Gain and Phase Frequency Response of Nominal Op-amp.

Process corner simulations revealed very different results.

Parameter	Specs	Process Corners Simulation Results				
		NN	SS	SF	FS	FF
Corner	-	NN	SS	SF	FS	FF
LF Gain	80 dB	98.32 dB	-0.197 dB	79.84 dB	76.36 dB	76.77 dB
0dB BW*	160 MHz	235.03 MHz	N/A	141.1 MHz	132.1 MHz	124.7 MHz
Phase Margin*	55°	79.19°	N/A	82.5°	89.9°	93.6°

Table 2 – Frequency Response Results, Nominal and Corner Simulations

First, it is revealed that the slow-slow process corner results in a catastrophic failure, effectively turning the entire op-amp off. The other process corners show substantial reductions in bandwidth, below the specifications, and a reduction in gain by almost 20 dB. This is likely occurring because the common mode feedback circuit for the common source output stage is failing due to current starvation. Unlike the folded cascode stage drawing 400 μ A, the output stage draws nearly 6 mA. The CMFB circuit can react accordingly due to improper biasing. This is causing the second stage to effectively turn off, dropping the gain and decreasing the bandwidth.

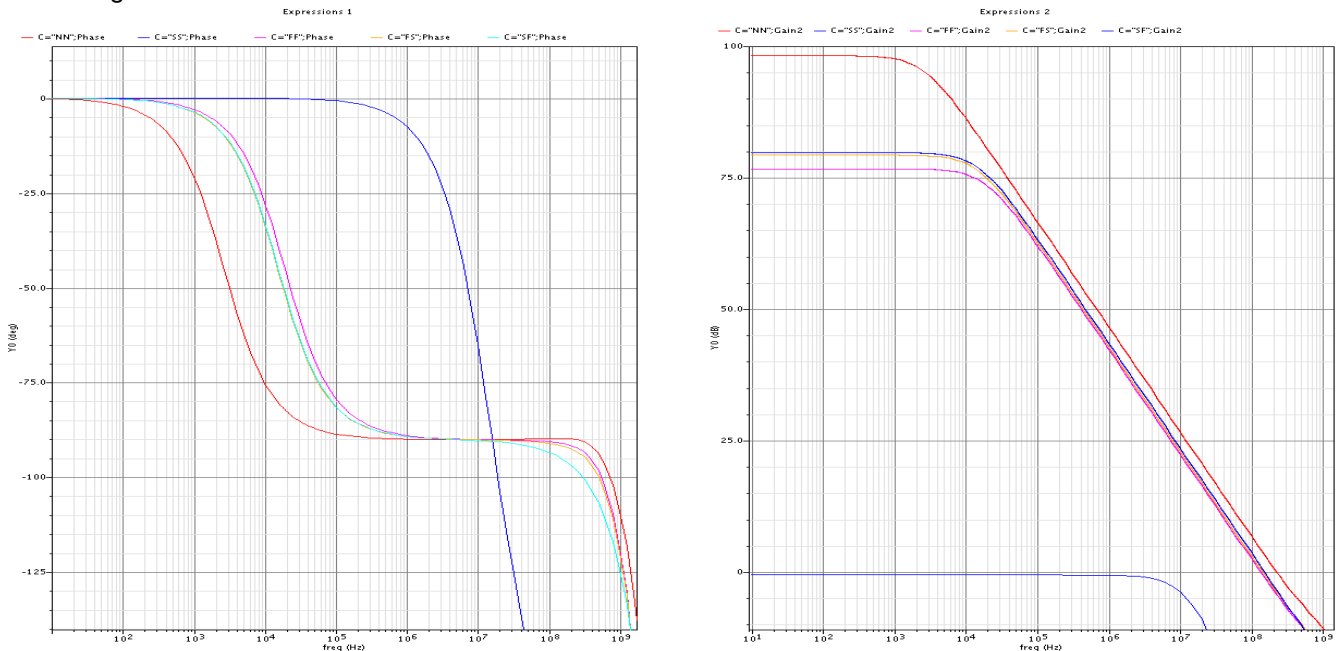


Figure 8 – Gain and Phase Frequency Response, Corner simulations. Red trace is always nominal. Dark blue is the slow-slow. Cyan is the slow-fast. Magenta is the fast-fast. Orange is the fast-slow.

CMRR & PSRR

The common mode rejection ratio is a measure of how sensitive the fully differential op-amp is to changing common mode input level. Ideally, changes in the common mode input should have no effect on the differential gain of the amplifier. The higher the common mode rejection ratio, the more effective it is. The common mode gain was measured by applying a 1 V AC signal with identical polarity to each input (in addition to the common mode input voltage) and then measuring the differential output gain. If the amplifier is perfectly balanced, each output should be amplified by the same amount and thus the difference should be zero. A graph of the CMRR corner simulations (including the nominal NN case) over the frequency range is shown below.

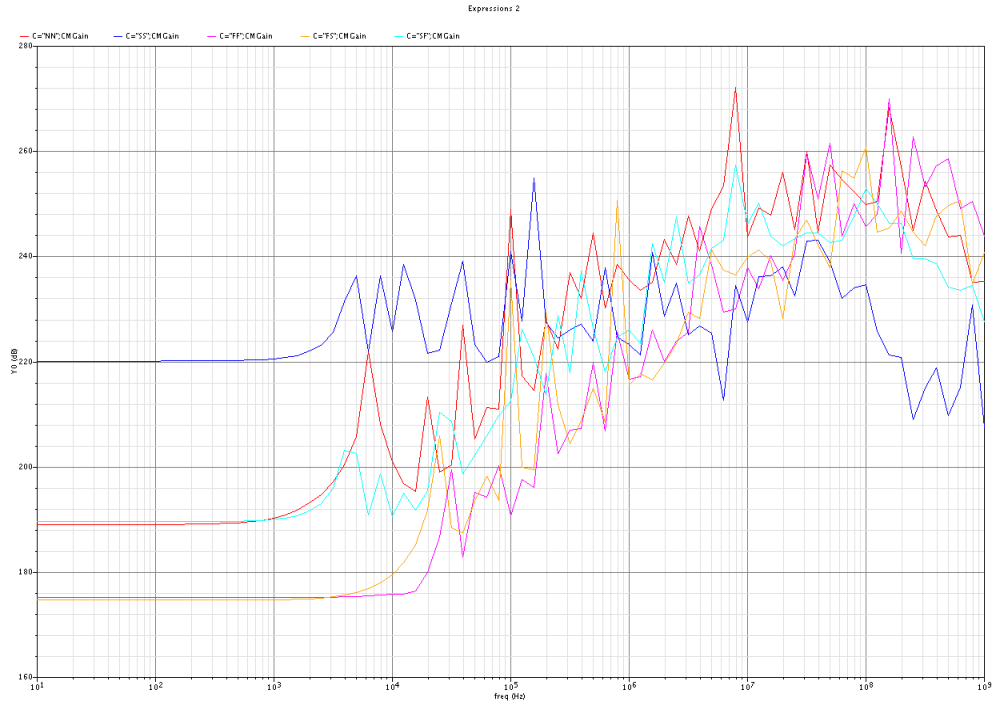


Figure 9 – Common Mode Rejection Ratio, Nominal and Corner simulations.

The power supply rejection ratio was measured by disabling all AC sources at the inputs, leaving just the common mode input voltage source. A 1V AC source was added in series with the 1.8V V_{DD} . Over a frequency sweep, the differential gain at the outputs (as a result of this power supply variation) was measured. Similar to the CMRR, the PSRR can be found by dividing the differential gain by the gain of the amplifier to the power supply ac signal. For an ideal op-amp, changes in the power supply have no effect on the output differential gain, so the higher the PSRR the better the op-amp performs. Process corners were run for PSRR and plotted in the graph below.

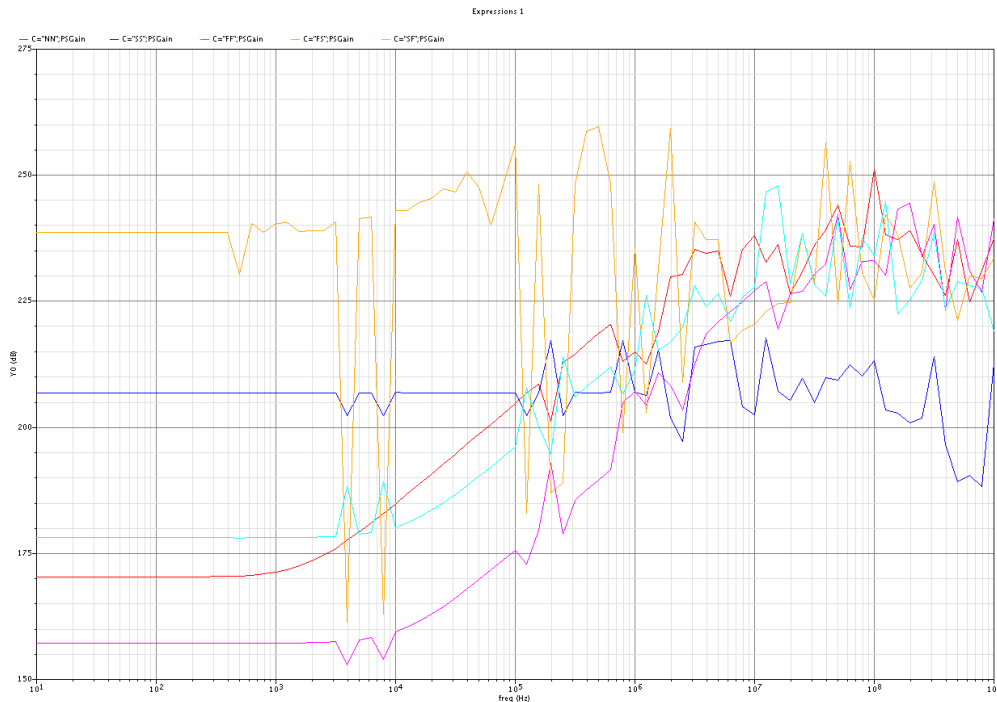


Figure 10 – Power Supply Rejection Ratio, Nominal and Corner simulations.

A summary of the CMRR and PSRR data for all the process corners is shown below.

Parameter	Specs	Process Corners Simulation Results				
		NN	SS	SF	FS	FF
Corner	-	NN	SS	SF	FS	FF
CMRR	> 50 dB	189.10 dB	N/A	189.59 dB	174.71 dB	175.20 dB
PSRR	> 50 dB	170.27 dB	N/A	178.10 dB	238.73 dB	157.15 dB

Table 3 – Rejection Ratio Results, Nominal and Corner Simulations

The amplifier significantly exceeded the specification of CMRR and PSRR being greater than 50 dB. The slow-slow corner has been excluded due to its catastrophic failure.

Output Swing

The output swing is simply a measure of the highest and lowest voltage the op-amp can output while keeping all its transistors in saturation. In series with the DC common mode input voltage, opposite polarity sinusoidal voltage sources with an amplitude of approximately 1 mV and a frequency of 100 Hz were placed at the V_{in+} and V_{in-} inputs. The differential output was measured and plotted from $0 < t < 50$ ms. Due to the gain of the amplifier being greater than 80 dB, a 1mV input signal will cause the amplifier to reach its maximum high and low output voltage. A sinusoidal output was not specified. The differential output $V_{P,P}$ was measured and divided by four to obtain the averaged output swing for each input, as it is noted in the specifications. The output swing of the nominal and the four non-catastrophic corners were well above the minimum specifications of ± 0.6 V. The course of simple common-source output stage aids affords a greater headroom compared with telescopic or cascoded output stages, where more than one transistor exists between ground and the V_{DD} rail. Process corners show similar results with little variation. None, except for the slow-slow corner, fail the specifications.

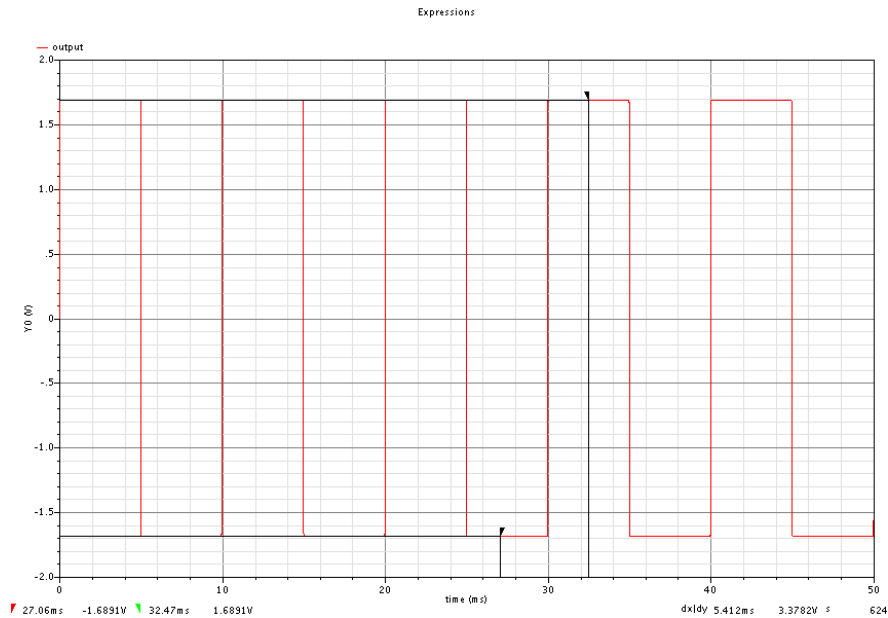


Figure 11 –Output Swing, Nominal simulation.

Settling Time

For settling time measurement, a closed loop configuration using resistors³ was used. In series with the common mode input voltage were reverse polarity pulsed voltage source that would output a differential step pulse (-0.6V to 0.6V). Simulation settings were adjusting to improve the accuracy of the time domain plot, and

³ Dr. K. Gard, ECE 511 Lecture Notes. Lecture 21. pg. 3-5.

the Cadence integration method of gear2 was used. Even for the nominal case, the settling time is well beyond the maximum stated in the specifics. The lowest settling time was achieved with the fast-fast corner, which had a settling time of 53.26 ns.

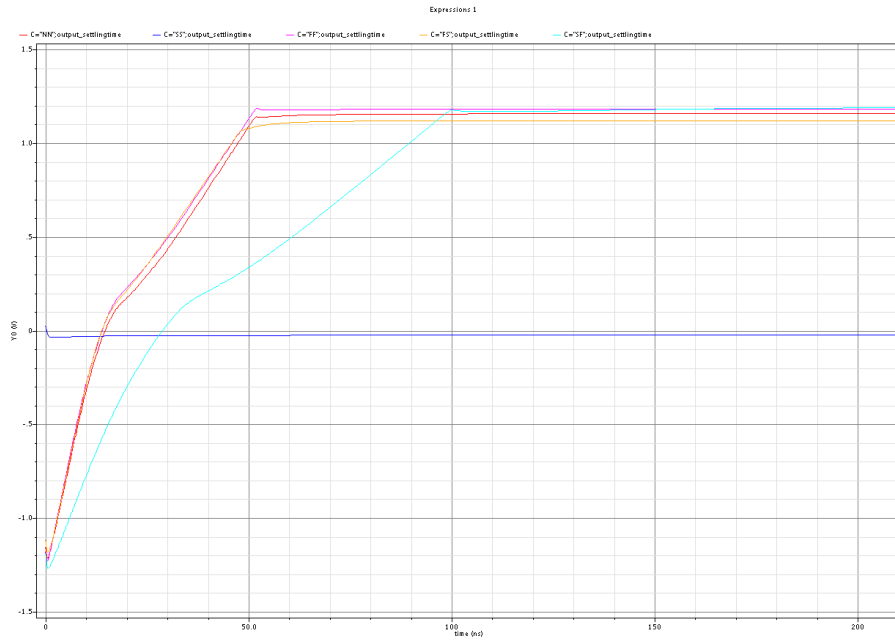


Figure 12 – Response to differential step input, Nominal and Corner simulation.

This long settling time is primarily due to the dominant pole, which is related to the size of C_C . With a specified phase margin of just 55° , a substantial amount of phase margin should have been traded for a smaller C_C . This would have slid the dominant f_{-3dB} dominant pole to the right, speeding up the settling time.

Parameter	Specs	Process Corners Simulation Results				
Corner	-	NN	SS	SF	FS	FF
Output Swing	± 0.6 V	± 0.84 V	N/A	± 0.81 V	± 0.861 V	± 0.837 V
Settling Time	< 10 ns	63.13 ns	N/A	160.12ns	72.925ns	58.257 ns

Table 4 – Transient Simulation Results, Nominal and Corner Simulations

Conclusion

Lessons Learned & Strategy for New Design

Over the course of the design process, several important lessons were learned. The common mode feedback circuit should be implemented very early on in the process, as it will aid in regulating the common mode voltage levels without requiring tedious adjustments of transistor sizes or bias voltages. As mentioned in an earlier section, using identical CMFB circuits for both the input and output stages was a critical error with severe and readily observable consequences. The importance of the overdrive voltages for each transistor is not to be understated. Fully understood only late into the process was the recognition that while it is clear that one should size and bias the transistors for a minimum V_{DS} voltage of approximately 0.1V to 0.15V (to allow for high output swing), this minimum stage need not to be sought after while identifying an appropriate common mode input level. Not only do small overdrives help increase headroom, they also improve gain, CMRR, and PSRR.⁴ These benefits come at the expense of the unity-gain bandwidth, so being cognizant of this trade off is important.

This project gave me new insights into practical circuit design, and observing the poor performance of my op-amp design has instilled a new sense of determination to improve my op-amp design with the knowledge and skills gained from this first effort.

⁴ Gray Hurst Lewis Meyer, Analysis and Design of Integrated Analog Circuits, 4th edition. Wiley & Sons, New York:NY. © 2001. pg. 439.