Operational Amplifier

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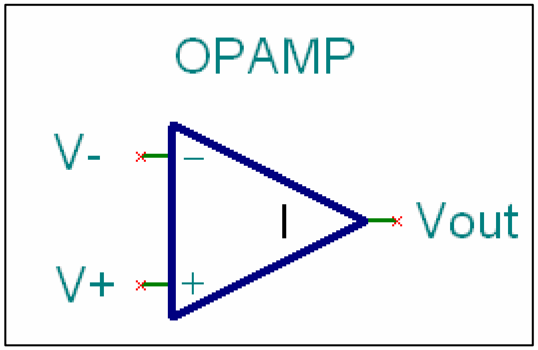
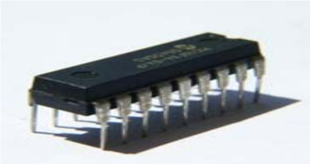


$$V_o = (A\,V_+ - A\,V_-)$$
$$= A\,(V_+ - V_-)$$

Basic and most common circuit building device. Ideally,

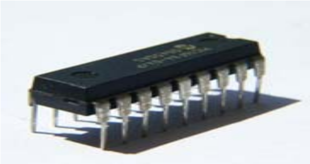
1. No current can enter terminals V_+ or V_-. Called *infinite input impedance*.
2. $V_{out}=A(V_+ - V_-)$ with $A \rightarrow \infty$
3. In a circuit V_+ is forced equal to V_-. This is the *virtual ground* property
4. An opamp needs two voltages to power it V_{cc} and $-V_{ee}$. These are called the *rails*.

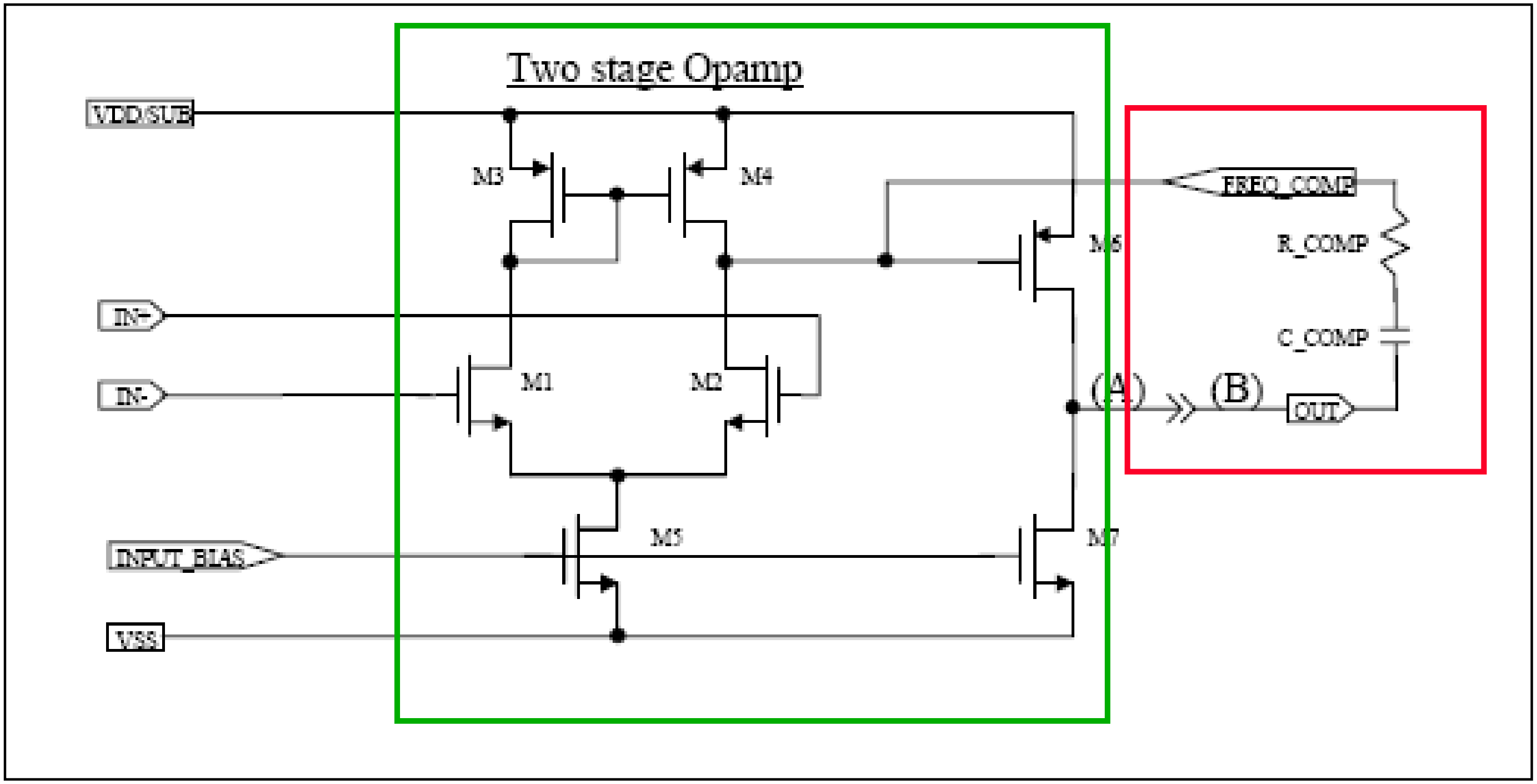
Opamp Preliminaries



- Differential Gain: Very High.
- Input Impedance: Very high.
- Output Impedance: Very Low.

Two Stage Opamp Schematic





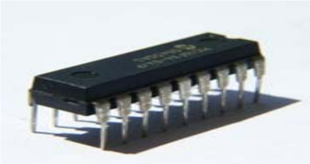
Calculation : Gain

First Stage Gain : $-g_{m1}(r_{o2}||r_{04})$

Second Stage Gain : $-g_{m5}(r_{05}||r_{06})$

Total Gain (A_v) :

$$g_{m1}\, g_{m5}(r_{05}||r_{06})(r_{o2}||r_{04})$$



Calculation : Poles

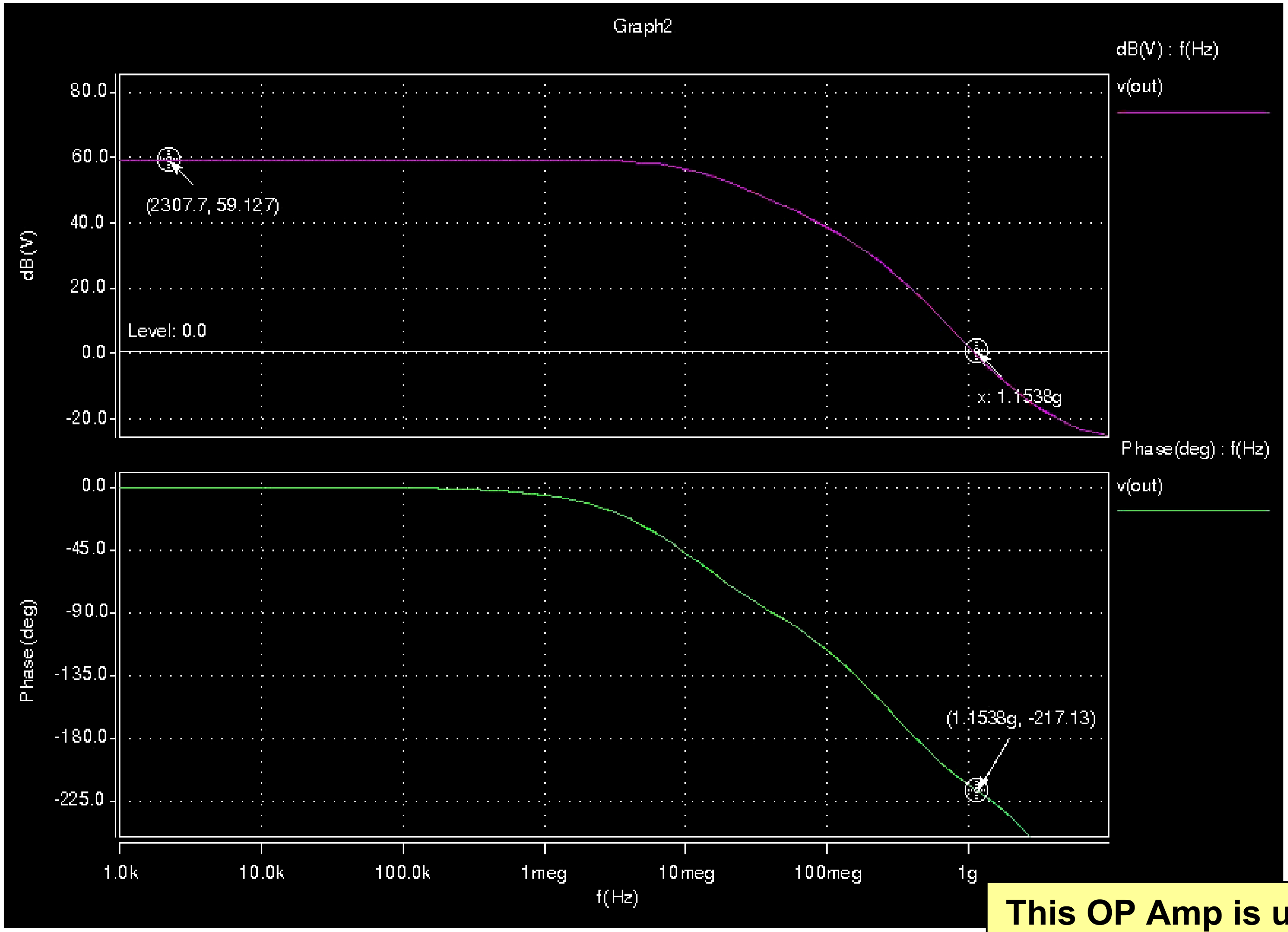
- **First Pole :**

$$p_1 = \frac{-1}{C_{load}(r_{05} \parallel r_{06})}$$

- **Second Pole :**

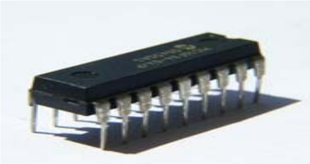
$$p_2 = \frac{-1}{C_{1stStage}(r_{02} \parallel r_{04})}$$

Simulation Results

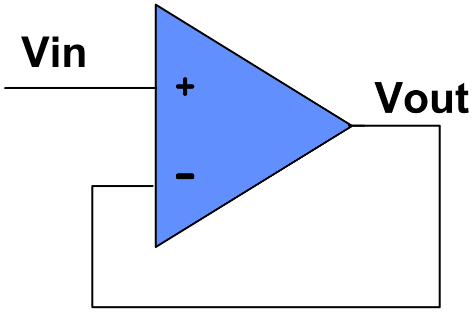


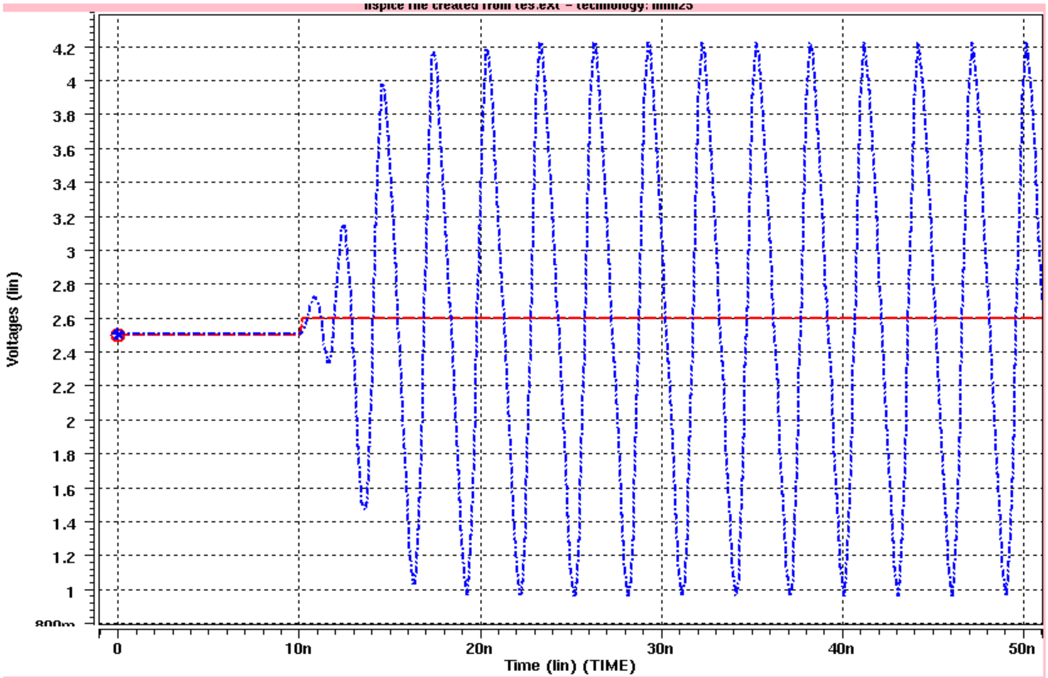
This OP Amp is unstable!

Without frequency compensation



- A unit gain buffer characteristic





Stability and Phase Margin

- Difference between actual phase shift when $|A_v|$ is 0dB and -180^0.
- Φ_M(Phase Margin)= $\Phi[A_v(\omega)]_{|A(v)|=1} = -180^0$
- For a stabe amplifier Φ_M is positive.
- For a good design Φ_M takes a value near 60^0.

Gain with Feedback

Closed Loop Transfer Function H(jw) =

$$\frac{A(j\omega)}{1 + A(j\omega)\beta(j\omega)}$$

System becomes unstable if denominator tends to zero.

Small Signal Dynamics

- *Note :* **The signal fedback to the input of the opamp be of such amplitude that it will not continue to regenerate itself around the loop. This causes**

- **Output clamping to one supply potentials.**
- **Oscillation (regeneration at some frq other than dc).**

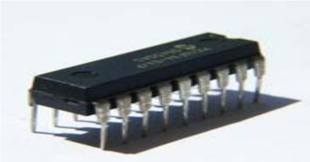
$$|A(j\omega_0)\beta(j\omega_0)| = |L(j\omega_0)| < 1$$

Where w_0 is defined by

$$\mathrm{Arg}[-A(j\omega_0)F(j\omega_0)] = 0^0$$

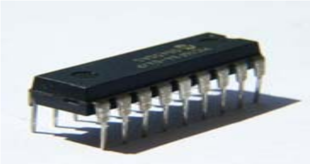
This one ensures stable closed loop operation

Compensation



- Compensation is a technique to modify an opamp for stabilization purpose.
- For stability, feedback signal should not regenerate itself around the loop. It will clamp the output to the power supply.
- For stability $Arg[A(j\omega_0)\beta(j\omega_0)] < 180^0$.
- ω_0 is defined by $A(j\omega_0)\beta(j\omega_0) = 1$

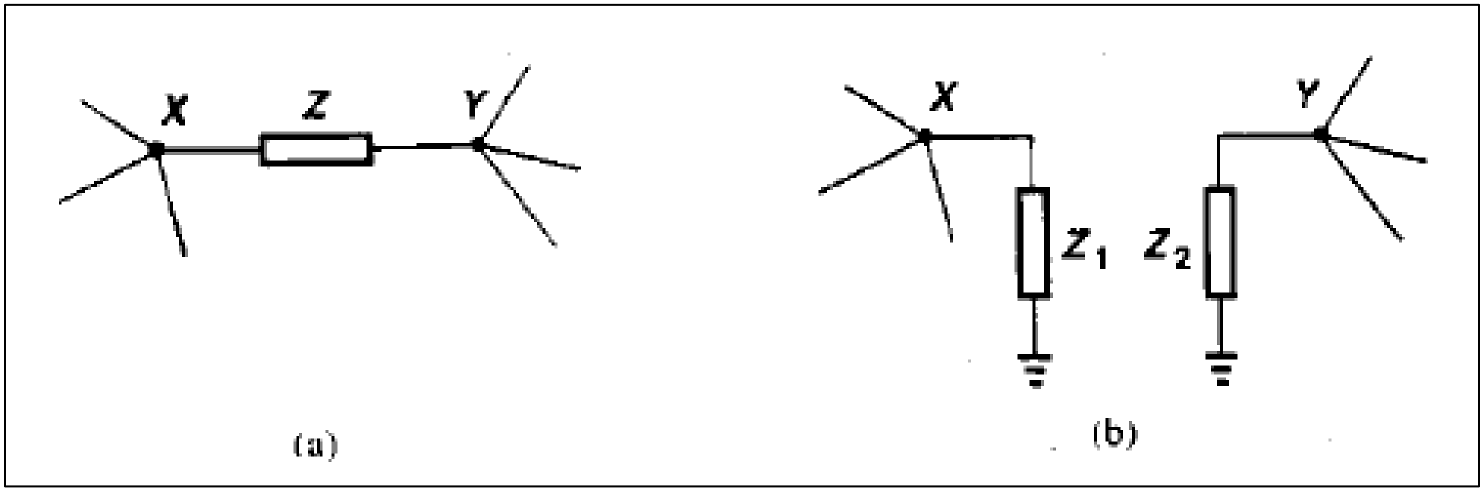
Compensation Technique



- **Pole Splitting : Split the poles far apart so that one of them becomes sufficiently dominant and other moves to near the BW frequency. Hence at Gain=0dB Φ_M is sufficiently high.**

Pole Splitting : Miller's Theorem

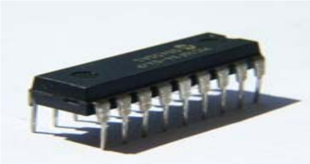
- If the circuit of the figure in (a) can be converted to figure in (b)



- Then $Z_1 = \dfrac{Z}{1 - A_V}$ and $Z_2 = \dfrac{Z}{(1 - \frac{1}{A_V})}$

- where $A_V = \dfrac{V_Y}{V_X}$

Results of Compensation



- $A = V_0/V_2$

  $= - G_{m2}R_{02}$

Applying Miller's Theorem we get

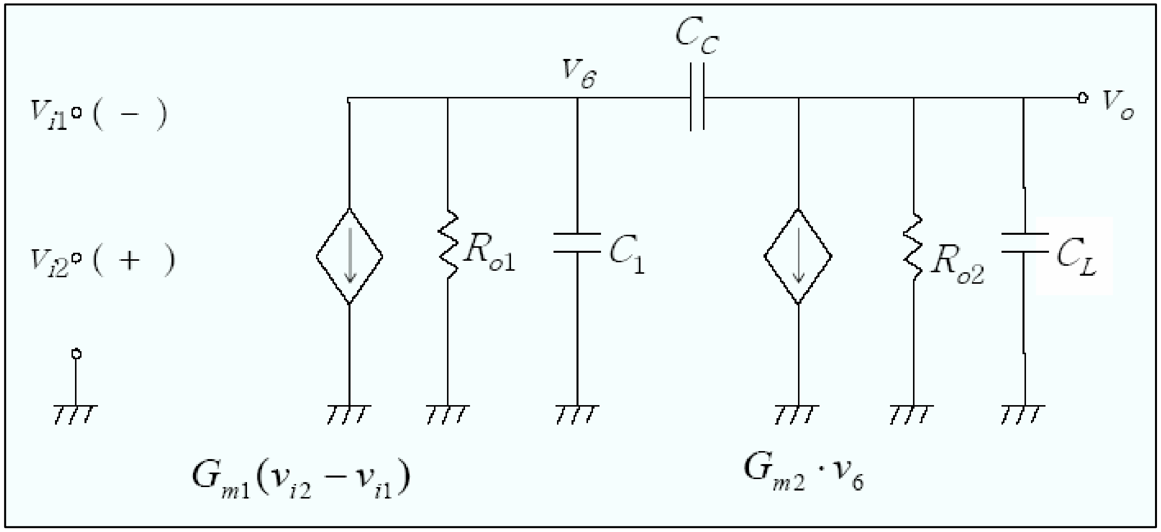
$C_{1eff} = C_1 + C_c(1-A)$

$= C_c G_{m2} R_{02}$

$C_{2eff} = C_2 + C_c(1-A^{-1})$

$= C_2 + C_c$ (approx)

Small Signal Model



KCL at v6 and vo nodes

$$G_{m1} \cdot (v_{i2} - v_{i1}) + \left\{ s(C_1 + C_C) + \frac{1}{R_{o1}} \right\} \cdot v_6 - sC_C \cdot v_o = 0$$

$$(G_{m2} - sC_C) \cdot v_6 + \left\{ s(C_L + C_C) + \frac{1}{R_{o2}} \right\} \cdot v_o = 0$$

Small Signal Model (Continued)

$$A_{dv}(s)=\frac{v_o}{v_{i2}-v_{i1}}=\frac{(G_{m1}R_{o1})\cdot(G_{m2}R_{o2})\cdot(1-sC_C/G_{m2})}{\begin{bmatrix}1+s\cdot\{C_LR_{o2}+C_1R_{o1}+C_C\cdot(G_{m2}R_{o2}R_{o1}+R_{o1}+R_{o2})\}\\ +s^2\cdot\{C_1C_L+(C_1+C_L)C_C\}\cdot R_{o1}R_{o2}\end{bmatrix}}$$

$$A_{dv}(s)=\frac{A_{dv}(0)\cdot\left(1-\frac{s}{z_1}\right)}{\left(1-\frac{s}{p_1}\right)\cdot\left(1-\frac{s}{p_2}\right)}\approx\frac{A_{dv}(0)\cdot\left(1-\frac{s}{z_1}\right)}{1-\frac{s}{p_1}+\frac{s^2}{p_1p_2}}$$

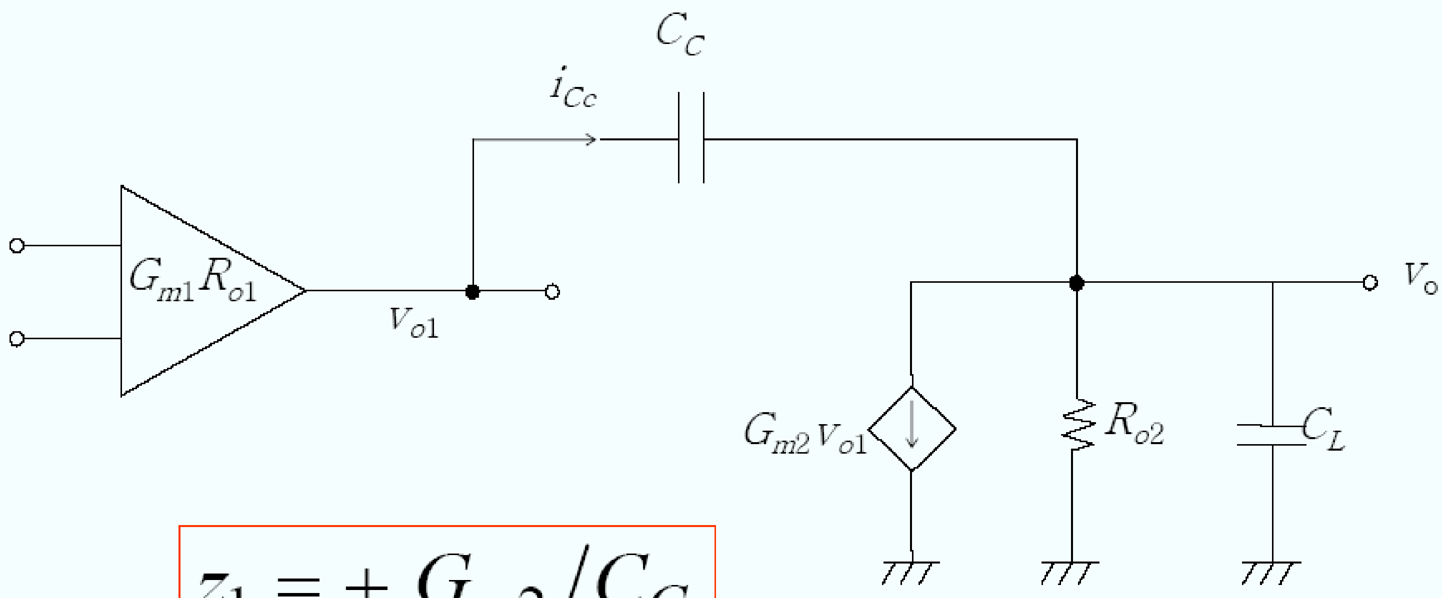
Dominant pole approximation: $|p_1|<<|p_2|$

$$p_1=\frac{-1}{C_C\cdot(G_{m2}R_{o2}R_{o1}+R_{o1}+R_{o2})+C_LR_{o2}+C_1R_{o1}}\approx\frac{-1}{R_{o1}\cdot G_{m2}R_{o2}\cdot C_C}$$

$$p_2=\frac{+1}{p_1\cdot\{C_C(C_1+C_L)+C_1C_L\}R_{o1}R_{o2}}=\frac{-G_{m2}C_C}{C_C(C_1+C_L)+C_1C_L}$$

Positive Zero & Pole-Zero Cancellation

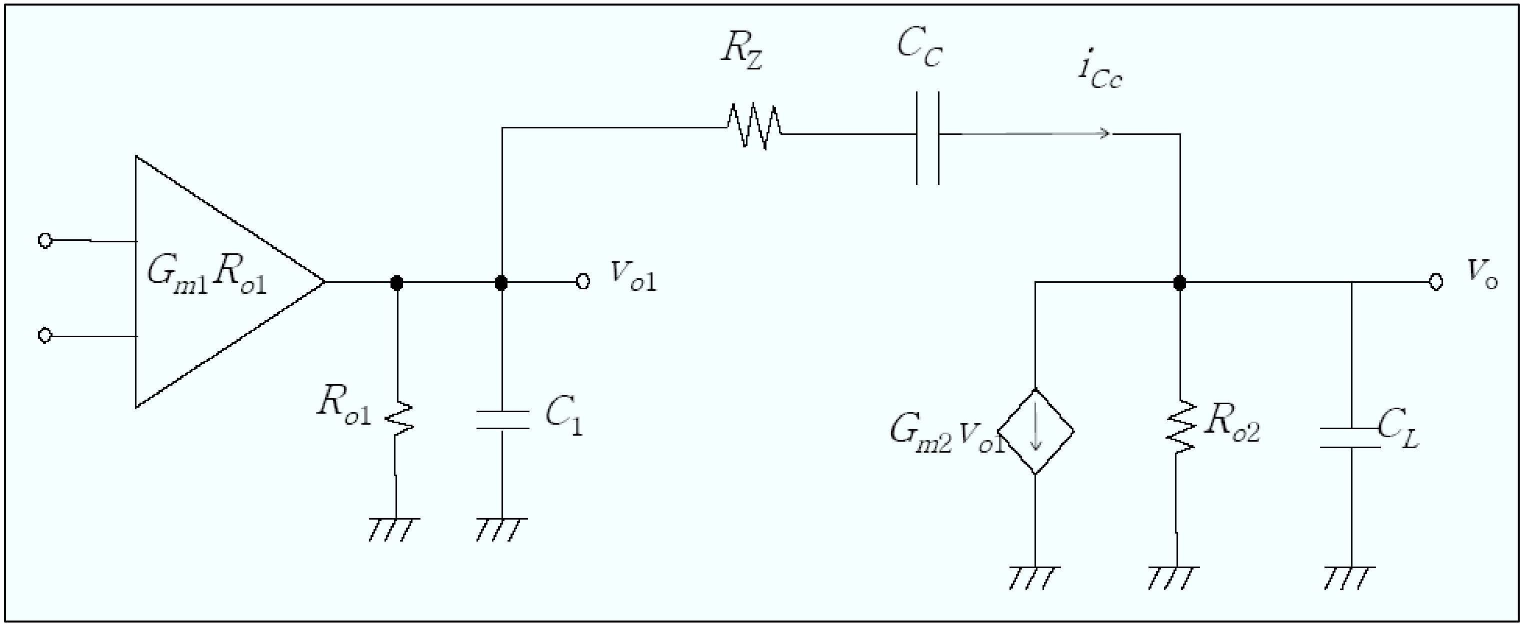
❑ Feed Forward



$$z_1 = +\, G_{m2} / C_C$$

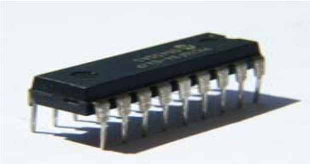
Positive Zero & Pole-Zero Cancellation

❑ Pole-Zero Cancellation



$$z_1 = \frac{G_{m2}}{C_C} \cdot \frac{1}{1 - G_{m2} \cdot R_Z}$$

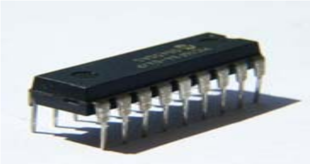
Positive Zero & Pole-Zero Cancellation (contd)

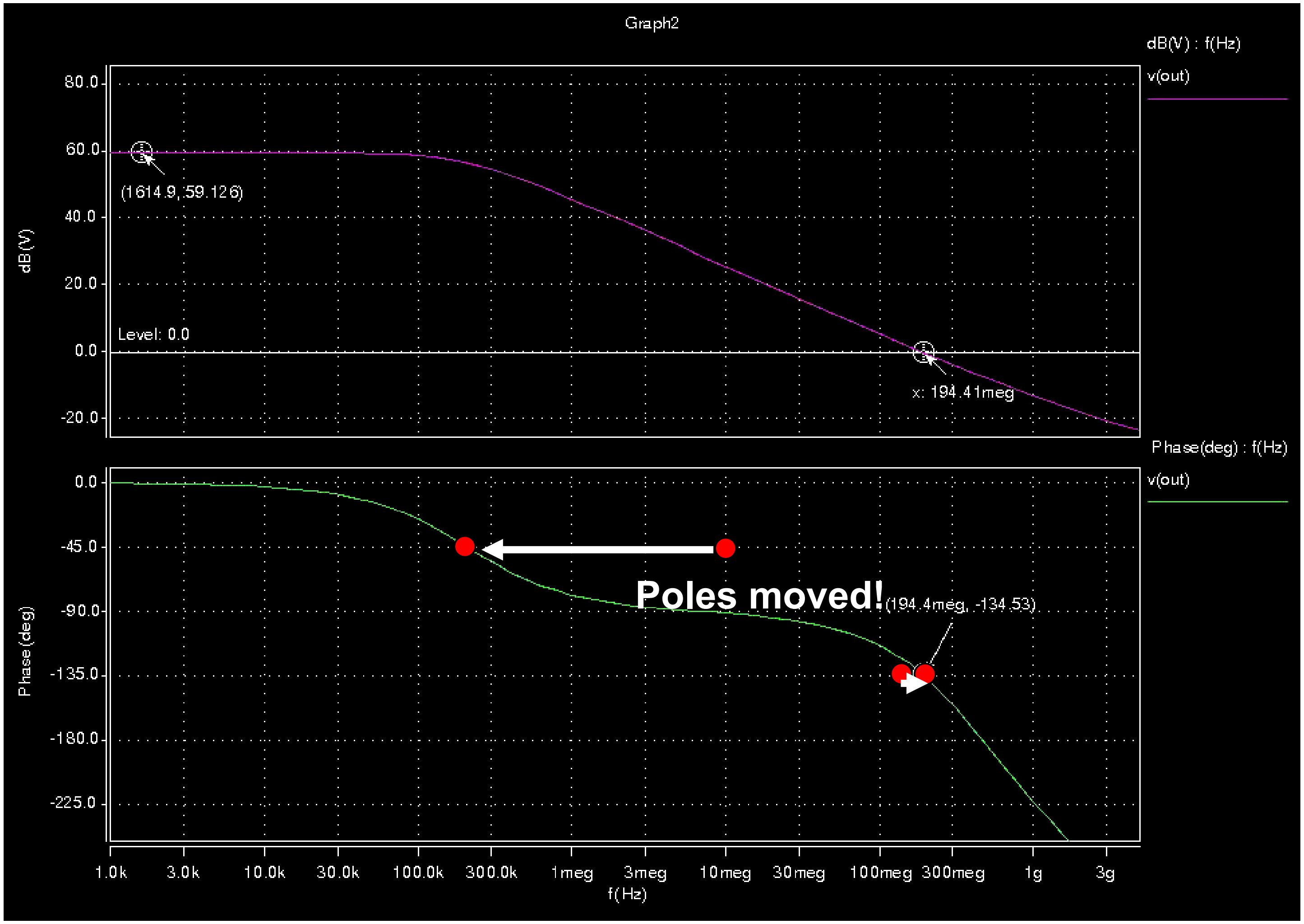


$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a[1 - s\{\frac{C_C}{G_{m2}} - R_z C_c\}]}{1 + bs + cs^2 + ds^3}$$

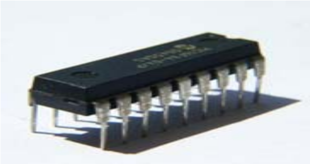
The resistor R_z allows independent control over placement of zero.

An Example of Frequency Compensation

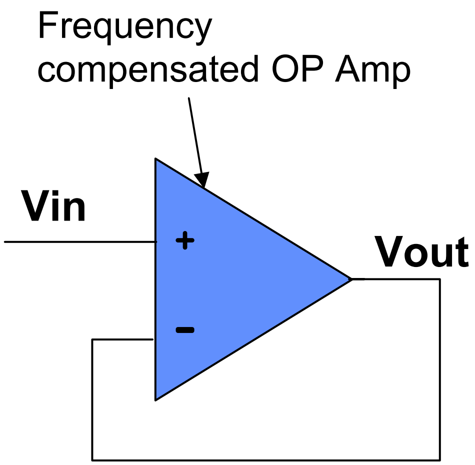


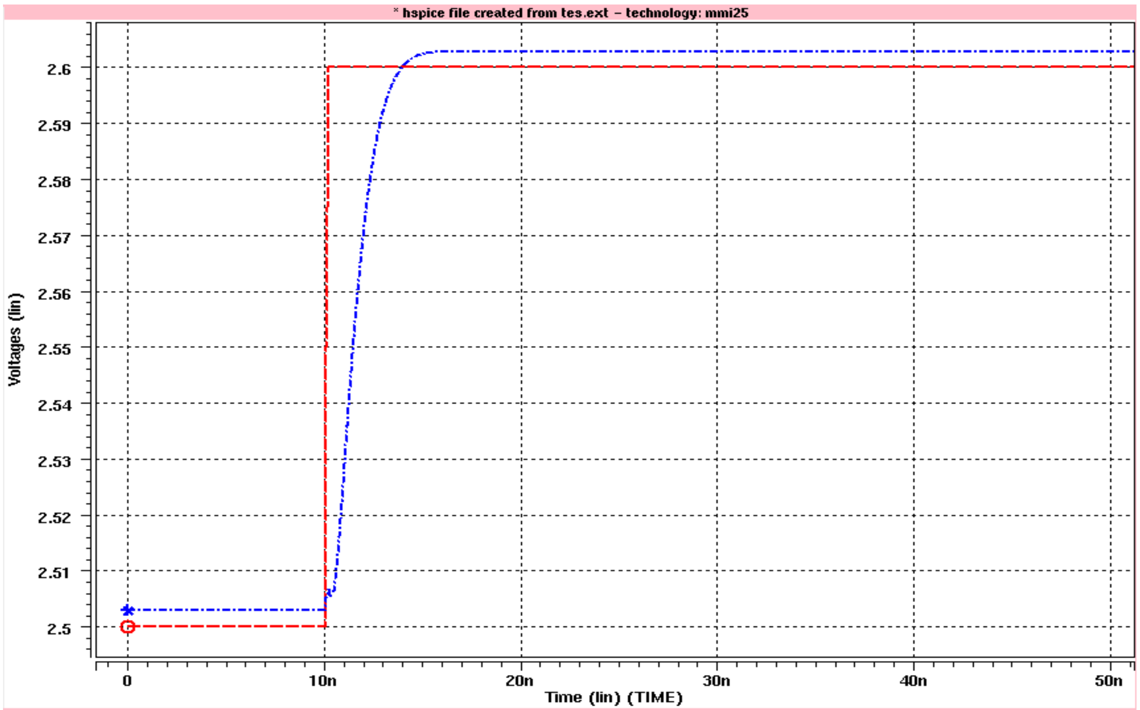


After Frequency Compensation



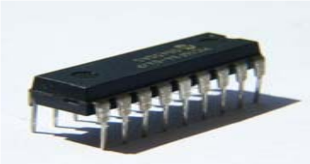
- A unit gain buffer characteristic with frequency compensation

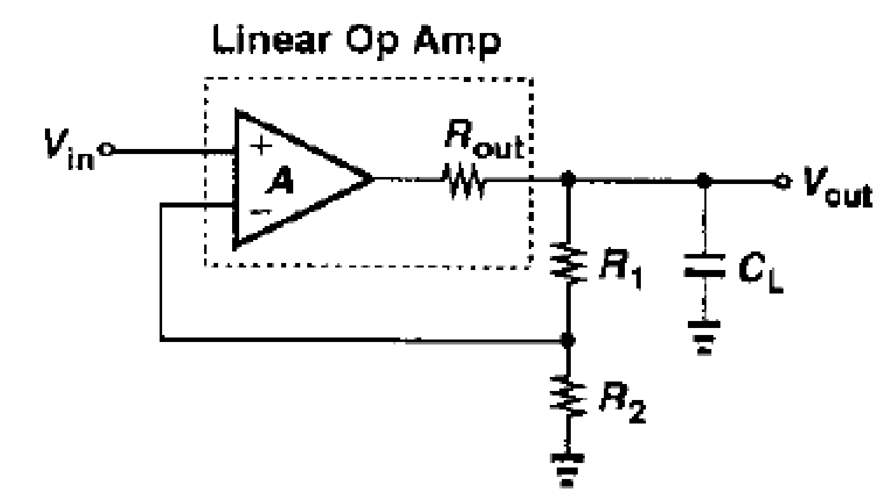




Frequency Compensation must be considered in designing OP Amps

Response of step response of opamp



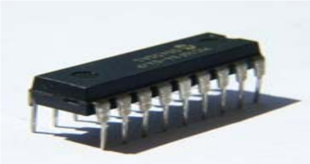


$$\left[\left(V_{in} - V_{out}\frac{R_2}{R_1 + R_2}\right)A - V_{out}\right]\frac{1}{R_{out}} = \frac{V_{out}}{R_1 + R_2} + V_{out}C_L s.$$

where

$$\frac{V_{out}}{V_{in}}(s) \approx \frac{A}{\left(1 + A\frac{R_2}{R_1 + R_2}\right)\left[1 + \frac{R_{out}C_L}{1 + AR_2/(R_1 - R_2)}s\right]}.$$

Step response (contd.)

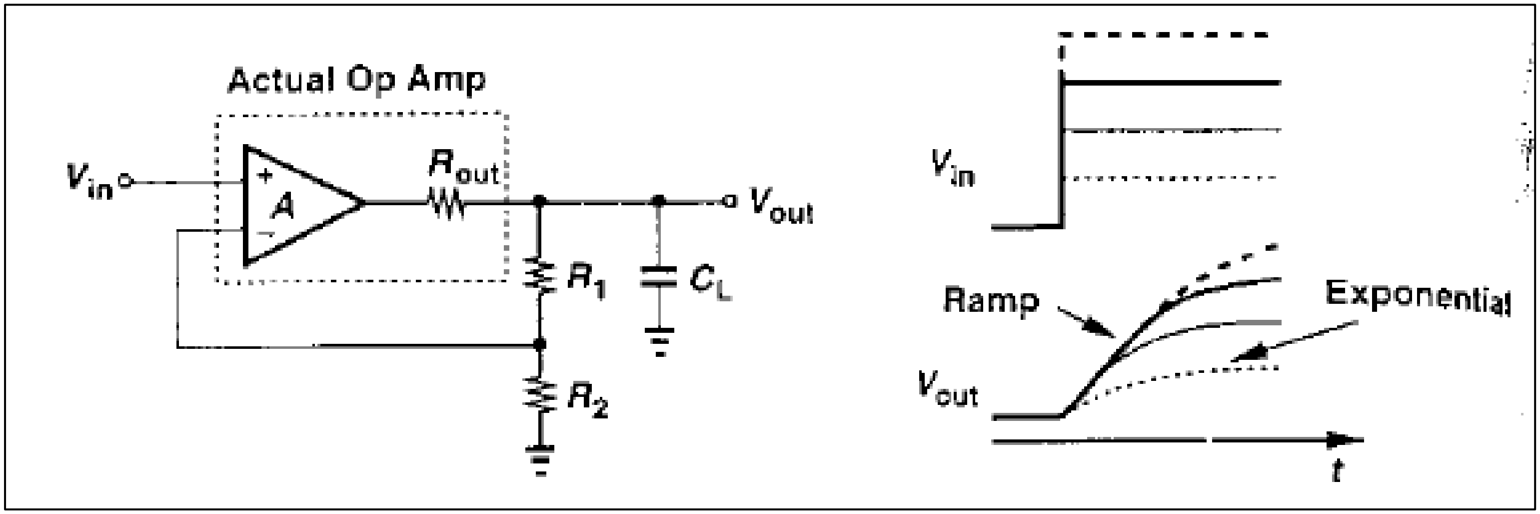


$$V_{out} = V_0 \frac{A}{1 + A\dfrac{R_2}{R_1 + R_2}} \left(1 - \exp \frac{-t}{\dfrac{C_L R_{out}}{1 + A R_2/(R_1 + R_2)}} \right) u(t).$$

This response is called linear settling

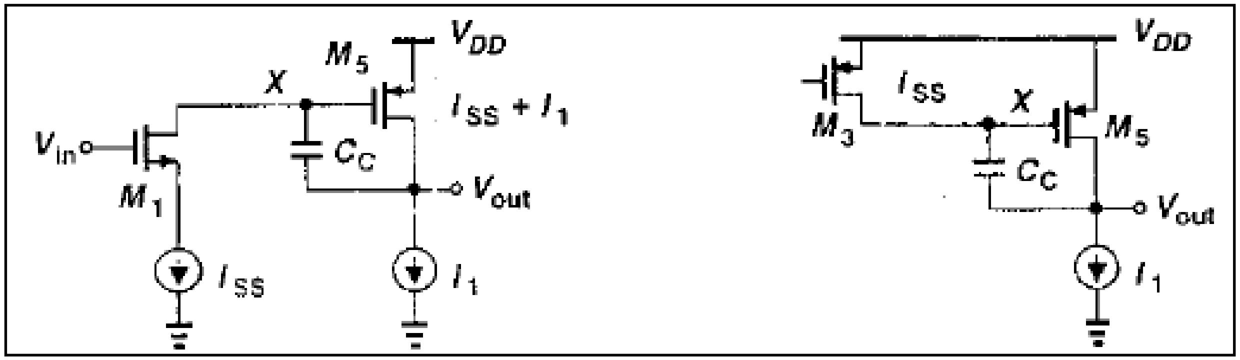
Slew Rate

- Opamp in feedback configuration exibits a large signal behavior called "slewing".



- For realistic opamp with large input steps the output displays a linear ramp having a constant slope. The slope of the ramp is called "slewing".

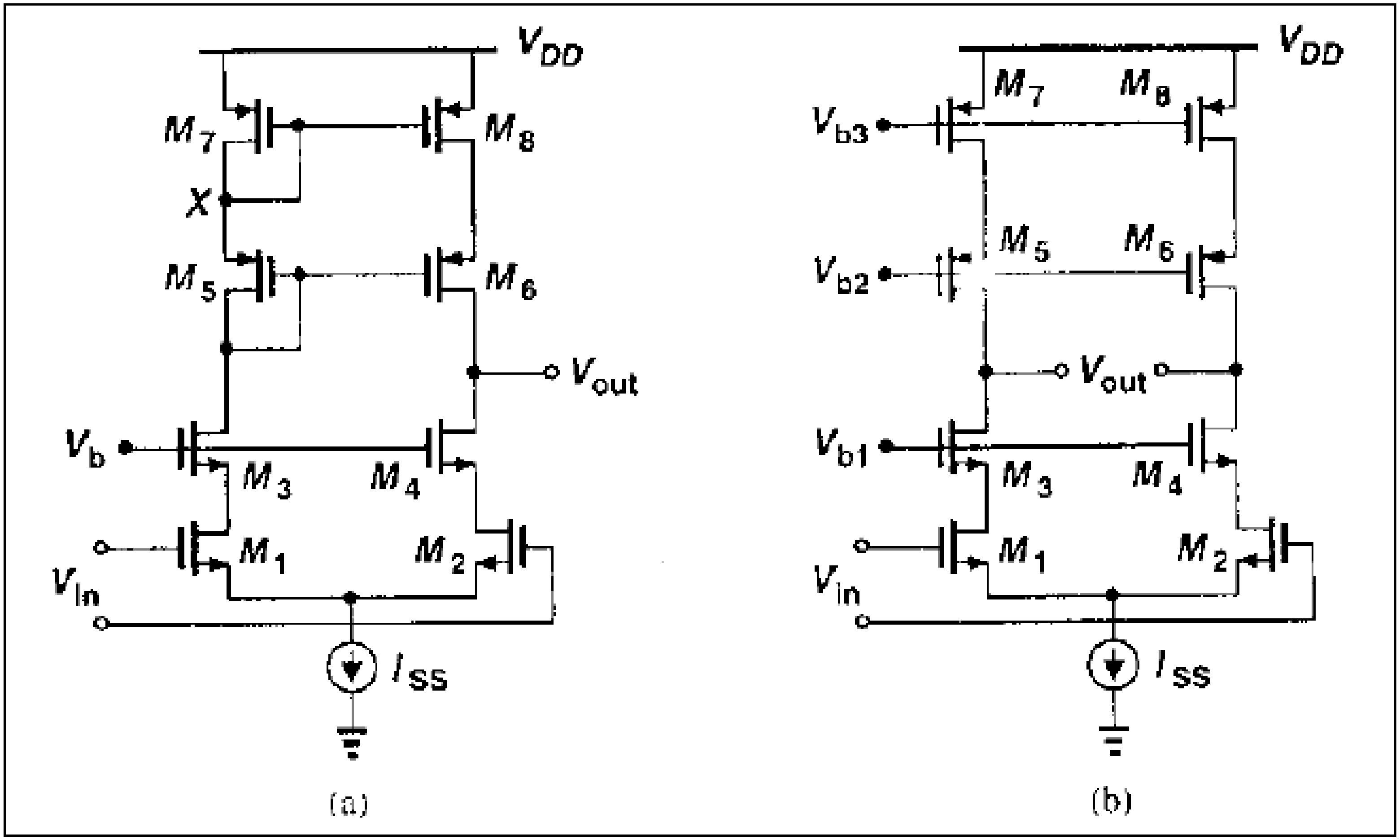
Slewing in Opamp



$$V_{out} \approx \frac{I_{ss} t}{C_C}$$

Hence Slew Rate = $\frac{I_{ss}}{C_C}$

Cascoding of Opamp



Cascoding of Opamp (Contd)

- Such circuits display a gain of the order of

$$g_{mN}\{(g_{mN}r_{oN}{}^{2})\,||\,(g_{mP}r_{oP}{}^{2})\}$$

- Output swings are relatively limited. Hence it is difficult to use cascode opamp for the application of unity gain buffer.

Problem

- Opamp with 2 poles and 1 zero. If zero is forced to ten times higher than GB. Then the 2nd pole has to be placed at what location for a 60^0 phase margin ?

$180^0 - \tan^{-1}(w/p_1) - \tan^{-1}(w/p_2) - \tan^{-1}(w/z_1) = 60^0$

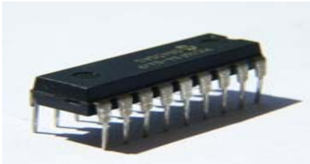
At w = GB

$\tan^{-1}(w/p_1) = 90^{0.}$

$\tan^{-1}(w/z_1) \approx \tan^{-1}0.1$

Leads to $\tan^{-1}(w/p_2) \approx 24.3^0$. $p_2 \geq 2.2GB$

Design of Two Stage Opamp



Basic Requirements

- Gain
- Bandwidth
- Settling time
- Slew rate
- ICMR$^+$
- ICMR$^-$
- PSRR
- Output Voltage Swing
- Output Resistance
- Offset
- Noise
- Layout Area

Design of two stage opamp

Boundary Conditions

- V_{dd}
- V_{ss}
- Supply current range
- Process Specific Parameters :
  - V_{th}
  - K_p, K_n
  - C_{ox}
- Operating temperature range

Design Equations

$$\text{SlewRate} = \frac{I_{tail}}{C_c}$$

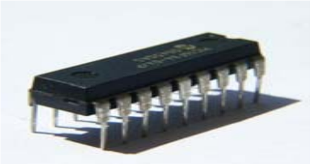
$$A_{v1} = \frac{-g_{m1}}{g_{ds_2} + g_{ds4}}$$

$$A_{v2} = \frac{-g_{m6}}{g_{ds6} + g_{ds7}}$$

$$\text{GainBandwidth} = \frac{g_{m1}}{C_c}$$

$$\text{OutputPole} = \frac{-g_{m6}}{C_L}$$

Design Equations (Continued)



$$\text{RHPzero} = \frac{g_{m6}}{C_c}$$

$$\text{CMR(max)} = V_{DD} - \sqrt{\frac{I_{tail}}{\beta_3}} - |V_{t,p}| + V_{t,n}$$

$$\text{CMR(min)} = Vss + \sqrt{\frac{I_{tail}}{\beta_1}} + V_{t,n} + V_{DStail}$$

$$\text{SaturationVoltage}(V_{DStail}) = \sqrt{\frac{2I_{tail}}{\beta}}$$

Design Steps

- **Step I :** $C_c > k_1 C_L$
- **Step 2 :** $I_{tail} = SR \cdot C_c$
- **Step 3 :** $(W/L)_3 = (I_{tail}) / K_3' (V_{dd} - V_{inmax} - |V_{tp}| + V_{tn})$
- **Step 4 :** $g_{m1} = GB \cdot C_c$
- **Step 5 :** $(W/L)_1 = (g_{m1}^2) / (K_1').(I_{tail})$

Steps to design (contd.)

- **Step 6 :** $(W/L)_5 = 2.I_{tail} / (K_5'. V_{ds5}^2)$

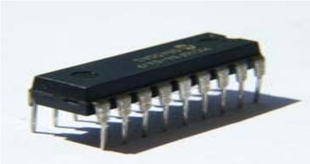
- **Step 7 :** $g_{m6} = 2.2 (g_{m2}C_L) / C_c$

- **Step 8 :** $(W/L)_6 = (W/L)_4 . (g_{m6} / g_{m4})$

- **Step 9 :** $I_6 = g_{m6}^2/\{2.K_6' (W/L)_6 \}$

- **Step 10 :** $(W/L)_7 = (I_6 / I_5). (W/L)_5$

Steps to design (contd.)



- **Step 11 :** $$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2+\lambda_4)I_6(\lambda_6+\lambda_7)}$$

Noise and PSRR

- **Input Referred Noise :** Arise primarily from load and input transistor of the first stage.
- **Flicker Noise :**

$$V_n^{\,2} = \frac{K}{C_{ox}WL}\frac{1}{f}$$

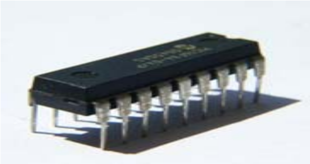
- **Thermal Noise :** Thermal noise of MOS transistor

$$I_n^{\,2} = 4kT\gamma g_m$$

- The maximum output noise voltage that a single MOSFET can generate is

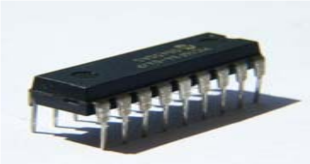
$$V_n^{\,2} = 4kT(\frac{2}{3}g_m)r_o^{\,2}$$

Noise and PSRR (Contd.)



- $^1/_f$ noise can be decreased by increasing device area.
- Thermal noise can be generated can be reduced by increasing its g_m.
- Increase in output resistance of M_5 contributes improvement in PSRR.

Problem :



- Design a two stage opamp (0.18u process) for the following given specifications.

  SR = 10 V/usec

  A_v = 5000 V/V

  GB = 5 MHz

  C_L = 10 pF

  P_{diss} < 0.3 mWatt

  $ICMR^+$ = 1.5 Volt

  $ICMR^-$ = 0.2 Volt