Basic Two-Stage Operational Amplifier Design

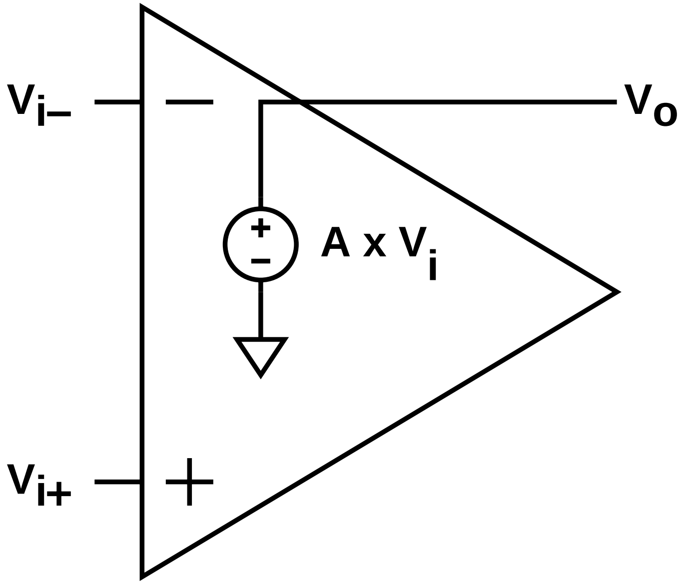
Jieh-Tsorng Wu

December 23, 2002

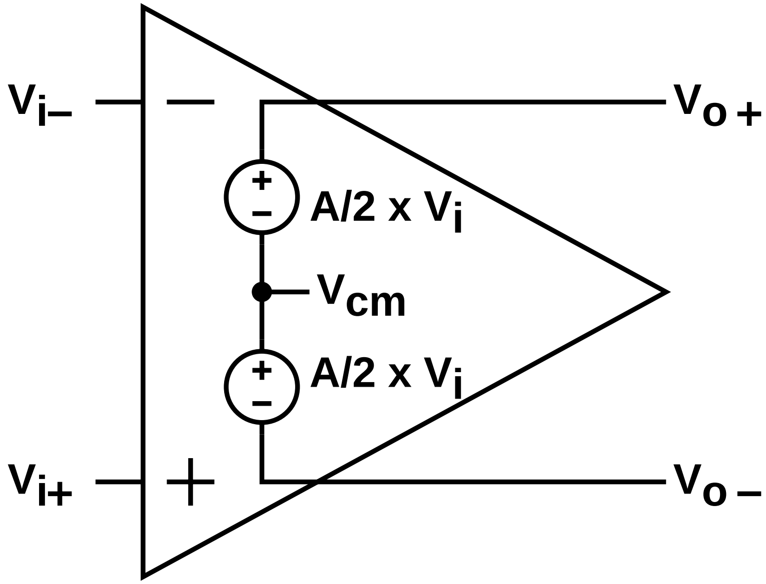
National Chiao-Tung University
Department of Electronics Engineering

Ideal Operational Amplifier

Single-Ended Output

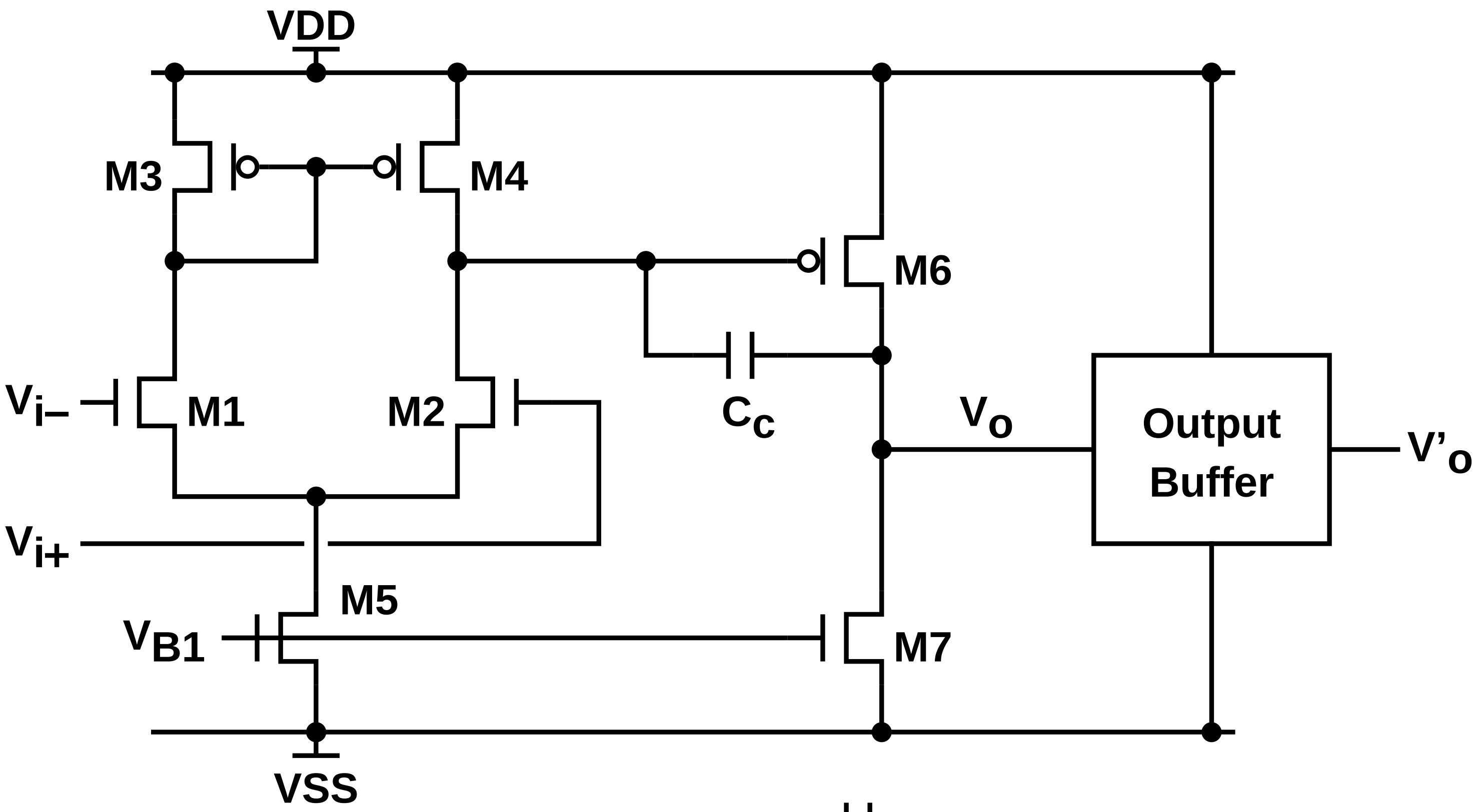


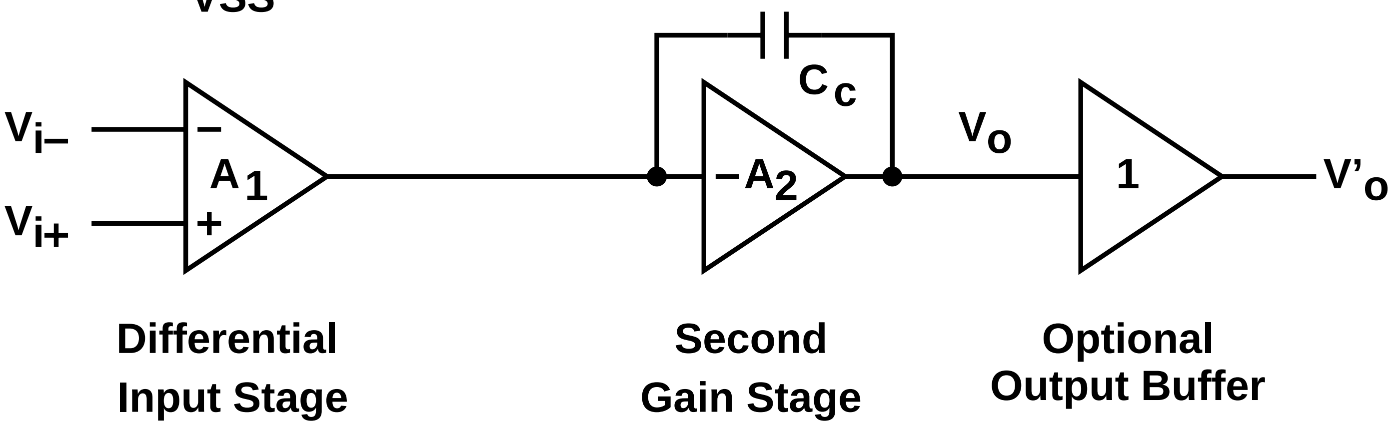
Fully Differential



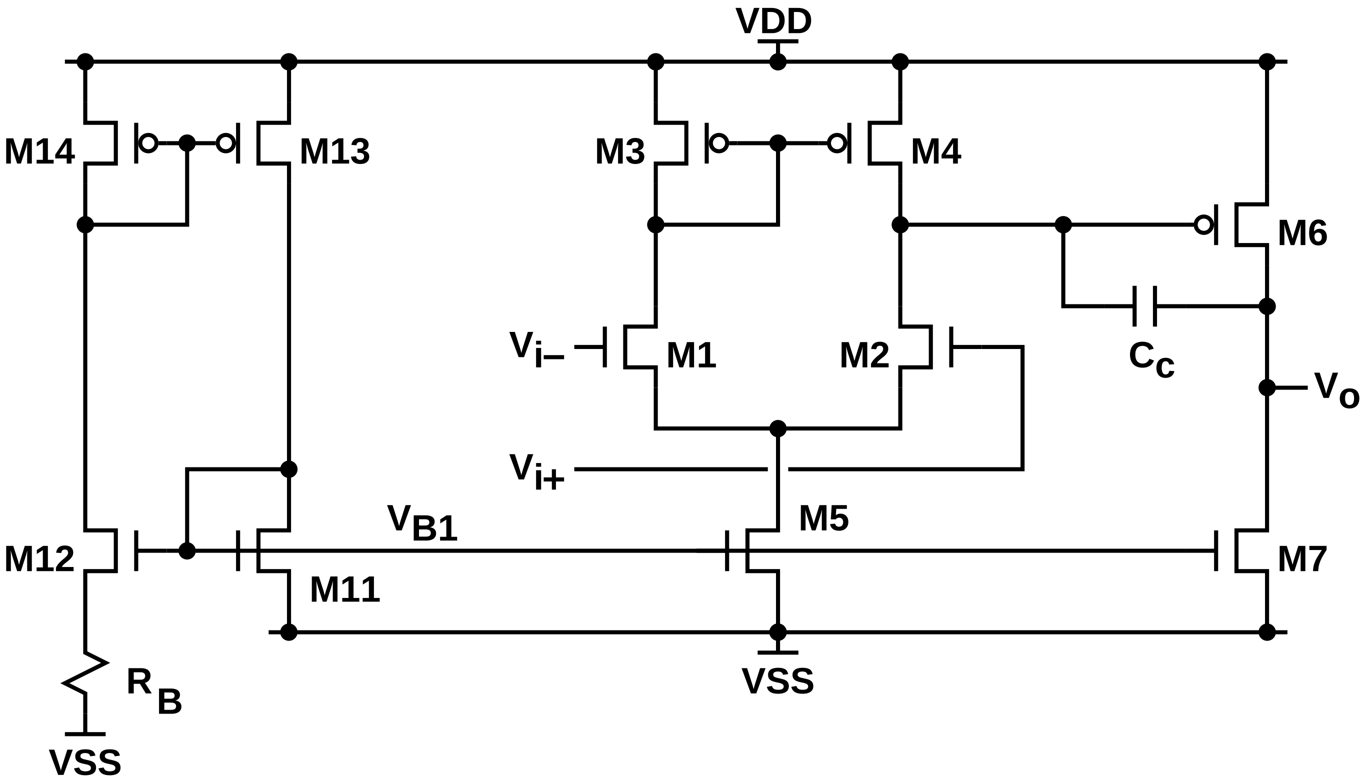
- $V_o = A \times V_i$
- Ideal opamp:
  - $A \rightarrow \infty$, $Z_{in} \rightarrow \infty$, $Z_{out} \rightarrow 0$.
  - No frequency dependence.

Basic 2-Stage CMOS Opamp





Constant g_m Bias Generator



$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$$

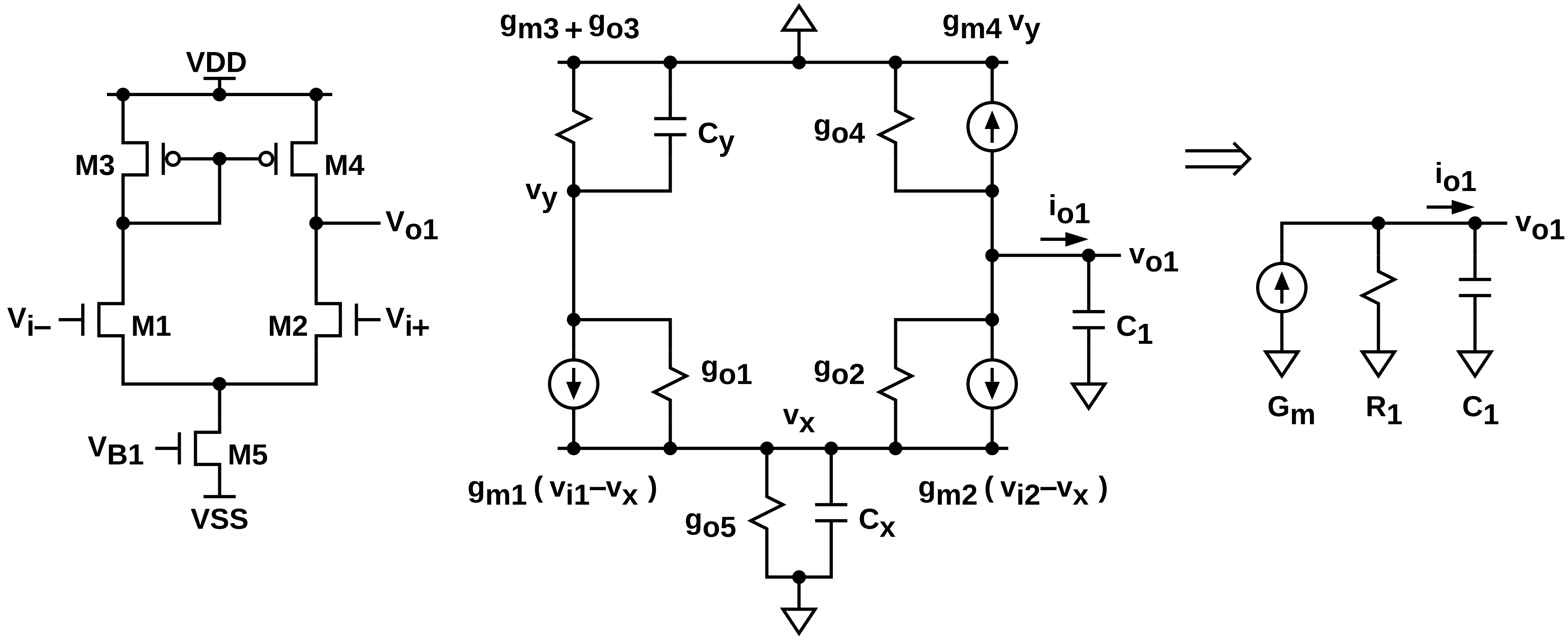
$$\left(\frac{W}{L}\right)_{13} = \left(\frac{W}{L}\right)_{14}$$

$$\left(\frac{W}{L}\right)_{12} = \alpha \cdot \left(\frac{W}{L}\right)_{11}$$

$$g_m = \sqrt{2\mu C_{ox}(W/L)I_D} \quad g_{m11} = \frac{2}{R_B}\frac{\sqrt{\alpha}-1}{\sqrt{\alpha}} \quad g_{m1,m2} = g_{m11} \cdot \sqrt{\frac{(W/L)_1}{(W/L)_{11}}}\sqrt{\frac{1}{2}\frac{(W/L)_5}{(W/L)_{11}}}$$

$$g_{m3,m4} = g_{m11} \cdot \sqrt{\frac{\mu_p}{\mu_n}}\sqrt{\frac{(W/L)_3}{(W/L)_{11}}}\sqrt{\frac{1}{2}\frac{(W/L)_5}{(W/L)_{11}}} \quad g_{m6} = g_{m11} \cdot \sqrt{\frac{\mu_p}{\mu_n}}\sqrt{\frac{(W/L)_6}{(W/L)_{11}}}\sqrt{\frac{(W/L)_7}{(W/L)_{11}}}$$

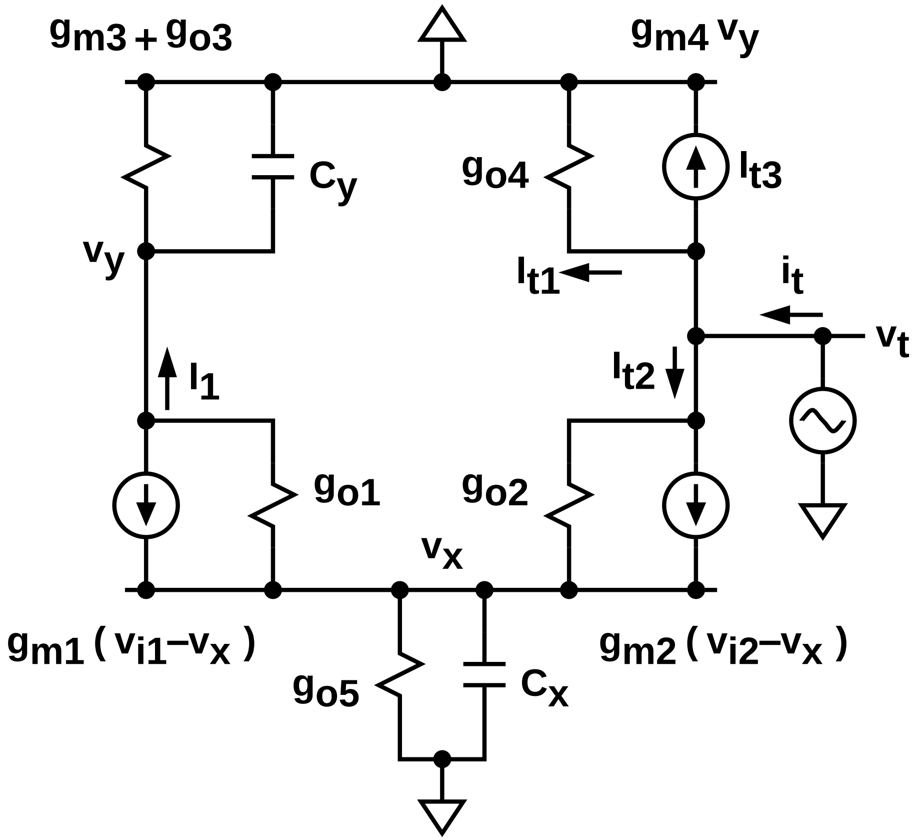
Input Stage Small-Signal Model



$$g_{m1} = g_{m2} \qquad g_{m3} = g_{m4} \qquad g_{o1} = g_{o2} \qquad g_{o3} = g_{o4} \qquad g_m \gg g_o$$

$$C_y \approx C_{gs3} + C_{gs4} = 2C_{gs3}$$

Input Stage Output Impedance



$$v_{i1} = v_{i2} = 0 \qquad G_1 = 1/R_1 = v_t/i_t$$

$$i_t = i_{t1} + i_{t2} + i_{t3} \qquad i_{t1} = v_t \cdot g_{o4}$$

$f \rightarrow \infty$

$$i_{t2} \approx v_t \cdot g_{o2} \quad i_{t3} \approx i_1 \approx 0$$

$$G_1 = g_{o2} + g_{o4}$$

$f \rightarrow 0$

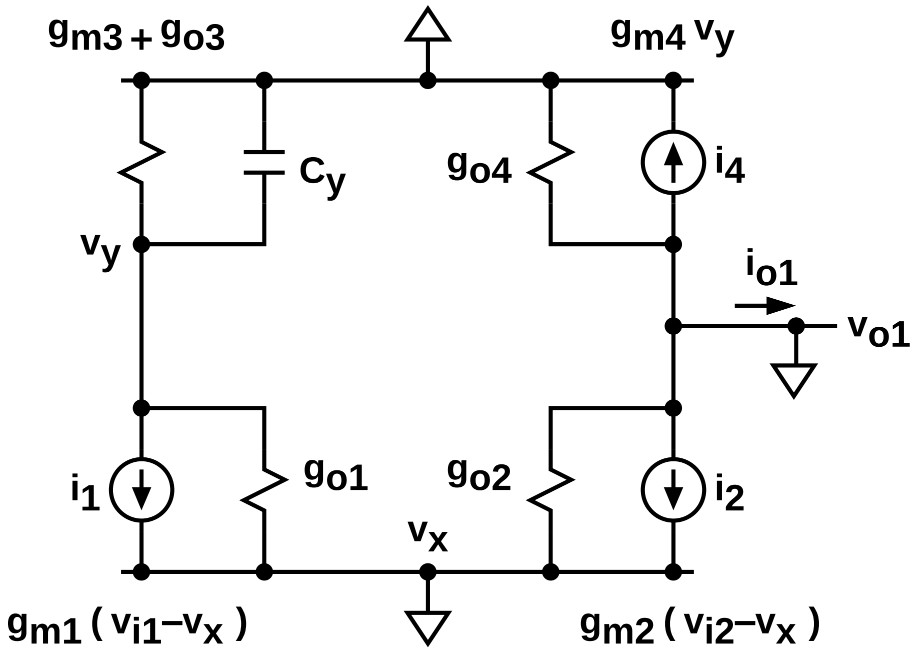
$$i_{t2} \approx v_t \cdot g_{o2}/2 \quad i_{t3} \approx i_1 \approx i_{t2}$$

$$G_1 = g_{o2} + g_{o4}$$

$$\frac{i_{t2}}{v_t} = \frac{g_{o2}(g'_{m1} + g_{o5} + sC'_x)}{g_{m2} + g_{mb2} + g_{o2} + g'_{m1} + g_{o5} + sC'_x} \approx \frac{g_{o2}}{2} \cdot \frac{1 + sC'_x/g'_{m1}}{1 + sC'_x/(2g'_{m1})}$$

$$g'_{m1} = g_{m1} + g_{mb1} \qquad C'_x = C_x + C_{gs1} + C_{gs2}$$

Input Stage Differential-Mode Transconductance



$$v_{id} = v_{i2} - v_{i1} \quad v_{i1} = -\frac{1}{2}v_{id} \quad v_{i1} = +\frac{1}{2}v_{id}$$

$$i_1 = g_{m1}v_{i1} = -\frac{1}{2}g_{m1}v_{id}$$

$$i_2 = g_{m2}v_{i2} = +\frac{1}{2}g_{m1}v_{id}$$

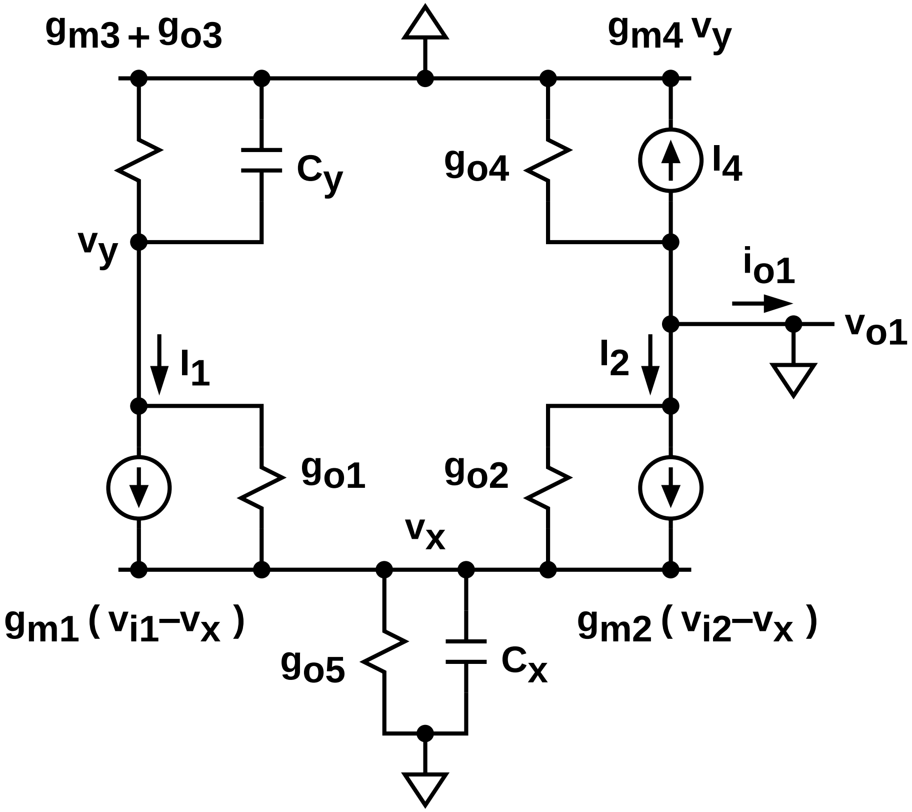
$$\frac{-i_4}{i_1} = \frac{g_{m4}}{g_{m3} + g_{o1} + g_{o3} + sC_y} \approx \frac{g_{m3}}{g_{m3} + sC_y}$$

$$i_o = -i_4 - i_2$$

$$G_{md}(s) \equiv \frac{i_o}{v_{id}} = -\frac{1}{2}g_{m1}\left[1 + \frac{g_{m3}}{g_{m3} + sC_y}\right] = -g_{m1} \cdot \frac{1 + sC_y/(2g_{m3})}{1 + sC_y/g_{m3}} = -g_{m1} \cdot \frac{1 - s/z_m}{1 - s/p_m}$$

$$z_m = \text{Mirror Zero} = -\frac{2g_{m3}}{C_y} \approx -\omega_{t3} \qquad p_m = \text{Mirror Pole} = -\frac{g_{m3}}{C_y} \approx -\frac{\omega_{t3}}{2}$$

Input Stage Common-Mode Transconductance



$$v_{ic} = v_{i1} = v_{i2}$$

$$i_1 = i_2(1 - \epsilon_d)$$

$$-i_4 = i_1(1 - \epsilon_m)$$

$$i_{o1} = -i_4 - i_2 = i_1(1 - \epsilon_m) - i_2$$

$$\Rightarrow i_{o1} = -i_2(\epsilon_d + \epsilon_m - \epsilon_d\epsilon_m) \approx -i_2(\epsilon_d + \epsilon_m)$$

$$G_{mc} = \frac{i_{o1}}{v_{ic}} \approx -\frac{i_2}{v_{ic}} \cdot (\epsilon_d + \epsilon_m)$$

$$\frac{i_2}{v_{ic}} = \frac{g_{m1}}{1 + \frac{2(g_{m1}+g_{mb1})}{(g_{o5}+sC_x)}} = \frac{g_{m1}(g_{o5} + sC_x)}{2(g_{m1} + g_{mb1}) + g_{o5} + sC_x} \approx \frac{g_{o5} + sC_x}{2 + sC_x/g_{m1}} = \frac{g_{o5}}{2} \cdot \frac{1 - s/z_t}{1 - s/p_t}$$

$$z_t = \text{Tail Zero} = -\frac{g_{o5}}{C_x} \qquad p_t = \text{Tail Pole} = -\frac{2g_{m1}}{C_x}$$

Input Stage Common-Mode Transconductance

For the M1-M2 source-coupled pair,

$$i_1 = g_{m1}(v_{ic} - v_x) + g_{o1}(v_y - v_x)$$

$$i_2 = g_{m2}(v_{ic} - v_x) + g_{o2}(0 - v_x) = g_{m1}(v_{ic} - v_x) - g_{o1}v_x$$

$$v_y = -\frac{i_1}{g_{m3} + g_{o3} + sC_y}$$

We have

$$i_1 = i_2 + g_{o1}v_y = i_2 - i_1 \cdot \frac{g_{o1}}{g_{m3} + g_{o3} + sC_y}$$

$$i_1 = i_2 \frac{1}{1 + \frac{g_{o1}}{g_{m3}+g_{o3}+sC_y}} \approx i_2 \left(1 - \frac{g_{o1}}{g_{m3} + g_{o3} + sC_y}\right) = i_2(1 - \epsilon_d)$$

$$\epsilon_d = \frac{g_{o1}}{g_{m3} + g_{o3} + sC_y} \approx \frac{g_{o1}}{g_{m3} + sC_y} = \frac{g_{o1}}{g_{m3}} \cdot \frac{1}{1 + sC_y/g_{m3}} = \frac{g_{o1}}{g_{m3}} \cdot \frac{1}{1 - s/p_m}$$

Input Stage Common-Mode Transconductance

For the M3-M4 current mirror,

$$-\frac{i_4}{i_1} = \frac{g_{m4}}{g_{m3} + g_{o3} + sC_y} = \frac{g_{m3}}{g_{m3} + g_{o3} + sC_y} = 1 - \frac{g_{o3} + sC_y}{g_{m3} + g_{o3} + sC_y} = 1 - \epsilon_m$$

$$\epsilon_m = \frac{g_{o3} + sC_y}{g_{m3} + g_{o3} + sC_y} \approx \frac{g_{o3} + sC_y}{g_{m3} + sC_y} = \frac{g_{o3}}{g_{m3}} \cdot \frac{1 + sC_y/g_{o3}}{1 + sC_y/g_{m3}} = \frac{g_{o3}}{g_{m3}} \cdot \frac{1 + sC_y/g_{o3}}{1 - s/p_m}$$

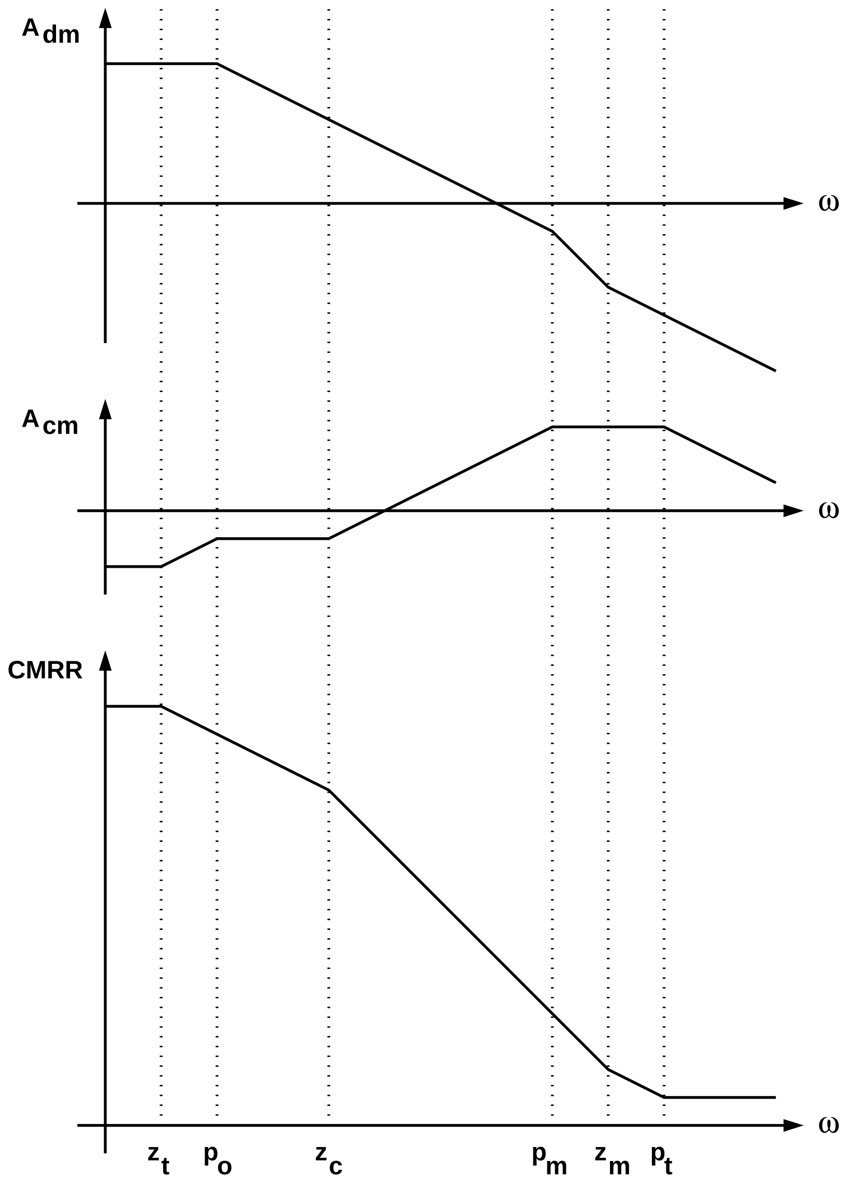
The common-mode transconductance is

$$G_{mc}(s) \approx -\frac{i_2}{v_{ic}} \cdot (\epsilon_d + \epsilon_m)$$

$$\approx -\frac{g_{o5}}{2} \cdot \frac{1 - s/z_t}{1 - s/p_t} \cdot \left(\frac{g_{o1}}{g_{m3}} \cdot \frac{1}{1 - s/p_m} + \frac{g_{o3}}{g_{m3}} \cdot \frac{1 + sC_y/g_{o3}}{1 - s/p_m} \right)$$

$$= -\frac{g_{o5}(g_{o1} + g_{o3})}{2g_{m3}} \cdot \frac{(1 - s/z_t)(1 - s/z_c)}{(1 - s/p_t)(1 - s/p_m)} \qquad z_c = -\frac{g_{o1} + g_{o3}}{C_y}$$

Input Stage Voltage Gain



$$A_{dm} = G_{dm} \cdot Z_1 \qquad A_{cm} = G_{cm} \cdot Z_1$$

$$Z_1 = \frac{1}{G_1 + sC_1} = \frac{1}{g_{o2} + g_{o4}} \cdot \frac{1}{1 - s/p_o}$$

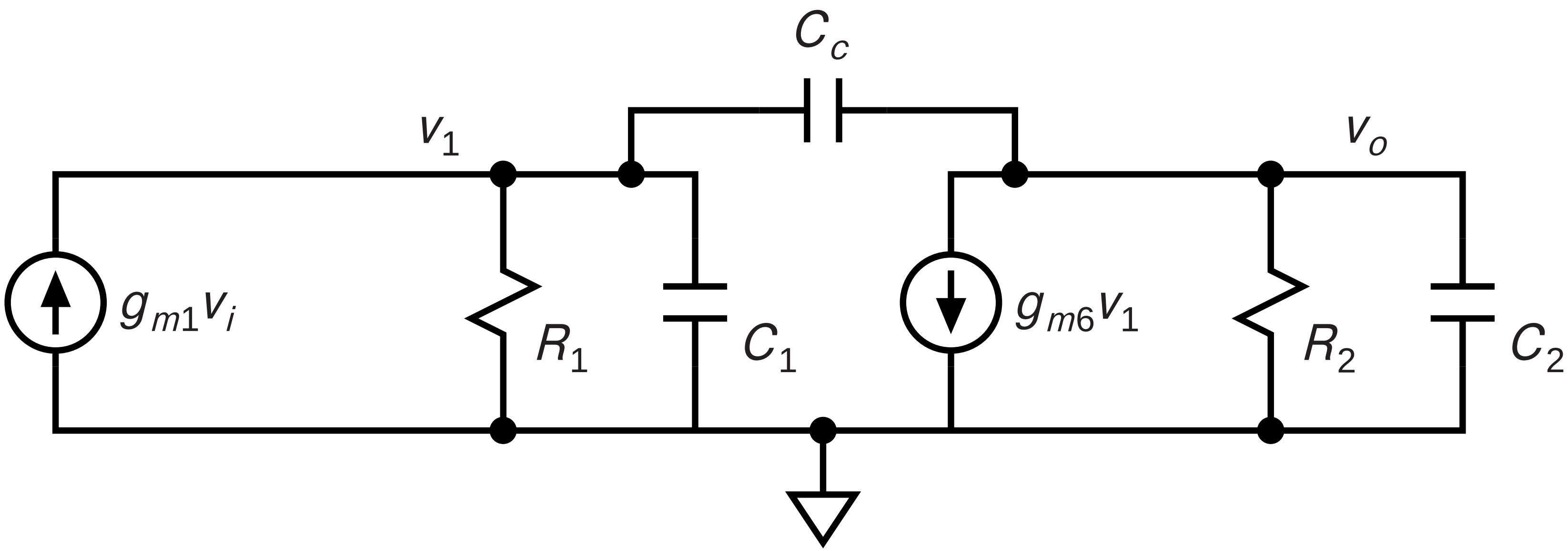
$$p_o = \text{Output Load Pole} = -\frac{g_{o2} + g_{o4}}{C_1}$$

$$\text{CMRR} = \left| \frac{G_{md}}{G_{mc}} \right|$$

$$= \frac{2g_{m1}g_{m3}}{g_{o5}(g_{o1} + g_{o3})} \cdot \frac{(1 - s/z_m)(1 - s/p_t)}{(1 - s/z_t)(1 - s/z_c)}$$

$$\text{CMRR}(\infty) = \frac{g_{m1}/2}{g_{m1}} = \frac{1}{2}$$

Simplified Two-Stage Model



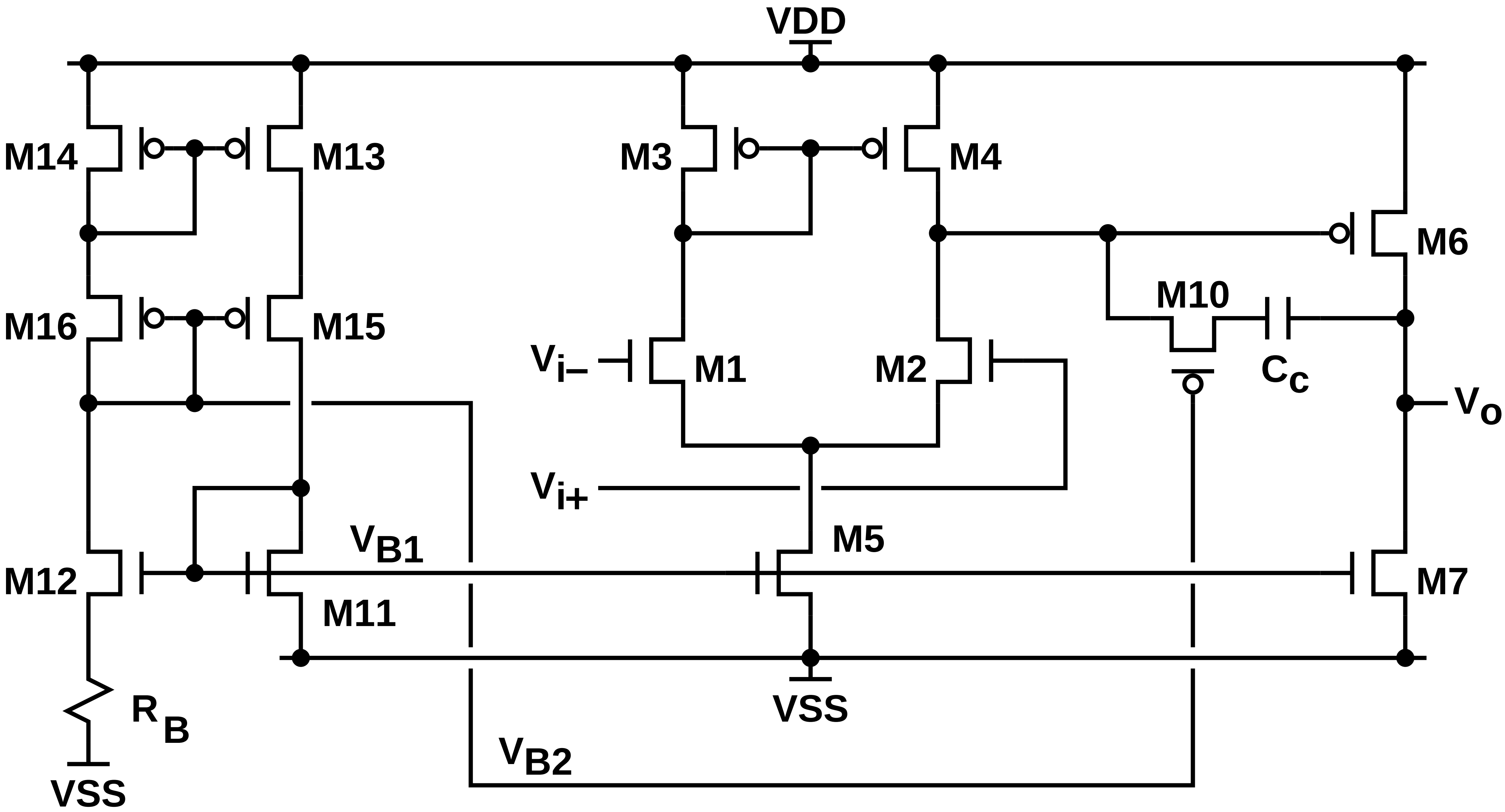
$$G_1 = g_{o2} + g_{o4} \qquad G_2 = g_{o6} + g_{o7} \qquad C_1 \simeq C_{gs6}$$

$$A_v \equiv \frac{v_o}{v_i} = A_v(0)\frac{1 - s/z_1}{(1 - s/p_1)(1 - s/p_2)}$$

$$A_v(0) = g_{m1}g_{m6}R_1R_2$$

$$p_1 \approx -\frac{g_{m1}}{C_c} \times \frac{1}{A_v(0)} \qquad p_2 \approx -\frac{g_{m6}}{C_1 + C_2} \qquad z_1 = +\frac{g_{m6}}{C_c}$$

Frequency Compensation Using Nulling Resistor



Frequency Compensation Using Zero-Nulling Resistor

- The zero-nulling resistor R_c is realized by M10 in the triode region.

$$z_1 = \frac{1}{(1/g_{m6} - R_c)C_c} = -\frac{g_{m6}}{(g_{m6}R_c - 1)C_c}$$

- Let $\frac{(W/L)_{13}}{(W/L)_{14}} = \frac{(W/L)_{15}}{(W/L)_{16}}$ and $\frac{(W/L)_7}{(W/L)_{11}} = \frac{(W/L)_6}{(W/L)_{13}}$, then

$$V_{ov6} = V_{ov13} = V_{ov14} \qquad V_{ov10} = V_{ov15} = V_{ov16} \qquad \frac{V_{ov6}}{V_{ov10}} = \frac{V_{ov13}}{V_{ov15}} = \sqrt{\frac{(W/L)_{15}}{(W/L)_{13}}}$$

$$g_{m6}R_c = \frac{g_{m6}}{g_{m10}} = \frac{(W/L)_6}{(W/L)_{10}}\frac{V_{ov6}}{V_{ov10}} = \frac{(W/L)_6}{(W/L)_{10}}\sqrt{\frac{(W/L)_{15}}{(W/L)_{13}}}$$

- $p_2/z_1 \approx (g_{m6}R_c - 1)C_c/(C_1 + C_2)$ is independent of process and temperature variations.

Voltage and Current Range

Input Common-Mode Range

$$V_{ic(max)} = V_{DD} - V_{GS3} + V_{t1} \qquad V_{ic(min)} = V_{SS} + V_{DSAT5} + V_{GS1}$$

- The range is limited to the voltage levels where any transistor goes out of saturation.

Output Voltage Range

$$V_{o(max)} = V_{DD} - V_{DSAT6} \qquad V_{o(min)} = V_{SS} + V_{DSAT7}$$

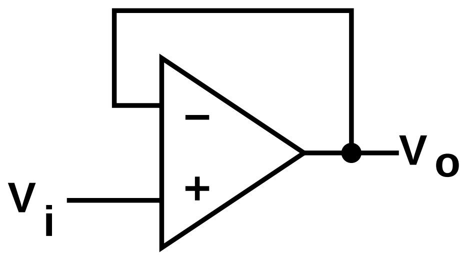
- Output resistive load can also limit the voltage range, if the available output current is insufficient.

Maximum Output Current

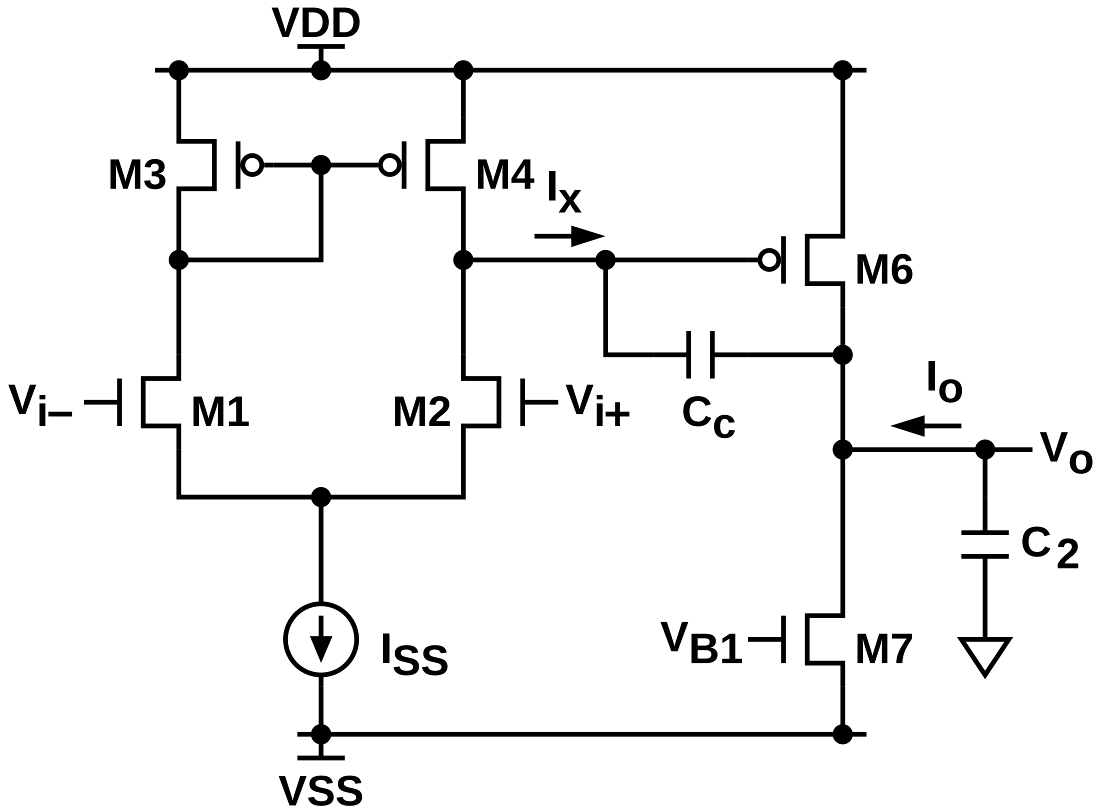
$$I_{o(\text{sink,max})} = I_{D7} \qquad I_{o(\text{source,max})} = \frac{1}{2}k'_p\left(\frac{W}{L}\right)_6 [V_{gs6(max)} - V_{t6}]^2 - I_{D7}$$

$$V_{gs6(max)} = V_{DD} - V_{i+} + V_{t2}$$

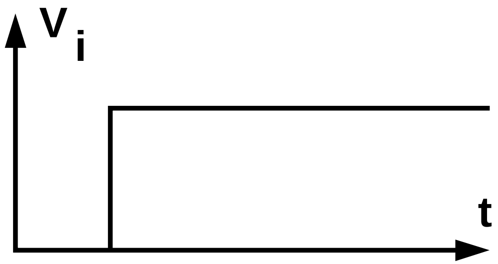
Slew Rate



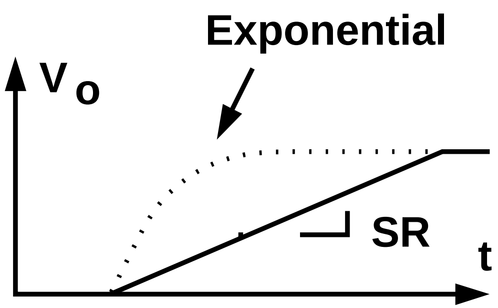
−
+
V i
V o



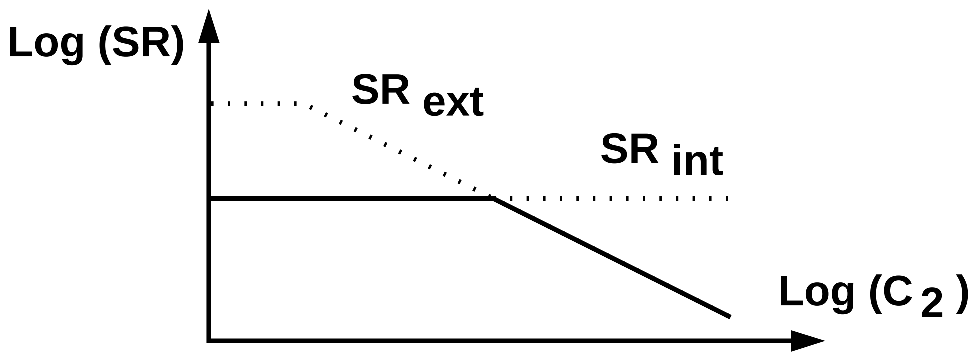
VDD
M3
M4
I x
M6
C c
I o
V o
V i−
M1
M2
V i+
C 2
I SS
V B1
M7
VSS



V i
t



Exponential
V o
SR
t



Log (SR)
SR ext
SR int
Log (C 2)

Slew Rate

The *internal slew rate* is generally limited by current available to charge and discharge C_c from input stage. Therefore,

$$
\begin{aligned}
\mathrm{SR}_{int} &= \left.\frac{dV_o}{dt}\right|_{max} = \frac{I_{x(max)}}{C_c} = \frac{I_{SS}}{C_c} \\
&= \frac{I_{SS}}{g_{m1}} \times \frac{g_{m1}}{C_c} = \frac{I_{SS}}{g_{m1}} \times \omega_u \\
&= (V_{GS1} - V_{t1}) \times \omega_u \\
&= V_{ov1} \times \omega_u
\end{aligned}
$$

The *external slew rate* is limited by the available current to charge and discharge C_2. Thus,

$$
\mathrm{SR}_{ext} = \frac{I_{D7} - I_x(max)}{C_2} = \frac{I_{D7} - I_{SS}}{C_2}
$$

Settling Time

The frequency response and step response of a single-pole amplifier is

$$A(s) = \frac{A_o}{1 + s/\omega_p} \qquad V_o(t) = A_o\left(1 - e^{-\omega_p t}\right)$$

The settling time can be written as

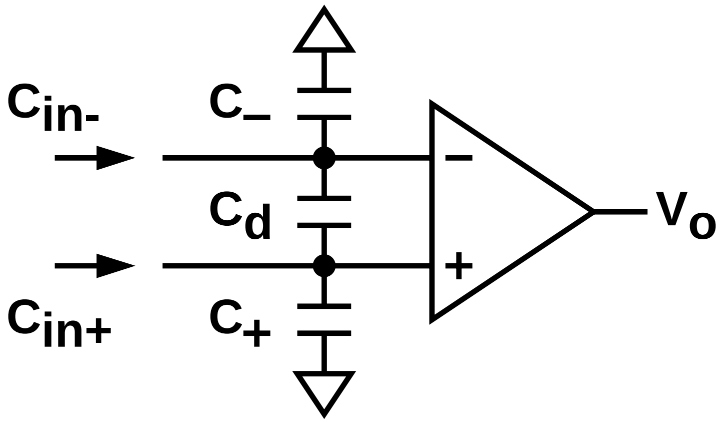
$$t_s(\epsilon) = \frac{1}{\omega_p}\ln\frac{1}{\epsilon} = \frac{A_o}{\omega_u}\ln\frac{1}{\epsilon}$$

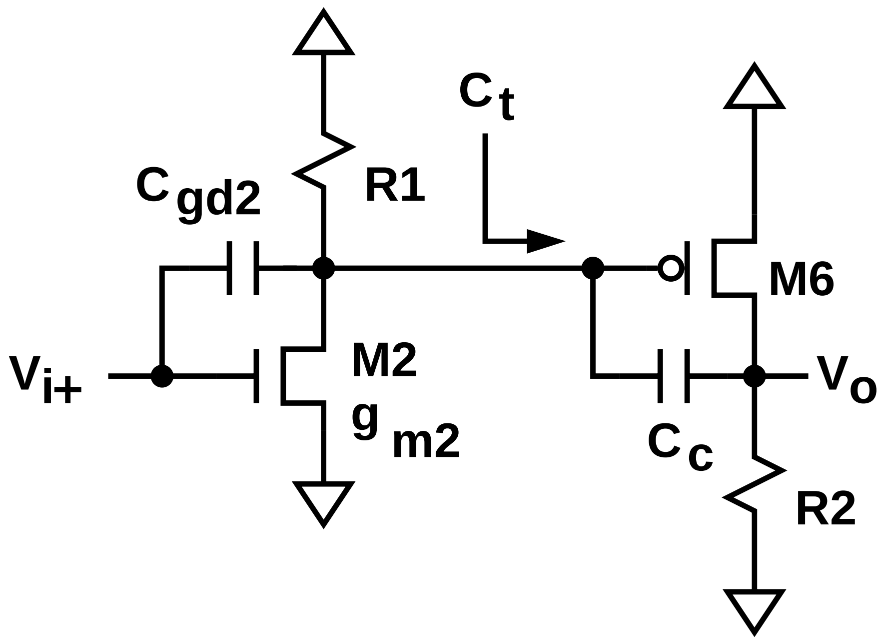
- $\omega_u = A_o \cdot \omega_p$ is the dominant-pole unity-gain frequency.
- $\epsilon = 1 - |V_o(t_s)/A_o|$ is the error when settling occurs.

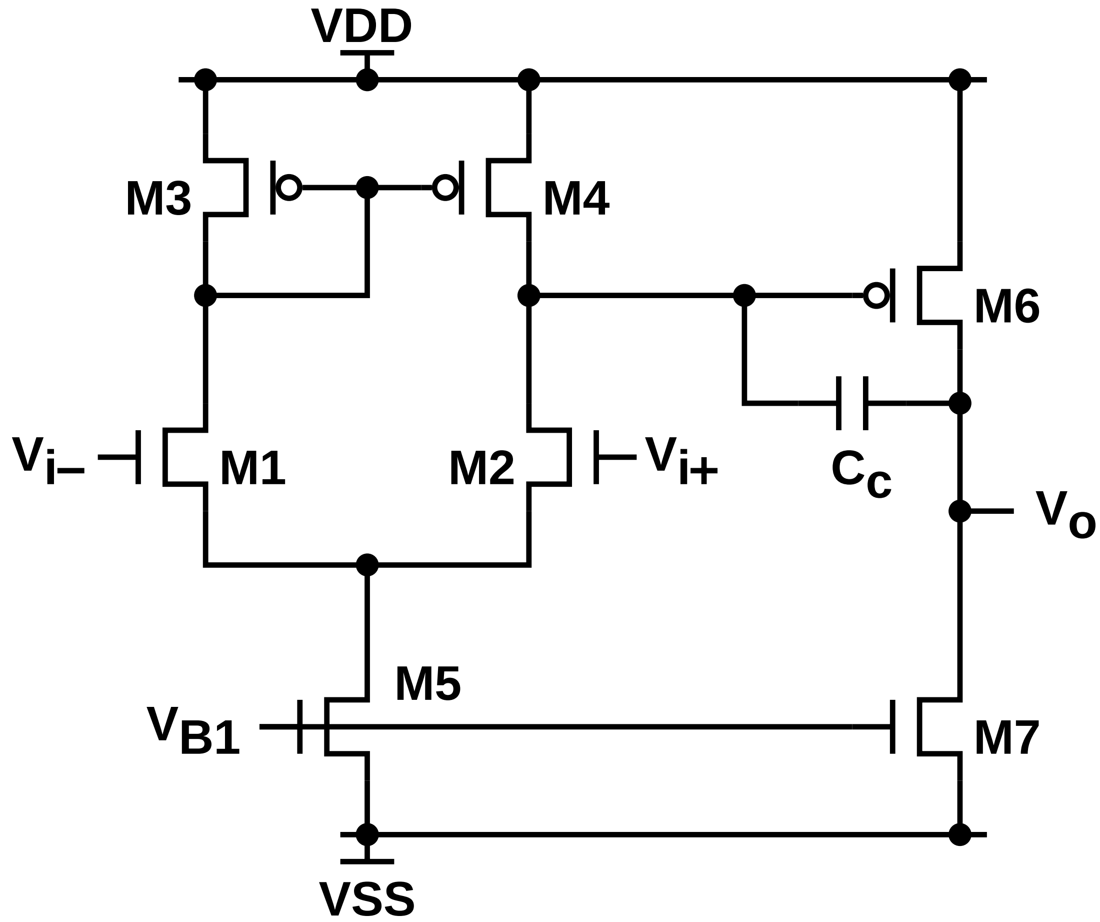
The 10% to 90% rise time is

$$t_r = \frac{1}{\omega_p}\ln(9) = \frac{2.2}{\omega_p} = \frac{0.35}{f_p} \qquad \omega_p = 2\pi f_p$$

Input Impedance







Input Impedance

Shorting the noninverting input to ground,

$$C_{in-} = C_d + C_- \approx \frac{C_{gs1}}{2}$$

Shorting the inverting input to ground,

$$C_{in+} = C_d + C_+ \approx \frac{C_{gs1}}{2} + C_{gd2} \cdot (1 + A_{o1}) \qquad A_{o1} = g_{m2} R_1$$

And we have

$$C_d \approx \frac{C_{gs2}}{2} \qquad C_- \approx 0 \qquad C_+ \approx C_{gd2} \cdot (1 + A_{o1})$$

Input Impedance

The equivalent voltage gain of the M2 stage decreases with increasing frequency, due the the effect of C_t. The capacitance C_+ is then modified as

$$C_+ \approx C_{gd2} \cdot A_{o1} \cdot \frac{1 + \frac{C_{gd2}}{g_{m2}} s}{1 + A_{o1} \frac{C_{gd2}+C_t}{g_{m2}} s}$$

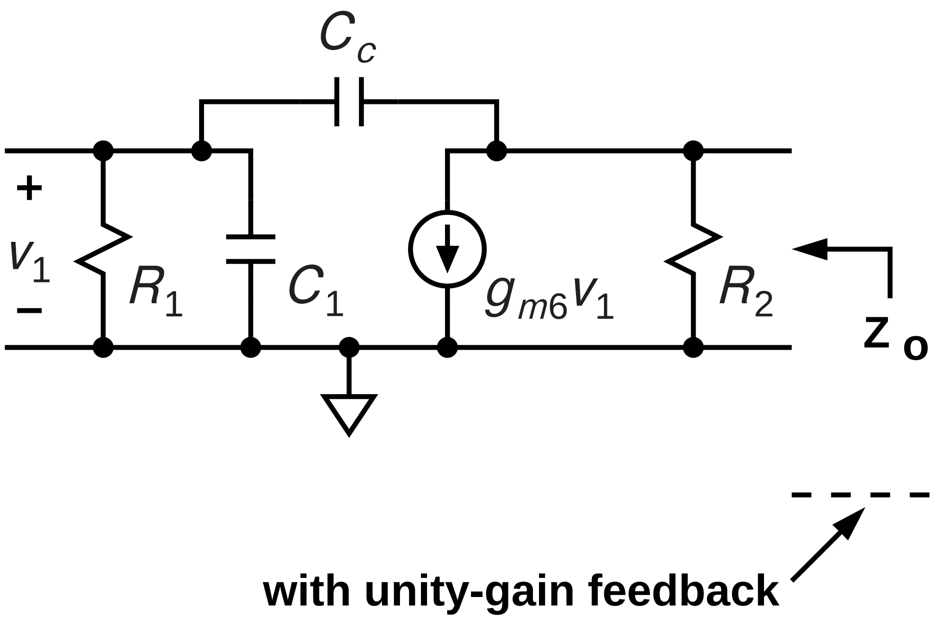
where

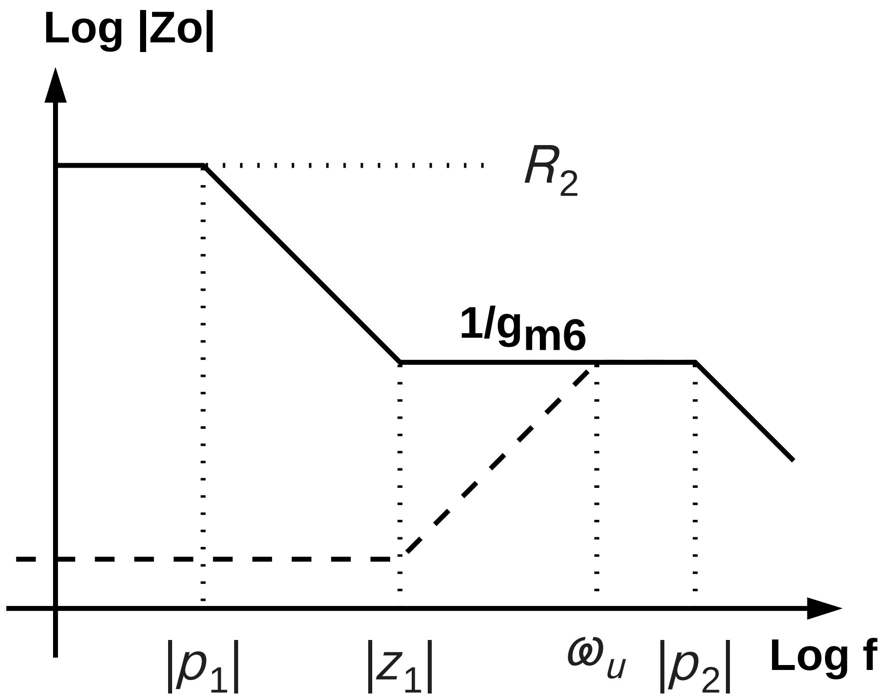
$$C_t = C_{gs6} + C_c \cdot (1 + A_{o2}) = C_{gs6} + C_c \cdot (1 + g_{m6} R_2)$$

- For $g_{m2}/[A_{o1}(C_{gd2} + C_t)] < \omega < g_{m2}/C_{gd2}$, C_+ become resistive, and

$$C_+ \quad \rightarrow \quad R_+ \approx \frac{1}{g_{m2}} \cdot \left(1 + \frac{C_t}{C_{gd2}}\right)$$

Output Impedance





Assuming $g_{m6} \gg R_1$ and R_2, we have

$$Z_o = R_2 \cdot \frac{1 + sR_1(C_c + C_1)}{1 + sg_{m6}R_1R_2C_c + s^2R_1C_1R_2C_c}$$

$$p_1 \approx -\frac{1}{g_{m6}R_1R_2C_c} = -\frac{g_{m1}}{C_c} \cdot \frac{1}{|A_v(0)|} \qquad p_2 \approx -\frac{g_{m6}}{C_1} \qquad z_1 \approx -\frac{1}{R_1(C_c + C_1)}$$

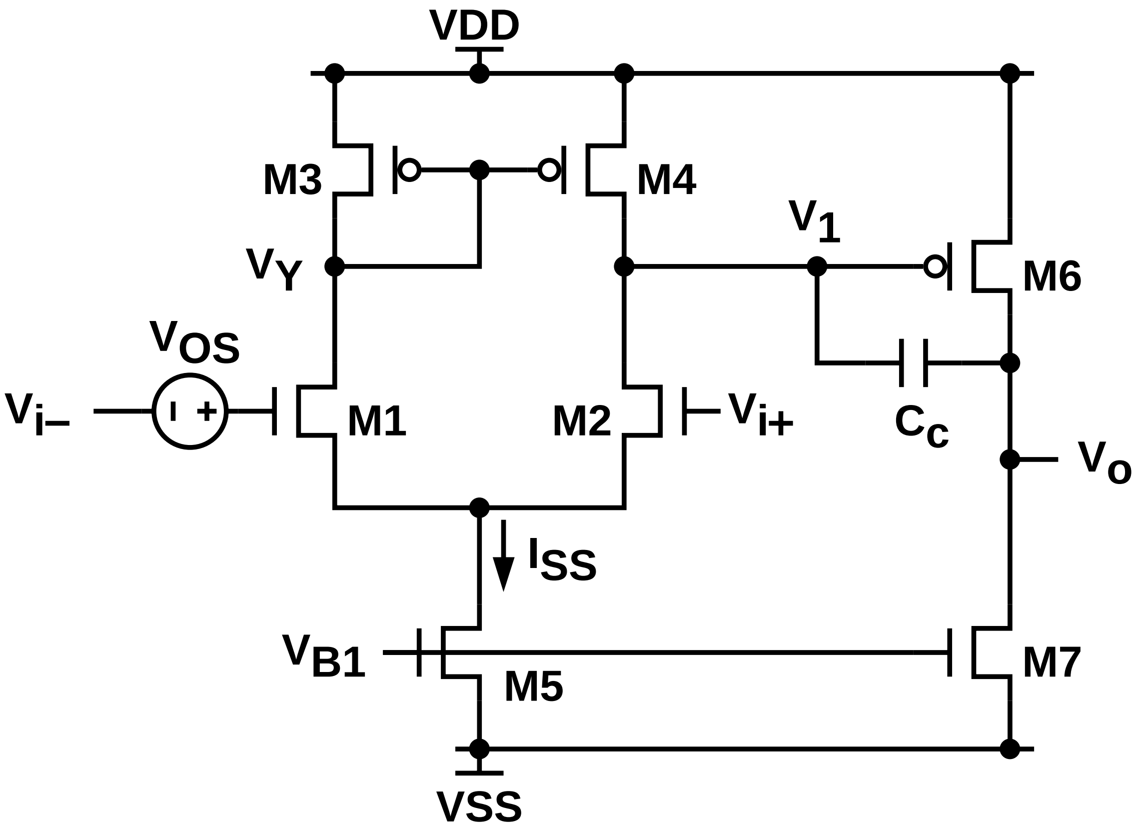
Output Impedance

- For frequencies larger than z_1, C_c acts as a short, the Z_o is a resistive $1/g_{m6}$.
- The closed-loop Z_o of the unity-gain buffer is

$$Z_{oc} \approx \frac{Z_o}{A_v} \approx \frac{R_2}{A_v(0)} \cdot (1 - s/z_1) \quad \text{for} \quad \omega < \omega_u$$

where $\omega_u = g_{m1}/C_c$.

Systematic Input Offset Voltage



$$I_D = \frac{1}{2} k V_{ov}^2 (1 + \lambda V_{DS})$$

$$\lambda_1 = \lambda_2 \qquad \lambda_3 = \lambda_4$$

$$\Delta I_{1-2} = I_{D1} - I_{D2} = \frac{I_{SS}}{2} \lambda_1 (V_Y - V_1)$$

$$\Delta I_{3-4} = |I_{D3}| - |I_{D4}| = \frac{I_{SS}}{2} \lambda_3 (V_1 - V_Y)$$

The systematic input referred dc offset can be expressed as

$$-V_{OS,s} = \frac{1}{g_{m1}} \cdot (\Delta I_{1-2} - \Delta I_{3-4}) = \frac{V_{ov,1-2}}{2} \cdot (\lambda_1 + \lambda_3)(V_Y - V_1)$$

Systematic Input Offset Voltage

- The systematic offset is caused by asymmetry in the dc biasing of V_Y and V_1.
- To minimize $V_{OS,s}$, want $V_{DS3} = V_{DS4} = V_{GS6}$, then

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{(W/L)_5}{2(W/L)_7}$$

- Further, to minimize process induced variations choose

$$L_3 = L_4 = L_6$$

However, this constraint may conflict with frequency response and noise constraints.

Random Input Offset Voltage

$$\Delta V_{i-j} = |V_i| - |V_j| \qquad V_{i-j} = \frac{|V_i| + |V_j|}{2} \qquad \Delta I_{i-j} = |I_i| - |I_j| \qquad I_{i-j} = \frac{|I_i| + |I_j|}{2}$$

$$\Delta\left(\frac{W}{L}\right)_{i-j} = \left(\frac{W}{L}\right)_i - \left(\frac{W}{L}\right)_j \qquad \left(\frac{W}{L}\right)_{i-j} = \frac{1}{2}\left[\left(\frac{W}{L}\right)_i + \left(\frac{W}{L}\right)_j\right]$$

$$\Rightarrow \qquad \frac{\Delta I_{D,3-4}}{I_{D,3-4}} = \frac{\Delta(W/L)_{3-4}}{(W/L)_{3-4}} - 2\frac{\Delta V_{t,3-4}}{V_{ov,3-4}} = \frac{\Delta I_{D,1-2}}{I_{D,1-2}}$$

$$-V_{OS,r} = \Delta V_{t,1-2} + \frac{V_{ov,1-2}}{2}\left[\frac{\Delta I_{D,1-2}}{I_{D,1-2}} - \frac{\Delta(W/L)_{1-2}}{(W/L)_{1-2}}\right]$$

$$= \Delta V_{t,1-2} - \frac{V_{ov,1-2}}{V_{ov,3-4}} \cdot \Delta V_{t,3-4} + \frac{V_{ov,1-2}}{2}\left[-\frac{\Delta(W/L)_{1-2}}{(W/L)_{1-2}} + \frac{\Delta(W/L)_{3-4}}{(W/L)_{3-4}}\right]$$

$$= \Delta V_{t,1-2} - \frac{g_{m3}}{g_{m1}} \cdot \Delta V_{t,3-4} + \frac{V_{ov,1-2}}{2}\left[-\frac{\Delta(W/L)_{1-2}}{(W/L)_{1-2}} + \frac{\Delta(W/L)_{3-4}}{(W/L)_{3-4}}\right]$$

Input Offset Voltage and Common-Mode Rejection Ratio

The output voltage change due to common-mode input variation is

$$\Delta V_o = A_{cm} \cdot \Delta V_{ic}$$

Want to change differential input so that $\Delta V_o = 0$, then

$$\Delta V_{id} = -\frac{\Delta V_o}{A_{dm}} = -\frac{A_{cm}}{A_{dm}} \cdot \Delta V_{ic}$$

Therefore, we have

$$\text{CMRR} \equiv \left|\frac{A_{dm}}{A_{cm}}\right| = \left|\left(\left.\frac{\partial V_{id}}{\partial V_{ic}}\right|_{\Delta V_o=0}\right)^{-1}\right| = \left|\left(\frac{\partial V_{OS}}{\partial V_{ic}}\right)^{-1}\right|$$

CMRR Due to Systematic and Random Offset

Since

$$V_{OS} = V_{OS,s} + V_{OS,r}$$

We have

$$\frac{1}{\text{CMRR}} = \left| \frac{\partial V_{OS,s}}{\partial V_{ic}} + \frac{\partial V_{OS,r}}{\partial V_{ic}} \right|$$

$$\frac{\partial V_{OS,s}}{\partial V_{ic}} = \frac{\partial V_{OS,s}}{\partial V_{ov1}} \cdot \frac{\partial V_{ov1}}{\partial I_{d1}} \cdot \frac{\partial I_{d1}}{\partial V_{ic}} = -\frac{1}{2}(\lambda_1 + \lambda_3)(V_Y - V_1) \cdot \frac{1}{g_{m1}} \cdot \frac{g_{m1}}{1 + 2(g_{m1} + g_{mb1})r_{o5}}$$

$$= -\frac{1}{2}(\lambda_1 + \lambda_3)(V_Y - V_1) \cdot \frac{1}{1 + 2(g_{m1} + g_{mb1})r_{o5}} \approx -\frac{(\lambda_1 + \lambda_3)(V_Y - V_1)}{4(g_{m1} + g_{mb1})r_{o5}}$$

$$\frac{\partial V_{OS,r}}{\partial V_{ic}} = \frac{\partial V_{OS,r}}{\partial V_{ov1}} \cdot \frac{\partial V_{ov1}}{\partial I_{d1}} \cdot \frac{\partial I_{d1}}{\partial V_{ic}} = -\frac{1}{2}\left[-\frac{\Delta(W/L)_{1-2}}{(W/L)_{1-2}} + \frac{\Delta(W/L)_{3-4}}{(W/L)_{3-4}}\right] \cdot \frac{1}{1 + 2(g_{m1} + g_{mb1})r_{o5}}$$

$$= -\left[-\frac{\Delta(W/L)_{1-2}}{(W/L)_{1-2}} + \frac{\Delta(W/L)_{3-4}}{(W/L)_{3-4}}\right] \cdot \frac{1}{4(g_{m1} + g_{mb1})r_{o5}}$$

Mismatches and Input Stage Transconductance

Define

$$\Delta g_{m,i-j} = g_{m,i} - g_{m,j} \quad g_{m,i-j} = \frac{g_{m,i} + g_{m,j}}{2} \quad \Delta r_{o,i-j} = r_{o,i} - r_{o,j} \quad r_{o,i-j} = \frac{r_{o,i} + r_{o,j}}{2}$$

Then

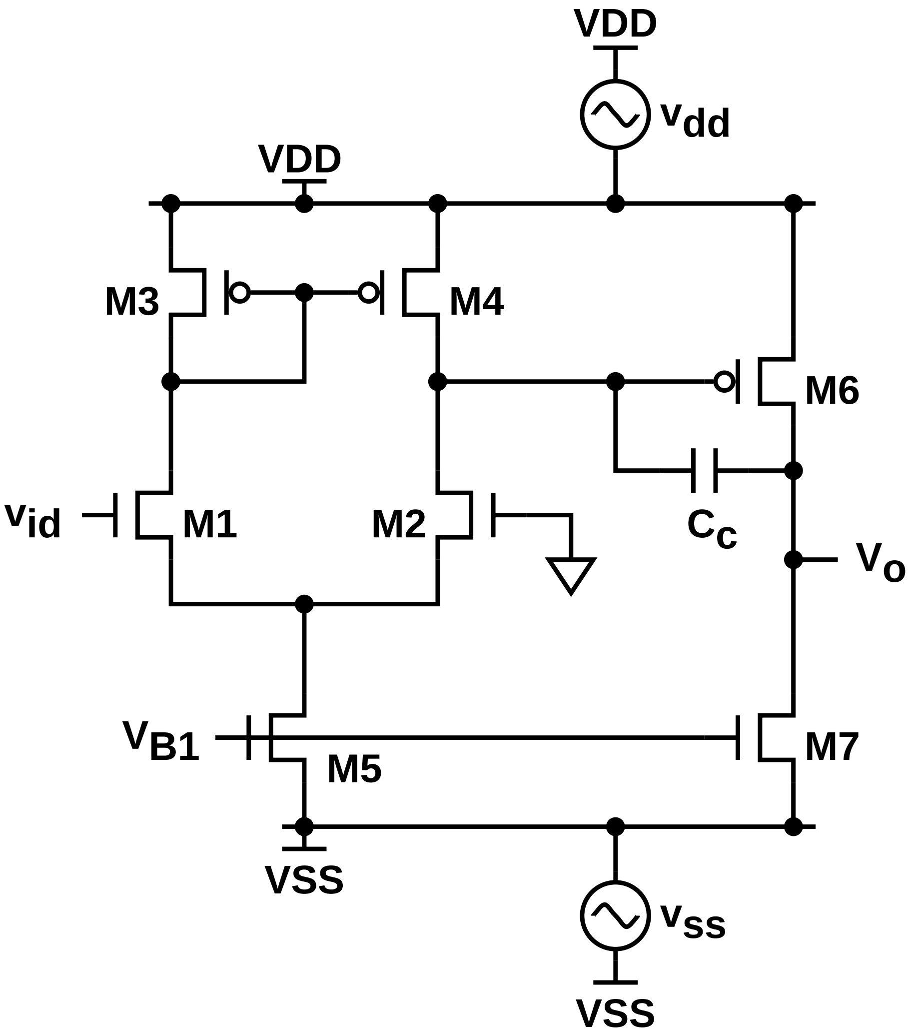
$$G_{md} \approx g_{m,1-2} \cdot \frac{1 - \left(\frac{\Delta g_{m,1-2}}{2g_{m,1-2}}\right)^2}{1 + \left(\frac{\Delta g_{m,3-4}}{2g_{m,3-4}}\right)} \qquad G_{mc} \approx -\frac{g_{m,1-2}}{1 + 2g_{m,1-2}r_{o5}} \cdot (\epsilon_d + \epsilon_m)$$

where

$$\epsilon_d \approx \frac{1}{g_{m3}r_{o1}} - \frac{\Delta g_{m,1-2}}{g_{m,1-2}}\left(1 + \frac{2r_{o5}}{r_{o1}}\right) - \frac{2r_{o5}}{r_{o1}} \cdot \frac{\Delta r_{o,1-2}}{r_{o,1-2}}$$

$$\epsilon_m = \frac{1}{1 + g_{m3}r_{o3}} + \frac{(g_{m3} - g_{m4})r_{o3}}{1 + g_{m3}r_{o3}} \approx \frac{1}{g_{m3}r_{o3}} + \frac{\Delta g_{m,3-4}}{g_{m,3-4}}$$

Power Supply Rejection Ratio (PSRR)



$$v_o = -A_v v_{id} + A_{dd} v_{dd} + A_{ss} v_{ss}$$

$$\text{PSRR}_{DD} \equiv \frac{A_v}{A_{dd}}$$

$$\text{PSRR}_{SS} \equiv \frac{A_v}{A_{ss}}$$

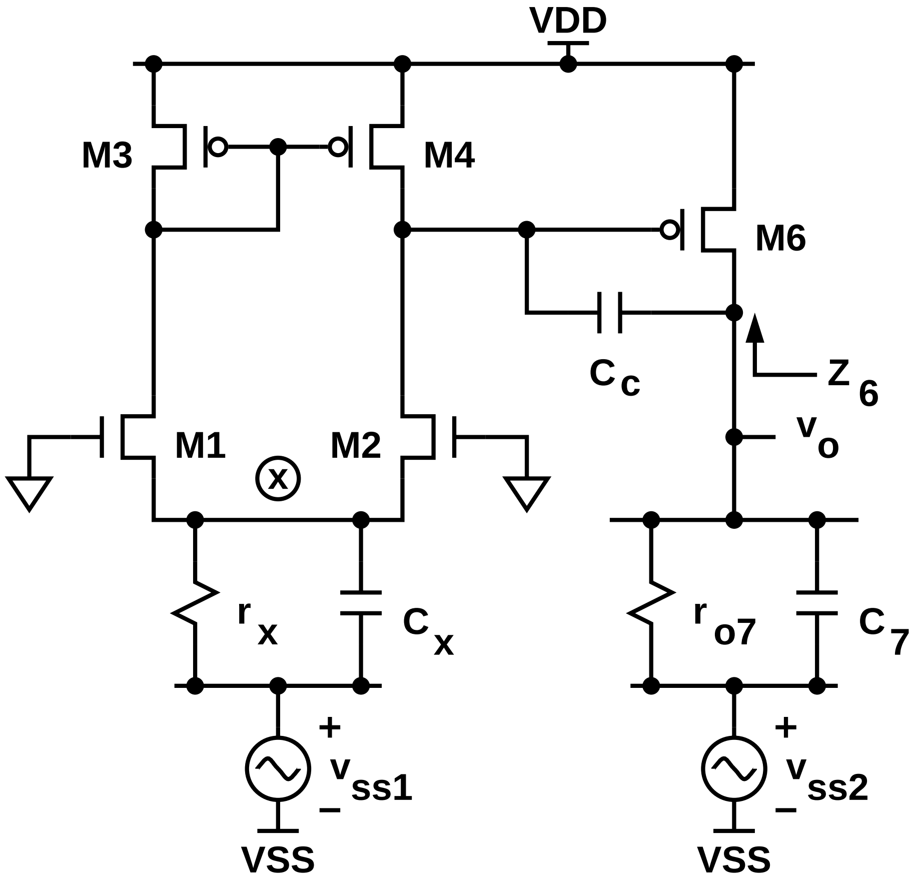
$$A_v = \frac{A_v(0)}{1 - s/p_1}$$

$$A_v(0) = g_{m1} g_{m6} R_1 R_2$$

$$A_v(0) p_1 = -\frac{g_{m1}}{C_c}$$

$$A_v \approx \frac{g_{m1}}{sC_c} \qquad \text{for} \quad \omega \gg |p_1|$$

Power Supply Rejection Ratio ($PSRR_{SS}$)



$$\frac{v_o}{v_{ss1}} = A_{v,cm} = \frac{A_v}{\text{CMRR}}$$

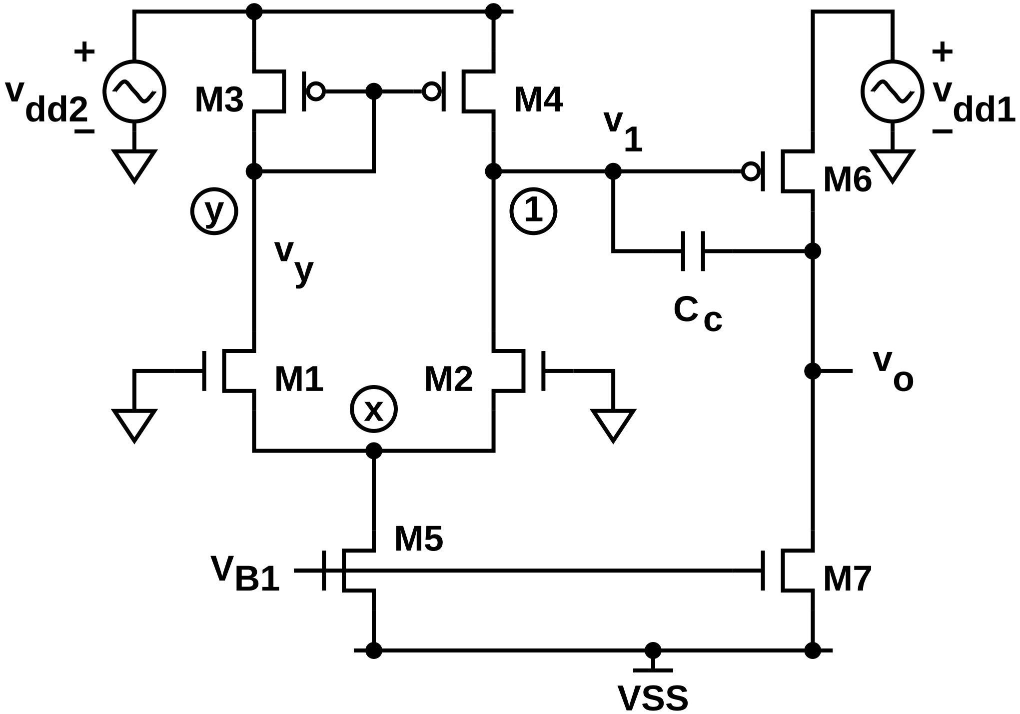
$$Z_6 \approx \frac{1}{g_{m6}}$$

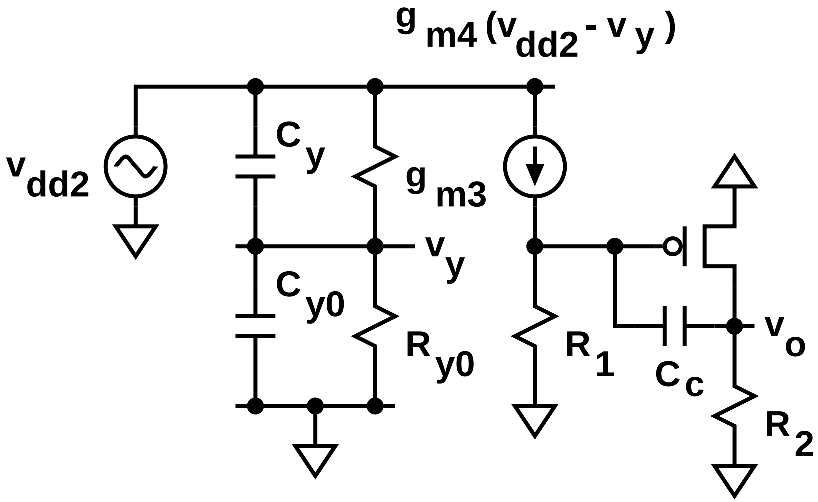
$$Z_7 = \frac{1}{g_{o7} + sC_7}$$

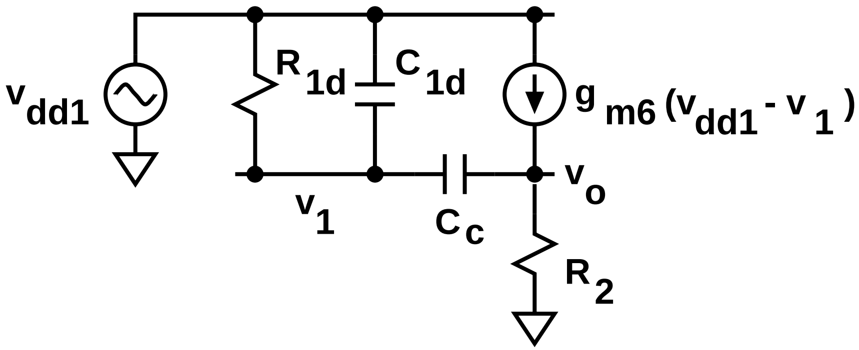
$$\frac{v_o}{v_{ss2}} = \frac{Z_6}{Z_6 + Z_7} \approx \frac{Z_6}{Z_7} \approx \frac{g_{o7} + sC_7}{g_{m6}}$$

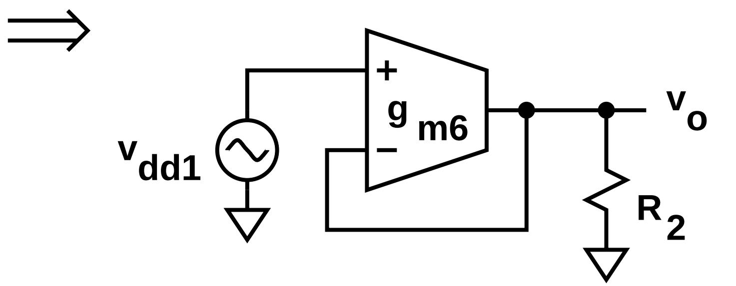
$$\frac{1}{\text{PSRR}_{SS}} = \frac{v_o/v_{ss1} + v_o/v_{ss2}}{A_v} = \frac{1}{\text{CMRR}} + \frac{(1 + sr_{o7}C_7)(1 - s/p_1)}{g_{m6}r_{o7}A_v(0)} \approx \frac{1}{\text{CMRR}}$$

Power Supply Rejection Ratio ($PSRR_{DD}$)









Power Supply Rejection Ratio (PSRR_{DD})

The voltage gain from v_{dd1} to v_o is

$$\frac{v_o}{v_{dd1}} = \frac{1}{1 + \frac{1+(g_{1d}+sC_{1d})/(sC_c)}{R_2(g_{1d}+sC_{1d})+g_{m6}R_2}} \approx \frac{1}{1 + \frac{C_{1d}/C_c}{g_{m6}R_2}} \approx 1$$

For v_{dd2} input, since $g_{m3} + sC_y \gg G_{y0} + sC_{y0}$, the resulting current flow in M3 is approximately

$$i_{y0} \approx v_{dd2} \cdot (g_{y0} + sC_{y0})$$

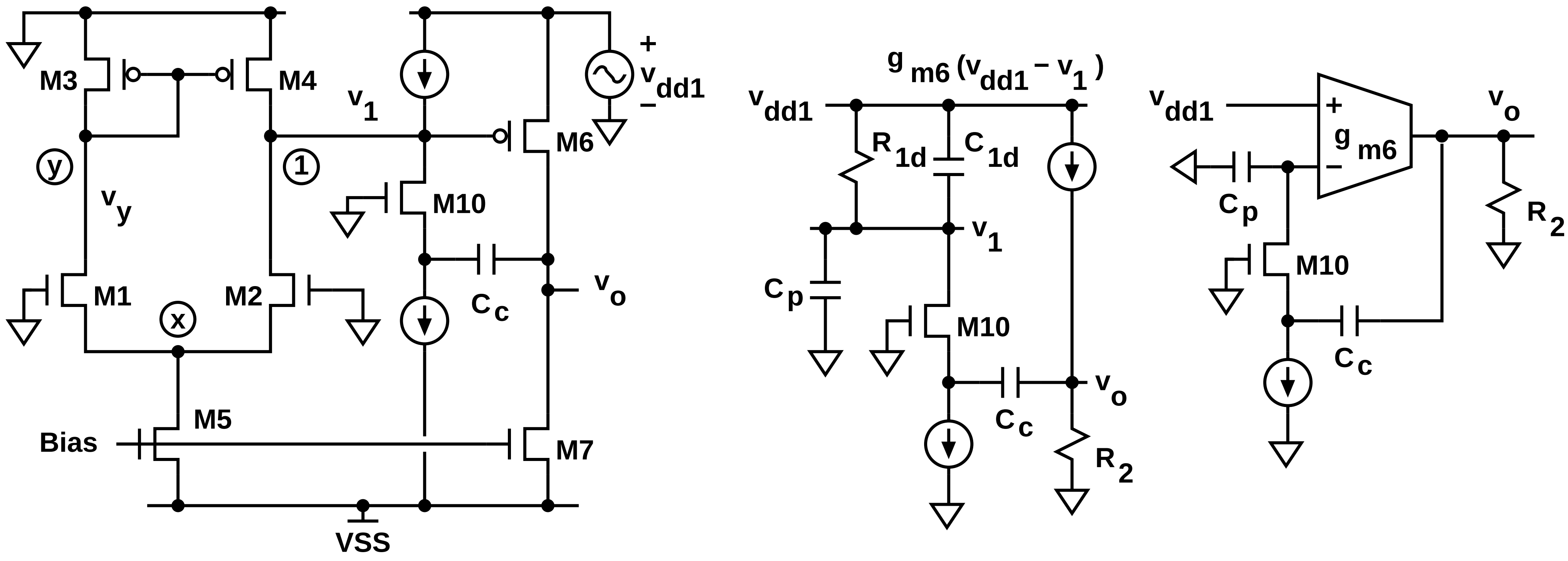
The current is mirrored in M4, and amplified by M6 and C_c. The voltage gain is

$$\frac{v_o}{v_{dd2}} = i_{y0} \cdot A_{v2} \approx -\frac{g_{y0} + sC_{y0}}{sC_c} \qquad \Rightarrow \qquad \frac{v_o}{v_{dd2}} \ll \frac{v_o}{v_{dd1}}$$

Thus

$$\text{PSRR}_{DD} \approx \frac{A_v}{v_o/v_{dd1}} \approx A_v$$

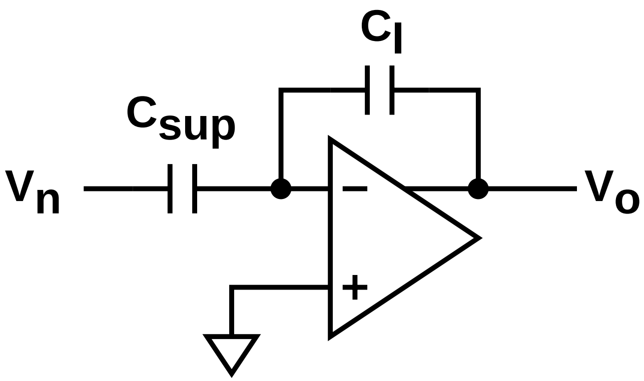
$PSRR_{DD}$ with Common-Gate Miller Compensation



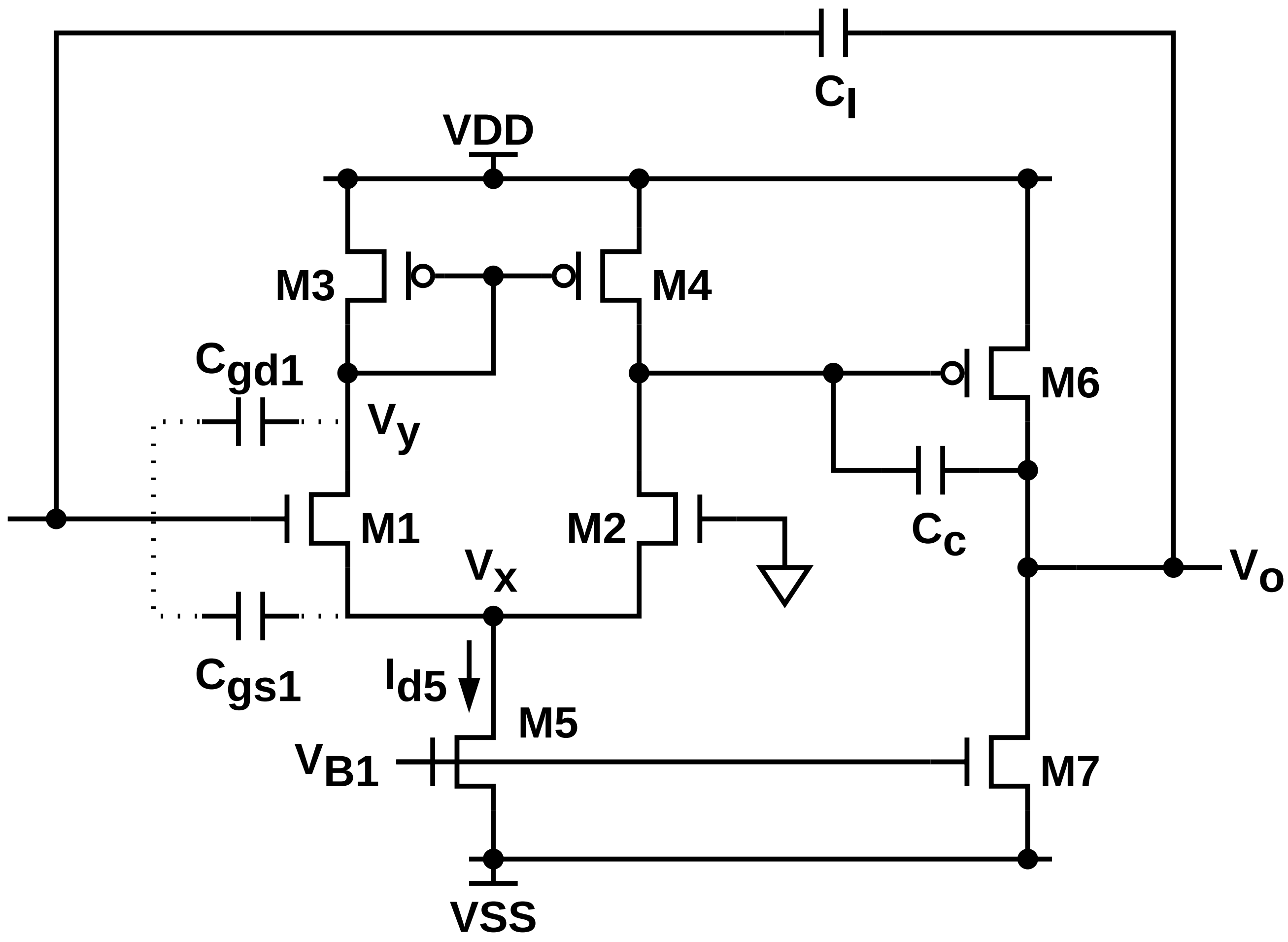
Assume the M10 stage has $R_{in} = 1/g_{m10}$ and $A_I = 1$. Neglecting R_{1d} and C_{1d}, we have

$$\frac{v_o}{v_{dd1}} = \frac{1}{\frac{1}{1+sC_c/g_{m10}} \cdot \left(\frac{C_c}{C_p} + \frac{sC_c}{g_{m6}}\right) + \frac{1}{g_{m6}R_2}} \approx \frac{C_p}{C_c} \cdot \left(1 + s\frac{C_c}{g_{m10}}\right)$$

Supply Capacitance



$$V_o = -\frac{C_{sup}}{C_l} \cdot V_n$$



- Both C_{gs1} and C_{gd1} can function as C_{sup}, and noises at V_x and V_y can leak to the output.

Power-Supply Rejection and Supply Capacitance

- The V_{DD} noise can be coupled to V_y through the diode-connected M3 device. The use of cascode input stage can overcome this problem.

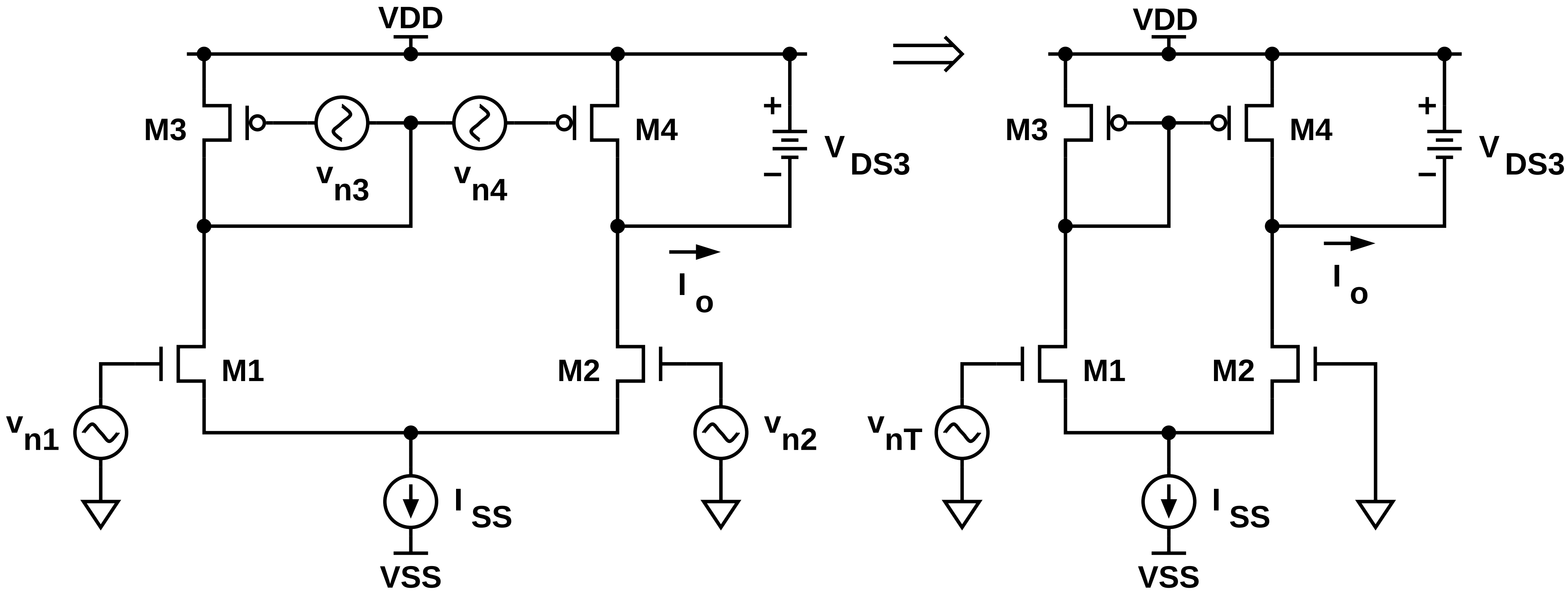
- If I_{d5} is modulated by the supply voltage variation, then $v_x \approx i_{d5}/(2g_{m1})$. The use of supply-independent bias reference can overcome this problem.

- The noises at the substrate/well terminals of M1 and M2 can change the V_t of the devices due to body effect, and cause V_{gs} variation, introducing noises at V_x. A solution is to place both M1 and M2 in a single well, and connect well and source terminals together to eliminate body effect.

- Interconnect crossovers can introduce undesired coupling capacitors to the V_{i-} summing node. Careful layout is required.

- Fully-differential circuit topology generally has better power-supply rejection performance.

Device Noise Analysis



$$\overline{v_n^2} \approx 4kT\left(\frac{2}{3}\cdot\frac{1}{g_m}\right) + \frac{K_f}{WLC_{ox}}\cdot\frac{1}{f} \qquad \overline{i_n^2} \approx 0$$

$$\overline{v_{nT}^2} = \overline{v_{n1}^2} + \overline{v_{n2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2\left(\overline{v_{n3}^2} + \overline{v_{n4}^2}\right)$$

Thermal Noise Performance

Assuming M1=M2 and M3=M4, and knowing $I_{D1} = I_{D3}$ so that

$$\left(\frac{g_{m3}}{g_{m1}}\right)^2 = \frac{\mu_p C_{ox}(W/L)_3}{\mu_n C_{ox}(W/L)_1} = \frac{\mu_p (W/L)_3}{\mu_n (W/L)_1} \qquad k'_n = \mu_n C_{ox} \qquad k'_p = \mu_p C_{ox}$$

The input referred thermal noise is

$$\frac{\overline{v^2_{(\Theta)T}}}{\Delta f} = 4kT\left(\frac{4}{3}\frac{1}{g_{m1}}\right) + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \times 4kT\left(\frac{4}{3}\frac{1}{g_{m3}}\right) = 4kT\left(\frac{4}{3}\frac{1}{g_{m1}}\right) \times \left[1 + \frac{g_{m3}}{g_{m1}}\right]$$

$$= 4kT\left(\frac{4}{3}\cdot\frac{1}{\sqrt{2k'_n(W/L)_1 I_{D1}}}\right) \times \left[1 + \sqrt{\frac{\mu_p}{\mu_n}\cdot\frac{(W/L)_3}{(W/L)_1}}\right]$$

- The load contribution can be made small by making $g_{m1} > g_{m3}$ or $(W/L)_1 > (W/L)_3$.
- g_{m1} should be made as large as possible to minimize thermal noise contribution.

Flicker Noise Performance

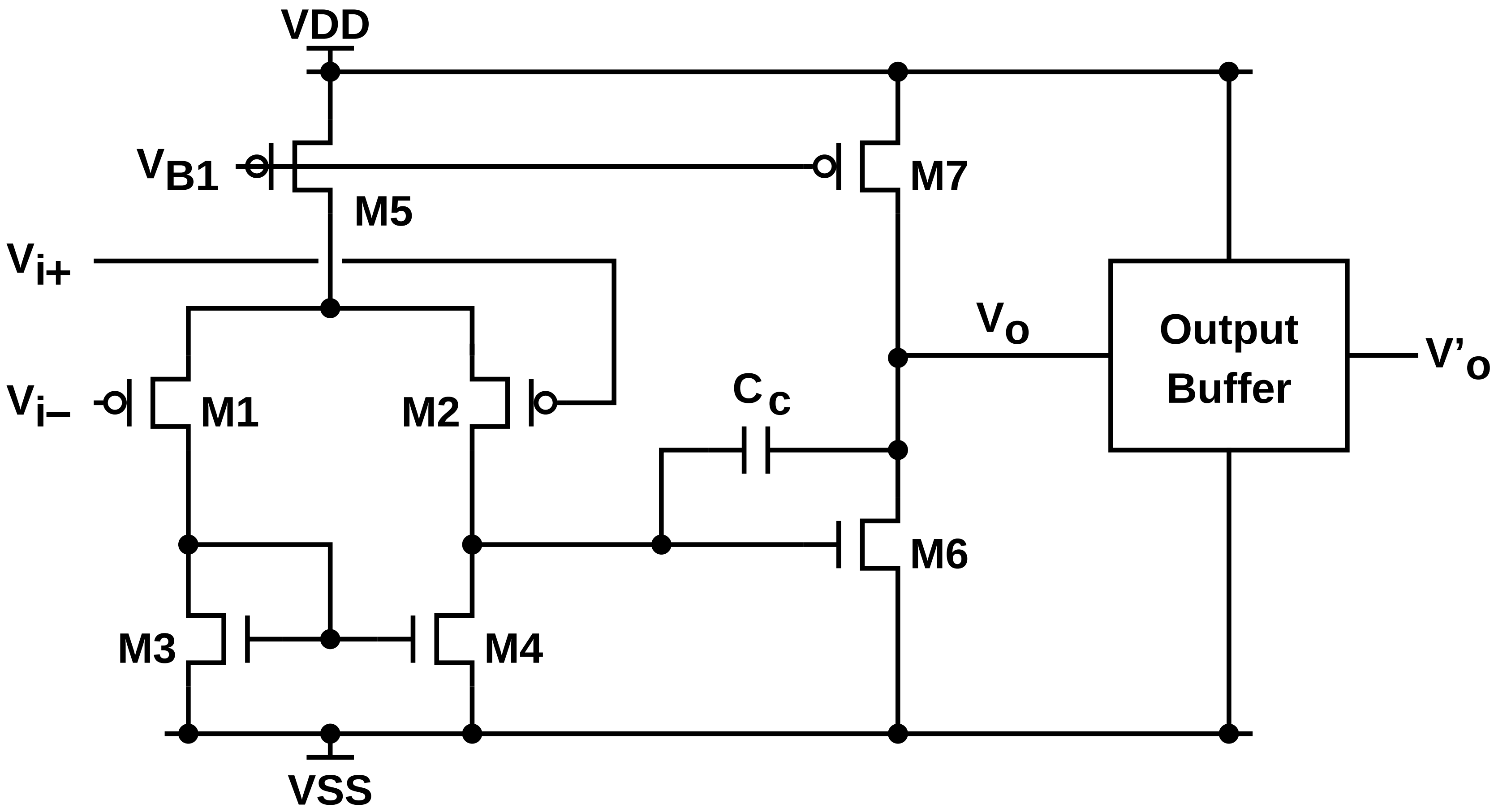
The input referred $1/f$ noise is

$$\frac{\overline{v^2_{(1/f)T}}}{\Delta f} = \frac{2K_{fn}}{W_1 L_1 C_{ox} f} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \times \frac{2K_{fp}}{W_3 L_3 C_{ox} f} = \frac{2K_{fn}}{W_1 L_1 C_{ox} f} + \frac{\mu_p (W/L)_3}{\mu_n (W/L)_1} \times \frac{2K_{fp}}{W_3 L_3 C_{ox} f}$$

$$= \frac{1}{f} \times \frac{2K_{fn}}{W_1 L_1 C_{ox}} \left(1 + \frac{K_{fp}}{K_{fn}} \cdot \frac{\mu_p}{\mu_n} \cdot \frac{L_1^2}{L_3^2}\right)$$

- K_{fp} is typically smaller than K_{fn} by a factor of two or more.
- The load contribution can be made small by making $L_3 > L_1$. But longer L_3 can limits the signal swing somewhat.
- The width of load devices does not affect the $1/f$ noise performance. But make it wider can maximize signal swing.
- Making W_1 wider can reduce $1/f$ noise.

2-Stage Opamp with pMOST Input Stage



2-Stage Opamp with pMOST Input Stage

Comparing to the nMOST-input opamps, the pMOST-input opamps have

- Similar dc voltage gain.
- Smaller g_{m1} and larger g_{m6}.
- Larger unity-gain frequency since $\omega_u \simeq |p_2|$ and $|p_2| = g_{m6}/C_2$.
- Better slew rate since both V_{ov1} and ω_u are larger.
- Better 1/f noise performance.
- Poorer thermal noise performance.