

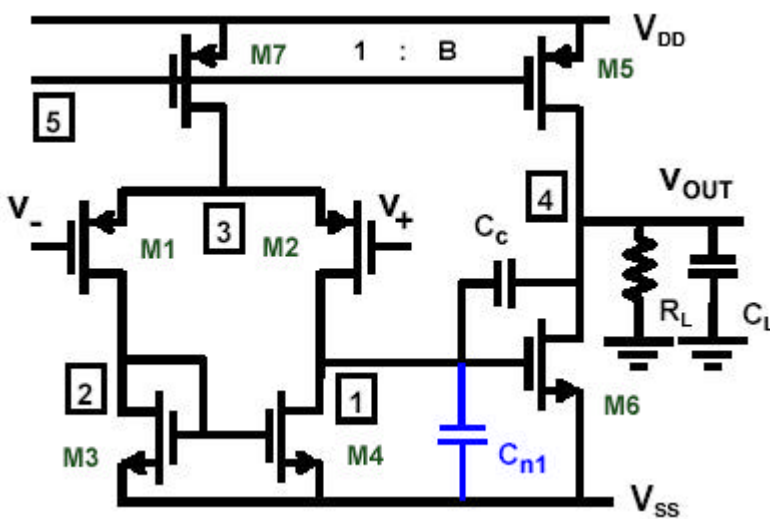
# Miller Opamp Design

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[www.sunshadow.co.uk/chris.htm](http://www.sunshadow.co.uk/chris.htm)

This sheet is used to design a low speed Miller Operational Amplifier, using the technique explained by **Willy Sansen** in his book "Analog Design Essentials" chapters 1 and 6, main slide 0629.

PMOS input devices are chosen as these normally have better matching and lower noise.  
 Cc in the following schematic is replaced with Cc and Rc in series.

Design Inputs yellow; BSIM inputs blue; outputs green



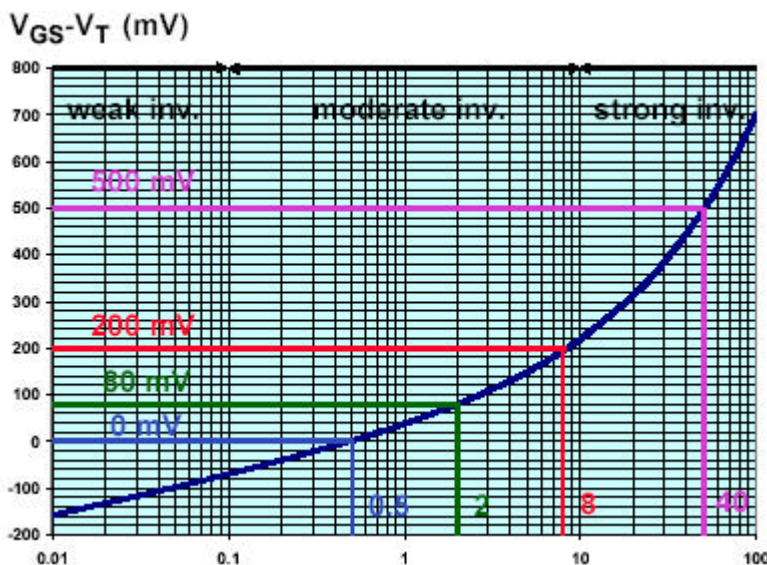
$$\text{kohm} := 1000 \cdot \text{ohm} \quad \mu\text{m} := \frac{\text{m}}{10^6}$$

$$q := 1.60217733 \cdot 10^{-19} \cdot \text{coul}$$

$$k_b := 1.380658 \cdot 10^{-23} \cdot \frac{\text{joule}}{\text{K}}$$

$$T := 270\text{K}$$

$$\epsilon_{\text{ox}} := 8.8542 \cdot 10^{-12} \cdot 3.9 \cdot \frac{\text{F}}{\text{m}}$$



The starting point of the analysis focuses on this graph, which shows the EKV model and gives the inversion coefficient for Vgs-Vt.

The EKV model allows a single equation to be used for both the strong inversion and weak inversion operating zones on the FET.

This model allows Vgs-Vt (Vgt) to be negative and typically vary from -0.2 to 0.5V. It is unusually positive, otherwise the ROUT is too low and we get no gain.

**STEP 1.** Design requirements in yellow. Blue are the BSIM3 MOS parameters.

$$CL = \alpha Cc, Cc = \beta Cgs6, F6 = \gamma GBW$$

Normally these are 2 3 2

$$C_L := 1pF$$

$$GBW := 20MHz$$

$$V_{gt6} := 0.2V$$

$$\alpha := 3$$

$$\beta := 3$$

$$\gamma := 2$$

$$TOX := 5 \cdot 10^{-9} m$$

$$U_{0n} := 388 \frac{cm^2}{V \cdot s}$$

$$U_{An} := 6.5 \times 10^{-9} \frac{m}{V}$$

$$U_{Bn} := 4.2 \times 10^{-18} \cdot \frac{m^2}{V^2}$$

$$NFACTOR_n := 1.14$$

$$V_{TH0n} := 0.633V$$

$$VSAT_n := 86301 \frac{m}{s}$$

$$U_{0p} := 139 \frac{cm^2}{V \cdot s}$$

$$U_{Ap} := 1.399 \times 10^{-9} \frac{m}{V}$$

$$U_{Bp} := 1.0 \times 10^{-19} \cdot \frac{m^2}{V^2}$$

$$NFACTOR_p := 1.54$$

$$V_{TH0p} := 0.673V$$

$$VSAT_p := 103503 \frac{m}{s}$$

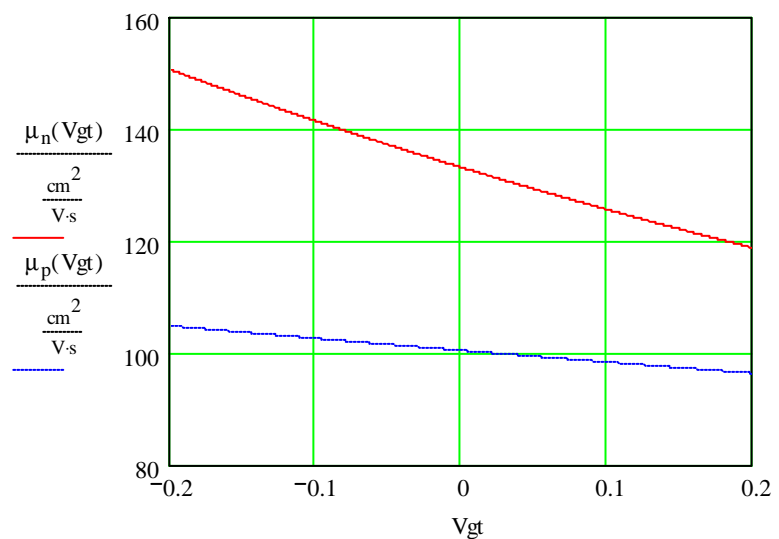
**STEP 2.** From  $U_0$  and the other BSIM mobility parameters, we can calculate the mobility for the NMOS and the PMOS devices, as this changes with  $V_{gt}$ . The equations for this are from **W Liu "Mosfet Models for Spice Simulation", page 249**. I assume  $MOBMOD=1$  which is the default.

$$\mu_n(V_{gt}) := \frac{U_{0n}}{1 + U_{An} \cdot \frac{V_{gt} + 2 \cdot V_{TH0n}}{TOX} + U_{Bn} \cdot \left( \frac{V_{gt} + 2 \cdot V_{TH0n}}{TOX} \right)^2}$$

$$\mu_p(V_{gt}) := \frac{U_{0p}}{1 + U_{Ap} \cdot \frac{V_{gt} + 2 \cdot V_{TH0p}}{TOX} + U_{Bp} \cdot \left( \frac{V_{gt} + 2 \cdot V_{TH0p}}{TOX} \right)^2}$$

$$\mu_n(V_{gt6}) = 118.769 \frac{cm^2}{V \cdot s}$$

This shows how the mobility changes with  $V_{gt}$  for NMOS and PMOS



**STEP 3.** Calculate FT (frequency at which gain equals 1) for transistor M6 to get the gain-bandwidth. From this we can calculate L (Gate Length) and we use the same L for most of the transistors. The EKV model is used, as this is what Samson uses, refer slides: **0138, 0140, 0165, 0627**. The gate length needs to be at least twice the minimum.

$$V_{GSTtn} := 2 \cdot NFACTOR_n \cdot \frac{k_b \cdot T}{q} \quad \mathbf{0138} \quad i(Vgt) := \left[ \ln \left[ e^{\left( \frac{Vgt}{V_{GSTtn}} \right)} + 1 \right] \right]^2 \quad \mathbf{0138}$$

$$GM(Vgt) := \frac{1 - e^{-\sqrt{i(Vgt)}}}{\sqrt{i(Vgt)}} \quad \mathbf{0140} \quad F_T := \alpha \cdot \beta \cdot \gamma \cdot \left( 1 + \frac{1}{\beta} \right) \cdot GBW \quad \mathbf{0627}$$

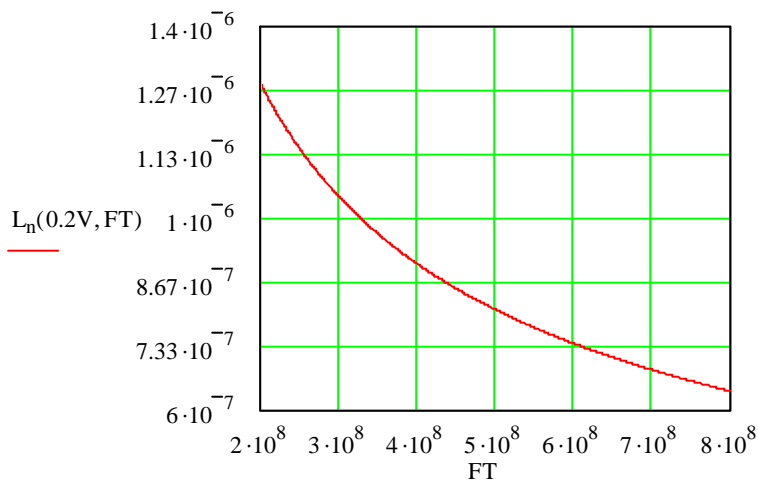
$$L_n(Vgt, F_T) := \sqrt{\frac{\mu_n(Vgt) \cdot \frac{k_b \cdot T}{q}}{\pi \cdot F_T} \cdot \left[ \sqrt{i(Vgt)} \cdot \left( 1 - e^{-\sqrt{i(Vgt)}} \right) \right]} \quad \mathbf{0165}$$

$$V_{GSTtn} = 0.053 \text{ V}$$

$$i(Vgt6) = 14.386$$

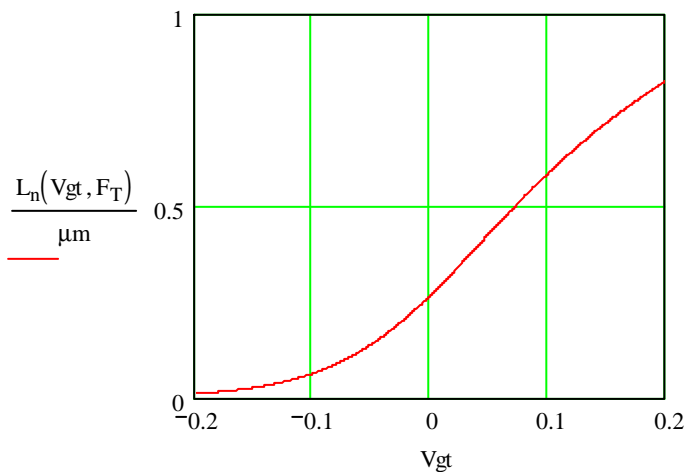
$$F_T = 480 \text{ MHz}$$

$$L_n(Vgt6, F_T) = 0.824 \mu\text{m}$$



$$L := 2\mu\text{m}, 2.1\mu\text{m}.. 10\mu\text{m}$$

This graph shows how the length of the gate influences the FT (frequency at which gain is 1)



We also get this strange graph that shows how the required gate length changes with Vgt.

**STEP 4.** Use the following equations to calculate the widths and currents of M6 and M5, which are dependent on CL.

$$C_c := \frac{C_L}{\alpha} \quad C_{gs6} := \frac{C_L}{\alpha \cdot \beta} \quad \mathbf{0621} \quad C_{ox} := \frac{\epsilon_{ox}}{TOX} \quad W_6 := C_{gs6} \cdot \frac{3}{2} \cdot \frac{1}{L_n(V_{gt6}, F_T) \cdot C_{ox}} \quad \mathbf{0161}$$

$$I_{DSt6} := \mu_n(V_{gt6}) \cdot C_{ox} \cdot \frac{W_6}{L_n(V_{gt6}, F_T)} \cdot (V_{GSTtn})^2 \quad I_{DS6} := I_{DSt6} \cdot \left( \ln \left( 1 + e^{\ln(e^{\sqrt{i(V_{gt6})} - 1)}} \right) \right) \quad \mathbf{0138}$$

$$g_{m6} := \frac{GM(V_{gt6}) \cdot I_{DS6} \cdot 2}{V_{GSTtn}} \quad \mathbf{0141} \quad R_c := \frac{1}{g_{m6}} \quad I_{DSt6} = 8.199 \mu A \quad C_c = 0.333 pF$$

$$I_{DS6} = 31.099 \mu A \quad W_6 = 29.278 \mu m$$

Rc is calculated according to notes from Redman-White

$$R_c = 3.31 \text{ kohm}$$

$$g_{m6} = 0.302 \frac{mA}{V}$$

**STEP 5.** We need the Early voltage for M6 so that we can calculate the output resistance to get the voltage gain. From this we can convert Cc to the equivalent input capacitance from the Miller equation. **W Liu "Mosfet Models for Spice Simulation", equations A-62, A-78.** The equivalent Early voltage is VA and this converts to the ro6 by the slope at the point of operation. The output impedance is halved as M5 needs to be considered and is assumed to be equal to rout of M6. Also a 1/2 adjustment is made for ro, as we are working near VTH0 and ro is reduced.

$$\epsilon_{sat6} := \frac{2 \cdot VSAT_n}{\mu_n(V_{gt6})} \quad VA6 := \epsilon_{sat6} \cdot L_n(V_{gt6}, F_T) \quad ro6 := \frac{1}{2} \left( \frac{VA6 + V_{TH0n} + V_{gt6}}{I_{DS6}} \right)$$

$$V_{gain6} := g_{m6} \cdot \frac{ro6}{2} \quad C_{n1} := C_{gs6} + (1 + V_{gain6}) \cdot C_c \quad ro6 = 2.06 \times 10^5 \text{ ohm} \quad VA6 = 11.979 V$$

$$C_{n1} = 10.818 pF \quad V_{gain6} = 31.119$$

**STEP 6.** Now scale M1 and M2. Keep Vgt1 low to minimise noise. B needs to be high to save current. L needs to be greater than twice the process minimum.

$$B := 1$$

$$V_{gt1} := 0.1V$$

$$g_{m1} := 2 \cdot \pi \cdot C_{n1} \cdot GBW \quad \mathbf{063} \quad I_{DS1} := \frac{I_{DS6}}{2 \cdot B} \quad GM1 := \frac{g_{m1}}{I_{DS1}} \cdot NFACTOR_p \cdot \frac{k_b \cdot T}{q} \quad \mathbf{0141}$$

$$i := 1 \quad \text{Given} \quad GM1 = \frac{1 - e^{-\sqrt{i}}}{\sqrt{i}} \quad i := \text{Find}(GM1)$$

$$V_{GSTtp} := 2 \cdot NFACTOR_p \cdot \frac{k_b \cdot T}{q} \quad L_p := \sqrt{\frac{\mu_p(V_{gt1}) \cdot \frac{k_b \cdot T}{q} \cdot \left[ \sqrt{i} \cdot \left( 1 - e^{-\sqrt{i}} \right) \right]}{\pi \cdot \frac{F_T}{4}}} \quad \mathbf{0165} \quad \text{and } \mathbf{065} \text{ for } FT$$

$$W_1 := \frac{\frac{I_{DS1}}{i} \cdot L_p}{\mu_p(V_{gt1}) \cdot C_{ox} \left[ (V_{GSTtp})^2 \right]}$$

0138

$$g_{m1} = 1.359 \frac{\text{mA}}{\text{V}}$$

$$L_p = 0.515 \mu\text{m}$$

$$W_1 = 36.276 \mu\text{m}$$

$$W_4 := \frac{W_6}{2} \cdot \frac{1}{B}$$

**STEP 7.** Calculate the voltage gain for stage 1 and then calculate the overall voltage gain. The output resistance is the Early voltage divided by the current. This is halved because both there are two FETS and the gain is halved again as we are working near VTH0 and the output resistance is slightly lower at this point.

$$\epsilon_{sat1} := \frac{2 \cdot V_{SATp}}{\mu_p(V_{gt1})}$$

$$VA1 := \epsilon_{sat1} \cdot L_p$$

$$ro1 := \frac{1}{2} \left( \frac{VA1 + V_{TH0p} + V_{gt1}}{\frac{I_{DS1}}{2}} \right)$$

$$VA1 = 10.827 \text{ V}$$

$$V_{gain1} := g_{m1} \cdot \frac{ro1}{2}$$

$$\text{Gain}_{dB} := 20 \log(V_{gain1} \cdot V_{gain6})$$

$$V_{gain1} = 507.055$$

## Summary of circuit values

$$L_n(V_{gt6}, F_T) = 0.824 \mu\text{m}$$

$$L_p = 0.515 \mu\text{m}$$

$$C_c = 0.333 \text{ pF}$$

$$I_{DS6} = 31.099 \mu\text{A}$$

$$W_6 = 29.278 \mu\text{m}$$

$$W_1 = 36.276 \mu\text{m}$$

$$R_c = 3.31 \text{ kohm}$$

$$\text{Gain}_{dB} = 83.962$$

$$W_4 = 14.639 \mu\text{m}$$

$L_n$  is the length of all devices except M1 and M2

$L_p$  is the length of M1 and M2

$R_c$  is the usually done with an NMOS

$W_6$  is the width of M6, M5 and M7.

$W_1$  is the width of M1 and M2

$W_4$  is the width of M3 and M4

**Simulations.** The amplifier is simulated using the BSIM3 parameters available from the BSIM3 website at Berkeley (and used in the calculations). The current reference is set to 31uA. Output range is to within 300mV of the rails.

The GBW is tested using a feedback amplifier configuration as a buffer, i.e connecting the output to the negative input and inputing a signal on the positive. The GBW is measured as 100MHz, whereas the design aim was 20MHz, but there is clearly some peaking here so not the best measure but the easiest one!!

The gain is measured by sweeping one input relative to the other. There is a difference to calculated I suspect because RON is less than I use here in the calculations. I am not sure how to get a better simple estimate. I already reduce the RON by 2 from the calculated value using VA. The Early voltage VA is very accurate.

A transient response is also plotted also with the feedback amp to check stability.

On the whole, a resonable amplifier.

$$\text{gain}_{\text{dB}} := 20 \cdot \log\left(\frac{2.73 - 0.284}{1.5008 - 1.499}\right)$$

$$\text{gain}_{\text{dB}} = 62.664$$

