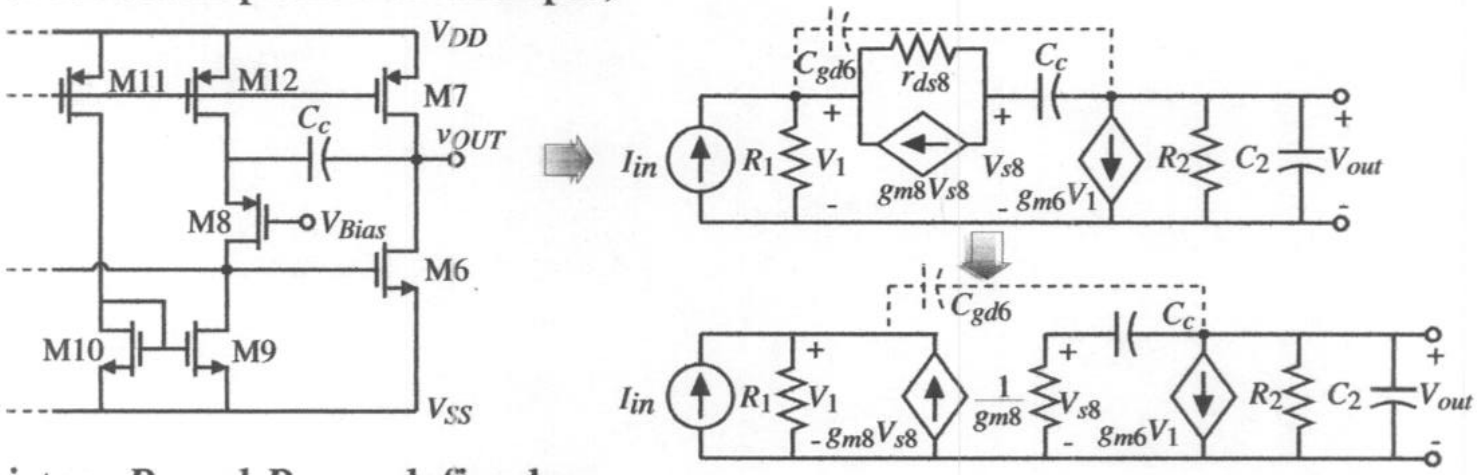
CMOS Operational Amplifier (2)

Increasing the magnitude of the output pole

The magnitude of the output pole , p_2, can be increased by introducing gain in the Miller capacitor feedback path. For example,



The resistors R_1 and R_2 are defined as

$$R_1 = \frac{1}{g_{ds2} + g_{ds4} + g_{ds9}} \qquad \text{and } R_2 = \frac{1}{g_{ds6} + g_{ds7}}$$

where transistors M2 and M4 are the output transistors of the first stage.

Nodal equations:

$$I_{in} = G_1 V_1 - g_{m8} V_{s8} = G_1 V_1 - \left(\frac{g_{m8} s C_c}{g_{m8} + s C_c}\right) V_{out} \quad \text{and} \quad 0 = g_{m6} V_1 + \left[G_2 + s C_2 + \frac{g_{m8} s C_c}{g_{m8} + s C_c}\right] V_{out}$$

Increasing the magnitude of the output pole

Solving for the transfer function V_{out}/I_{in} gives,

$$\frac{V_{out}}{I_{in}} = \left(\frac{-g_{m6}}{G_1 G_2}\right)\left[\frac{\left(1+\frac{sC_c}{g_{m8}}\right)}{1+s\left[\frac{C_c}{g_{m8}}+\frac{C_2}{G_2}+\frac{C_c}{G_2}+\frac{g_{m6}C_c}{G_1G_2}\right]+s^2\left(\frac{C_cC_2}{g_{m8}G_2}\right)}\right]$$

Using the approximate method of solving for the roots of the denominator gives

$$p_1 = \frac{-1}{\frac{C_c}{g_{m8}}+\frac{C_c}{G_2}+\frac{C_2}{G_2}+\frac{g_{m6}C_c}{G_1G_2}} \approx \frac{-6}{g_{m6}r_{ds}^2C_c}$$

and

$$p_2 \approx \frac{-\frac{g_{m6}r_{ds}^2C_c}{6}}{\frac{C_cC_2}{g_{m8}G_2}} = \frac{g_{m8}r_{ds}^2G_2}{6}\left(\frac{g_{m6}}{C_2}\right) = \left(\frac{g_{m8}r_{ds}}{3}\right)|p_2'|$$

where all the various channel resistance have been assumed to equal r_{ds} and p_2' is the output pole for normal Miller compensation.

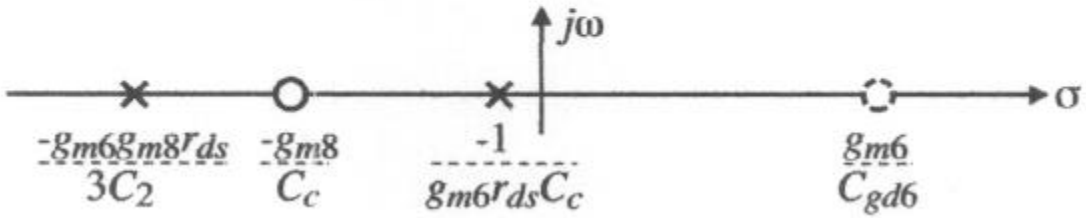
Result:

Dominant pole is approximately the same and the output pole is increased by $\approx g_m r_{ds}$.

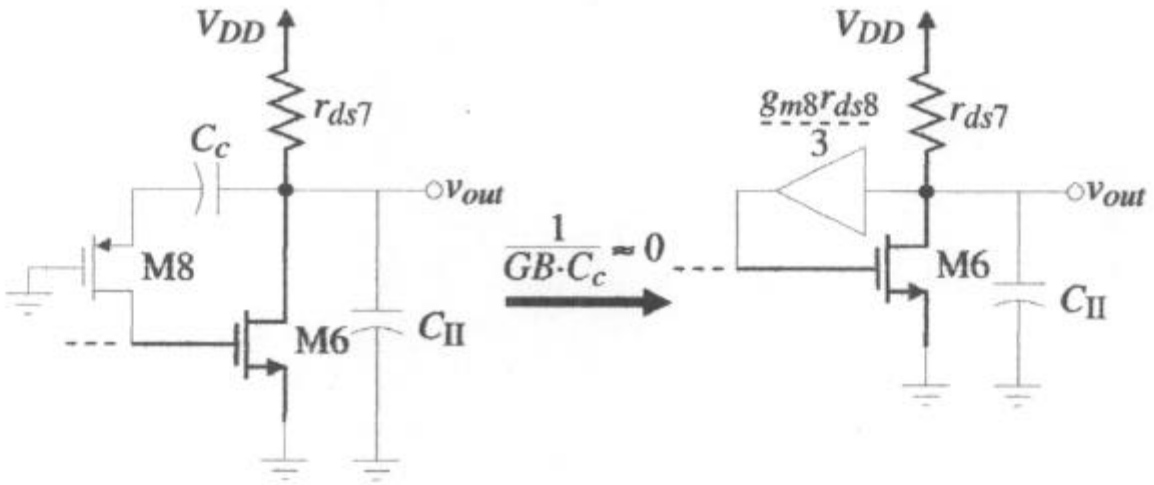
Increasing the magnitude of the output pole

In addition there is a LHP zero at $-g_{m8}/sC_c$ and a RHP zero due to C_{gd6} (shown dashed in the model) at g_{m6}/C_{gd6}.

Roots are:



Concept behind the increasing of magnitude of the output pole



$$R_{out} = r_{ds7} \| \left(\frac{3}{g_{m6} g_{m8} r_{ds8}} \right) \approx \frac{3}{g_{m6} g_{m8} r_{ds8}}$$

Therefore, the output pole is approximately,

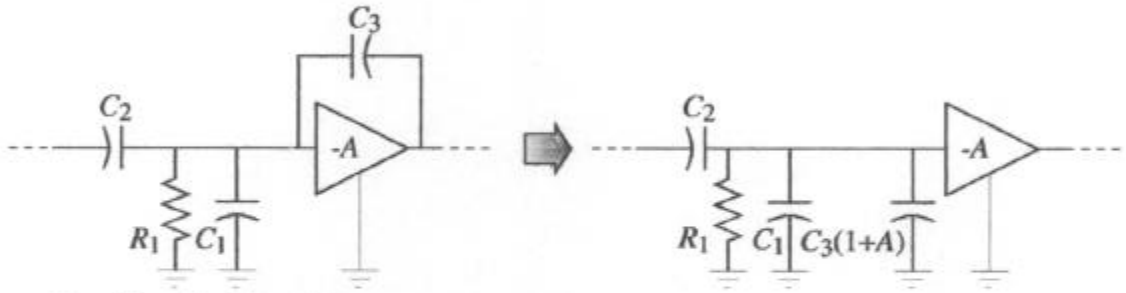
$$|p_2| \approx \frac{g_{m6} g_{m8} r_{ds8}}{3 C_{II}}$$

Identification of poles from a schematic

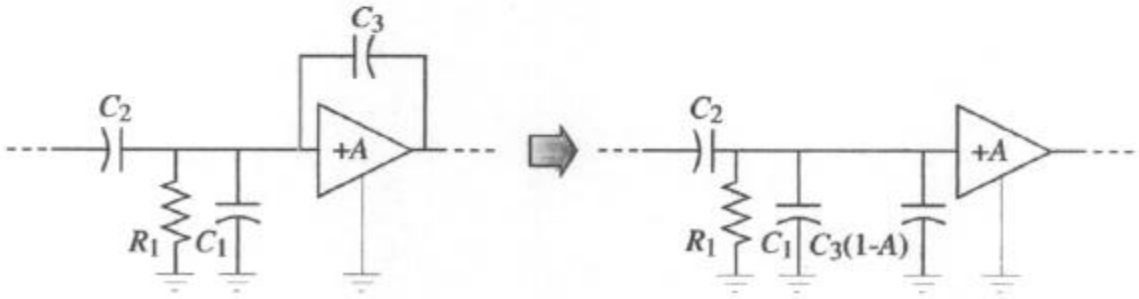
1.) Most poles are equal to the reciprocal product of the resistance from a node to ground and the capacitance connected to that node.

2.) Exceptions (generally due to feedback):

a.) Negative feedback:

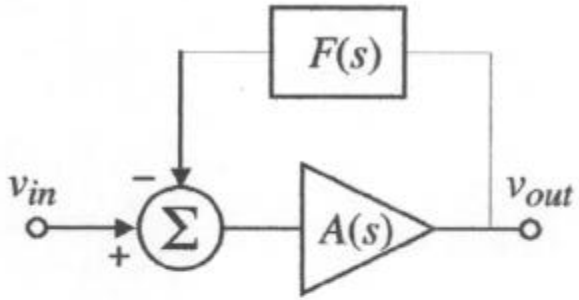


b.) Positive feedback (A<1):



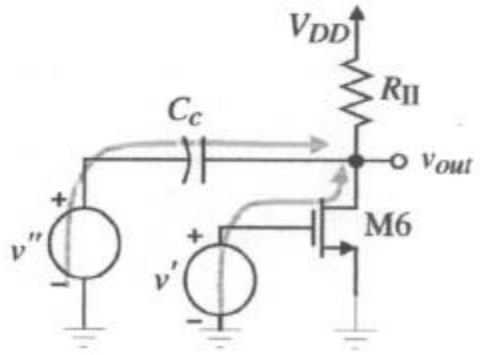
Identification of zeros from a schematic

1.) Zeros arise from poles in the feedback path.



$$\text{If } F(s)=\frac{1}{\frac{s}{p_1}+1}\text{, then } \frac{V_{out}}{V_{in}}=\frac{A(s)}{1+A(s)F(s)}=\frac{A(s)}{1+A(s)\frac{1}{\frac{s}{p_1}+1}}=\frac{A(s)\left(\frac{s}{p_1}+1\right)}{\frac{s}{p_1}+1+A(s)}$$

2.) Zeros are also created by two paths from the input to the output and one of more of the paths is frequency dependent.



Feedforward compensation

Use two parallel paths to achieve a LHP zero for lead compensation purposes.

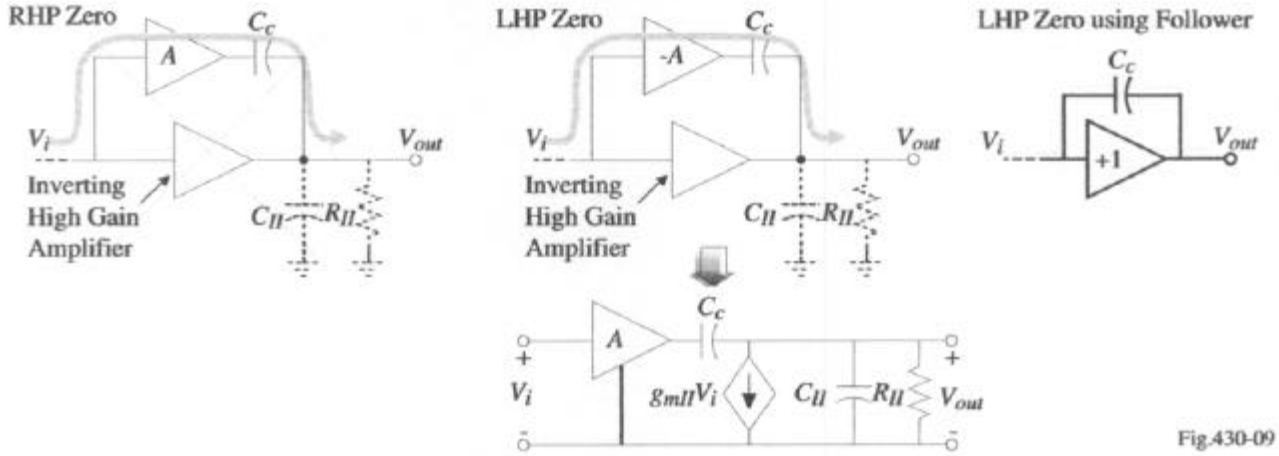


Fig.430-09

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{AC_c}{C_c + C_{II}}\left(\frac{s + g_{mII}/AC_c}{s + 1/[R_{II}(C_c + C_{II})]}\right)$$

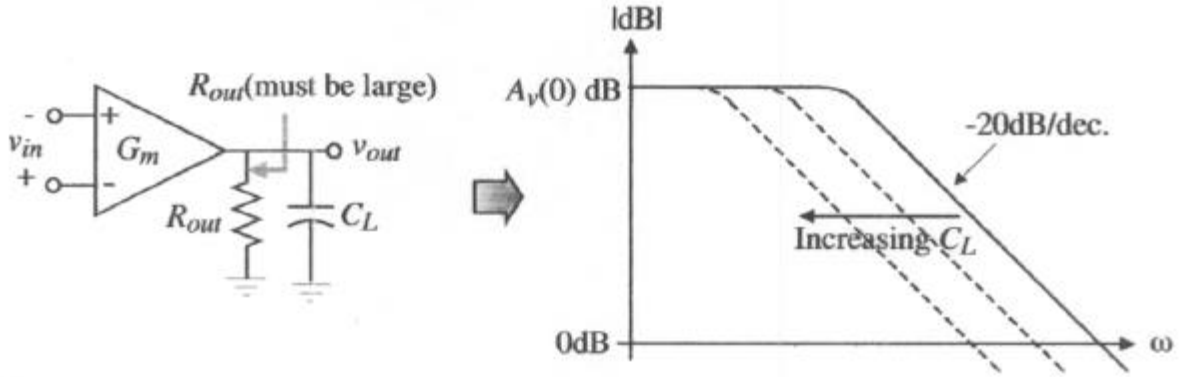
To use the LHP zero for compensation, a compromise must be observed.

- Placing the zero below *GB* will lead to boosting of the loop gain that could deteriorate the phase margin.
- Placing the zero above *GB* will have less influence on the leading phase caused by the zero.

Note that a source follower is a good candidate for the use of feedforward compensation.

Self-compensated Op Amp

Self compensation occurs when the load capacitor is the compensation capacitor (can never be unstable for resistive feedback)



Voltage gain:

$$\frac{v_{out}}{v_{in}} = A_v(0) = G_m R_{out}$$

Dominant pole:

$$p_1 = \frac{-1}{R_{out} C_L}$$

Unity-gainbandwidth:

$$GB = A_v(0) \cdot |p_1| = \frac{G_m}{C_L}$$

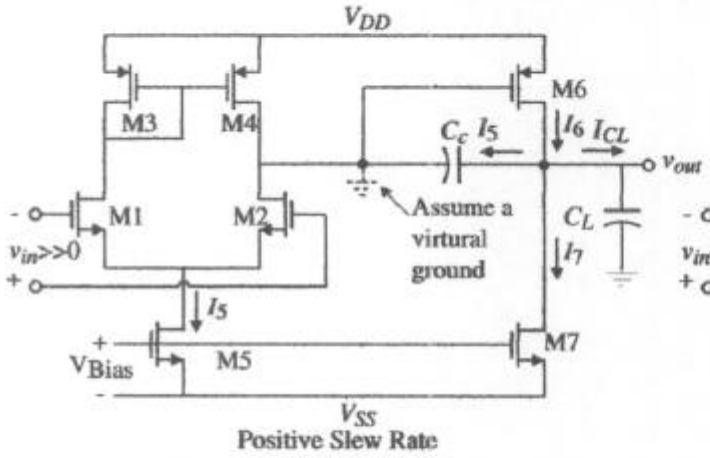
Stability:

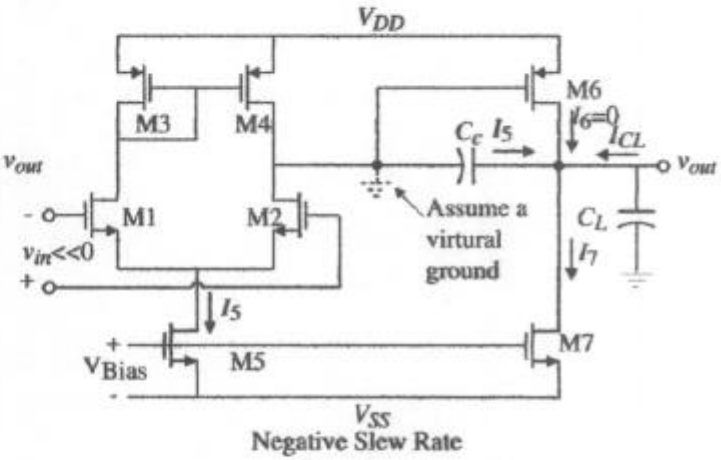
Large load capacitors simply reduce *GB* but the phase is still 90° at *GB*.

Slew Rate of a two-stage CMOS Op Amp

Remember that slew rate occurs when currents flowing in a capacitor become limited and is given as

$I_{lim} = C\frac{dv_C}{dt}$ where v_C is the voltage across the capacitor C.



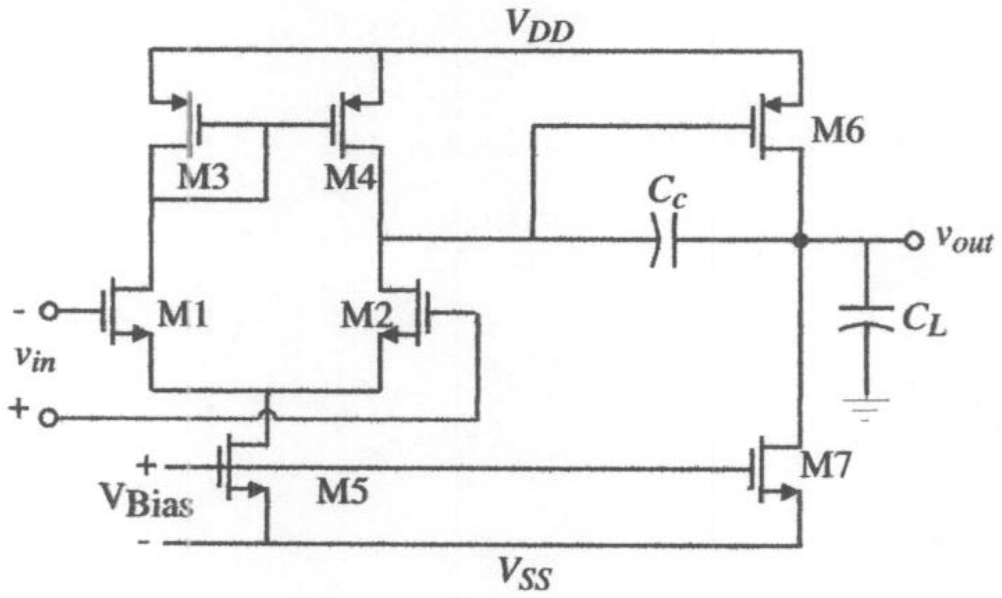


$SR^+ = \min\left[\frac{I_5}{C_c}, \frac{I_6-I_5-I_7}{C_L}\right] = \frac{I_5}{C_c}$ because $I_6 >> I_5$ $\quad SR^- = \min\left[\frac{I_5}{C_c}, \frac{I_7-I_5}{C_L}\right] = \frac{I_5}{C_c}$ if $I_7 >> I_5$.

Therefore, if C_L is not too large and if I_7 is significantly greater than I_5, then the slew rate of the two-stage op amp should be,

$$SR = \frac{I_5}{C_c}$$

Two stage op amp design



Notation:

$$S_i = \frac{W_i}{L_i} = W/L \text{ of the ith transistor}$$

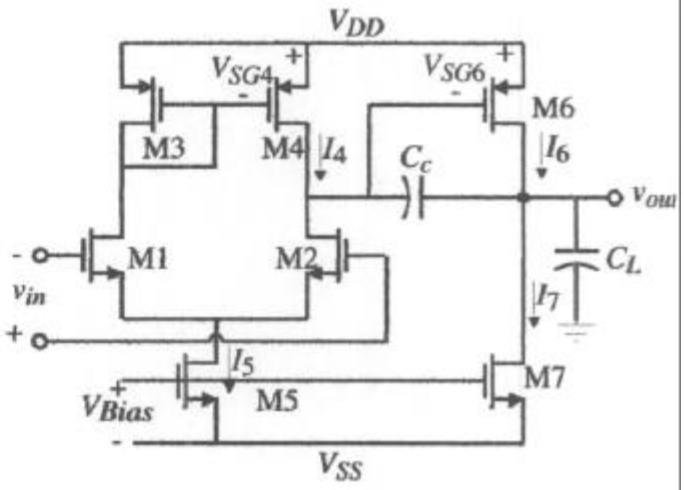
DC Balance conditions for the two stage op amp

For best performance, keep all transistors in saturation.

M4 is the only transistor that cannot be forced into saturation by internal connections or external voltages.

Therefore, we develop conditions to force M4 to be in saturation.

1.) First *assume* that $V_{SG4} = V_{SG6}$. This will cause "proper mirroring" in the M3-M4 mirror. Also, the gate and drain of M4 are at the same potential so that M4 is "guaranteed" to be in saturation.



2.) *If* $V_{SG4} = V_{SG6}$, then $I_6 = \left(\frac{S_6}{S_4}\right) I_4$

3.) However, $I_7 = \left(\frac{S_7}{S_5}\right) I_5 = \left(\frac{S_7}{S_5}\right) (2I_4)$

4.) For balance, I_6 must equal $I_7 \Rightarrow$ $\boxed{\frac{S_6}{S_4} = \frac{2S_7}{S_5}}$ called the "balance conditions"

5.) So if the balance conditions are satisfied, then $V_{DG4} = 0$ and M4 is saturated.

Design relationships for the two stage op amp

Slew rate $SR = \frac{I_5}{C_c}$ (Assuming $I_7 >> I_5$ and $C_L > C_c$)

First-stage gain $A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(\lambda_2 + \lambda_4)}$

Second-stage gain $A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(\lambda_6 + \lambda_7)}$

Gain-bandwidth $GB = \frac{g_{m1}}{C_c}$

Output pole $p_2 = \frac{-g_{m6}}{C_L}$

RHP zero $z_1 = \frac{g_{m6}}{C_c}$

60° phase margin requires that $g_{m6} = 2.2g_{m2}(C_L/C_c)$ if all other roots are $\geq 10GB$.

Positive ICMR $V_{\text{in(max)}} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|_{(\max)} + V_{T1(\min)})$

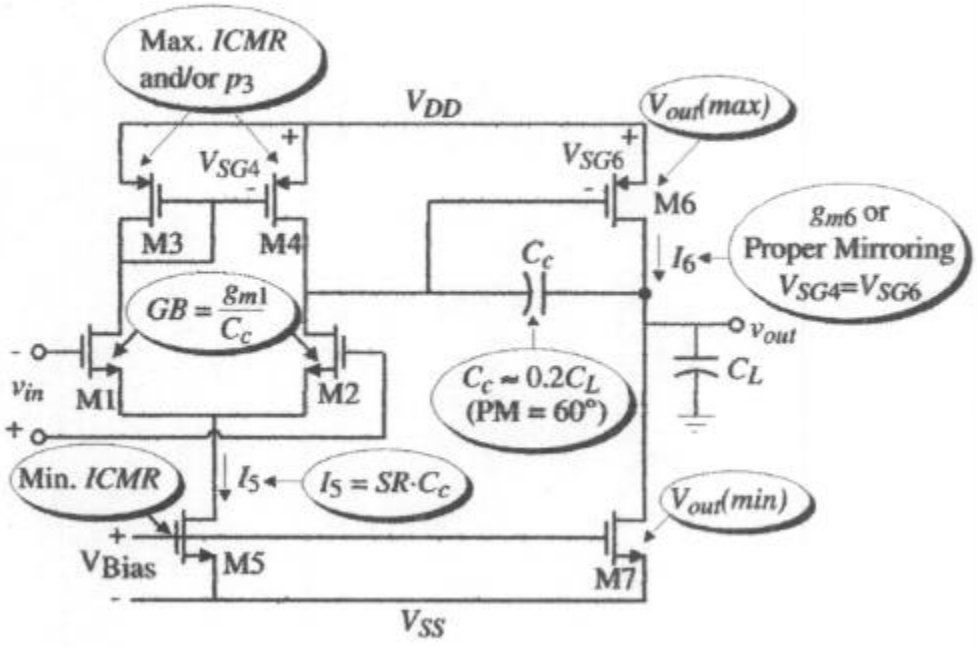
Negative ICMR $V_{\text{in(min)}} = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1(\max)} + V_{DS5}(\text{sat})$

Saturation voltage $V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}}$ (all transistors are saturated)

Op Amp specification

The following design procedure assumes that specifications for the following parameters are given.

1. Gain at dc, $A_v(0)$
2. Gain-bandwidth, *GB*
3. Phase margin (or settling time)
4. Input common-mode range, ICMR
5. Load Capacitance, C_L
6. Slew-rate, *SR*
7. Output voltage swing
8. Power dissipation, P_{diss}



Unbuffered Op Amp Design Procedure

This design procedure assumes that the gain at dc (A_v), unity gain bandwidth (GB), input common mode range (V_{in}(min) and V_{in}(max)), load capacitance (C_L), slew rate (SR), settling time (T_s), output voltage swing (V_{out}(max) and V_{out}(min)), and power dissipation (P_{diss}) are given. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.

1. From the desired phase margin, choose the minimum value for C_c, i.e. for a 60° phase margin we use the following relationship. This assumes that $z \geq 10GB$.

$$C_c > 0.22C_L$$

2. Determine the minimum value for the "tail current" (I_5) from the largest of the two values.

$$I_5 = SR \cdot C_c \qquad \text{or} \qquad I_5 = 10\left(\frac{V_{DD} + |V_{SS}|}{2 \cdot T_s}\right)$$

3. Design for S_3 from the maximum input voltage specification.

$$S_3 = \frac{I_5}{K'_3[V_{DD} - V_{in}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2}$$

4. Verify that the pole of M3 due to C_{gs3} and C_{gs4} ($= 0.67W_3L_3C_{ox}$) will not be dominant by assuming it to be greater than 10 GB

$$\frac{g_{m3}}{2C_{gs3}} > 10GB.$$

Unbuffered Op Amp Design Procedure

5. Design for S_1 (S_2) to achieve the desired GB.

$$g_{m1} = GB \cdot C_c \rightarrow S_2 = \frac{g_{m2}^2}{K'_2 I_5}$$

6. Design for S_5 from the minimum input voltage. First calculate $V_{DS5}(\text{sat})$ then find S_5.

$$V_{DS5}(\text{sat}) = V_{in}(\text{min}) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\text{max}) \geq 100 \text{ mV} \rightarrow S_5 = \frac{2I_5}{K'_5[V_{DS5}(\text{sat})]^2}$$

7. Find S_6 by letting the second pole (p_2) be equal to 2.2 times GB and assuming that $V_{SG4} = V_{SG6}$.

$$g_{m6} = 2.2 g_{m2}(C_L/C_c) \quad \text{and} \quad \frac{g_{m6}}{g_{m4}} = \frac{\sqrt{2K_P'S_6I_6}}{\sqrt{2K_P'S_4I_4}} = \sqrt{\frac{S_6I_6}{S_4I_4}} = \frac{S_6}{S_4} \rightarrow S_6 = \frac{g_{m6}}{g_{m4}} S_4$$

8. Calculate I_6 from

$$I_6 = \frac{g_{m6}^2}{2K'_6 S_6}$$

Check to make sure that S_6 satisfies the $V_{out}(\text{max})$ requirement and adjust as necessary.

9. Design S_7 to achieve the desired current ratios between I_5 and I_6.

$$S_7 = (I_6/I_5)S_5$$ (Check the minimum output voltage requirements)

Unbuffered Op Amp Design Procedure

10. Check gain and power dissipation specifications.

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)} \qquad P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

11. If the gain specification is not met, then the currents, I_5 and I_6, can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they are satisfied. If the power dissipation is too high, then one can only reduce the currents I_5 and I_6. Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.
12. Simulate the circuit to check to see that all specifications are met.

Example 1 Design of a two-stage op amp

Using the material and device parameters given in Tables 3.1-1 and 3.1-2, design an amplifier similar to that shown in Fig. 6.3-1 that meets the following specifications. Assume the channel length is to be 1μm and the load capacitor is $C_L = 10\text{pF}$.

$A_v > 3000\text{V/V}$	$V_{DD} = 2.5\text{V}$	$V_{SS} = -2.5\text{V}$
$GB = 5\text{MHz}$	$SR > 10\text{V/μs}$	60° phase margin
V_{out} range $= \pm 2\text{V}$	$ICMR = -1$ to 2V	$P_{diss} \leq 2\text{mW}$

Solution

1.) The first step is to calculate the minimum value of the compensation capacitor C_c,

$$C_c > (2.2/10)(10\text{ pF}) = 2.2\text{ pF}$$

2.) Choose C_c as 3pF. Using the slew-rate specification and C_c calculate I_5.

$$I_5 = (3\text{x}10^{-12})(10\text{x}10^{6}) = 30\ \mu\text{A}$$

3.) Next calculate $(W/L)_3$ using ICMR requirements.

$$(W/L)_3 = \frac{30\text{x}10^{-6}}{(50\text{x}10^{-6})[2.5 - 2 - .85 + 0.55]^2} = 15 \quad \rightarrow \quad \boxed{(W/L)_3 = (W/L)_4 = 15}$$

Example 1

4.) Now we can check the value of the mirror pole, p_3, to make sure that it is in fact greater than $10GB$. Assume the $C_{ox} = 0.4\text{fF}/\mu\text{m}^2$. The mirror pole can be found as

$$p_3 \approx \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K'_p S_3 I_3}}{2(0.667)W_3 L_3 C_{ox}} = 2.81\text{x}10^9(\text{rads/sec})$$

or 448 MHz. Thus, p_3, is not of concern in this design because $p_3 >> 10GB$.

5.) The next step in the design is to calculate g_{m1} to get

$$g_{m1} = (5\text{x}10^6)(2\pi)(3\text{x}10^{-12}) = 94.25\mu\text{S}$$

Therefore, $(W/L)_1$ is

$$(W/L)_1 = (W/L)_2 \approx \frac{g_{m1}^2}{2K'_N I_1} = \frac{(94.25)^2}{2 \cdot 110 \cdot 15} = 2.79 \approx 3.0 \quad \Rightarrow \quad \boxed{(W/L)_1 = (W/L)_2 \approx 3}$$

6.) Next calculate V_{DS5},

$$V_{DS5} = (-1) - (-2.5) - \sqrt{\frac{30\text{x}10^{-6}}{110\text{x}10^{-6}.3}} - .85 = 0.35\text{V}$$

Using V_{DS5} calculate $(W/L)_5$ from the saturation relationship.

$$(W/L)_5 = \frac{2(30\text{x}10\text{-}6)}{(110\text{x}10\text{-}6)(0.35)^2} = 4.49 \approx 4.5 \quad \rightarrow \quad \boxed{(W/L)_5 = 4.5}$$

Example 1

7.) For 60° phase margin, we know that

$$g_{m6} \geq 10 g_{m1} \geq 942.5\mu S$$

Assuming that $g_{m6} = 942.5\mu S$ and knowing that $g_{m4} = 150\mu S$, we calculate $(W/L)_6$ as

$$(W/L)_6 = 15 \frac{942.5\text{x}10\text{-}6}{(150\text{x}10\text{-}6)} = 94.25 \approx 94$$

8.) Calculate I_6 using the small-signal g_m expression:

$$I_6 = \frac{(942.5\text{x}10\text{-}6)2}{(2)(50\text{x}10\text{-}6)(94.25)} = 94.5\mu A \approx 95\mu A$$

If we calculate $(W/L)_6$ based on V_{out}(max), the value is approximately 15. Since 94 exceeds the specification and maintains better phase margin, we will stay with $(W/L)_6 = 94$ and $I_6 = 95\mu A$.

With $I_6 = 95\mu A$ the power dissipation is

$$P_{diss} = 5V \cdot (30\mu A + 95\mu A) = 0.625mW.$$

Example 1

9.) Finally, calculate $(W/L)_7$

$$(W/L)_7 = 4.5\left(\frac{95\text{x}10\text{-}6}{30\text{x}10\text{-}6}\right) = 14.25 \approx 14 \quad \rightarrow \quad \boxed{(W/L)_7 = 14}$$

Let us check the V_{out}(min) specification although the W/L of M7 is so large that this is probably not necessary. The value of V_{out}(min) is

$$V_{out}(\text{min}) = V_{DS7}(\text{sat}) = \sqrt{\frac{2 \cdot 95}{110 \cdot 14}} = 0.351\text{V}$$

which is less than required. At this point, the first-cut design is complete.

10.) Now check to see that the gain specification has been met

$$A_v = \frac{(92.45\text{x}10\text{-}6)(942.5\text{x}10\text{-}6)}{15\text{x}10\text{-}6(.04 + .05)95\text{x}10\text{-}6(.04 + .05)} = 7{,}697\text{V/V}$$

which exceeds the specifications by a factor of two. .An easy way to achieve more gain would be to increase the W and L values by a factor of two which because of the decreased value of λ would multiply the above gain by a factor of 20.

11.) The final step in the hand design is to establish true electrical widths and lengths based upon ΔL and ΔW variations. In this example ΔL will be due to lateral diffusion only. Unless otherwise noted, ΔW will not be taken into account. All dimensions will be rounded to integer values. Assume that $\Delta L = 0.2\mu\text{m}$. Therefore, we have

Example 1

$W_1 = W_2 = 3(1 - 0.4) = 1.8\ \mu m \approx 2\mu m$
$W_3 = W_4 = 15(1 - 0.4) = 9\mu m$
$W_5 = 4.5(1 - 0.4) = 2.7\mu m \approx 3\mu m$
$W_6 = 94(1 - 0.4) = 56.4\mu m \approx 56\mu m$
$W_7 = 14(1 - 0.4) = 8.4 \approx 8\mu m$

The figure below shows the results of the first-cut design. The W/L ratios shown do not account for the lateral diffusion discussed above. The next phase requires simulation.

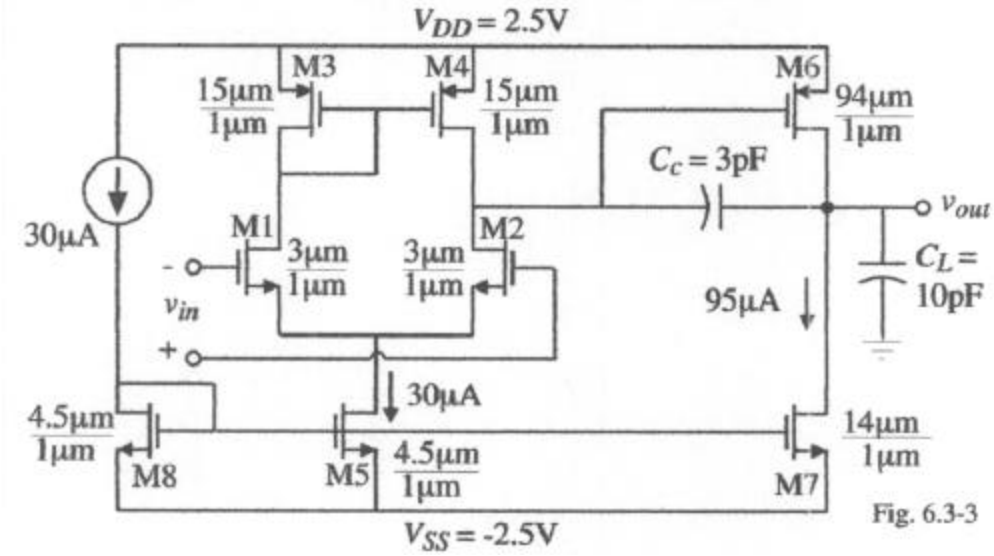
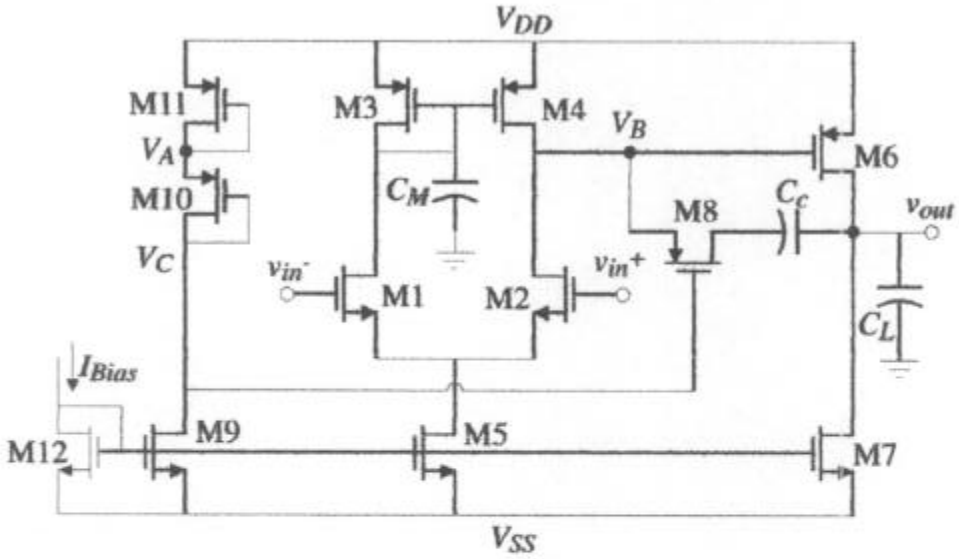


Fig. 6.3-3

Incorporating the nulling resistor into the Miller compensated two-stage op amp

Circuit:



We saw earlier that the roots were:

$$p_1 = -\frac{g_{m2}}{A_v C_c} = -\frac{g_{m1}}{A_v C_c} \qquad p_2 = -\frac{g_{m6}}{C_L}$$

$$p_4 = -\frac{1}{R_z C_I} \qquad z_1 = \frac{-1}{R_z C_c - C_c/g_{m6}}$$

where $A_v = g_{m1} g_{m6} R_I R_{II}$.

(Note that p_4 is the pole resulting from the nulling resistor compensation technique.)

Design of the nulling resistor (M8)

In order to place the zero on top of the second pole (p_2), the following relationship must hold

$$R_z = \frac{1}{g_{m6}}\left(\frac{C_L + C_c}{C_c}\right) = \left(\frac{C_c+C_L}{C_c}\right)\frac{1}{\sqrt{2K'_P S_6 I_6}}$$

The resistor, R_z, is realized by the transistor M8 which is operating in the active region because the dc current through it is zero. Therefore, R_z, can be written as

$$R_z = \frac{\partial v_{DS8}}{\partial i_{D8}}\bigg|_{V_{DS8}=0} = \frac{1}{K'_P S_8 (V_{SG8}-|V_{TP}|)}$$

The bias circuit is designed so that voltage V_A is equal to V_B.

$$\therefore \quad |V_{GS10}| - |V_T| = |V_{GS8}| - |V_T| \Rightarrow \quad V_{SG11} = V_{SG6} \quad \Rightarrow \quad \left(\frac{W_{11}}{L_{11}}\right) = \left(\frac{I_{10}}{I_6}\right)\left(\frac{W_6}{L_6}\right)$$

In the saturation region

$$|V_{GS10}| - |V_T| = \sqrt{\frac{2(I_{10})}{K'_P(W_{10}/L_{10})}} = |V_{GS8}| - |V_T|$$

$$\therefore \quad R_z = \frac{1}{K'_P S_8}\sqrt{\frac{K'_P S_{10}}{2I_{10}}} = \frac{1}{S_8}\sqrt{\frac{S_{10}}{2K'_P I_{10}}}$$

Equating the two expressions for R_z gives $\left(\frac{W_8}{L_8}\right) = \left(\frac{C_c}{C_L + C_c}\right)\sqrt{\frac{S_{10}S_6 I_6}{I_{10}}}$

Example 2

Use results of Ex. 1 and design compensation circuitry so that the RHP zero is moved from the RHP to the LHP and placed on top of the output pole p_2. Use device data given in Ex. 1.

Solution

The task at hand is the design of transistors M8, M9, M10, M11, and bias current I_{10}. The first step in this design is to establish the bias components. In order to set V_A equal to V_B, then V_{SG11} must equal V_{SG6}. Therefore,

$$S_{11} = (I_{11}/I_6)S_6$$

Choose $I_{11} = I_{10} = I_9 = 15\mu A$ which gives $S_{11} = (15\mu A/95\mu A)94 = 14.8 \sim 15$.

The aspect ratio of M10 is essentially a free parameter, and will be set equal to 1. There must be sufficient supply voltage to support the sum of V_{SG11}, V_{SG10}, and V_{DS9}. The ratio of I_{10}/I_5 determines the (W/L) of M9. This ratio is

$$(W/L)_9 = (I_{10}/I_5)(W/L)_5 = (15/30)(4.5) = 2.25 \approx 2$$

Now $(W/L)_8$ is determined to be

$$(W/L)_8 = \left(\frac{3pF}{3pF+10pF}\right)\sqrt{\frac{1\cdot 94\cdot 95\mu A}{15\mu A}} = 5.63 \sim 6$$

Example 2

It is worthwhile to check that the RHP zero has been moved on top of p_2. To do this, first calculate the value of R_z. V_{SG8} must first be determined. It is equal to V_{SG10}, which is

$$V_{SG10} = \sqrt{\frac{2I_{10}}{K'_P S_{10}}} + |V_{TP}| = \sqrt{\frac{2 \cdot 15}{50 \cdot 1}} + 0.7 = 1.474\text{V}$$

Next determine R_z.

$$R_z = \frac{1}{K'_P S_8 (V_{SG10} - |V_{TP}|)} = \frac{10^6}{50 \cdot 5.63(1.474 - .7)} = 4.590\text{k}\Omega$$

The location of z_1 is calculated as

$$z_1 = \frac{-1}{(4.590 \times 10^3)(3\text{x}10^{-12}) - \frac{3\text{x}10^{-12}}{942.5\text{x}10^{-6}}} = -94.46\text{x}10^6 \text{ rads/sec}$$

The output pole, p_2, is

$$p_2 = \frac{942.5\text{x}10^{-6}}{10\text{x}10^{-12}} = -94.25\text{x}10^6 \text{ rads/sec}$$

Thus, we see that for all practical purposes, the output pole is canceled by the zero that has been moved from the RHP to the LHP.

The results of this design are summarized below.

$W_8 = 6\ \mu\text{m}$ $W_9 = 2\ \mu\text{m}$ $W_{10} = 1\ \mu\text{m}$ $W_{11} = 15\ \mu\text{m}$

An alternate form of nulling resistor

To cancel p_2,

$$z_1 = p_2 \rightarrow \quad R_z = \frac{C_c + C_L}{g_{m6A} C_C} = \frac{1}{g_{m6B}}$$

Which gives

$$g_{m6B} = g_{m6A}\left(\frac{C_c}{C_c + C_L}\right)$$

In the previous example,

$g_{m6A} = 942.5\mu S$, $C_c = 3pF$

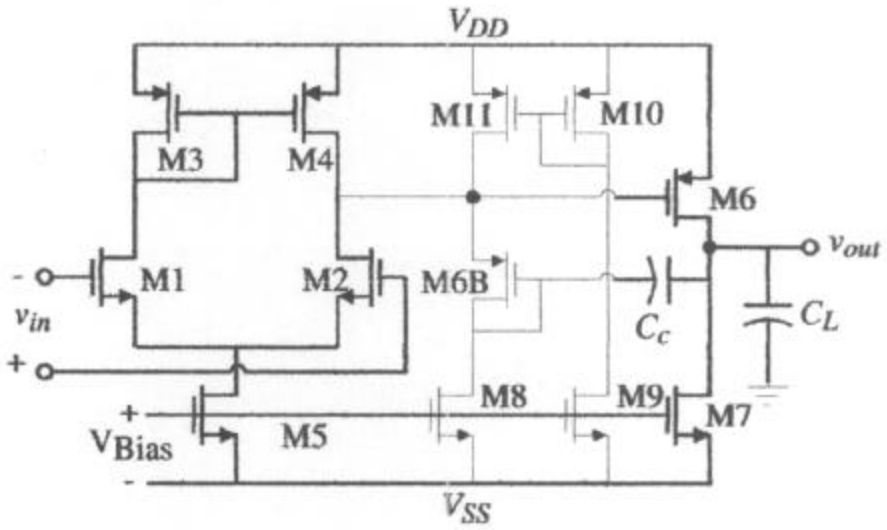
and $C_L = 10pF$.

Choose $I_{6B} = 10\mu A$ to get

$$g_{m6B} = \frac{g_{m6A} C_c}{C_c + C_L} \rightarrow \sqrt{\frac{2K_P W_{6B} I_{6B}}{L_{6B}}} = \left(\frac{C_c}{C_c + C_L}\right)\sqrt{\frac{2K_P W_{6A} I_{D6}}{L_{6A}}}$$

or

$$\frac{W_{6B}}{L_{6B}} = \left(\frac{3}{13}\right)^2 \frac{I_{6A}}{I_{6B}} \frac{W_{6A}}{L_{6A}} = \left(\frac{3}{13}\right)^2 \left(\frac{95}{10}\right)(94) = 47.6 \rightarrow W_{6B} = 48\mu m$$



Programmability of the two-stage op amp

The following relationships depend on the bias current, I_{bias}, in the following manner and allow for programmability after fabrication.

$$A_v(0) = g_{mI}g_{mII}R_IR_{II} \propto \frac{1}{I_{Bias}}$$

$$GB = \frac{g_{mI}}{C_c} \propto \sqrt{I_{Bias}}$$

$$P_{diss} = (V_{DD}+|V_{SS}|)(1+K_1+K_2)I_{Bias} \propto I_{bias}$$

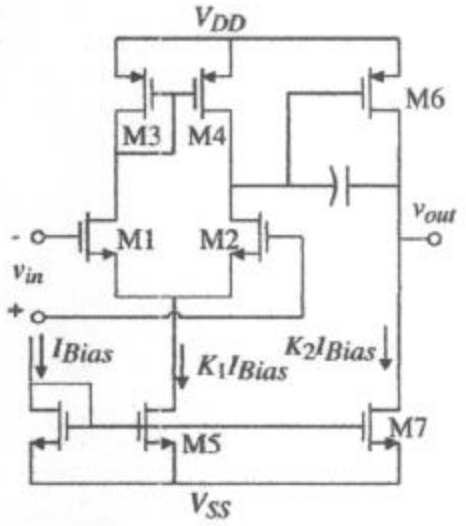
$$SR = \frac{K_1 I_{Bias}}{C_c} \propto I_{Bias}$$

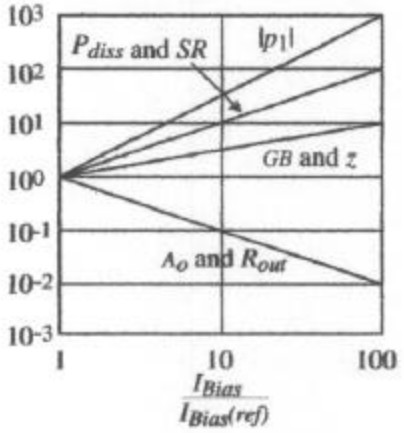
$$R_{out} = \frac{1}{2\lambda K_2 I_{Bias}} \propto \frac{1}{I_{Bias}}$$

$$|p_1| = \frac{1}{g_{mII}R_IR_{II}C_c} \propto \frac{I_{Bias}^2}{\sqrt{I_{Bias}}} \propto I_{Bias}^{1.5}$$

$$|z| = \frac{g_{mII}}{C_c} \propto \sqrt{I_{Bias}}$$

Illustration of the I_{bias} dependence →





Simulation of the electrical design

Area of source or drain = AS = AD = W[L1 + L2 + L3]

where

L1 = Minimum allowable distance between the contact in the S/D and the polysilicon (5μm)

L2 = Width of a minimum size contact (5μm)

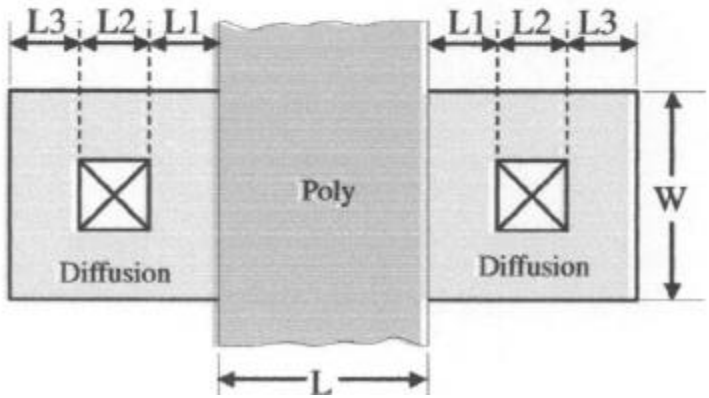
L3 = Minimum allowable distance from contact in S/D to edge of S/D (5μm)

∴ AS = AD = Wx15μm

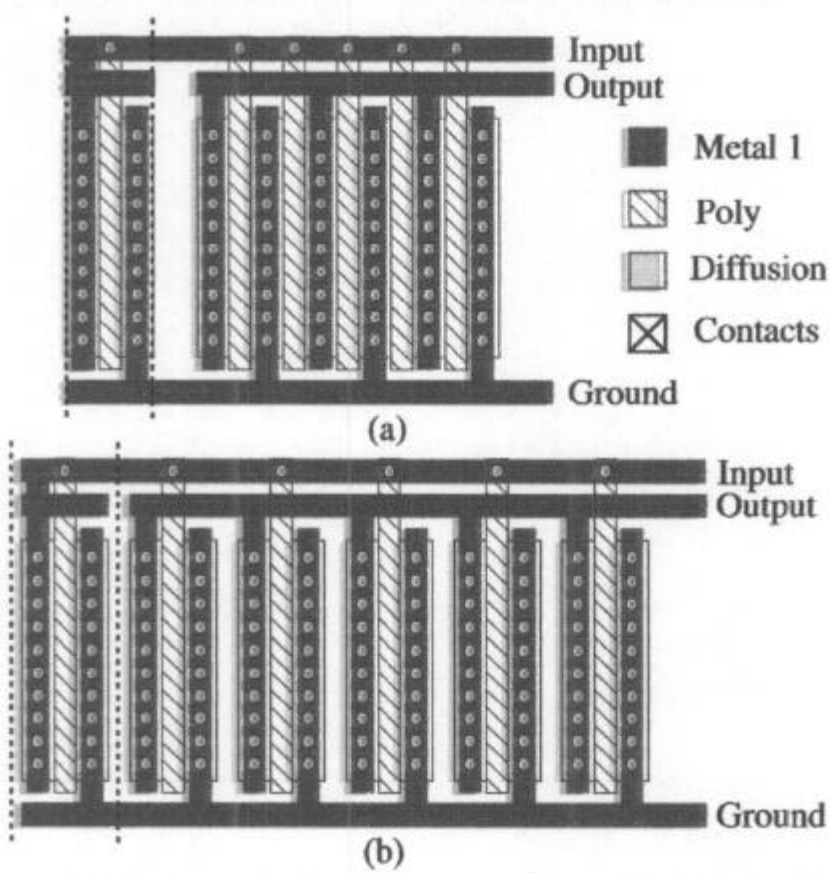
Perimeter of the source or drain = PD = PS = 2W + 2(L1+L2+L3)

∴ PD = PS = 2W + 30μm

Illustration:



5-to-1 Current Mirror with different physical performances



The layout of a 5-to-1 current mirror. (a) Layout which minimizes area at the sacrifice of matching. (b) Layout which optimizes matching.

1-to-1.5 Transistor Matching

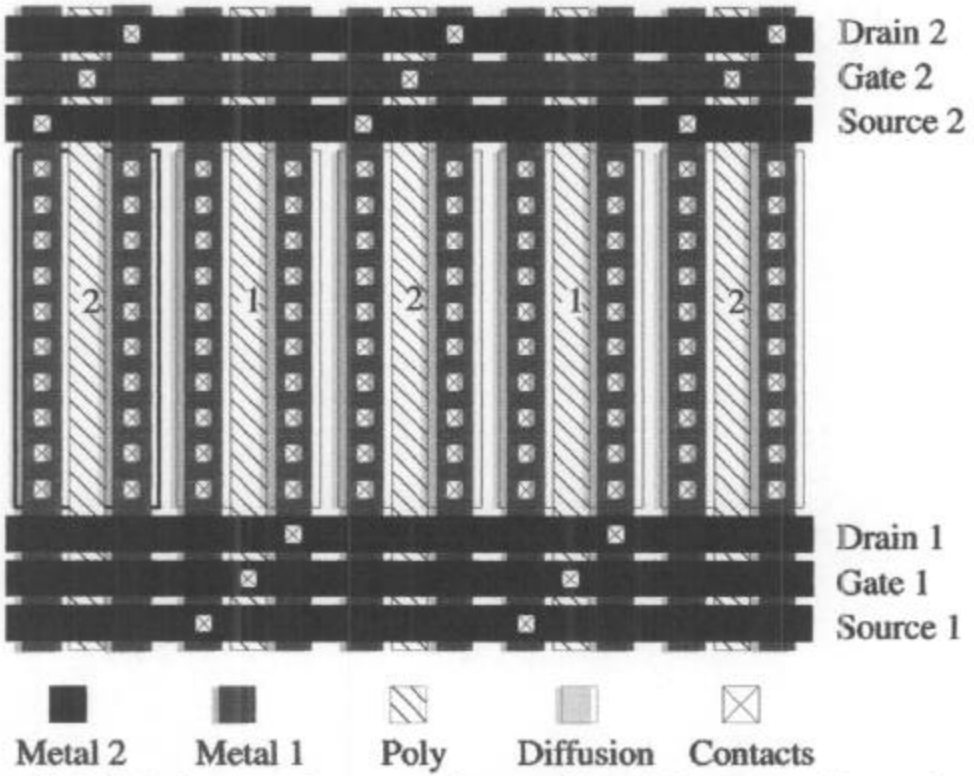


Figure 6.3-7 The layout of two transistors with a 1.5 to 1 matching using centroid geometry to improve matching.

Reduction of Parasitics

Reduction of Parasitics

The major objective of good layout is to minimize the parasitics that influence the design.

Typical parasitics include:

Capacitors to ac ground

Series resistance

Capacitive parasitics is minimized by minimizing area and maximizing the distance between the conductor and ac ground.

Resistance parasitics are minimized by using wide busses and keeping the bus length short.

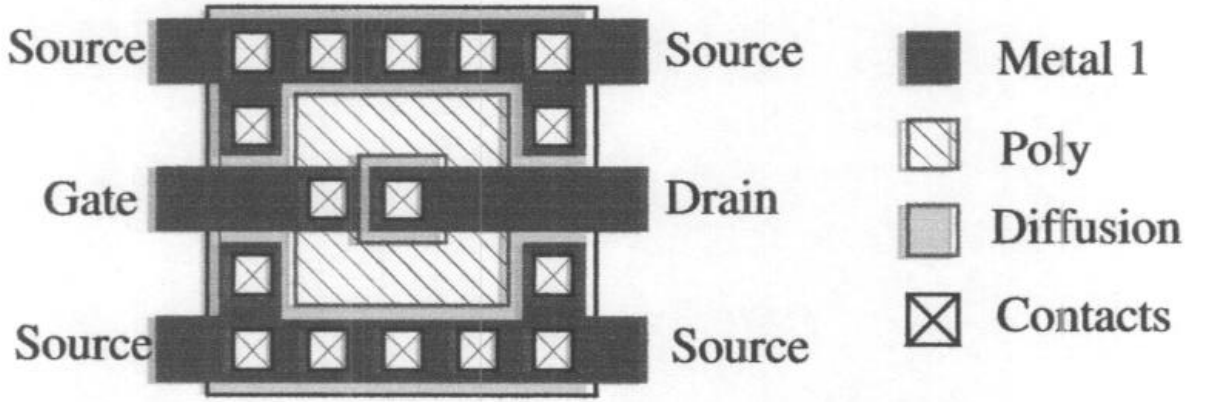
For example:

At 2mΩ/square, a metal run of 1000μm and 2μm wide will have 1Ω of resistance.

At 1 mA this amounts to a 1 mV drop which could easily be greater than the least significant bit of an analog-digital converter. (For example, a 10 bit ADC with V_{REF} = 1V has an LSB of 1mV)

Technique for reducing the overlap capacitance

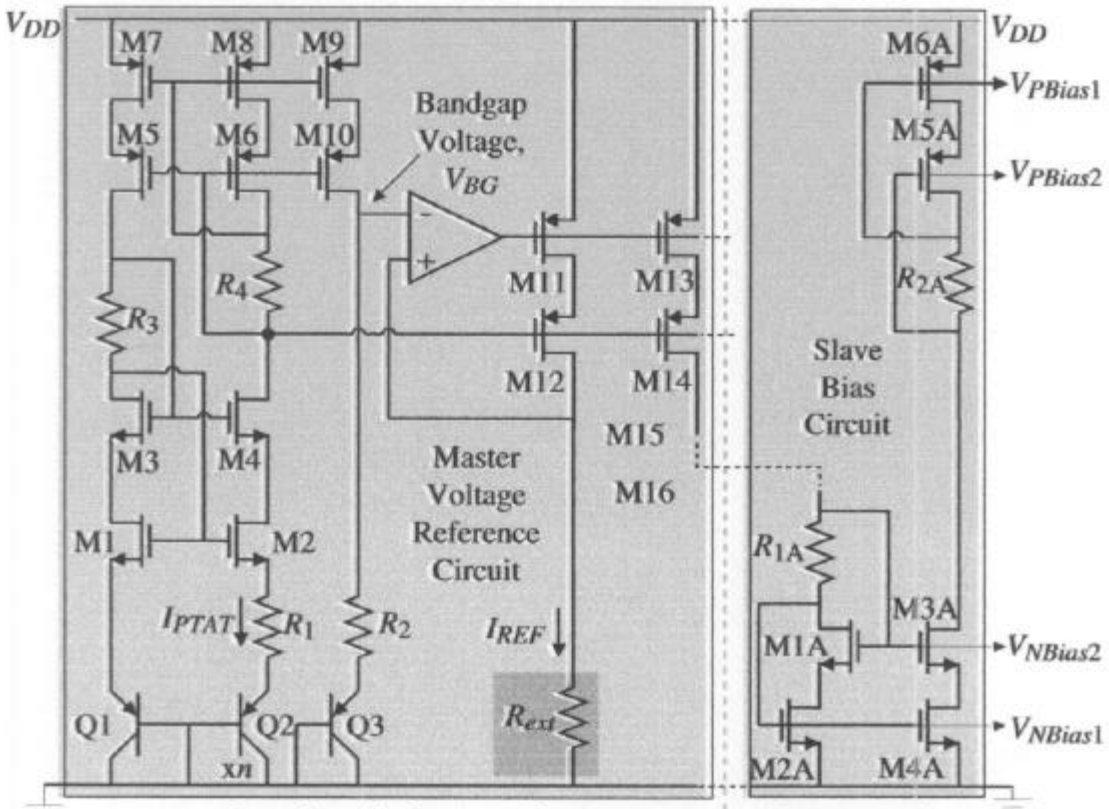
Square Donut Transistor:



Reduction of C_{gd} by a donut shaped transistor.

Note: Can get more W/L in less area with the above geometry.

Chip voltage bias distribution scheme

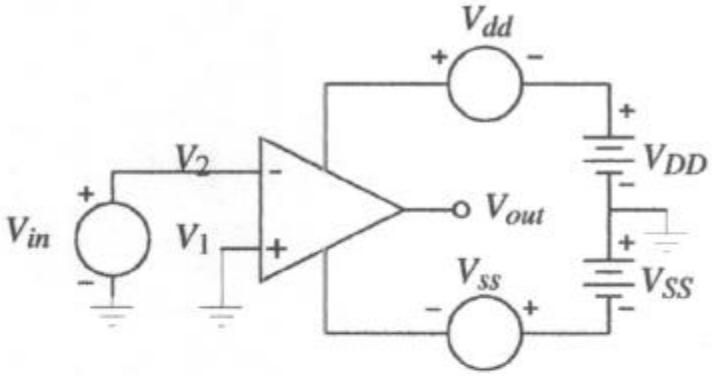


Generation of a reference voltage which is distributed on the chip as a current to slave bias circuits.

PSRR of the two-stage op amp

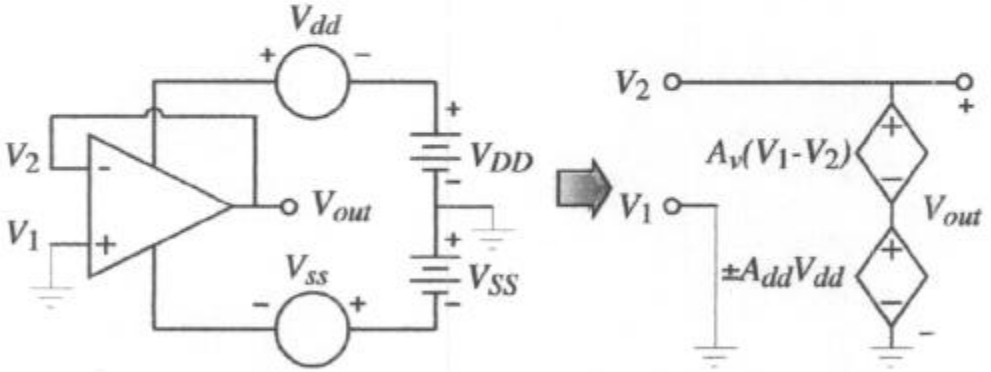
What is *PSRR*?

$$PSRR = \frac{A_v(V_{dd}=0)}{A_{dd}(V_{in}=0)}$$



How do you calculate *PSRR*?

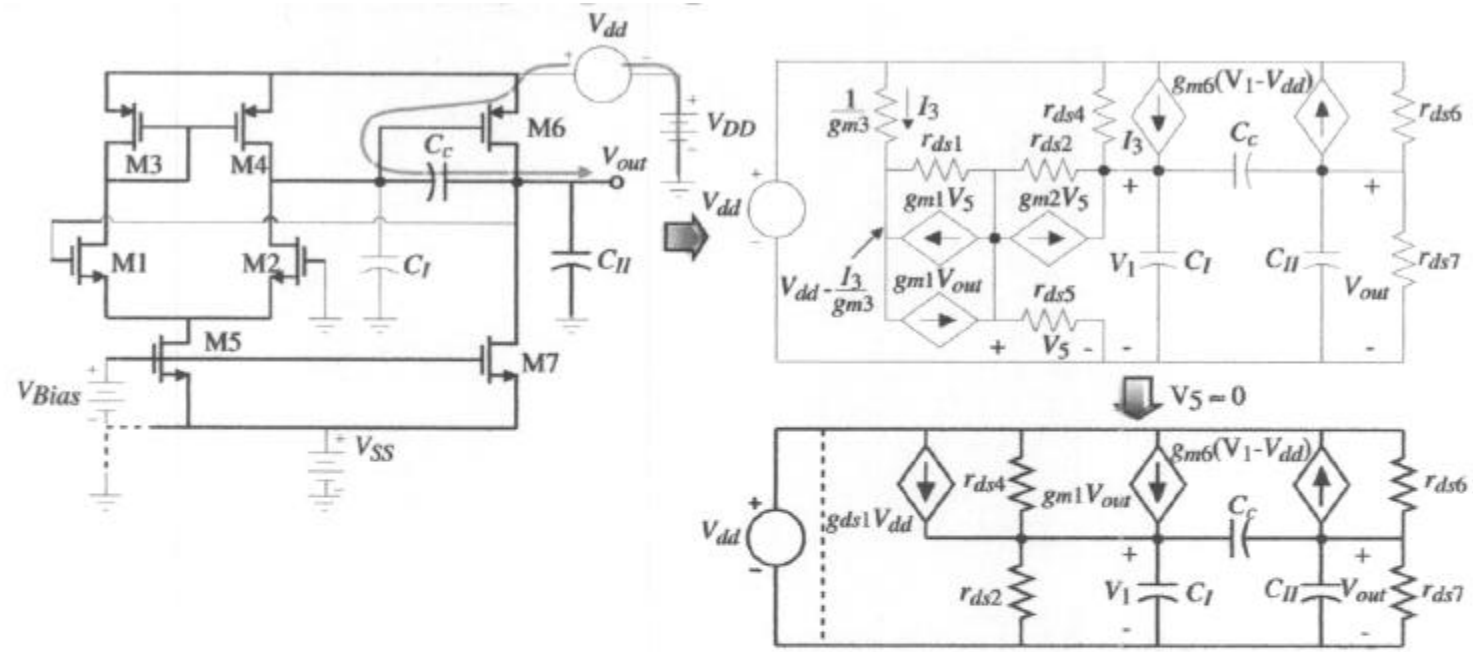
You could calculate A_v and A_{dd} and divide, however



$$V_{out} = A_{dd}V_{dd} + A_v(V_1-V_2) = A_{dd}V_{dd} - A_vV_{out} \rightarrow \quad V_{out}(1+A_v) = A_{dd}V_{dd}$$

$$\therefore \quad \frac{V_{out}}{V_{dd}} = \frac{A_{dd}}{1+A_v} \approx \frac{A_{dd}}{A_v} = \frac{1}{PSRR^+} \qquad \text{(Good for frequencies up to } GB\text{)}$$

Positive PSRR of the two-stage op amp



The nodal equations are:

$$(g_{ds1} + g_{ds4})V_{dd} = (g_{ds2} + g_{ds4} + sC_c + sC_I)V_1 - (g_{m1} + sC_c)V_{out}$$

$$(g_{m6} + g_{ds6})V_{dd} = (g_{m6} - sC_c)V_1 + (g_{ds6} + g_{ds7} + sC_c + sC_{II})V_{out}$$

Using the generic notation the nodal equations are:

$$G_I V_{dd} = (G_I + sC_c + sC_I)V_1 - (g_{mI} + sC_c)V_{out}$$

$$(g_{mII} + g_{ds6})V_{dd} = (g_{mII} - sC_c)V_1 + (G_{II} + sC_c + sC_{II})V_{out}$$

where $G_I = g_{ds1} + g_{ds4} = g_{ds2} + g_{ds4}$, $G_{II} = g_{ds6} + g_{ds7}$, $g_{mI} = g_{m1} = g_{m2}$ and $g_{mII} = g_{m6}$

Positive PSRR of the two-stage op amp

Using Cramers rule to solve for the transfer function, V_{out}/V_{dd}, and inverting the transfer function gives the following result.

$$\frac{V_{dd}}{V_{out}} = \frac{s2[C_cC_I+C_IC_{II}+C_{II}C_c]+ s[G_I(C_c+C_{II}) + G_{II}(C_c+C_I) + C_c(g_{mII} - g_{mI})] + G_IG_{II}+g_{mI}g_{mII}}{s[C_c(g_{mII}+G_I+g_{ds6}) + C_I(g_{mII} + g_{ds6})] + G_Ig_{ds6}}$$

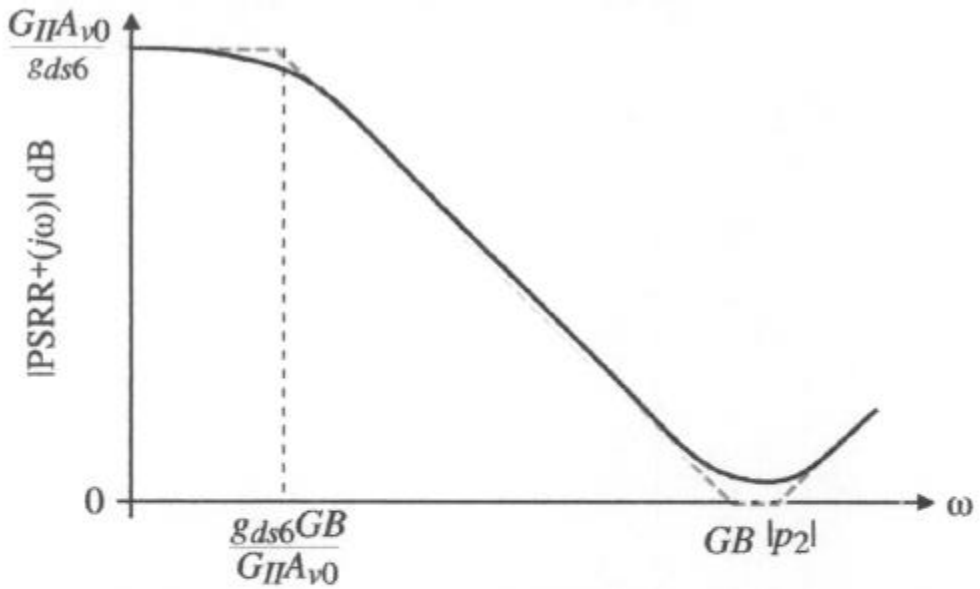
We may solve for the approximate roots of numerator as

$$PSRR+ = \frac{V_{dd}}{V_{out}} \cong \left(\frac{g_{mI}g_{mII}}{G_Ig_{ds6}}\right)\left[\frac{\left(\frac{sC_c}{g_{mI}}+1\right)\left(\frac{s(C_cC_I+C_IC_{II}+C_cC_{II})}{g_{mII}\,C_c}+1\right)}{\left(\frac{sg_{mII}C_c}{G_Ig_{ds6}}+1\right)}\right]$$

where $g_{mII} > g_{mI}$ and that all transconductances are larger than the channel conductances.

$$\therefore \quad PSRR+ = \frac{V_{dd}}{V_{out}} = \left(\frac{g_{mI}g_{mII}}{G_Ig_{ds6}}\right)\left[\frac{\left(\frac{sC_c}{g_{mI}}+1\right)\left(\frac{sC_{II}}{g_{mII}}+1\right)}{\frac{sg_{mII}C_c}{G_Ig_{ds6}}+1}\right] = \left(\frac{G_{II}A_{vo}}{g_{ds6}}\right)\frac{\left(\frac{s}{GB}+1\right)\left(\frac{s}{|p2|}+1\right)}{\left(\frac{sG_{II}A_{vo}}{g_{ds6}GB}+1\right)}$$

Positive PSRR of the two-stage op amp

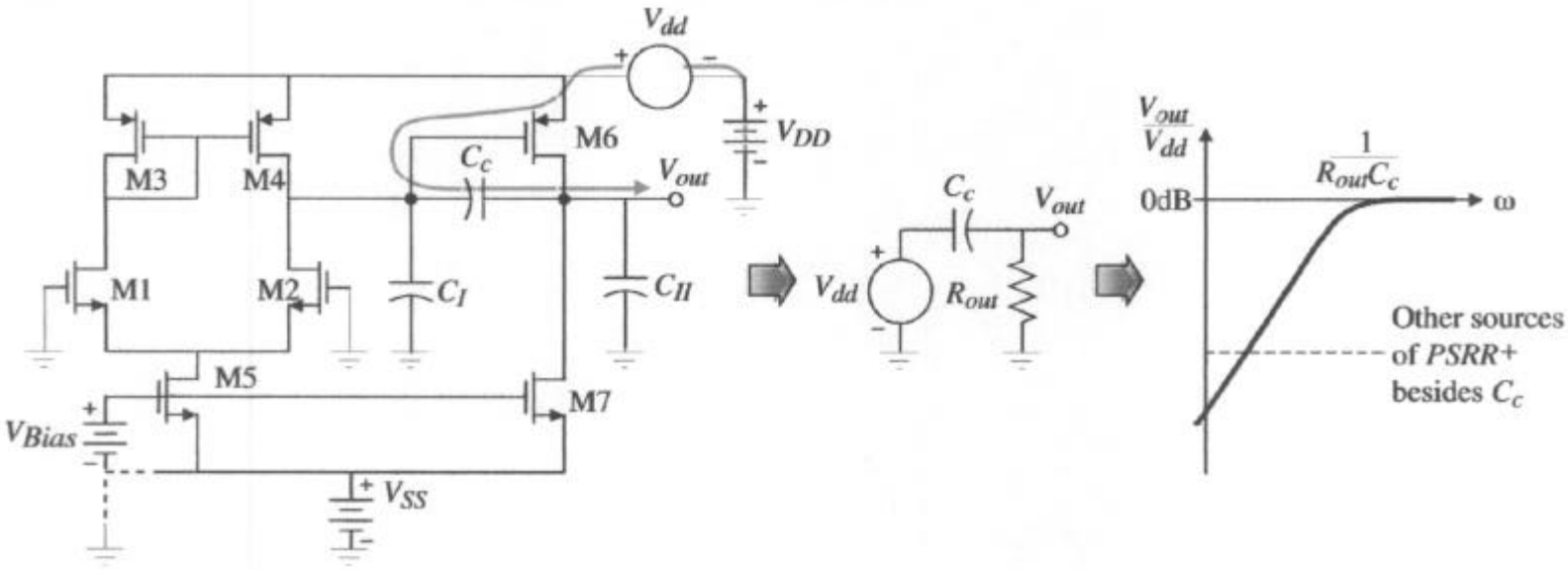


At approximately the dominant pole, the *PSRR* falls off with a -20dB/decade slope and degrades the higher frequency $PSRR^+$ of the two-stage op amp.

Using the values of Example 1 we get:

$PSRR^+(0) = 68.8\text{dB}$, $z_1 = -5\text{MHz}$, $z_2 = -15\text{MHz}$ and $p_1 = -906\text{Hz}$

Concept of the PSRR+ for the two-stage op amp



1.) The M7 current sink causes V_{SG6} to act like a battery.
2.) Therefore, V_{dd} couples from the source to gate of M6.
3.) The path to the output is through any capacitance from gate to drain of M6.

Conclusion:

The Miller capacitor C_c couples the positive power supply ripple directly to the output.

Must reduce or eliminate C_c.

Negative PSRR of the two-stage op amp with V_{bias}, grounded

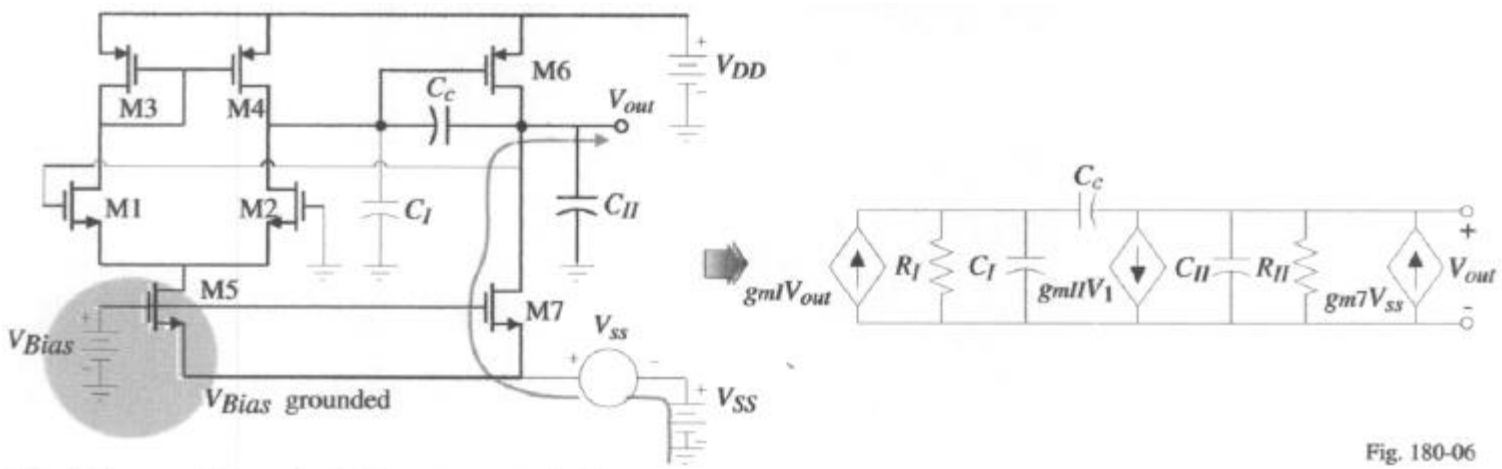


Fig. 180-06

Nodal equations for V_{Bias} grounded:

$$0 = (G_I + sC_c + sC_I)V_1 - (g_{mI} + sC_c)V_o$$

$$g_{m7}V_{ss} = (g_{MII} - sC_c)V_1 + (G_{II} + sC_c + sC_{II})V_o$$

Solving for V_{out}/V_{ss} and inverting gives

$$\frac{V_{ss}}{V_{out}} = \frac{s^2[C_cC_I + C_IC_{II} + C_{II}C_c] + s[G_I(C_c + C_{II}) + G_{II}(C_c + C_I) + C_c(g_{mII} - g_{mI})] + G_IG_{II} + g_{mI}g_{mII}}{[s(C_c + C_I) + G_I]g_{m7}}$$

Negative PSRR of the two-stage op amp with V_{bias} grounded

Again using techniques described previously, we may solve for the approximate roots as

$$PSRR^- = \frac{V_{ss}}{V_{out}} \cong \left(\frac{g_{mI}g_{mII}}{G_I g_{m7}}\right) \left[\frac{\left(\frac{sC_c}{g_{mI}} + 1\right)\left(\frac{s(C_cC_I+C_IC_{II}+C_cC_{II})}{g_{mII}\,C_c} + 1\right)}{\left(\frac{s(C_c+C_I)}{G_I} + 1\right)}\right]$$

This equation can be rewritten approximately as

$$PSRR^- = \frac{V_{ss}}{V_{out}} \cong \left(\frac{g_{mI}g_{mII}}{G_I g_{m7}}\right) \left[\frac{\left(\frac{sC_c}{g_{mI}} + 1\right)\left(\frac{sC_{II}}{g_{mII}} + 1\right)}{\left(\frac{sC_c}{G_I} + 1\right)}\right] = \left(\frac{G_{II}A_{v0}}{g_{m7}}\right) \left[\frac{\left(\frac{s}{GB} + 1\right)\left(\frac{s}{|p_2|} + 1\right)}{\left(\frac{s}{GB}\frac{g_{mI}}{G_I} + 1\right)}\right]$$

Comments:

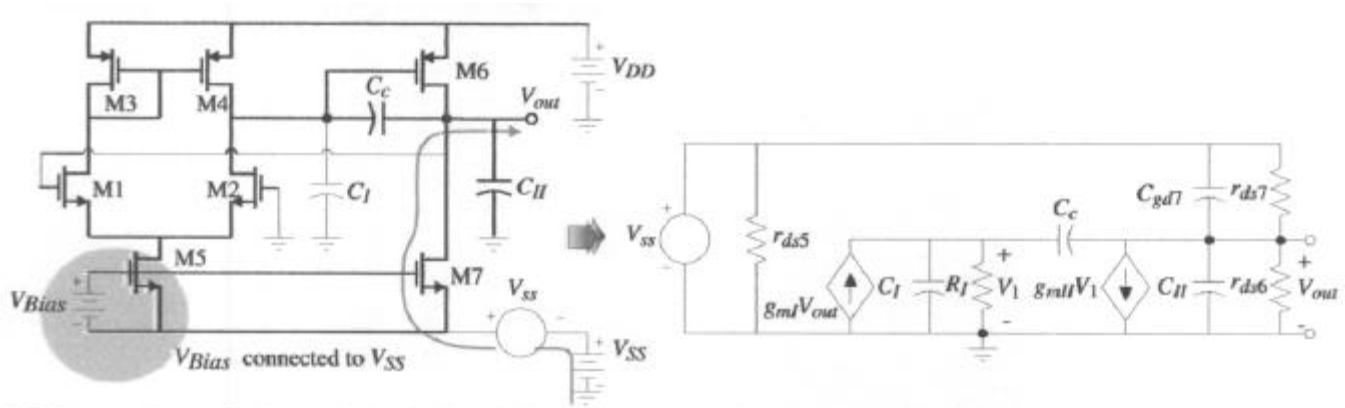
$PSRR^-$ zeros = $PSRR^+$ zeros

DC gain ≈ Second-stage gain,

$PSRR^-$ pole ≈ (Second-stage gain) x ($PSRR^+$ pole)

Assuming the values of Ex. 6.3-1 gives a gain of 23.7 dB and a pole -147 kHz. The dc value of $PSRR^-$ is very poor for this case, however, this case can be avoided by correctly implementing V_{Bias} which we consider next.

Negative PSRR of the two-stage op amp with V_{bias} connected to V_{SS}



If the value of V_{Bias} is independent of V_{ss}, then the model shown results. The nodal equations for this model are

$$0 = (G_I + sC_c + sC_I)V_1 - (g_{mI} + sC_c)V_{out}$$

and

$$(g_{ds7} + sC_{gd7})V_{ss} = (g_{mII} - sC_c)V_1 + (G_{II} + sC_c + sC_{II} + sC_{gd7})V_{out}$$

Again, solving for V_{out}/V_{ss} and inverting gives

$$\frac{V_{ss}}{V_{out}} = \frac{s^2[C_cC_I+C_IC_{II}+C_{II}C_c+C_IC_{gd7}+C_cC_{gd7}]+s[G_I(C_c+C_{II}+C_{gd7})+G_{II}(C_c+C_I)+C_c(g_{mII}-g_{mI})]+G_IG_{II}+g_{mI}g_{mII}}{(sC_{gd7}+g_{ds7})(s(C_I+C_c)+G_I)}$$

Negative PSRR of the two-stage op amp with V_{bias} connected to V_{SS}

Assuming that $g_{mII} > g_{mI}$ and solving for the approximate roots of both the numerator and denominator gives

$$PSRR^- = \frac{V_{ss}}{V_{out}} \cong \left(\frac{g_{mI}g_{mII}}{G_I g_{ds7}}\right)\left[\frac{\left(\frac{sC_c}{g_{mI}}+1\right)\left(\frac{s(C_cC_I+C_IC_{II}+C_cC_{II})}{g_{mII}C_c}+1\right)}{\left(\frac{sC_{gd7}}{g_{ds7}}+1\right)\left(\frac{s(C_I+C_c)}{G_I}+1\right)}\right]$$

This equation can be rewritten as

$$PSRR^- = \frac{V_{ss}}{V_{out}} \sim \left(\frac{G_{II}A_{v0}}{g_{ds7}}\right)\left[\frac{\left(\frac{s}{GB}+1\right)\left(\frac{s}{|p_2|}+1\right)}{\left(\frac{sC_{gd7}}{g_{ds7}}+1\right)\left(\frac{sC_c}{G_I}+1\right)}\right]$$

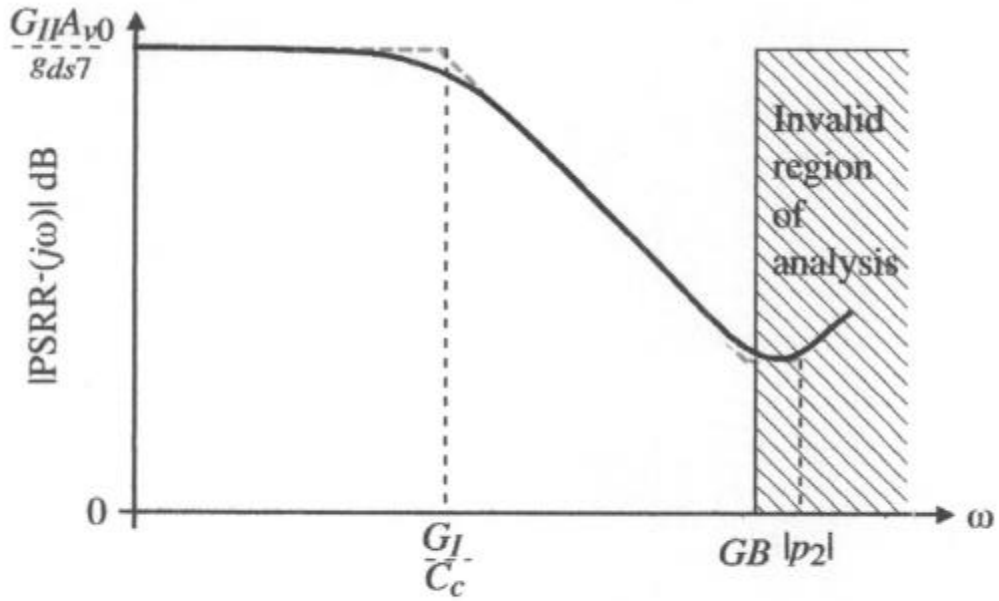
Comments:

- DC gain has been increased by the ratio of G_{II} to g_{ds7}
- Two poles instead of one, however the pole at $-g_{ds7}/C_{gd7}$ is large and can be ignored.

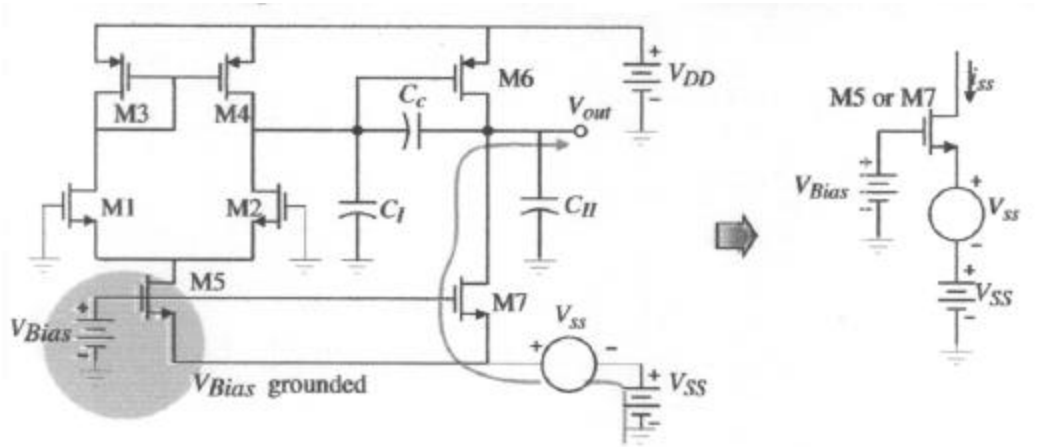
Using the values of Ex. 1 and assume that $C_{ds7} = 10$fF, gives,

$PSRR^-(0) = 76.7$dB and Poles at -71.2kHz and -149MHz

Frequency response of the negative PSRR of the two-stage op amp with V_{Bias} connected to V_{SS}



Approximate model for negative PSRR with V_{Bias} connected to ground

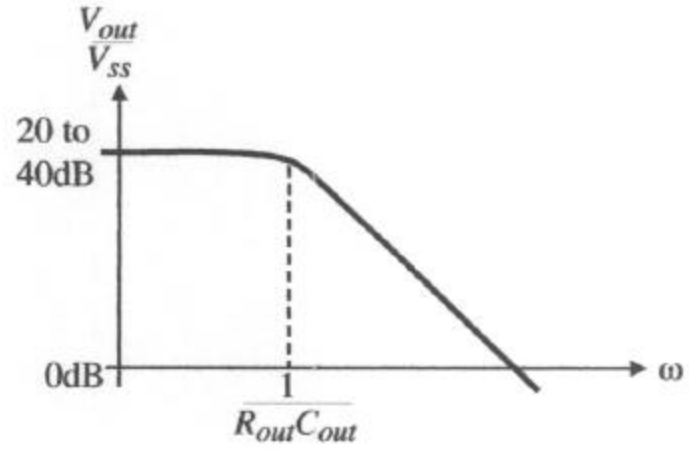


Path through the input stage is not important as long as the *CMRR* is high.

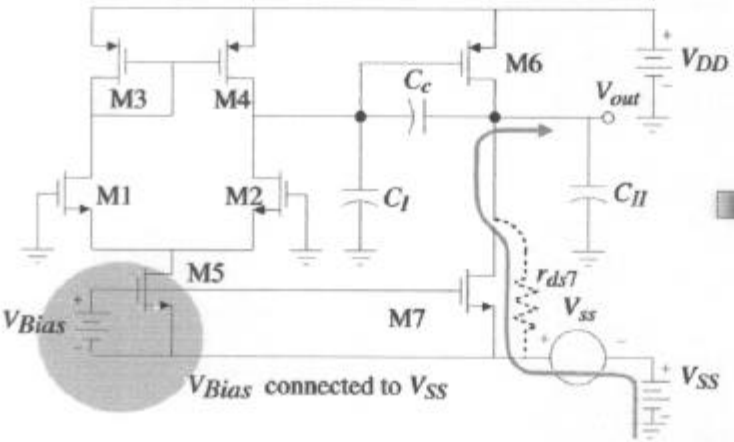
Path through the output stage:

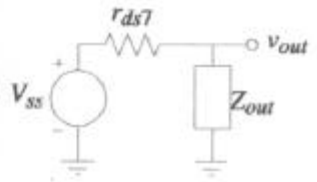
$$v_{out} \approx i_{ss} Z_{out} = g_{m7} Z_{out} V_{ss}$$

$$\therefore \quad \frac{V_{out}}{V_{ss}} = g_{m7} Z_{out} = g_{m7} R_{out} \left(\frac{1}{sR_{out}C_{out}+1} \right)$$



Approximate model for negative PSRR with V_{Bias} connected to V_{SS}





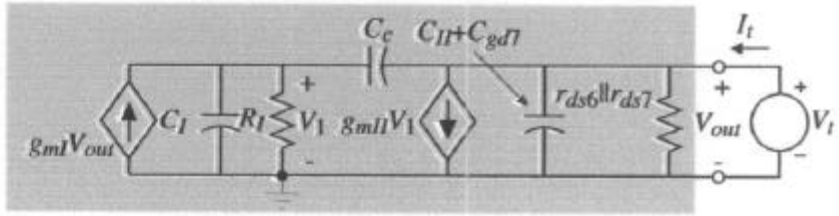
Path through C_{gd7} is negligible

What is Z_{out}?

$$Z_{out} = \frac{V_t}{I_t} \Rightarrow$$

$$I_t = g_{mII}V_1 = g_{mII}\left(\frac{g_{mI}V_t}{G_I + sC_I + sC_c}\right)$$

$$\text{Thus, } Z_{out} = \frac{G_I + s(C_I + C_c)}{g_{mI}g_{MII}}$$



$$\therefore \quad \frac{V_{ss}}{V_{out}} = \frac{1 + \frac{r_{ds7}}{Z_{out}}}{1} = \frac{s(C_c + C_I) + G_I + g_{mI}g_{mII}r_{ds7}}{s(C_c + C_I) + G_I} \quad \Rightarrow \quad \text{Pole at } \frac{-G_I}{C_c + C_I}$$

The two-stage op amp will never have good *PSRR* because of the Miller compensation.