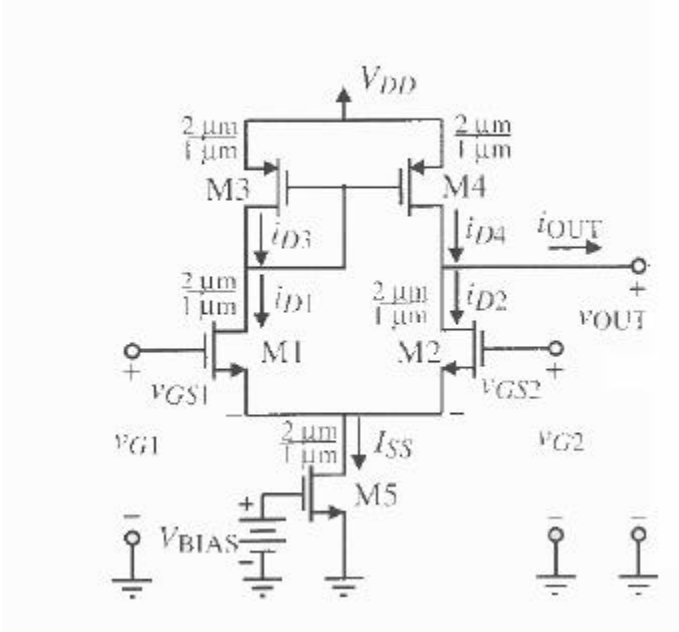
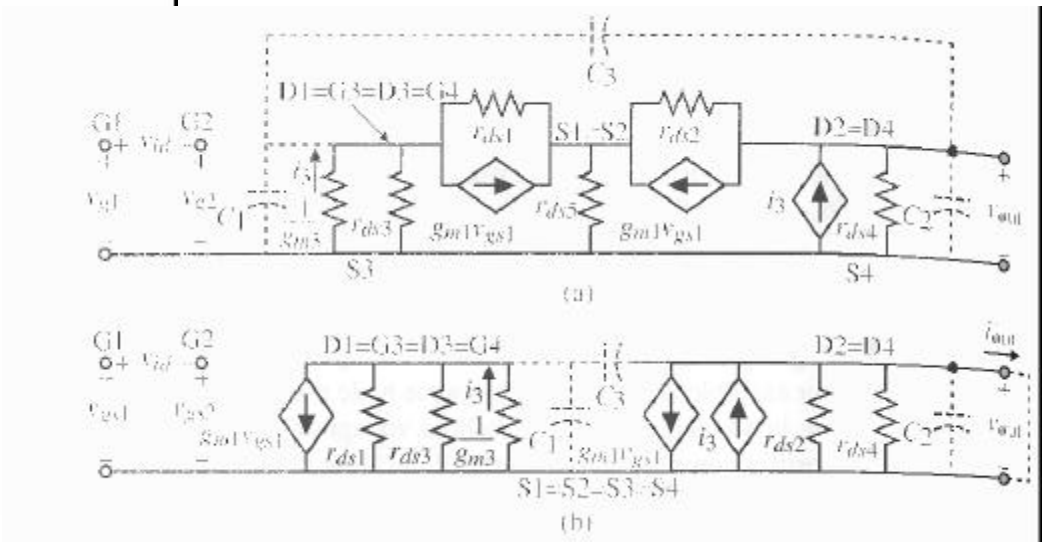
Differential amplifier (2)

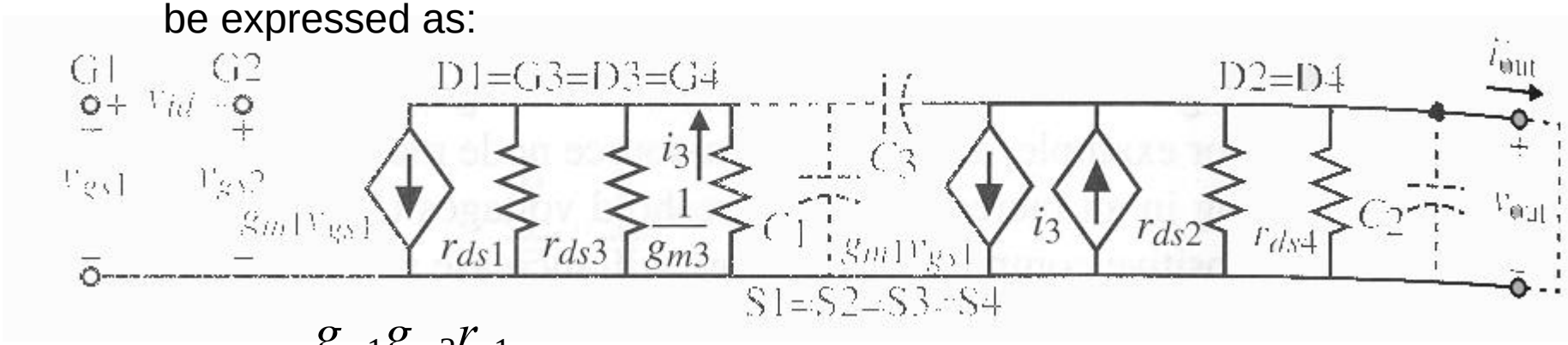
Small-signal model of CMOS differential amplifier





Differential-transconductance gain

- Both side of the amplifier are assumed to be perfectly matched (It can be shown that the current mirror causes this assumption to be invalid because the drain loads of M1 and M2 are not matched!)
- If this condition is satisfied then the point where the two sources of M1 and M2 are connected can be considered to be at ac ground.
- If we assume that the differential stage is unloaded, then with the output shorted to ac ground, the differential-transconductance gain can be expressed as:



$$i'_{out} = \frac{g_{m1}g_{m3}r_{p1}}{1+g_{m3}}v_{gs1} - g_{m2}v_{gs2} \longrightarrow i'_{out} \cong g_{m1}v_{gs1} - g_{m2}v_{gs2} = g_{md}v_{id}$$

- Where $g_{m1}=g_{m2}=g_{md}$, $r_{p1}=r_{ds1}//r_{ds2}$ and i'_{out} is the output current in the short circuit

Differential voltage gain

- The unloaded differential stage gain can be determined by finding the small-signal output resistance of the differential amplifier.

$$r_{out} = \frac{1}{g_{ds2} + g_{ds4}} \qquad A_V = \frac{v_{out}}{v_{id}} = \frac{g_{md}}{g_{ds2} + g_{ds4}}$$

$$A_V = \frac{v_{out}}{v_{id}} = \frac{(K'_1 I_{SS} W_1 / L_1)^{1/2}}{(l_2 + l_4)(I_{SS}/2)} = \frac{2}{l_2 + l_4}\left(\frac{K'_1 W_1}{I_{SS} L_1}\right)^{1/2}$$

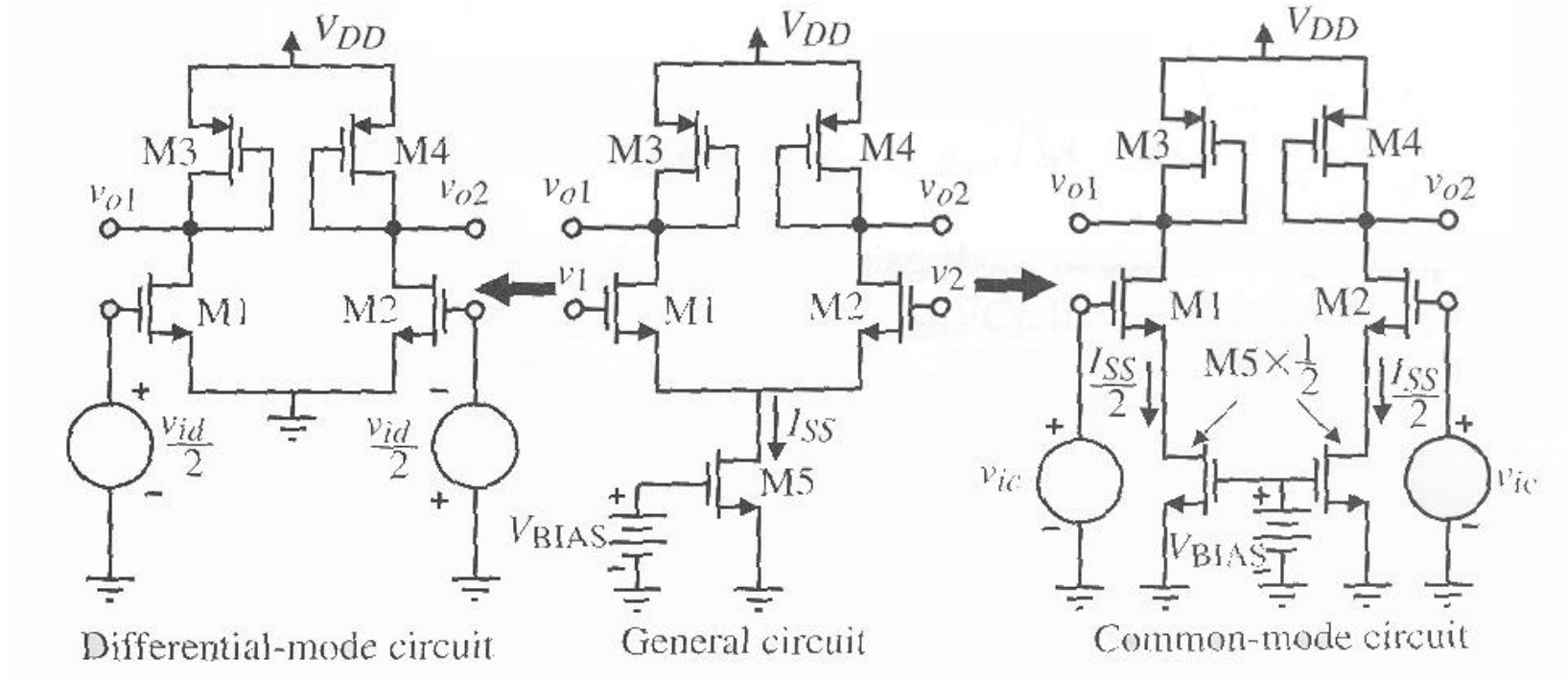
- We note the dependence of the small-signal gain on the inverse of $I_{SS}^{1/2}$ similar to that of the inverter. The relationship is in fact valid until I_{SS} approaches subthreshold values.

Common-mode and mismatches

- The common-mode gain of the CMOS differential amplifiers is ideally zero.This is because the current mirror load rejects any common-mode signal.
- The fact that a common-mode response might exist is due to the mismatches in the differential amplifier.
- These mismatches consist of a nonunity current gain in the current mirror and geometrical mismatches between M1 and M2.

Simplification of the differential amplifier for small-signal analysis

- To demonstrate how to analyze the small-signal common-mode voltage gain of the differential amplifier, consider the differential amplifier of the following figures



Differential-mode voltage gain (2)

- The small-signal differential mode analysis is identical with the small-signal analysis except the input is reduced by a factor of 2.
- The small-signal differential-mode voltage gain is given as:

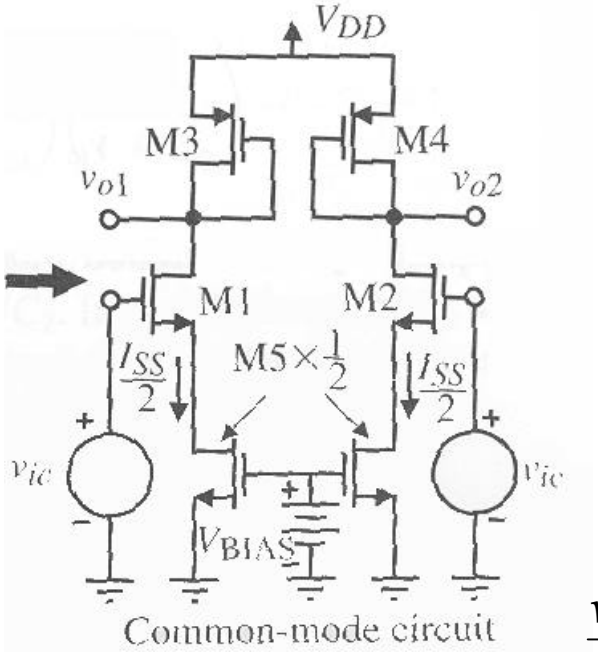
$$\frac{v_{o1}}{v_{id}} = -\frac{g_{m1}}{2g_{m3}}$$

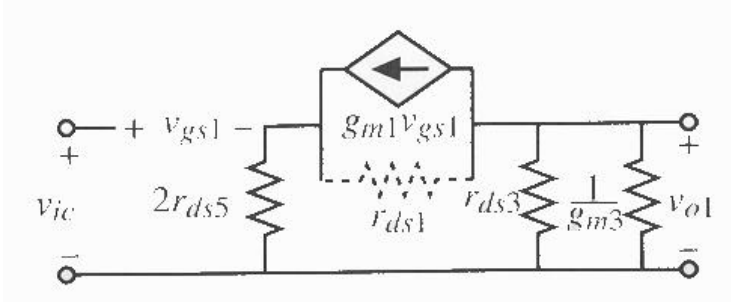
$$\frac{v_{o2}}{v_{id}} = +\frac{g_{m2}}{2g_{m4}}$$

- We see that the small-signal, differential-mode voltage gain is half of the small-signal voltage gain of the active load inverter. The reason is that the input signal is divided half to M1 and half to M2

The small-signal common mode voltage gain

- Note that $2r_{ds5}$ represents the small-signal output resistance of M5x0.5 transistor. (If the dc current is decreased by one-half, the small-signal output resistance will be increased by 2)





$$v_{gs1} = v_{ic} - 2g_{m1}r_{ds5}v_{gs1}$$

$$v_{gs1} = \frac{v_{ic}}{1+2g_{m1}r_{ds5}v_{gs1}}$$

$$\frac{v_{o1}}{v_{ic}} = -\frac{g_{m1}\left[r_{ds3} \parallel (1/g_{m3})\right]}{1+2g_{m1}r_{ds5}} \approx \frac{(g_{m1}/g_{m3})}{1+2g_{m1}r_{ds5}} \approx \frac{g_{ds5}}{2g_{m3}}$$

If the r_{ds5} is large, the common-mode gain is reduced.

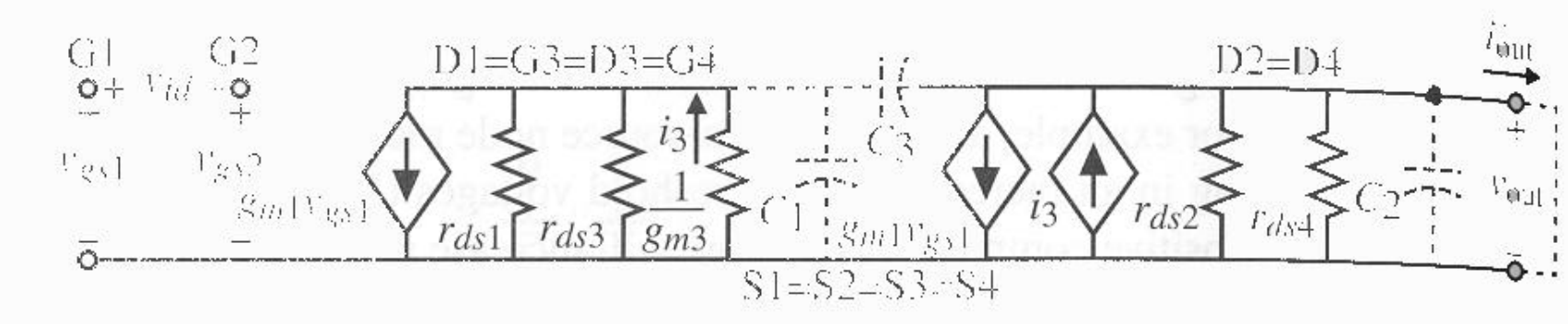
CMRR

$$CMRR = \frac{g_{m1}/2g_{m3}}{g_{ds5}/2g_{m3}} = g_{m1}r_{ds5}$$

- This result shows how to increase the CMRR. Obviously, the easiest way is to use a cascode current sink in place of M5.
- This would increase the CMRR by a factor of $g_m r_{ds}$ at a cost of decreased ICMR

Frequency response

- The frequency response of the CMOS differential amplifier is due to the varous parasitic capacitors at each node of the circuit.
- C1=Cgd1,Cbd1,Cgs3,Cgs4; C2=Cbd2,Cbd4, Cgd2 and any CL
- C3=Cgd4. To simplify the analysis C3 is assumed to be zero.



Frequency response (2)

$$V_{out}(s) \cong \frac{g_{m1}}{g_{ds2}+g_{ds4}}\left[\left(\frac{g_{m3}}{g_{m3}+sC_1}\right)V_{gs1}(s) - V_{gs2}(s)\right]\left(\frac{w_2}{s+w_2}\right)$$

$$w_2 = \frac{g_{ds2}+g_{ds4}}{C_2}$$

- If $\frac{g_{m3}}{C_1} >> \frac{g_{ds2}+g_{ds4}}{C_2} \Rightarrow \frac{V_{out}(s)}{V_{id}(s)} \cong \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{w_2}{s+w_2}\right)$

- The first-order analysis of the frequency response of a differential amplifier consists of a single pole. We have ignored the zeros.

Intuitive Method of Small-Signal Analysis

- The technique identifies the transistor or transistors that convert input voltage to current (*transconductance transistor*).
- The currents that the transconductance transistors create are traced to where they flow into a resistance to ac ground.
- Multiplying this resistance by the current gives the voltage at this node.

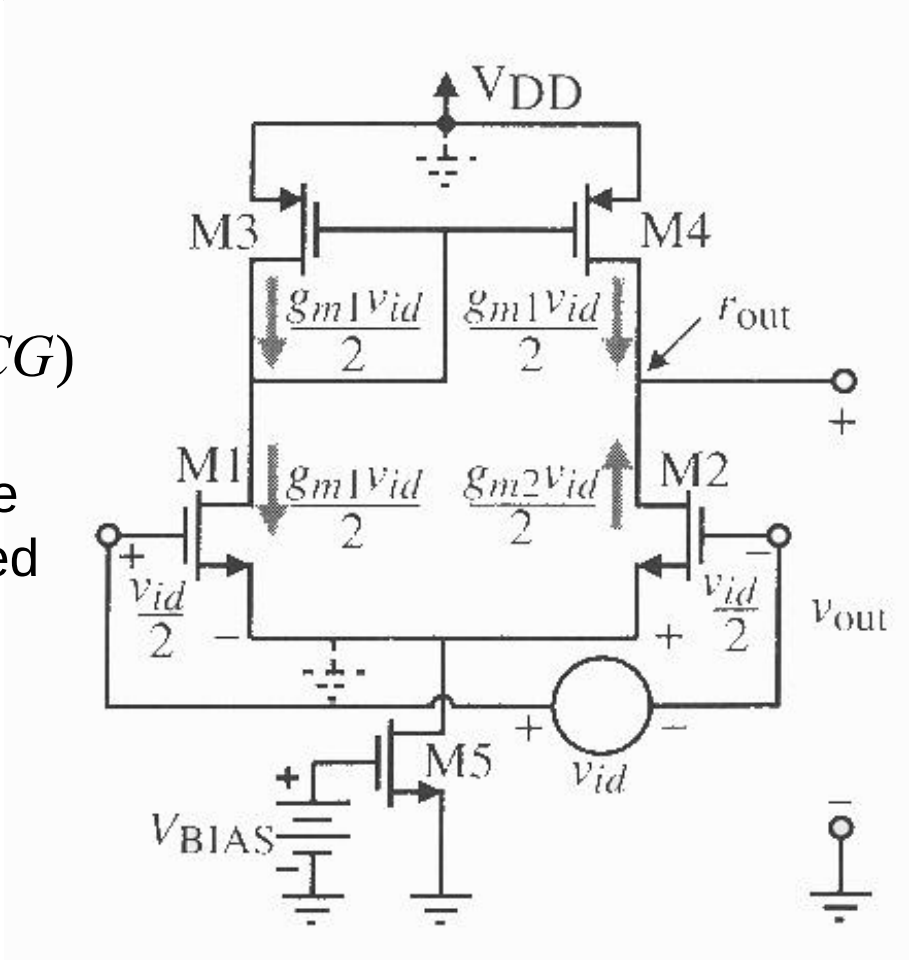
Intuitive analysis of the CMOS differential amplifier

$$A_V = \frac{v_{out}}{v_{id}} = \frac{g_{md}}{g_{ds2} + g_{ds4}}$$

$$r_{out}(cascode) = r_{ds}(CS) \times g_m r_{ds}(CG)$$

If the source of the transconductance transistor has a resistance connected to ground:

$$g_m(eff) = \frac{g_m}{1 + g_m R}$$



Slew rate

- The *slew rate* (SR) performance depends on the value of I_{SS} and the capacitance from the output node to ac ground.

- SR is defined as the maximum output-voltage rate, either positive or negative.

- Since the slew rate is determined by the amount of current that can be sourced or sink into the output/compensating capacitor, it is given by:

$$\text{Slew rate} = I_{SS}/C$$

where C is the total capacitance connected to the output node.

Noise performance

- The noise performance can be due to both thermal and 1/f noise.
- Depending on the frequency range of interest, one source can be neglected in favor of the other.
- At low frequency, 1/f noise is important whereas at high frequencies/low currents thermal noise is important.

Noise model of a p-channel differential amplifier

- N the figure it is shown the p-channel differential amplifier with equivalent-noise voltage sources ignoring the noise of I_{DD}, given by:

$$i_n^2 = \left[\frac{8kTg_m(1+\eta)}{3} + \frac{(KF)I_D}{fC_{ox}L^2}\right]\Delta f$$

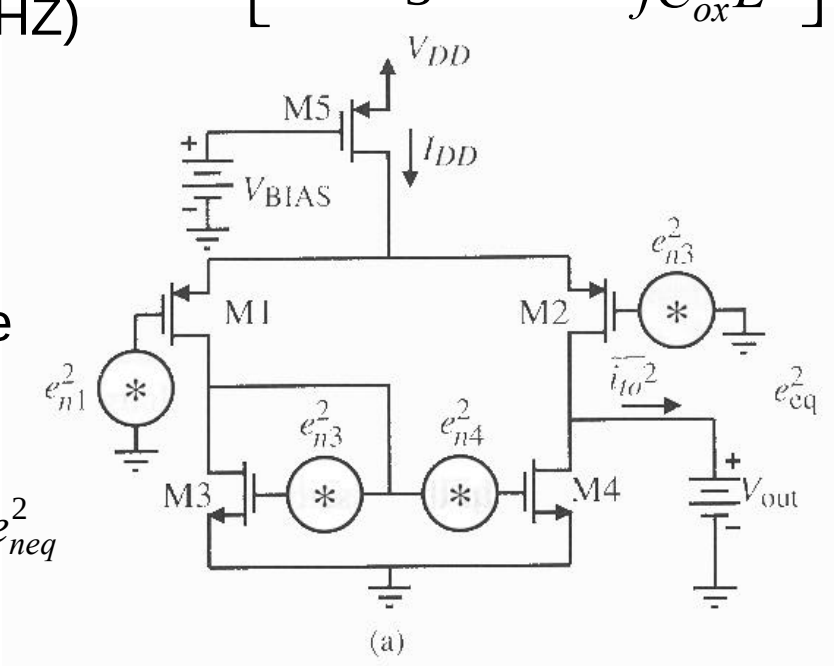
Δf= a small bandwidth (typically 1HZ) at a frequency f

η=gmbs/gm

k= Boltzmann's costant

g_m=small-signal transconductance

KF= flicker noise coefficient



$$i_{to}^2 = g_{m1}^2 e_{n1}^2 + g_{m2}^2 e_{n2}^2 + g_{m3}^2 e_{n3}^2 + g_{m4}^2 e_{n4}^2 = g_{m1}^2 e_{neq}^2$$

Equivalent-noise model

- Assuming gm1=gm2 and gm3=gm4:

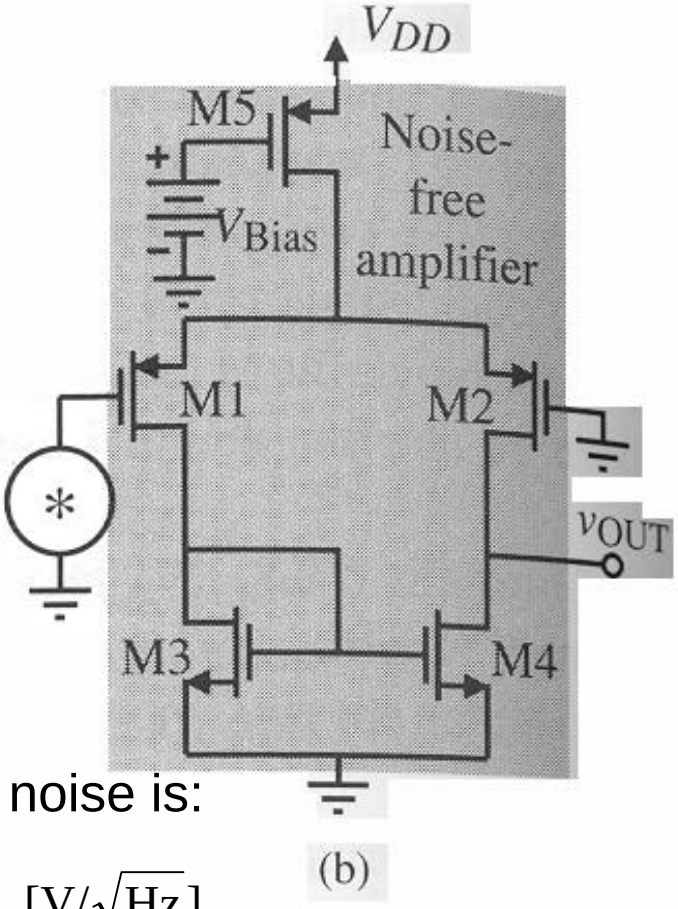
$$e_{eq}^2 = e_{n1}^2 + e_{n2}^2 + \left(\frac{g_{m3}}{g_{m4}}\right)^2 [e_{n3}^2 + e_{n4}^2]$$

- Assuming that en1=en2 and en3=en4:

$$e_{eq}(1/f) = \sqrt{\frac{2B_p}{fW_1L_1}}\sqrt{1+\left(\frac{K'_N B_N}{K'_P B_P}\right)\left(\frac{L_1}{L_2}\right)^2} \qquad [\mathrm{V}/\sqrt{\mathrm{Hz}}]$$

being $(B/fWL)^{1/2}$ the flicker noise of each transistor and B a constant and the thermal noise is:

$$e_{eq(th)} = \sqrt{\frac{16kT}{3[2K'_p I_1(W_1/L_1)]^{1/2}}}\sqrt{1+\sqrt{\left(\frac{K'_N (W_3/L_3)}{K'_P (W_1/L_1)}\right)}} \qquad [\mathrm{V}/\sqrt{\mathrm{Hz}}]$$

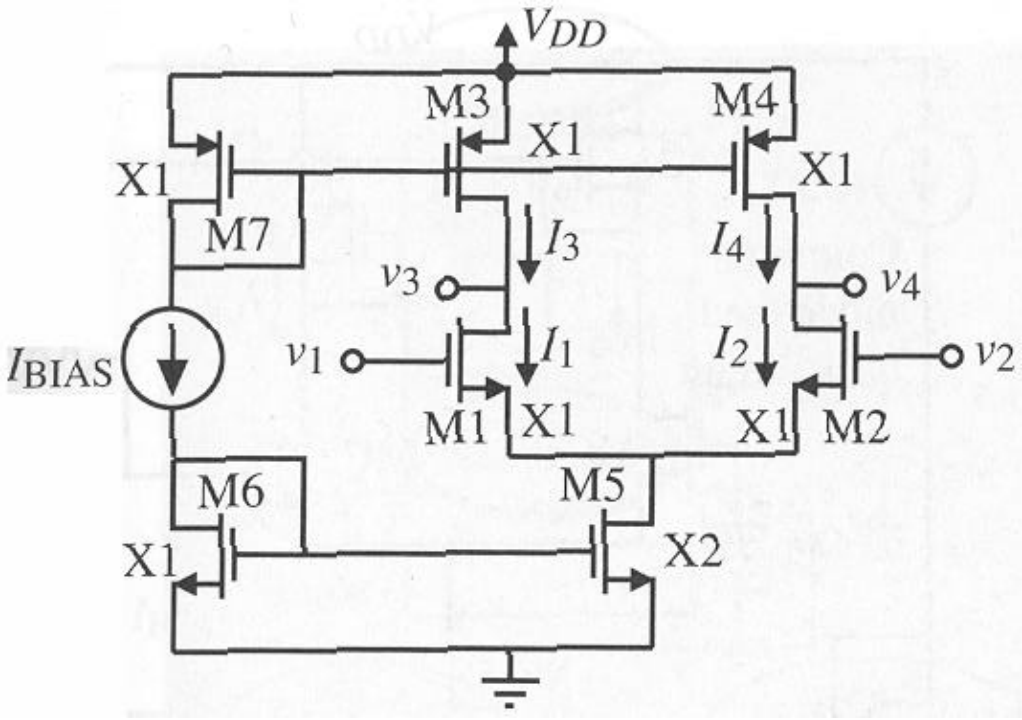


Noise and transistors aspect ratio

- If the load device length is much larger than that of the gain device, then the input-referred 1/f noise is determined primarily by the contribution of the input devices.

- Making the aspect ratio of the input device much larger than that of the load device ensures that the total thermal noise contribution is dominated by the input devices.

Current source load differential amplifier

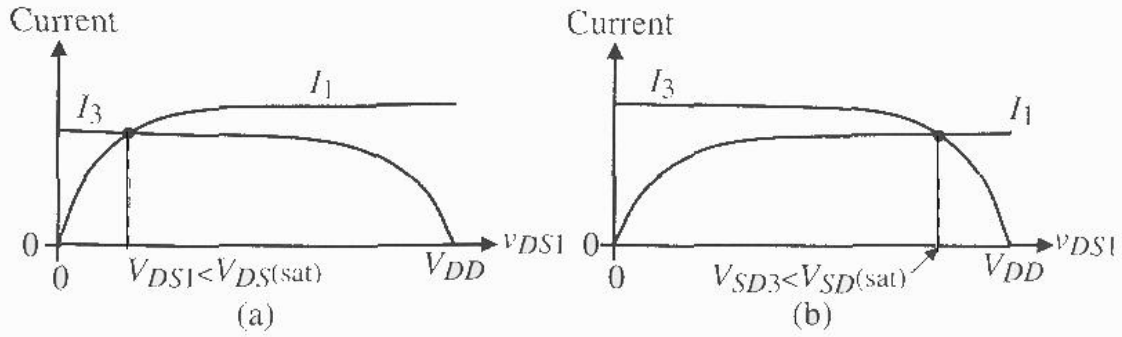


This configuration has the advantage of:

- a larger ICMR because M3 is no longer connected in the diode configuration.
- The small-signal voltage gain is the same.

Current-source load

- The differential amplifier shown presents a challenge that is not immediately obvious. Note that I_{BIAS} defines the currents in M3 and M4 as well as the current in M5.
- It is likely that these currents will not be exactly equal.
- What will happen in this case?
- In general if a dc current flows through both a PMOS and a NMOS transistor, the transistor with the larger dc current will become active.
- This is because the only way the currents can match is for the larger current to reduce the V_{DS} and leave the saturation region.



(a) $I_1 > I_3$. (b) $I_3 > I_1$.

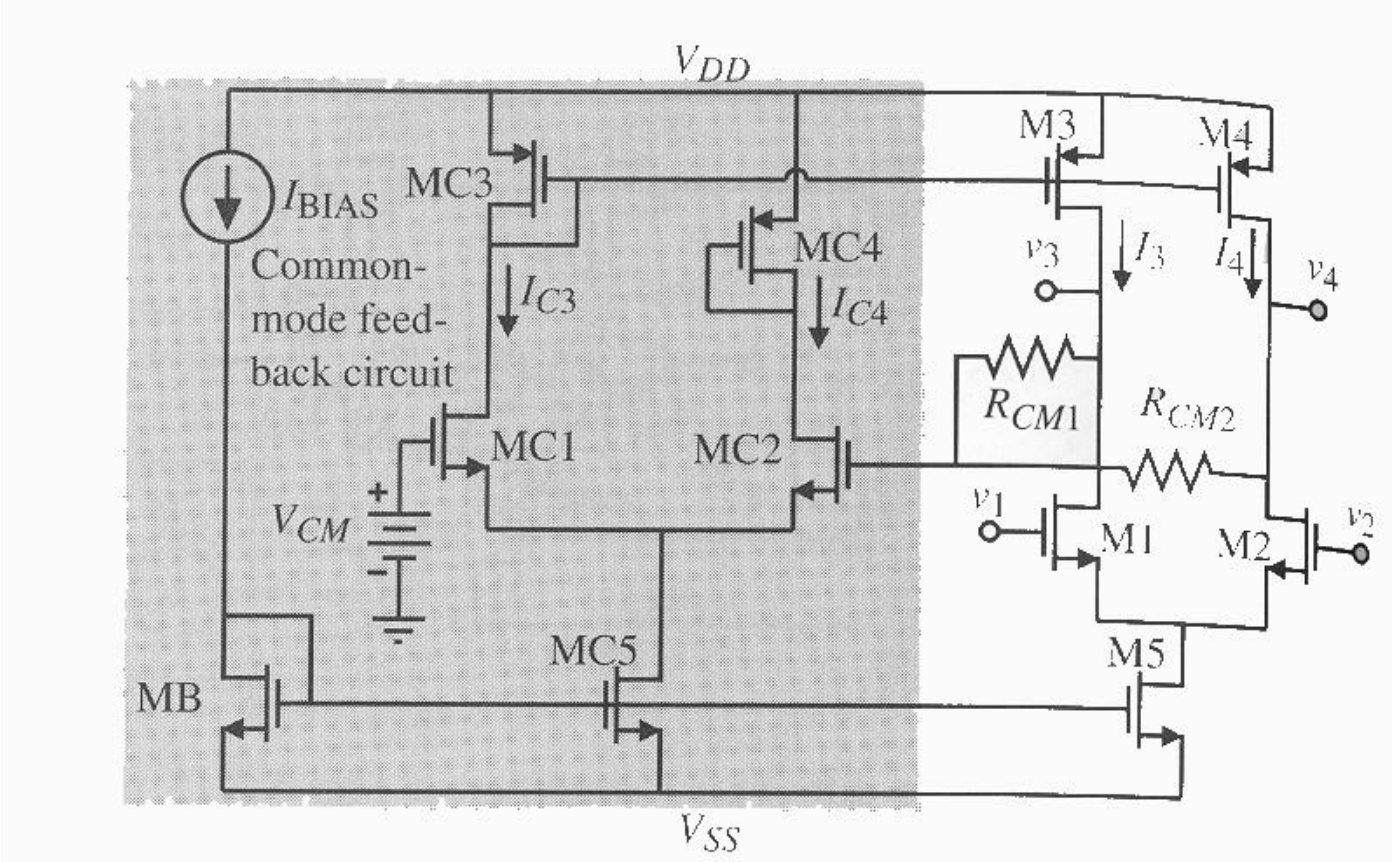
Common-mode output voltage feedback to stabilize the bias current

- As consequence the outputs of the differential amplifier will increase or decrease.

- The key to solving this problem is to note that **both** outputs will increase or decrease.

- Therefore, if we can provide a common-mode feedback scheme, we will be able to stabilize the common mode output voltages of the differential amplifier while allowing the differential-mode output voltage to be determined by the differential input to the amplifier.

Common-mode output voltage feedback to stabilize the bias current



Design of a CMOS Differential Amplifier

- It is important to select the appropriate relationships that connect the design specifications to the design parameters.

- The design in most CMOS circuits consists of an architecture represented by a schematic, W/L values, and dc currents

- Example: for the NMOS inputs OTA, the design parameters are the W/L values of M1 through M5 and the current in M5, I_5 (V_{BIAS} is an external voltage that defines I_5 and generally is replaced by the input of a current mirror)

The starting point of design consists of two types of information:

1) Design constraints (power supply, technology, temperature)

2) Specifications:
    a) Small-signal gain A_V
    b) Frequency response for a given load capacitance ω_{-3dB}
    c) Input common-mode range (ICMR) or maximum and minimum input common-mode voltage [V_{IC}(max) and V_{IC}(min)]
    d) Slew rate for a given load capacitance, SR
    e) Power dissipation, P_{diss}

Design relationship for the differential amplifier

- $A_V=g_{m1}R_{out}$

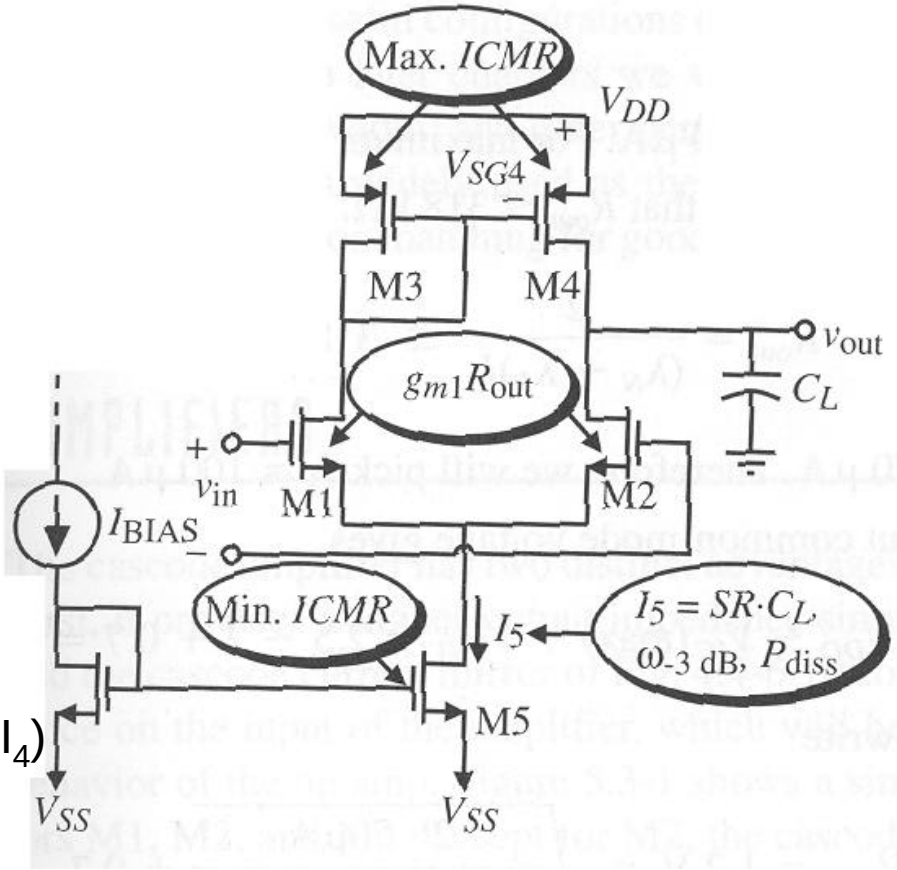
  $\omega_{-3dB}=1/(R_{out}C_L)$

- $V_{IC}(max)=V_{DD}-V_{SG3}+V_{TN1}$

- $V_{IC}(min)=V_{DS5}(sat)+V_{GS1}$

- $SR=I_5/C_L$

- $P_{diss}=(V_{DD}+|V_{SS}|)(I5)=(V_{DD}+|V_{SS}|)(I_3+I_4)$



Current mirror load differential amplifier design procedure

The design procedure assume that A_V, ω_{-3dB}, $V_{IC}(max)$, $V_{IC}(min)$, SR, P_{diss}, are given.

1. Choose I_5 to satisfy the slew rate knowing C_L or the power dissipation, P_{diss}.
2. Check to see R_{out} will satisfy the frequency response and if not, change I_5 or modify the circuit (choose a different topology)
3. Design W3/L3 (W4/L4) to satisfy the upper ICMR
4. Design W1/L1 (W2/L2) to satisfy the small signal voltage gain A_V
5. Design W5/L5 to satisfy the lower ICMR
6. Iterate where necessary.

Design example

- Design the currents and W/L values of the current-mirror load differential amplifier of the scheme seen before to satisfy the following specifications:
- VDD=-VSS=2.5V, SR>/=10V/us (CL=5pF), a small-signal differential gain of 100V/V, ICMR</=2V, f-3dB>/=100kHz (CL=5pF), and Pdiss</=1mW.
- Use the model parameters of K_N'=110uA/V^2, K_P'=50uA/V^2, V_{TN}=0.7V, V_{TP}=-0.7V, λn=0.04V^{-1}, λp=0.05V^{-1}.