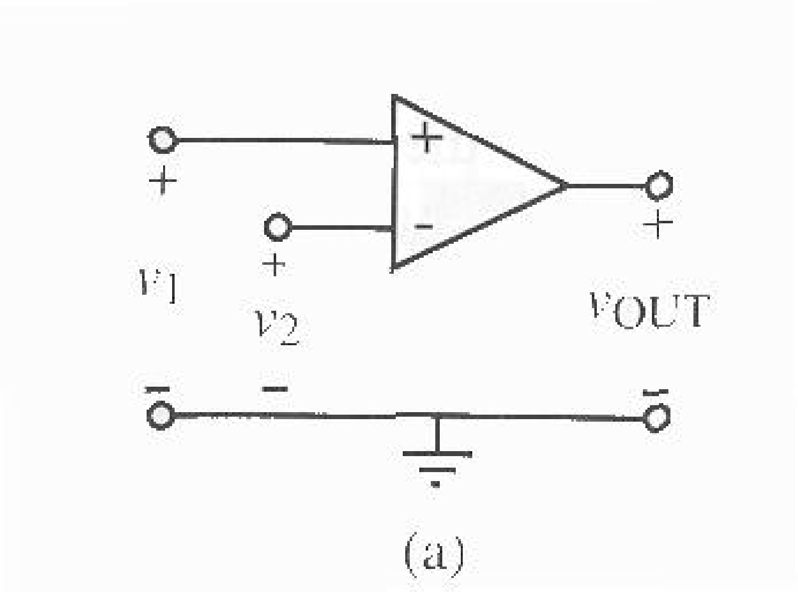
Differential amplifiers

Schematic model for a differential amplifier



- v_1, v_2, v_{OUT} are called single-ended voltages: they are defined respect to ground

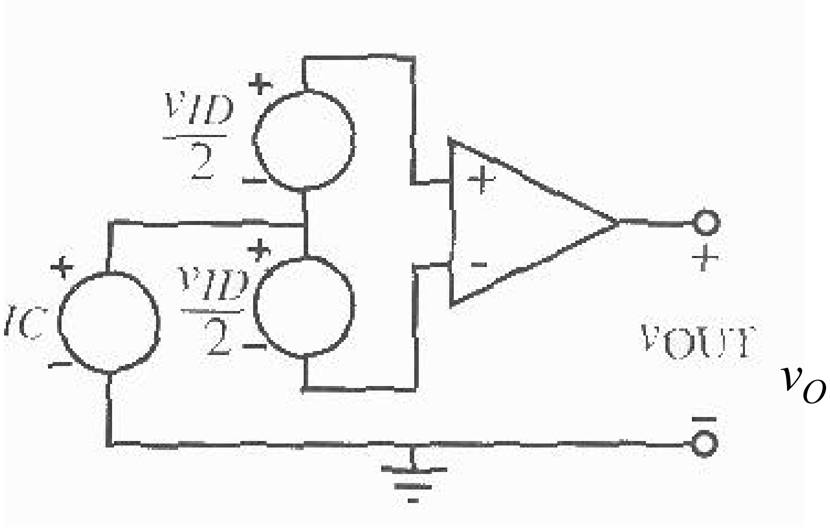
- v_{ID} =differential-mode input voltage

  $v_{ID}=v_1-v_2$

- v_{IC}=common-mode input voltage, is defined as the average value of v_1 and v_2

$$v_{IC}=\frac{v_1+v_2}{2}$$

Differential mode and common-mode



$$v_1 = v_{IC} + \frac{v_{ID}}{2}$$

$$v_2 = v_{IC} - \frac{v_{ID}}{2}$$

$$v_{OUT} = A_{VD} v_{ID} \pm A_{VC} v_{IC} = A_{VD}(v_1 - v_2) \pm A_{VC}\left(\frac{v_1 + v_2}{2}\right)$$

A_{VD}=the differential-mode voltage gain
A_{VC}=the common-mode voltage gain
The +/- sign preceding the common-mode voltage gain implies that the polarity of this voltage gain is not known beforehand.

Differential amplifier characteristics

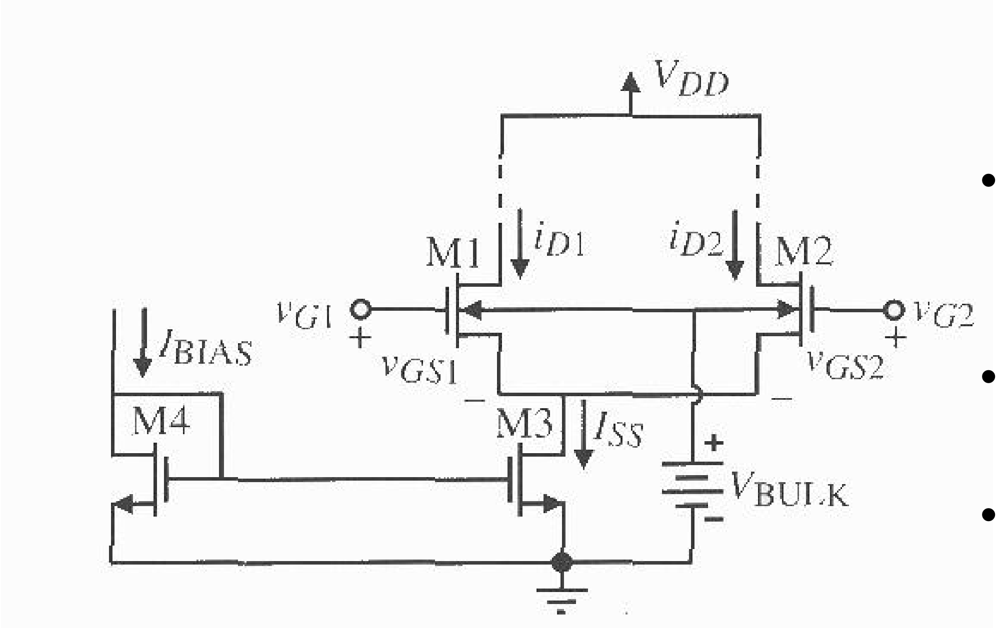
- The objective of the differential amplifier is to amplify only the difference between two different potentials regardless of the common-mode value.
- Thus it can be characterized by its common-mode rejection ratio CMRR, which is the ratio of the magnitude of the differential gain to the common-mode gain.
- An ideal differential amplifier will have a zero value of A_{VC} and therefore an infinite CMRR.
- The input common-mode range (ICMR) specifies over what range of common-mode voltages the differential amplifier continues to sense and amplify the difference signal with the same gain.

Offset voltage

- Another characteristic affecting performance of the differential amplifier is offset voltage.

- In CMOS differential amplifier, the most serious offset is the offset voltage.
- Ideally when the input terminals are connected together, the output voltage is at a desired quiescent point. In a real differential amplifier, the output offset voltage is the difference between the actual output voltage and the ideal output voltage when the input terminals are connected together.
- If this offset voltage is divided by the differential voltage gain of the differential amplifier, then it is called the input offset voltage (VOS [5-20 mV]).

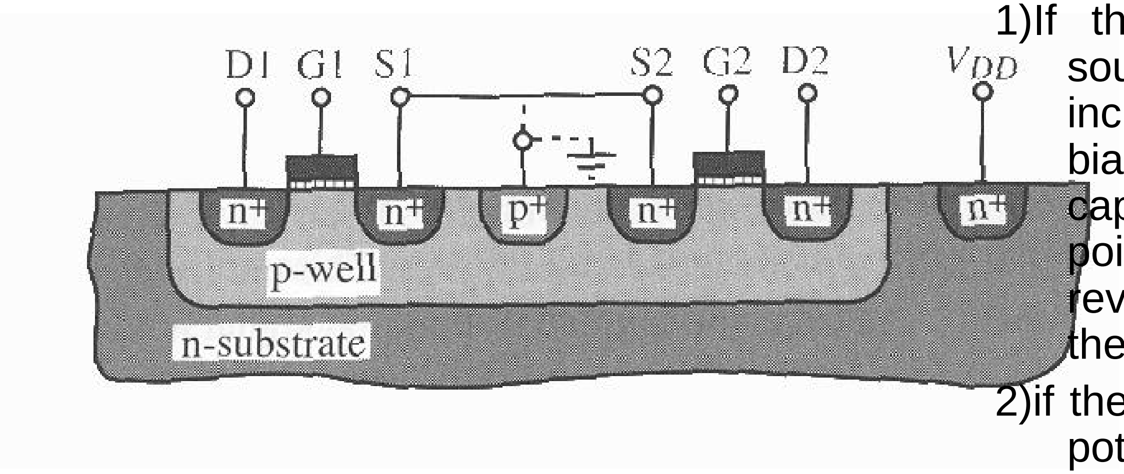
Large signal analysis



- M1 and M2 are biased by the current I_{SS}
- M1 and M2 are called source-coupled pair
- M3, M4 are a current sink
- Because the source of M1 and M2 are not connected to ground, the question of where to connect the bulk arises.

  It depends on the technology.

Bulk connection



- If the CMOS technology is p-well, then the nMOS are fabricated inside the well.

The solutions possible are:

1) Bulks of M1 and M2 connected to the source and let the well float
2) To connect the well to ground

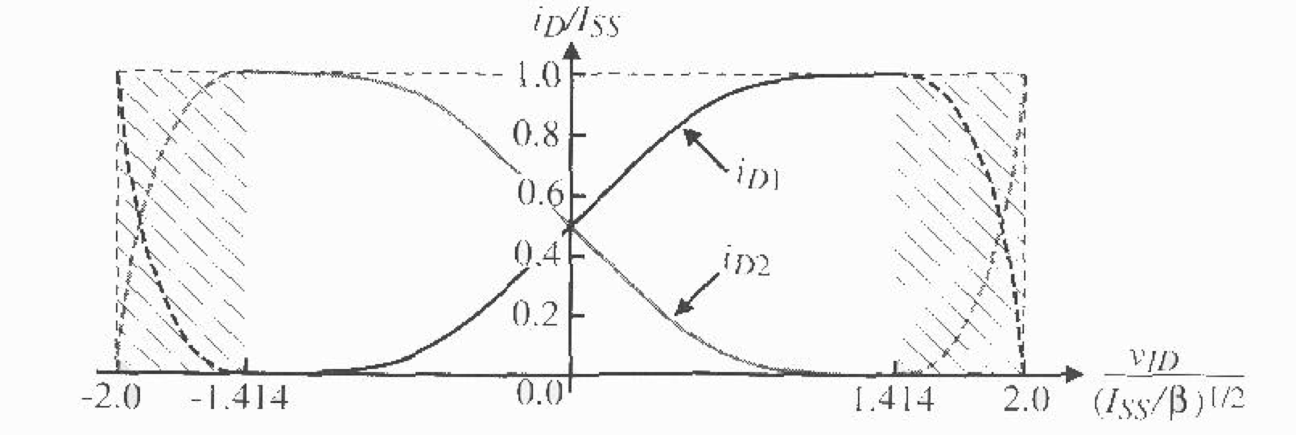
Consequence:

1)If the p-well is connected to the sources, the threshold voltage is not increased because of the reverse-biased bulk-source junction. The capacitance at the source-coupled point to ground becomes the entire reverse-biased pn junction between the p-well and the n-substrate.

2)if the p-well is connected to the lower potential (ground), then the threshold voltage will increase and vary with the common-mode input voltage but the capacitance is reduced to the reversed biased sources and the p-well

Large signal transconductance characteristic

- The large signal analysis begins by assuming that M1 and M2 are perfectly matched.
- The large-signal characteristics can be developed by assuming that M1 and M2 are always in saturation. This condition is reasonable in most cases and demonstrates the behavior even when this assumption is not valid.



Large-signal behavior

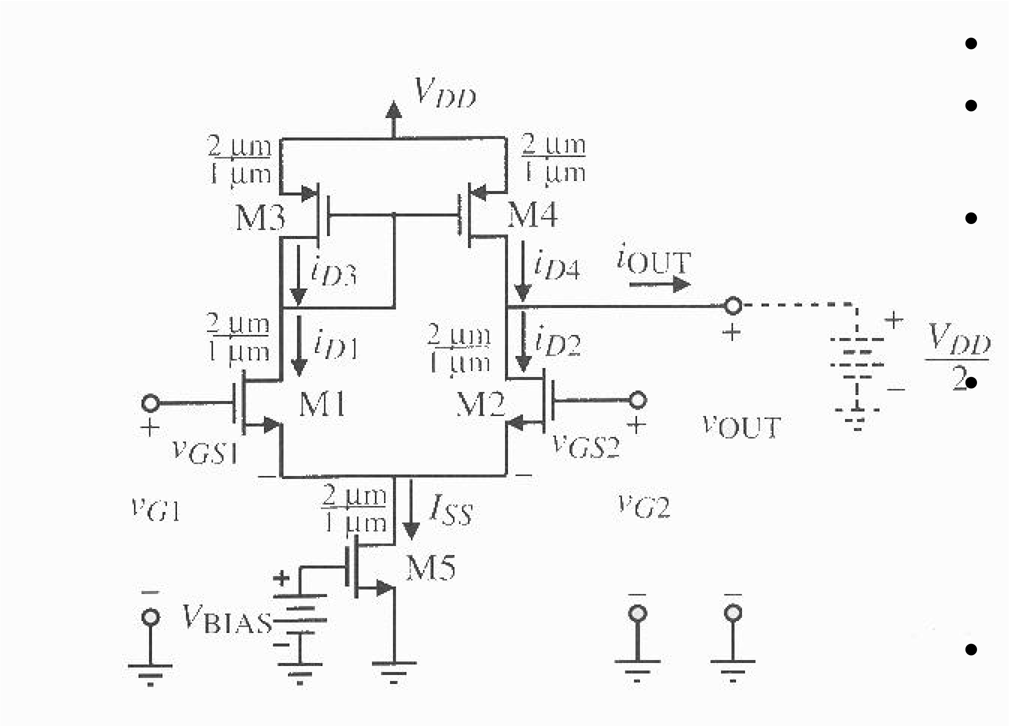
$$v_{ID} = v_{GS1} - v_{GS2} = \left(\frac{2i_{D1}}{b} \right)^{1/2} - \left(\frac{2i_{D2}}{b} \right)^{1/2}$$

$$I_{SS} = i_{D1} + i_{D2}$$

$$i_{D1} = \frac{I_{SS}}{2} + \frac{I_{SS}}{2} \left(\frac{bv_{ID}}{I_{SS}} - \frac{b^2 v_{ID}}{4I_{SS}^2} \right) \qquad i_{D2} = \frac{I_{SS}}{2} - \frac{I_{SS}}{2} \left(\frac{bv_{ID}}{I_{SS}} - \frac{b^2 v_{ID}}{4I_{SS}^2} \right)$$

$$g_m = \frac{\partial I_{D1}}{\partial V_{ID}} (V_{ID} = 0) = (bI_{SS} / 4)^{1/2} = \left(\frac{k'_1 I_{SS} W_1}{4L_1} \right)^{1/2}$$

Large signal analysis



- For $v_{ID}=0$ $I_{D1}=I_{D2}=I_{SS}/2$
- The current in M1 fixes the current in M3 mirrored in M4
- If $v_{GS1}=v_{GS2}$ and M1 and M2 matched, the currents in M1 and M2 are equal.
- Thus, the current tha M4 sources to M2 should be equal to the curren that M2 requires, causing i_{OUT} to be zero-provided that the load is negligible.
- If these current are not equal, if the external load is infinite that current flow in the self resistance of M2 and M4 ($r_{02}//r_{04}$)

- If $v_{GS1} > v_{GS2}$, then i_{D1} increases with respect to i_{D2} since

$$I_{SS} = i_{D1} + i_{D2}.$$

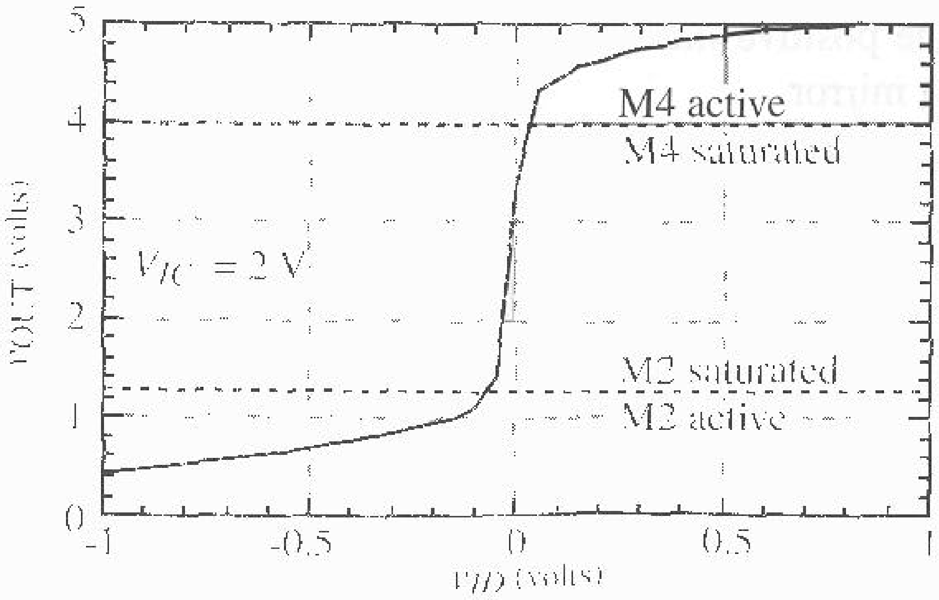
This increase in i_{D1} implies an increase in i_{D3} and i_{D4}.
However i_{D2} decreases when v_{GS1} is greater than v_{GS2}.
Therefore the only way to establish circuit equilibrium is for i_{OUT} to become positive and v_{OUT} to increase.

- If $v_{GS1} < v_{GS2}$ i_{OUT} becomes negative and v_{OUT} decreases.
- The differential-in, differential-out transconductance is twice gm:

$$g_{md} = \frac{\partial i_{OUT}}{\partial V_{ID}} (V_{ID} = 0) = \left(\frac{k'_1 I_{SS} W_1}{L_1} \right)^{1/2}$$

Which is exactly equal to the transconductance of the common-source MOS if $I_D = I_{SS}/2$

The large-signal voltage transfer function



- V_{IC}=2V
- v_{ID} is swept from –1 to 1V.
- The characteristic can be either inverting or noninvarting depending on how the input signal is applied.
- If v_{IN}=v_{GS1}-v_{GS2}, then the voltage gain is noninverting.
- The largest small-signal gain occurs when both M2and M4 are saturated.
- M2 is saturated when:

$$v_{DS2} \geq v_{GS2} - V_{TN} \rightarrow v_{OUT} - V_{S1} \geq V_{IC} - 0.5 v_{ID} - V_{S1} - V_{TN}$$

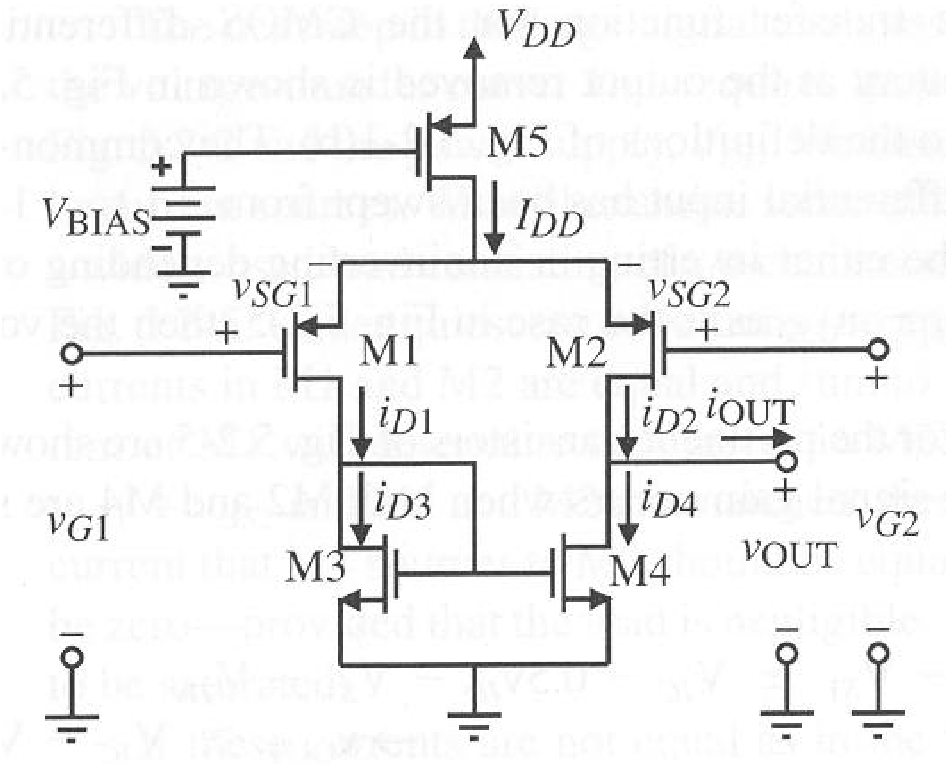
$$\rightarrow \mathrm{v_{OUT}} \geq V_{IC} - V_{TN}$$

- M4 is saturated when:

$$v_{SD4} \geq v_{GS4} - |V_{TP}| \rightarrow V_{DD} - v_{OUT} \geq v_{SG4} - |V_{TP}|$$

$$\rightarrow \mathrm{v_{OUT}} \leq V_{DD} - v_{SG4} + |V_{TP}|$$

CMOS differential amplifier using pMOS input



- If the tecnology is n-well, then the bulks of the input pMOS can be connected either to VDD or to their sources assuming that M1 and M2 are fabricated in their own n-well that can float.

Input common-mode range ICMR

- ICMR is found setting v_{ID} to zero and vary v_{IC} until one of the transistors in the differential amplifier is not longer saturated.

  (connecting the input together and sweeping the common-mode input voltage).

  For the differential amplifier n-MOS input seen before the highest V_{IC} (max) can be found as follows.

  There are two paths from V_{IC} to V_{DD} that we must examine.

  The first is from G1 through M1 and M3 to V_{DD}. The second is from G2 through M2 and M4 to V_{DD}.

1st path:

$$V_{IC}(\max) = V_{G1}(\max) = V_{DD} - V_{SG3} - V_{DS1} + V_{GS1}$$

$$V_{IC}(\max) = V_{DD} - V_{SG3} + V_{TN}$$

2nd path

$$V_{IC}(\max)' = V_{DD} - V_{DS4}(sat) - V_{DS2} + V_{GS2} = V_{DD} - V_{DS4}(sat) + V_{TN2}$$

- Since the 2nd path allows higher value of V_{IC}(max), we will select the 1st path from a worst-case viewpoint. Thus, the maximum input common-mode is equal to the power supply minus the drop across M3 plus the threshold voltage of M1.
- If we want to increase the positive limit of V_{IC}, we will need to select a load circuit that is different from the current mirror.
- The lowest input voltage at the gate of M1 (or M2) is found to be

$$V_{IC}(\min) = V_{SS} + V_{DS5}(sat) + V_{GS1} = V_{SS} + V_{DS5}(sat) + V_{GS2}$$

- Those equations are important in design phase: the value W3/L3 will determine the value of V_{IC}(max), W1/L1 and W2/L2 and W5/L5 will determnine the value of V_{IC}(min).

V_{IC} Shift due to the V_T

- To design the differential amplifier to meet a specified negative common-mode range the designer must consider the worst-case V_T spread (specified by the process) and adjust I_{SS} and β_3 to meet the requirements.

- The worst-case V_T spread affecting positive common-mode range for the configuration nMOS input is a p-channel threshold magnitude ($|V_{T03}|$) and a low n-channel threshold (V_{T01}).

- An improvement can be obtained when the substrates of the input devices are connected to ground. This connection results in negative feedback to the sources of the input devices.