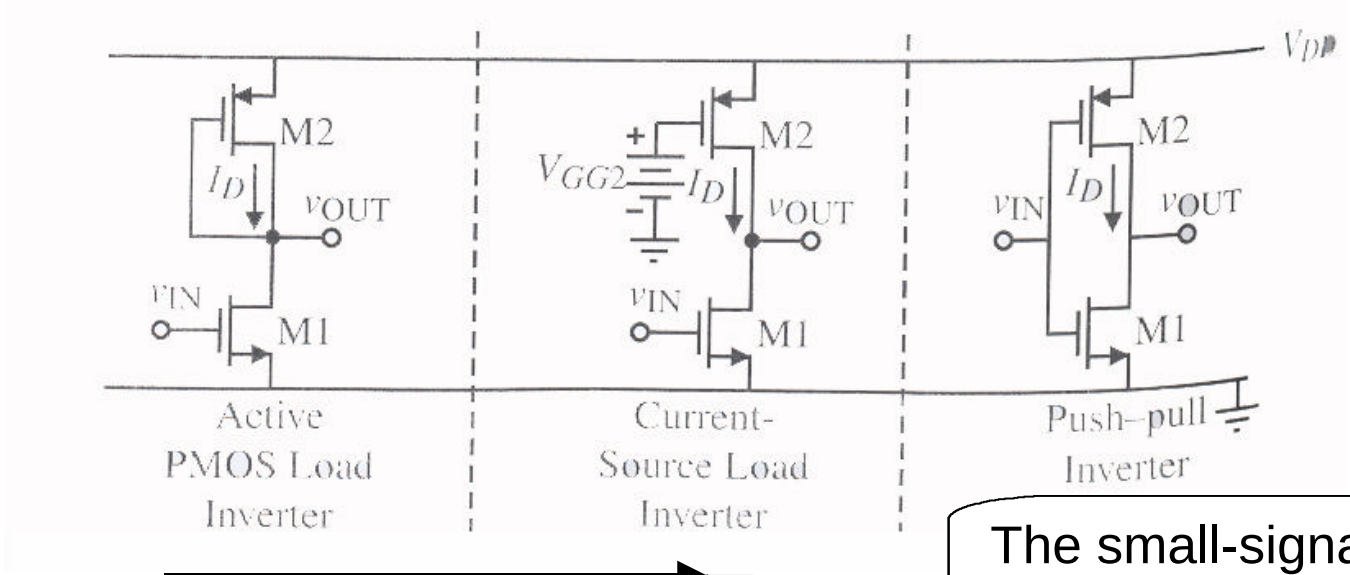
CMOS Amplifier

Inverters

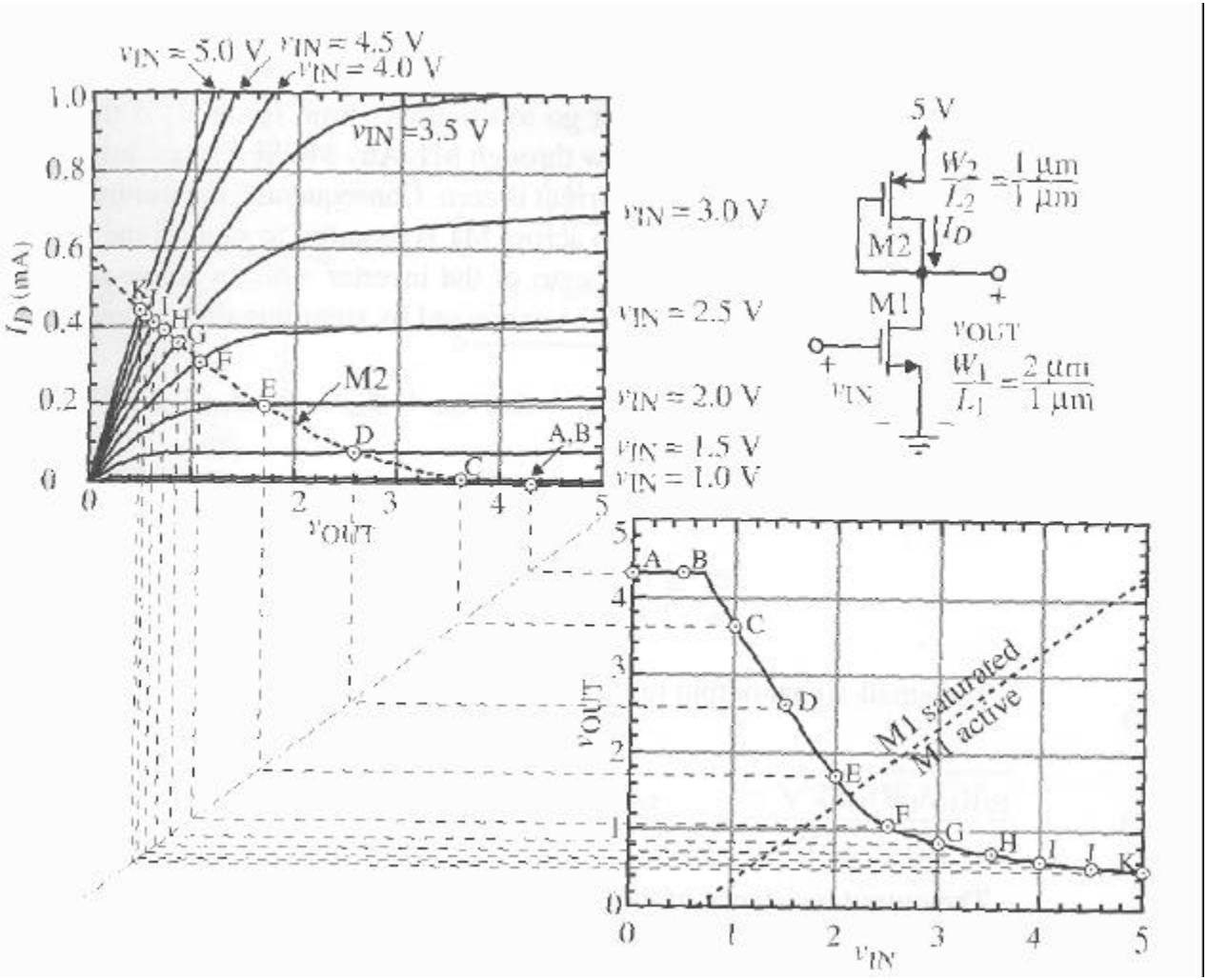
- The inverter is the basic gain stage for CMOS circuits.

- Typically, the inverter uses the common source configuration with either an active resistor for a load or a current sink/source as a load resistor.



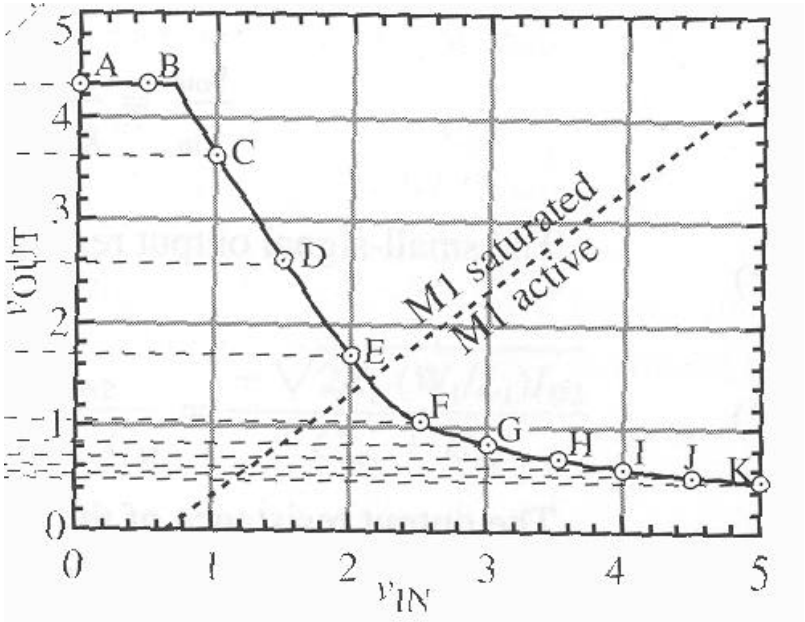
The small-signal gain increse

Active Load Inverter: voltage-transfer function



1) The output-signal swing will experience a limitation for negative swings.
2) Low gain

Large-signal swing limitations of the active-resistor load inverter



$$V_{out}(\max) \cong V_{DD} - |V_{TP}|$$

- This limit ignores the subthreshold current that flows in every MOSFET.
- This very small current will eventually allow the output voltage to approach V_{DD}.
- In order to find V_{out}(min) we first assume that M1 will be in the nonsaturated (active) region and that $V_{T1}=|V_{T2}|=V_T$.

Large-signal swing limitations of the active-resistor load inverter

- We have determined the region where M1 is active by plotting the equation

$$V_{DS1} \geq V_{GS1} - V_{TN} \rightarrow V_{OUT} \geq V_{IN} - 0.7V$$

  which corresponds to the saturation voltage of M1.
- Below this region, the current through M1 is:

$$I_D = b_1\left((V_{GS1} - V_T)V_{DS1} - \frac{V_{DS1}^2}{2}\right) = b_1\left((V_{DD} - V_T)V_{OUT} - \frac{V_{OUT}^2}{2}\right) \quad \text{assuming} V_{IN}(\max) = V_{DD}$$

- And the current through M2 is:

$$I_D = \frac{b_2}{2}\left(V_{GS2} - |V_T|\right)^2 = \frac{b_2}{2}\left(V_{DD} - V_{OUT} - |V_T|\right)^2$$

- Equating (1) and (2) and solving for Vout gives

$$V_{OUT}(\min) = V_{DD} - V_T - \frac{V_{DD} - V_T}{\sqrt{1 + (b_2 / b_1)}}$$

- We have assumed in developing this expression that the maximum value of Vin is equal to VDD.

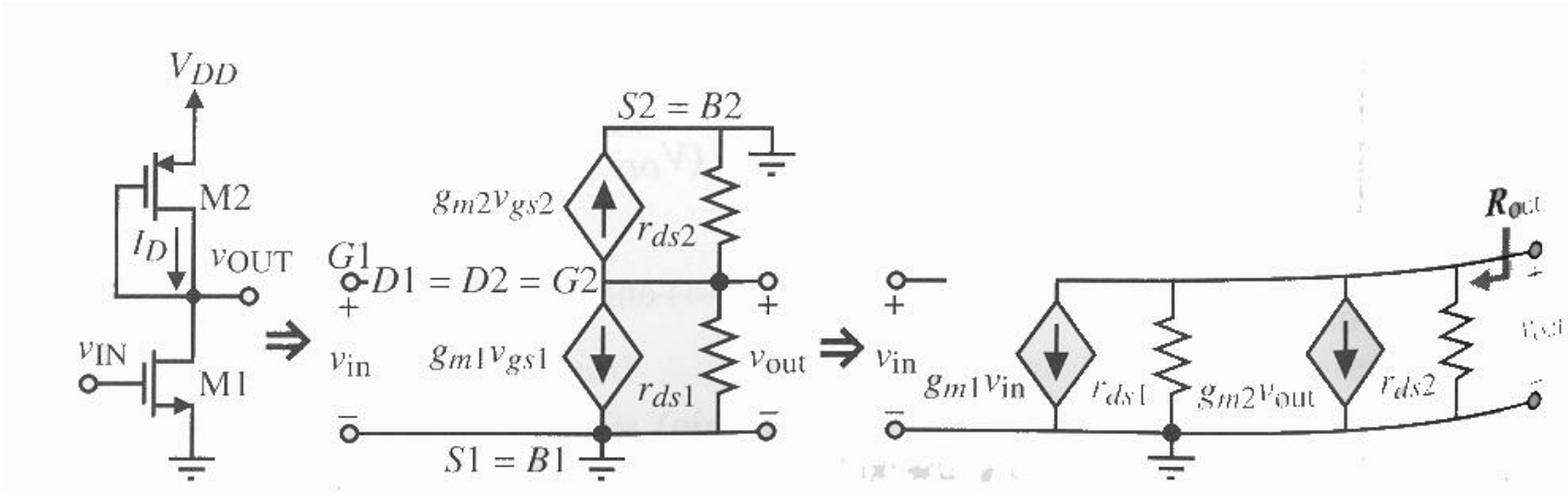
- It is important to understand how the lower limit of this equation comes. The reason that the output voltage cannot go to the lower limit (ground) is that the voltage across M2 produces current that must flow through M1.

  Any MOSFET can only have zero voltage across its drain-source if the drain current is zero. Consequently, the minimum value VOUT is equal to whatever drain-source drop across M1 is required to support the current defined by M2.

Active load inverter: small-signal gain

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2} + g_{m2}} \cong -\frac{g_{m1}}{g_{m2}} = -\left(\frac{K'_N W_1 L_2}{K'_P L_1 W_2} \right)^{1/2}$$

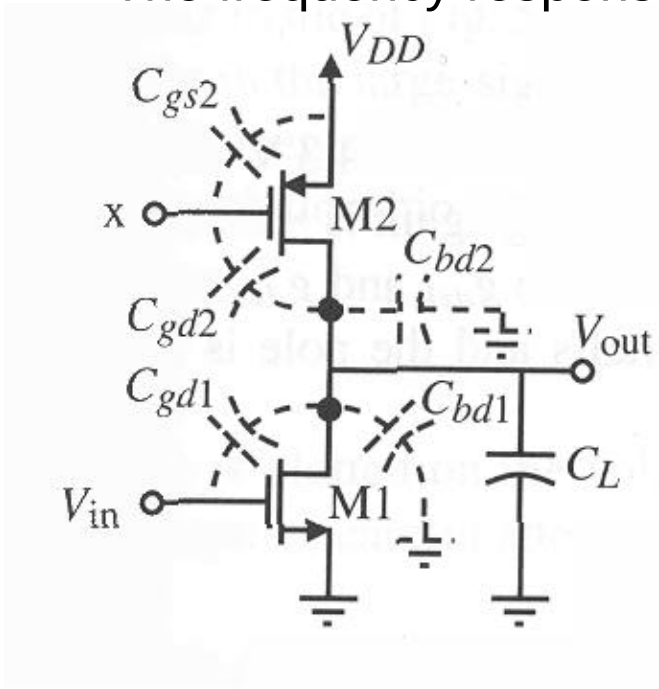
$$R_{OUT} = \frac{1}{g_{ds1} + g_{ds2} + g_{m2}} \cong \frac{1}{g_{m2}}$$



Active load inverter: frequency response

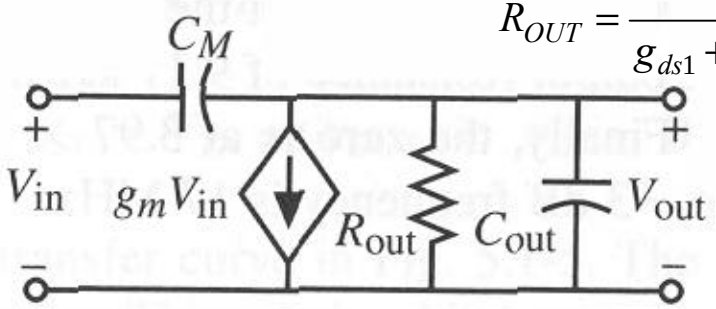
- The frequency response of the cirtcuit is:

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{-g_m R_{OUT}(1 - s/z_1)}{1 - s/p_1}$$



$$g_m = g_{m1}$$

$$R_{OUT} = \frac{1}{g_{ds1} + g_{ds2} + g_{m2}} \cong \frac{1}{g_{m2}}$$



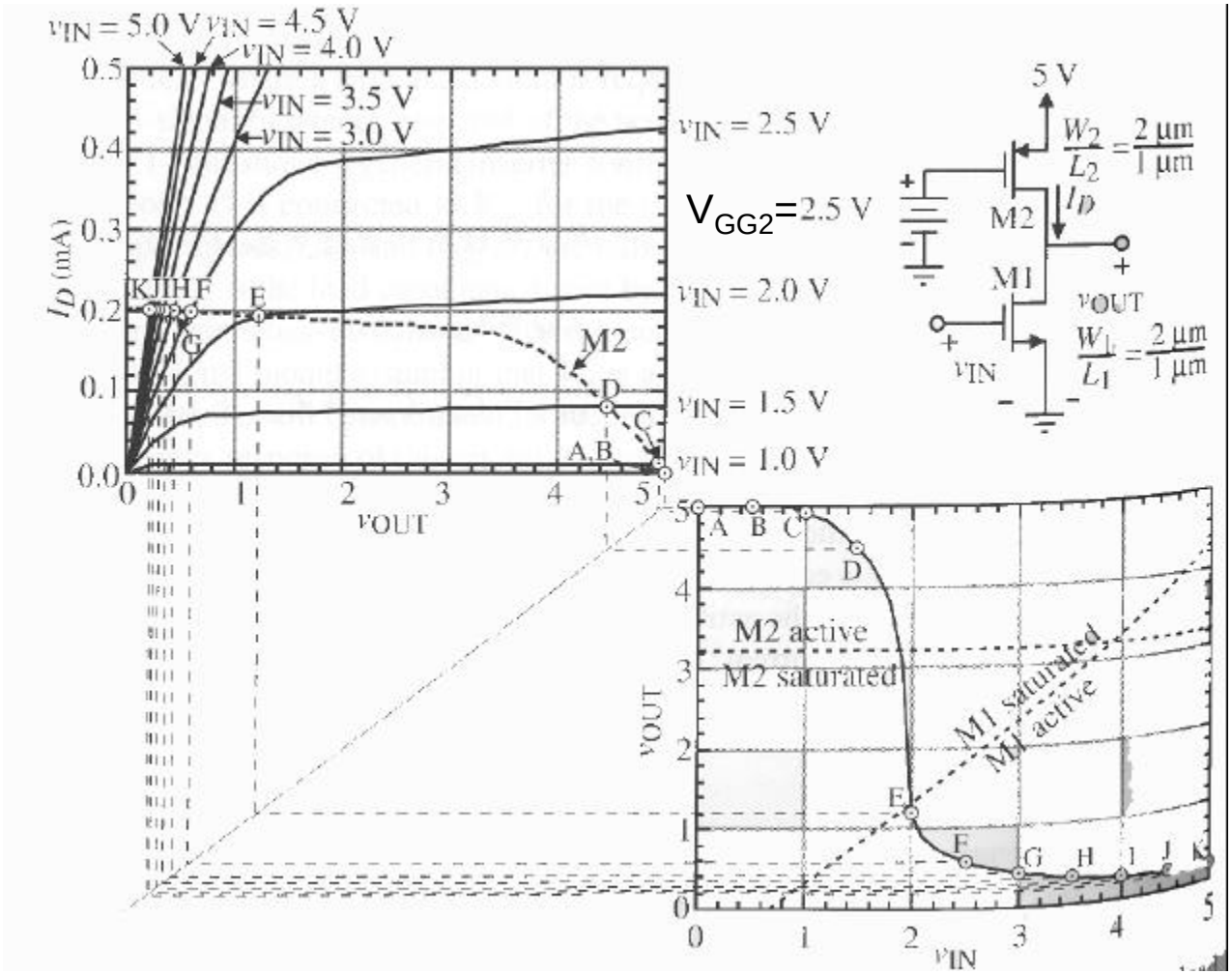
$$p_1 = \frac{-1}{R_{OUT}(C_{out} + C_M)} \approx \frac{-g_m}{C_{out} + C_M} = \frac{-\sqrt{2K_N(W_1/L_1)I_{D2}}}{C_{out} + C_M}$$

$$z_1 = \frac{g_m}{C_M}$$

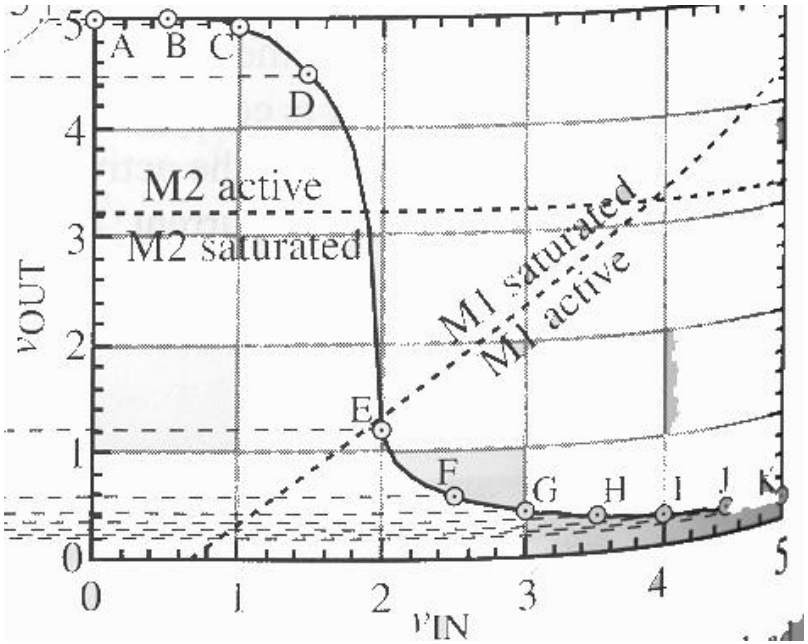
$$C_M = C_{gd1}$$

$$C_{OUT} = C_{bd1} + C_{bd2} + C_{gs2} + C_L$$

Current-source inverter: voltage-transfer function



Large-signal swing limitations of the current-source inverter



- The region of operation for the transistors are found by expressing the saturation relationship for each transistor

- For M1:

$$V_{DS1} \geq V_{GS1} - V_{TN} \rightarrow V_{OUT} \geq V_{IN} - 0.7V$$

- For M2:

$$V_{SD2} \geq V_{SG2} - |V_{TP}| \rightarrow V_{DD} - V_{OUT} \geq V_{DD} - V_{GG2} - |V_{TP}| \rightarrow V_{OUT} \leq 3.2V$$

When V_{OUT} is less than 3.2V M2 is saturated.

Large-signal swing limitations of the current-source inverter

- Since when M1 is off, the voltage across M2 can go to zero, allowing the output voltage to equal VDD providing no output dc current is required.

$$V_{OUT}(\max)=V_{DD}$$

- The lower limit can be found by assuming that M1 will be in the non saturation region.

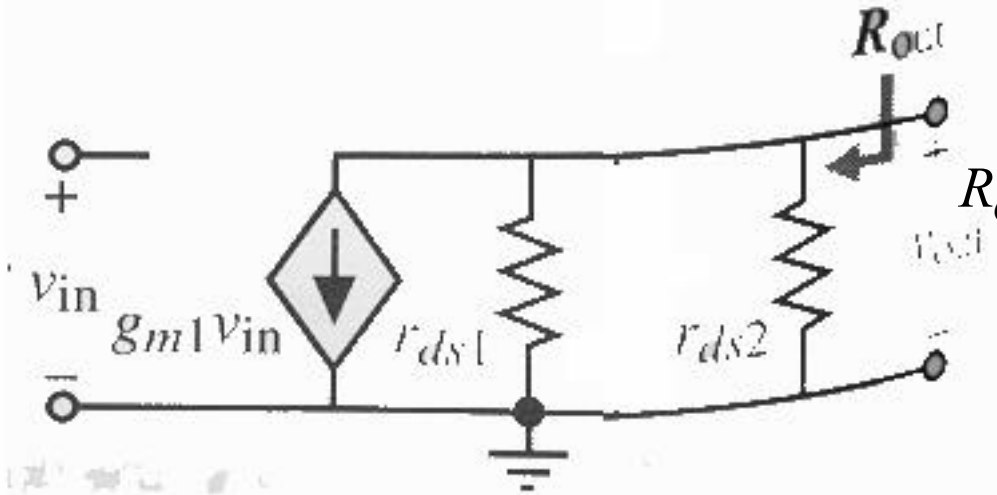
$$V_{OUT}(\min) = (V_{DD} - V_{T1})\left\{1-\left[1-\left(\frac{b_2}{b_1}\right)\left(\frac{V_{SG2}-|V_{T2}|}{V_{DD}-V_{T1}}\right)^2\right]^{1/2}\right\}$$

This results assumes that V_{IN} is taken to V_{DD}.

Current-source inverter : small-signal gain

- The small-signal performance can be found using the small-signal model with $g_{m2}v_{gs2}=0$ (this account for the fact that the gate of M2 in on ac ground).

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1}+g_{ds2}} = \left(\frac{2K'_N W_1}{L_1 I_D}\right)^{1/2}\left(\frac{-1}{l_1-l_2}\right) \propto \frac{1}{\sqrt{I_D}}$$



$$R_{OUT} = \frac{1}{g_{ds1}+g_{ds2}} \cong \frac{1}{I_D(l_1+l_2)}$$

- Higher gain, higher output resistance.

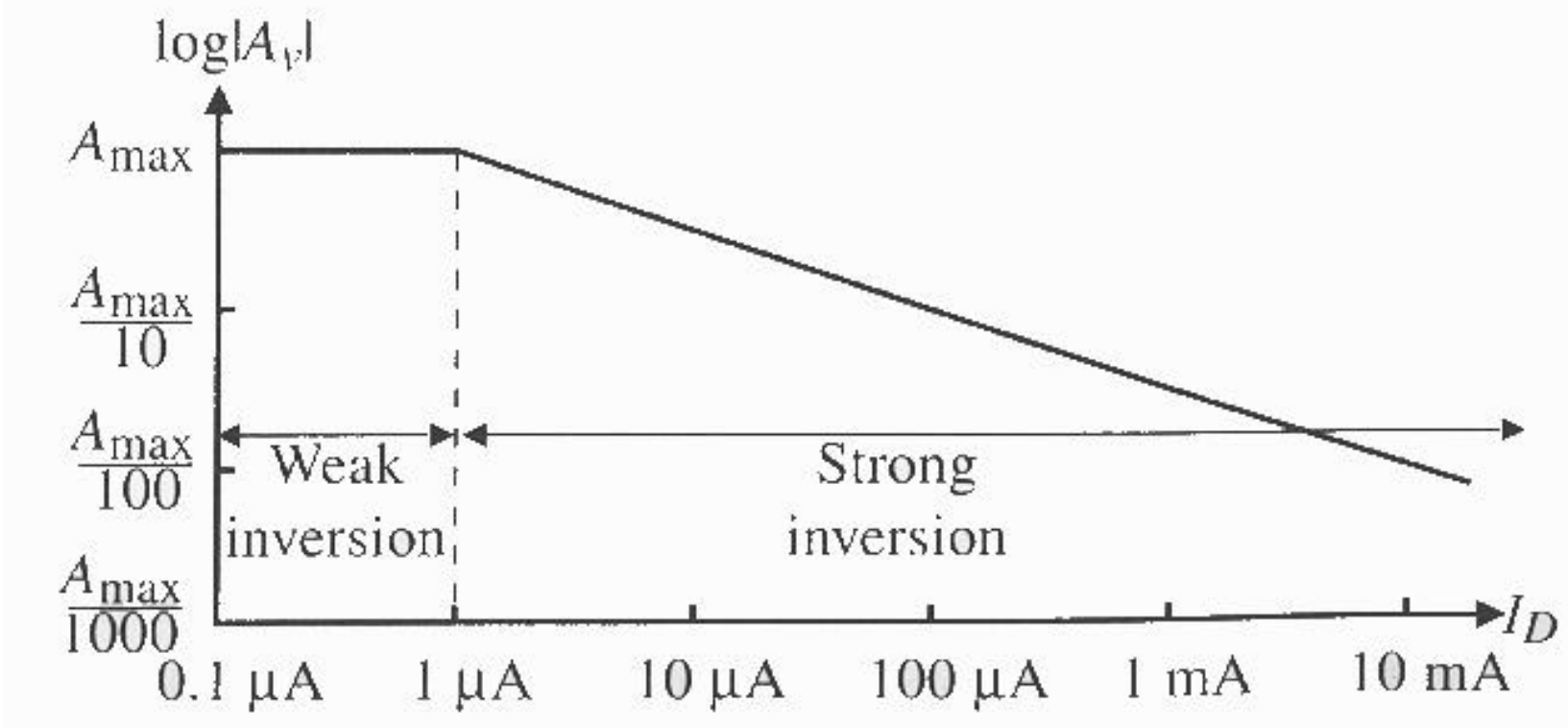
Current-source inverter : small-signal gain

- This is a significant result in that the gain increases as the dc current decreases. It is a result of the output conductance being proportional to the bias current, whereas the transconductance is proportional to the square root of the bias current.

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1}+g_{ds2}} = \left(\frac{2K'_N W_1}{L_1 I_D}\right)^{1/2}\left(\frac{-1}{l_1 - l_2}\right) \propto \frac{1}{\sqrt{I_D}}$$

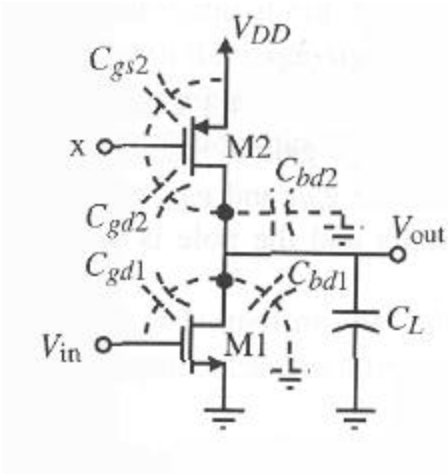
- The increase of gain as I_D decreases hold true until this current reaches the subthreshold region of operation, where weak inversion occurs. At this point the transconductance becomes proportional to the bias current and the small-signal voltage gain becomes constant as a function of bias current.

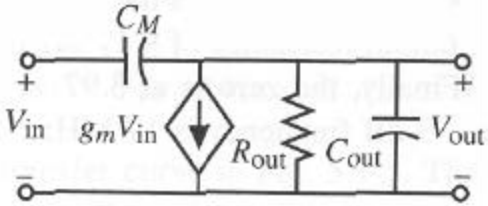
Current source inverting amplifier: influence of the dc drain current on the small-signal voltage gain



Current-source inverter : frequency response

- Lower bandwidth





$$R_{OUT} = \frac{1}{g_{ds1} + g_{ds2}} \qquad g_m = g_{m1}$$

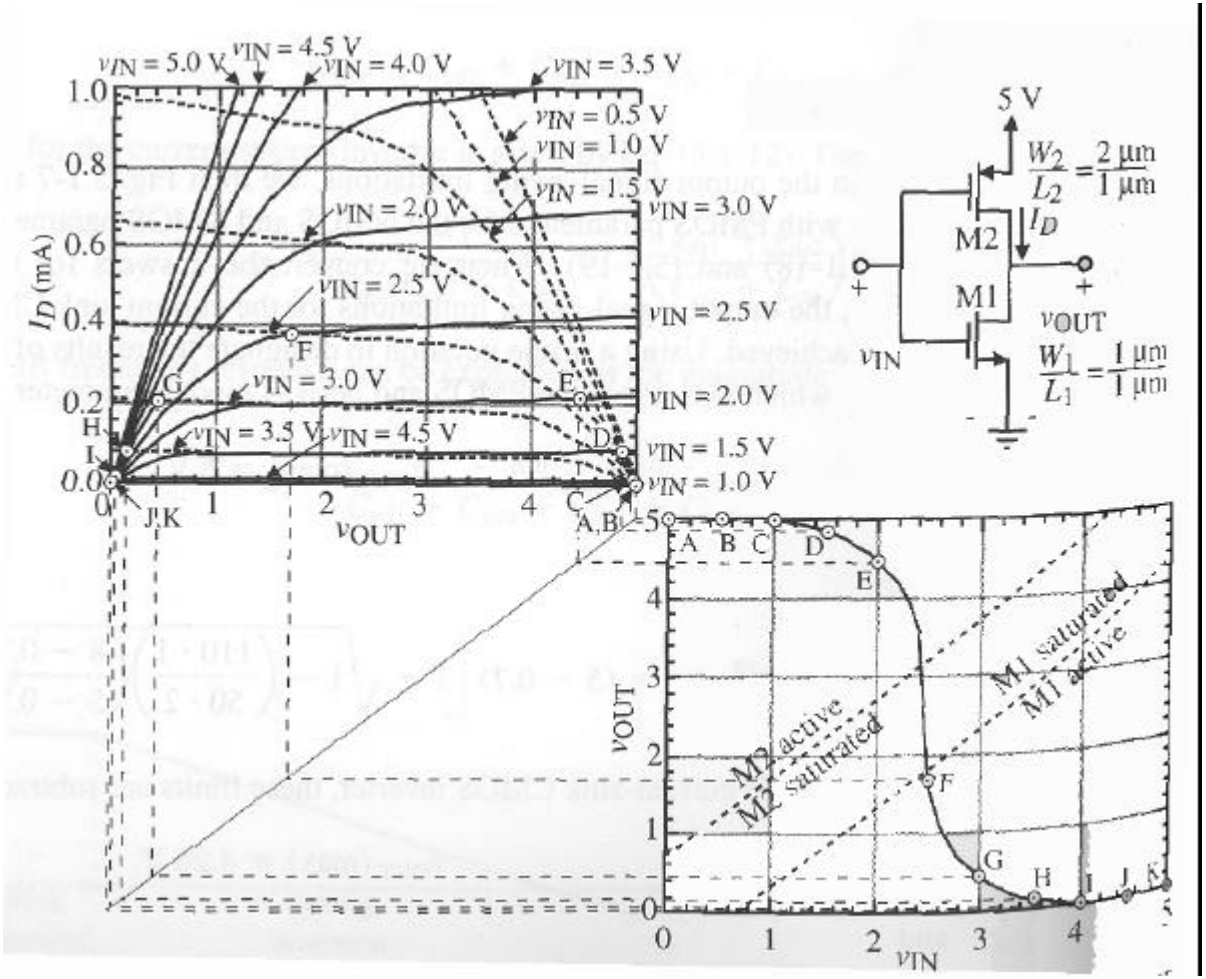
$$C_M = C_{gd1}$$

$$C_{OUT} = C_{bd1} + C_{bd2} + C_{gd2} + C_L$$

$$p_1 = \frac{-1}{R_{OUT}(C_{out} + C_M)} = -\left(\frac{g_{ds1} + g_{ds2}}{C_{out} + C_M}\right)$$

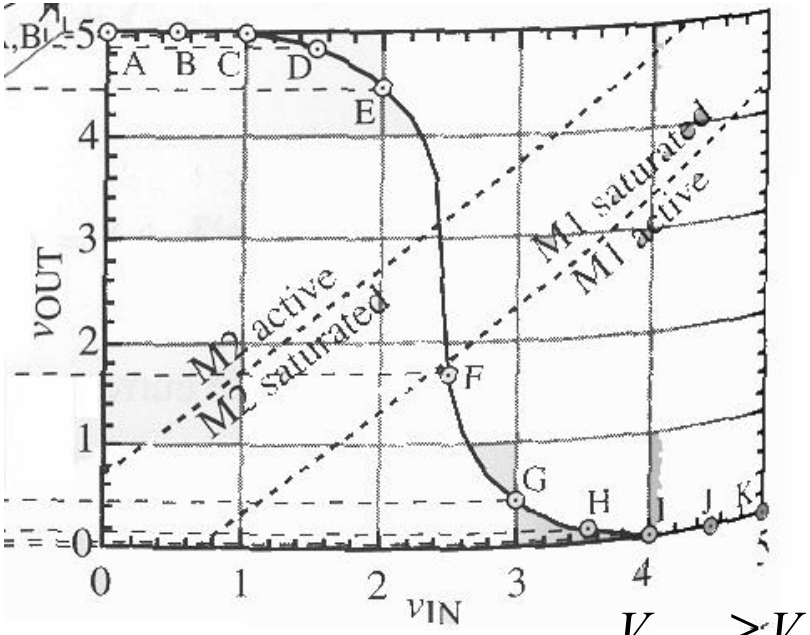
$$z_1 = \frac{g_m}{C_M}$$

Push-Pull inverter: voltage-transfer function



Higher gain

Large-signal swing limitations of the Push-Pull inverter



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- For M2:

$$V_{SD2} \geq V_{SG2} - |V_{TP}| \rightarrow V_{DD} - V_{OUT} \geq V_{DD} - V_{IN} - |V_{TP}|$$

$$\rightarrow V_{OUT} \leq V_{IN} + 0.7V$$

- Largest gain (steepest slope) always occurs when all transistors are saturated

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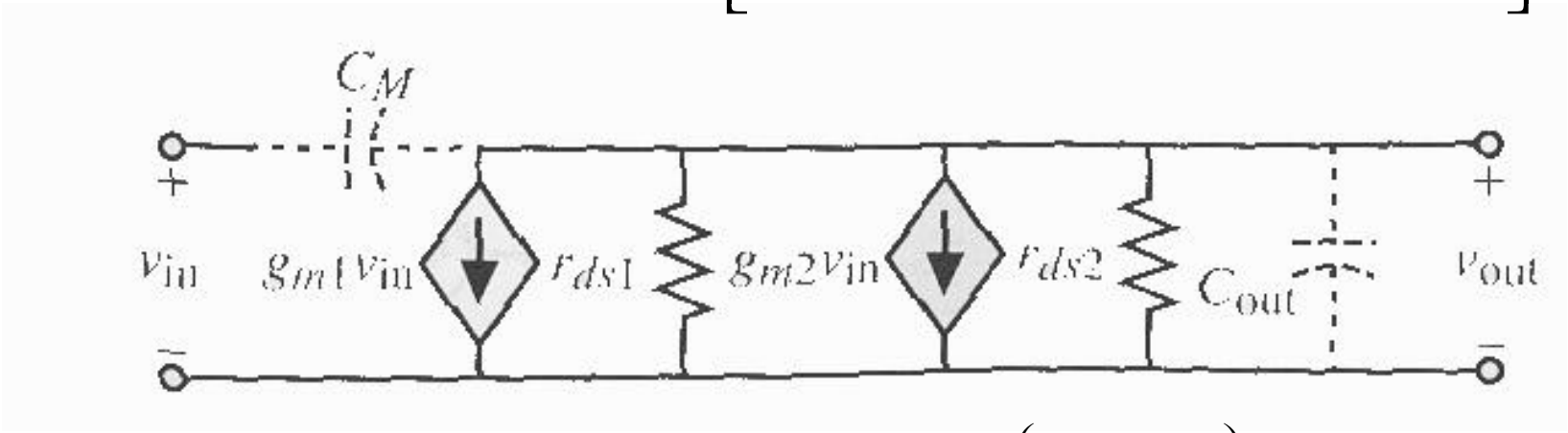
Push-Pull inverter: small-signal gain

$$\frac{v_{out}}{v_{in}} = \frac{-(g_{m1}+g_{m2})}{g_{ds1}+g_{ds2}} = -\sqrt{2/I_D}\left[\frac{\sqrt{K'_N(W_1/L_1)}+\sqrt{K'_P(W_2/L_2)}}{l_1+l_2}\right]$$



$$R_{OUT} = \frac{1}{g_{ds1}+g_{ds2}}$$

$$p_1 = \frac{-1}{R_{OUT}(C_{out}+C_M)} = -\left(\frac{g_{ds1}+g_{ds2}}{C_{out}+C_M}\right)$$

$$z_1 = \frac{g_{m1}+g_{m2}}{C_M} = \frac{g_{m1}+g_{m2}}{C_{gd1}+C_{gd2}}$$