MODIFICATIONS TO DIFFERENTIAL AMPLIFIERS

(READING: Text-Sec. 4.3.5)

INTRODUCTION

The objective of this presentation is:

1.) Show how to improve the performance of differential amplifiers

2.) Demonstrate the design of a MOSFET differential amplifier

Outline

- Folded load MOS differential amplifiers
- Modifications of active load amplifiers
  - Hyperbolic sine
  - Linear transconductor
  - Cross-coupled differential amplifier
- Design of a differential amplifier
- Summary

FOLDED MOS DIFFERENTIAL AMPLIFIER WITH A CURRENT MIRROR LOAD

Folding Concept

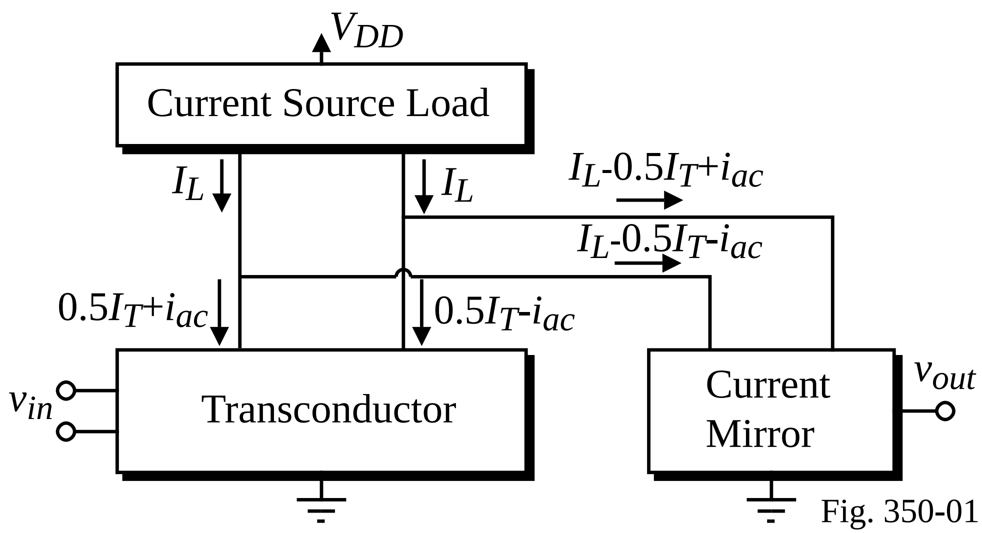


Fig. 350-01

Advantages:

- Increases the upper common-mode voltage range
- Allows balanced loads
- Smaller power supplies

Disadvantage:

- Introduces more poles (generally not dominant)
- I_L must be greater than I_T+i_{ac} to prevent the current mirror from being "starved" → Also implies more power dissipation

Folded MOS Differential Amplifier

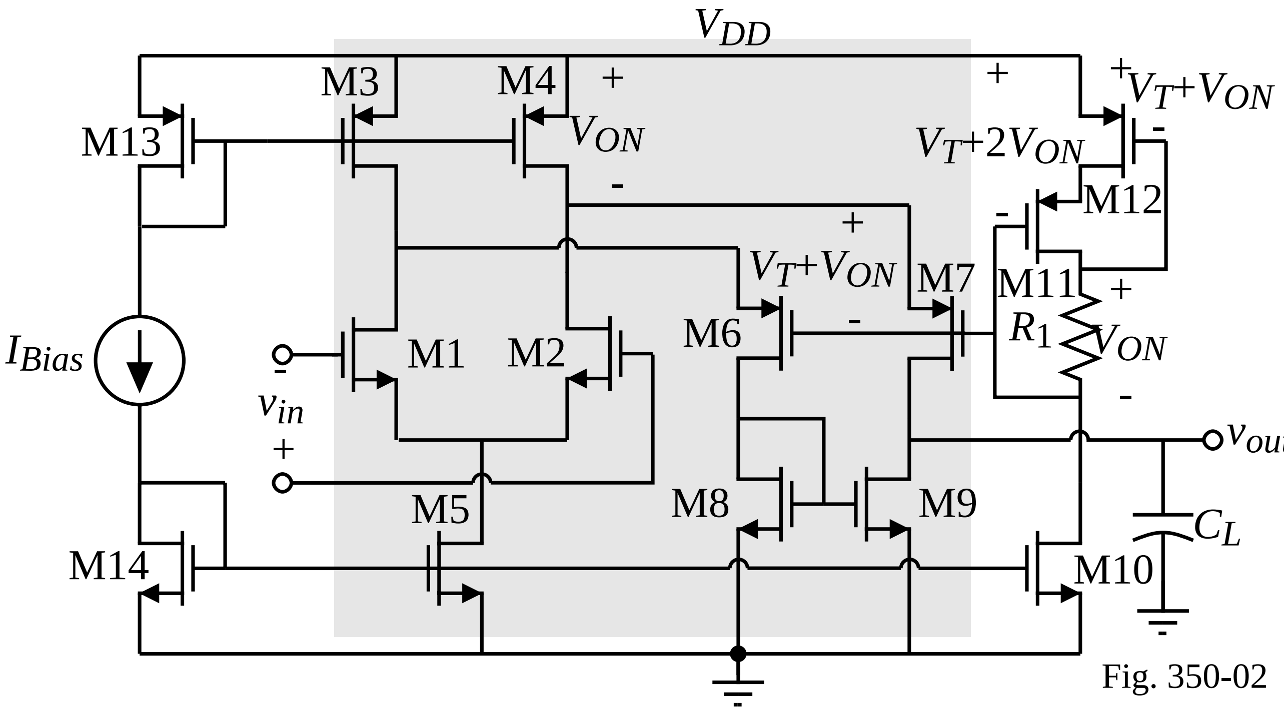


Fig. 350-02

Observations:

- Maximum input common-mode range is $V_{SS} + 2V_{ON} + V_T < V_{CM} < V_{DD}\text{-}V_{ON}\text{+}V_T$
- Voltages at the drains of M1 and M2 are identical, which reduces systematic offsets (Early voltage/channel-length modulation effects)
- Only high impedance point is at the output, which creates a dominant pole with C_L

Small Signal Analysis

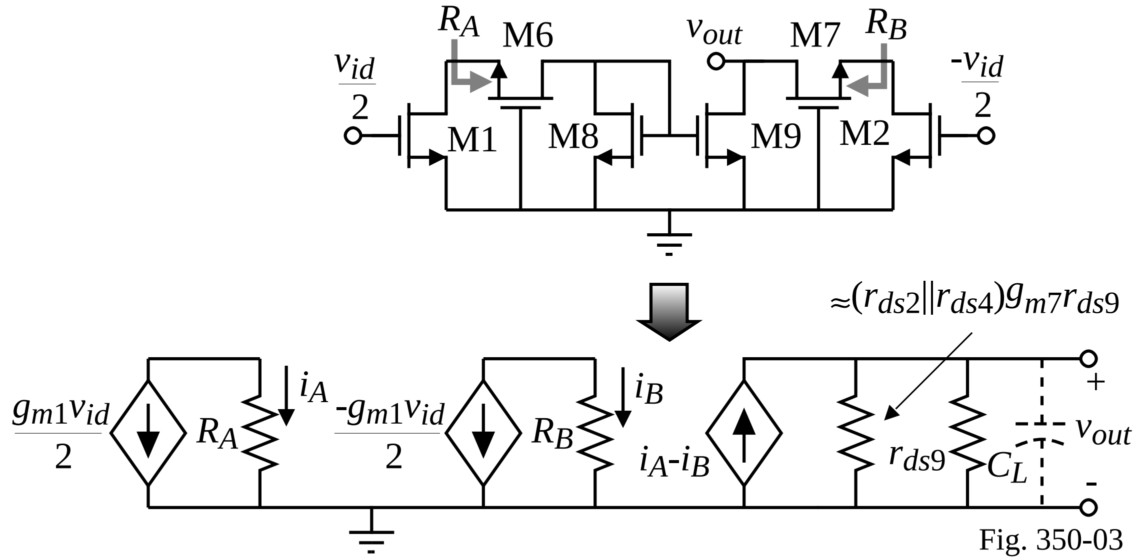


Fig. 350-03

Recall: $R_A \approx 1/g_{m6}$ & $R_B \approx 1/g_{m7}$ & $r_{out7} \approx \{r_{ds7}(1+g_{m7}[r_{ds2}//r_{ds4}]) + r_{ds2}//r_{ds4}\}//r_{ds9}$

And $v_{out} = -(i_2 + i_9)(r_{ds9}//r_{out7}) \approx -(i_2 + i_9)(r_{ds9})$

Where $i_2 \approx (-0.5v_{id}g_{m2}/g_{m7})g_{m7} = -0.5v_{id}g_{m2}$

& $I_9 \approx (0.5v_{id}[-g_{m1}]/g_{m6})(g_{m6}/g_{m8})g_{m9} = -0.5v_{id}g_{m1}$ if $g_{m8} = g_{m9}$ (design choice!)

$$\therefore \quad v_{out} = \left(\frac{g_{m1}+g_{m2}}{2}\right) r_{ds9}\, v_{id} \approx g_{m1} r_{ds9}\, v_{id} \Rightarrow \frac{v_{out}}{v_{id}} = g_{m1} r_{ds9}$$

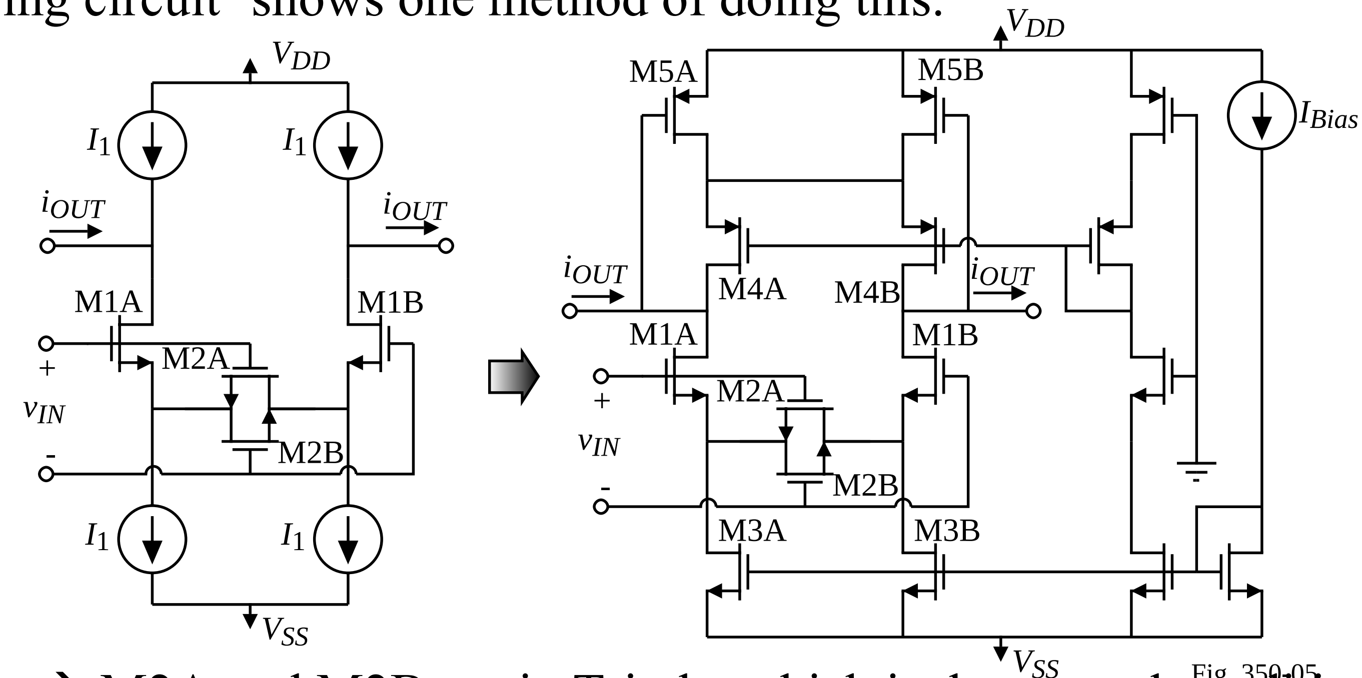
-3dB frequency: $$\omega_{\text{-3dB}} = \frac{1}{r_{ds9}C_L}$$

MODIFICATIONS OF ACTIVE LOAD AMPLIFIERS

Linear CMOS Transconductor

In many applications, it is necessary to linearize the transconductance of a differential amplifier. The following circuit† shows one method of doing this.

Goal: Desensitize g_m of square-law depend. & sensitize to a more linear element!



$v_{GS\_1A} = v_{GS\_2A}$

$v_{GS\_1B} = v_{GS\_2B}$

$v_{CM} - V_{GS\_1A} = V_{S\_A}$

if balanced, $V_{S\_A} = V_{S\_B}$ → M2A and M2B are in Triode, which is the normal condition.

The small signal drain-source resistance of M2A and M2B is

$$r_{2A} = r_{2B} \approx \frac{1}{\beta_2(V_{GS1}-V_{TN})} \quad \rightarrow \quad i_D = \beta[(v_{GS}-V_T)v_{DS}-v_{DS}^2] \approx \beta(v_{GS}-V_T)v_{DS}$$

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† F. Krummenacher and N. Joehl, "A 4-MHz CMOS Continuous-Time Filter with On-Chip Automatic Tuning," *IEEE J. of Solid-State Circuits*, vol. 23, no. 3, pp. 750-758, June 1988.

Linear CMOS Transconductor - Continued

The small signal transconductance of M1A and M1B are

$$g_{m1} = g_{m1A} = g_{m1B} = \beta_1(V_{GS1}-V_{TN})$$

Using the half-circuit approach for differential operation, the small signal output current is derived as, where $r_{2a}//r_{2b} = 0.5r_{2a}$,

$$i_{out} = g_{m1}v_{gs1} = g_{m1}(0.5v_{id} - 0.5r_{2a}i_{out}) \rightarrow i_{out} = \frac{0.5g_{m1}v_{id}}{1+0.5g_{m1}r_{2a}}$$

$$\rightarrow g_m(\text{eff}) = \frac{0.5g_{m1}}{1+0.5g_{m1}r_{2a}}$$

→ Intuitively, g_m(eff) is now more dependent on a more linear element (r_{2a}) and less sensitive to the less linear component (g_{m1}).

- Substituting the value of g_{m1} and r_{2a} gives

$$g_m(\text{eff}) = \frac{0.5\beta_1(V_{GS1}-V_{TN})}{1+\dfrac{0.5\beta_1(V_{GS1}-V_{TN})}{\beta_2(V_{GS2}-V_{TN})}} = \frac{\beta_1\beta_2\,(V_{GS1}-V_{TN})}{\beta_1+2\beta_2} = \frac{\beta_1\beta_2}{\beta_1+2\beta_2}\sqrt{\frac{2I_1}{\beta_1}}$$

Select the ratio of β_1/β_2 to linearize the transconductance.

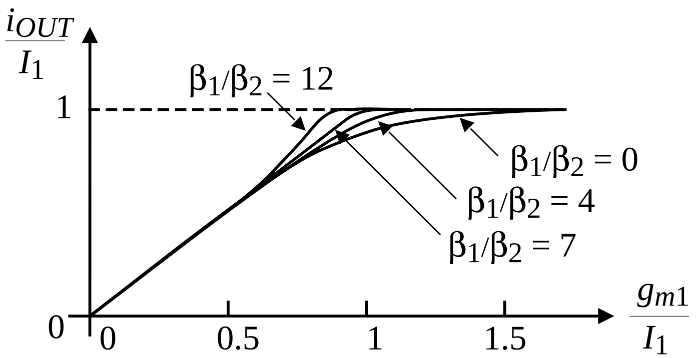

Fig. 350-06

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Cross-Coupled Differential Amplifier

This input stage is good for class B operation (push/pull).

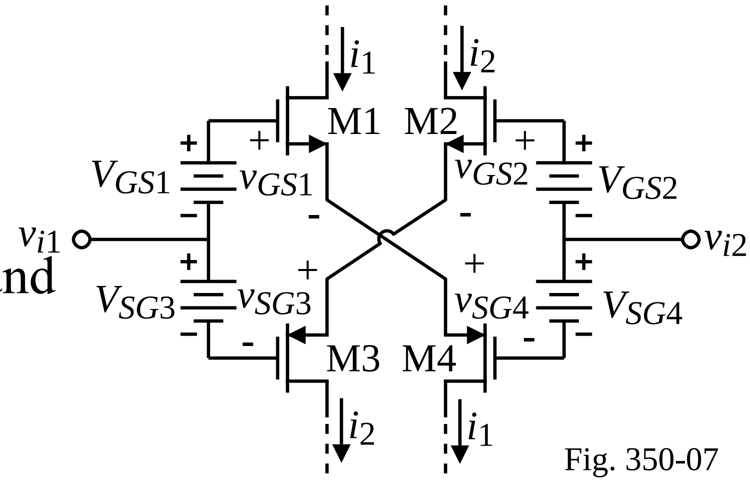

Fig. 350-07

Push/pull Operation:

* If v_{id}, which is $v_1 - v_2$, increases,

M1 & M4 conduct more current and M2/M3 less.

* If v_{id} decreases, M2 & M3 conduct more current and M1/M4 less.

AC Operation:

Using the notation for ac, dc, and total variables yields

$$v_{i1} - v_{i2} = -V_{GS1} + v_{GS1} + v_{SG4} - V_{SG4} = V_{SG3} - v_{SG3} - v_{GS2} + V_{GS2}$$

& canceling DC components: $v_{i1} - v_{i2} = v_{id} = (v_{gs1} + v_{sg4}) = -(v_{sg3} + v_{gs2})$

$$\{\text{e.g., } -V_{GS1} + v_{GS1} = v_{gs1}\}$$

if $v_{i1} = v_{id}$ & $v_{i2} = 0$,

$$i_1 = v_{gs}g_{m1} = (v_{id} - i_1/g_{m4})\, g_{m1} \quad \text{or} \quad i_1 = 0.5 g_{m1} v_{id} \quad \text{(if M1=M4)}$$

Cross-Coupled Differential Amplifier - Continued

If M1=M2=M3=M4, half of the differential input is applied across each side.

$$\therefore \quad i_1 = \frac{g_{m1}v_{id}}{2} = \frac{g_{m4}v_{id}}{2} \quad \text{and} \quad i_2 = -\frac{g_{m2}v_{id}}{2} = -\frac{g_{m3}v_{id}}{2}$$

Implementation:

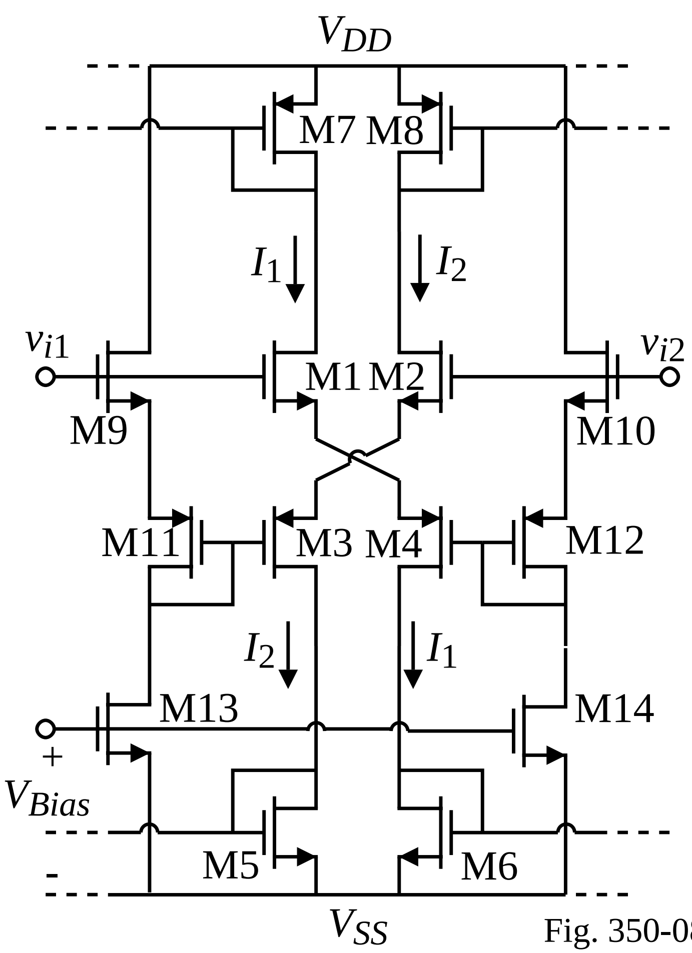

Fig. 350-08

Gain is reduced by a half because the input signal is dropped across two gate-sources.

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DESIGN OF A DIFFERENTIAL AMPLIFIER

CMOS Differential Amplifier with a Current Mirror Load

Design Considerations:

Constraints	Specifications
Power supply Technology Temperature Power Dissipation Area …	Small-signal gain (accuracy – 1+Aβ) Frequency response (C_L) ICMR Slew rate (C_L) Power dissipation OCMR Offsets …

Architecture:

- Input characteristics (R_{in}, ICMR)
- Output charact. (R_{out}, OCMR)
- Type of input
- Type of load
- Type of mirrors
- Output driver
- Type of feedback
- Number of stages
- …

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DESIGN OF A DIFFERENTIAL AMPLIFIER

CMOS Differential Amplifier with a Current Mirror Load

Sample Design:

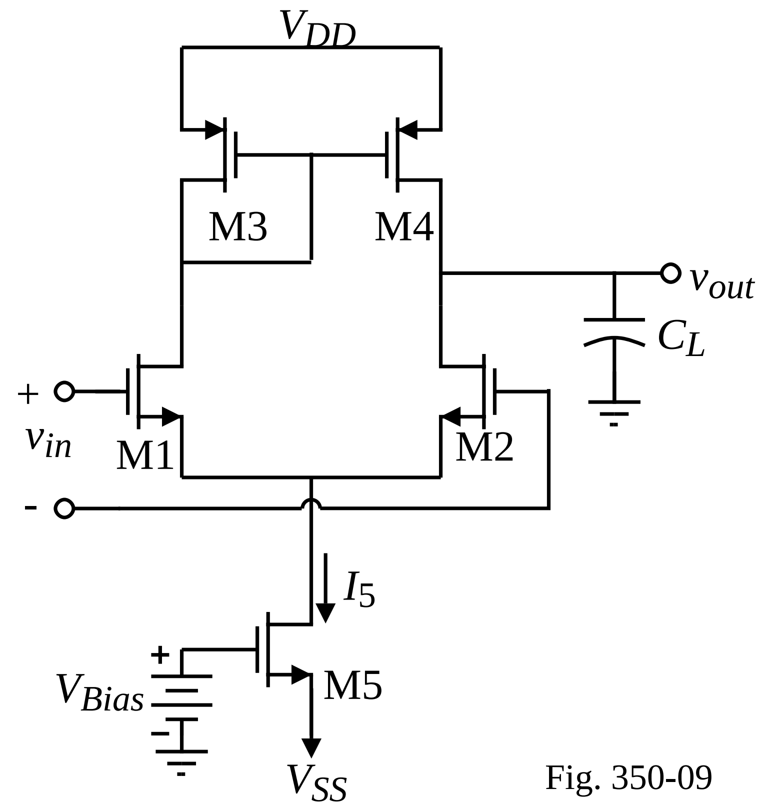

Fig. 350-09

Relationships

$A_v = g_{m1} R_{out}$

$\omega_{\text{-3dB}} = 1/R_{out}C_L$

$V_{IC}(\text{max}) = V_{DD} - V_{SG3} + V_{TN1}$

$V_{IC}(\text{min}) = V_{DS5}(\text{sat}) + V_{GS1} = V_{DS5}(\text{sat}) + V_{GS2}$

$SR = I_{SS}/C_L$ (dV_{out}/dt)

$P_{diss} = V_{DD}$ x (All dc currents flowing from V_{DD})

$+ |V_{SS}|$ x (All dc currents flowing to V_{SS})

Design of a CMOS Differential Amplifier with a Current Mirror Load - Continued

Sample procedure for a simple 5-transistor CMOS differential amplifier:

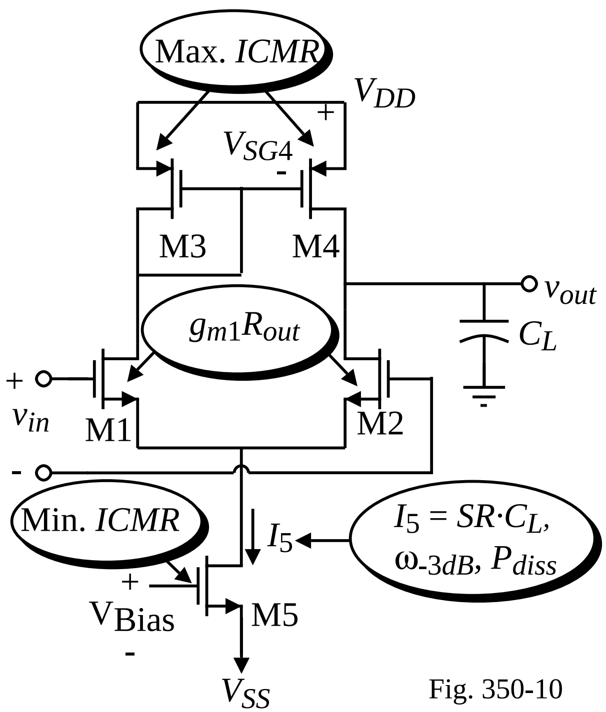

Fig. 350-10

1.) Pick I_{SS} to satisfy the slew rate, knowing C_L or the power dissipation.

2.) Check to see if R_{out} will satisfy the frequency response. If not, change I_{SS} or modify circuit.

3.) Design W_3/L_3 (W_4/L_4) to satisfy the upper *ICMR*.

4.) Design W_1/L_1 (W_2/L_2) to satisfy the gain.

5.) Design W_5/L_5 to satisfy the lower *ICMR*.

6.) Check functionality of the circuit

7.) Check all specifications

8.) Iterate where necessary.

Example 1 - Design of a MOS Differential Amplifier with a Current Mirror Load

Design the currents and *W/L* values of the MOS differential amplifier using a current mirror load to satisfy the following specifications: $V_{DD} = -V_{SS} = 2.5\text{V}$, $SR \geq 10\text{V}/\mu\text{s}$ with a 5pF load, $f_{-3\text{dB}} \geq 100\text{kHz}$ with a 5pf load, a small signal gain of 100V/V, $1.5\text{V} \leq ICMR \leq 2\text{V}$, and power loss must be less than 1mW. Assume $K_N' = 110\mu\text{A/V}^2$, $K_P' = 50\mu\text{A/V}^2$, $V_{TN} = 0.7\text{V}$, $V_{TP} = -0.7\text{V}$, $\lambda_N = 0.04\text{V}^{-1}$, and $\lambda_P = 0.05\text{V}^{-1}$.

Solution

1.) To meet the slew rate, $I_{SS} \geq 50\mu\text{A}$. For maximum P_{diss}, $I_{SS} \leq 200\mu\text{A}$.

2.) $f_{-3\text{dB}}$ of 100kHz $\Rightarrow R_{out} \leq 318\text{k}\Omega$. This gives $R_{out} = \dfrac{2}{(\lambda_N + \lambda_P)I_{SS}} \leq 318\text{k}\Omega$

$\therefore\ I_{SS} \geq 70\mu\text{A}$ Thus, pick $I_{SS} = 100\mu\text{A}$

3.) $V_{IC}(\text{max}) = V_{DD} - V_{SG3} + V_{TN1} \rightarrow 2\text{V} = 2.5 - V_{SG3} + 0.7$

$$\therefore\quad V_{SG3} \leq 1.2\text{V} = \sqrt{\frac{2\cdot 50\mu\text{A}}{50\mu\text{A/V}^2(W_3/L_3)}} + 0.7 \quad \rightarrow \quad \frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{2}{(0.5)^2} \geq 8$$

Maybe choose 10 for simplicity!

Example 1 - Continued

4.) $$100\text{V/V} = g_{m1}R_{out} = \frac{g_{m1}}{g_{ds2}+g_{ds4}} = \frac{\sqrt{2\cdot 110\mu\text{A/V}^2(W_1/L_1)}}{(0.04+0.05)\sqrt{50\mu\text{A}}} = 23.31\sqrt{\frac{W_1}{L_1}}$$

$$\therefore \quad \frac{W_1}{L_1} = \frac{W_2}{L_2} = 18.4$$

5.) $V_{IC}(\text{min}) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1}$

$$-1.5 = -2.5 + V_{DS5}(\text{sat}) + \sqrt{\frac{2\cdot 50\mu\text{A}}{110\mu\text{A/V}^2(18.4)}} + 0.7$$

$V_{DS5}(\text{sat}) \leq 0.3 - 0.222 = 0.078$!! (Subthreshold!)

$$\Rightarrow \quad \frac{W_5}{L_5} = \sqrt{\frac{2I_{SS}}{K_N' V_{DS5}(\text{sat})^2}} = 300$$

6.) Increase W_1/L_1 to reduce V_{GS1} and allow a smaller W_5/L_5. If $W_1/L_1 = 40$, then $W_5/L_5 = 9$ or 10. (Larger than specified gain should be okay.)

SUMMARY

- Active load amplifier consists of a transconductor and a load

  There are a large number of combinations of loads and transconductors possible. We have not considered the many cascoded possibilities and other configurations.
- The BJT amplifier generally has more gain and wider signal swing than the MOS amplifier
- The voltage gain of the MOS transconductor with a current source or current mirror load is inversely proportional to the square root of the bias current.
- The current mirror load differential amplifier is a widely used input stage
- The frequency response is generally determined by the dominant pole which is found at points in the circuit that are high impedance to ac ground and large capacitance
- The active load amplifier is the primary gain stage in operational amplifiers and other applications and will be a fundamental building block in more complex circuits
- Performances not considered include slew rate and noise