MOSFET DIFFERENTIAL AMPLIFIERS

(READING: Text-Sec. 3.5)

INTRODUCTION

Objective

The objective of this presentation is:

1.) Define and characterize the MOSFET differential amplifier

2.) Show the large-signal and small-signal performance

3.) Show alternate implementations of the differential amplifier

Outline

- Large-signal transconductance
- Large-signal voltage transfer
- Small-signal performance
- Other characteristics of the differential amplifier
- Summary

LARGE-SIGNAL TRANSCONDUCTANCE

Transconductance Performance of the Differential Amplifier

Consider the following n-channel differential amplifier (sometimes called a source-coupled pair):

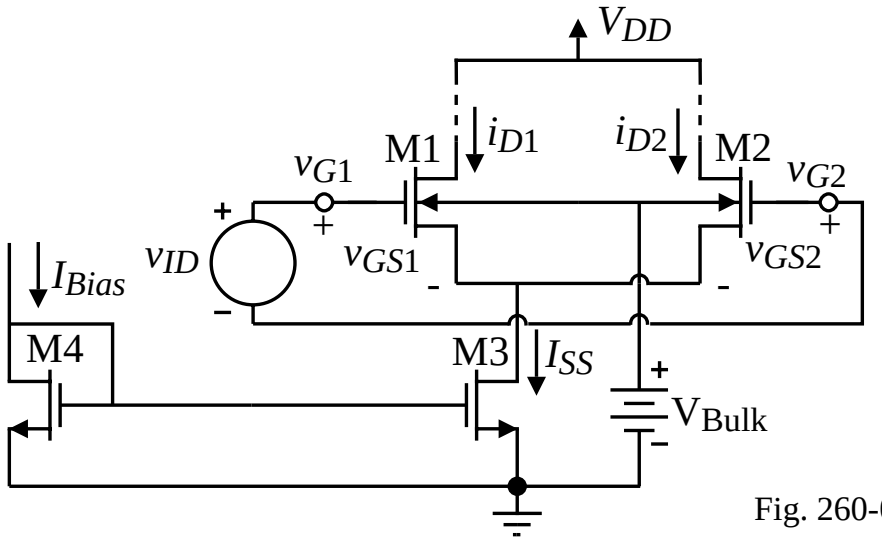


Fig. 260-01

Where should the bulk be connected? Consider a p-well, CMOS technology,

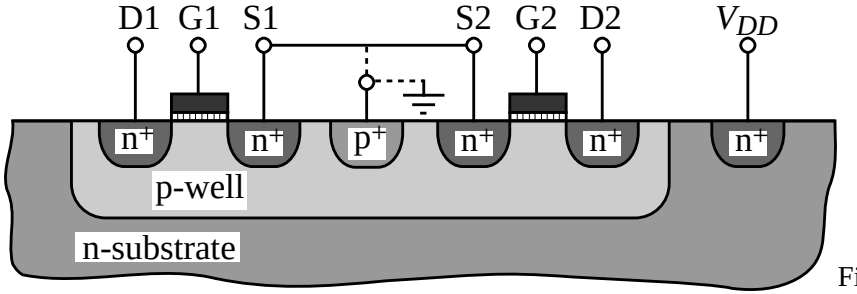


Fig. 260-02

1.) Bulks connected to the well: No modulation of V_T but large common mode parasitic capacitance to substrate → sensitive to substrate noise injection (PSRR Performance is degraded).

2.) Bulks connected to ground: Smaller common-mode parasitic capacitors, but modulation of V_T.

If the technology is n-well CMOS, the bulks must be connected to ground.

Transconductance Performance of the Differential Amplifier - Continued

Defining equations (Assume that the MOSFETs are in saturation):

$$v_{ID} = v_{GS1} - v_{GS2} = \left(\frac{2i_{D1}}{\beta}\right)^{1/2} - \left(\frac{2i_{D2}}{\beta}\right)^{1/2} \qquad \text{and} \qquad I_{SS} = i_{D1} + i_{D2}$$

Solution:

$$i_{D1} = \frac{I_{SS}}{2} + \frac{I_{SS}}{2}\left(\frac{\beta v_{ID}^2}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I_{SS}^2}\right)^{1/2} \quad \& \quad i_{D2} = \frac{I_{SS}}{2} - \frac{I_{SS}}{2}\left(\frac{\beta v_{ID}^2}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I_{SS}^2}\right)^{1/2}$$

which are valid for $v_{ID} < (2I_{SS}/\beta)^{1/2}$.

Illustration of the result:

If $v_{id} >>$, $\therefore v_{gs1} >> v_{gs2}$, $i_{D1} = I_{SS}$, $i_{D2} = 0$

If $v_{id} <<$, $\therefore v_{gs1} << v_{gs2}$, $i_{D1} = 0$, $i_{D2} = I_{SS}$

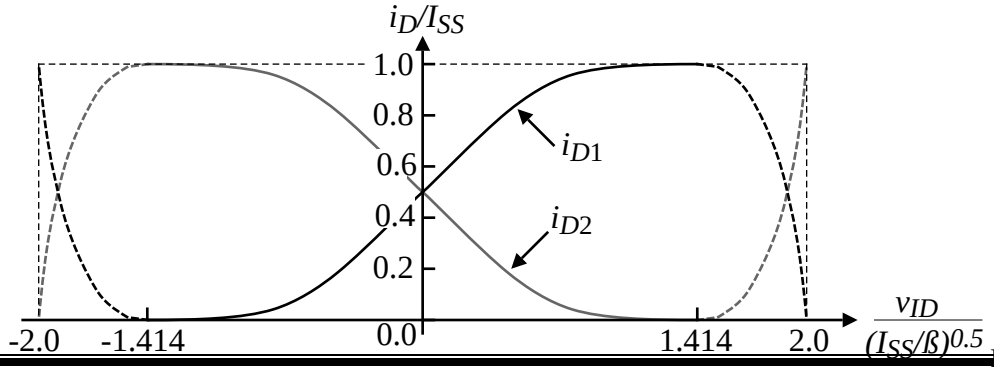


Fig 260-03

Differentiating i_{D1} (or i_{D2}) with respect to v_{ID} and setting V_{ID} =0V gives

$$g_m = di_{D1}/dv_{ID}(V_{ID} = 0) = (\beta I_{SS}/4)^{1/2} = \left(\frac{K'_1 I_{SS} W_1}{4L_1}\right)^{1/2}$$ (half the g_m of an inverting amplifier)

LARGE-SIGNAL VOLTAGE CHARACTERISTICS

Voltage Transfer Characteristic of the Differential Amplifier

MOS differential amplifier with resistor loads and MOSFETs in the saturation region. The differential output voltage is:

$$v_{OD} = V_{DD} - i_{D1}R_D - V_{DD} + i_{D2}R_D$$

$$= R_D(i_{D2}-i_{D1}) = R_D\left(I_{SS}\sqrt{\frac{\beta v_{ID}^2}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I_{SS}^2}}\right)$$

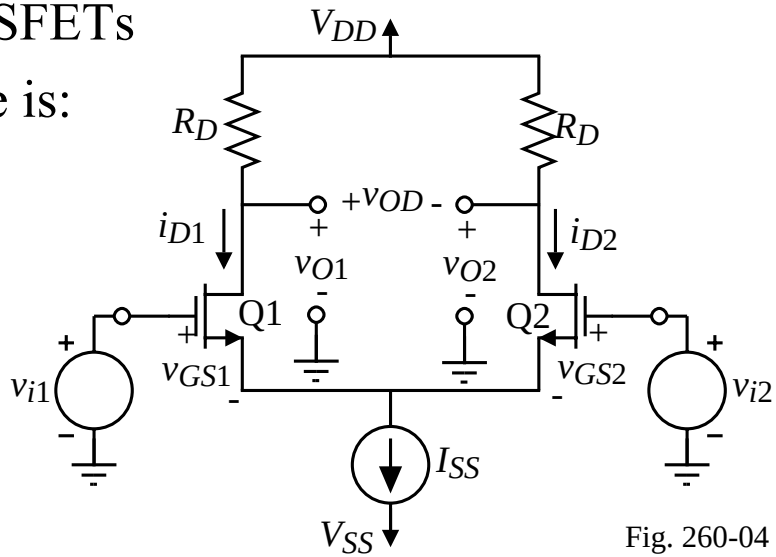


Fig. 260-04

Illustration of this relationship:

Note that typical values of $\sqrt{\frac{\beta}{I_{SS}}}$ range from 2-4V, which means that the linear range of MOS differential amplifiers is ±2-4V compared to ±0.1V for BJT diff. amps.

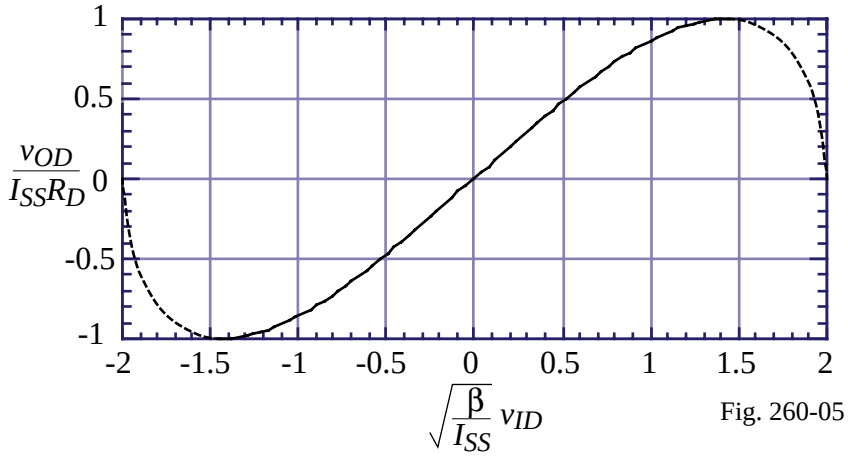


Fig. 260-05

Source Degeneration of the MOS Differential Amplifier

Increases the range over which the source-couple pair behaves as a linear amplifier by essentially decreasing the overall gain/transconductance (decreasing the slope).

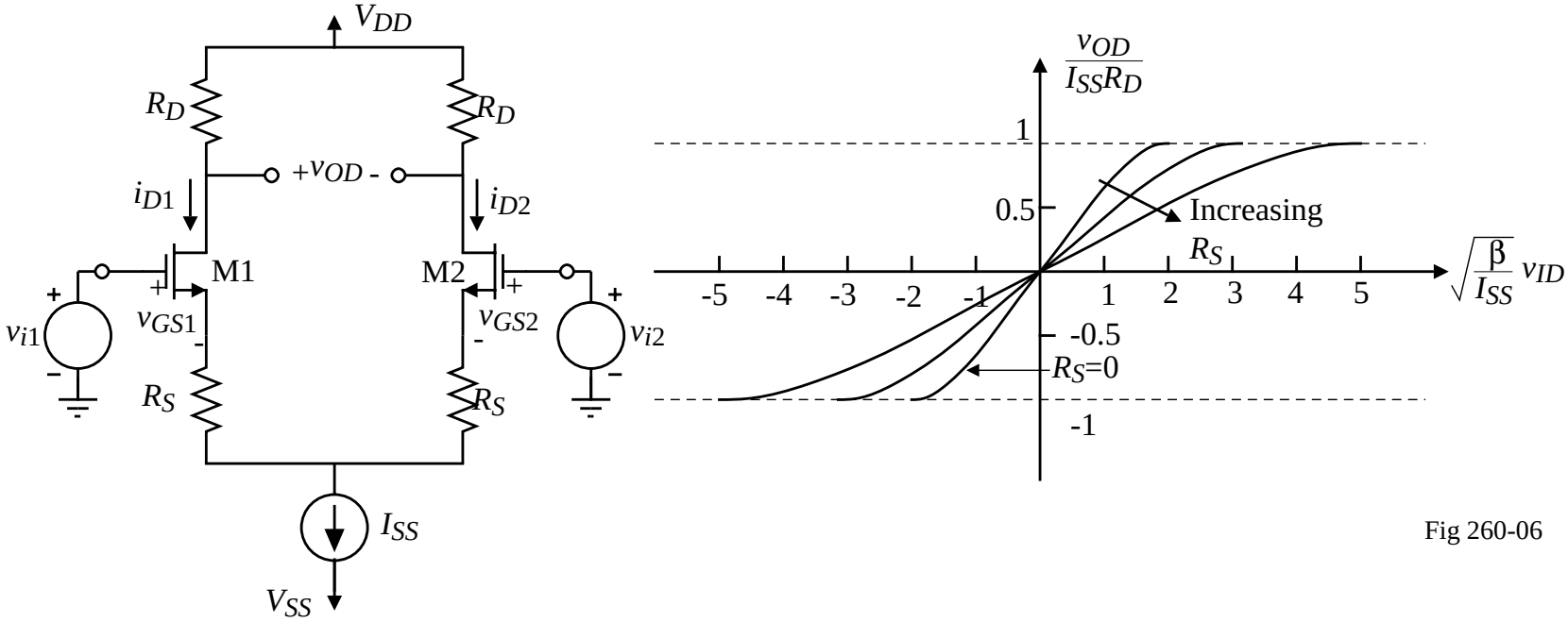


Fig 260-06

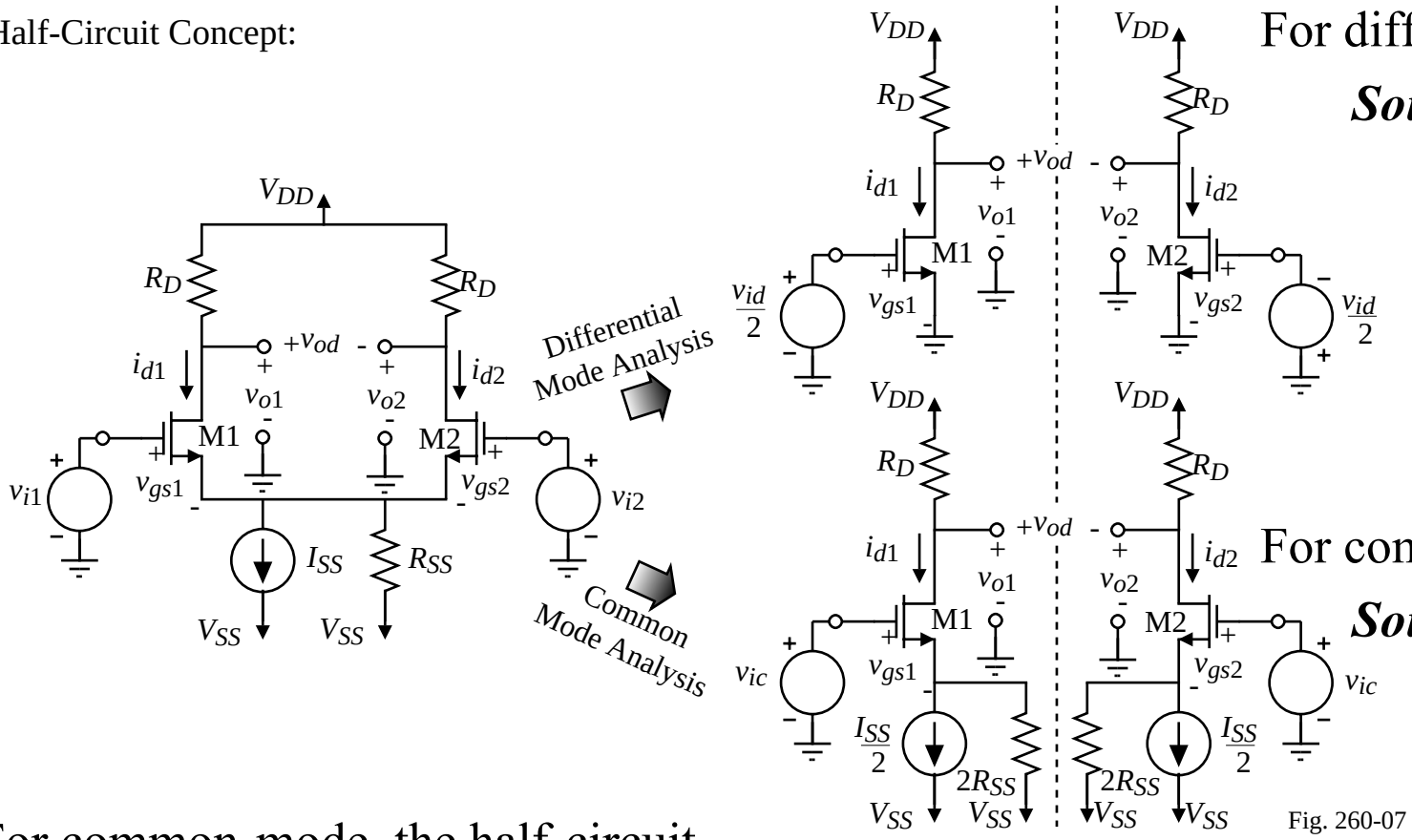
Because of the increased linear range of MOSFET differential amplifiers, source degeneration is not as useful as for BJT differential amplifiers because gain is lost, thereby making the linearity-gain tradeoff less attractive (gain is typically already lower with MOSFETs than with their BJT counterparts → smaller values of g_m).

SMALL-SIGNAL PERFORMANCE

Differential- and Common-mode Small-Signal Performance

The small-signal performance of a differential amplifier can be separated into a differential- and common-mode analysis. This separation allows us to take advantage of the following simplifications.

Half-Circuit Concept:



For differential analysis:

Source = ac gnd!

For common-mode:

Source-degenerated CS amplifier!

Fig. 260-07

For common-mode, the half-circuit concept is only valid if the resistance looking into each source is equal.

Small-Signal, Differential-Mode Performance of the MOS Differential Amplifier

Circuit and small-signal model:

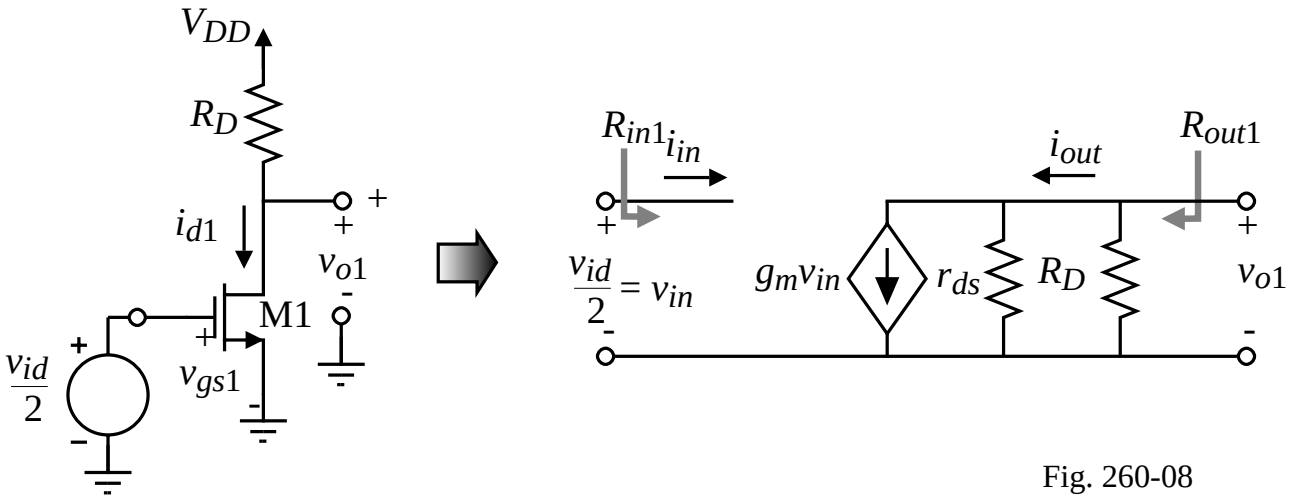


Fig. 260-08

Half-circuit performance:

$$R_{in1} = \infty,\ R_{out1} \approx R_D,\ \text{and}\ \frac{v_{o1}}{v_{id}} = \frac{-g_{m1}R_D}{2}$$

Differential performance: $R_{id} = \infty\ ,\ R_{od} = R_{out1} + R_{out2}$

$$\rightarrow R_{od} = v_t/i_t = (v_{o1} - v_{o2})/i_t = [(g_m v_{id}/2)R_{o1} + (g_m v_{id}/2)R_{o2}]/(g_m v_{id}/2) = R_{o1} + R_{o2}$$

and

$$\frac{v_{od}}{v_{id}} = \frac{v_{o1}}{v_{id}} - \frac{v_{o2}}{v_{id}} = \frac{-g_{m1}R_D}{2} - \frac{+g_{m2}R_D}{2} = -g_{m1}R_D$$

where $g_{m1} = g_{m2}$.

Small-Signal, Common-Mode Performance of the MOS Differential Amplifier

Circuit and small-signal model:

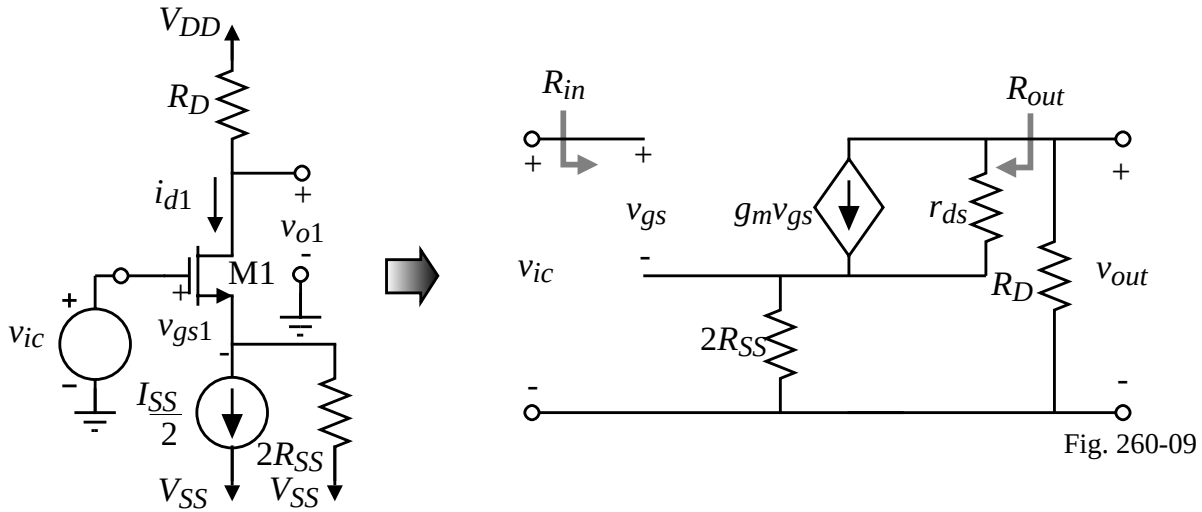


Fig. 260-09

Half-circuit performance:

$$R_{in1} = \infty, \qquad R_{out} = r_{ds}[1 + (g_m + g_{mbs})2R_{SS}] + 2R_{SS}, \qquad \text{and}$$

$$\frac{v_{o1}}{v_{o2}} \approx \frac{-g_m R_D}{1 + g_m 2R_{SS}}$$

Common-mode performance:

$$R_{ic} = \infty, \; R_{oc} = (r_{ds}[1 + (g_m + g_{mbs})2R_{SS}] + 2R_{SS}) || R_D, \; \& \; \frac{v_{oc}}{v_{ic}} \approx \frac{-g_m R_D}{1 + g_m 2R_{SS}},$$

where $g_{m1} = g_{m2}$ and $r_{ds1} = r_{ds2}$.

Common-Mode Rejection Ratio (CMRR)

The common-mode rejection ratio is a measure of the differential amplifier's ability to reject the common-mode signal and amplify the differential-mode signal.

$$\text{CMRR} = \left|\frac{A_{dm}}{A_{cm}}\right| = \left|\frac{v_{o1}/v_{id}}{v_{o1}/v_{ic}}\right| \approx \frac{\dfrac{-g_m R_D}{2}}{\dfrac{-g_m R_D}{1+g_m 2R_{SS}}} \approx g_m R_{SS}$$

Thus, the larger the input transconductance or R_{SS}, the larger the common-mode rejection ratio.

OTHER CHARACTERISTICS OF THE DIFFERENTIAL AMPLIFIER

Input Common-Mode Voltage Range

The input common-mode voltage range (ICMR) is the range of common-mode input voltages over which the differential amplifier amplifies the differential signal without significant change.

Consider the following:

$$I_{DD} \equiv I_{SS}$$

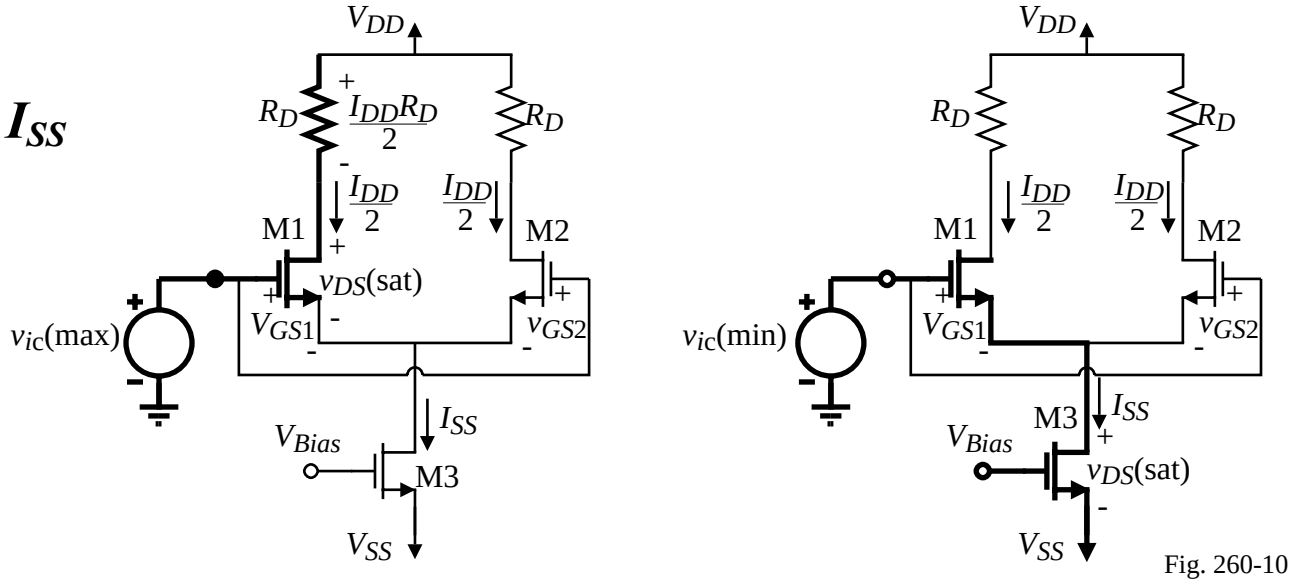


Fig. 260-10

Maximum ICMR Voltage:

$$v_{ic}(\max) = V_{DD} - 0.5 I_{SS} R_D - v_{DS1}(\text{sat}) + V_{GS1}$$

$$= V_{DD} - 0.5 I_{SS} R_D + V_{T1}$$

Minimum ICMR Voltage:

$$v_{ic}(\min) = V_{SS} + v_{DS3}(\text{sat}) + V_{GS1}$$

$$= V_{SS} + v_{DS3}(\text{sat}) + v_{DS1}(\text{sat}) + V_{T1}$$

Slew Rate of the MOSFET Differential Amplifier

Slew rate is a voltage rate because current available to charge a capacitor is constant.

$$\text{Slew rate} = \text{SR} = \frac{dv_C}{dt} = \frac{i_C}{C}$$

where i_C and v_C are the current through and voltage across a capacitor C.

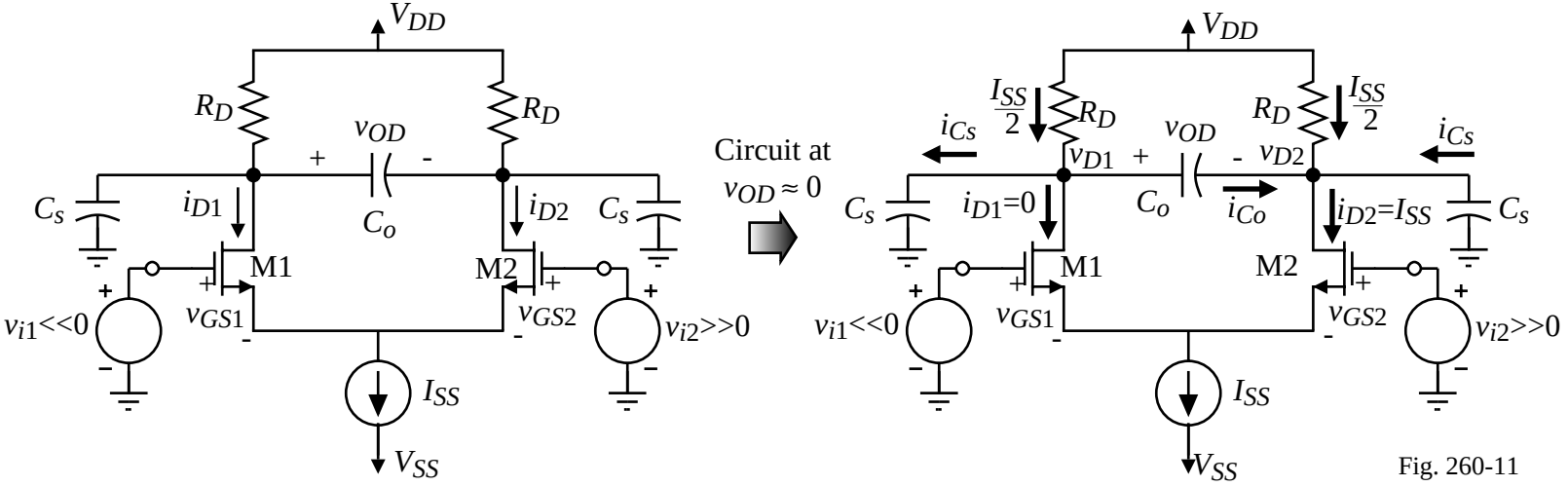


Fig. 260-11

Note that the current in M1 is 0 and M2 is I_{SS}. The slew rate can be found from,

$$0.5I_{SS} = C_s\frac{dv_{D1}}{dt} + C_o\frac{d}{dt}(v_{D1} - v_{D2}) \quad \& \quad 0.5I_{SS} = -C_s\frac{dv_{D2}}{dt} + C_o\frac{d}{dt}(v_{D1} - v_{D2})$$

Thus, summing the two relations, $I_{SS} = 2C_o\frac{d}{dt}(v_{D1}-v_{D2}) + C_s\frac{d}{dt}(v_{D1}-v_{D2})$

$$= (2C_o+C_s)\frac{d}{dt}(v_{D1}-v_{D2}) \Rightarrow \boxed{SR = \frac{I_{SS}}{2C_o+C_s} = \frac{0.5I_{SS}}{C_o+0.5C_s}}$$

SUMMARY

- Differential amplifier amplifies the difference signal between two voltages and rejects the common mode signal
- The transconductance characteristics of the MOS differential amplifier switches from all of the current in one side to the other side within ±2-4V
- Source degeneration increases the range over which the differential amplifier behaves as a linear amplifier
- The half circuit concept is very useful for analyzing the small-signal differential and common mode performance
- The maximum and minimum input common mode range is:

$$v_{ic}(\text{max}) = V_{DD} - 0.5 I_{SS} R_D + V_{T1}$$

$$v_{ic}(\text{min}) = V_{SS} + v_{DS3}(\text{sat}) + V_{GS1}$$

- The differential amplifier has a slew rate limit of I_{SS}/C_{eq} where C_{eq} is the equivalent capacitance seen from either of the drains to ground.