Tolga Dinç 10.11.2008
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# EL303
# ANALOG INTEGRATED CIRCUITS LAB #2
## Folded Cascode Design

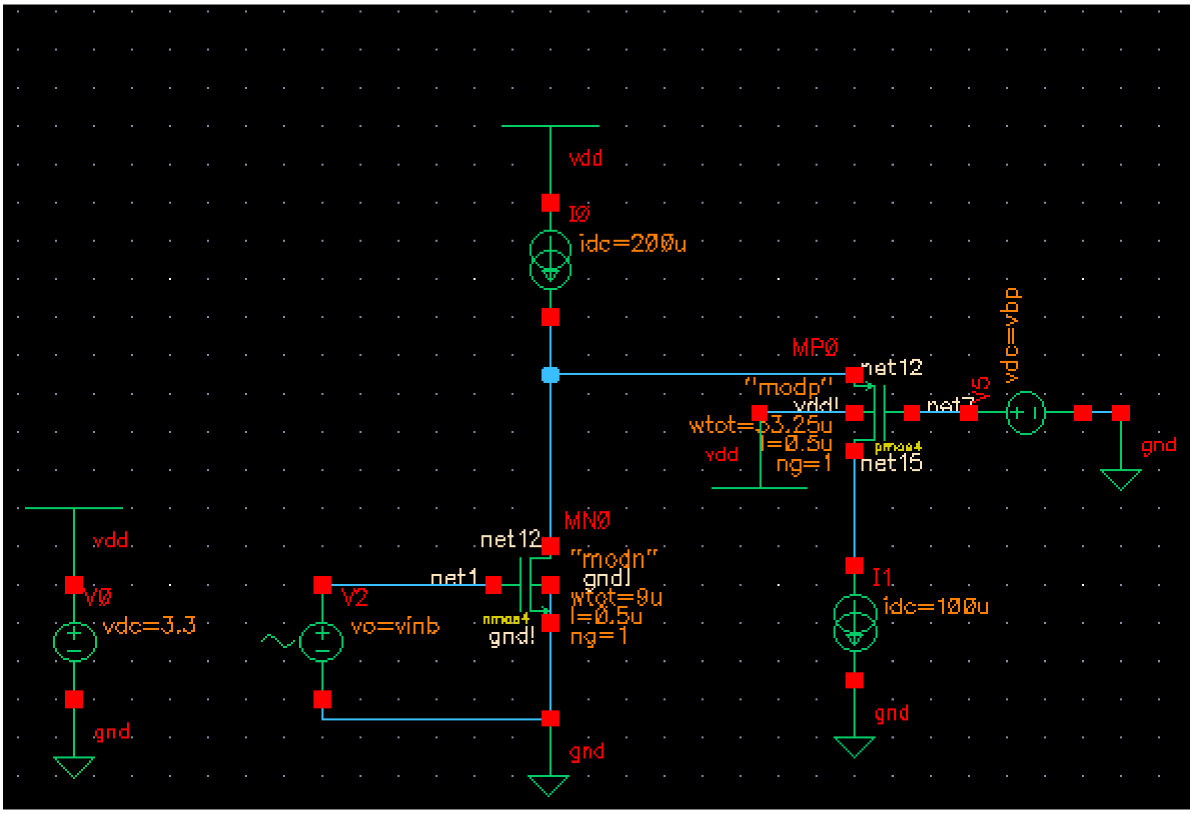

Figure 1.1: The Basic Shematic of Folded Cascode

In this assignment we are supposed to design a folded cascode, basicly as shown in Fig.1.1, and possess following specifications:

**Gain**: around 70dB, **Output Impedance**: at least 2M ohm, **Unit Gain Freq**: 10MHz

The idea behind designing a folded cascode amplifier is to transform input voltage to a current and apply this current to common gate configuration. Therefore cascode structure combine large transconductance of CS amplifier and favorable frequency response of common gate stage. Thus, this configuration may offer higher gain, higher bandwith and high input impedance.

As seen in Fig.1.1 we need additional constant current sources (I0=200uA and I1=100uA) in order to bias nmos and pmos circuits with 100uA currents. Also I1 behaves like an active load that is connected to drain of pmos common gate structure and output is taken on this active load. We need to implement these constant current sources by using current mirror configurations.

Designing process of Folded Cascode Amplifier can be divided into 2 stages:

1) Designing constant current sources and determining I-V characteristic of current mirrors.
2) Replacing constant currents sources in Fig.1.1 with current mirrors designed in first stage

and arranging operating points of transistors by changing aspect ratios (W/L) so that all mosfets operates in saturation region.

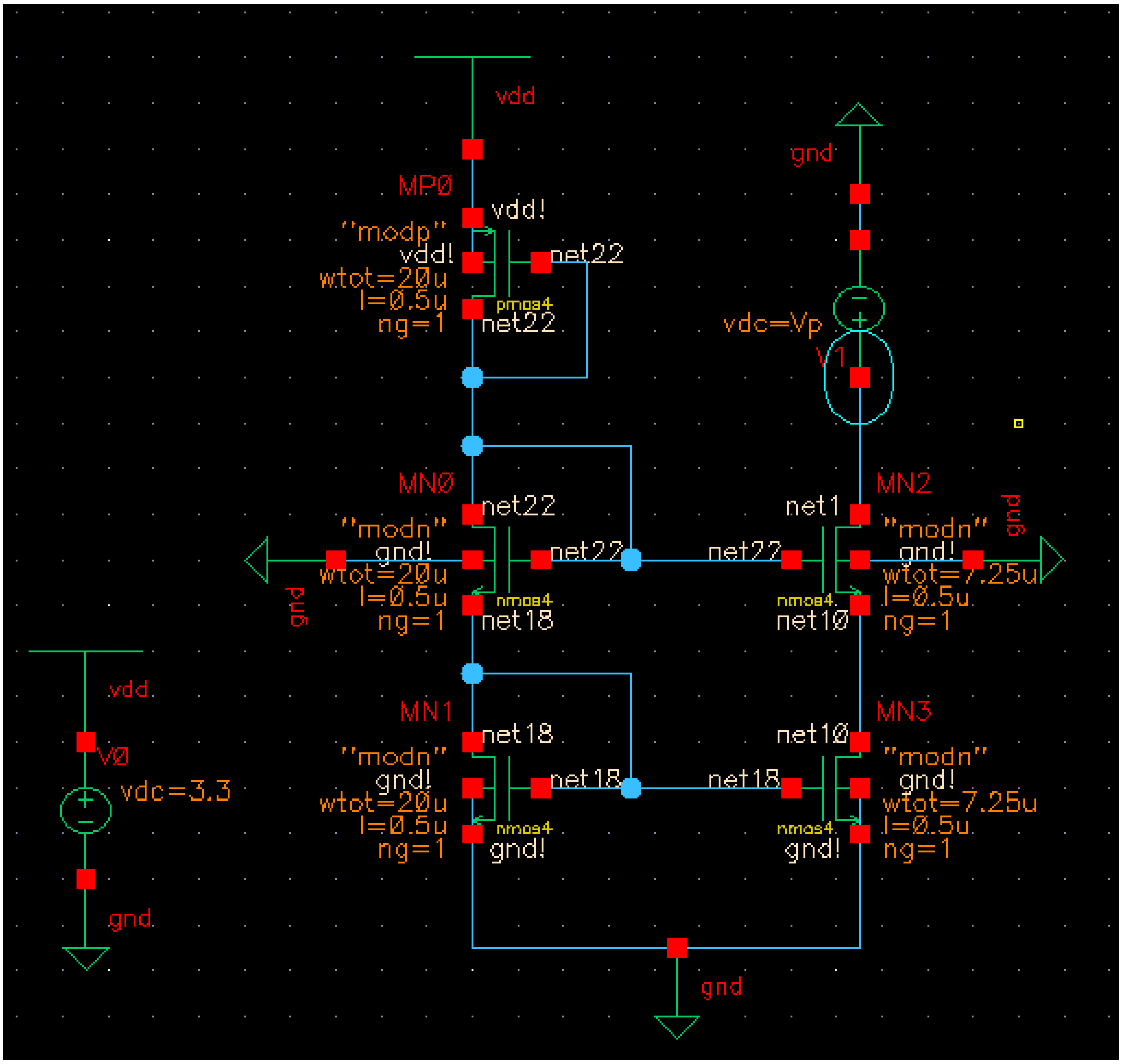

Figure 1.2: Implementing 100uA constant current source in Fig.1.1 by using Cascode MOS Mirror topology.

In order to implement 100uA current source (I1 in Fig.1.1), Cascode MOS Mirror structure is used rather than basic current mirror since cascoding increases output resistance of current source which behaves like as active load of folded cascode. The gain of folded cascode:

$Av=gm1*Rout$, where gm1 is the transconductance of nmos in Fig.1.1

Thus by using a current mirror with high output resistance we can obtain higher gain around 70dB easily. Output Resistance of current mirror in Fig.1.2:

$$Ro=ro2+[1+(gm2+gmb2)ro2]ro3 \sim gm2*(ro)^2$$

Also by using cascode current mirror it is easier to arrange stable currents in output while operating basic current mirror structure is a bit challanging. Although we are favor of implementing cascode current mirror to benefit from its high output resistance, there is a drawback of this configuration like consuming large portion of VDD voltage and restricting our output voltage swing.

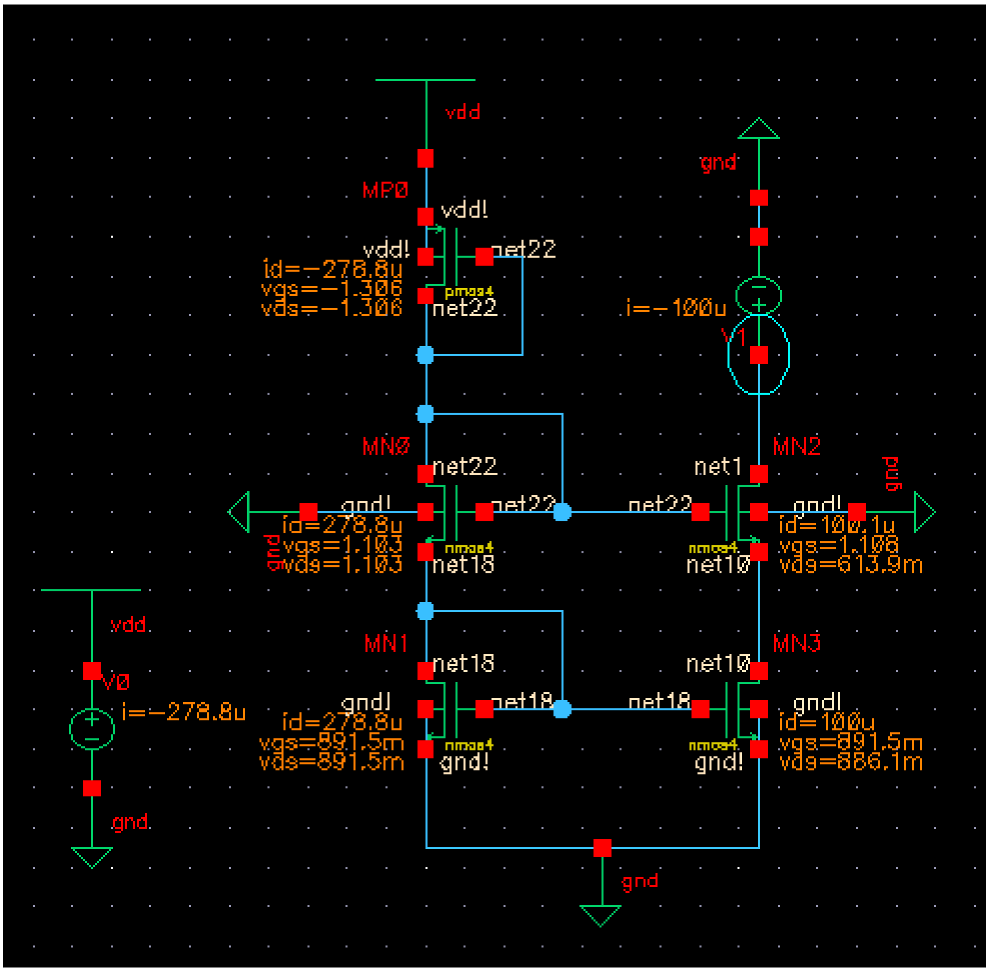

Figure 1.3: Quiescent Points of Cascode Current Mirror.

Generally Vov values of MOS in the range of 0.2V-0.4V range so to be consistent with convention I assumed Vov around 0.4V to make hand calculations. For ID=100uA, Vov=0.4V for 0.5um CMOS technology i deduced widths of MN2 and MN3 transistors approximately 3.3um. Therefore i started to Cascode current mirror design by using this values for MN2 and MN3. However for this values I obtained Vov voltages of MN2 and MN3 a bit higher than what i assumed. Probably this differences derived from the short channel effect. Then, in order to decrease overdrive voltages of MN2 and MN3, i tried different sets of values for transistors in Figure 1.2 and consequently i came up with values in Fig.1.2 and Vov=325mV for MN2 and MN3.

As seen in Fig.1.3 all transistors work in saturation region and we generate Iref=278.8uA current by simply using a diode connected pmos and we obtain 100uA as output current.

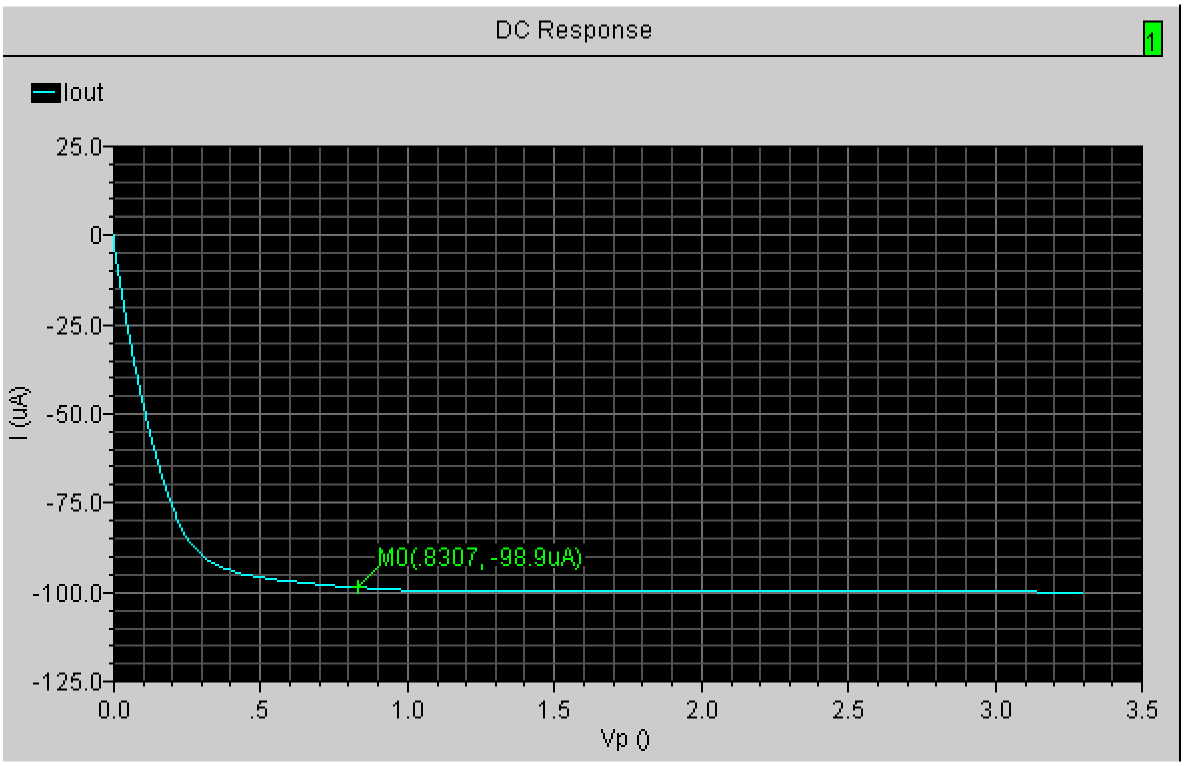

Figure 1.4: Vp vs Iout Graph of Cascode Current Mirror.

In Fig.1.4, Iout is not stable for 0<Vp<0.8-0.9V whereas Iout can be considered as constant for Vp>0.8-1V. The reason is that for 0<Vp<0.8-0.9V MN2 and MN3 nmos transistors are not in the saturation region simultaneously and for Vp>0.8-0.9V all transistors operates in saturation region.Also we can interpret Figure 1.4 as that, in order to implement circuit in Fig 1.2 as a 100uA constant current source in folded cascode configuration of Fig.1.1, we need to bias Vp in the range roughly 1V to 3.3V

Another observation about this current mirror is that it pull current and functions like a current sink.

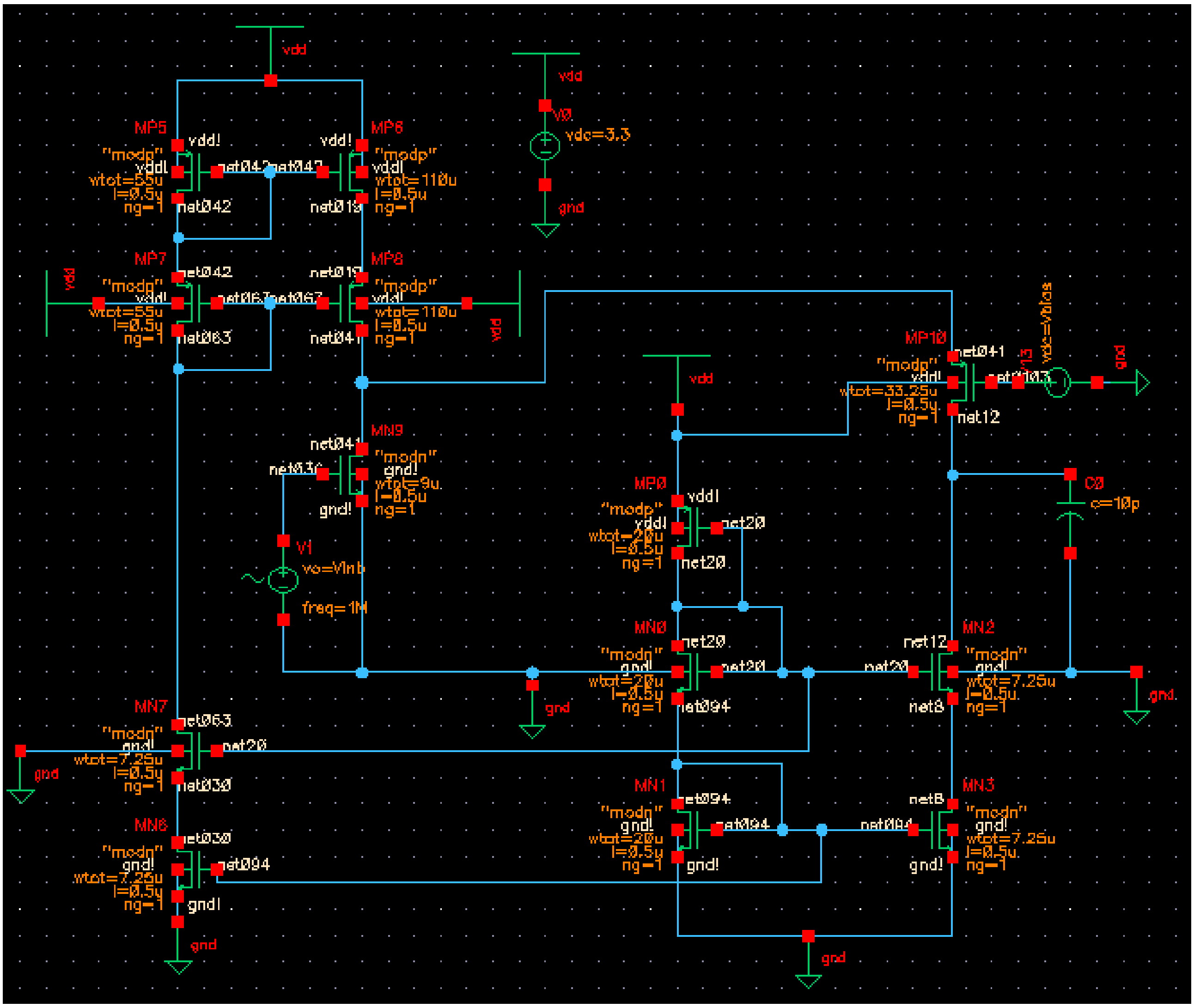

Figure 1.5: Shematic of Folded Cascode with implementation of constant current sources. Component parameters of all nmos and pmos transistors.

In integrating circuit design convention, once a current is generated at particular location, then this current is replicated and distributed to other locations via current steering to bias other components. As seen in Fig.1.5, 200uA current source is implemented by a simple current steering circuit based on pulling 100uA current from MP5 and MP7 pmos transistors by using a current mirror and pushing 200uA current from MP6 and MP8 pmos transistors to folded cascode circuit. In order to push 200uA current from NP6 and NP8, width ratios are arranged like that:

$$(W6/W5)=(110/55)$$

$$(W8/W7)=(110/55)$$

Before 200uA current source is inserted to folded cascode circuit, its Iout versus Voltage dependency is checked in a similar fashion to 100uA current source, by simply sweeping voltage at drain of MP8. The results roughly was that : for 0 < VDP8(voltage at drain of MP8) < 2.3V

200uA constant current is obtained and for VDP8>2.3V current through MP8 and MP6 starts to decay since these two transistors are not in saturation region simultaneously.

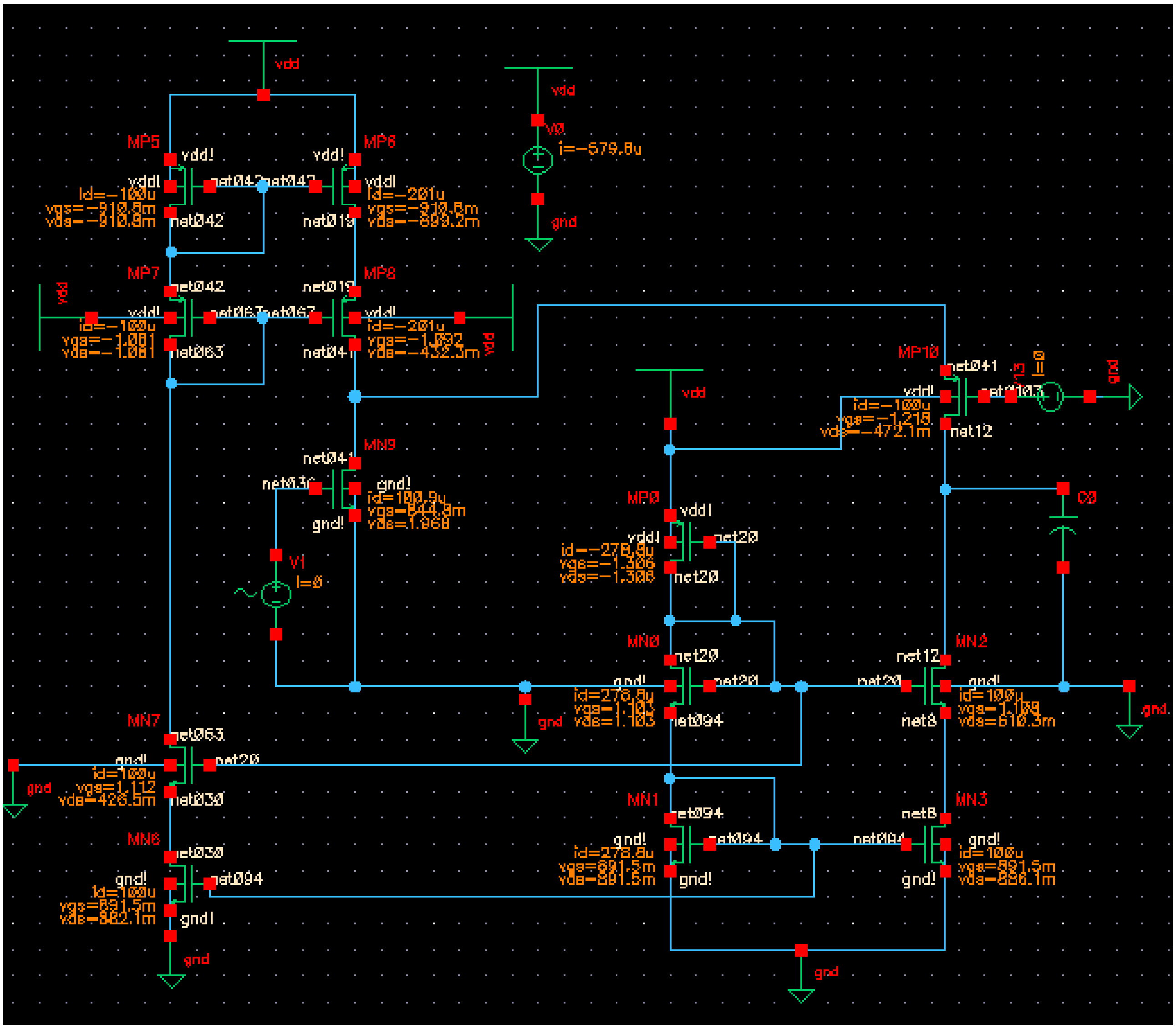

Figure 1.6: DC Operating Points of Folded Cascode Design.

As seen in Fig.1.6 all mosfets that are used in designing process of Folded Cascode Amplifier are biased in saturation region. In order to accomplish this, Vinb=0.8448V offset voltage is given in input terminal and Vbias=0.75V is given to gate of MP10. The reason for chosing Vinb=0.8448 is that when we sweep a dc input voltage and plot Vo/Vi transfer characteristic of circuit, Vinb=0.8448 was the point that slope is steepest or in other words Av=Vo/Vi is highest.

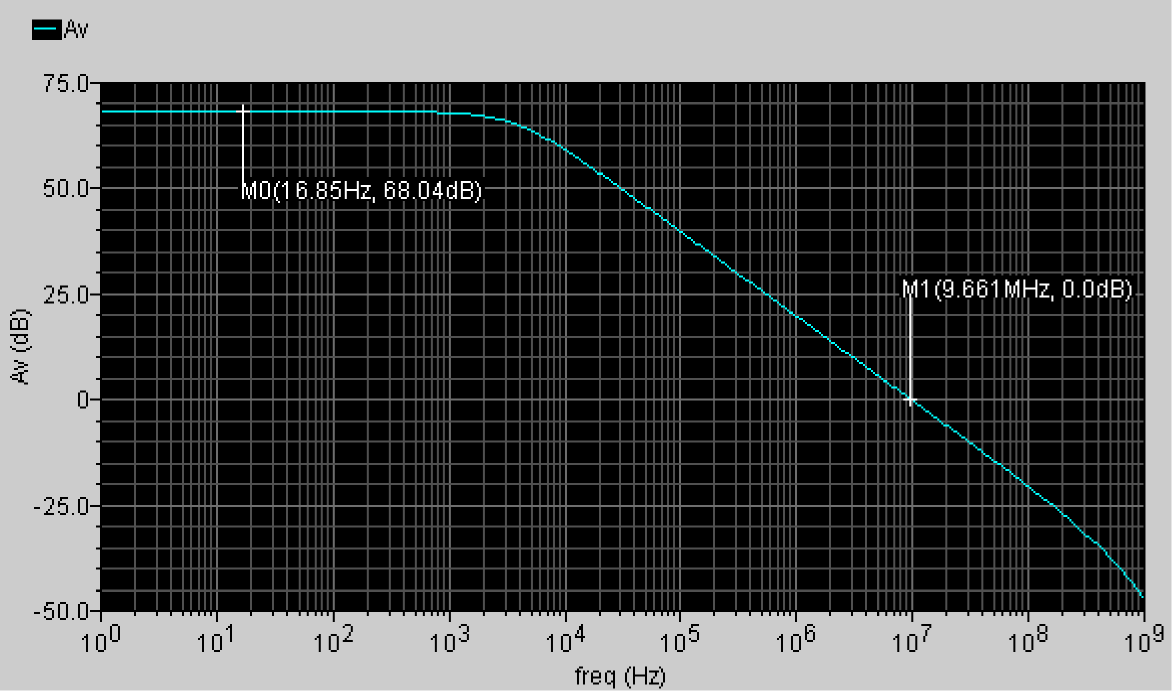

Figure 1.7: Gain-Frequency graph of Folded Cascode.

As seen in graph above, unity gain frequency is W=9.661MHz and Av=68dB for low frequencies. In order to obtain higher gain (like above 70dB) I can increase L of MN2 and MN3. The idea behind increasing L is that $\lambda$ is inversely proportional to the length selected for channel. Thus increasing L leads to decreasing of $\lambda$ and we obtain larger ro values for MN2 and MN3 since ro=1/( $\lambda$ID). As it is stated before active load implemented by 100uA current mirror is roughly gm2*(ro)^2 and increasing of L lead to larger Rout and in return it triggers higher gain.

Deducing Rout:

Av=gm*Rout where gm is transconductance of MN9

Av=68dB~2500V/V

gm=616.6u A/V (obtained by checking parameters of MN9)

Rout=Av/gm=2500/616.6 ~4M ohm

Also we could check Rout by applying a small test voltage vx, and finding current ix drawn from vx.

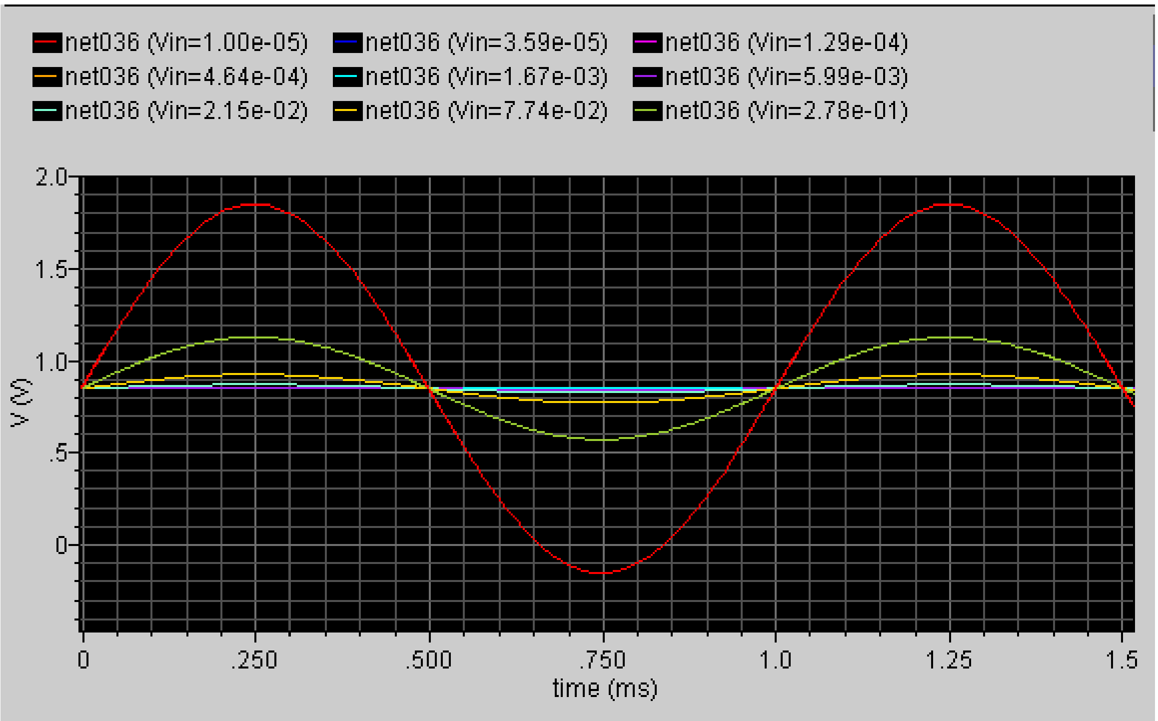

Figure 1.8: Input Voltage Swing

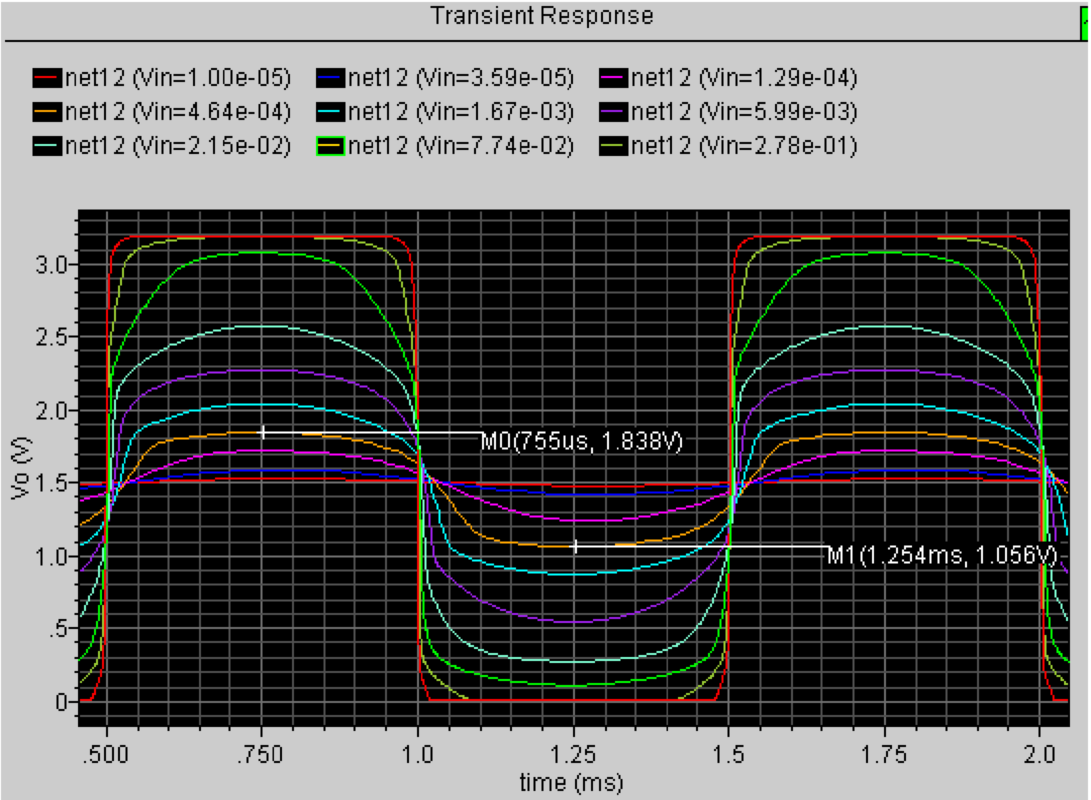

Figure 1.9: Output voltage swing corresponding to input voltage in Fig.1.8 analysis.

As seen in Fig.1.9, output voltage start to distort and clip arount vomax=1.83V and vomin=1V. Therefore it can be said that voltage swing is from 1V to 1.838V. This is also coincide with expectations since output voltage is restricted from below (across 100uA current source) roughly by Vth+2Vdsat~1.1V. In addition output voltage headroom is restricted by 3pmos (MP6, MP8, MP10) so that vomax~3.3V-3Vov~2.1V.

BONUS 1:

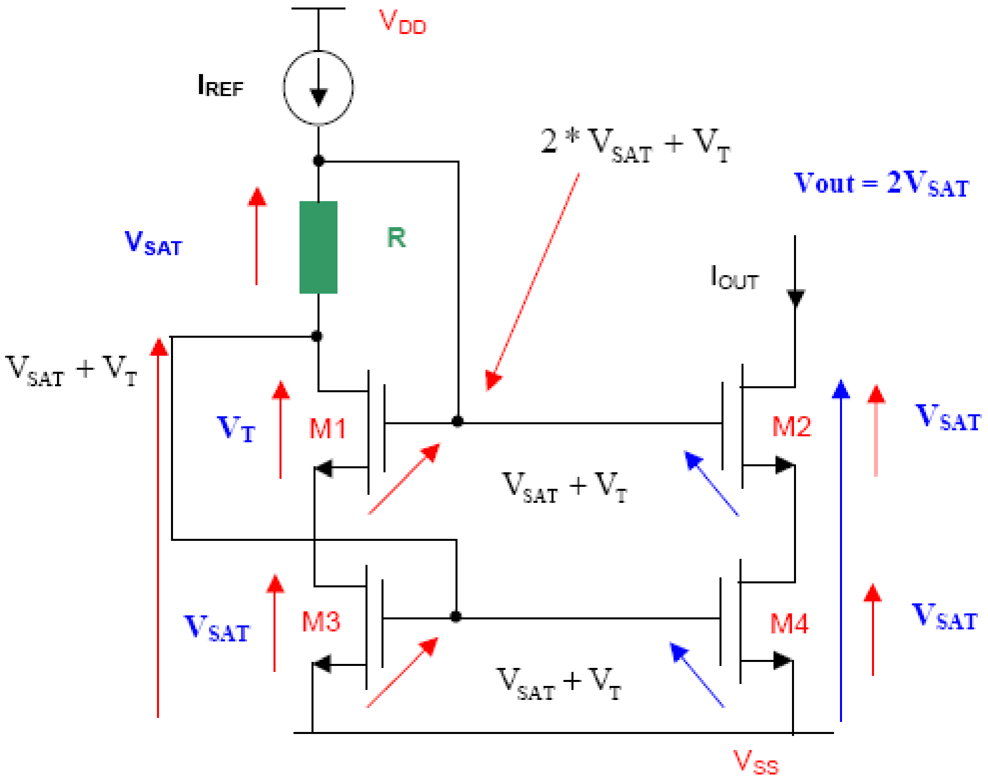

Figure 1.10: Modified Cascode Current Sink to reduce voltage drop across M2 and M4 and increase output voltage swing.

Although voltage drop across M2 and M4 is 2Vsat+Vt for Cascode Current Mirror that we used in Folded Cascode design, modified currenk sink configuration shown as in Fig.1.10, offers a voltage drop 2Vsat. Thus **vo**min is decreased by a amount Vt~0.7V and voltage swing is improved by same amount.

| Rout | Av | Unity Gain Freq. | Output Swing |
|---|---|---|---|
| ~4M ohm | 68dB | 9.661MHz | 1.05V to 1.83V |

Fig.1.10 is taken from www.rfic.co.uk

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# ANALOG INTEGRATED CIRCUITS LAB#2B

## Folded Cascode Layout

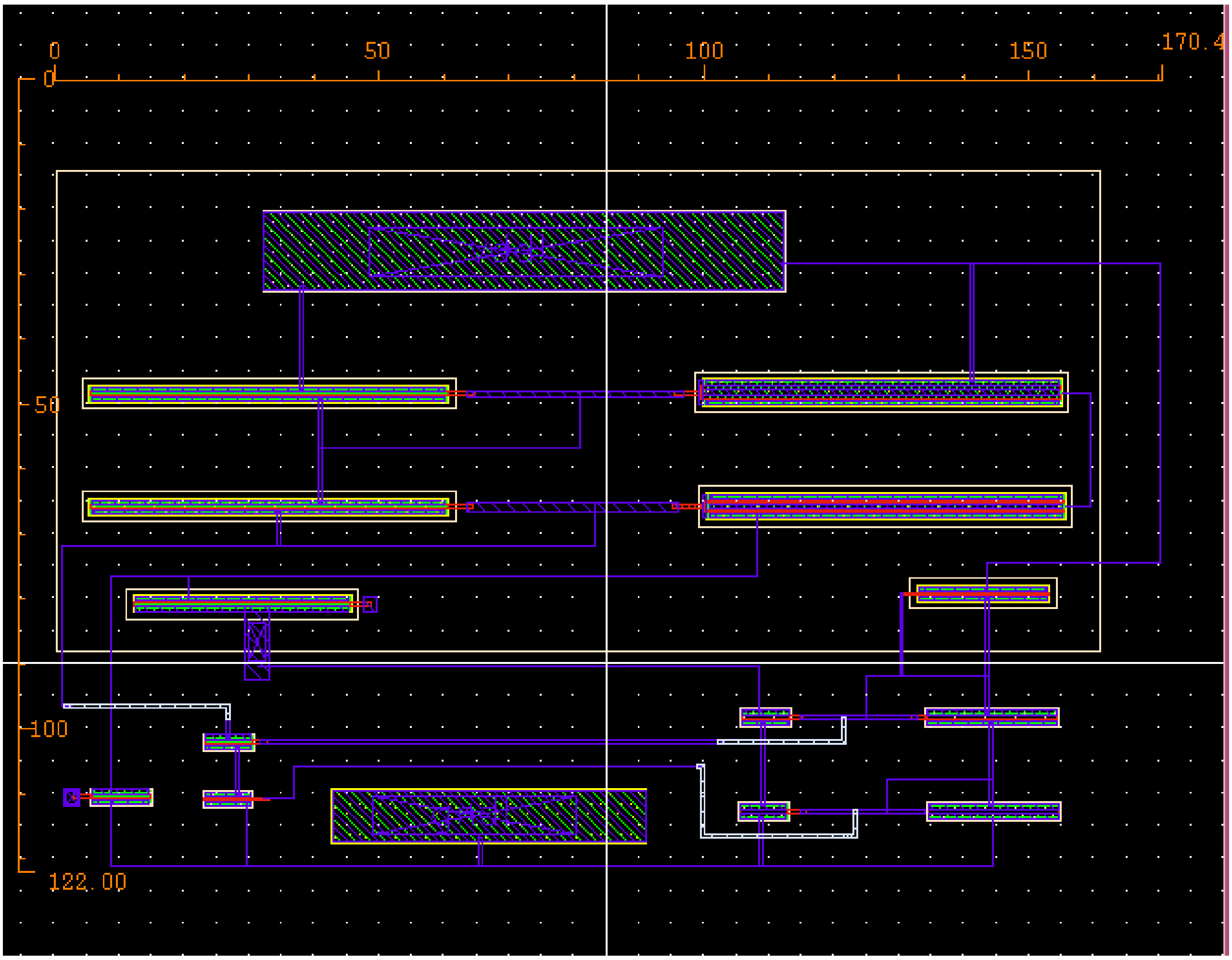
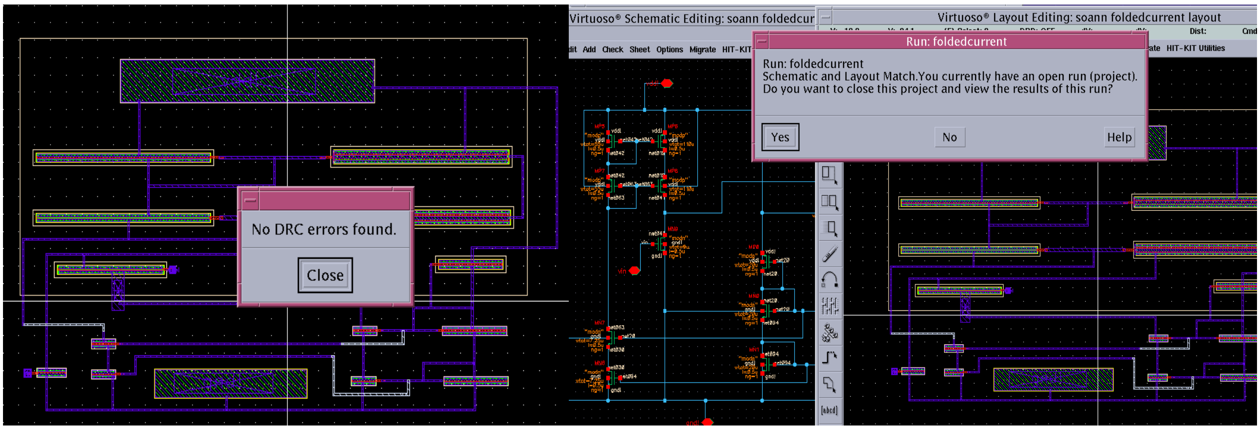


Figure 1.1: General Outlook of Folded Cascode Layout

Layout of the folded cascode amplifier that is designed in shematic level as previous assignment can be seen in *Fig.1.1* . As seen in figure, layout design covers an area approximately$122x10^{-6}x170x10^{-6} \cong 0.02x10^{-6}$. This value for folded cascade layout's area is quite high and it can be decreased by further compression such as increasing number of gates of transistors that possess large width(for pmos transistors that have 110um and 55um widths), bringing mosfets closer to each other and using minimum available paths for metal connections.



No DRC errors found.

Run: foldedcurrent
Schematic and Layout Match.You currently have an open run (project).
Do you want to close this project and view the results of this run?

Figure 1.2: DRC and LVS analysis of folded cascade layout.

As seen in Figure 1.2, no DRC errors found (for grid, no antenna, no coverage, no erc and no generated layers) and layout and schematic of folded cascade amplifier is matched.

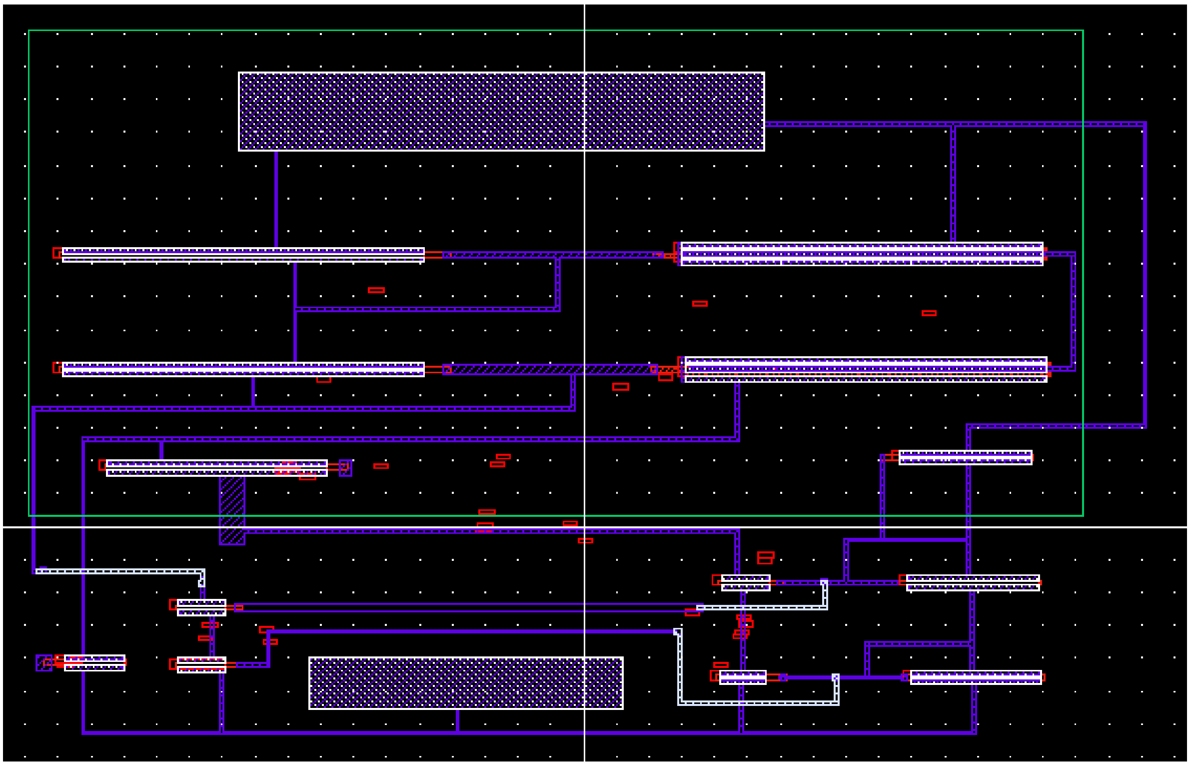
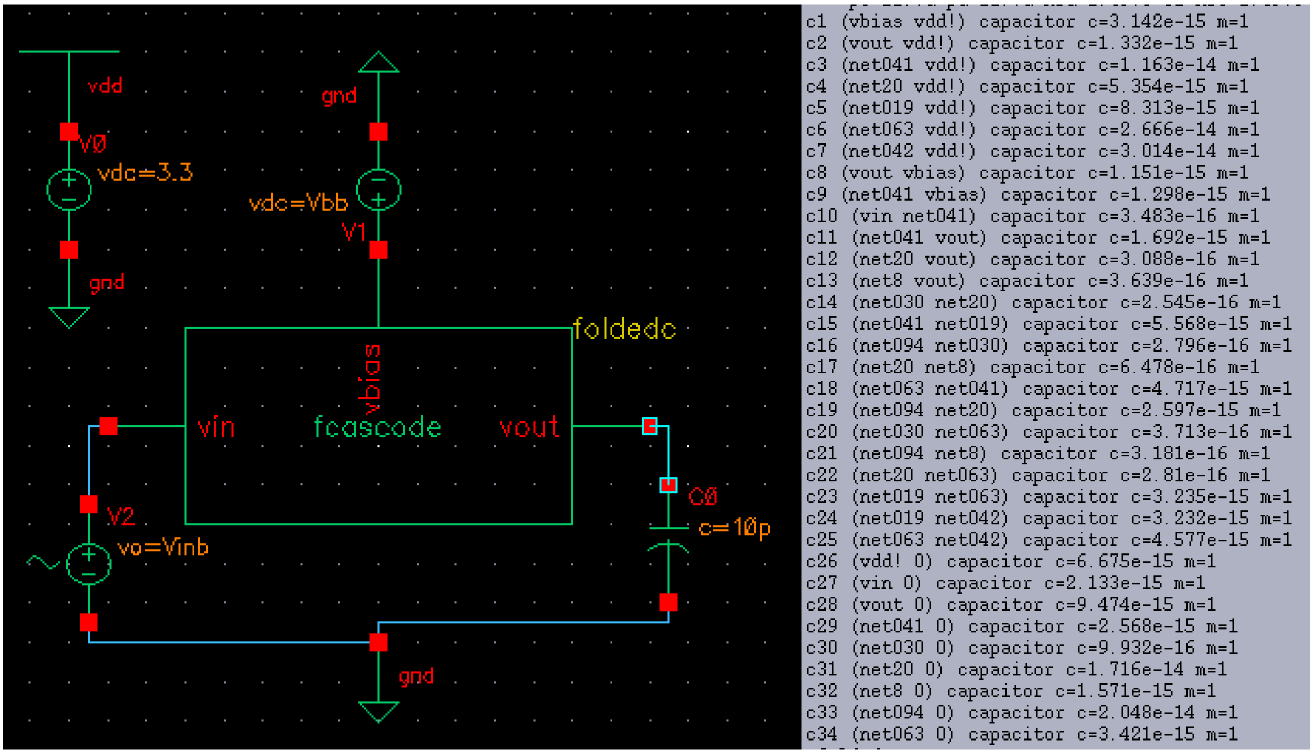


Figure 1.3: Layout of Folded Cascode with Parasitic Capacitances.

When RCX analysis of layout for only C is done, as seen in *Fig.1.2* , layout contains lots of small parasitic capacitances that derives from interconnects and source/drain areas, affects performance of circuit by changing dc operating points of transistors and frequency response of circuit. Prominent of these capacitances (larger ones) are listed in ***Table 1***.

| | | | | | |
|---|---|---|---|---|---|
| C Values | 30.14fF | 20.48fF | 17.16fF | 11.63fF | 9.474fF |
| C Values | 8.313fF | 6.675fF | 5.354fF | 4.717fF | 4.577fF |

Table 1: Values of high capacitances encountered in Fig.1.3.



```
c1 (vbias vdd!) capacitor c=3.142e-15 m=1
c2 (vout vdd!) capacitor c=1.332e-15 m=1
c3 (net041 vdd!) capacitor c=1.163e-14 m=1
c4 (net20 vdd!) capacitor c=5.354e-15 m=1
c5 (net019 vdd!) capacitor c=8.313e-15 m=1
c6 (net063 vdd!) capacitor c=2.666e-14 m=1
c7 (net042 vdd!) capacitor c=3.014e-14 m=1
c8 (vout vbias) capacitor c=1.151e-15 m=1
c9 (net041 vbias) capacitor c=1.298e-15 m=1
c10 (vin net041) capacitor c=3.483e-16 m=1
c11 (net041 vout) capacitor c=1.692e-15 m=1
c12 (net20 vout) capacitor c=3.088e-16 m=1
c13 (net8 vout) capacitor c=3.639e-16 m=1
c14 (net030 net20) capacitor c=2.545e-16 m=1
c15 (net041 net019) capacitor c=5.568e-15 m=1
c16 (net094 net030) capacitor c=2.796e-16 m=1
c17 (net20 net8) capacitor c=6.478e-16 m=1
c18 (net063 net041) capacitor c=4.717e-15 m=1
c19 (net094 net20) capacitor c=2.597e-15 m=1
c20 (net030 net063) capacitor c=3.713e-16 m=1
c21 (net094 net8) capacitor c=3.181e-16 m=1
c22 (net20 net063) capacitor c=2.81e-16 m=1
c23 (net019 net063) capacitor c=3.235e-15 m=1
c24 (net019 net042) capacitor c=3.232e-15 m=1
c25 (net063 net042) capacitor c=4.577e-15 m=1
c26 (vdd! 0) capacitor c=6.675e-15 m=1
c27 (vin 0) capacitor c=2.133e-15 m=1
c28 (vout 0) capacitor c=9.474e-15 m=1
c29 (net041 0) capacitor c=2.568e-15 m=1
c30 (net030 0) capacitor c=9.932e-16 m=1
c31 (net20 0) capacitor c=1.716e-14 m=1
c32 (net8 0) capacitor c=1.571e-15 m=1
c33 (net094 0) capacitor c=2.048e-14 m=1
c34 (net063 0) capacitor c=3.421e-15 m=1
```

Figure 1.4: Schematic of Post-Layout Simulation and Capacitances in Netlist.

As stated before, how the layout is designed is crucial in effecting the performance of circuit since parasitic capacitances are generated according to it. In order to determine how the folded cascade would work from layout we need to perform a post-layout simulation by using the schematic shown in *Fig.1.4.* As seen in netlist, there are 34 capacitances extracted from layout (match with Table 1 too) and we will take into account all these parasitic capacitances while doing simulation.

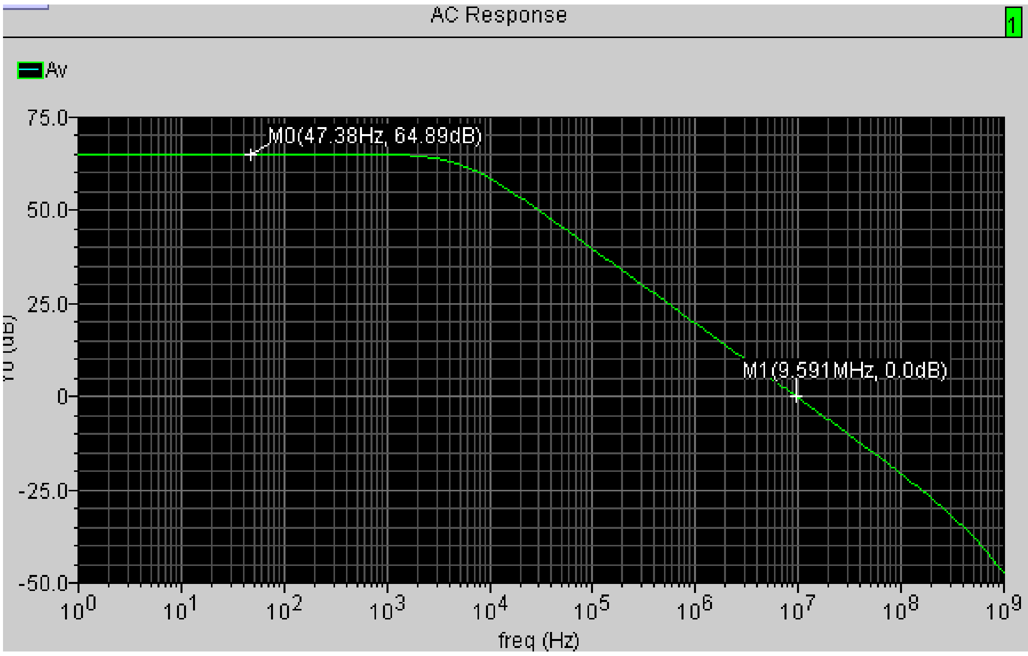


Figure 1.5: Gain-Frequency graph of Folded Cascode with parasitic capacitances for Vinb=844.8mV and Vbb=481.5mV.

As stated in previous lab report, we had biased circuit in schematic level with 0.8448V offset voltage in input and Vbb=0.75V in the gate of pmos whose drain is used to take output. When these values are entered as post-layout schematic bias voltages, transistor marked in Figure 1.6 operates in triode region and thus gain decreases to roughly$Av = 40dB$.

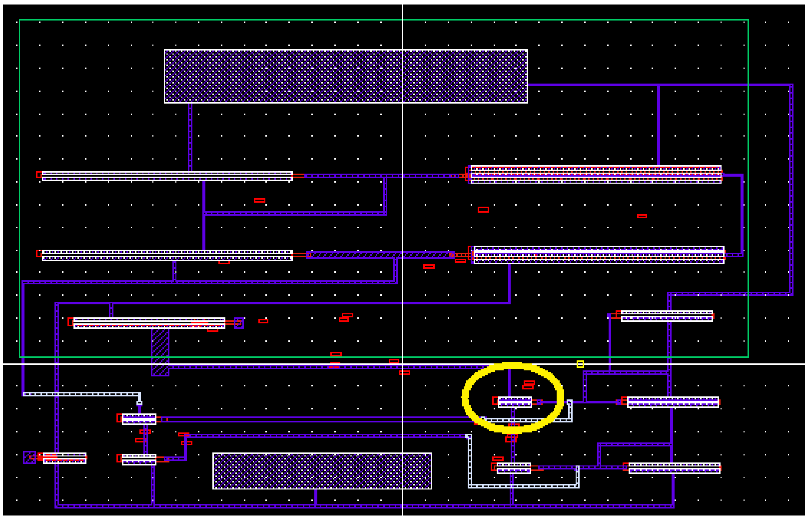


Figure 1.6: Marked NMOS transistor of constant current source operates in triode region for Vbb=0.75V and Vinb=0.8448 for circuit in Fig.1.4.

Constant current source behave like active load of folded cascode ($Ro \cong gm.ro^2$ ) where gm and ro belong to marked nmos and nmos below it. Thus while marked transistor is in triode, output resistance of it decreases and active load of folded cascade (Ro) decreases. This is the reason of decrease in gain.

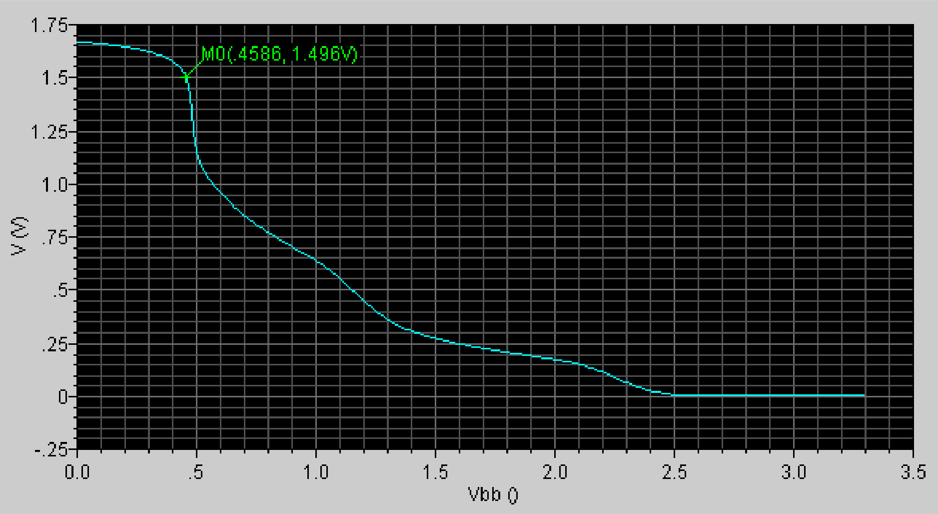


Figure 1.7: Sweep Analysis of Vbb bias voltage.It is obvious from graph for Vbb=0.75V, Vo biased around 0.8V and thus constant current source does not perform properly.

As we recall from report of schematic design, constant current source for I=100uA was working properly for $V_O$ *biased at roughly in the range* $1V$ *to* $3.3V$ and we had biased folded cascode for $V_O = 1.496$V. Therefore, in order to determine whether it is possible to bias $V_O$around 1.496V while parasitic capacitances are considered, sweep analysis performed for Vbb bias voltage. The output of this analysis is obvious in Fig.1.7 and it shows that it is possible to bias $V_O$ around 1.496V for Vbb is about 0.458V. In other words, for Vbb=0.458, $V_O$biased around 1.496V, designed constant current source will work properly with all transistors in saturation region and it would allow us to obtain higher gain.

By using inspection explained above, I start to perform ac analysis for $Vinb = 844.8mV \ and \ Vbb = 458mV$and all transistors were in saturation, gain around 57dB is obtained. Then, by increasing this initial point, I managed to increase gain to 64.89dB as seen in Fig. 1.5 (page 3) for $Vbb = 481.5mV$. Also as in Fig.1.5 it is obvious that unity gain frequency is equal to 9.591Mhz.

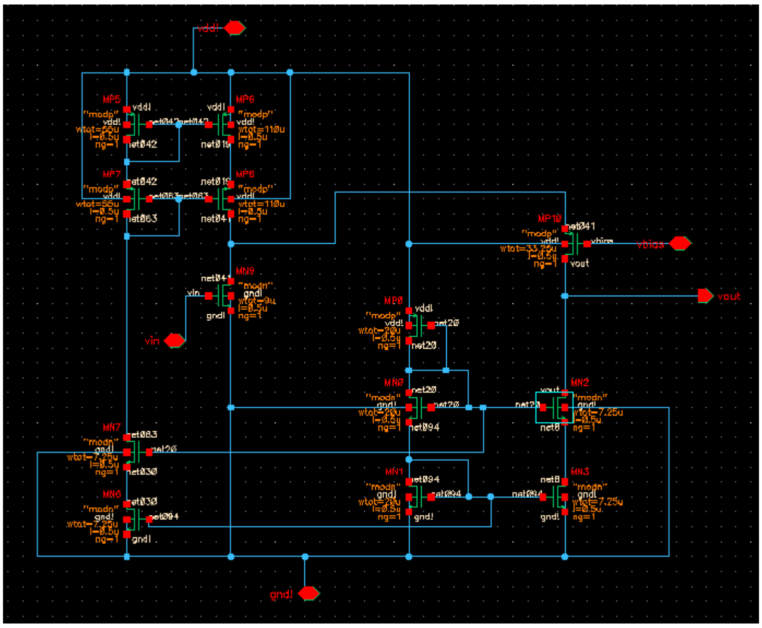


Figure 1.8: Schematic of folded cascode when descended into symbol shown in Fig.1.4

Deducing Rout for Post-Layout simulation:

$$Av = gm.Rout$$

$$Rout = \frac{Av}{gm} \ where \ gm \ is \ transconductance \ of \ MN9 \text{ shown in Fig.1.8}$$

$$Rout \cong \frac{1757}{612.3x(10^{-6})} \cong 2.87Mohm$$

As seen, Rout deduced when parasitic capacitances of layout is considered, is lower than Rout we found in schematic analysis of folded cascode.

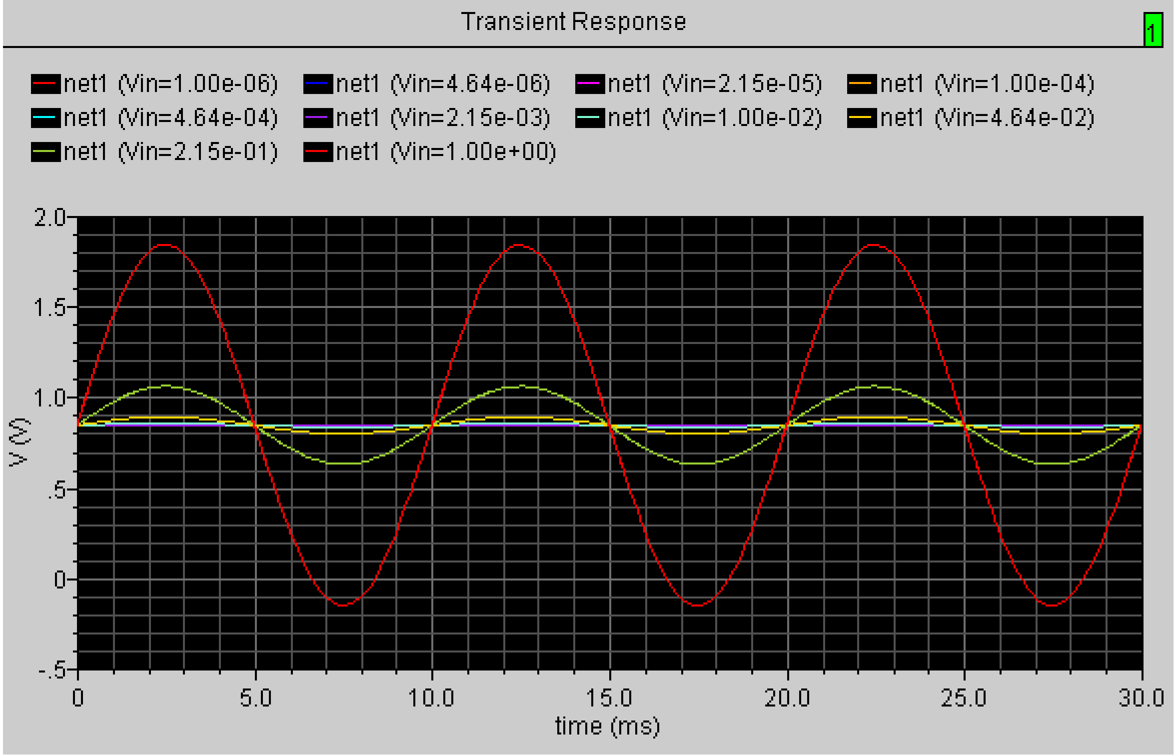


Figure 1.9: Input voltage swing.

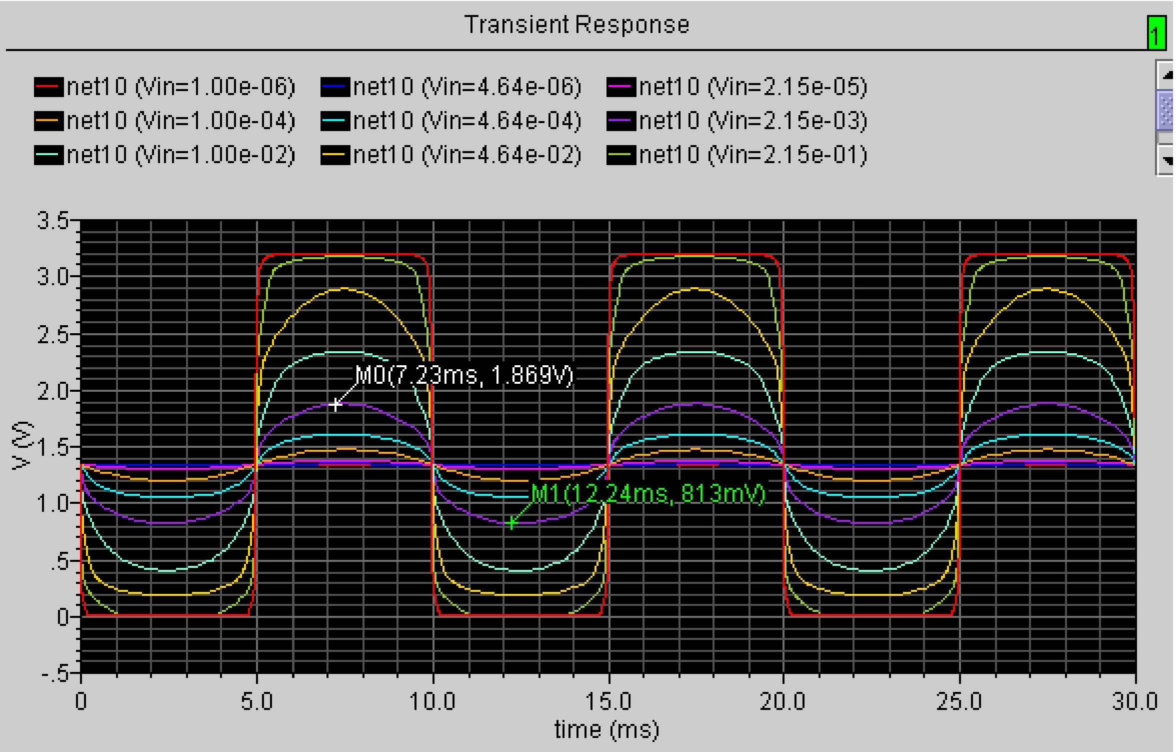


Figure 1.10: Output voltage swing corresponding to input voltage in Fig 1.9

As seen in Fig.1.10, output voltage start to distort and clip around $v_{omax} = 1.869V\ and\ v_{omin} = \ 0.813v$. Thus output voltage swing is from 0.813V to 1.869V.

|  | Av | Rout | Unity Gain Frequency | Output Swing |
|---|---|---|---|---|
| Shematic | 68dB | 4Mohm | 9.661MHz | 1.05V to 1.83V |
| Layout | 64.89dB | 2.87Mohm | 9.591Mhz | 0.813V to 1.869 |
| Deviation | %4.5 | %28.25 | %0.72 | %2 |

Table 2: Comparison of values obtained in schematic and layout simulation with extracted capacitances.