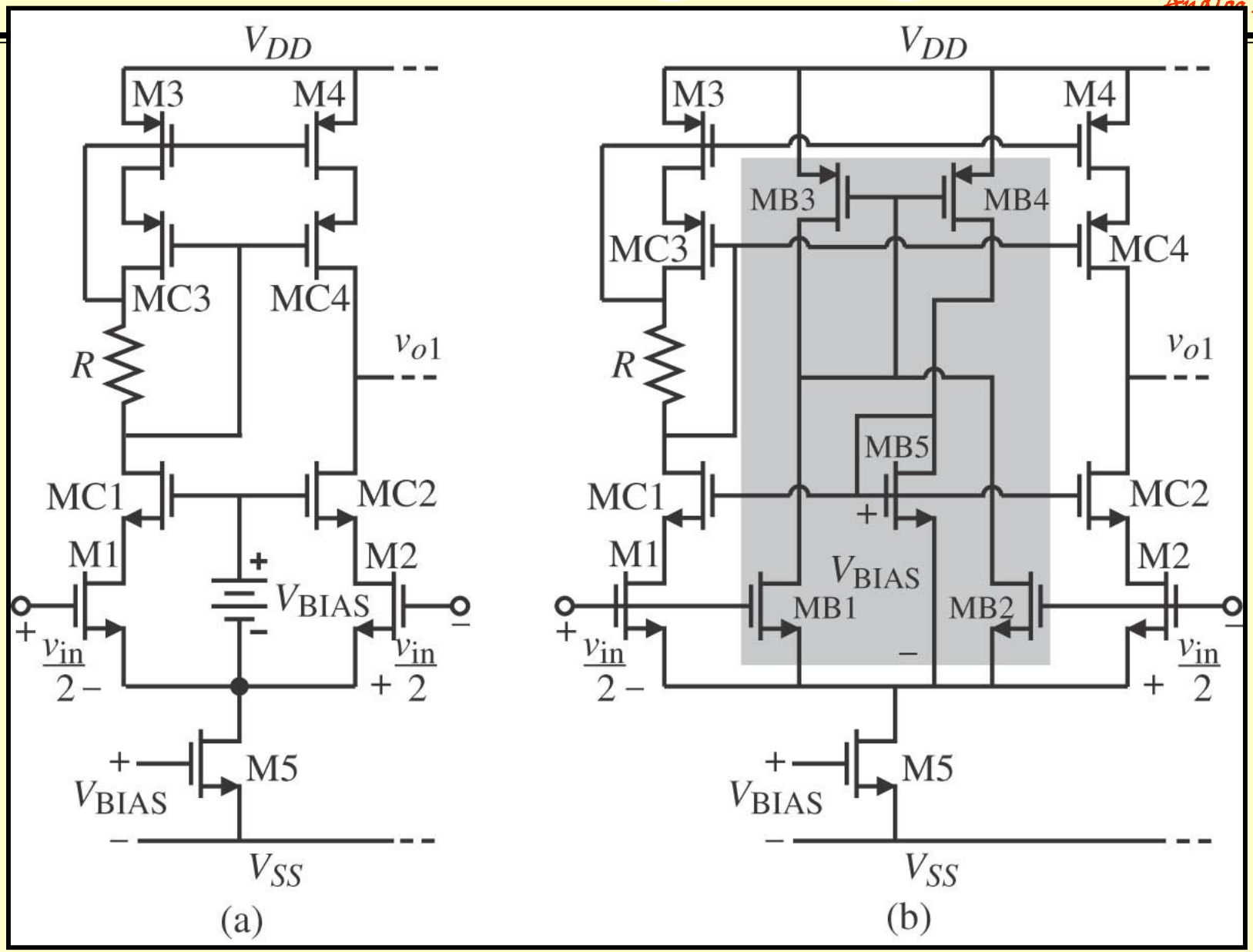
Cascode & Other Improved Amplifier Building Blocks

ECEN 4228/5008

Fall 2004

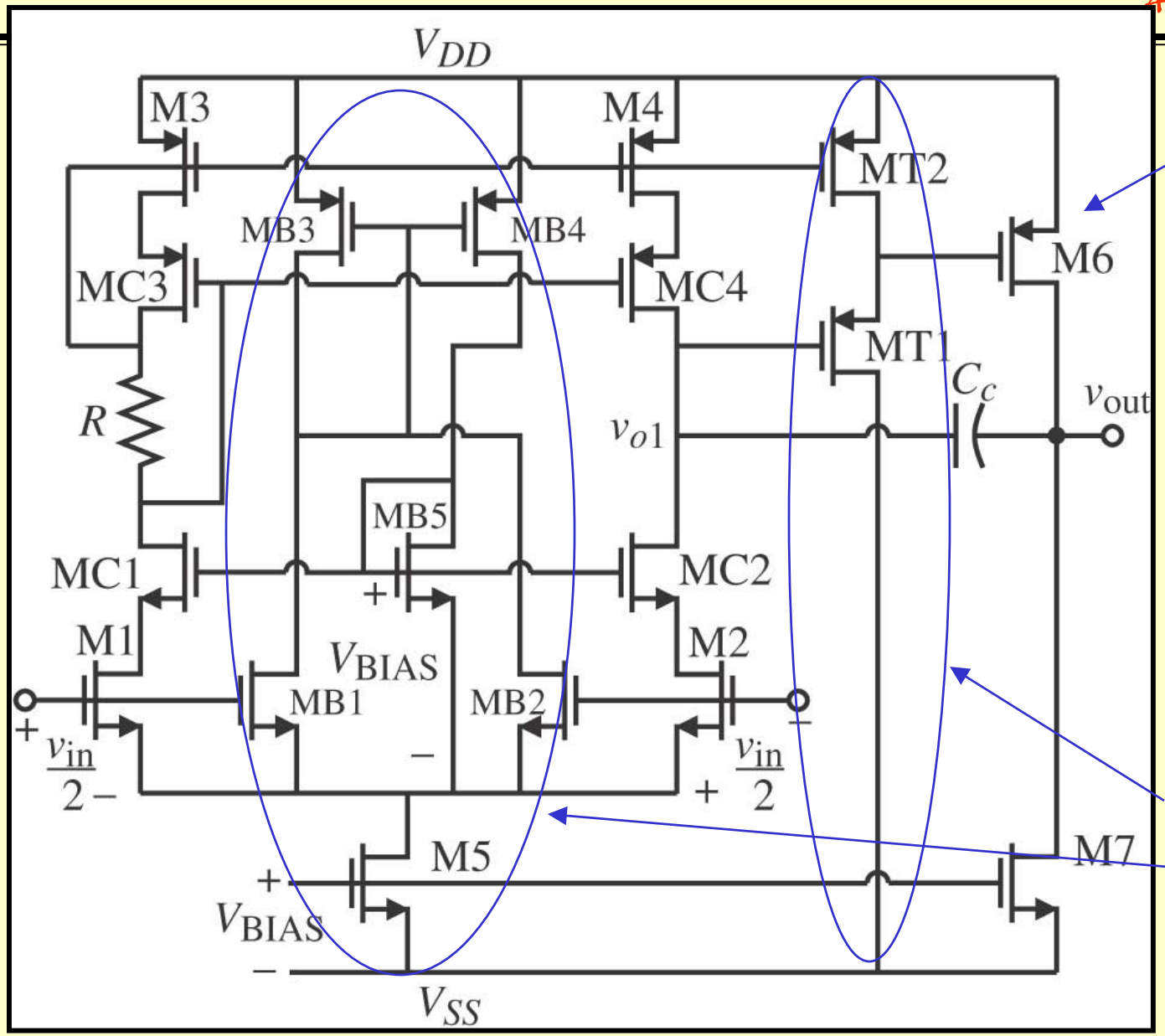
* Figure examples from [Allen/Holberg] reference text unless otherwise stated

Cascode – Input Stage



Text Figure 6.5-1

Two-Stage w/ Cascode Input

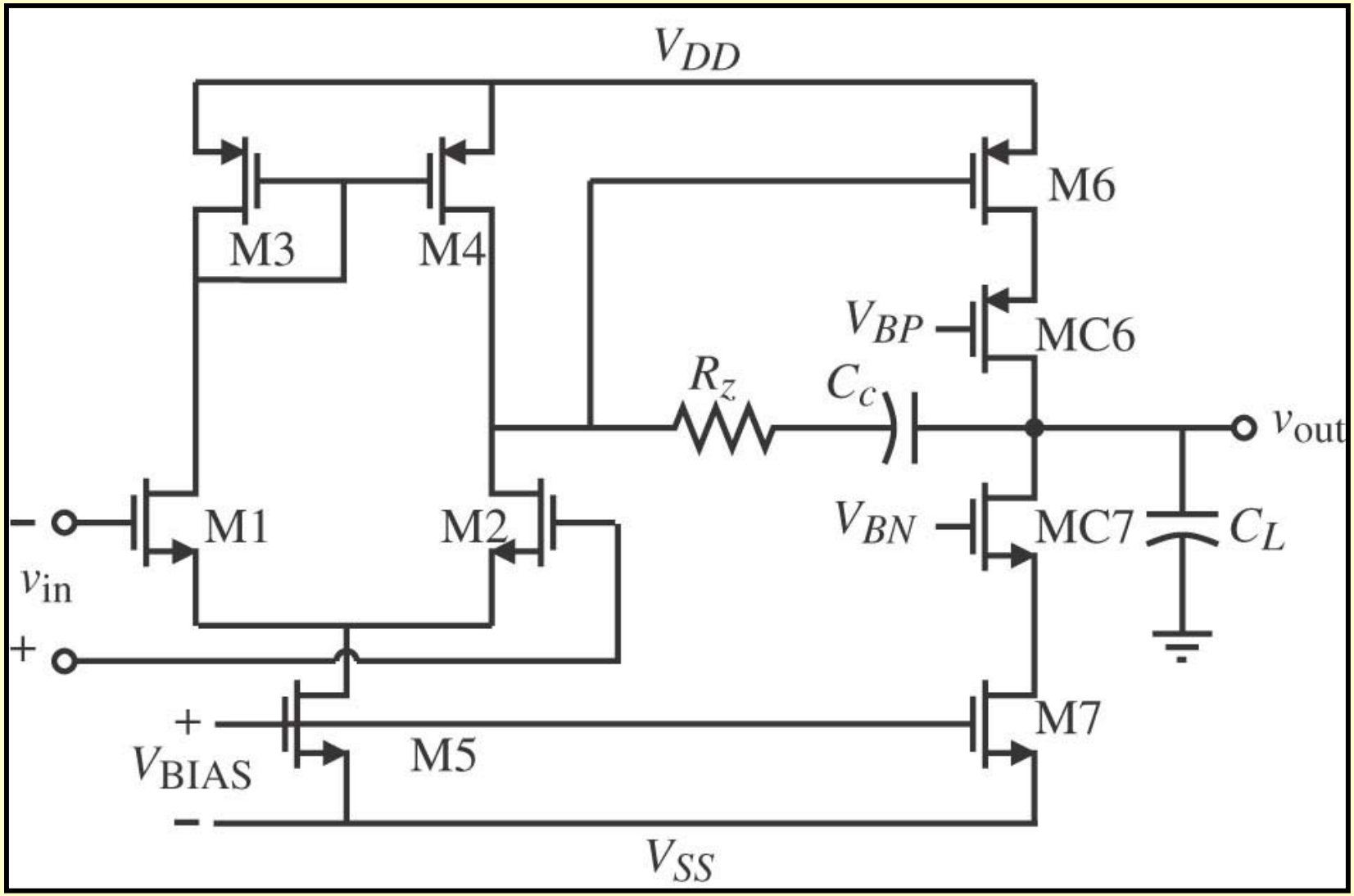


2nd Stage

Cascode bias

Text Figure 6.5-2

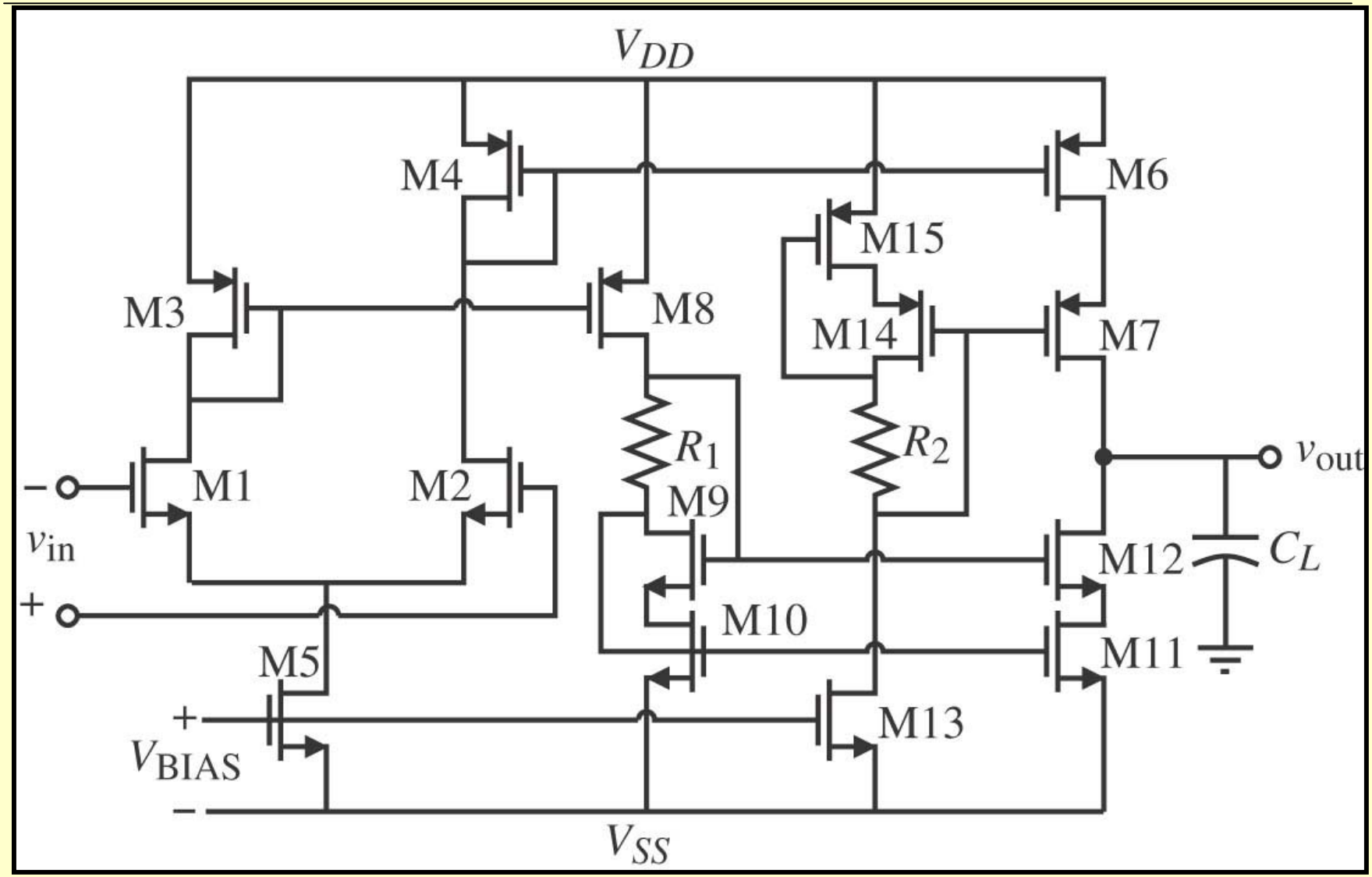
Cascode: 2nd "Miller" Stage



Text Figure 6.5-3

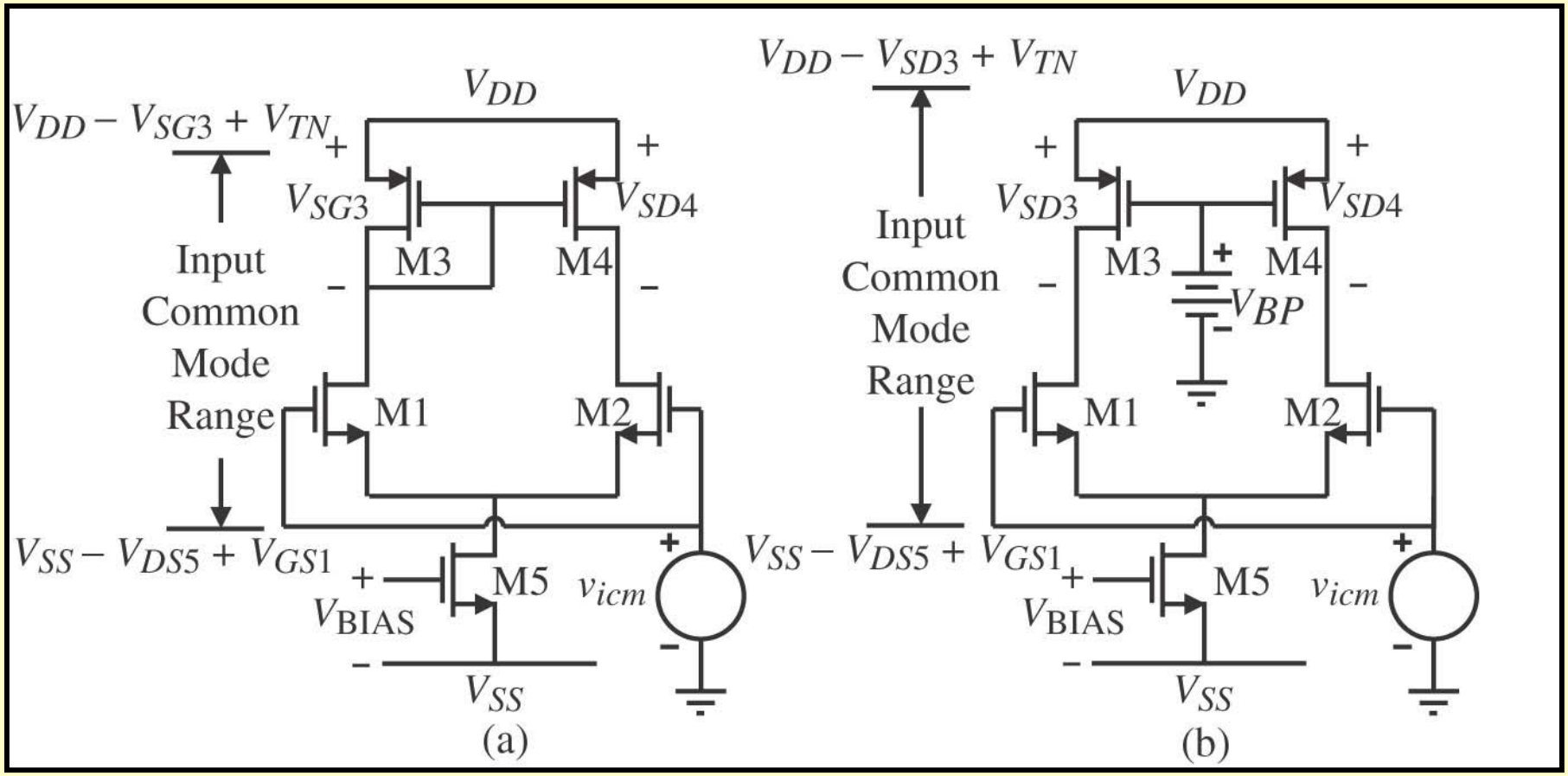
Cascode: Symmetrical OTA

(Push-Pull)



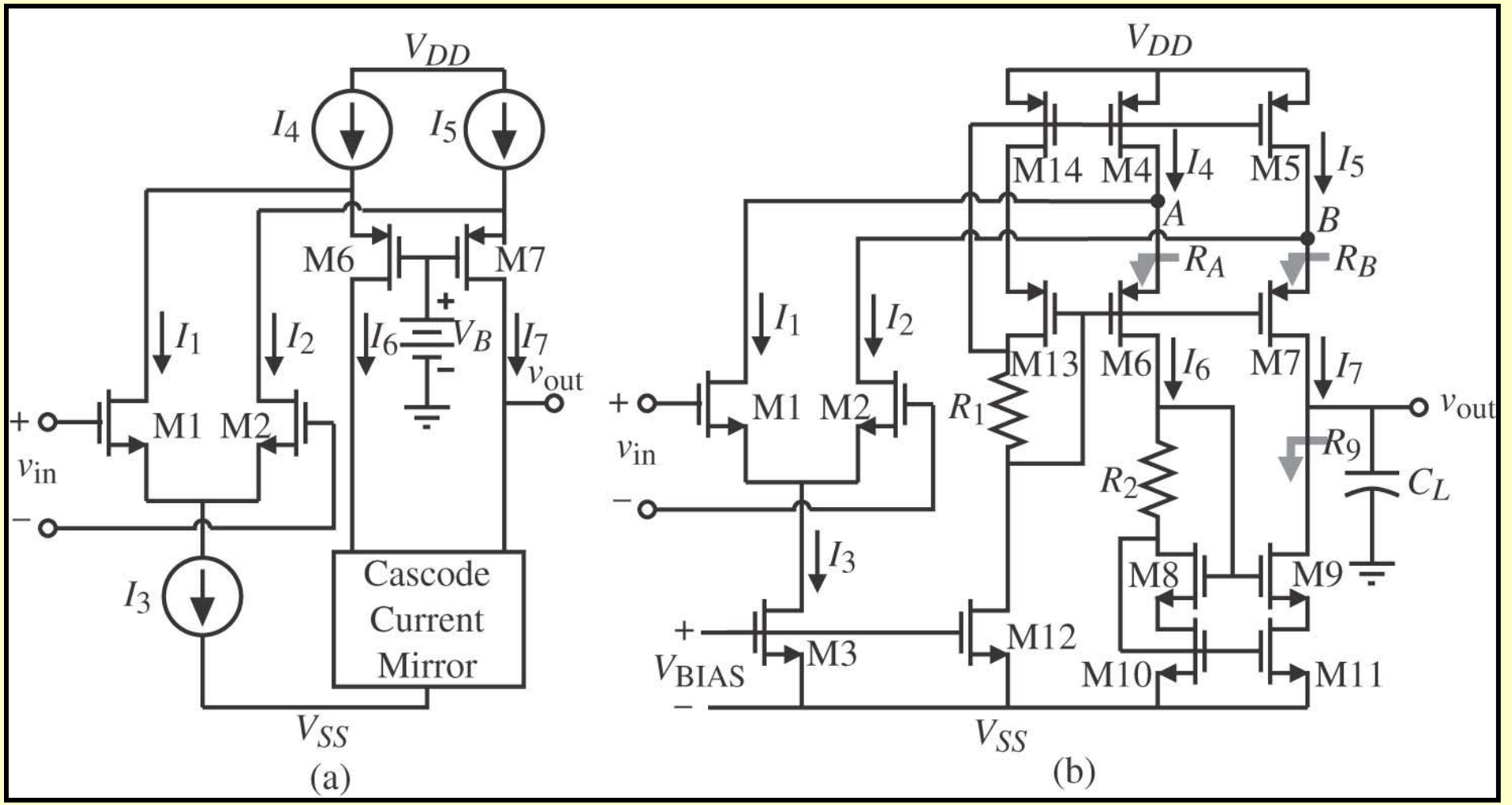
Text Figure 6.5-4

Improve ICMR: I-Source Load



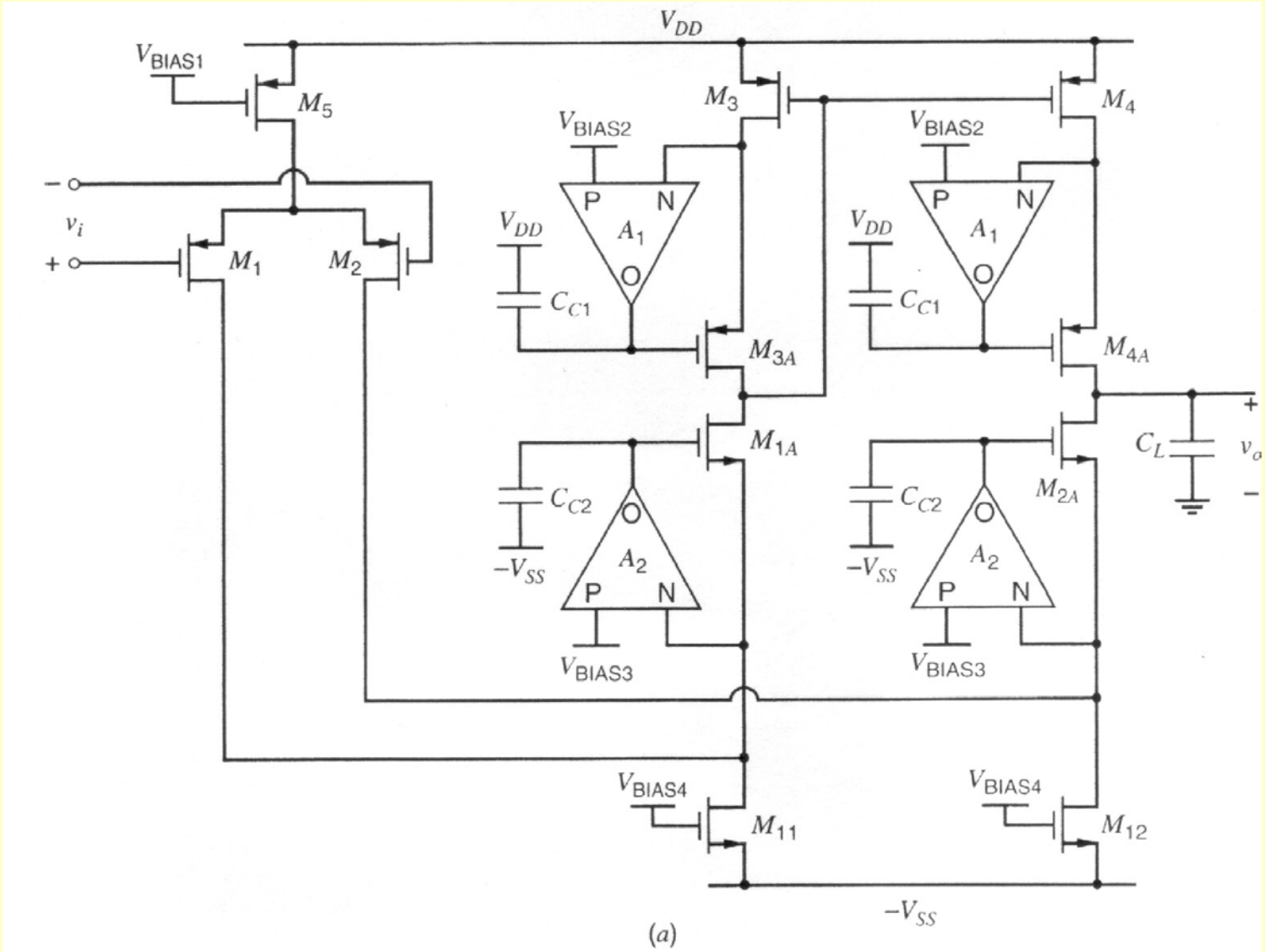
Text Figure 6.5-6

Folded Cascode



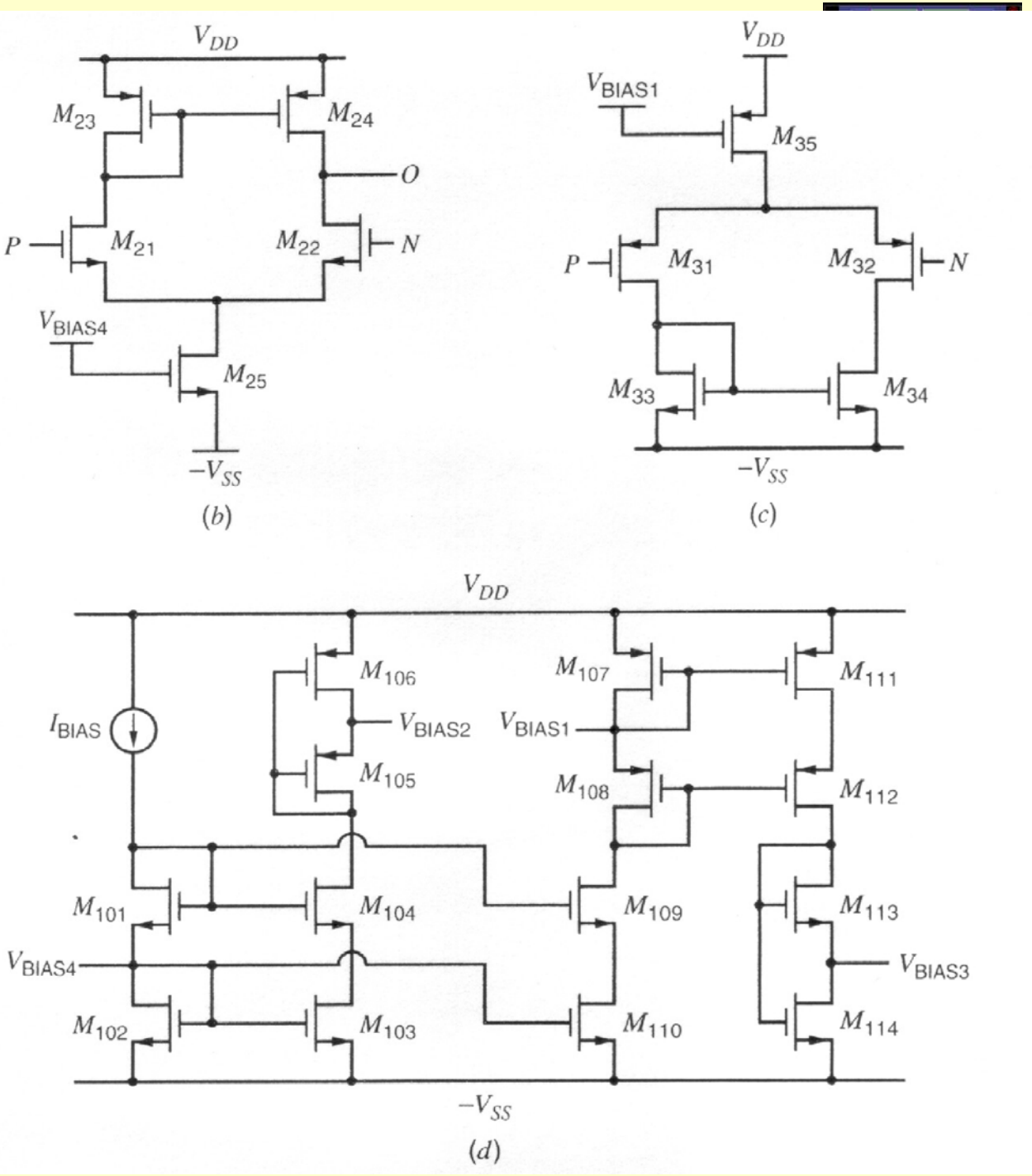
Text Figure 6.5-7

High gain, folded cascode



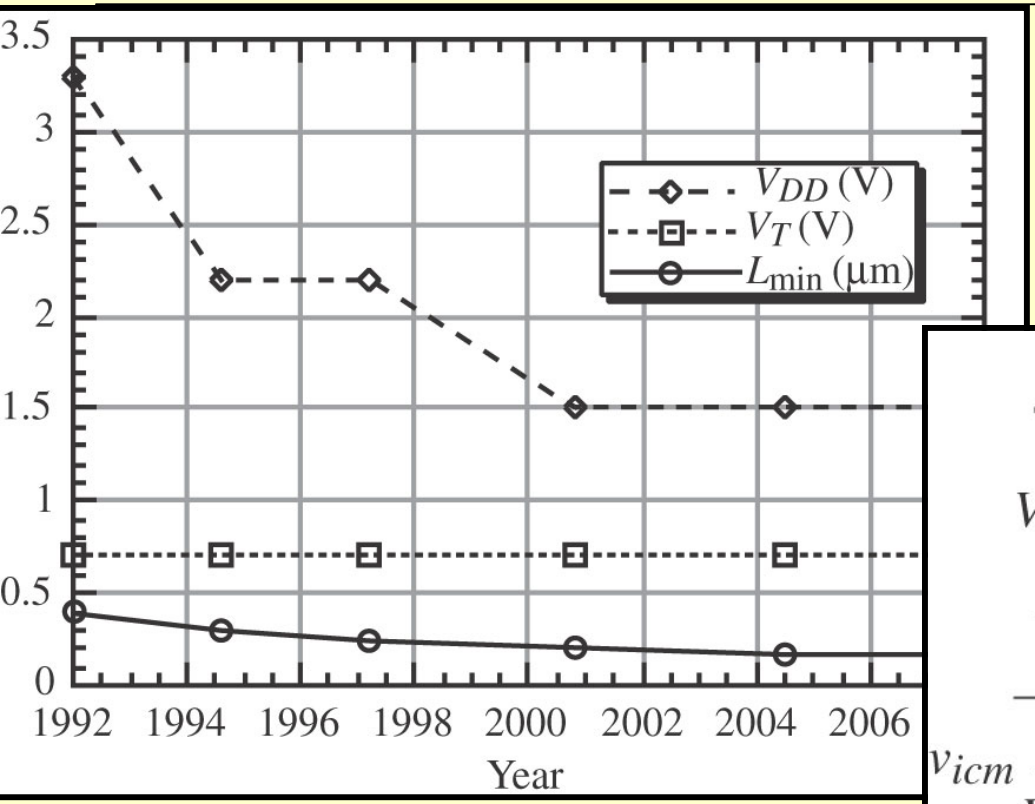
* [Grey/Meyer] reference text, Fig. 6.30

Bias circuits for high gain folded cascode

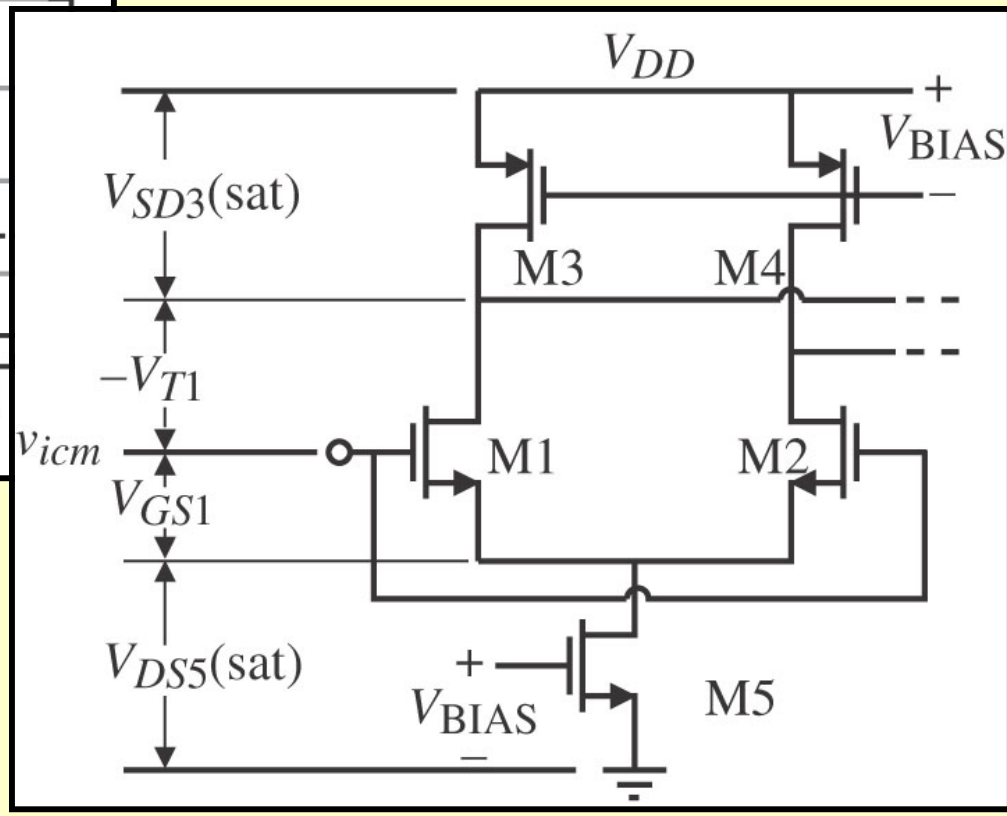


* [Grey/Meyer] reference text, Fig. 6.30

Issues w/ ICMR

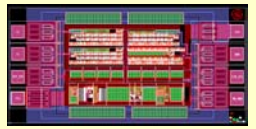


Text Figure 7.6-1



Text Figure 7.6-3

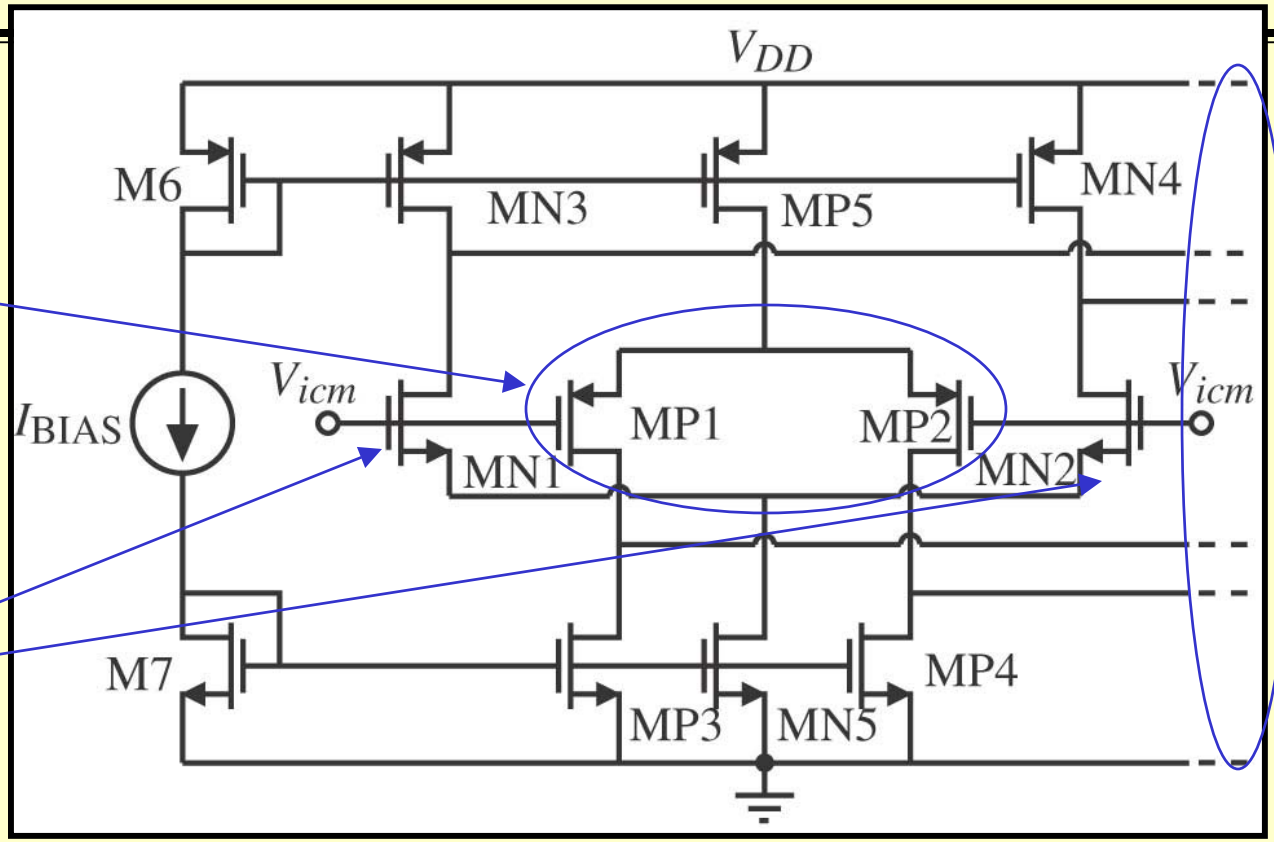
Rail-to-Rail Concept



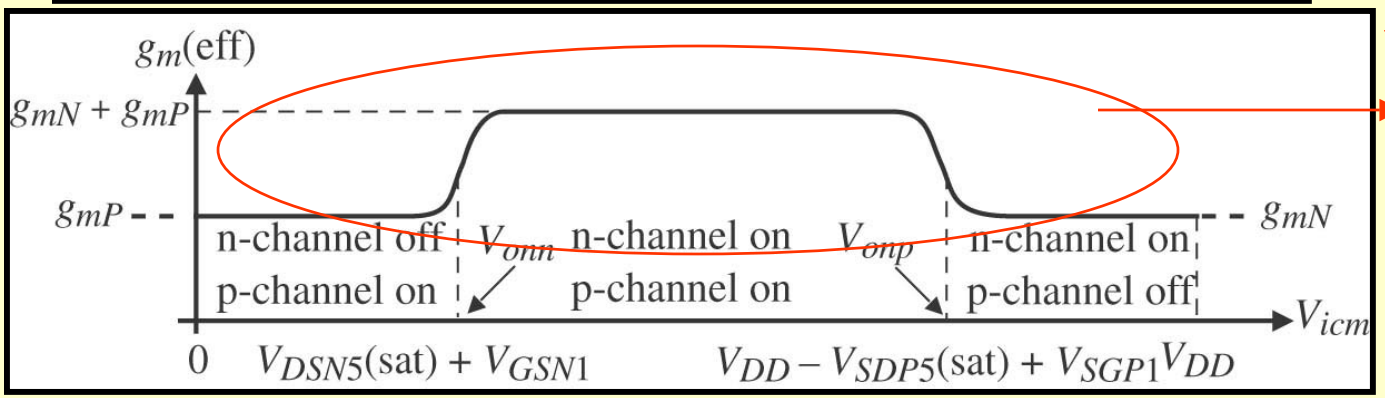
Analog IC Design

p-ch pair

n-ch pair



Mirror to output stage



Variable gain

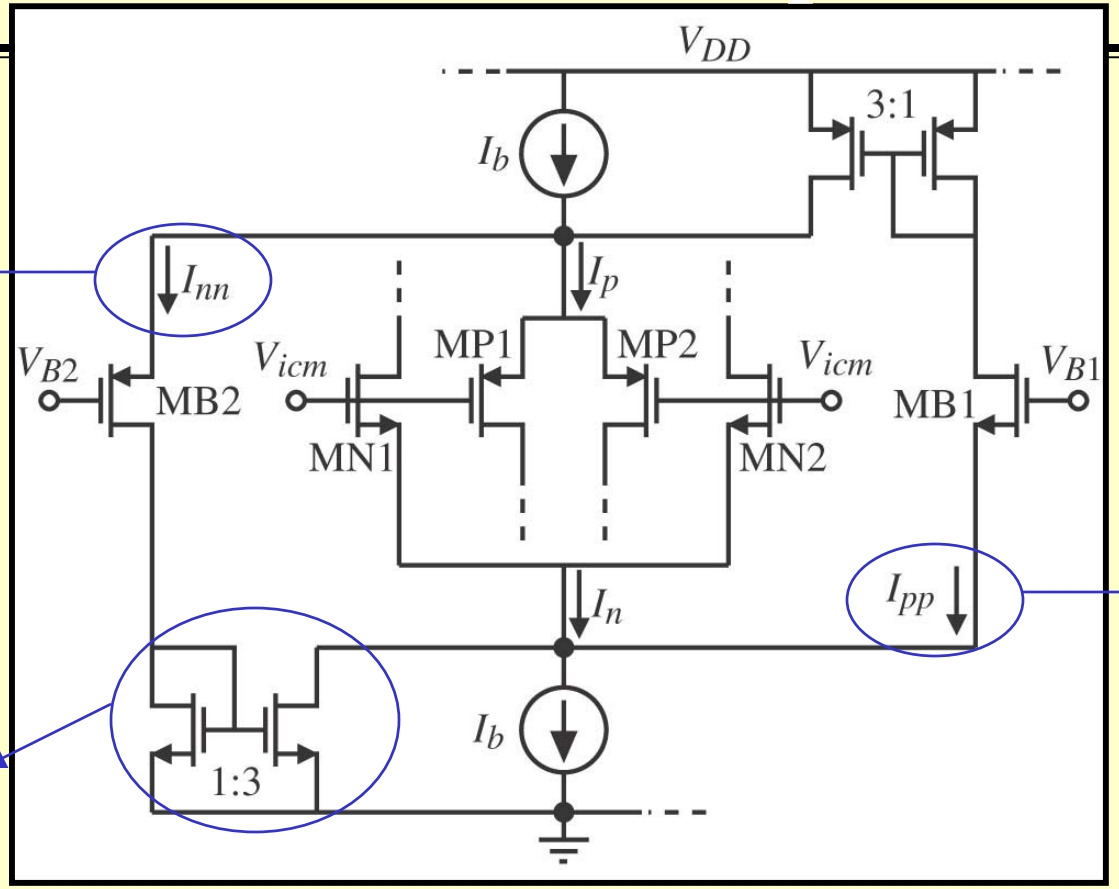
Text Figures 7.6-4 & 7.6-5

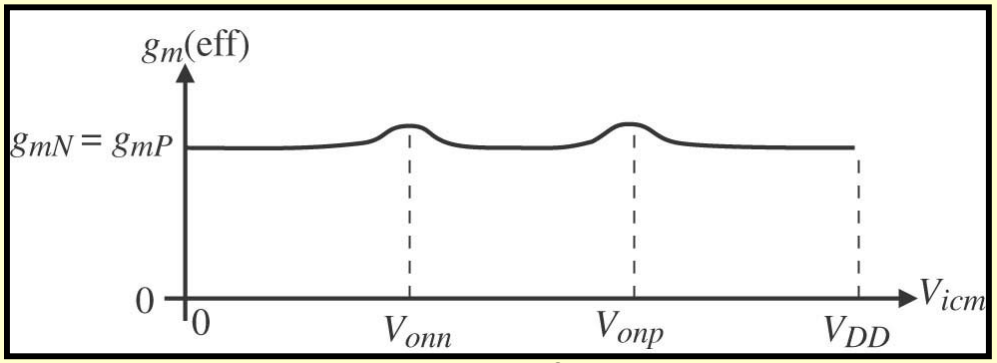
One Solution → adaptive Ib

= Ib if MP1/MP2 cut-off

Drives 4x current in n-ch when p-ch cut-off

= Ib if MN1/MN2 cut-off





Figures 7.6-6 & 7.6-7

Another Solution

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 31, NO. 7, JULY 1996

Compact CMOS Constant-g_m Rail-to-Rail Input Stage with g_m-Control by an Electronic Zener Diode

Ron Hogervorst, John P. Tero, and Johan H. Huijsing

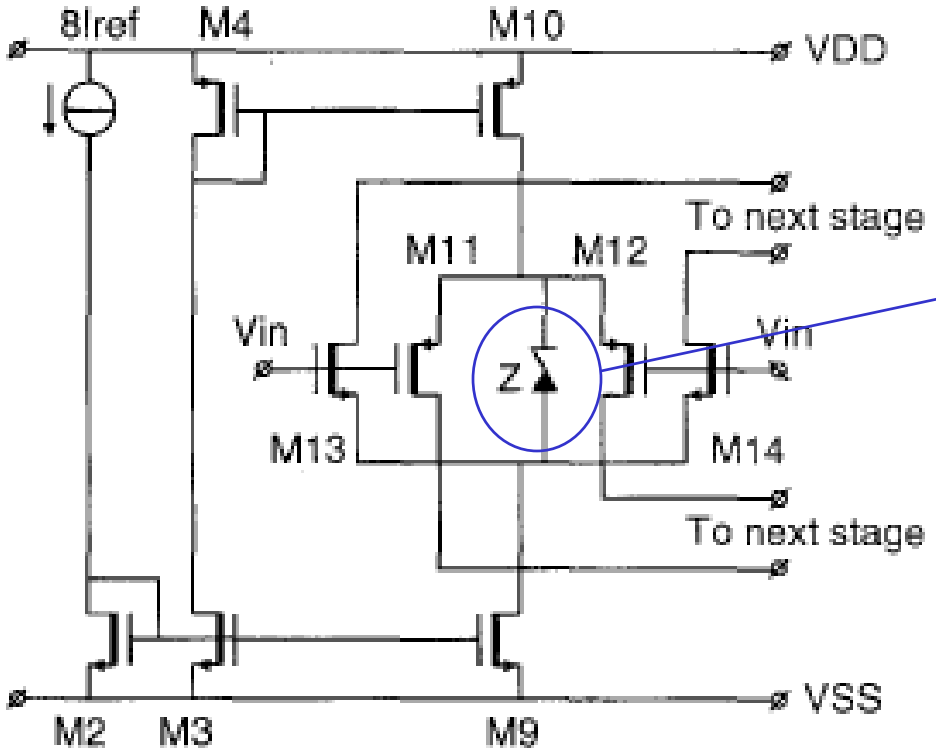
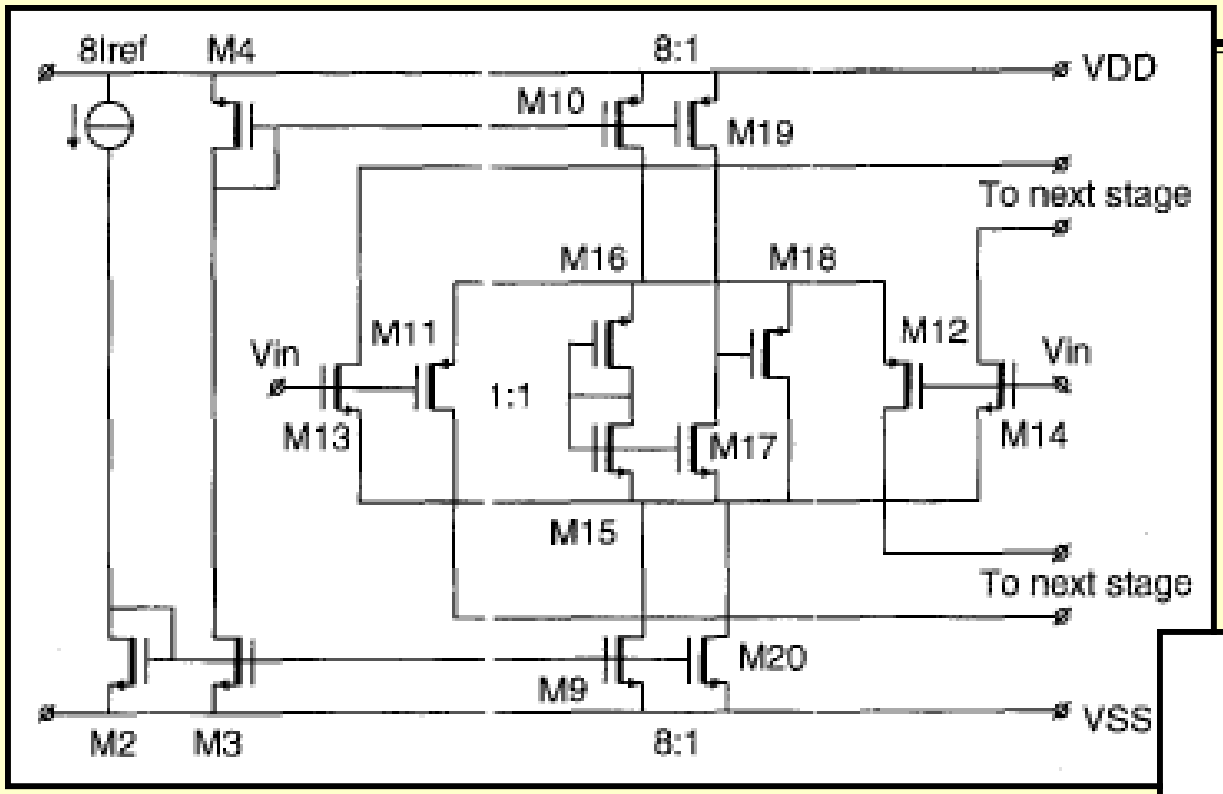
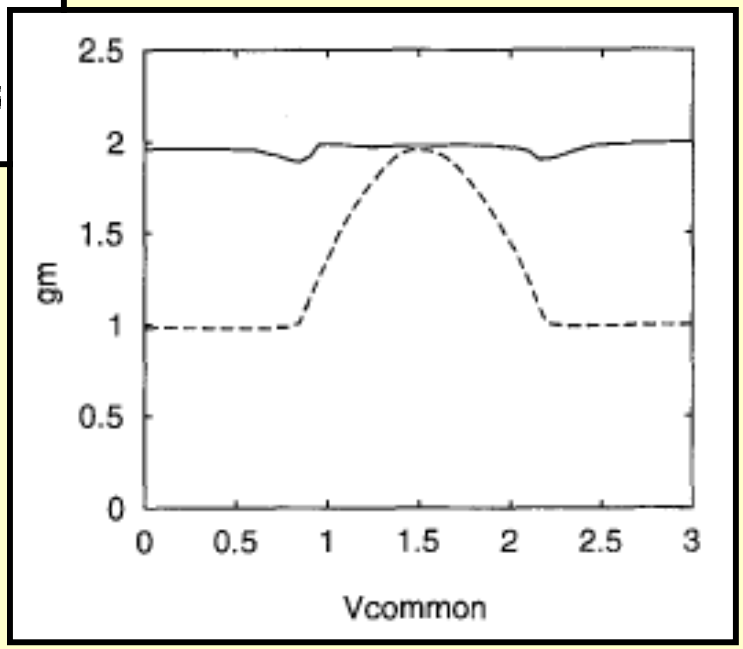


Fig. 1. Rail-to-rail input stage. The zener diode regulates the g_m at a constant value.

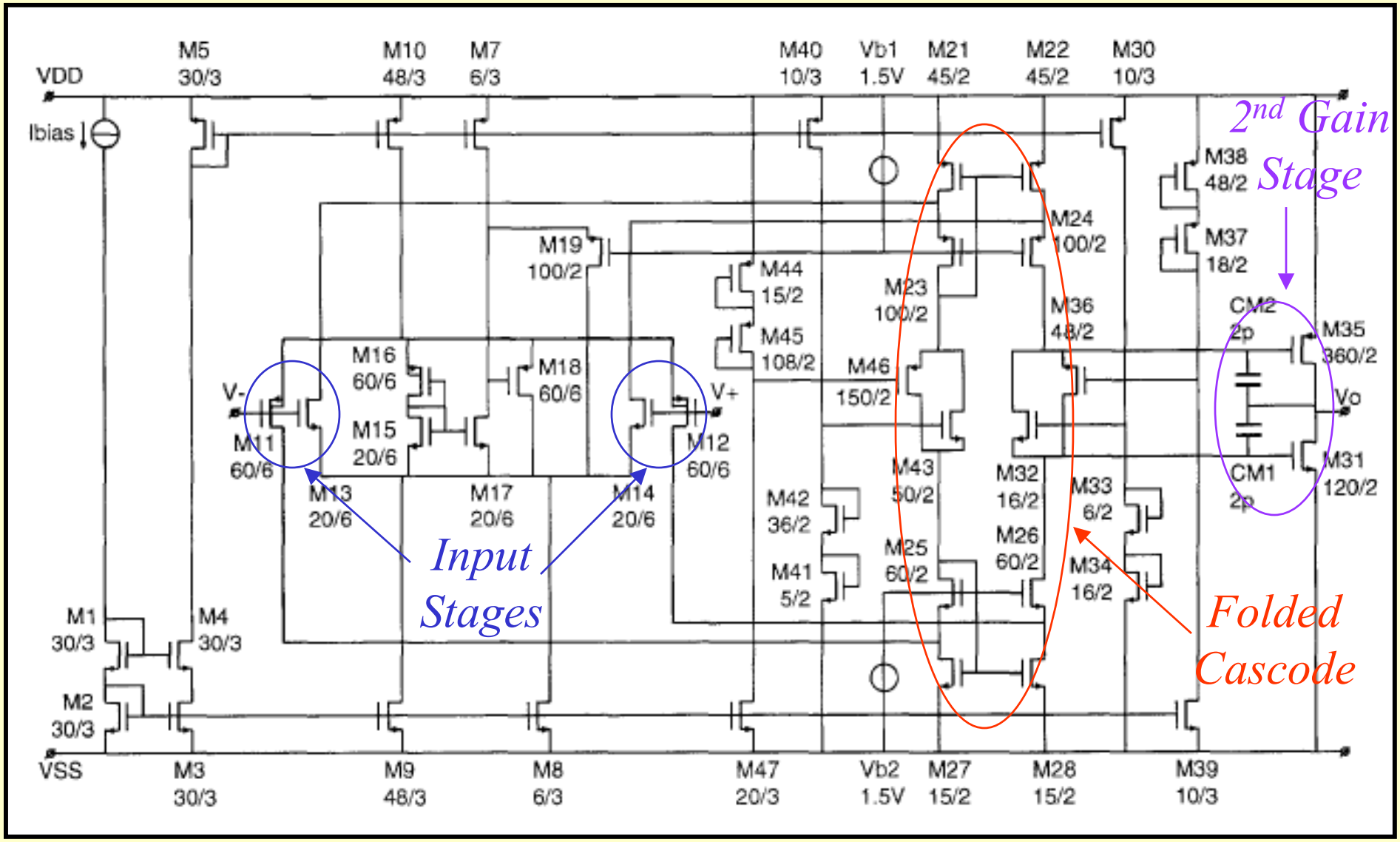
Zener absorbs 6Iref when both n & p-ch are on

Implementation

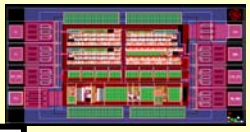




Complete Amplifier

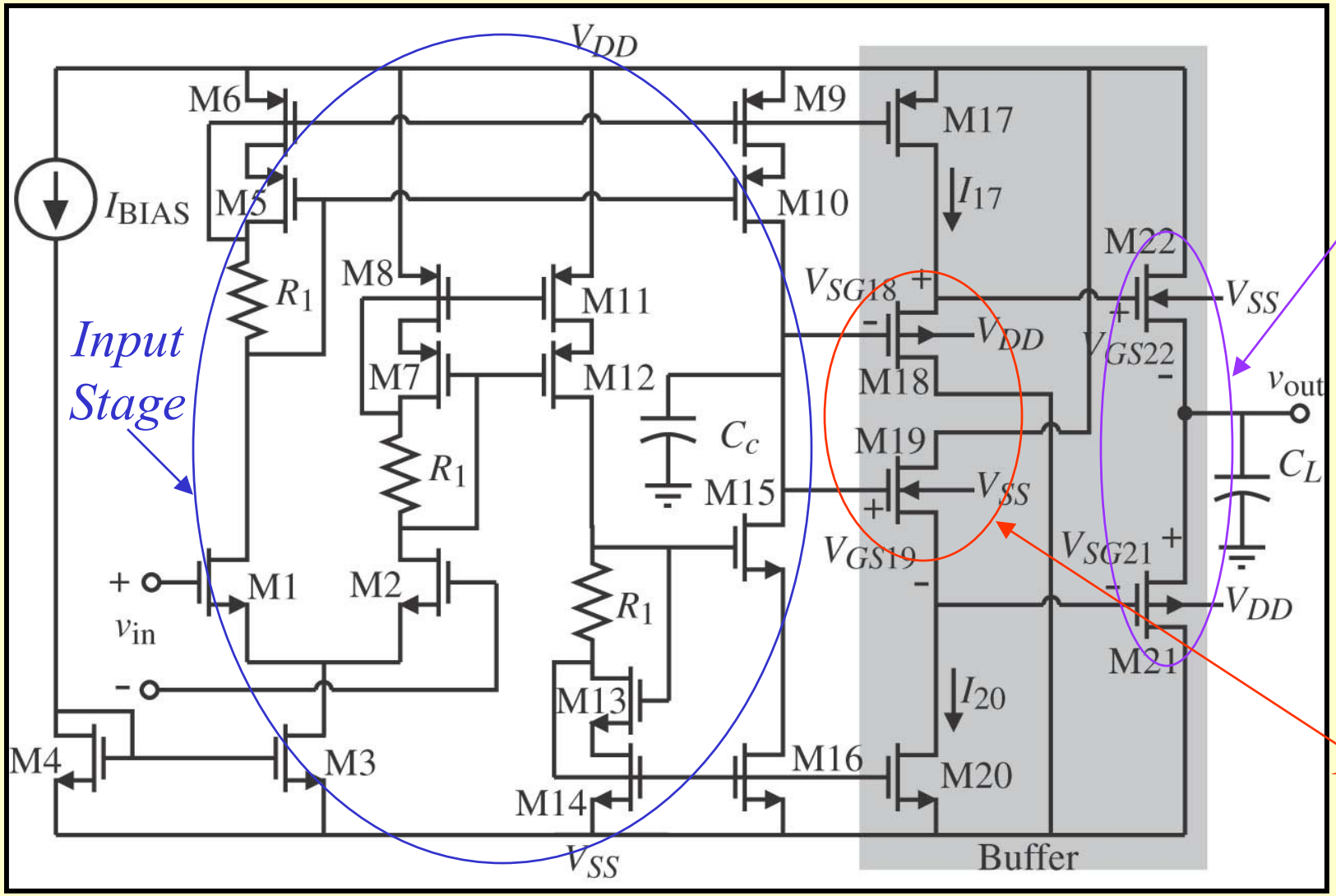


Specifications



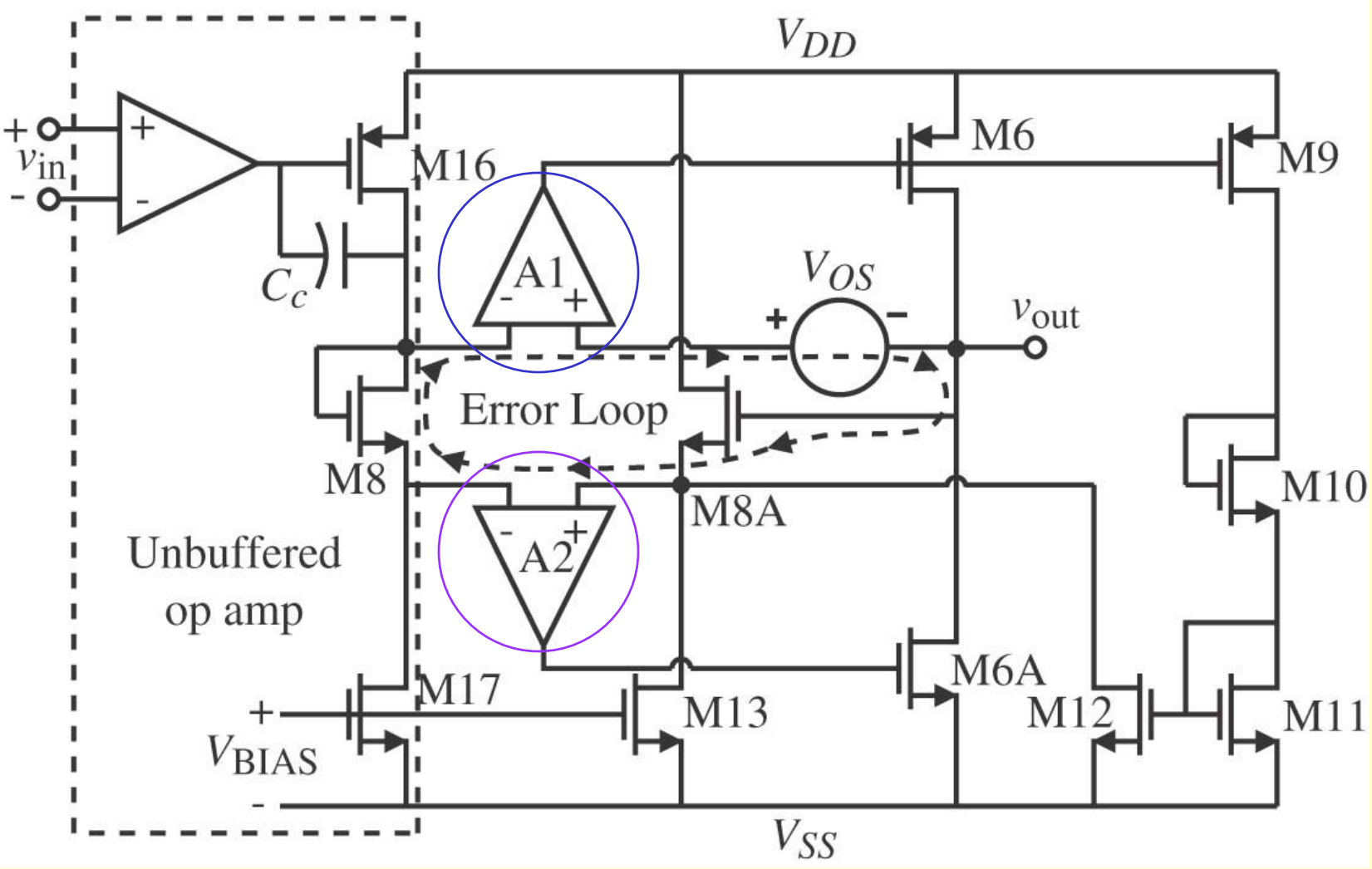
Parameter	opamp1	opamp2	unit
Die area	0.06	0.06	mm^2
Supply voltage range	2.7 to 6	2.7 to 6	V
Quiescent current	210	215	µA
Peak output current	7.5	7.5	mA
Common-mode input voltage range	V_{SS}-.5 to V_{DD}+.8	V_{SS}-.5 to V_{DD}+.8	V
Output voltage swing	V_{SS}+.1 to V_{DD}-.1	V_{SS}+.1 to V_{DD}-.1	V
Offset voltage	3	3	mV
CMRR V_{common}: from V_{SS}-0.5V to V_{SS}+.6 from V_{SS}+0.6V to V_{SS}+1.1V from V_{SS}+1.1V to V_{DD}-1.1V from V_{DD}-1.1V to V_{DD}-0.5V from V_{DD}-0.5V to V_{DD}+.8V	 80 43 74 43 70	 80 43 74 43 70	dB
Open-loop gain	83	85	dB
Unity-gain frequency	1.7	1.9	MHz
Unity-gain phase margin	76	80	°
Slew-rate	8	8	V/µs
Settling-time (1%, Vstep=1V)	0.3	0.3	µs

Class A/B Output Stage



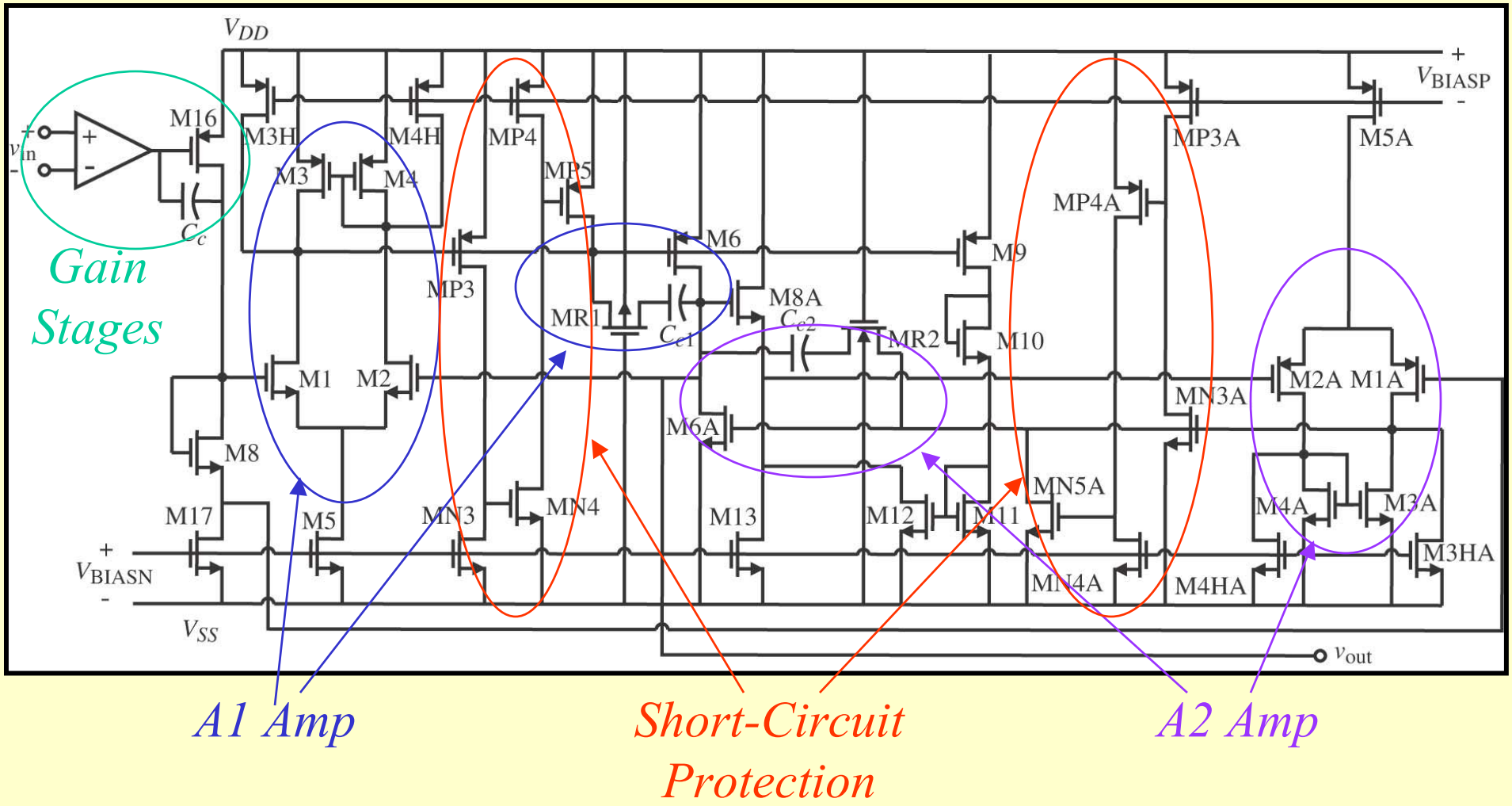
Text Figure 7.1-1

Very Low Rout: Feedback



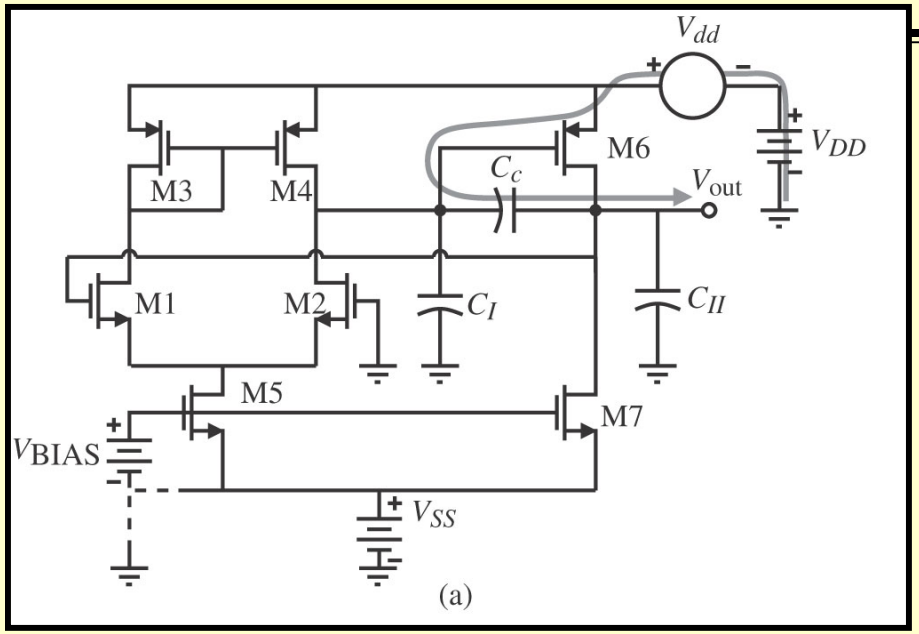
Text Figure 7.1-6

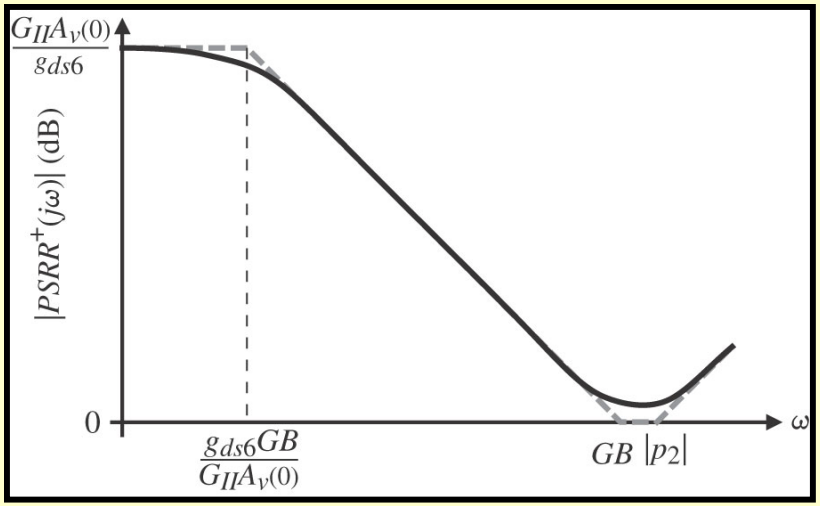
Complete Low Rout Amp

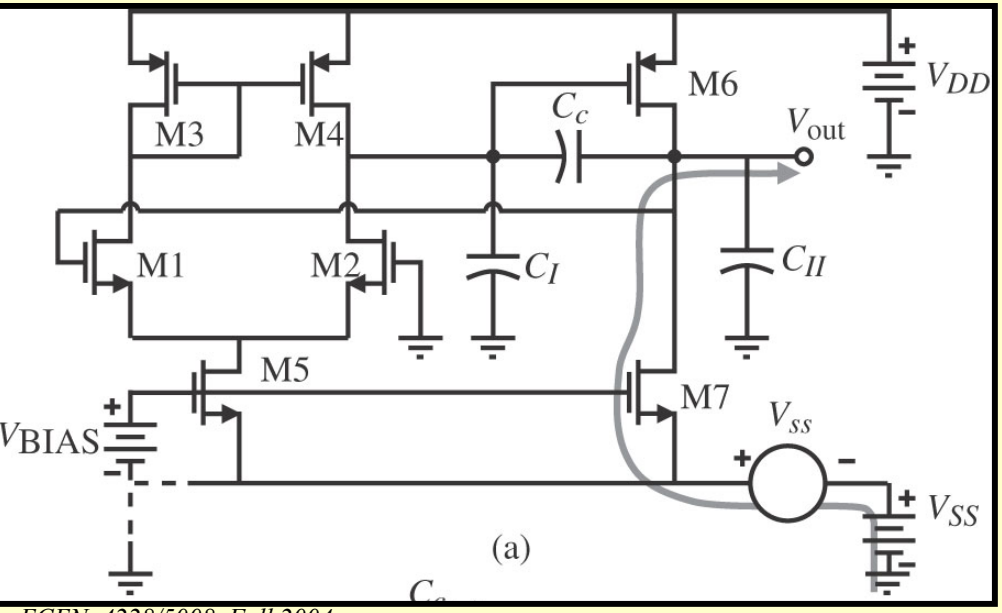


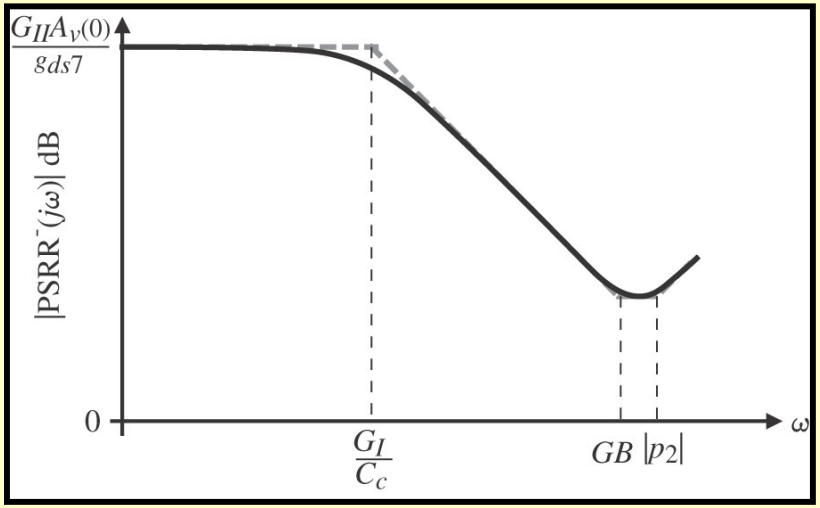
Text Figure 7.1-8

Power Supply Rejection Ratio



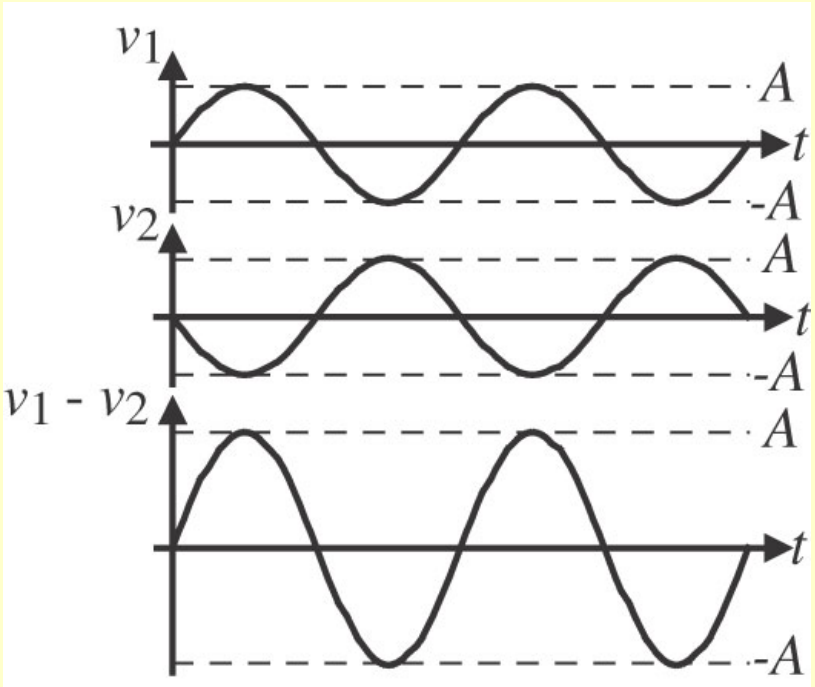




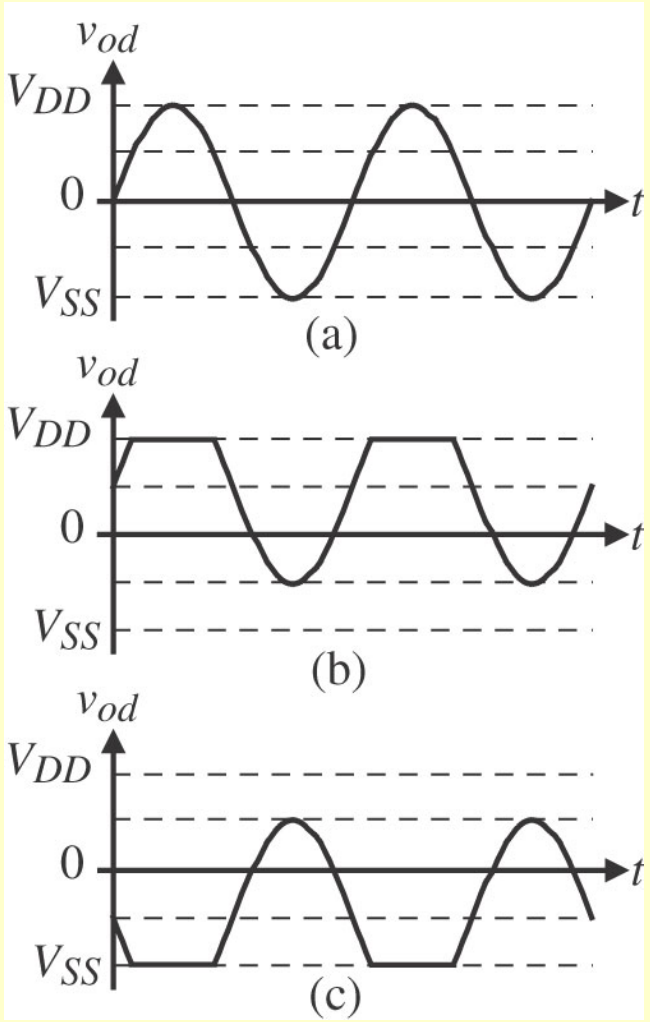


Text Figures 6.4-2 – 6.4-5

Fully Differential

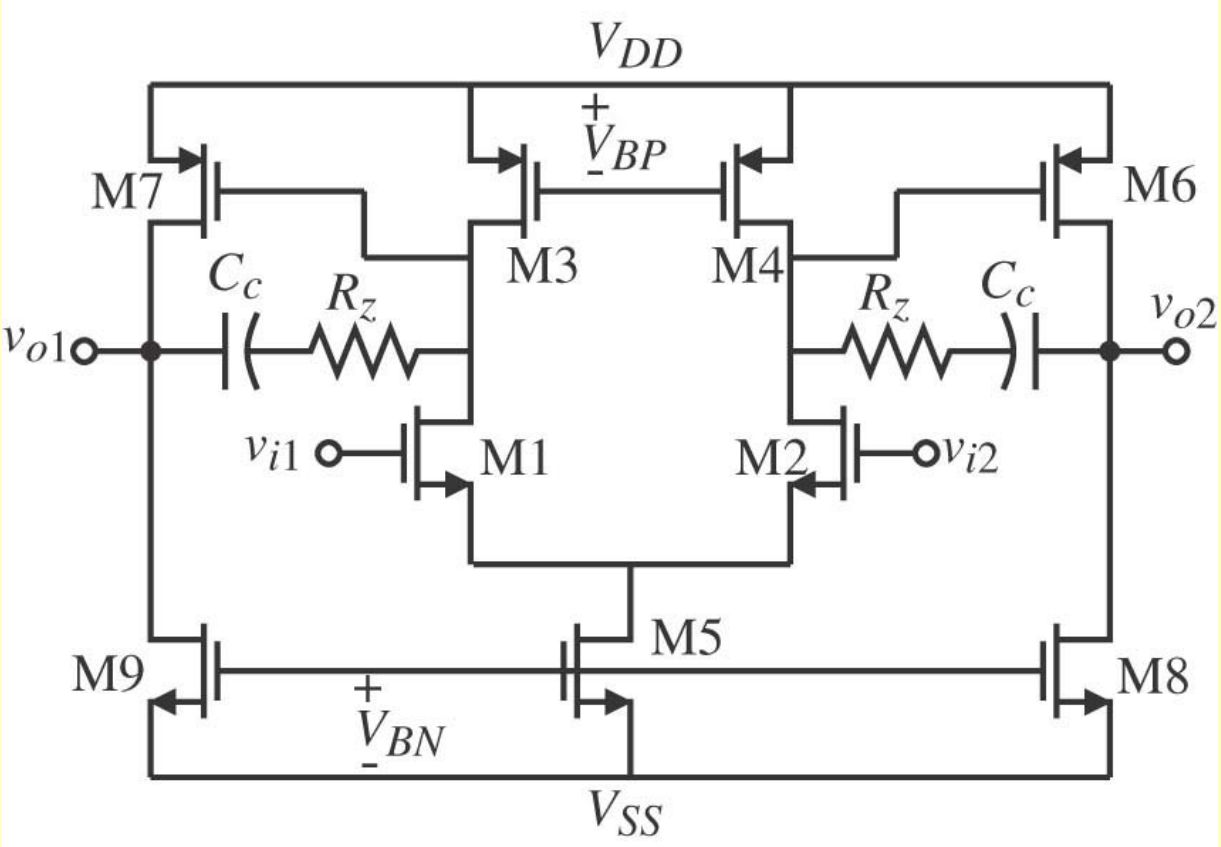


Text Figure 7.3-1



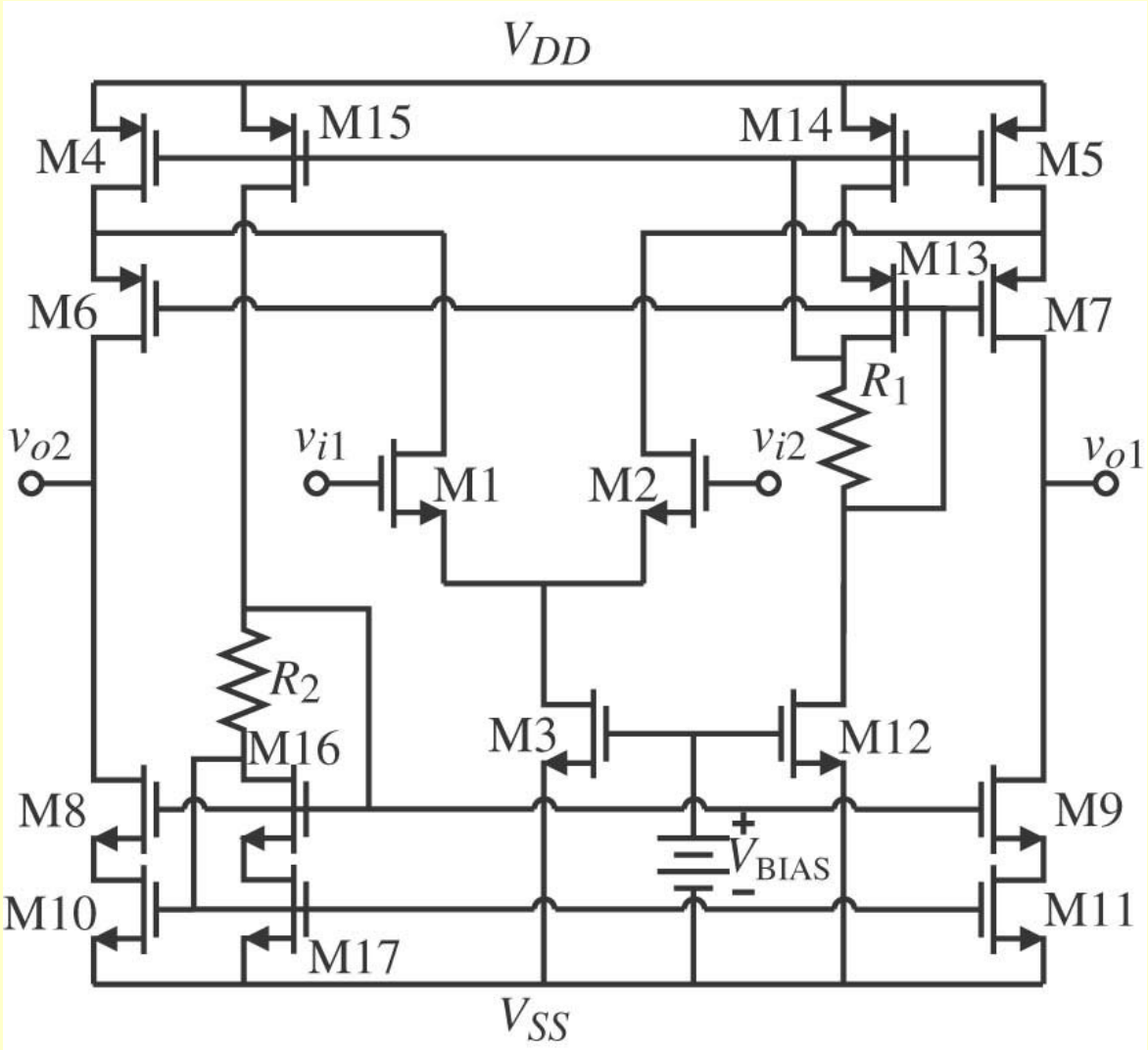
Text Figure 7.3-2

2-stage Miller Differential Out



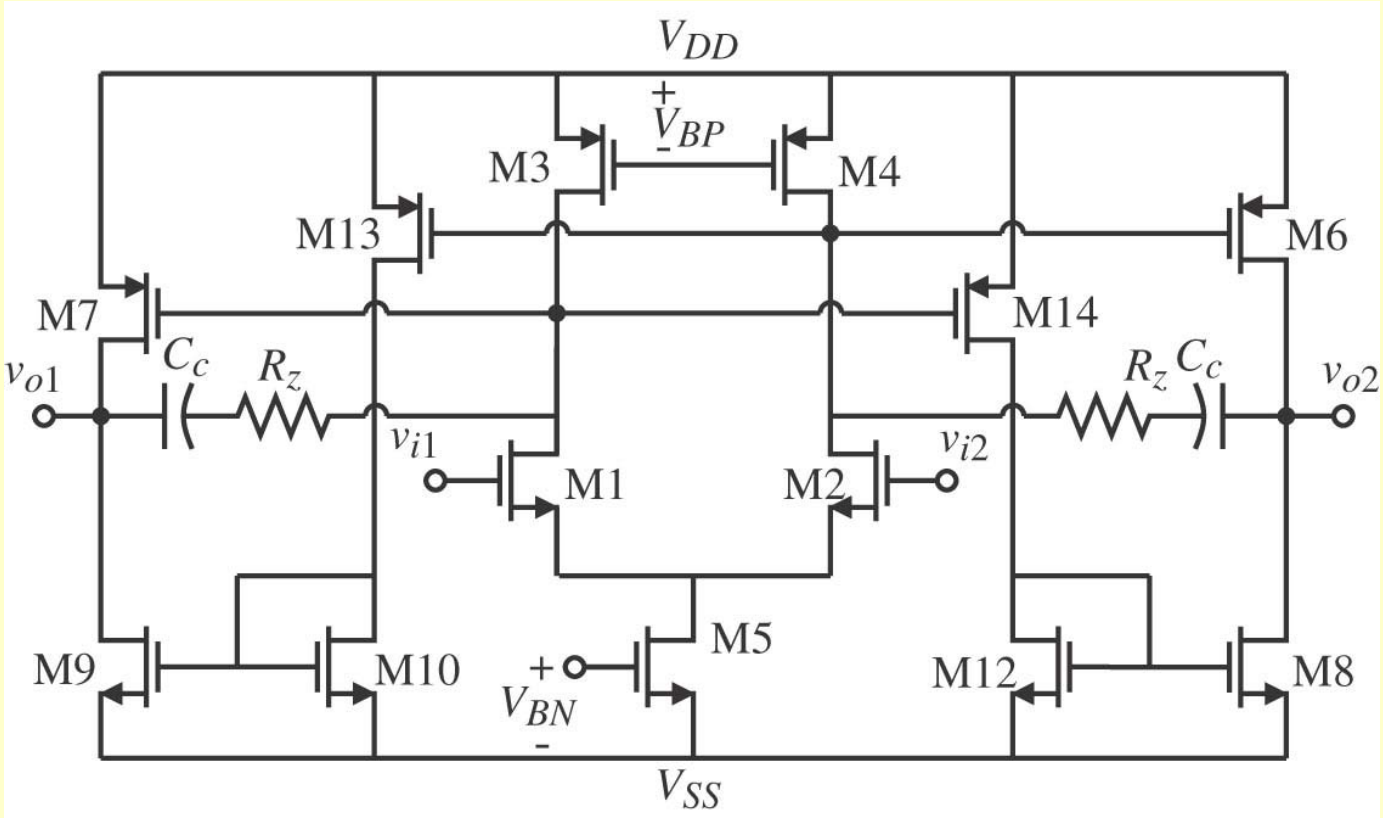
Text Figure 7.3-3

Folded-Cascode Differential Out



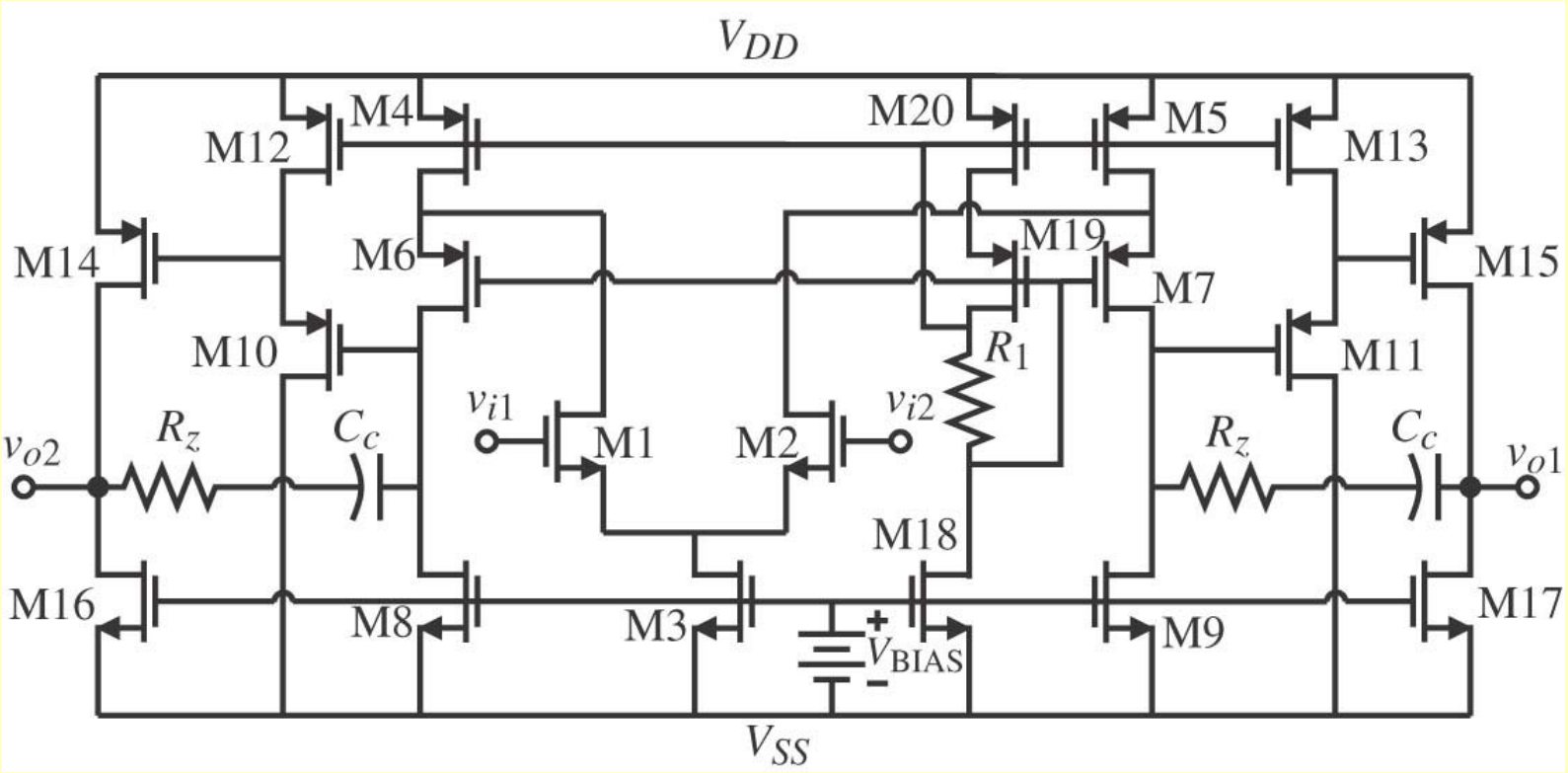
Text Figure 7.3-5

2-stage, push-pull, diff-out



Text Figure 7.3-6

2-stage, folded cascode, diff-out



Text Figure 7.3-7

1-stage, cascode, symmetrical, cross-coupled (high SR)!

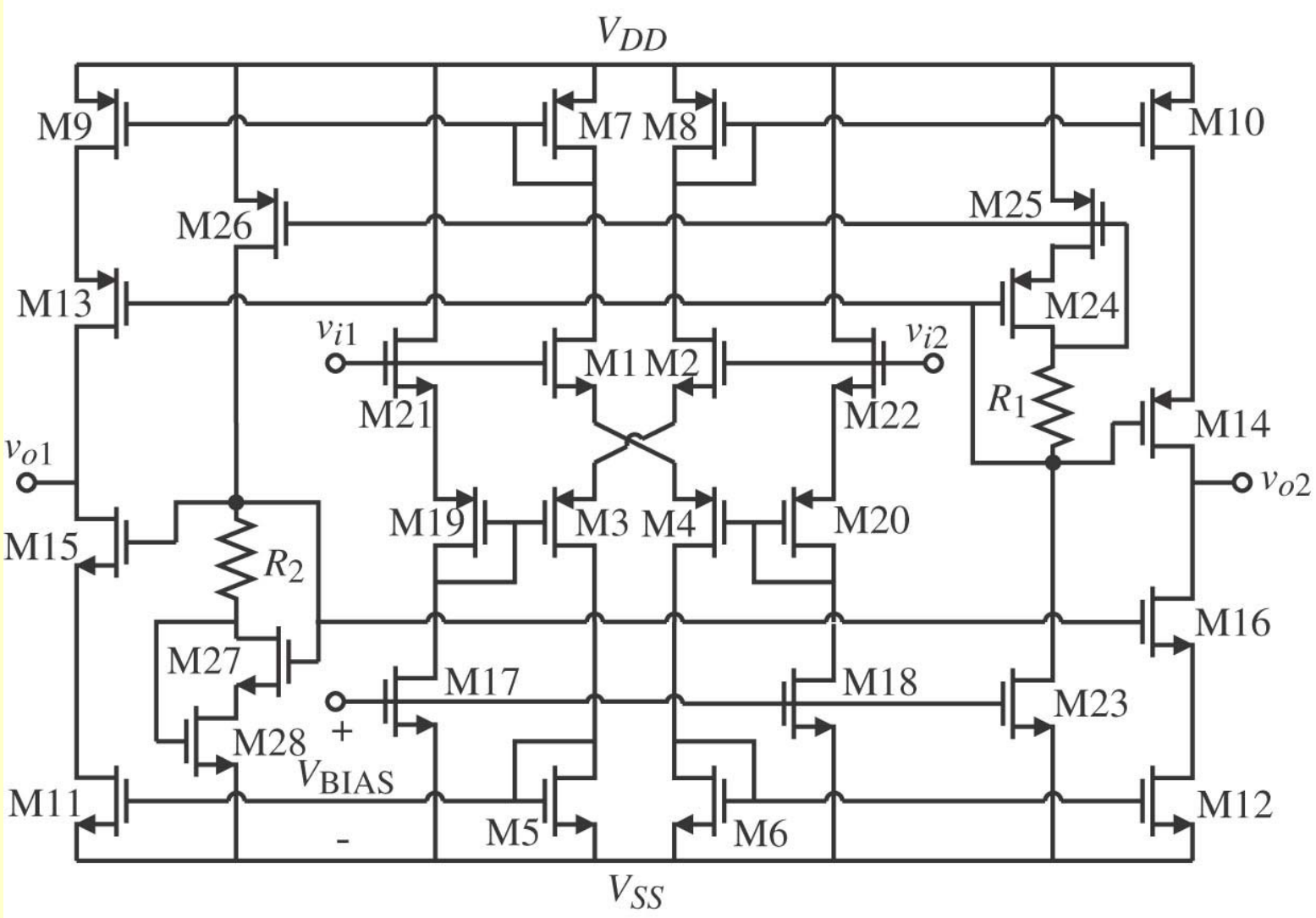
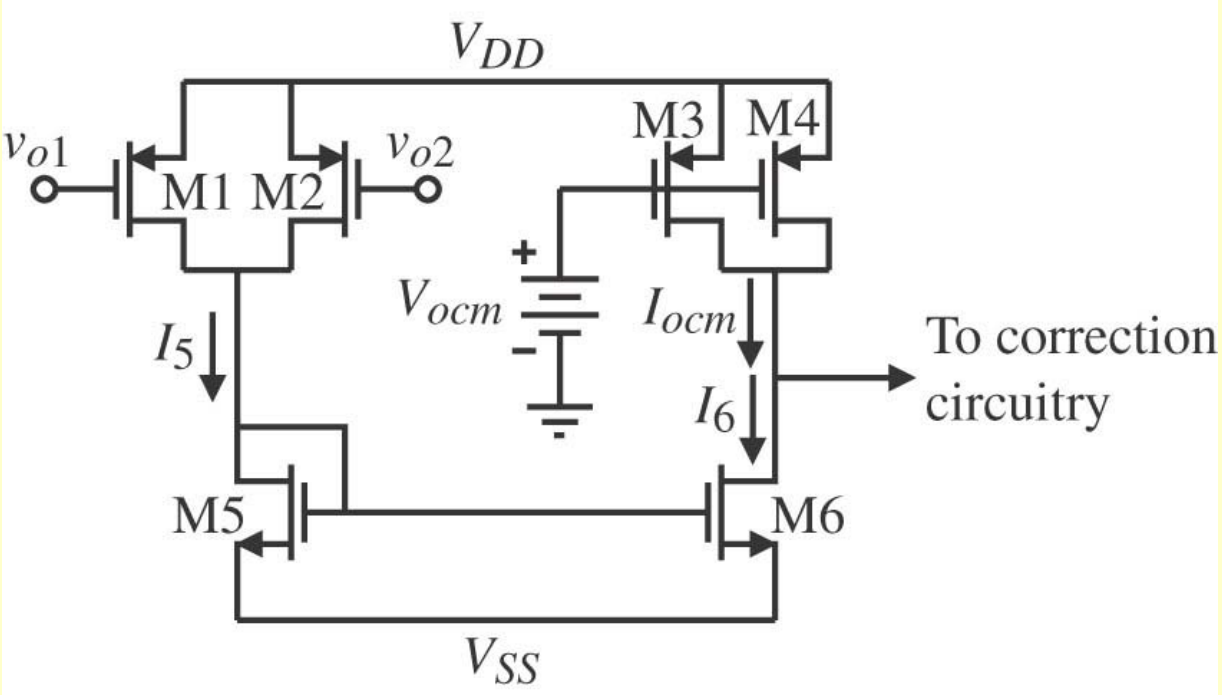


Figure 7.3-10

CMFB

Common-mode-feedback



Text Figure 7.3-13