
CMOS Voltage Comparator

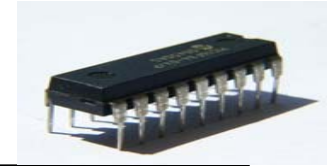
Advanced VLSI Design Lab, IIT Kharagpur



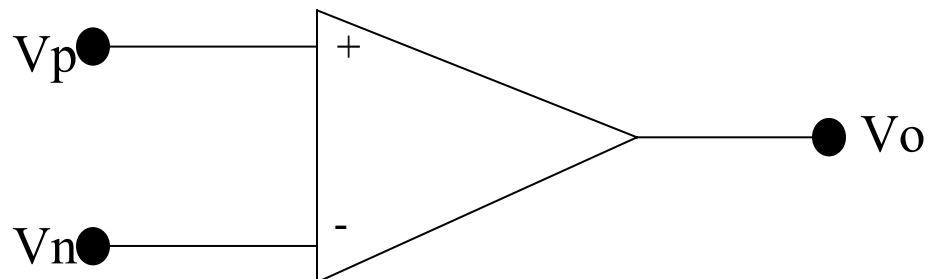
Ramen Dutta

Electronics & Electronic Communication Engg.,
Indian Institute of Technology Kharagpur

Voltage Comparator Requirement

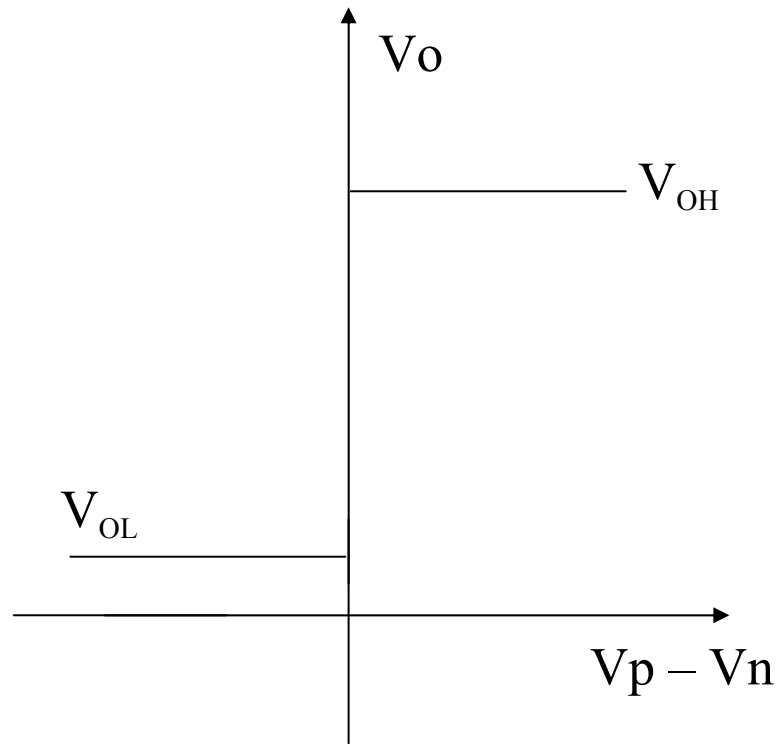
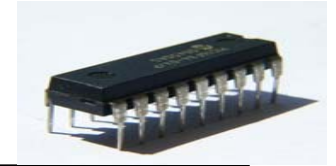


- ❑ Compares one analog signal (voltage) to another analog voltage or a reference voltage and gives a binary output depending on the comparison.
- ❑ Widely used in Analog to Digital Converter (ADC). Comparator is considered as 1-bit ADC.
- ❑ Also used in detection purpose of low swing and high speed digital bus.



Symbol of a comparator

Comparator Static Characteristics



Static Characteristics :

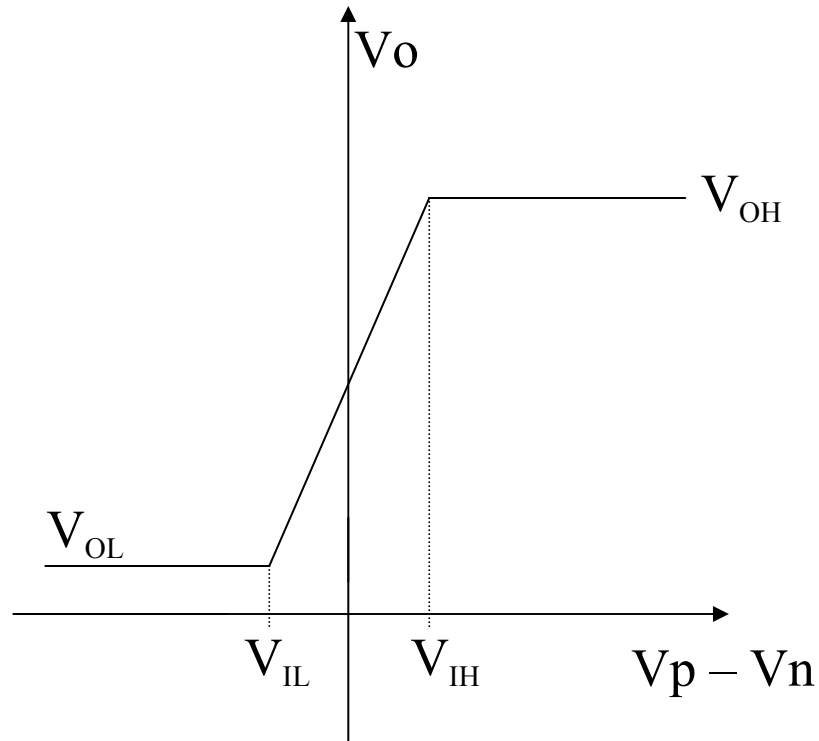
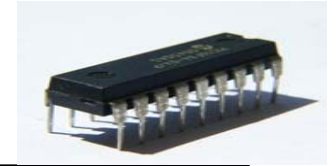
- **Gain**
- **Output High and Low states (V_{OH} and V_{OL})**
- **Input Resolution**
- **Offset**
- **Noise**

Ideal Voltage Transfer (Gain \sim infinity)

$$A_V = \lim(\Delta V \rightarrow 0) \{ (V_{OH} - V_{OL}) / \Delta V \}$$

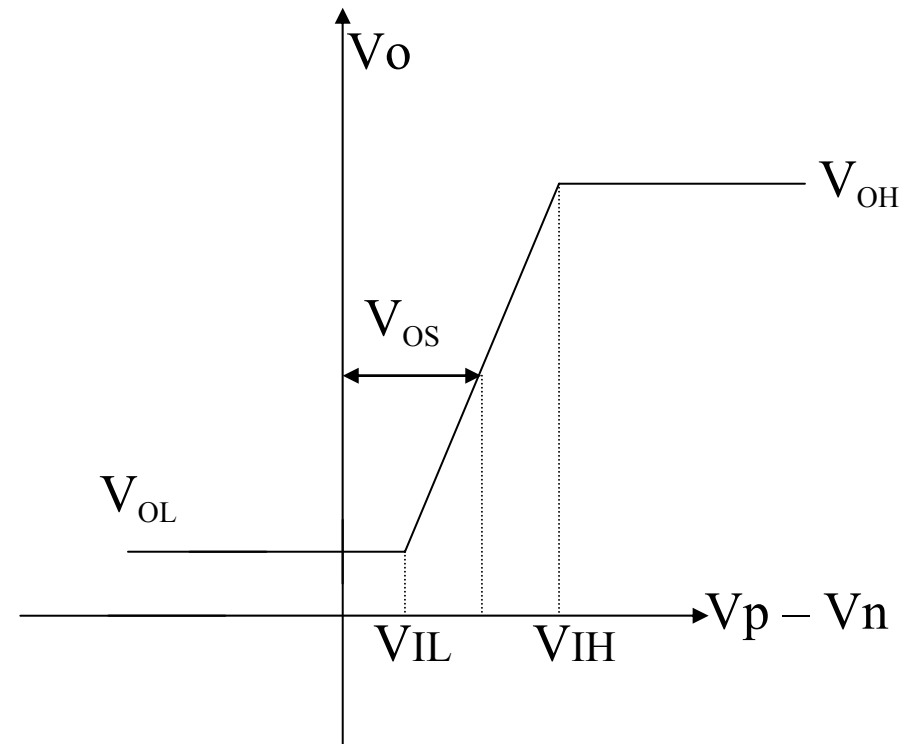
Where ΔV is the input voltage change

Comparator Static Characteristics



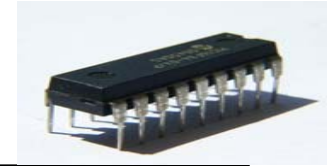
Voltage transfer curve with finite gain.

$$A_V = \{ (V_{OH} - V_{OL}) / (V_{IH} - V_{IL}) \}$$



Voltage transfer curve with input-offset voltage.

Static Characteristics



- **Offset:** There are two types of offset, 1. Systematic offset. 2. Random offset.

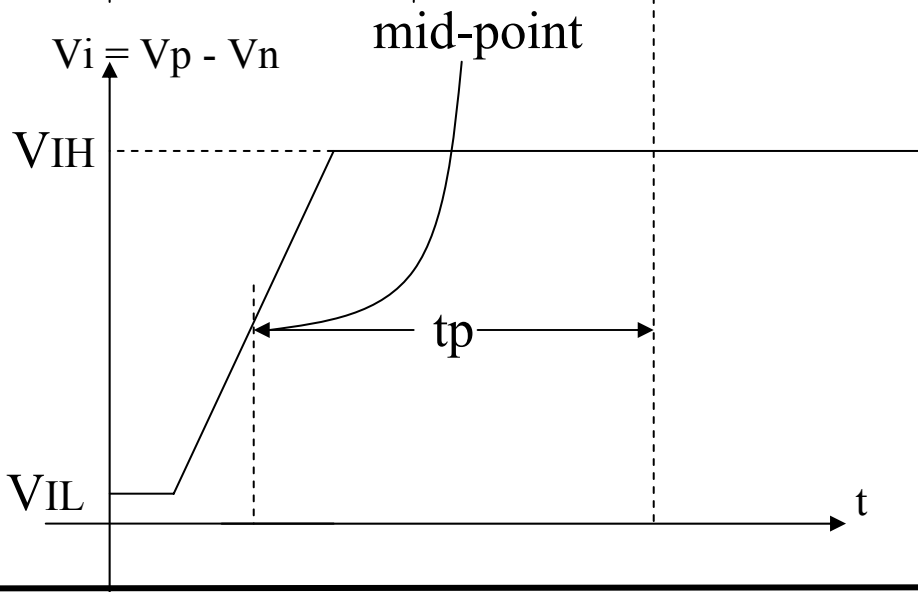
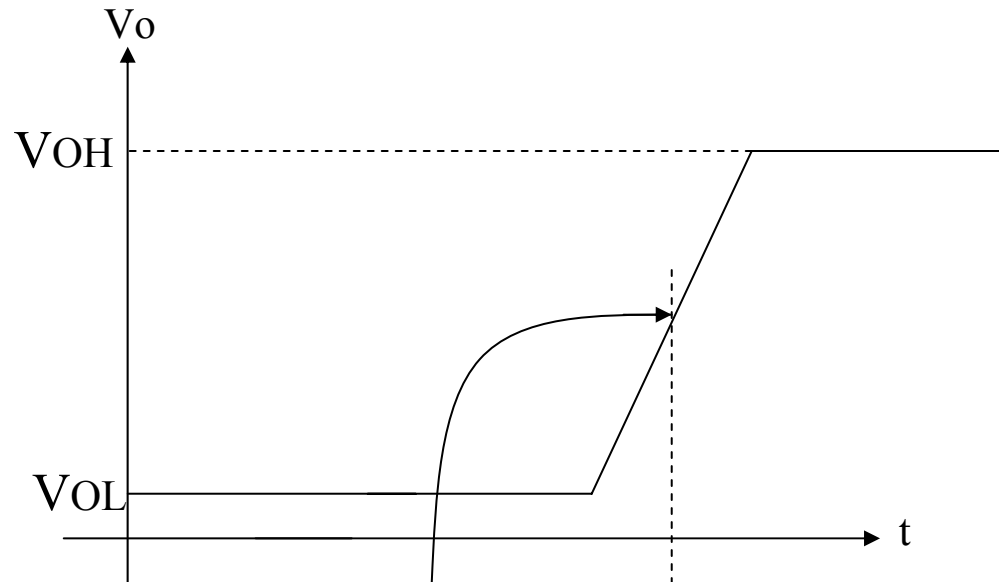
Effect of offset can be reduced but can not be totally avoided

- **Resolution :** It is the input voltage change necessary to make the output swing to valid binary states.

- **Noise:** Noise leads to an uncertainty in the transition in the voltage transfer curve. This uncertainty in the transition region can lead to jitter or phase noise.

- **Input Common Mode Range (ICMR):** This is the input voltage range where the comparator function normally (i.e. meets all other required specification).

Dynamic Characteristics – Propagation Delay

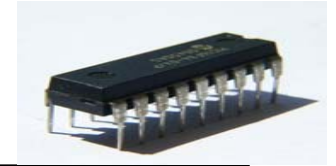


Dynamic Characteristics :

- Propagation Delay
- Slew Rate

Total Propagation delay time =
(Rising propagation delay time +
Falling propagation delay time) / 2

Propagation Delay and Slew Rate



- **For a Single Pole System:**

$$A_v(s) = A_v(0) / (s\tau + 1) \quad \longrightarrow \quad V_{out}(t) = A_v(0) [1 - \exp(-t/\tau)] V_{in}(\min)$$

$$V_{out} = (V_{OH} - V_{OL}) / 2 \quad \text{at} \quad t = t_p$$

Therefore if $V_{in}(\min)$ is applied, $t_p = \tau \ln(2) = 0.693\tau$

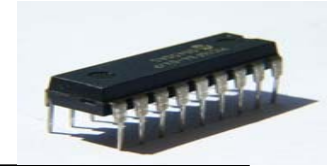
Overdrive applied to the input \uparrow \longrightarrow Propagation Delay Time \downarrow

- For very high input voltage the comparator enters into the large-signal mode of operation. For this case slew-rate defined by the maximum current available will define the propagation delay.

$$i = C (dv/dt)$$

$$t_p = (V_{OH} - V_{OL}) / 2 * SR$$

Different Comparator Types



❑ **Open loop comparator.**

- These comparator basically are operational amplifier without compensation. Comparators are required to have lesser gain and higher bandwidth than opamps.

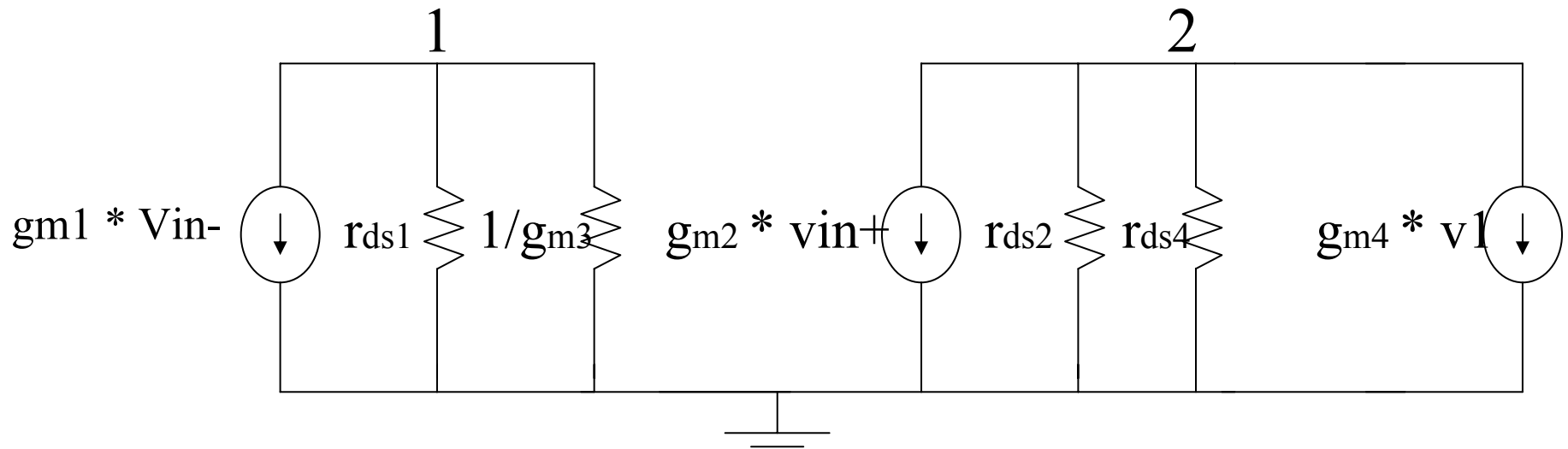
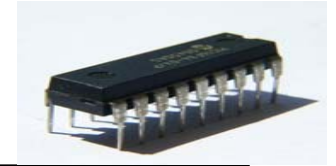
❑ **Regenerative Comparator.**

- These comparator uses positive feedback like a latch to compare to signals.

❑ **High Speed Comparator.**

- These comparators are a combination of above two which leads to a faster response.

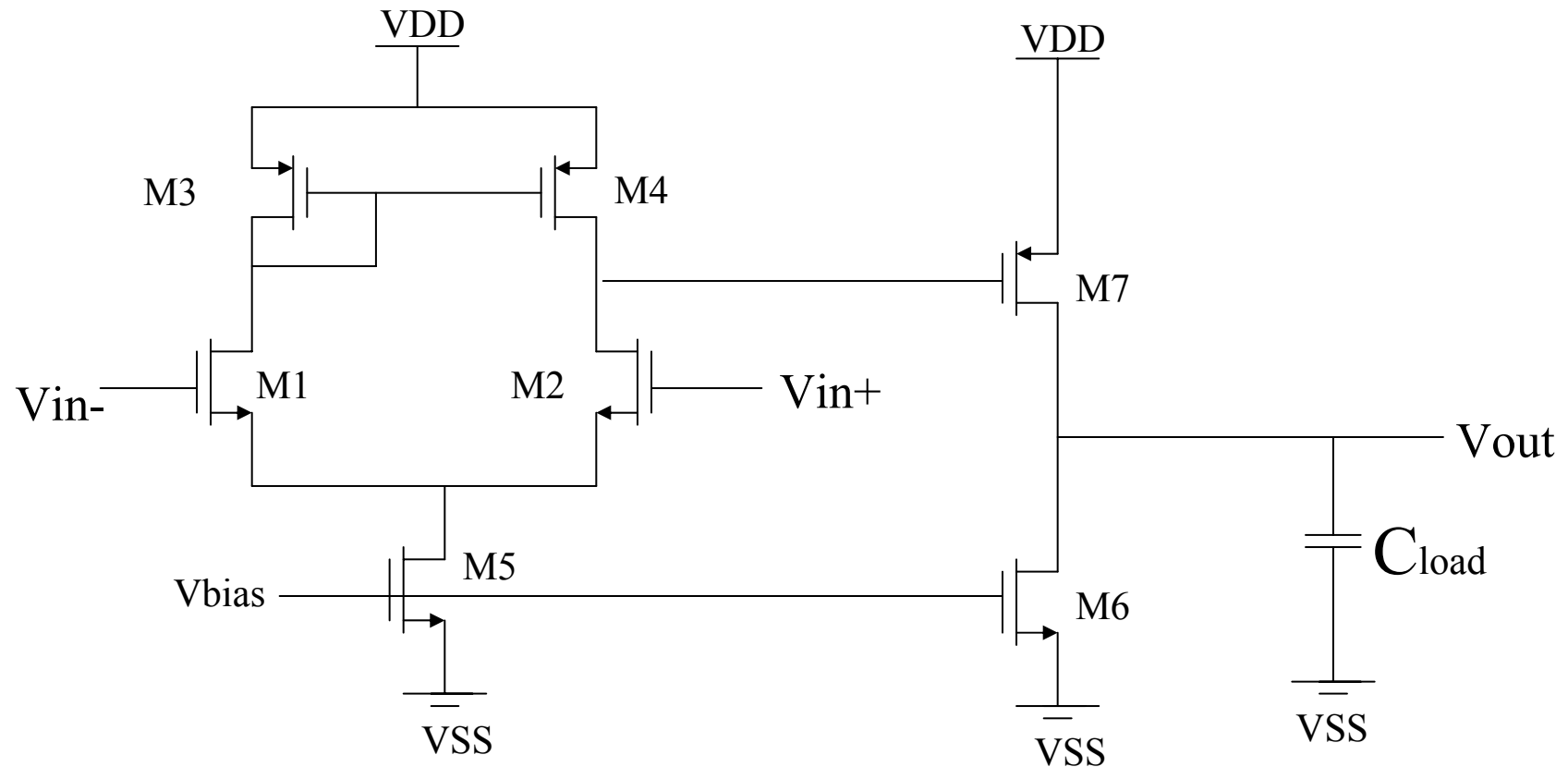
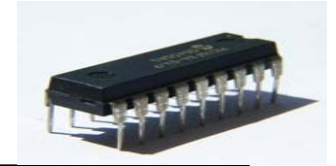
Small Signal Model of Diff. Amp.



Note: $g_{m1} = g_{m2}$; $g_{m3} = g_{m4}$

Gain : $A_v = g_{m1} (r_{ds2} || r_{ds4})$

Two Stage Comparator

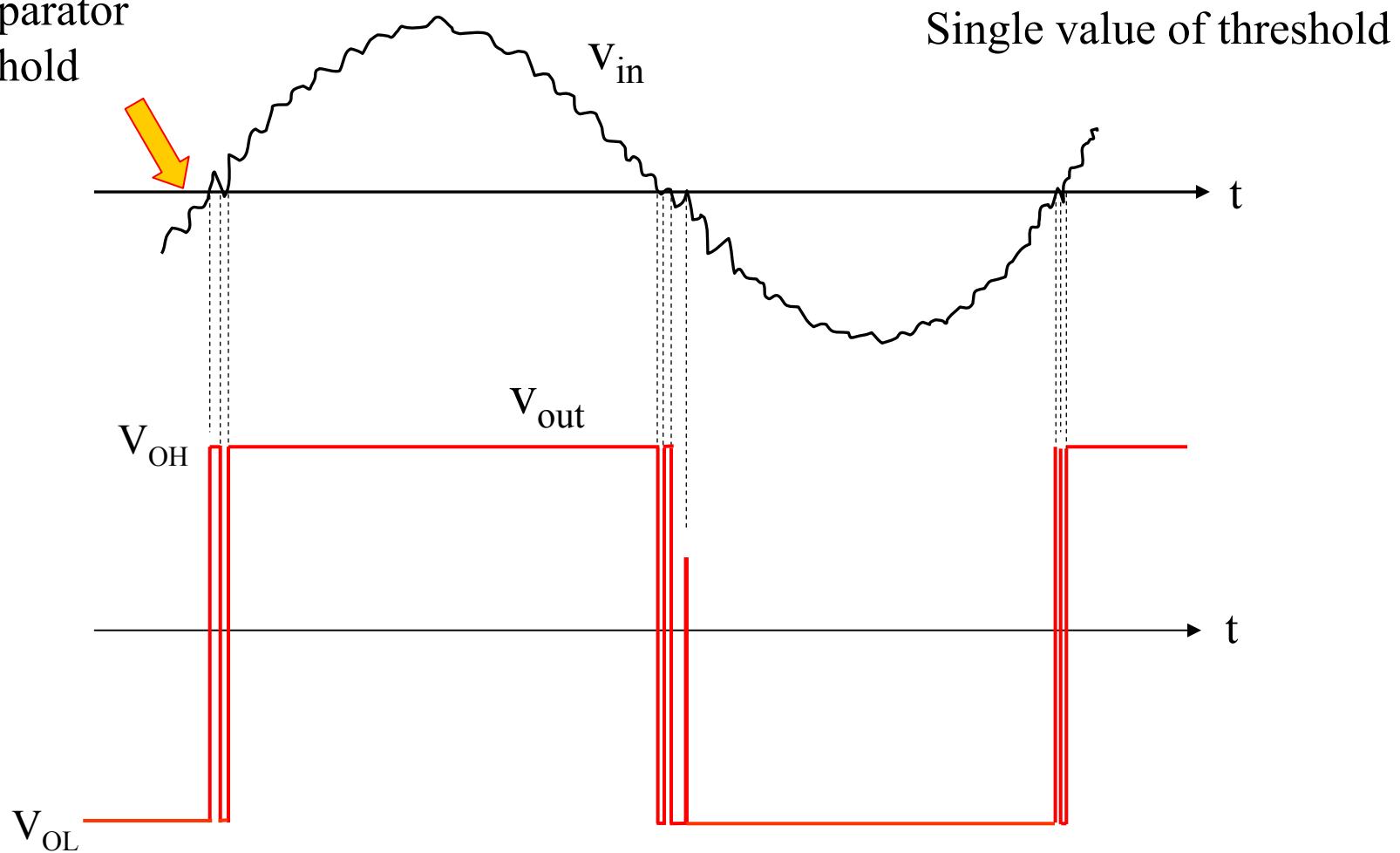


$$\text{Gain, } A_v = g_{m1} (r_{ds2} \parallel r_{ds4}) * g_{m7} (r_{ds6} \parallel r_{ds7})$$

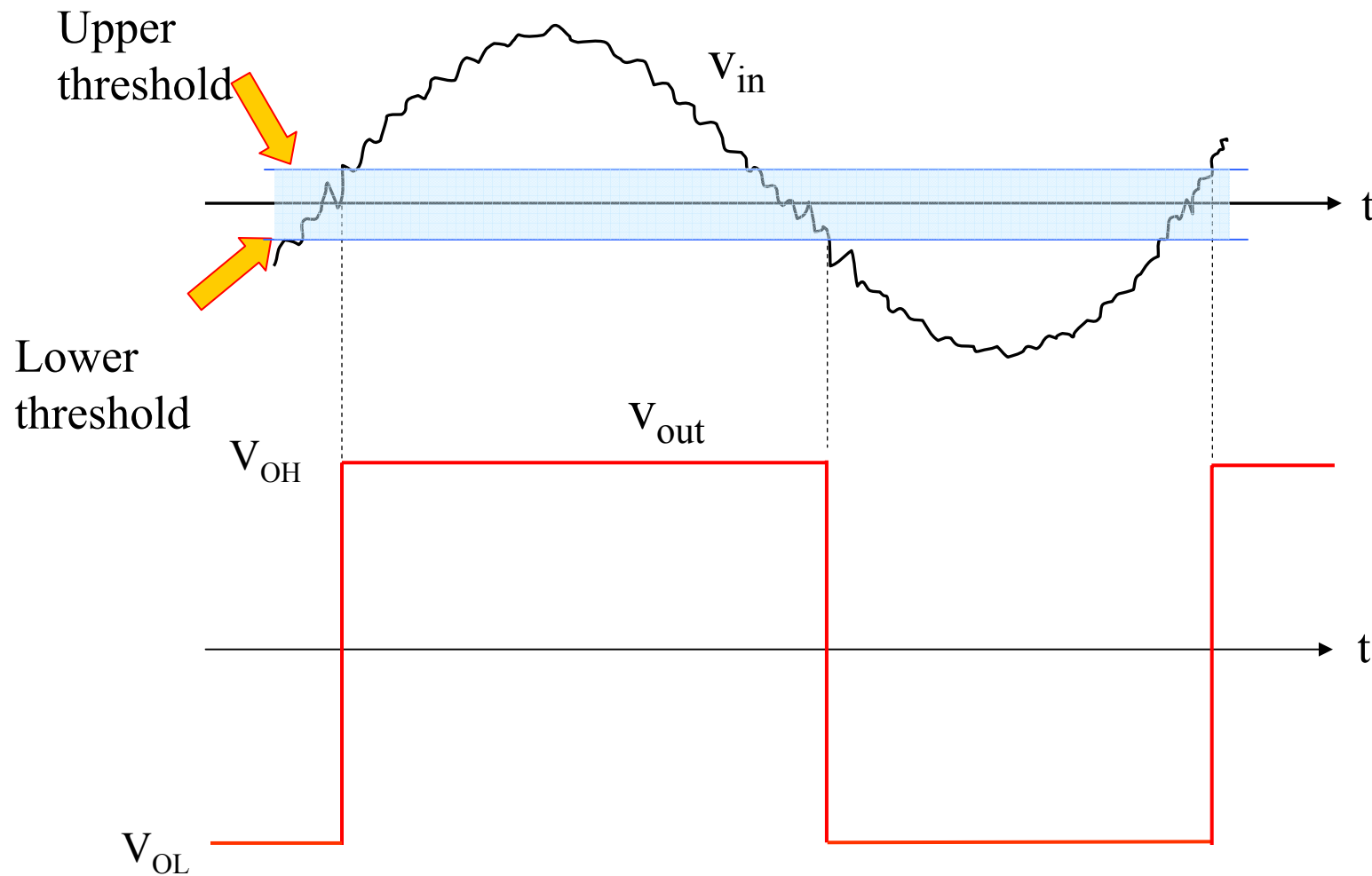
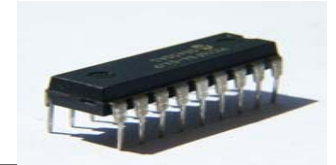
Response of a Comparator in a Noisy Environment



Comparator
threshold

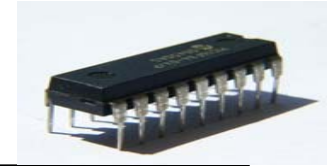


Comparator with Hysteresis in a Noisy Environment



Different trip points for rising and falling V_{in}

Characteristics of a Comparator with Hysteresis



- ❖ Comparator threshold changes with the state of the output
 - * One trip point (V_{TRP+}) for V_{OL}
 - * Another trip point (V_{TRP-}) for V_{OH}

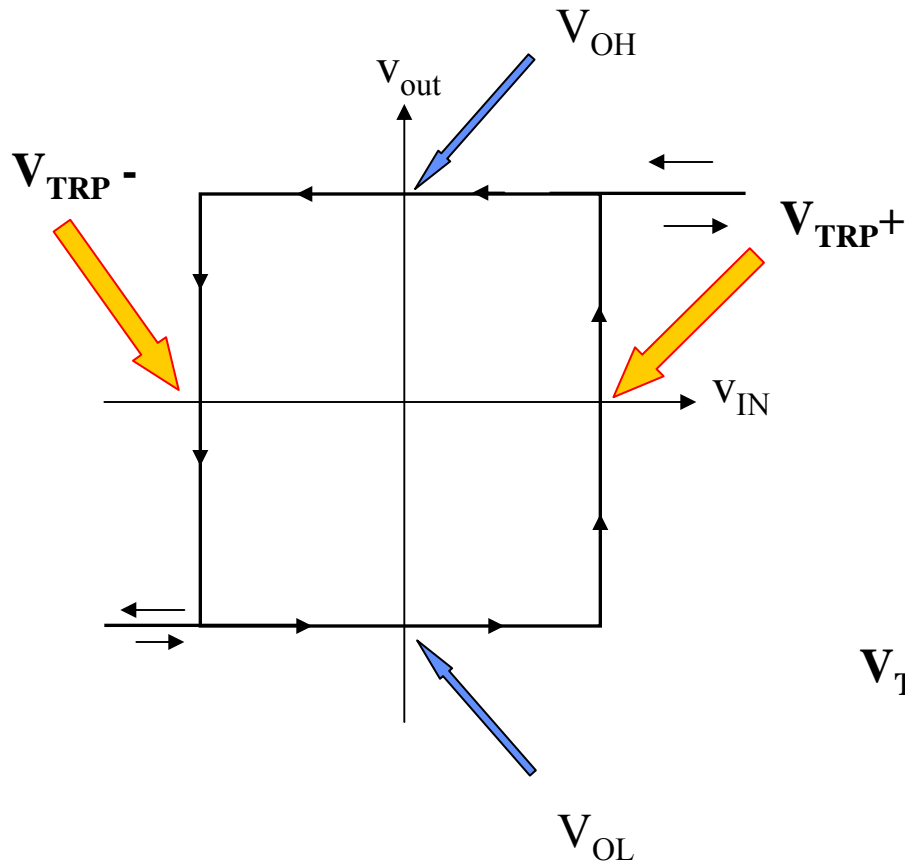
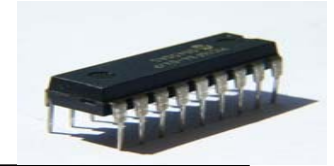
- ❖ Existence of a *hysteresis band*
 - * output voltage doesn't change as long as input is within this band.
 - * output changes only when the input *comes out* of the band.

- ❖ In a hysteresis comparator the output depends both on the present and the past values of V_{in} ----- dependency on history.

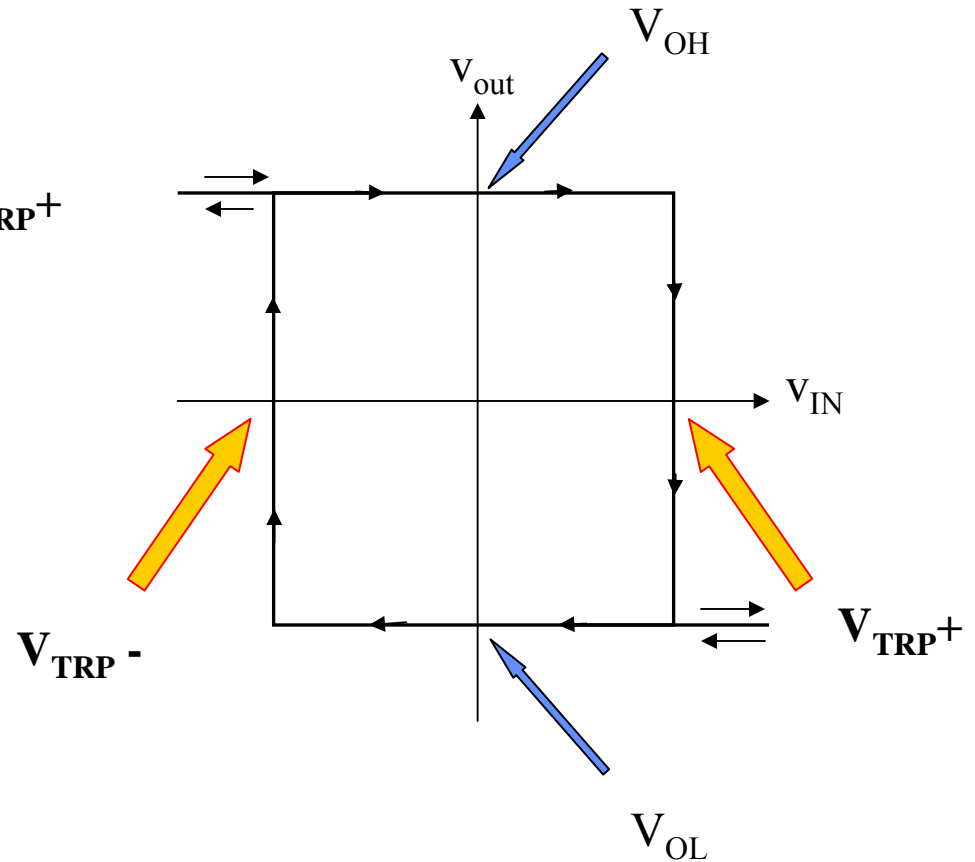
How to get the hysteresis:

1. External feedback.
2. Internal feedback.

Transfer curve of a Comparator with Hysteresis

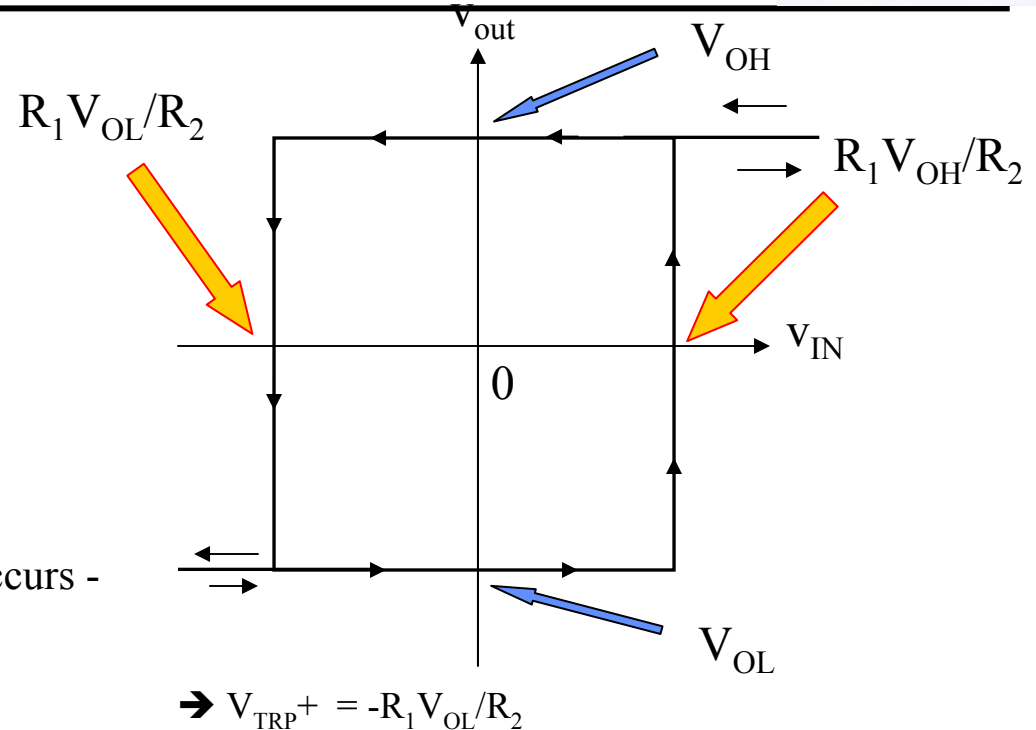
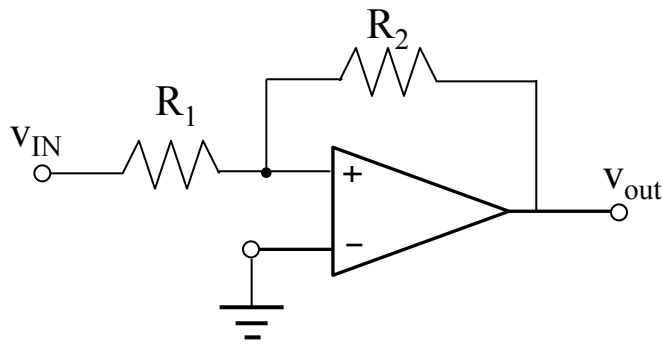


Counterclockwise Bistable



Clockwise Bistable

Noninverting Comparator using External Positive Feedback



Upper Trip Point:

We have $v_{OUT} = V_{OL}$, the upper trip point occurs -

$$0 = \left(\frac{R_1}{R_1 + R_2} \right) V_{OL} + \left(\frac{R_2}{R_1 + R_2} \right) V_{TRP^+}$$

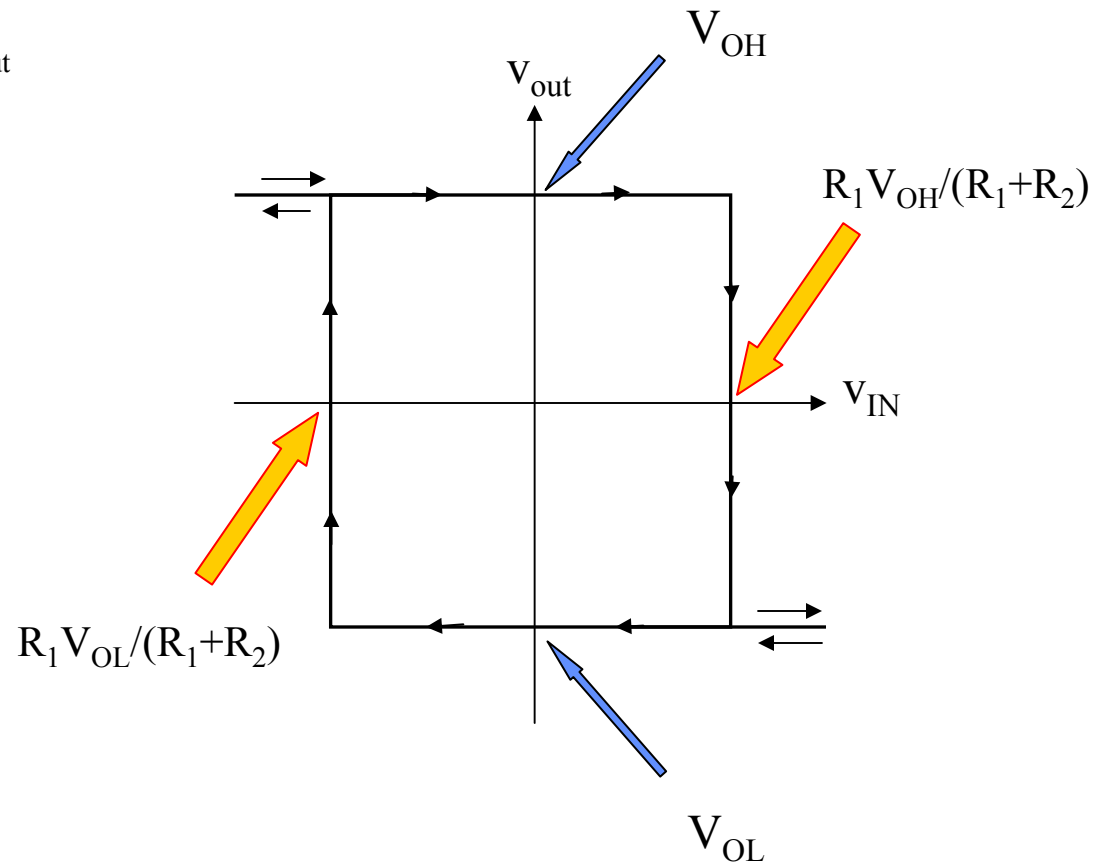
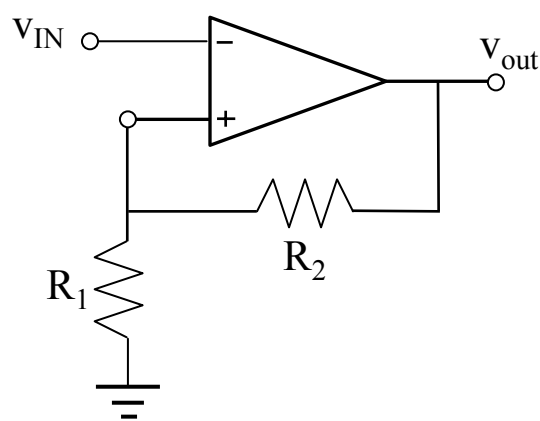
Lower Trip Point:

Here we have $v_{OUT} = V_{OH}$, the lower trip point occurs when,

$$0 = \left(\frac{R_1}{R_1 + R_2} \right) V_{OH} + \left(\frac{R_2}{R_1 + R_2} \right) V_{TRP^-} \quad \rightarrow V_{TRP^-} = -R_1 V_{OH} / R_2$$

$$\text{Width of the band: } \Delta v_{in} = V_{TRP^+} - V_{TRP^-} = (R_1 / R_2)(V_{OH} - V_{OL})$$

Inverting Comparator using External Positive Feedback



Upper Trip Point:

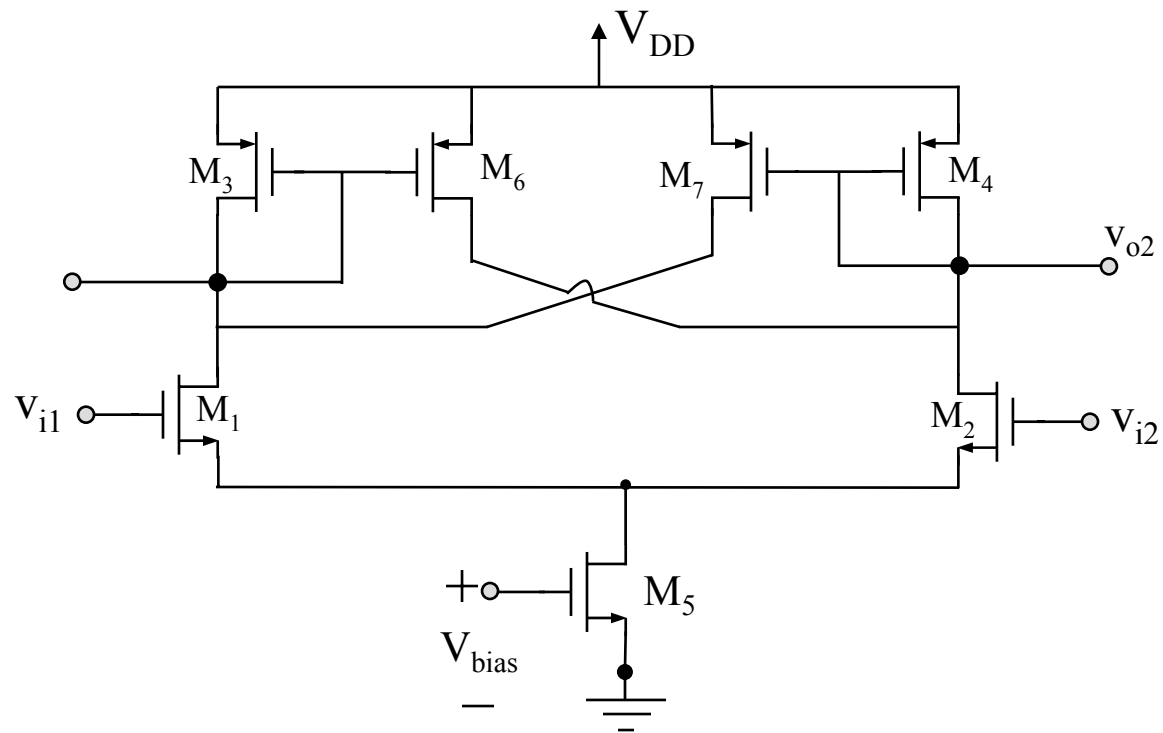
$$V_{TRP^+} = \left(\frac{R_1}{R_1 + R_2} \right) V_{OH}$$

Lower Trip Point:

$$V_{TRP^-} = \left(\frac{R_1}{R_1 + R_2} \right) V_{OL}$$

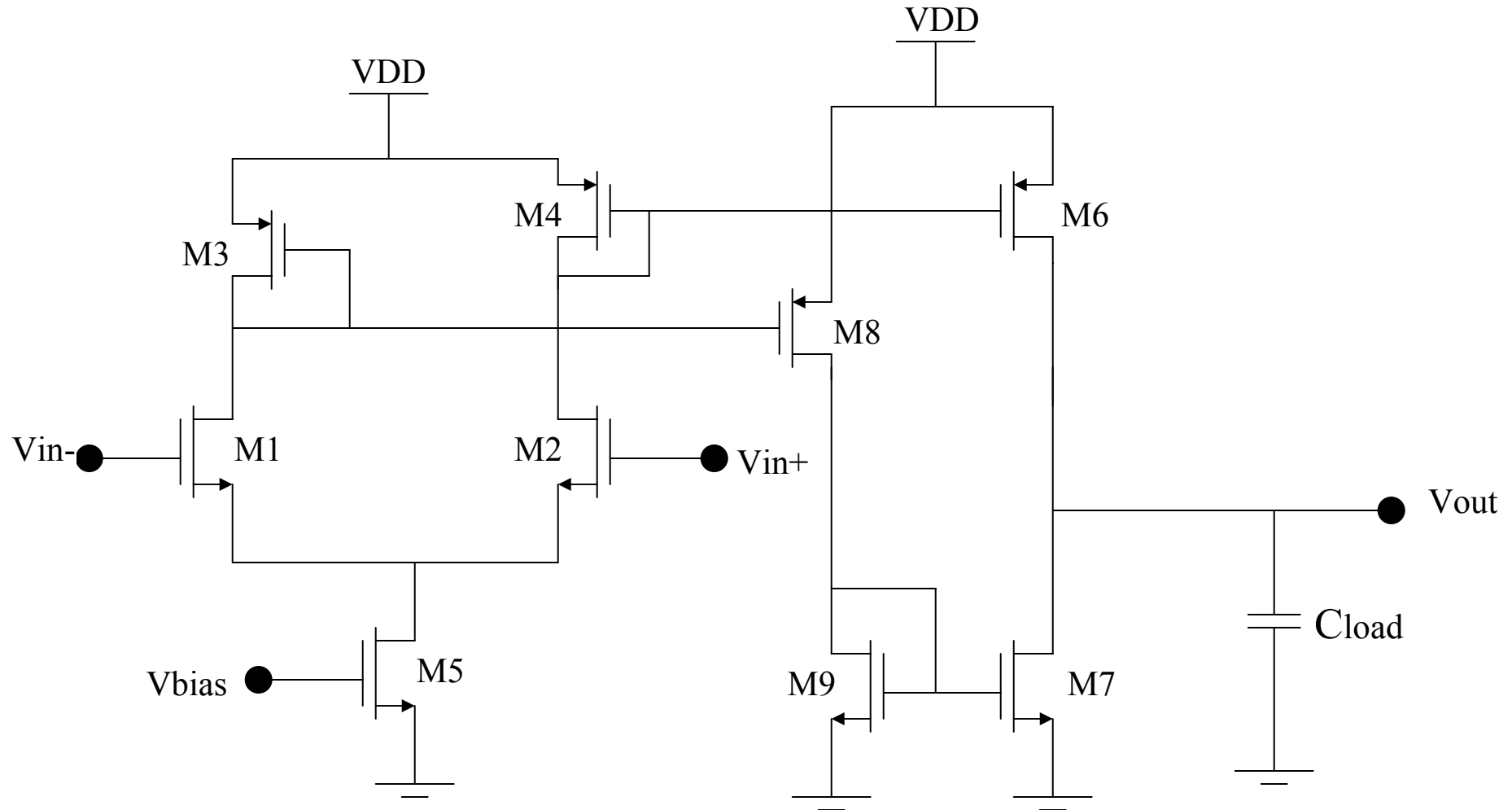
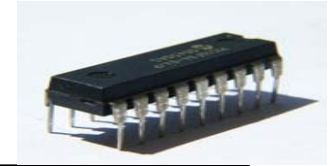
Width of the band: $\Delta v_{in} = V_{TRP^+} - V_{TRP^-} = [R_1/(R_1+R_2)](V_{OH} - V_{OL})$

Hysteresis using Internal Positive Feedback



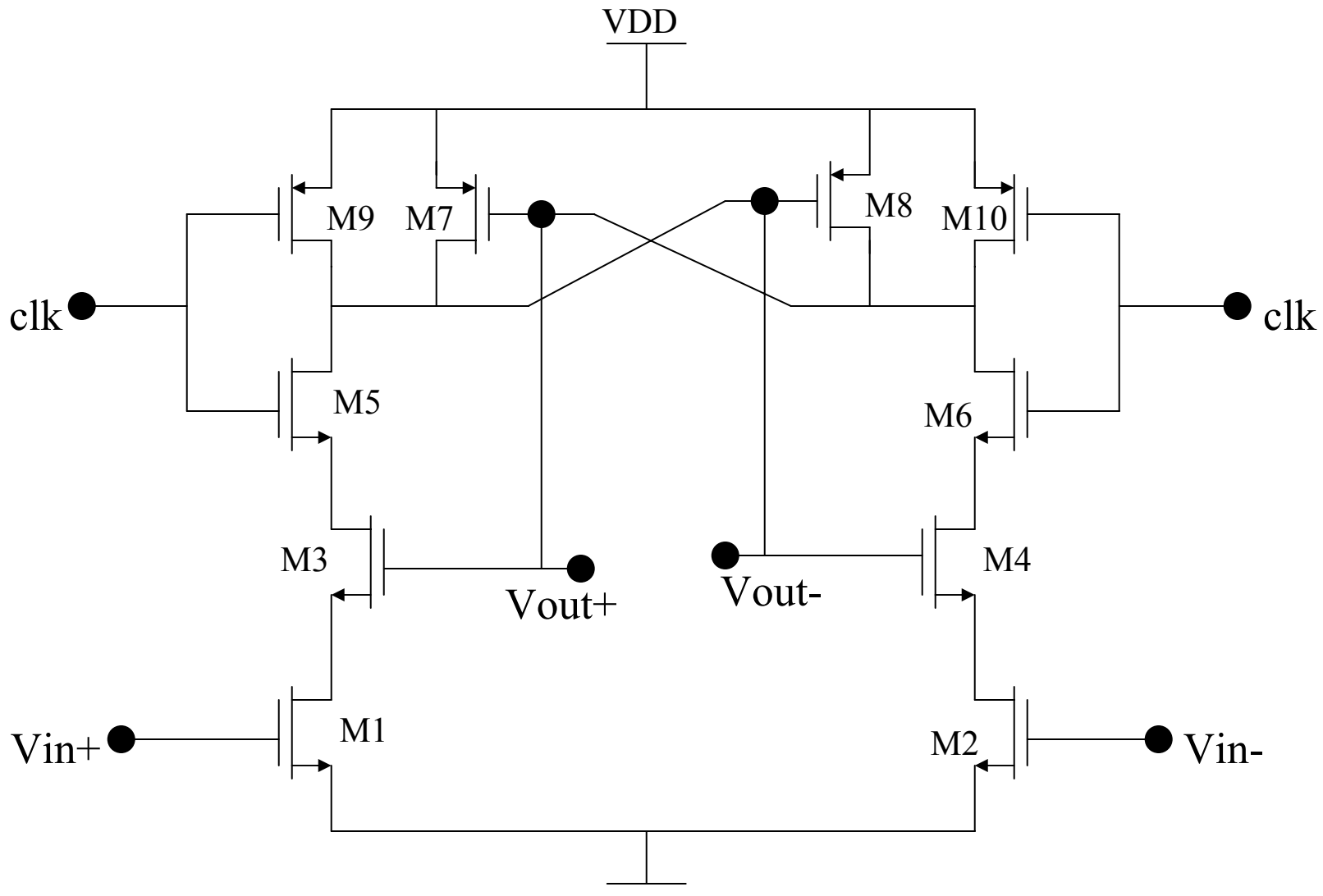
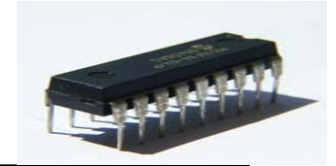
A Simple Comparator with an internal positive feedback

Push-Pull Output Comparators

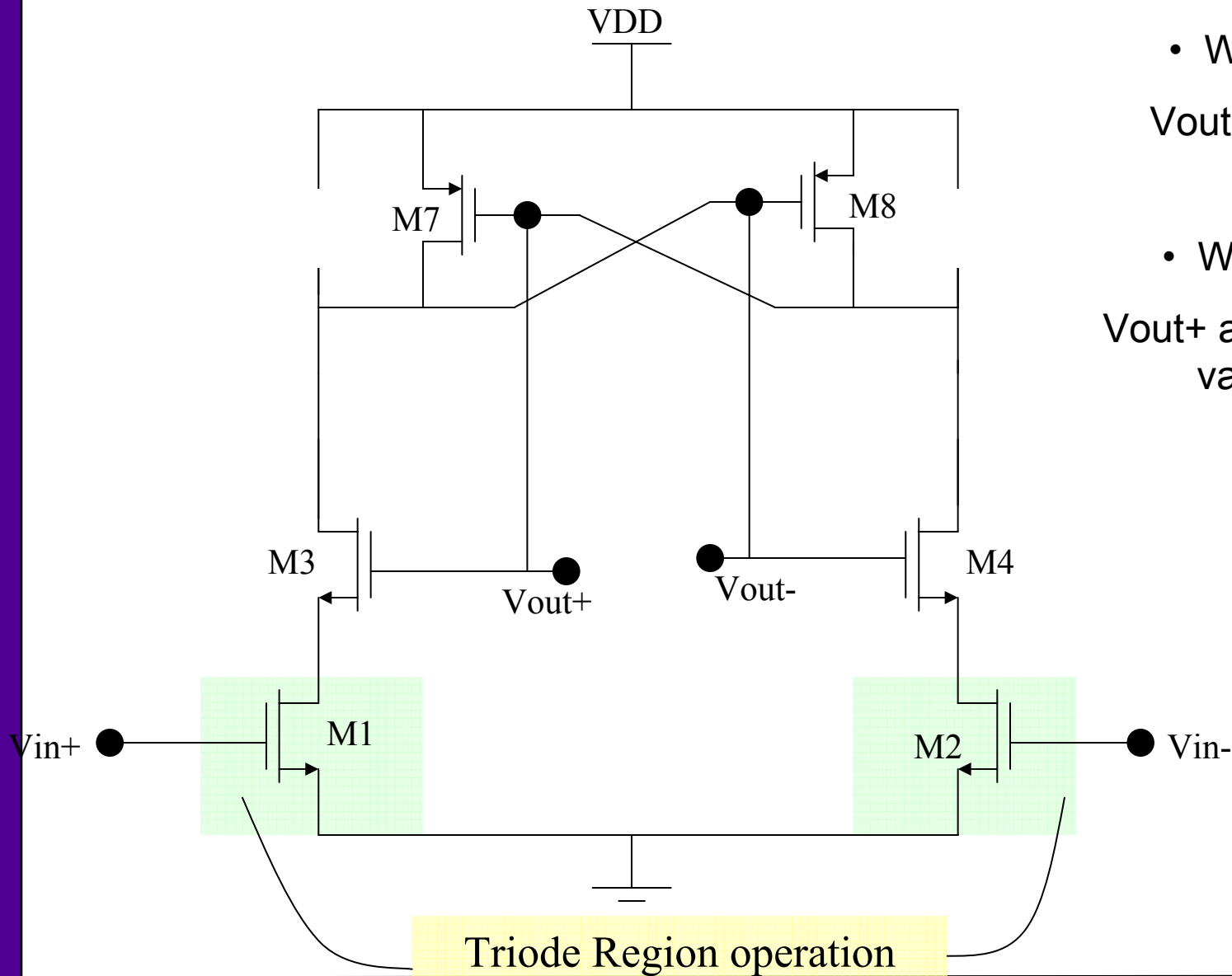
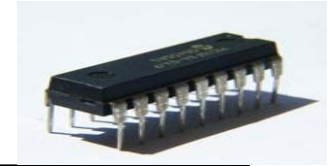


- Low gain
- Able to sink/source large amount of current in the output capacitance.

Latched Comparator

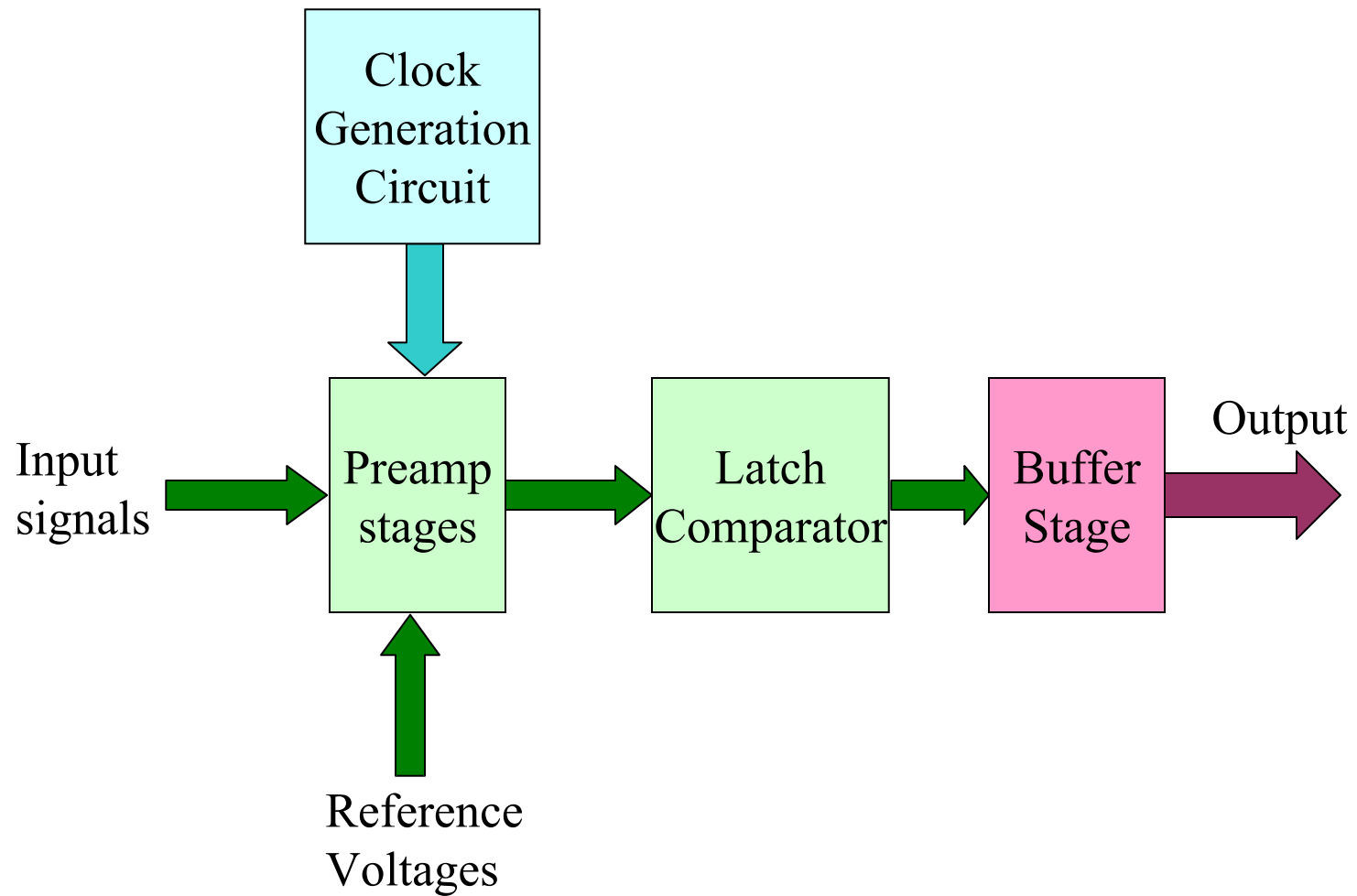
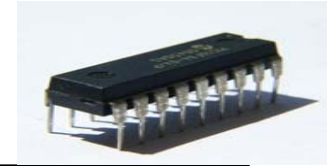


Latched Comparator - Operation

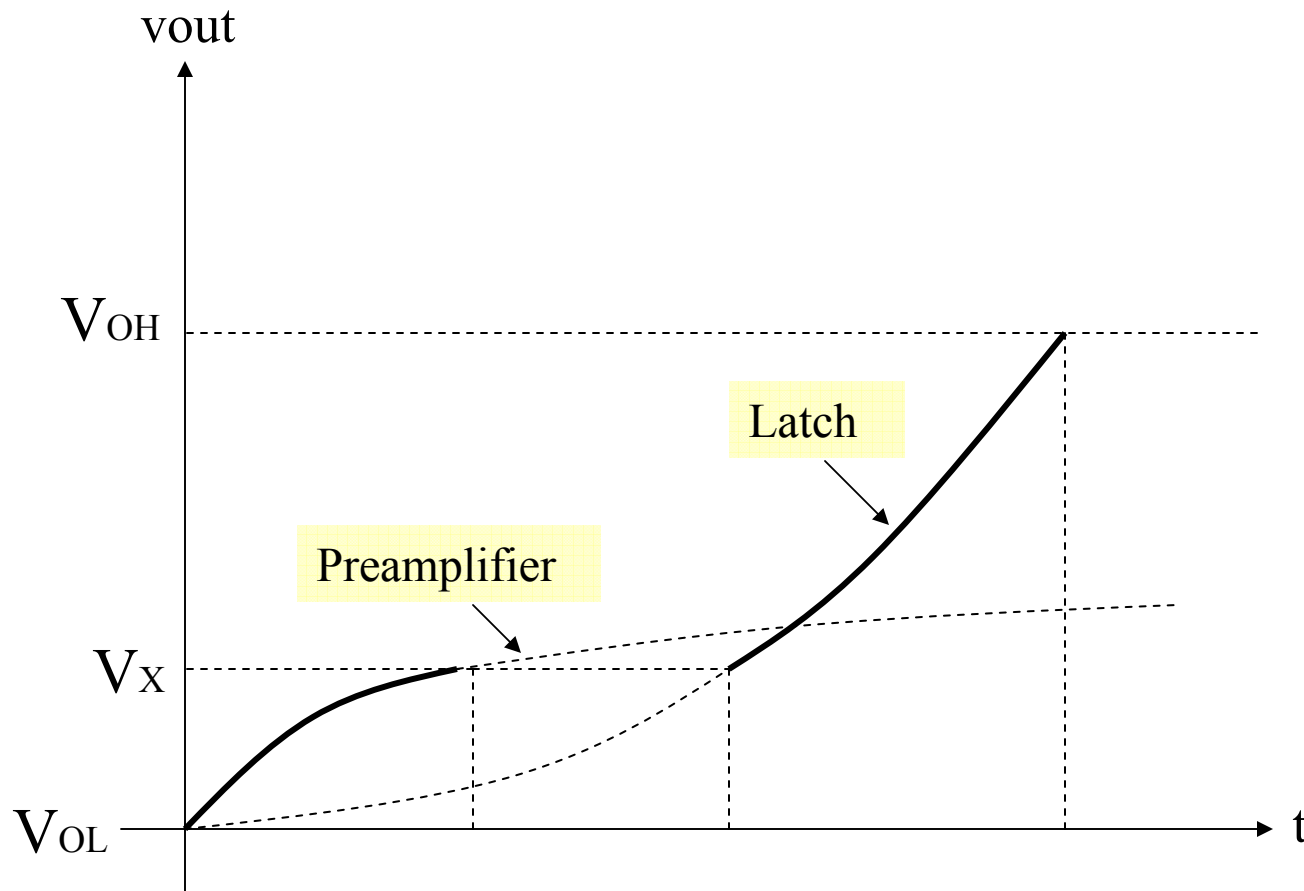
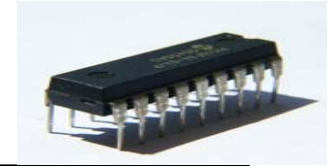


- When CLK=0
 $V_{out+} = V_{out-} = V_{DD}$
- When CLK=1
Vout+ and Vout- gives valid output

ARCHITECTURE

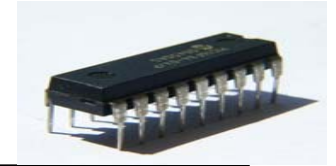


Minimization of Propagation Delay



Use a cascade of linear amplifiers to quickly build up the signal level and apply this amplified signal level to a latch for quick transition to the full binary output swing.

High Speed Comparator Stages

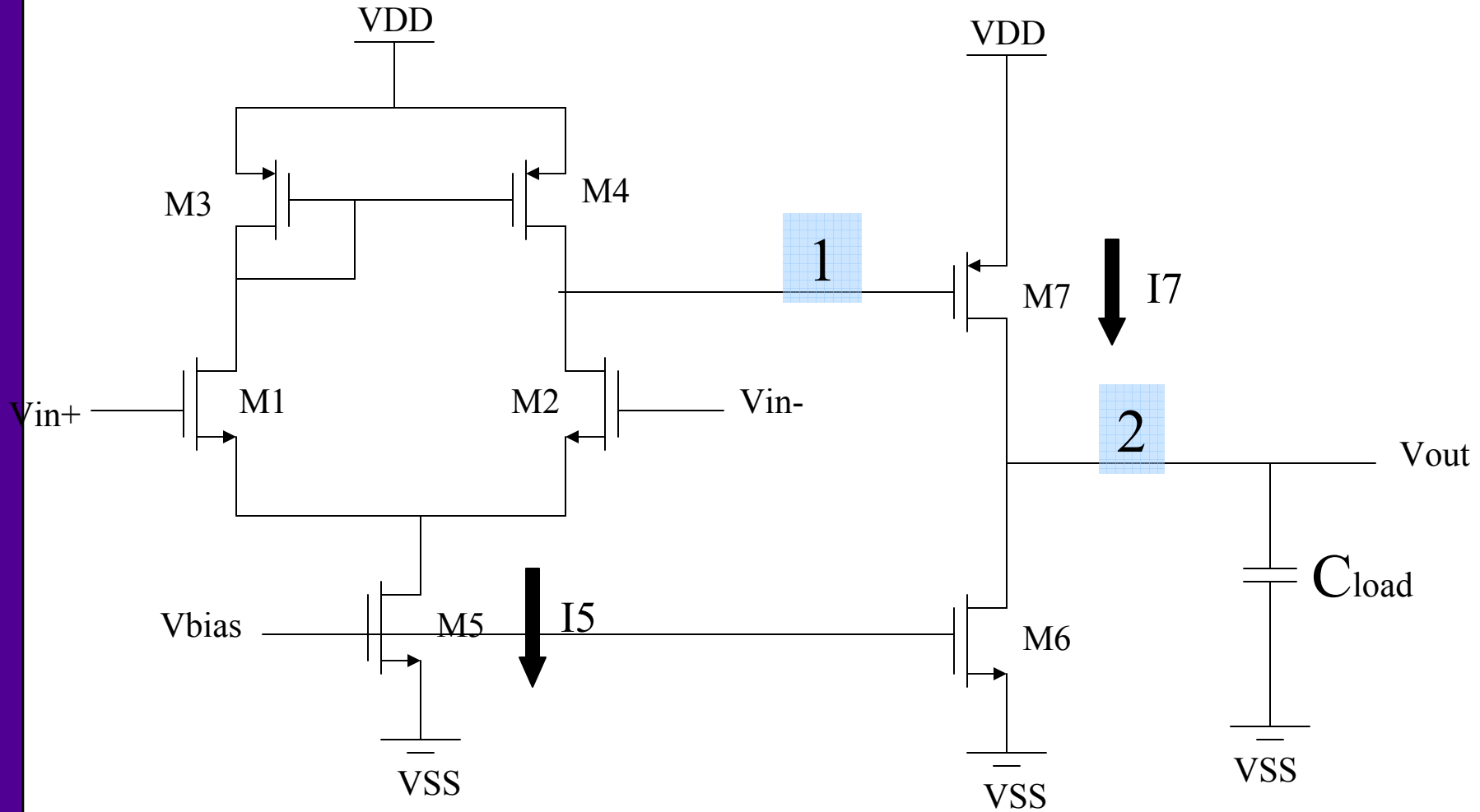
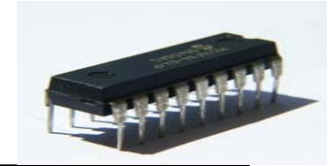


- ❑ **The preamplifier advantages:**
 - reduces the comparator input-offset voltage.
 - Reduces kick-back noise.

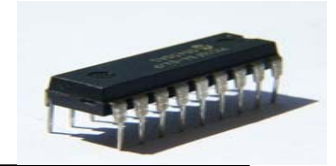
- ❑ **The latch comparator:**
 - Gives high gain.
 - Positive feedback always saturates the output.

- ❑ **The latch comparator:**
 - Drives high load capacitance.
 - Gives output in proper shape.

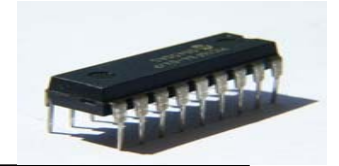
Design of a two-stage Comparator for slewing response



Two Stage Comparator Specifications



- ❑ **Design a two stage comparator which meets the following specification.(180nm CMOS9, VDD=1.8V)**
 - **DC gain > 100**
 - **ICMR = 0.6V to 1.2V**
 - **Propagation delay < 500ps**
 - **Min input voltage < 20mV.**
 - **Output capacitance = 100fF.**
 - **Maximum power consumption = 1mW.**



Have a Nice Day

Thank You

See you in the lab