Chapter 11

ADVANCED AMPLIFIER DESIGN

11.1 Introduction

As mentioned in previous chapters, performance of operational amplifiers will inevitably be degraded if it is to be operated at lower supply voltages, at higher speeds, and/or with lower power consumption. In this chapter, advanced techniques to improve amplifiers' performance will be discussed, including common-mode feedback and gain-enhancement techniques. In addition, designs for high power-supply rejection ratio and fast settling time will be addressed. Finally, advanced current mirrors suitable for applications with low-supply voltages and high output swings will be presented.

11.2 Common-Mode Feedback CMFB [1]

Active loads are frequently used for high-gain differential amplifiers. The main problem is that, without feedback or special consideration from the subsequent stages, the dc voltage at the outputs is in general undefined, and it is quite difficult to keep the amplifier to operate in the proper region for both maximum gain and maximum output swing.

As a possible solution, common-mode feedback circuits can be considered to stabilize the common-mode output voltage to be at a desirable constant. The main principle for such a CMFB circuit is to sense the common-mode output voltage and feed it back to adjust the bias current source accordingly. In contrast to a differential pair, a good common-mode feedback circuit should have very high differential-mode rejection.

11.2.1 CMFB Using Resistors

Figure 11.1 illustrates a simple CMFB using a pair of resistors connected at the outputs. The output common-mode is sensed from the middle points of the resistors and fed back to adjust the bias current for the main amplifier.

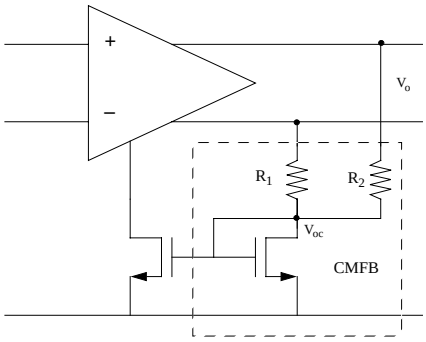

Fig. 11.1 Schematic of a simple CMFB using resistors

A major disadvantage of this design is that resistors would inevitably introduce extra loading to the output nodes. To minimize the loading, large resistors can be used. However, this would not only require a large chip area but also add extra capacitance loading to the output. Alternatively, source followers can be inserted between the output nodes and the resistors at the cost of more power.

Another interesting variation of this CMFB design is shown in Fig. 11.2, where the common-mode output voltage is sensed and fed back to the loads, which are realized using NMOS in the saturation region.

11.2.2 CMFB Using Capacitors

The resistors for CMFB in Fig. 11.1 can be replaced by capacitors as shown in Fig. 11.3. If the leakage from the middle node is negligible, the output common-mode voltage is kept constant and is equal to

$$V_{0C} = V_{GS_1} + V_C \tag{11.1}$$

where V_C is the initial voltage across the capacitors.

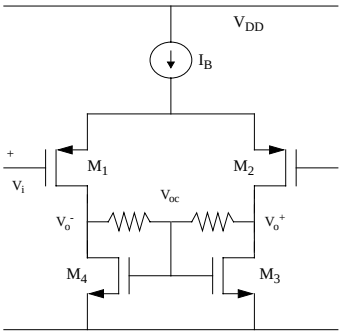

Fig. 11.2 Schematic of a CMFB using resistors and saturation MOS transistors as the

A problem with this design is that large capacitors required for the CMFB are connected directly at the output nodes and thus degrade the speed. Similar to the resistor case, this problem can be alleviated by employing source followers between the output nodes and the capacitors.

In addition, in practice, the capacitors would need to be frequently refreshed to compensate for the leakage and to keep the initial voltage the same.

11.2.3 CMFB Using Source-Coupled Pair

A source-coupled pair can also be used for CMFB as shown in Fig. 11.4, in which the output common-mode voltage is given by

$$V_{0C} = V_{GS_2} + V_{GS_4} \tag{11.2}$$

Unlike the CMFB using resistors, the CMFB using a source-coupled pair may become asymmetrical due to the non-linearity of the transistors in the source-coupled pair for large output differential swing.

11.2.4 CMFB Using Linear MOS Transistors

Figure 11.5 shows a possible implementation of a CMFB using MOS transistors M_2 and M_3 in the linear region. The equivalent resistance given by M_2 and M_3 can be easily shown to be

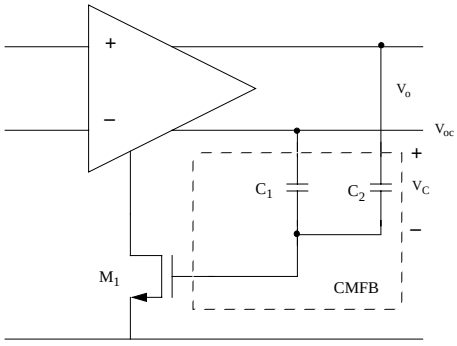

Fig. 11.3 Schematic of a CMFB using capacitors

$$R_{eq} = R_{eq2} \parallel R_{eq3} = \frac{1}{K(V_O^+ + V_O^- - 2V_T)} = \frac{1}{K(2V_{OC} - 2V_T)} \tag{11.3}$$

As a result, the resistances of M_2 and M_3 can sense the output common-mode voltage and adjust the bias current accordingly to stabilize the output common-mode voltage.

11.3 Improved Unity-Gain Buffer

In many applications, unity-gain buffers are required and source followers can be conveniently used. However, to achieve a small output impedance for a gain close to unity, in particular at high frequencies, the device size and the bias current need to quite large.

Feedback can be used to achieve unity-gain buffers with much improved performance as shown in Fig. 11.6. This is a series-shunt feedback configuration, and it can be easily proved that the overall closed-loop small-signal parameters are given by

$$A_f = \frac{A_o}{1 + A_o} \approx 1 \tag{11.4}$$

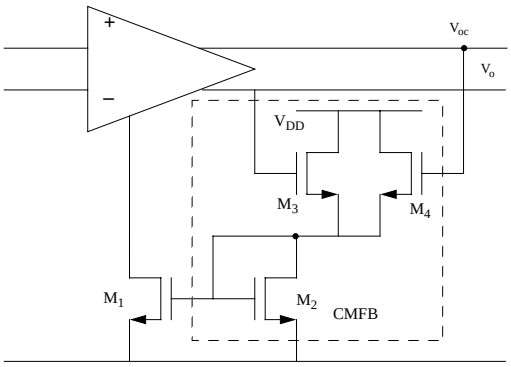

Fig. 11.4 Schematic of a CMFB using a source-coupled pair

$$R_{in_f} = R_{in} \times (1 + A_o) \tag{11.5}$$

$$R_{o_f} = \frac{R_o}{1 + A_o} = \frac{1}{A_o g_m} \tag{11.6}$$

where A_o, R_{in}, and R_o are the open-loop parameters of the amplifier.

11.4 Gain-Boosting Techniques [1][2]

Cascode circuits are popularly used to increase the output impedance and thus the voltage gain of amplifiers without sacrificing the bandwidth. Triple-cascode can also be used to further increase the gain. However, the output swing would be quite limited, which could be a serious problem for applications with low supply voltages. In such a case, the gain-boosting or gain-enhancement technique can be used.

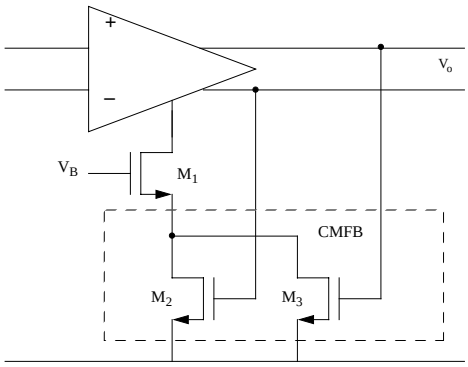

Fig. 11.5 Schematic of a CMFB using linear MOS transistors

A simplified circuit schematic of a cascode circuit with gain boosting is shown in Fig. 11.7. Since the feedback is in a series configuration at the output, the closed-loop output impedance becomes

$$R_{o_f} = R_o(1 + A_{aux}) = A_{aux} g_m r_o^2 \tag{11.7}$$

and the overall closed-loop voltage gain is given by

$$A_f = A_{aux} g_m^2 r_o^2 \tag{11.8}$$

both of which have been boosted by a factor of A_{aux}.

Intuitively, this technique, also referred to as regulated cascode, increases the effective output impedance by using feedback to keep the voltage at Node B and thus the current through M_1 relatively constant.

The high-frequency behavior and performance of the gain-enhancement amplifier can be understood by considering the plots in Fig. 11.8. Figure 11.8a shows the Bode's plot for the gain of

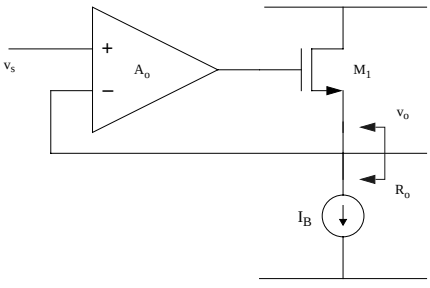

Fig. 11.6 Schematic of a unity-gain buffer with feedback

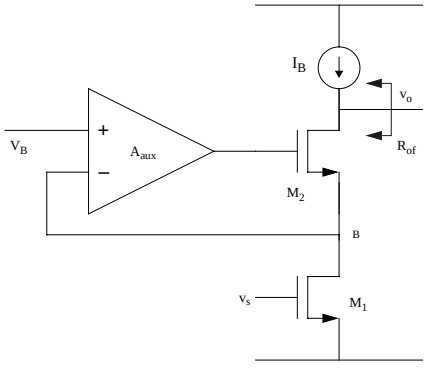

Fig. 11.7 Schematic of a cascode circuit with the gain-boosting technique

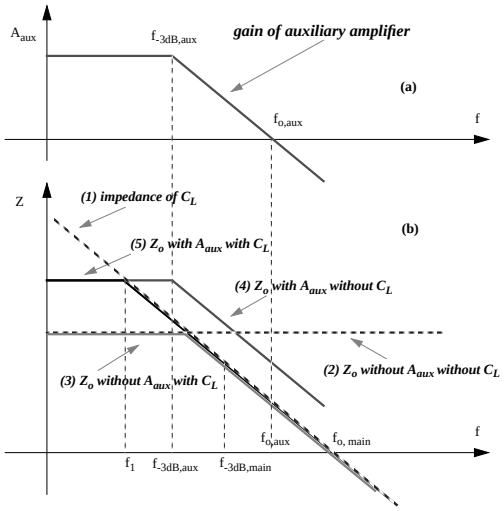

Fig. 11.8 Gain of auxiliary amplifier (a) and output impedance (b) versus frequency

the auxiliary amplifier with a bandwidth $f_{-3dB,aux}$. Figure 11.8b compares the output impedances of the main amplifier with and without consideration of the auxiliary amplifier and the load capacitance C_L.

In Fig. 11.8b, the impedance of the load capacitor C_L is shown as Curve 1. Without the auxiliary amplifier A_{aux} and without C_L, the output impedance is a constant as a function of frequency (Curve 2). The equivalent output impedance without A_{aux} but with C_L is plotted as Curve 3. Finally, the equivalent output impedance with A_{aux} with and without C_L are shown as Curves 4 and 5, respectively. The corresponding gain plots are shown in Fig. 11.9.

At low frequencies, the output impedance is dominated by the enhanced output impedance. However, at frequencies above f_1, the impedance of the capacitive load takes over, and the overall gain starts dropping. Consequently, as long as the bandwidth of the auxiliary amplifier is larger than

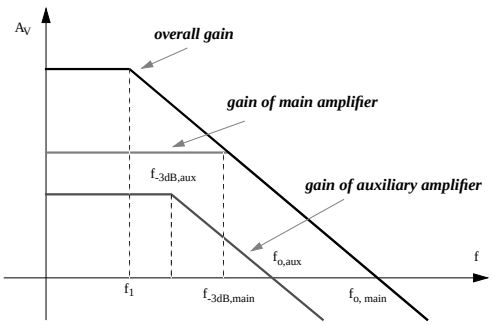

Fig. 11.9 Bode's plots of the gains for the main, auxiliary and overall amplifiers

f_1, the single-pole behavior of the overall gain can be maintained. Equivalently, it is necessary that the unity-gain bandwidth of the auxiliary gain $f_{o,aux}$ is larger than the 3dB bandwidth of the main amplifier $f_{-3dB,main}$ but can be smaller than the unity-gain bandwidth of the main amplifier $f_{o,main}$.

The simplest way to implement the auxiliary amplifier A_{aux} for the gain boosting is to employ a common-source stage as shown in Fig. 11.10. The transistor M_3 together with the bias current I_{B2} provides the extra gain A_{aux} for gain boosting.

The overall gain is indeed boosted by A_{aux} using this simple circuit. However, the main disadvantage is that the minimum drain-to-source voltage of M_1 is now limited by the gate-to-source voltage of M_3, which is typically too large. In addition, the Miller capacitance due to the gate-to-drain capacitance of M_3 and the auxiliary gain stage can significantly lower the pole at Node B and affect the settling time of the amplifier.

To address these problems, a folded-cascode structure can be used for the auxiliary amplifier as opposed to the simple common-source transistor as shown in Fig. 11.11.

Note that the Miller capacitance due to the gate-to-drain capacitance of M_3 is eliminated by the cascode. Also, the folded-cascode auxiliary amplifier can be designed so that the drain-to-source voltage of the input device M_1 remains at the minimum possible level, $V_{GS} - V_T$, and thus give a larger output swing compared to the implementation using a common-source amplifier.

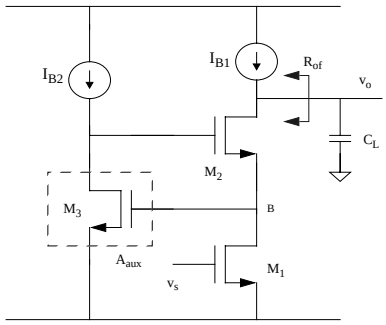

Fig. 11.10 Simplest implementation of a cascode circuit with the gain-boosting technique

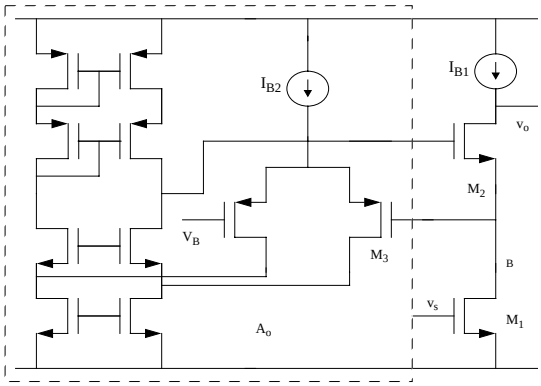

Fig. 11.11 A gain-boosting implementation using a folded-cascode amplifier

In practice, the same gain-enhancement technique can and should be used for the load to increase the overall impedance and the overall gain.

11.5 Power-Supply Rejection Ratio PSRR [3]

For mixed-signal systems, analog and digital circuits may need to operate from the same supply voltages. Due to the non-zero impedance of the power lines, there exists undesirable coupling which would cause the actual supply voltages to fluctuate and without enough rejection would introduce noise to the output and degrade the system performance.

Similar to the common-mode rejection ratio used to measure how sensitive an amplifier is to the common-mode signal, the power-supply rejection ratio is a measurement of how well an amplifier can reject the supply fluctuation and is defined as the ratio between the differential-mode gain A_{dm} and the supply gain A_{sup}

$$\text{PSRR} = \frac{A_{dm}}{A_{sup}} \tag{11.9}$$

$$A_{sup} = \frac{\partial V_o}{\partial V_{sup}} \tag{11.10}$$

In general, at low frequencies, the supply noise that can be coupled to the output is mainly due to variation in bias circuits and mismatches in differential structures. At high frequencies, coupling from parasitic capacitance becomes more and more dominant.

Consider a standard two-stage CMOS amplifier used as an integrator with a capacitor C_F connected from the output to the input as shown in Fig. 11.12. Also shown in the figure are the input capacitor C_I and the equivalent stray capacitances from the input node to the supply voltages C_{DD} and C_{SS}. Noise from supply voltages can be coupled into the output and hence degrade the PSRR through each of the gain stages by different mechanism.

11.5.1 Effect of the First Gain Stage to PSRR

First, let us consider how the first gain stage contributes to the PSRR. Since the input node is virtual ground, noise from supply voltages will be coupled to the output through the charge transfer between C_{DD} and C_{SS} and C_F, respectively. The supply noise gain and PSRR due to these capacitors can be estimated as follows.

$$A_{sup^+} = \frac{\partial V_o}{\partial V_{sup^+}} = -\frac{C_{DD}}{C_F} \tag{11.11}$$

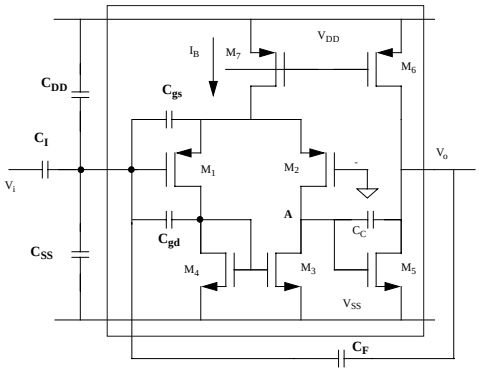

Fig. 11.12 Schematic of a two-stage CMOS amplifier for PSRR consideration

$$\text{PSRR}^+ = \frac{A_{dm}}{A_{sup^+}} = \frac{-C_I/C_F}{-C_{DD}/C_F} = \frac{C_I}{C_{DD}} \tag{11.12}$$

$$A_{sup^-} = \frac{\partial V_o}{\partial V_{sup^-}} = -\frac{C_{SS}}{C_F} \tag{11.13}$$

$$\text{PSRR}^- = \frac{A_{dm}}{A_{sup^-}} = \frac{-C_I/C_F}{-C_{SS}/C_F} = \frac{C_I}{C_{SS}} \tag{11.14}$$

To reduce the noise gain due to these stray capacitances, it is desirable to maximize the input and feedback capacitors and to minimize the stray capacitance by employing good layout techniques.

Noise from the supply voltages can be coupled to the output not only through the stray capacitances but also through the input capacitance of the amplifier itself. First, noise from V_{SS} will couple to the drain of M_4 and appear at the output via C_{gd} and C_F. Second, any variation in the bias current I_B due to the supply noise will change the gate-to-source voltage of M_1 and be coupled to the

output via C_{gs} and C_F. In addition, noise from V_{DD} will change the threshold voltage V_{T1} through body effect. For the same bias current, this results in the same change in the gate-to-source voltage V_{GS1} and contributes additional gain to the output via C_{gs} and C_F.

In summary, it can be easily shown that the gain of the noise from both the negative and positive supply voltages are given by

$$A_{sup^-} = -\frac{C_{gd}}{C_F} - \frac{C_{gd}}{C_F}\left(\frac{1}{2g_{m4}}\frac{\partial}{\partial V_{SS}}I_B\right) - \frac{C_{gs}}{C_F}\left(\frac{1}{2g_{m1}}\frac{\partial}{\partial V_{SS}}I_B\right) \tag{11.15}$$

$$A_{sup^+} = -\frac{C_{gd}}{C_F}\left(\frac{1}{2g_{m4}}\frac{\partial}{\partial V_{DD}}I_B\right) - \frac{C_{gs}}{C_F}\left(\frac{1}{2g_{m1}}\frac{\partial}{\partial V_{DD}}I_B\right) + \frac{C_{gs}}{C_F}\left(\frac{\partial}{\partial V_{DD}}V_T\right) \tag{11.16}$$

From the above discussion, to achieve high PSRR, it is necessary that

- The bias current should be designed to be independent of supply voltages
- If possible, the source and bulk of the input devices should be connected to eliminate the body effect
- The size of the input devices should be small to reduce their parasitic capacitance while the feedback capacitor should be large
- Cascode structure should be used whenever possible to improve isolation and reduce the noise coupling from the supply voltages

11.5.2 Effect of the Second Gain Stage to PSRR

Now, consider the second gain stage formed by M_5, M_6 and C_C. At low frequencies, both the gain from the output voltage to the supply voltages V_{DD} and V_{SS} are dominated by the ratio of their output impedances and are approximately -3dB each. Hence, both PSRR+ and PSRR- are 3 dB above the differential mode gain A_{dm}.

At high frequencies, the compensation capacitor C_C becomes short-circuited, and the transistor M_5 becomes diode-connected. Since the gate-to-source voltage V_{GS5} remains the same due to the constant bias current, any noise from V_{SS} will directly transferred unattenuated to the output. In addition, the negative supply noise appears a very low impedance from the output. As a result, the gain of the negative supply voltage A_{sup-} is close to unity and the PSRR− decreases for frequencies beyond the unity-gain frequency of the amplifier as illustrated in Fig. 11.13.

On the other hand, for the positive supply voltage, the noise still appears to be a high impedance from the output. Due to decrease of the output impedance of M_5 and that of the capacitive load C_L, its noise gain will start to drop at the same frequency and at the same rate as the signal. Consequently, the PSRR+ remains almost constant.

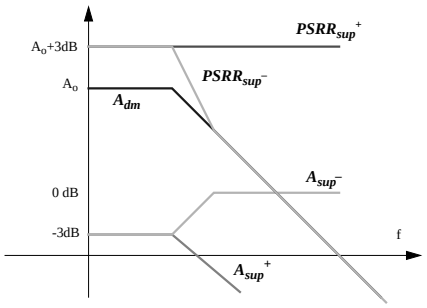

Fig. 11.13 Bode's plots of the supply noise gains and PSRR from the second gain stage

An effective way to reduce the gain from the supply voltages is to employ cascode configuration for both gain and load devices. In addition, to alleviate the effect of the compensation capacitor, a transistor operated in the saturation region M_C can be inserted as illustrated in Fig. 11.14. Even at high frequencies when the compensation capacitor is shorted, the impedance from the gate of M_5 to the output is quite large. Consequently, the noise coupling from the V_{SS} will be significantly reduced. Note that at the same time the impedance from the output to the gate is still small, $1/g_m$, which can still be effectively used as a resistor to cancel the right-half-plane zero.

The challenge with this solution is to provide two perfectly matched and supply-independent current sources I_C without contributing too much loading and noise to the amplifier.

11.6 Settling Time

In general, the settling time of an amplifier is defined as the time it takes for the output to reach a specified value when a step input voltage is applied. There are two distinct components contributing to the settling time. The first, referred to as the linear settling time, is due to the fact that the unity-gain bandwidth of the amplifier is not infinity and is independent of the input and output steps. The other component, commonly referred to as the non-linear settling time, is due to the slew rate of the amplifier and is dependent on the input and output steps.

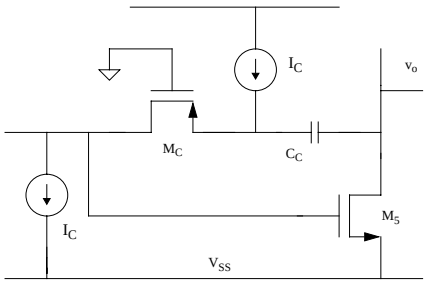

Fig. 11.14 Insertion of M_C in saturation region to eliminate the effect of C_C to PSRR

As a review, consider an amplifier with a dominant pole p, whose transfer function is given by:

$$A(s) = \frac{A_o}{\left[1 - \frac{s}{p}\right]} \tag{11.17}$$

If a step input is applied to the amplifier, the output voltage will increase with a non-zero rise time. Here we would like to find out how the rise time is related to the 3dB frequency of the amplifier.

Let $v_i(t) = v_a\, u(t)$, the output waveform can be obtained as follows:

$$v_o(t) = \Im^{-1}[v_o(s)] = \Im^{-1}[A(s)\cdot V_i(s)] = \Im^{-1}\left[\frac{A_0}{\left[1 - \frac{s}{p}\right]}\cdot\frac{v_a}{s}\right] = A_0 v_a \Im^{-1}\left[\frac{1}{s} - \frac{1}{s-p}\right] \tag{11.18}$$

As a result,

$$v_o(t) = A_0 v_a(1 - e^{pt})u(t) \tag{11.19}$$

It follows that the settling time τ_s for the output to settle to x% of its final steady-state value can be calculated to be:

$$\tau_s = \frac{1}{|p|}\ln\frac{1}{1-x} = \tau\ln\frac{1}{1-x} \tag{11.20}$$

where τ is defined as the time constant of the amplifier and being equal to the reciprocal of |p| and of the 3dB frequency of the amplifier. As examples, the settling times for the output to reach 90% and 99% of its final value are 2.2 τ and 4.6 τ, respectively.

The settling time is dependent on the -3 dB bandwidth, which in turn depends on the unity-gain frequency and the closed-loop gain of the amplifier. For a classical two-stage amplifier, the unity-gain bandwidth only depends on the compensation capacitor but not on the load capacitor. However, for many other configurations, including folded-cascode amplifiers, the unity-gain bandwidth depends strongly on the load capacitance. As a consequence, the settling time for these amplifiers will also depend on the equivalent load capacitance.

Figure 11.15 shows a typical configuration to measure the settling time and thus to determine the -3 dB bandwidth of an amplifier, where C_P represents the total parasitic capacitance at the input.

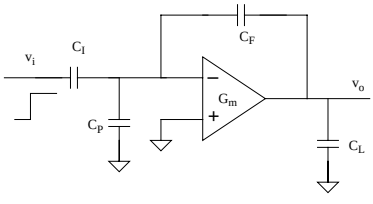

Fig. 11.15 A setup to measure the settling time of an amplifier

Assume a finite open-loop gain A(s) with the unity-gain frequency and the -3dB frequency being ω_o and p_o, respectively. At high frequencies,

$$A(s) = \frac{A_o}{1 + \frac{s}{p_o}} \approx \frac{A_o}{\frac{s}{p_o}} = \frac{\omega_o}{s} \tag{11.21}$$

The closed-loop gain can be derived to be

$$A_f \approx \frac{C_I}{C_F}\frac{1}{1+\frac{C_F+C_I+C_P}{C_F}\frac{1}{A(s)}} \approx \frac{C_I}{C_F}\frac{1}{1+\frac{C_F+C_I+C_P}{C_F}\frac{s}{\omega_o}} \tag{11.22}$$

from which, it can be seen that the closed-loop -3dB bandwidth is given by

$$\omega_{-3dB} = \beta\omega_o = \frac{\omega_o}{\frac{C_F+C_I+C_P}{C_F}} \tag{11.23}$$

where β, referred sometimes confusingly to as "the feedback factor", is defined as

$$\beta = \frac{C_F}{C_F+C_I+C_P} \tag{11.24}$$

Note that this feedback factor is completely different from that previously used in the feedback analysis.

The equivalent load capacitance seen by the op-amp output is given by

$$C_{LT} = C_L + \frac{C_F(C_I+C_P)}{C_F+C_I+C_P} \tag{11.25}$$

It follows that the unity-gain and -3 dB frequencies can be obtained as

$$\omega_o = \frac{G_m}{C_{LT}} = \frac{G_m}{C_L+\frac{C_F(C_I+C_P)}{C_F+C_I+C_P}} \tag{11.26}$$

$$\omega_{-3dB} = \frac{1}{\tau} = \beta\omega_o = \frac{G_m}{C_L+C_I+C_P+C_L\frac{C_I+C_P}{C_F}} \tag{11.27}$$

11.7 Advanced Current Mirrors [4]

One of the main challenges in designing high-performance amplifiers at low supply voltages is to design current sources. To achieve a high impedance, cascode can be used. However, the minimum output voltage would be large and the output swing would be limited.

As a review, for the MOS cascode current source shown in Fig. 11.16, to ensure that all the transistors are in saturation region, it is necessary that:

$$V_2 = V_t + \Delta V_{GS} \tag{11.28}$$

where ΔV_{GS} is the minimum saturation drain-to-source voltage, given by:

$$\Delta V_{GS} = V_{DS,sat} = \sqrt{\frac{2I_D}{\mu C_{ox}(W/L)}} \tag{11.29}$$

It follows that

$$V_3 = 2(V_t + \Delta V_{GS}) \tag{11.30}$$

$$V_1 = (V_t + \Delta V_{GS}) \tag{11.31}$$

$$V_o \geq (V_t + 2\Delta V_{GS}) \tag{11.32}$$

Typically, this results in a minimum output voltage of ~ 1.4V, which is significantly large!

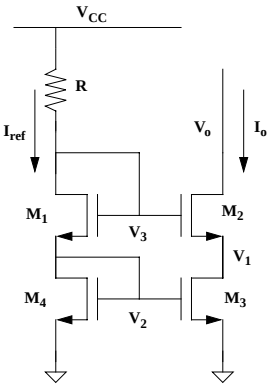

Fig. 11.16 Schematic of a MOS cascode current source

To reduce the minimum output voltage of the current source, a high-swing cascode current source can be used as shown in Fig. 11.17.

One problem with this circuit is that the drain-to-source voltages of M_4-M_6 are not the same. As a result, there exist mismatches between the reference and output currents due to the channel-length modulation effect. To eliminate this problem, the circuit shown in Fig. 11.18 can be used. It can be shown that the minimum output voltage is the same as that for the high-swing cascode current source, which can be as low as

$$V_{o,min} = 2(V_{GS} - V_{th}) \approx 0.4V \tag{11.33}$$

The transistor M_2 is added as shown to ensure good matching for M_4 and M_5 by providing the same drain-to-source voltage for the transistors, which can be estimated as

$$V_{DS_4} = V_{DS_5} = V_{GS} - V_{th} \approx 0.2V \tag{11.34}$$

Interestingly, the drain-to-source voltage of M_2 is exactly one threshold voltage, that is

$$V_{DS_2} = V_{GS_4} - V_{DS_4} = V_{th} \tag{11.35}$$

Note that the devices would be out of saturation when the input current I_{in} is larger than the bias current I_B. As a result, the bias current bias current I_B should be designed to be close to the

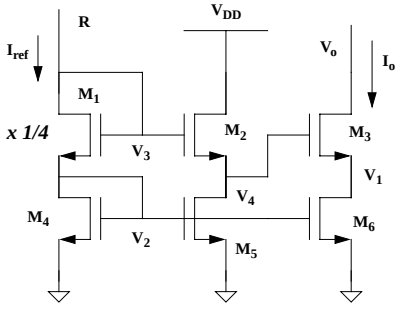

Fig. 11.17 Schematic of a MOS high-swing cascode current source

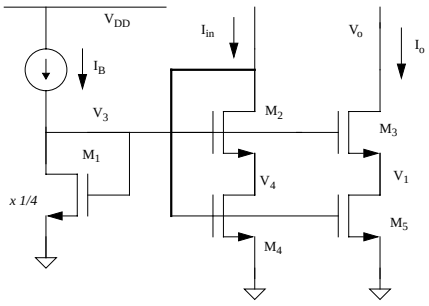

Fig. 11.18 Schematic of an improved MOS high-swing cascode current mirror

maximum value of the input current I_{in}. In addition, to reduce the power consumption, the bias current and the W/L of M_1 can be scaled down while keeping the same current density.

To increase the impedance of the cascode current source, the regulated-cascode configuration used in the gain-enhancement techniques can be employed. Such an implementation is illustrated in Fig. 11.19.

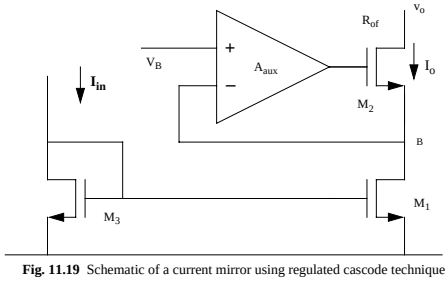

Fig. 11.19 Schematic of a current mirror using regulated cascode technique

As discussed in the gain-boosting section, the auxiliary amplifier can be simply a common-source amplifier at a cost of a limited output swing.

To improve the output swing, a folded-cascode amplifier can be used as the auxiliary amplifier. Alternatively, a diode-connected transistor acted as a level shifter can be inserted at the input of the auxiliary amplifier as illustrated in Fig. 11.20.

If matching between M_3 and M_1 is critical, the same regulated-cascoded configuration for the output can be used for the input M_3. Figure 11.21 shows an example of such an implementation.

11.8 Current-Mirror Amplifiers

In addition to the classical two-stage amplifiers, the telescopic amplifiers, and the folded-cascoded amplifiers, current-mirror amplifiers can be considered for high performance at low supply voltages. Figure 11.22 shows a simplified schematic of a current-mirror amplifiers.

As in folded-cascode amplifiers, since all the nodes except the output node have low impedance, the -3 dB and unity-gain frequencies should be quite high and are mainly dependent on the load capacitance. On the other hand, since the current mirrors can be scaled to have a current gain

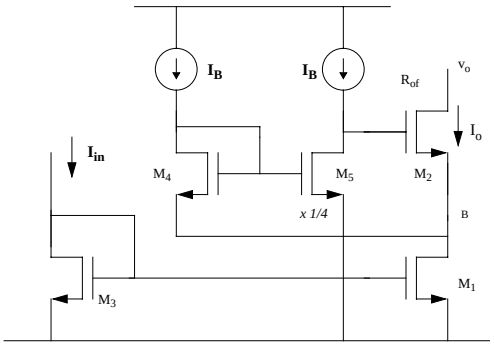

Fig. 11.20 A regulated-cascode current mirror with a level shift

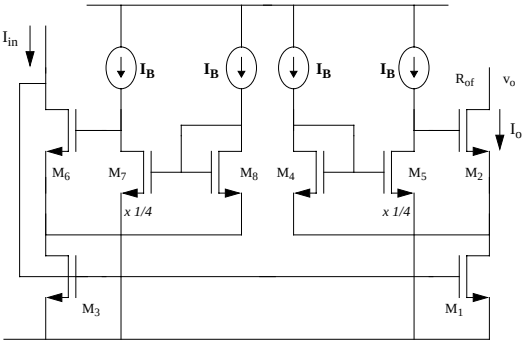

Fig. 11.21 A regulated-cascode current mirror with a level shift and matched input

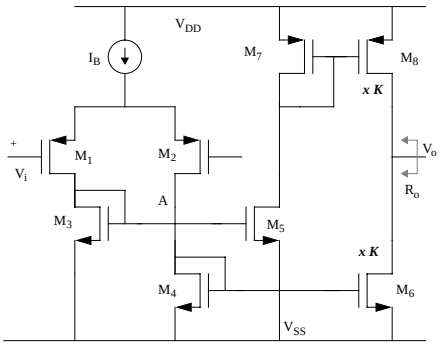

Fig. 11.22 Simplified schematic of a CMOS current-mirror amplifier

of K, the unity-gain bandwidth and the slew rate can be superior to those of folded-cascode amplifiers. It can be easily shown that

$$\omega_o = \frac{Kg_{m_1}}{C_L} \tag{11.36}$$

$$SR = \frac{KI_B}{C_L} \tag{11.37}$$

The disadvantage is that for the same total power consumption, the bias current for the input stage needs to be reduced, which results in larger noise contribution. Also, for the same reason, the input devices may need to be smaller, and hence the input offset voltage may be increased.

11.9 Class AB Amplifiers

For many high-speed applications where amplifiers with extremely high slew rate and low power consumption is required, class AB amplifiers should be considered. An example of such amplifiers is shown in Fig. 11.23.

The bias current of the output devices are determined by the translinear loops formed by M_5, M_1, M_2, M_7 and M_6, M_3, M_4, M_8. The output transconductance gain can be proved to be

$$G_m = \frac{2g_{m_7}}{1 + \frac{g_{m_7}}{g_{m_2}}} \simeq g_{m_7} \tag{11.38}$$

The main advantage is that the output currents is dependent on the input voltage and can be quite large, both positively and negatively. As the input voltage increases, the output current is increased virtually without a limit. As a result, the slew rate can be much larger than any other configuration. At the same time, since it is a class AB configuration, the quiescent current can be quite small, and thus the power consumption can be minimum.

11.10 Supply-Independent Bias Circuitry [5]

As discussed previously, to achieve high power-supply rejection ratio, it is necessary to control the bias currents and make them insensitive to the variations in power supply.

A useful parameter that is popularly used to measure the change in a bias current IB to the change in the supply voltage VDD is the sensitivity, defined as

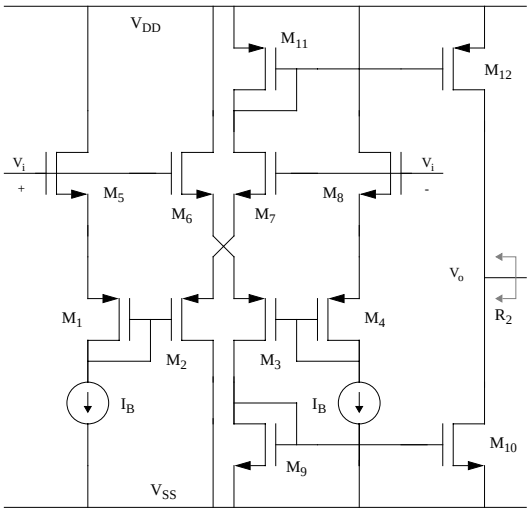

Fig. 11.23 A CMOS Class AB amplifier

$$S_{V_{DD}}^{I_B} = \frac{V_{DD}\partial I_B}{I_B \partial V_{DD}} \tag{11.39}$$

To achieve a supply-independent bias, the current must be generated not based on the supply voltage but based on some standard quantities, such as a base-emitter junction voltage V_{BE}, a MOS's threshold voltage V_{th}, or the thermal voltage V_T.

Figure 11.24 shows a simple bias circuit using V_{BE} as the reference. For large current gain β, it can be easily seen that

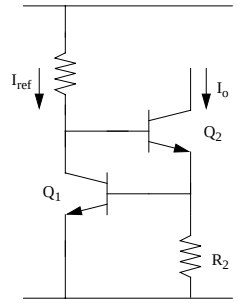

Fig. 11.24 A bias current source based on V_{BE}

$$I_o = \frac{V_{BE_1}}{R_2} = \frac{V_T}{R_2}\ln\left(\frac{I_{ref}}{I_{S_1}}\right) \tag{11.40}$$

The main problem with this circuit is that the supply voltage will inevitably affect the reference current and thus the voltage V_{BE}. The sensitivity is typically still too high to be useful.

An improved version is based on self-biasing circuit as shown in Fig. 11.25. In this case, the output current can be derived to be

$$I_o = \frac{V_{BE_1}}{R_2} = \frac{V_T}{R_2}\ln\left(\frac{I_{ref}}{I_{S_1}}\right) = \frac{V_T}{R_2}\ln\left(\frac{I_o}{I_{S_1}}\right) \tag{11.41}$$

In addition to the desired operating point, the circuit has zero as another stable point. As a result, in practice, it is important to include a start-up circuitry to ensure that the final operating point is not at zero.

Similar circuit configurations can be implemented in CMOS technology. Figure 11.26 shows one example of such a circuit, where the output current is based on the threshold voltage of MOS transistors. As long as the aspect ratio W/L of M_1 is large and the reference current is small, the saturation voltage ΔV_{GS} can be neglected, and

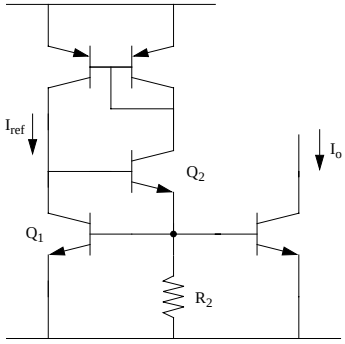

Fig. 11.25 A self-biasing BJT current source based on V_{BE}

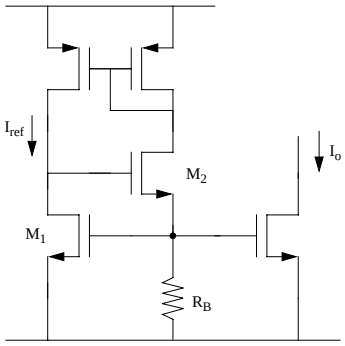

Fig. 11.26 A self-biasing CMOS current source based on V_{th}

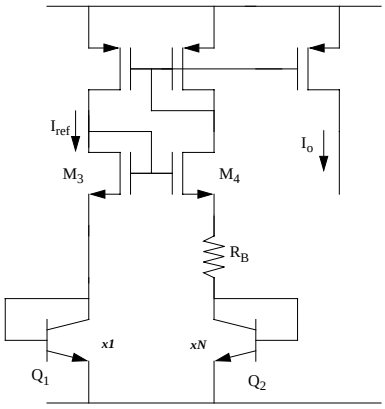

Fig. 11.27 A self-biasing CMOS current source based on the thermal voltage V_T

$$I_o = \frac{V_{GS_1}}{R_B} = \frac{V_{th} + \Delta V_{GS_1}}{R_B} \simeq \frac{V_{th}}{R_B} \tag{11.42}$$

The circuit shown in Figs. 11.25 and 11.26 can be modified so that the output current is dependent on the thermal voltage V_T. The basic idea is to generate the current using the difference between the base-emitter voltages of two bipolar transistors with different emitter areas. An implementation of such a bias circuit in a CMOS technology is shown in Fig. 11.27, where it can be proved that

$$I_o = \frac{V_{BE_1} - V_{BE_2}}{R_B} = \frac{V_T}{R_B}\ln\left(\frac{I_{S_2}}{I_{S_1}}\right) = \frac{V_T}{R_B}\ln N \tag{11.43}$$

11.11 Temperature-Independent Bias Circuitry [5]

As of now, we have only discussed how to generate bias voltages and currents that are independent of supply voltages. In practice, it is equally important to generate bias voltages and currents that are either independent of temperature or dependent on temperature in some well-controlled manner. Such a temperature-independent circuit can be realized using either Zener diodes or bandgap reference. However, since Zener diodes are not suitable for low-supply applications, we will focus only on the later.

The basic principle of a band-gap reference circuit is to combine a base-emitter junction voltage V_{BE}, which has a negative temperature coefficient of -2 mV/K, with a appropriately-scaled thermal voltage to achieve the desired temperature dependency.

Shown in Fig. 11.28 is a popular band-gap voltage reference. For CMOS processes, this circuit can also be implemented using parasitic vertical PNP transistors. With an ideal amplifier, it can be easily shown that the output voltage is given by

$$\begin{aligned} V_o &= V_{BE_2} + R_3 I_{C_2} = V_{BE_2} + R_1 I_{C_1} = V_{BE_2} + \frac{R_1}{R_2}(V_{BE_2} - V_{BE_1}) = V_{BE_2} + \frac{R_1}{R_2} V_T \ln\left(\frac{I_{S_1} I_{C_2}}{I_{S_2} I_{C_1}}\right) \\ &= V_{BE_2} + \frac{R_1}{R_2} V_T \ln\left(\frac{I_{S_1} R_1}{I_{S_2} R_3}\right) = V_{BE_2} + KV_T \end{aligned} \tag{11.44}$$

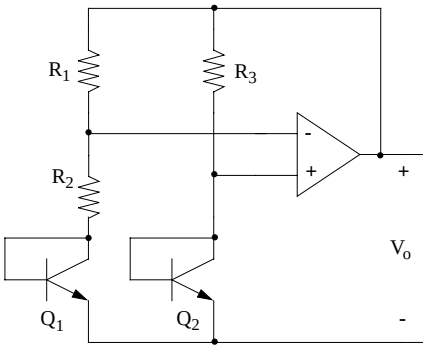

Fig. 11.28 A schematic of a band-gap reference circuit

where the constant K is given by

$$K = \frac{R_1}{R_2}\ln\left(\frac{I_{S_1}}{I_{S_2}}\frac{R_1}{R_3}\right) \tag{11.45}$$

The temperature coefficient of the output voltage TC becomes

$$TC(V_o) = \frac{\partial V_o}{\partial T} = \frac{\partial}{\partial T}V_{BE_2} + \frac{\partial}{\partial T}(KV_T) = -2mV + K\frac{k}{q} \tag{11.46}$$

With appropriate choices of the resistor ratios and the transistor sizes, the coefficient K and thus the temperature coeffient of the output voltage can be of any desirable value.

11.12 References

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