Large-Signal Transfer Function of Bipolar Differential Amplifier

- $V_{OD} = V_{O1} - V_{O2}$

  $V_{O1} = V_{CC} - I_{C1} R_C \qquad V_{O2} = V_{CC} - I_{C2} R_C$

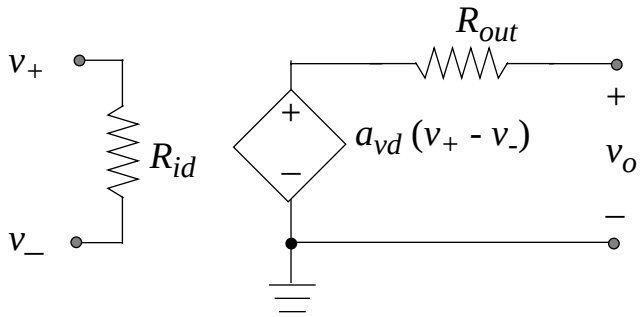
$$V_{OD} = (I_{C2} - I_{C1})R_C = \alpha_F I_{BIAS} R_C \left(\frac{1}{1 + e^{V_{ID}/V_{th}}} - \frac{1}{1 + e^{-V_{ID}/V_{th}}} \right)$$

... which can be written as:

$$V_{OD} = -\alpha_F I_{BIAS} R_C \tanh(V_{ID}/2V_{th})$$

Operational Amplifiers

- Two-port (differential) small-signal model of an op amp



- Ideal "general purpose" op amp:

  R_{id} --> infinity, R_{out} --> 0, a_{vd} --> infinity

  Examples: 741 op amp has

  R_{id} = 2.7 MΩ, R_{out} = 47 Ω, a_{vd} = 300,000 (approx).

  MOS inputs --> can get near-infinite differential input resistance

- *Many* other specifications ...

  DC input common-mode voltage range and output swings

  output current sourcing (out) or sinking (in) capability

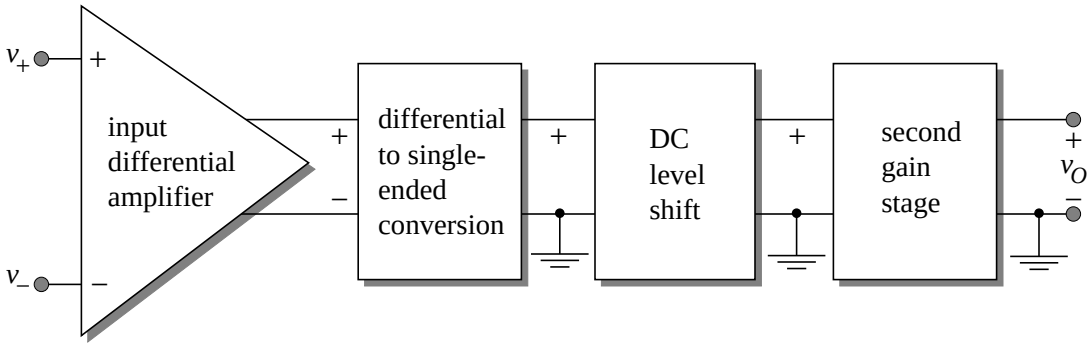
  offset voltage and its temperature dependence

Internal Op Amps

- "Internal" op amp: loads are *capacitive* --> no need for R_{out} --> 0 Ω

  therefore, *no* output stage (common-collector or common-drain)

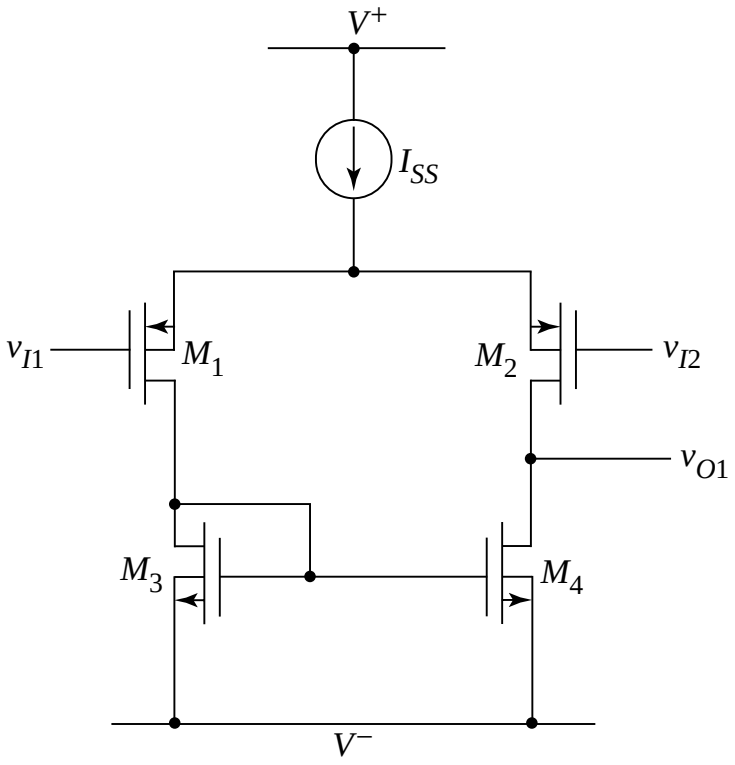
- Building block construction of an internal operational amplifier:



Differential Input Stage

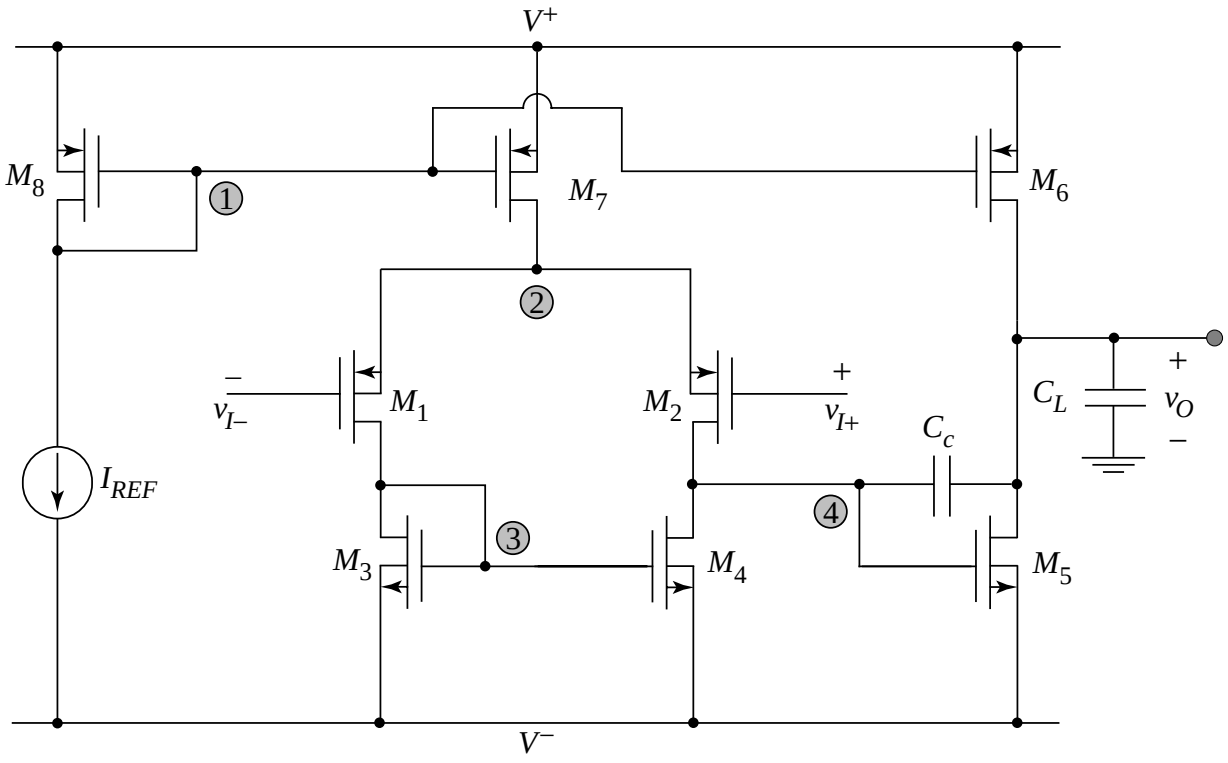
- By using a current-mirror, we can implement differential-to-single ended conversion together with the differential input stage (without loss of 3 dB gain)

  simple MOS version of input stage



Basic Two-Stage CMOS Op Amp Topology

- Add a second common-source gain stage to boost the overall voltage gain

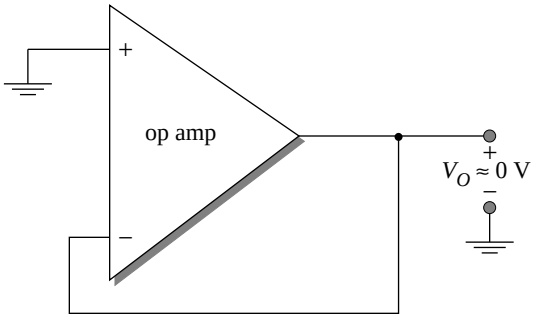


Capacitor C_c is important in the op amp frequency response

DC output is assumed to be $V_O = 0$ V

DC Bias Solution

- High gain --> place op amp in unity gain feedback loop to establish a stable DC operating point



- *Node 1*

  The source-gate voltage is defined by the DC current in M_8

$$V_1 = V^+ - \left(-V_{Tp} + \sqrt{\frac{2I_{REF}}{\mu_p C_{ox}(W/L)_8}} \right)$$

- *Node 2*

  The input voltages are at (nearly) zero volts, so the source-gate voltage of M_1 and M_2 determines V_2

$$V_2 = -V_{Tp} + \sqrt{\frac{2(-I_{D7}/2)}{\mu_p C_{ox}(W/L)_{1,2}}}$$

- *Node 3*

  The voltage is set by diode-connected M_3

$$V_3 = V^- + V_{Tn} + \sqrt{\frac{2(-I_{D7}/2)}{\mu_n C_{ox}(W/L)_{3,4}}}$$

DC Bias Solution (Cont.)

- *Node 4*

$$V_4 = V^- + V_{Tn} + \sqrt{\frac{2(-I_{D6})}{\mu_n C_{ox}(W/L)_5}}$$

- DC voltages of drains of M_1 and M_2 should be matched to avoid a systematic offset --> $V_3 = V_4$

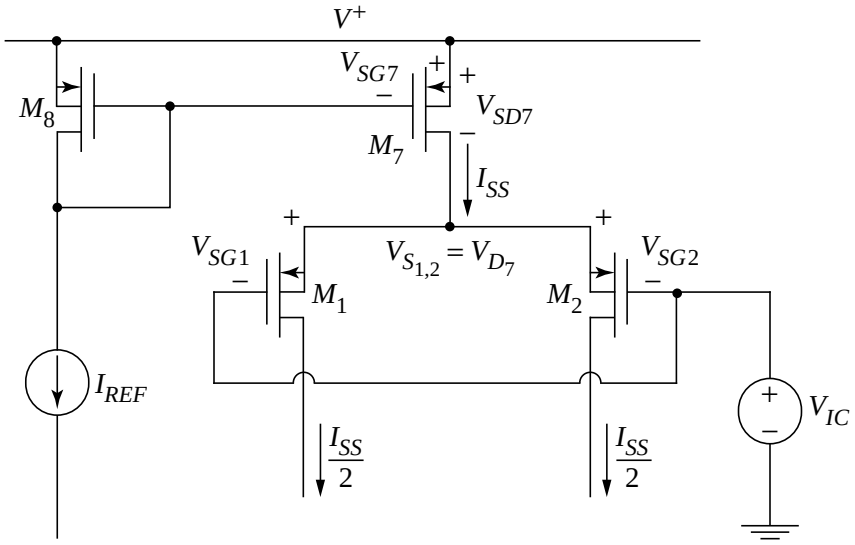
$$\sqrt{\frac{2(-I_{D7}/2)}{\mu_n C_{ox}(W/L)_{3,4}}} = \sqrt{\frac{2(-I_{D6})}{\mu_n C_{ox}(W/L)_5}}$$

$$\frac{-I_{D6}}{-I_{D7}} = \frac{(W/L)_5}{2(W/L)_{3,4}} = \frac{(W/L)_6}{(W/L)_7}$$

where the second equality follows from $V_{SG6} = V_{SG7}$

Common-Mode Input Voltage Range

- As V_{IC} increases, Node 2 follows and eventually M_7 will enter the triode region



$$V_{SD7} = V^+ - (V_{IC} + V_{SG1})$$

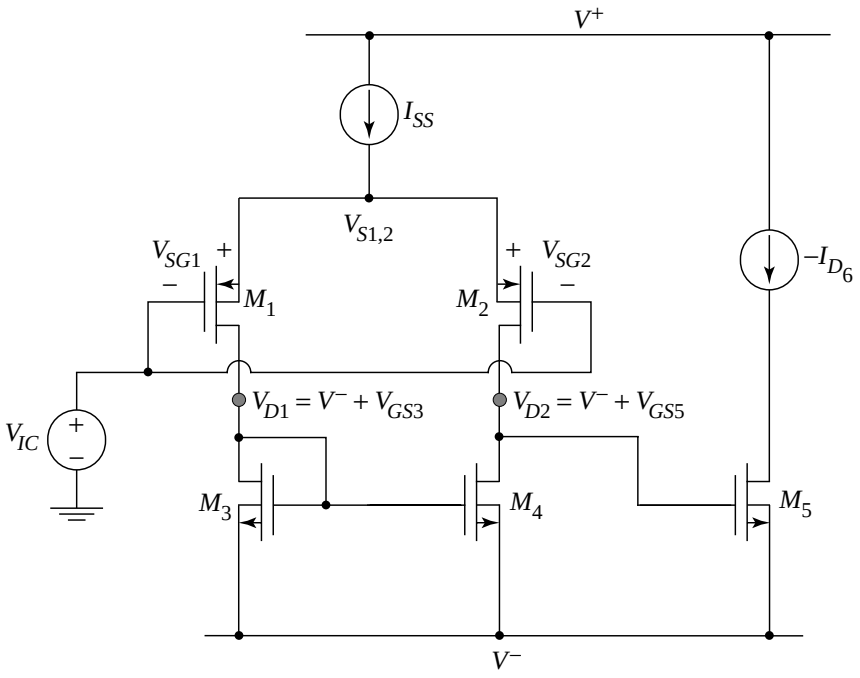
Maximum input common-mode voltage:

$$V_{SD7(sat)} = V_{SG7} + V_{Tp} = V^+ - (V_{IC,max} + V_{SG1})$$

$$V_{IC,max} = V^+ - V_{Tp} - V_{SG1} - V_{SG7}$$

Common-Mode Input Voltage Range (Cont.)

- As V_{IC} decreases, the input pair will eventually enter the triode region



$$V_{SD1} = (V_{IC} + V_{SG1}) - (V^{-} + V_{GS3}) \geq V_{SG1} + V_{Tp}$$

When M_1 just enters the triode region,

$$V_{IC,min} = V^{-} + V_{GS3} + V_{Tp} = V^{-} + V_{Tp} + V_{Tn} + \sqrt{\frac{2(I_{SS}/2)}{\mu_n C_{ox}(W/L)_3}}$$

Output Voltage Range

- The output node can increase until M_6 enters the triode region

$$V_{SD6} = V^+ - V_O \geq V_{SG6} + V_{Tp}$$

so the maximum output voltage is

$$V_{O,max} = V^+ - V_{Tp} - V_{SG6} = V^+ - \sqrt{\frac{2(-I_{D6})}{\mu_p C_{ox}(W/L)_6}}$$

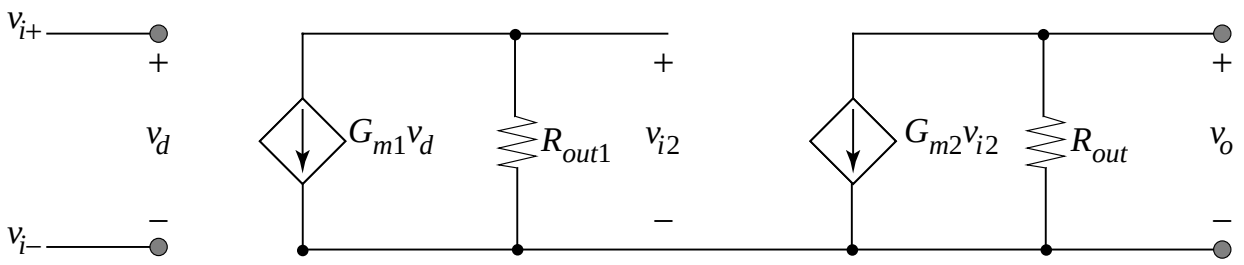
- Similarly, the output node can decrease until M_5 enters the triode region

$$V_{DS5} = V_O - V^- \geq V_{GS5} - V_{Tn}$$

$$V_{O,min} = V^- + \sqrt{\frac{2(-I_{D6})}{\mu_n C_{ox}(W/L)_5}}$$

Small-Signal Analysis of CMOS Two-Stage Op Amp

- Cascade two-port models of differential amplifier with current-mirror supply (input stage) and common-source amplifier with current supply (second gain stage)



- First stage:

  polarity of G_{m1} is inverted to reflect reversal of input terminals ... which is done to make the overall gain positive for $v_d > 0$

  $G_{m1} = g_{m1}$

  $R_{out1} = r_{o2} \parallel r_{o4}$

- Second stage:

  $G_{m2} = g_{m5}$

  $R_{out} = r_{o5} \parallel r_{o6}$

$$a_{vdo} = (-G_{m1}R_{out1})(-G_{m2}R_{out})$$

$$a_{vdo} = g_{m1}(r_{o2}||r_{o4})g_{m5}(r_{o5}||r_{o6})$$

Two-Stage CMOS Design Example

- Design constraints

  Typical situation for an internal op amp: area and power are both limited.

  Simplified area constraint -- set W_{max} = 150 μm

  (for minimize channel-length modulation, set L_{min} = 3 μm)

  Set DC power budget at 1.25 mW (including reference current) for case where we have symmetrical supplies: V^+ = 2.5 V and V^- = - 2.5 V.

- Initial Transistor Sizing:

  Make $(W/L)_1$ = (150 μm / 3 μm) in order to maximize G_{m1} and maximize common-mode input voltage range

  DC currents: assume I_{REF} = 50 μA

  Set DC bias current of differential amplifier = DC bias of common-source stage = 100 μA each as a first-cut --> total current drawn is 250 μA --> power spec. is just met

  Transistor dimensions: $(W/L)_5$ = (150 μm / 3 μm) to maximize g_{m5}

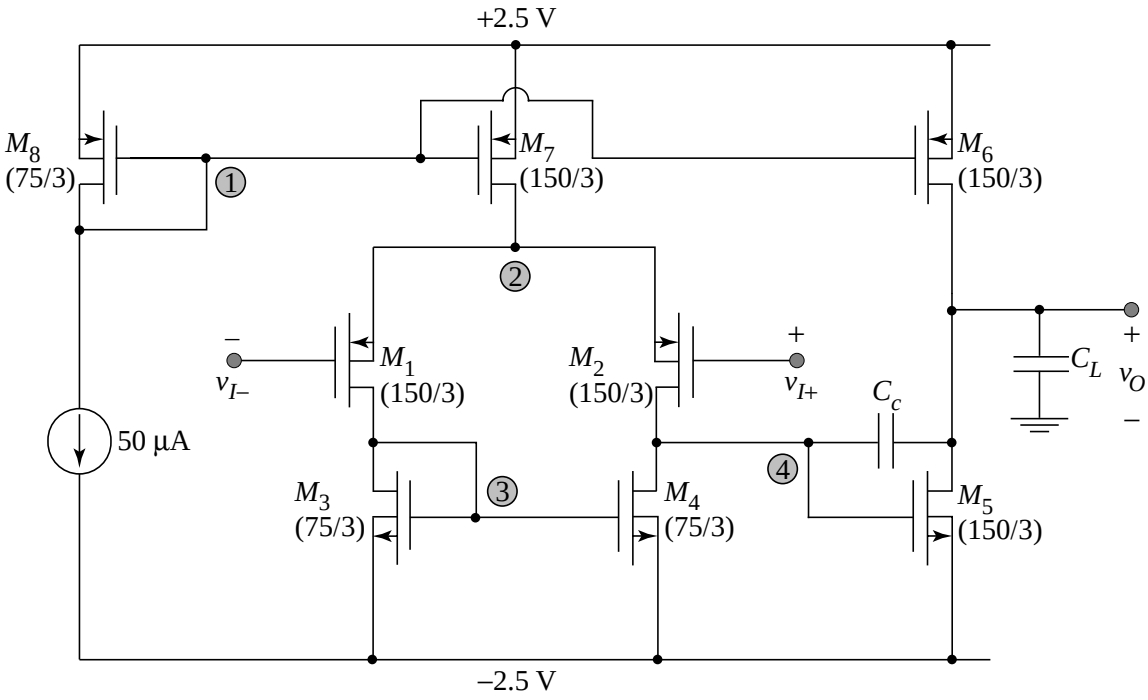
$$\frac{(W/L)_5}{2(W/L)_{3,4}} = \frac{-I_{D6}}{I_{D7}} = \frac{100\ \mu A}{100\ \mu A} = 1$$

  Therefore $(W/L)_{3,4} = (W/L)_5 /2 = 25$ --> $W_{3,4}$ = 75 μm since we use L_{min} to save area.

  For symmetrical output swing, we set $(W/L)_6 = (W/L)_5$ = (150 μm / 3 μm)

  To maximize common-mode input range, we also set $(W/L)_7$ = (150 μm / 3 μm)

First-Cut CMOS Two-Stage Op Amp



n-channel MOSFET

$\mu_n C_{ox} = 50 \frac{\mu A}{V^2}$	$t_{ox} = 15$ nm	$C_{ov} = 0.5$ fF/µm	$\phi_{Bn} = 0.95$ V
$V_{TOn} = 1.0$ V	$\lambda_n = \frac{0.1(\mu m/V)}{L}$	$C_{jno} = 0.1$ fF/µm^2	$m_{jn} = 0.5$
$\gamma_n = 0.6$ V$^{1/2}$	$2\phi_p = -0.8$ V	$C_{jswno} = 0.5$ fF/µm	$m_{jswn} = 0.33$

p-channel MOSFET

$\mu_p C_{ox} = 25 \frac{\mu A}{V^2}$	$t_{ox} = 15$ nm	$C_{ov} = 0.5$ fF/µm	$\phi_{Bp} = 0.95$ V
$V_{TOp} = -1.0$ V	$\lambda_p = \frac{0.1(\mu m/V)}{L}$	$C_{jpo} = 0.3$ fF/µm^2	$m_{jp} = 0.5$
$\gamma_p = 0.6$ V$^{1/2}$	$2\phi_n = 0.8$ V	$C_{jswpo} = 0.35$ fF/µm	$m_{jswp} = 0.33$

DC Bias Solution

- Assume that the DC input voltages are $V_{I+} = V_{I-} = 0$ V and $V_O = 0$ V

- Input common-mode voltage range

$$V_{IC,max} = 2.5\text{ V} - (-1\text{ V}) - 1.28\text{ V} - 1.4\text{ V} = 0.82\text{ V}$$

$$V_{IC,min} = -2.5\text{ V} + 1.28\text{ V} + (-1\text{ V}) = -2.22\text{ V}$$

  room for improvement in the upper limit -- possible at the expense of increased area (W/L) ratios must be increased.

- Output voltage swing

$$V_{O,max} = 2.5\text{ V} - 0.4\text{ V} = 2.1\text{ V}$$

$$V_{O,min} = -2.5\text{ V} + 0.28\text{ V} = -2.22\text{ V}$$

  output range in nearly symmetrical and adequate

Small-Signal Performance

- Small-signal parameters:

  $g_{m1} = g_{m2} = 357\ \mu S$

  $g_{m5} = 2\ g_{m1} = 714\ \mu S$

  $r_{o2} = r_{o4} = 600\ k\Omega$

  $r_{o5} = r_{o6} = 300\ k\Omega$

- Differential voltage gain:

$$a_{vdo} = (0.357)(600||600)(714)(300||300) = 1.15\times 10^4$$

in decibels, $|a_{vdo}|_{dB} = 81$ dB.