

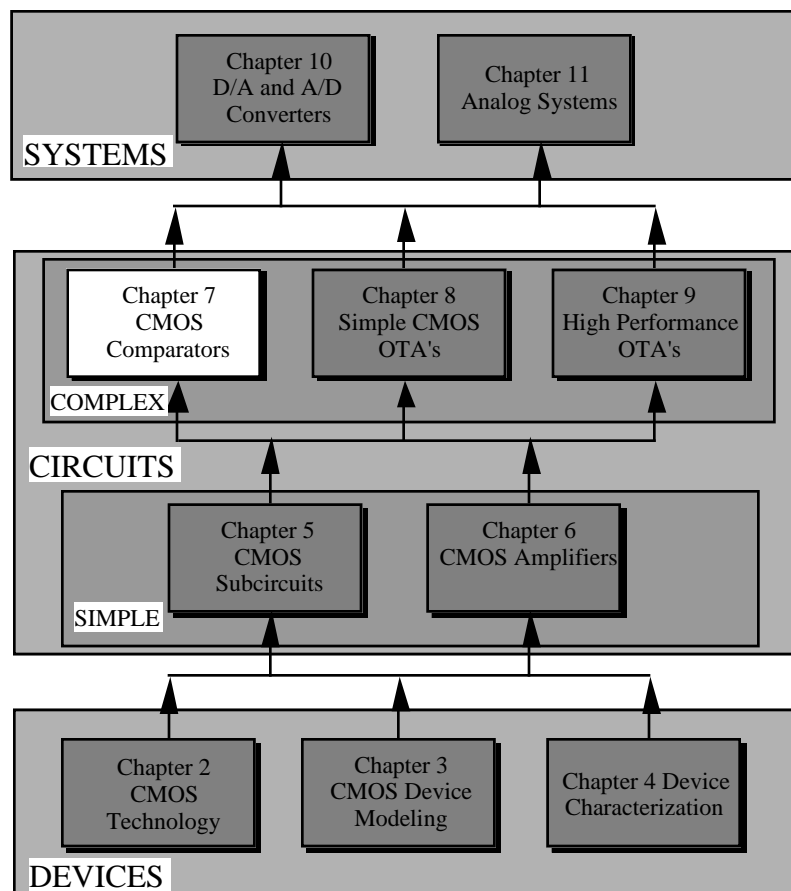
SECTION 7 - COMPARATORS

VII. COMPARATORS

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- VI.1 Comparators Models and Performance
- VI.2 Development of a CMOS Comparator
- VI.3 Design of a Two-Stage CMOS Comparator
- VI.4 Other Types of Comparators
- VI.5 Improvement in Comparator Performance
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 - B. Autozeroing
- VI.6 High Speed Comparators

Organization



VII.1 - CHARACTERIZATION OF COMPARATORS

What is a Comparator?

A comparator is a circuit which compares two analog signals and outputs a binary signal based on the comparison. (It can be an op amp without frequency compensation.)

Characterization of Comparators

We shall characterize the comparator by the following aspects:

- Resolving capability
- Speed or propagation time delay
- Maximum signal swing limits
- Input offset voltage
- Other Considerations

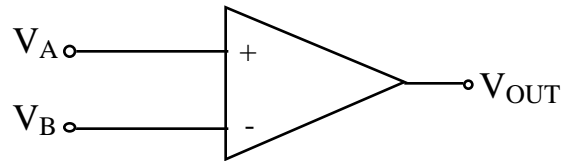
Noise

Power

Etc.

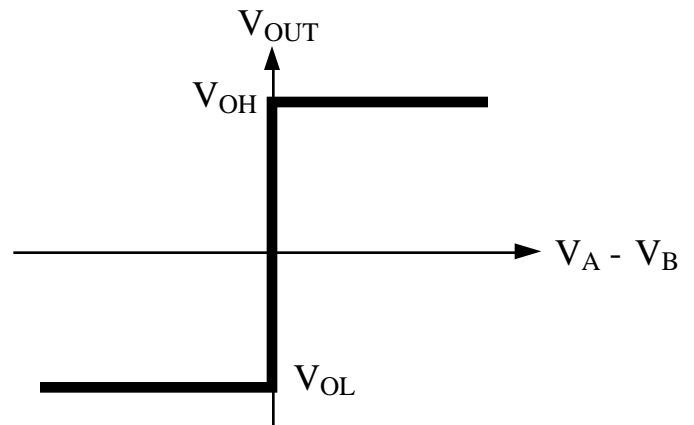
VOLTAGE COMPARATORS

Definition of a Comparator



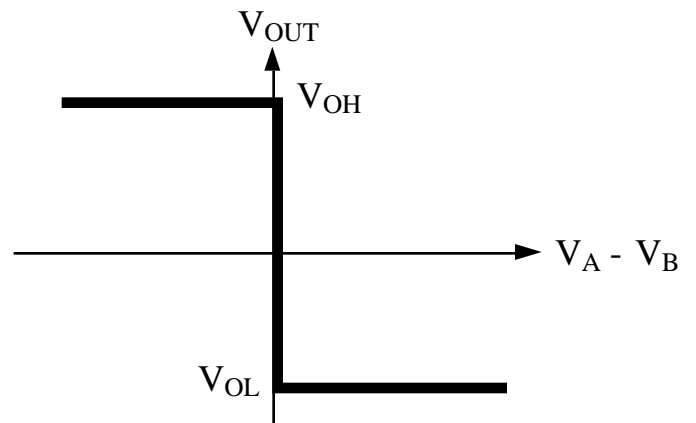
Noninverting

$$V_{OUT} = \begin{cases} V_{OH} & \text{when } V_A \geq V_B \\ V_{OL} & \text{when } V_A < V_B \end{cases}$$



Inverting

$$V_{OUT} = \begin{cases} V_{OL} & \text{when } V_A \geq V_B \\ V_{OH} & \text{when } V_A \leq V_B \end{cases}$$



COMPARATOR PERFORMANCE

1. Speed or propagation time delay.

The amount of time between the time when $V_A - V_B = 0$ and the output is 50% between initial and final value.

2. Resolving capability.

The input change necessary to cause the output to make a transition between its two stable states.

3. Input common mode range.

The input voltage range over which the comparator can detect $V_A = V_B$.

4. Output voltage swing (typically binary).

5. Input offset voltage.

The value of V_{OUT} reflected back to the input when V_A is physically connected to V_B .

APPROACHES TO THE DESIGN OF VOLTAGE COMPARATORS

Open Loop

Use of a high-gain differential amplifier.

$$\text{Gain} = \frac{V_{OH} - V_{OL}}{\text{resolution of the comparator}}$$

Regenerative

Use of positive feedback to detect small differences between two voltages, V_A and V_B . I.e., sense amplifiers in digital memories.

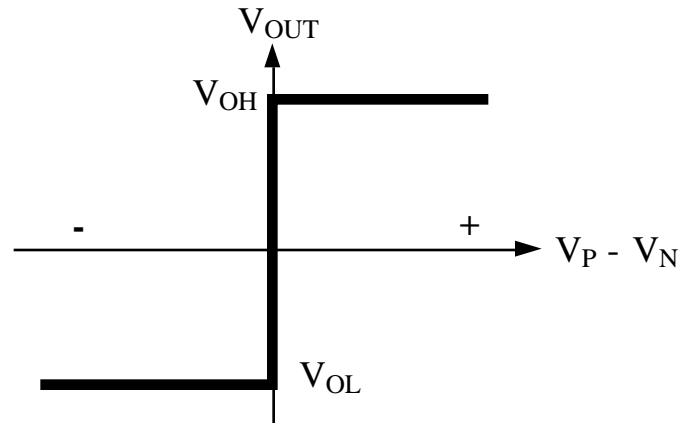
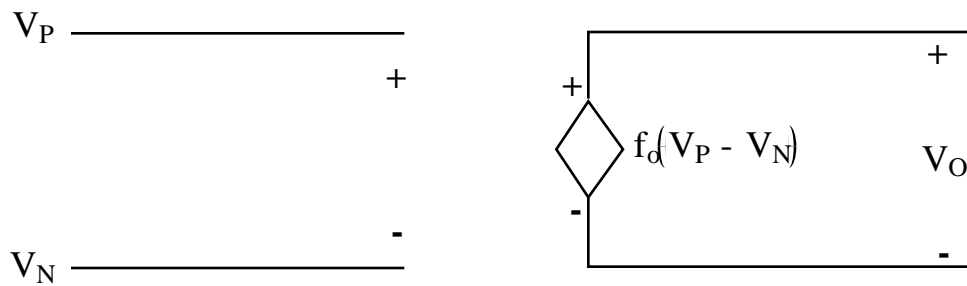
Open Loop - Regenerative

Use of low gain, high speed comparator cascaded with a latch. Results in comparators with very low propagation time delay.

Charge Balancing

Differential charging of a capacitor. Compatible with switched capacitor circuit techniques.

Type	Offset Voltage (Power supply)	Resolution	Speed (8 bit)
Open-loop	1-10 mV	300 μ V (\pm 5V)	10 MHz
Regenerative	0.1 mV	50 μ V (\pm 5V)	50 MHz
Charge Balancing	0.1 mV	5mV (5V)	30 MHz

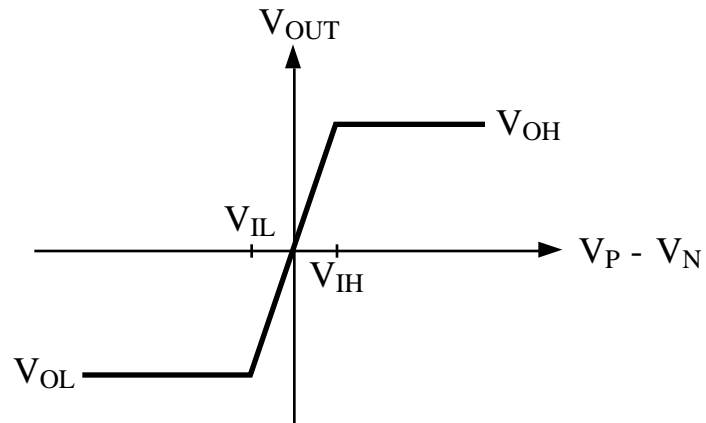
COMPARATOR MODELS - OPEN LOOPZero Order ModelModel

$$f_O(V_P - V_N) = \begin{cases} V_{OH} & \text{for } (V_P - V_N) \geq 0 \\ V_{OL} & \text{for } (V_P - V_N) \leq 0 \end{cases}$$

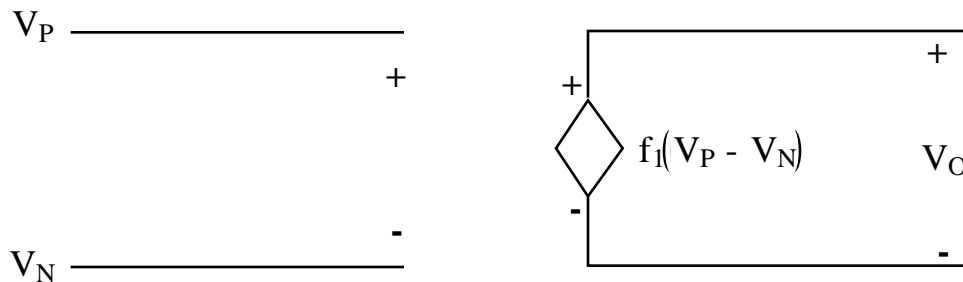
COMPARATOR MODELS - CONT'D

First Order Model

Transfer Curve



Model

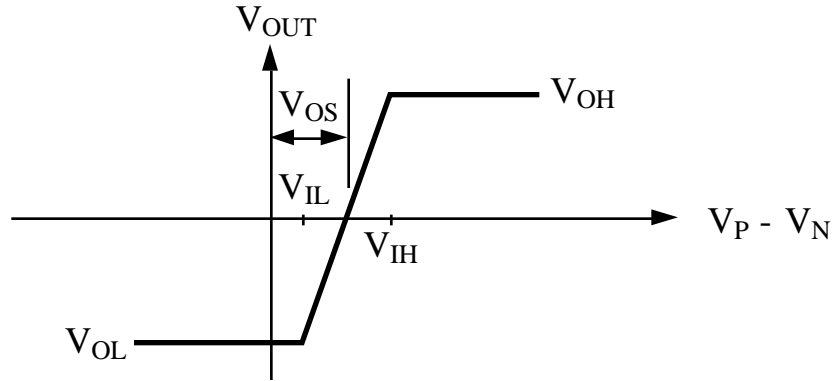


$$f_1(V_P - V_N) = \begin{cases} V_{OH} & \text{for } (V_P - V_N) \geq V_{IH} \\ A_V(V_P - V_N) & \text{for } V_{IL} \leq (V_P - V_N) \leq V_{IH} \\ V_{OL} & \text{for } (V_P - V_N) \leq V_{IL} \end{cases}$$

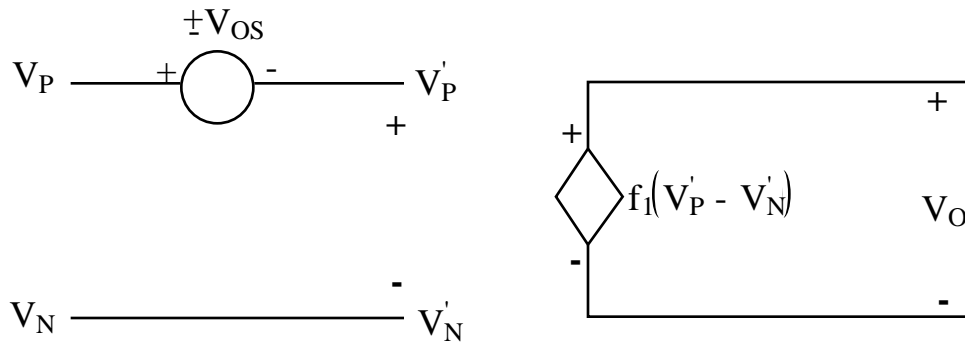
COMPARATOR MODELS - CONT'D

First Order Model with Offset

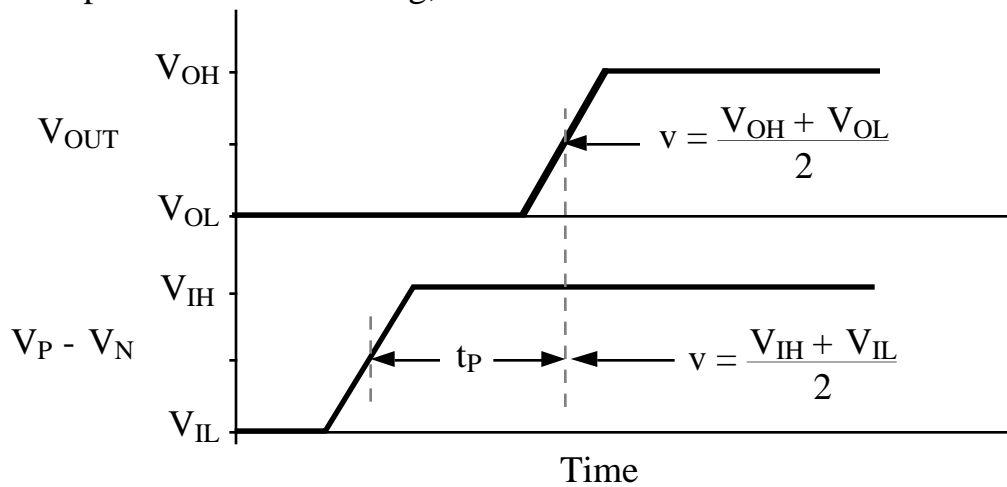
Transfer Curve



First Order Model with Offset



Time Response of Noninverting, first order model



VII.2 - DEVELOPMENT OF A CMOS COMPARATOR

SIMPLE INVERTING COMPARATOR

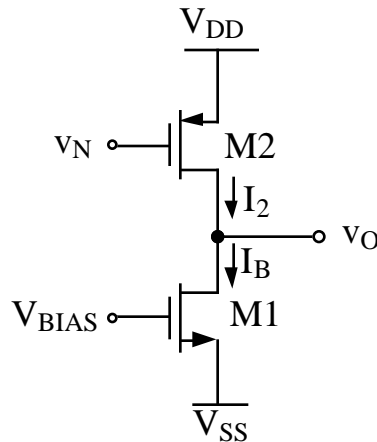


Fig. 7.2-1 Simple inverting comparator

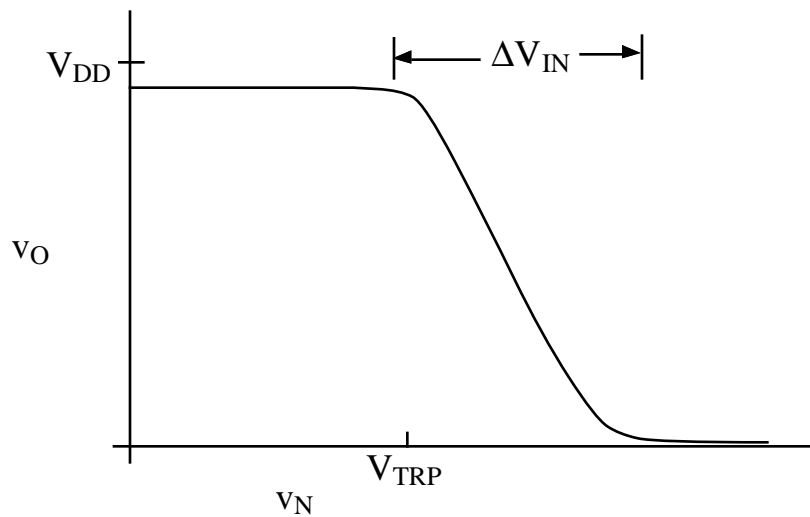
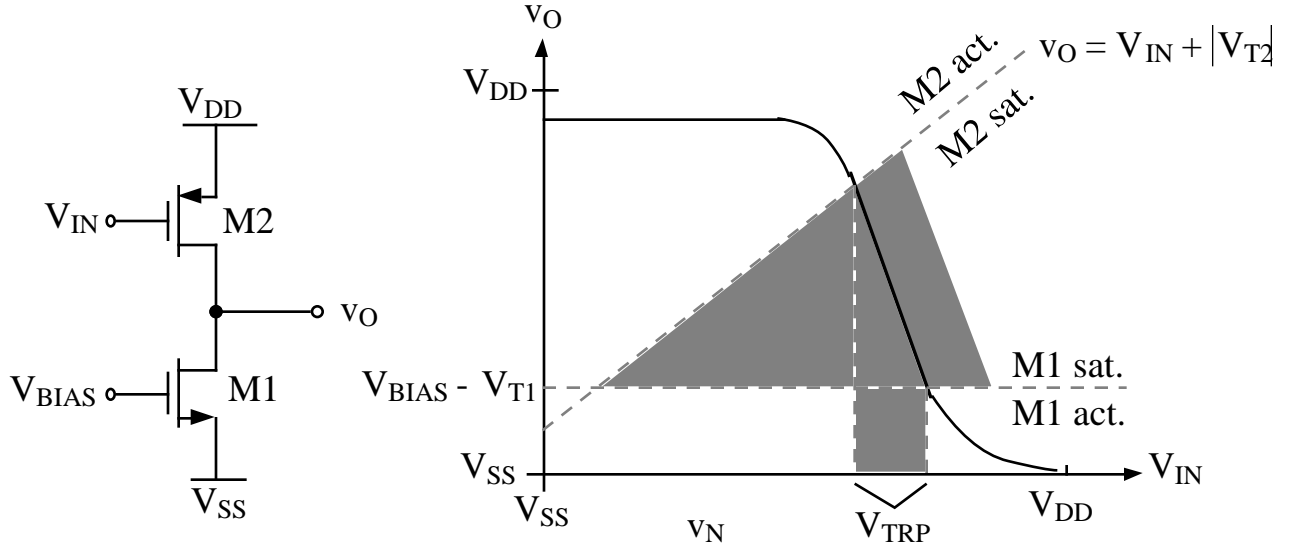


Fig. 7.2-2 DC transfer curve of a simple comparator

Low gain \Rightarrow Poor resolution

$$V_{TRP} = f(V_{DD}) + \text{process parameters}$$

CALCULATION OF THE TRIP POINT, V_{TRP}



Operating Regions-

$$v_{DS1} \geq v_{GS1} - V_T \quad \text{' } v_O - V_{SS} \geq V_{BIAS} - V_{SS} - V_{T1}$$

$$\underline{\underline{v_O \geq V_{BIAS} - V_{T1}}}$$

$$v_{SD2} \geq v_{SG2} - |V_{T2}| \quad \text{' } V_{DD} - v_O \geq V_{DD} - v_{IN} - |V_{T2}|$$

$$\underline{\underline{v_O \leq v_{IN} + |V_{T2}|}}$$

Trip Point-

Assume both M1 and M2 are saturated, solve and equate drain currents for V_{TRP} . Assume $\lambda \approx 0$.

$$i_{D1} = \frac{K_N}{2} \frac{W_1}{L_1} (V_{BIAS} - V_{SS} - V_{T1})^2$$

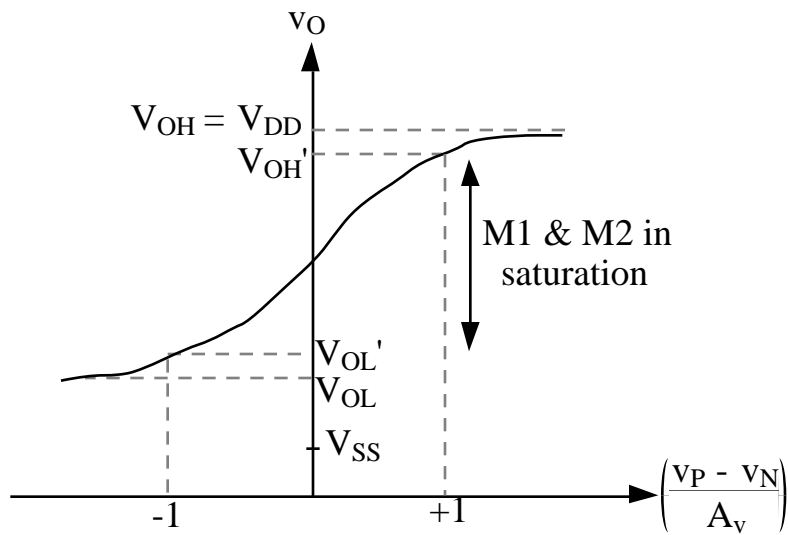
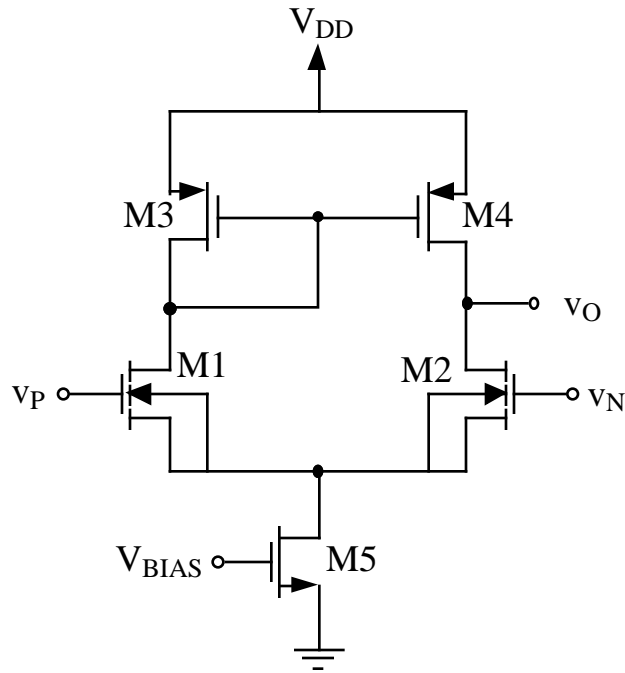
$$i_{D2} = \frac{K_P}{2} \frac{W_2}{L_2} (V_{DD} - v_{IN} - |V_{T2}|)^2$$

$$i_{D1} = i_{D2} \quad \text{' } \boxed{v_{IN} = V_{TRP} = V_{DD} - |V_{T2}| - \sqrt{\frac{K_N(W_1/L_1)}{K_P(W_2/L_2)} (V_{BIAS} - V_{SS} - V_{T1})}}$$

I.e. $V_{DD} = -V_{SS} = 5V$, $V_{BIAS} = -2V$ and $K_N \left(\frac{W_1}{L_1}\right) = K_P \left(\frac{W_2}{L_2}\right)$

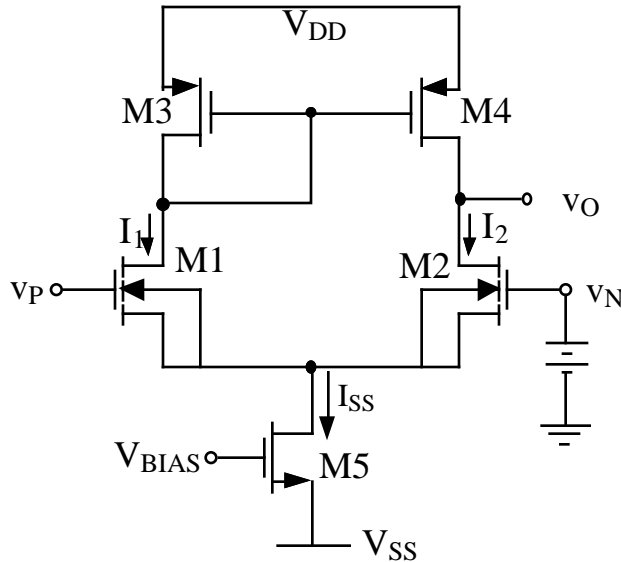
$$V_{TRP} = 5 - 1 - (-2 + 5 - 1) = 4 - 2 = \underline{\underline{2V}}$$

COMPARATOR USING A DIFFERENTIAL AMPLIFIER



Gain is still low for a comparator

DERIVATION OF OUTPUT SWING LIMITS



$v_P > v_N$

1. Current in M1 increases and current in M2 decreases.
2. Mirroring of M3-M4 will cause v_O to approach V_{DD} .
3. $V_{OH}' = V_{DD} - V_{DS4}(sat)$

$$V_{OH}' = V_{DD} - \sqrt{\frac{I_4}{\beta_4}}$$

$$V_{OH}' = V_{DD} - \sqrt{\frac{I_5}{K_p'(W_4/L_4)}}$$

$$\underline{\underline{V_{OH}' = V_{DD} - \sqrt{\frac{I_5}{K_p'(W_3/L_3)}}}}$$

$v_P < v_N$

Assume v_N is a fixed DC voltage

1. v_O starts to decrease, M3-M4 mirror is valid so that $I_1 = I_2 = I_{SS}/2$.
2. $V_{OL}' = v_N - V_{GS2} + V_{DS2}$
when M2 becomes non-sat. we have $V_{DS2}(sat) = V_{GS2} - V_T$ so that

$$\underline{\underline{V_{OL}' = v_N - V_{T2}}}$$

3. For further decrease in v_O , M2 is non-sat

and therefore the V_{GS2} can increase allowing the sources of M1 and M2 to fall (as v_P falls).

} I_1 still equals I_2 due to mirror

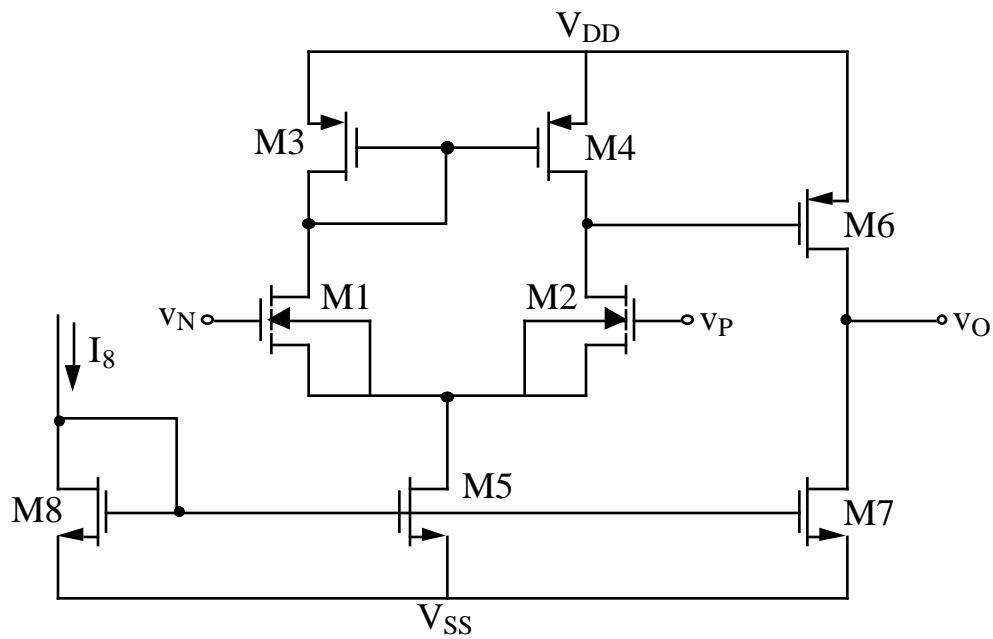
4. Eventually M5 becomes non-sat and I_5 starts to decrease to zero. M2 becomes a switch and v_O tracks $V_{S2}(V_{DS5})$ all the way to V_{SS} .

$$\therefore \underline{\underline{V_{OL} = V_{SS}}}$$

TWO-STAGE COMPARATOR

Combine the differential amplifier stage with the inverter stage.

- Sufficient gain.
- Good signal swing.



VII.3 - DESIGN OF A TWO-STAGE CMOS COMPARATOR

DC BALANCE CONDITIONS FOR TWO-STAGE COMPARATOR

- Try to keep all devices in saturation - more gain and wider signal swings.
- Based on gate-source and DC current relationship. I.e. if M1 and M2 are two matched devices and if $V_{GS1} = V_{GS2}$, then $I_{D1} = I_{D2}$ or vice versa.

Let $S_1 = \frac{W_1}{L_1}$,

M1 and M2 matched gives $S_1 = S_2$.

M3 and M4 matched gives $S_3 = S_4$.

also, $I_1 = I_2 = 0.5I_5$.

From gate-source matching, we have

$$V_{GS5} = V_{GS7} \quad I_7 = I_5 \left(\frac{S_7}{S_5} \right) \quad \text{and} \quad I_6 = I_4 \left(\frac{S_6}{S_4} \right) \quad \leftarrow \text{Assume}$$

$$V_{GS4} = V_{GS6}$$

For balance conditions, I_6 must be equal to I_7 , thus

$$\frac{I_5}{I_4} \cdot \frac{S_7}{S_5} = \frac{S_6}{S_4}$$

Since $\frac{I_5}{I_4} = 2$, then DC balance is achieved under the following:

$$\boxed{\frac{S_6}{S_4} = 2 \cdot \frac{S_7}{S_5}} \quad \text{' } V_{DG4} = 0 \quad \text{' M4 is saturated.}$$

SYSTEMATIC OFFSET ERROR

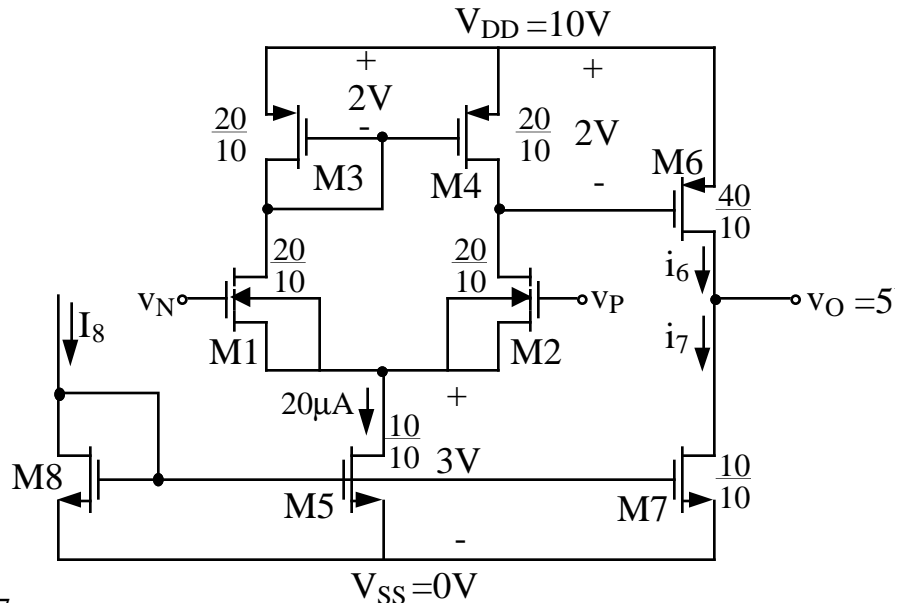
$$K_N = 24.75 \mu\text{A}/\text{V}^2$$

$$K_P = 10.125 \mu\text{A}/\text{V}^2$$

$$V_{TN} = -V_{TP} = 1\text{V}$$

$$\lambda_N = 0.015\text{V}^{-1}$$

$$\lambda_P = 0.020\text{V}^{-1}$$



Find V_{OS} to make $i_6 = i_7$

(1) Find the mismatch between i_6 and i_7

$$\frac{i_7}{i_5} = \left(\frac{1 + \lambda_N v_{DS7}}{1 + \lambda_N v_{DS5}} \right) \left(\frac{W_7/L_7}{W_5/L_5} \right) = \frac{1 + (0.015)(5)}{1 + (0.015)(3)} \quad (1) = 1.029$$

$$\frac{i_6}{i_4} = \left(\frac{1 + \lambda_P v_{DS6}}{1 + \lambda_P v_{DS4}} \right) \left(\frac{W_6/L_6}{W_4/L_4} \right) = \frac{1 + (0.02)(5)}{1 + (0.02)(2)} \quad (2) = 2.115$$

$$i_5 = 2i_4$$

$$\therefore i_7 = (1.029)(2)i_4 = 2.057i_4 \quad \text{and} \quad i_6 = 2.115i_4$$

(2) Find how much v_{GS6} must be reduced to make $i_6 = i_7$

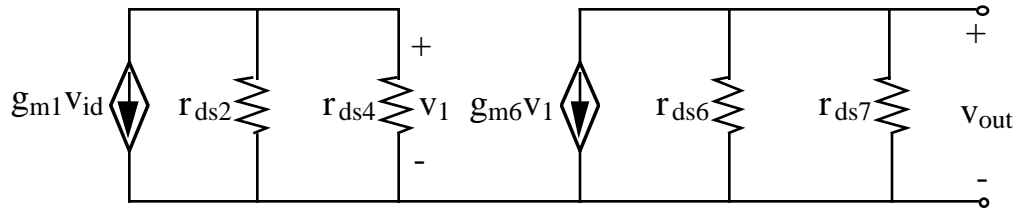
$$\Delta v_{GS6} = v_{GS6}(2.115i_4) - v_{GS6}(2.057i_4)$$

$$\Delta v_{GS6} = \sqrt{\frac{2L_6}{K_P W_6}} i_4 (\sqrt{2.115} - \sqrt{2.057}) = 14.11 \text{ mV}$$

(3) Reflecting Δv_{GS6} into the input

$$A_v(\text{diff}) = \left(\frac{2}{\lambda_2 + \lambda_4} \right) \sqrt{\frac{K_N (W_2/L_2)}{I_5}} = 89.9$$

$$\therefore V_{OS} = \frac{\Delta v_{GS6}}{A_v(\text{diff})} = \frac{14.1 \text{ mV}}{89.9} = \underline{\underline{0.157 \text{ mV}}}$$

GAIN OF THE TWO-STAGE COMPARATOR

$$V_{id} = V_P - V_N$$

$$A_v = \left(\frac{g_{m1}}{g_{ds2} + g_{ds4}} \right) \left(\frac{g_{m6}}{g_{ds6} + g_{ds7}} \right)$$

$$A_v = \frac{2 \sqrt{K_N K_P \left(\frac{W_1}{L_1} \right) \left(\frac{W_6}{L_6} \right)}}{(\lambda_2 + \lambda_4)(\lambda_6 + \lambda_7) \sqrt{I_1 I_6}}$$

Using $\frac{W_1}{L_1} = 5$, $\frac{W_6}{L_6} = 5$, $\lambda_N = 0.015V^{-1}$, $\lambda_P = 0.02V^{-1}$

and Table 3.1-2 values;

$$A_v = \frac{2 \sqrt{(17)(8)(5)(5)}}{(0.015+0.02)^2 \sqrt{I_1 I_6}} \cdot 10^{-6} = \frac{95199 \cdot 10^{-6}}{\sqrt{I_1 I_6}}$$

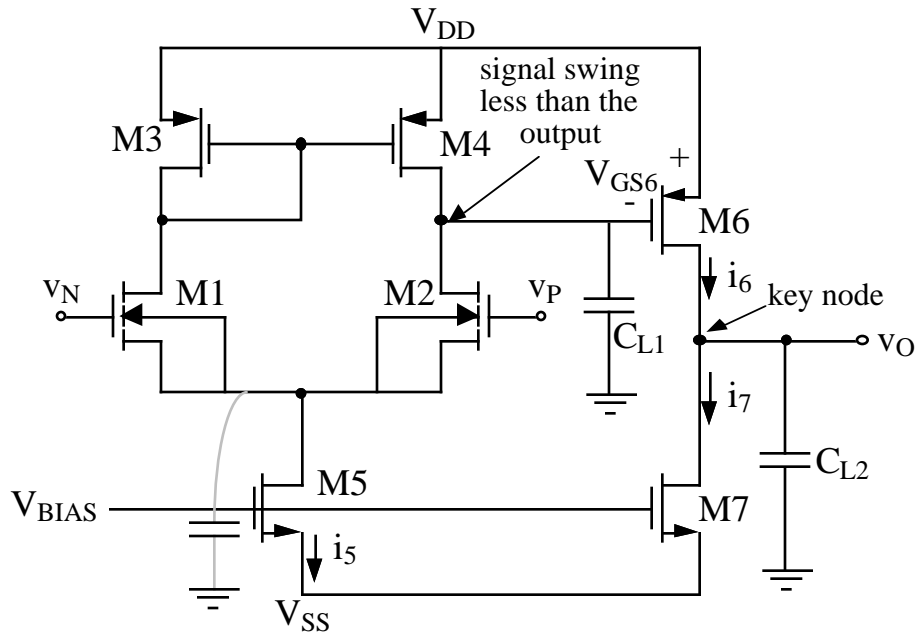
Assume $I_1 = 10 \mu A$ and $I_6 = 100 \mu A$

$$\underline{\underline{A_v = 3010}}$$

$$\frac{V_{OH} - V_{OL}}{A_v} = \text{Resolution} = 5 \text{ mV (assume)}$$

$$\text{then } V_{OH} - V_{OL} = \frac{5}{1000} \cdot 3000 = 15 \text{ Volts}$$

PROPAGATION DELAY OF THE TWO-STAGE COMPARATOR

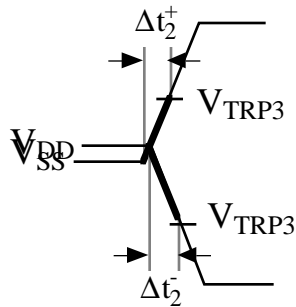


$$V_{GS6} = V_{DD} - (v_P + V_{DG2})$$

$$i_C = C \frac{dv}{dt}, \Delta t =$$

$$C \frac{\Delta v}{I}$$

$$\Delta t_{2+} = C_{L2} \left[\frac{V_{TRP3} - V_{SS}}{\frac{K_P W_6}{2 L_6} (V_{DD} - v_P - V_{DG2} - |V_{T6}|)^2 - I_7} \right]$$

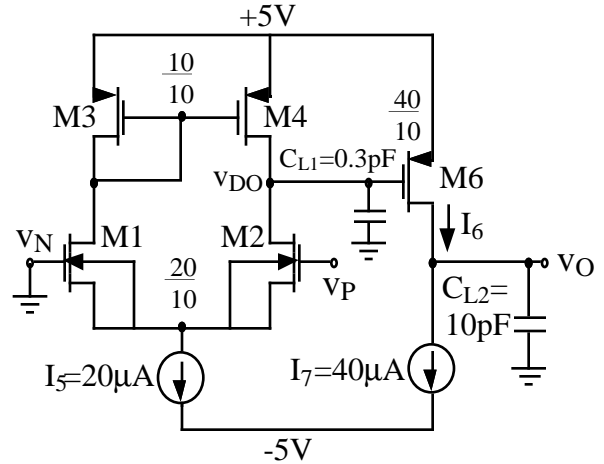


$$\Delta t_{2-} = C_{L2} \left[\frac{V_{DD} - V_{TRP3}}{\left(\frac{W_7}{L_7}\right) \left(\frac{L_5}{W_5}\right) i_5} \right]$$

$$\text{Slew rate} = \frac{i_{\text{source/sink}}}{C_{Li}}$$

CALCULATION OF COMPARATOR PROPAGATION DELAY

Find the total propagation delay of the comparator shown when the input v_P goes from -1 to $+1$ in 2ns . Assume the trip point of the output (next stage) is zero.



Total delay = 1st stage delay + 2nd stage delay

$$\Delta t = \Delta t_1 + \Delta t_2$$

$$\Delta t_1 = \frac{(v_{DO}(t_0) - V_{TRP2})}{I_5} C_{L1},$$

$$v_{DO}(t_0) = 5 \text{ because } v_P = -1\text{V}$$

$$V_{TRP2} = V_{DD} - V_{GS6}, \quad V_{GS6} = |V_{T6}| + \sqrt{\frac{2I_7}{K_{P6}'(W_6/L_6)}}$$

$$V_{GS6} = 1 + \sqrt{\frac{2 \cdot 40}{8 \cdot 4}} = 2.58 \text{ V}, \quad V_{TRP2} = 5 - 2.58 = 2.42 \text{ V}$$

$$\therefore \Delta t_1 = (5 - 2.42) \left(\frac{0.3 \text{ pF}}{20 \mu\text{A}} \right) = 38.7 \text{ ns}$$

$$\Delta t_2 = |v_O(t_0) - 0| \left(\frac{C_{L2}}{I_6 - I_7} \right) = 5 \left(\frac{C_{L2}}{I_6 - I_7} \right)$$

$$I_6 = \frac{K_{P6}'}{2} \left(\frac{W_6}{L_6} \right) (V_{DD} - V_{DO}(\min) - |V_{T6}|)^2$$

[$V_{DO}(\min)$ is an optimistic assumption based on $v_{DS2} \approx 0$]

$$V_{DO}(\min) \approx v_{DS2}(\approx 0) - v_{GS1} + v_N = -V_{T1} - \sqrt{\frac{I_5}{K_{N1}' \cdot 2}} = -1.77$$

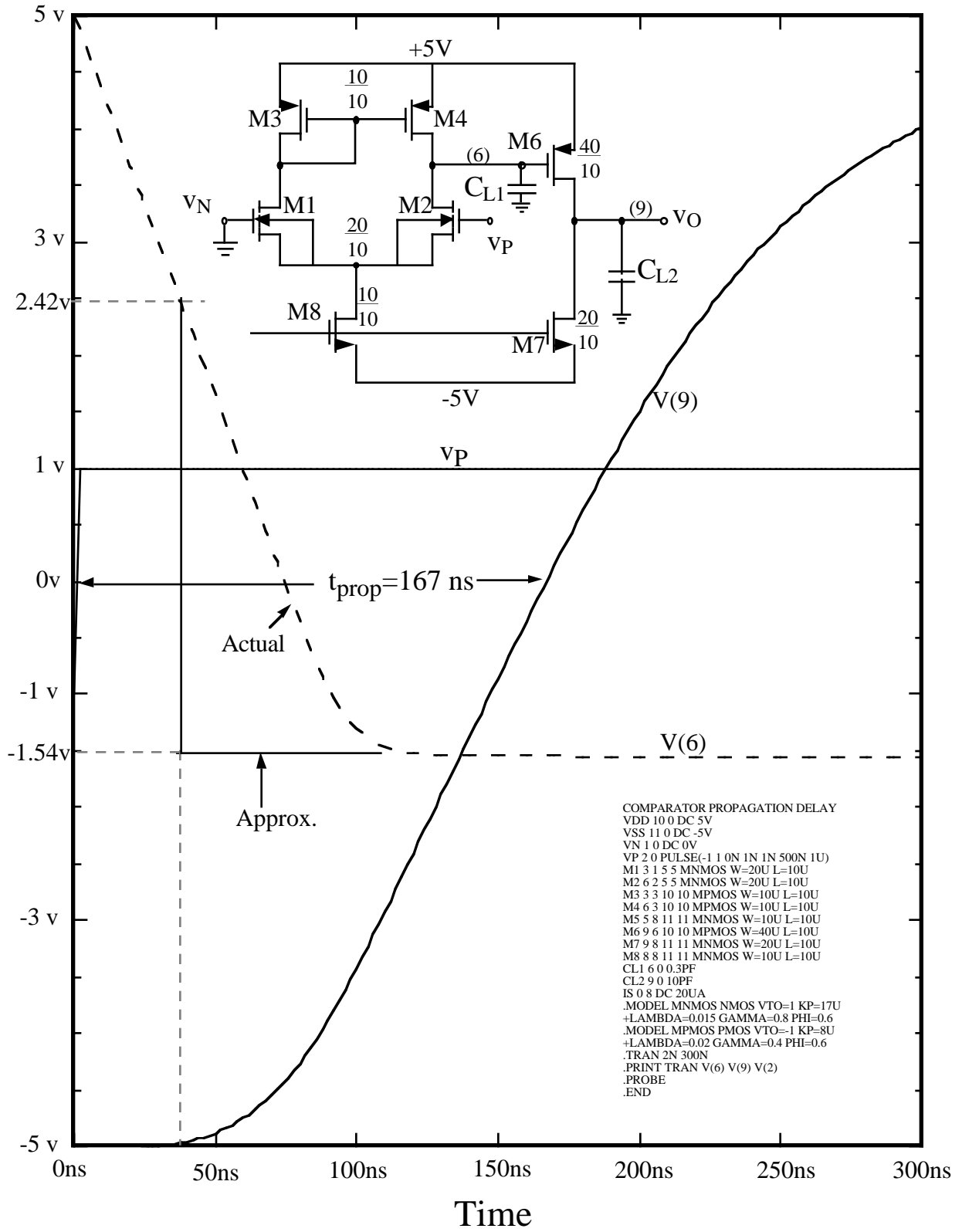
$$I_6 = \frac{8 \cdot 10^{-6}}{2} (4)(5 - (-1.77) - 1)^2 = 533 \mu\text{A}$$

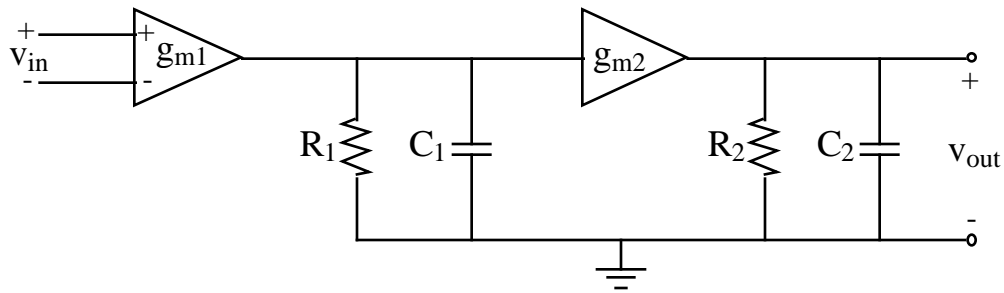
$$\therefore \Delta t_2 = 5 \frac{10 \text{ pF}}{(533 - 40) \mu\text{A}} = 101 \text{ ns}$$

$$\underline{\underline{\Delta t = \Delta t_1 + \Delta t_2 \approx 139 \text{ ns}}}$$

Second order consideration: Charging of C_{sb} of M1 and M2

SIMULATION OF THE PROPAGATION DELAY



SMALL SIGNAL PERFORMANCE

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{A_o \omega_{p1} \omega_{p2}}{(s + \omega_{p1})(s + \omega_{p2})}$$

$$\omega_{p1} = \frac{1}{R_1 C_1}$$

$$\omega_{p2} = \frac{1}{R_2 C_2}$$

$$A_o = g_{m1} g_{m2} R_1 R_2$$

Example - (Fig 7.3-4)

$$I_5 = 20\mu\text{A} \quad R_1 = \frac{1}{g_{ds2} + g_{ds4}} = \frac{1}{10\mu\text{A}} = 3.33\text{M}\Omega$$

$$\omega_{p1} = \frac{1}{(0.3\text{pF})(3.33\text{M}\Omega)} = 1\text{Mrps}$$

$$I_7 = 40\mu\text{A} \quad R_2 = \frac{1}{g_{ds6} + g_{ds7}} = \frac{1}{40\mu\text{A}(.03)} = 833\text{K}\Omega$$

$$\omega_{p2} = \frac{1}{(10\text{pF})(833\text{K}\Omega)} = 120\text{Krps}$$

$$g_{m1} = 26\mu\text{s}, \quad g_{m2} = 50.6\mu\text{s} \quad \underline{\underline{A_o = 1099}}$$

COMPARATOR DESIGN PROCEDURE

1. Set the output current to meet the slew rate requirements.

$$i = C \frac{dV}{dt}$$

2. Determine the minimum sizes for M6 and M7 for the proper output voltage swing.

$$v_{DS}(\text{sat}) = \sqrt{\frac{2I_D}{\beta}}$$

3. Knowing the second stage current and minimum device size for M6, calculate the second stage gain.

$$A_2 = \frac{-g_{m6}}{g_{ds6} + g_{ds7}}$$

4. Calculate the required first stage gain from A_2 and gain specifications.
5. Determine the current in the first stage based upon proper mirroring and minimum values for M6 and M7. Verify that P_{diss} is met.
6. Calculate the device size of M1 from A_1 and I_{DS1} .

$$A_1 = \frac{-g_{m1}}{g_{ds1} + g_{ds3}} \quad \text{and} \quad g_{m1} = \sqrt{\frac{2K'W/L}{I_{DS1}}}$$

7. Design minimum device size for M5 based on negative CMR requirement using the following ($I_{DS1} = 0.5I_{DS5}$):

$$v_{G1}(\text{min}) = V_{SS} + V_{DS5} + \sqrt{\frac{I_{DS5}}{\beta_1}} + V_{T1}(\text{max})$$

$$\text{where } V_{DS5} = \sqrt{\frac{2I_{DS5}}{\beta_5}} = V_{DS5}(\text{sat})$$

8. Increase either M5 or M7 for proper mirroring.
9. Design M4 for proper positive CMR using:

$$v_{G1}(\text{max}) = V_{DD} - \sqrt{\frac{I_{DS5}}{\beta_3}} - |V_{TO3}|(\text{max}) + V_{T1}$$

10. Increase M3 or M6 for proper mirroring.
11. Simulate circuit.

DESIGN OF A TWO-STAGE COMPARATOR

Specifications:

$$A_{vo} > 66 \text{ dB} \quad \text{Lambda} = 0.05\text{V}^{-1} \text{ (L} = 5 \text{ }\mu\text{m)}$$

$$P_{\text{diss}} < 10 \text{ mW} \quad V_{\text{DD}} = 10 \text{ V}$$

$$C_L = 2 \text{ pF} \quad V_{\text{SS}} = 0 \text{ V}$$

$$t_{\text{prop}} < 1 \text{ }\mu\text{s} \quad \text{Recall that } \beta = \frac{K'W}{L}$$

$$\text{CMR} = 4\text{-}6 \text{ V}$$

$$\text{Output swing is } V_{\text{DD}} - 2\text{V} \text{ and } V_{\text{SS}} + 2\text{V}$$

1). For $t_{\text{prop}} \ll 1 \text{ }\mu\text{s}$ choose slew rate at $100 \text{ V}/\mu\text{s}$

$$\therefore I_7 = C_L \frac{dv_{\text{OUT}}}{dt} = (2 \cdot 10^{-12})(100 \cdot 10^{-6}) = 200 \text{ }\mu\text{A}$$

2). Size M6 and M7 to get proper output swing,

M7:

$$2\text{V} > v_{\text{DS7(sat)}} = \sqrt{\frac{2I_7}{\beta_7}} = \sqrt{\frac{2(200\mu\text{A})}{17.0\mu\text{A}/\text{V}^2(W_7/L_7)}} \rightarrow \underline{\underline{\frac{W_7}{L_7} > 5.88}}$$

M6:

$$2\text{V} > v_{\text{DS6(sat)}} = \sqrt{\frac{2(I_{\text{OUT}}+I_7)}{\beta_6}} = \sqrt{\frac{2(400\mu\text{A})}{8.0\mu\text{A}/\text{V}^2(W_6/L_6)}} \rightarrow \underline{\underline{\frac{W_6}{L_6} > 12.5}}$$

$$3). A_2 = \frac{-g_{m6}}{g_{\text{ds6}} + g_{\text{ds7}}} = \left(\frac{-1}{\lambda_{\text{N}} + \lambda_{\text{P}}} \right) \sqrt{\frac{2K_{\text{P}}'W_6}{I_6L_6}} \approx -10$$

$$4). A_{vo} = A_1A_2 = 66 \text{ dB} \approx 2000 \rightarrow A_1 = 200$$

COMPARATOR DESIGN - CONT'D

5). Assuming $v_{GS4} = v_{GS6}$, then $I_4 = \frac{S_4}{S_6} I_6$

choose $S_4 = 1$ which gives $I_4 = \frac{1}{12.5} (200\mu A) = 16.0 \mu A$

Assume $S_5 = 1$ which gives $I_5 = \frac{S_5}{S_7} I_7 = \frac{200\mu A}{5.88} = 34 \mu A$

and $I_4 = \frac{1}{2} I_5 = 17 \mu A$

Choose $I_4 = 17 \mu A$ to keep $\frac{W}{L}$ ratios greater than 1.

$\therefore I_5 = 34 \mu A$ $\frac{W_4}{L_4} = \frac{W_6}{L_6} \left(\frac{17}{200} \right) = 1.06 \approx 1.0$

$P_{diss} = 10(I_7 + I_5) = 2.34 \text{ mW} < 10 \text{ mW}$

6). $A_1 = \frac{1}{\lambda_1 + \lambda_4} \sqrt{\frac{2K_N'W_1}{I_4L_1}} \rightarrow \frac{W_1}{L_1} = [(\lambda_1 + \lambda_4)A_1]^2 \frac{I_4}{2K_N'} = 200$

$\therefore \frac{W_1}{L_1} = 200$ (Good for noise)

7). $V_{DS5} = v_{G1}(\text{min}) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\text{max})$

$V_{DS5} = 4 - 0 - \sqrt{\frac{(34)}{2(17.0)(200)}} - 1 = 2.90 \text{ V}$

$V_{DS5} = \sqrt{\frac{2I_5}{\beta_5}} = \sqrt{\frac{2(34\mu)}{(17\mu)S_5}} \rightarrow \frac{W_5}{L_5} > 0.48$

8). $S_5 = \frac{I_5}{I_7} S_7 = \frac{34}{200} (5.88) = 1.0 \rightarrow \frac{W_5}{L_5} = 1.0$

COMPARATOR DESIGN - CONT'D

$$9). V_{G1(max)} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{TO3}|(max) + V_{T1}(min)$$

$$\beta_3 = \frac{I_5}{[V_{DD} - V_{G1(max)} - |V_{TO3}|(max) + V_{T1}(min)]^2}$$

$$= \frac{34 \mu A}{(10 - 6 - 1 + 0.5)^2} = 2.76 \cdot 10^{-6}$$

$$\therefore \frac{W_3}{L_3} = \frac{(2.76)(2)}{8} = 0.69 \quad \frac{W_3}{L_3} = \frac{W_4}{L_4} > 0.69$$

(Previously showed $\frac{W_4}{L_4} > 1.06$ so no modification is necessary)

10). Summary

$$W_{drawn} = \left(\frac{W}{L}\right)(L - 1.6)$$

Design Ratios	Actual Values with 5μm minimum geometry	Proper Mirroring and $L_D = 0.8\mu m$
$\frac{W_1}{L_1} = \frac{W_2}{L_2} = 200$	$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{1000}{5}$	$\frac{680}{5}$
$\frac{W_3}{L_3} = \frac{W_4}{L_4} = 1.0$	$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{5}{5}$	$\frac{3.4}{5}, \frac{5}{5}$
$\frac{W_5}{L_5} = 1.0$	$\frac{W_5}{L_5} = 1.0$	$\frac{3.4}{5}, \frac{5}{5}$
$\frac{W_6}{L_6} = 12.5$	$\frac{W_6}{L_6} = \frac{62.5}{5}$	$\frac{60}{5}$
$\frac{W_7}{L_7} = 5.88$	$\frac{W_7}{L_7} = \frac{30}{5}$	$\frac{30}{5}$

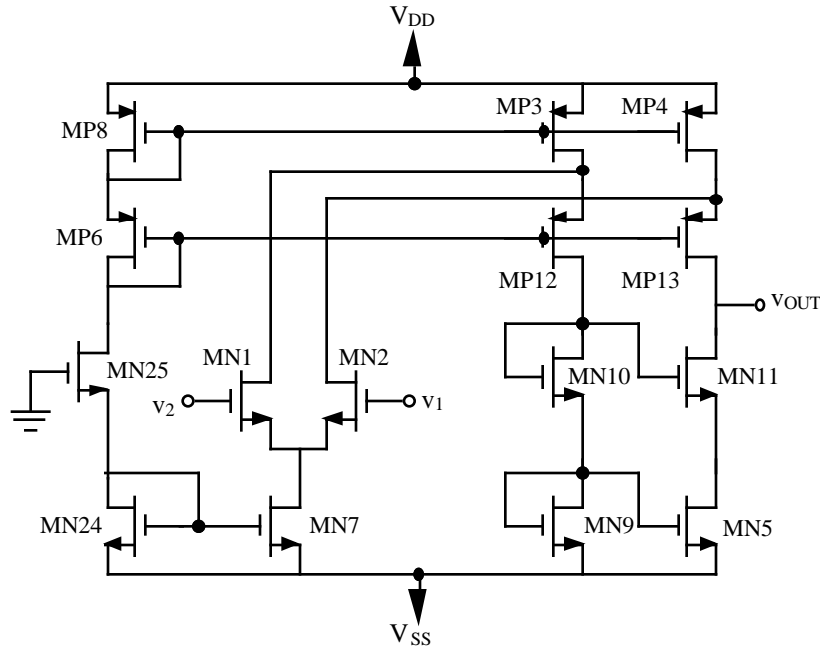
(Need to adjust for proper mirroring) \Rightarrow

$$\frac{S_6}{S_4} = 2 \frac{S_7}{S_5}$$

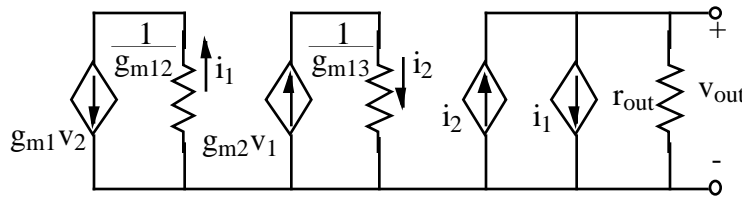
VII.4 - OTHER TYPES OF COMPARATORS

FOLDED CASCODE CMOS COMPARATOR

Circuit Diagram



Small Signal Model



where

$$R_{out} \approx (r_{ds5}g_{m11}r_{ds11}) \parallel ((r_{ds4} \parallel r_{ds2})g_{m13}r_{ds13}) =$$

$$= \frac{1}{\frac{g_{ds5}g_{ds11}}{g_{m11}} + \frac{(g_{ds2} + g_{ds4})g_{ds13}}{g_{m13}}}$$

The small signal voltage gain is

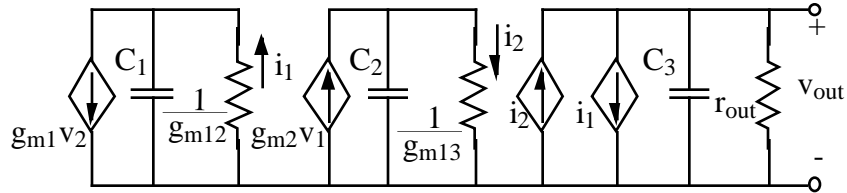
$$v_{out} = r_{out}(i_2 - i_1) = (g_{m2} + g_{m1})R_{out}v_{in} = \left(\frac{g_{m1} + g_{m2}}{\frac{g_{ds5}g_{ds11}}{g_{m11}} + \frac{(g_{ds2} + g_{ds4})g_{ds13}}{g_{m13}}} \right) v_{in}$$

where $v_{in} = v_1 - v_2$.

FOLDED CASCODE CMOS COMPARATOR - CONTINUED

Frequency Response

Small signal model-



where

$$C_1 = C_{GS12} + C_{BS12} + C_{DG3} + C_{BD3}$$

$$C_2 = C_{GS13} + C_{BS13} + C_{DG4} + C_{BD4}$$

and $C_3 = C_{DG11} + C_{BD11} + C_{DG13} + C_{BD13} + C_{Load}$

$$A_{VD}(s) \approx \frac{A_{VD0}\omega_3}{s + \omega_3}$$

where

$$\omega_3 = \frac{1}{r_{out}C_3}$$

Typical performance-

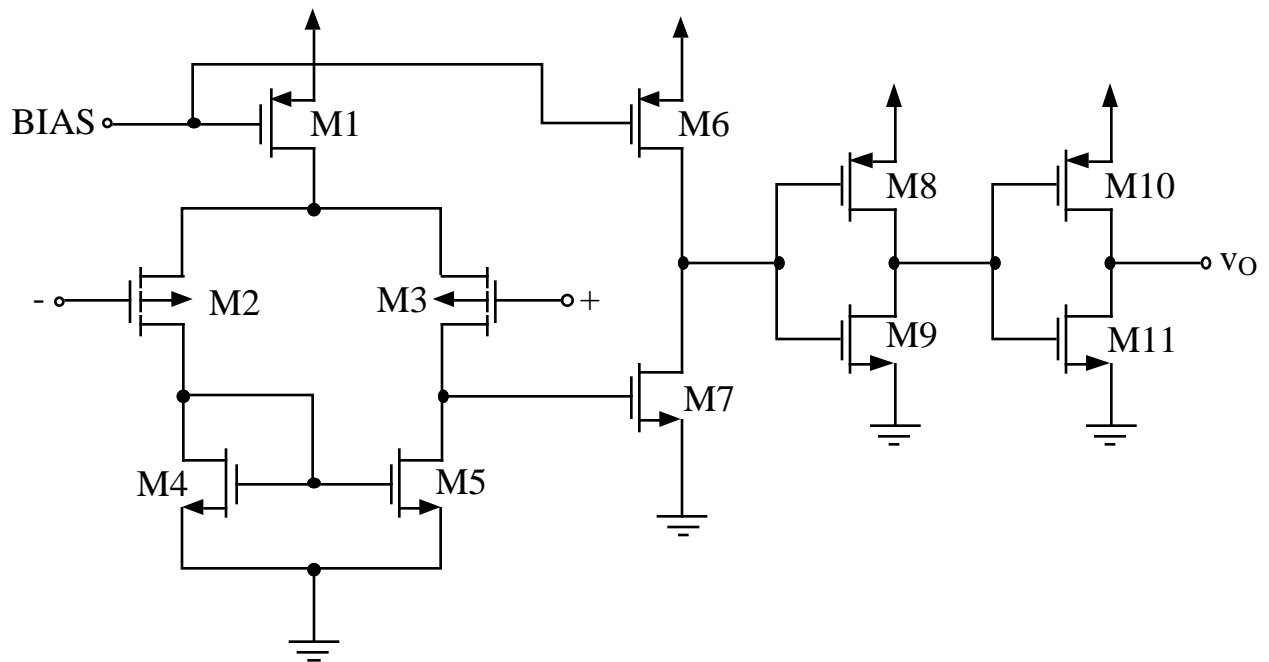
$$I_{D1} = I_{D2} = 50\mu\text{A} \text{ and } I_{D3} = I_{D4} = 100\mu\text{A}, \quad \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_{11}}{L_{11}} = \frac{W_{13}}{L_{13}} = 1, \text{ assume } C_3 \approx 0.5\text{pF}, \text{ and using the values of Table 3.1-2 gives:}$$

$$g_{m1} = g_{m2} = g_{m11} = 41.2\mu\text{S} \quad g_{m13} = 28.3\mu\text{S}$$

$$g_{ds5} = g_{ds11} = 0.5\mu\text{S} \quad g_{ds4} = g_{ds13} = 0.25\mu\text{S}$$

Therefore, $r_{out} = 121\text{M}\Omega$, $\omega_3 = 16.553\text{krps}$, and $A_{VD0} = 4,978$ resulting in a gain-bandwidth of 13.11MHz.

$$\text{Delay} = \Delta T = \frac{C_3\Delta V}{I_{max}} = \frac{0.5\text{pF} \times 10\text{V}}{100\mu\text{A}} = 50\text{nS}$$

OPEN LOOP COMPARATOR - MC 14575

Performance ($I_{SET} = 50 \mu\text{A}$)

$$\frac{\text{Rise time}}{\text{Fall time}} = 100 \text{ ns into } 50 \text{ pF}$$

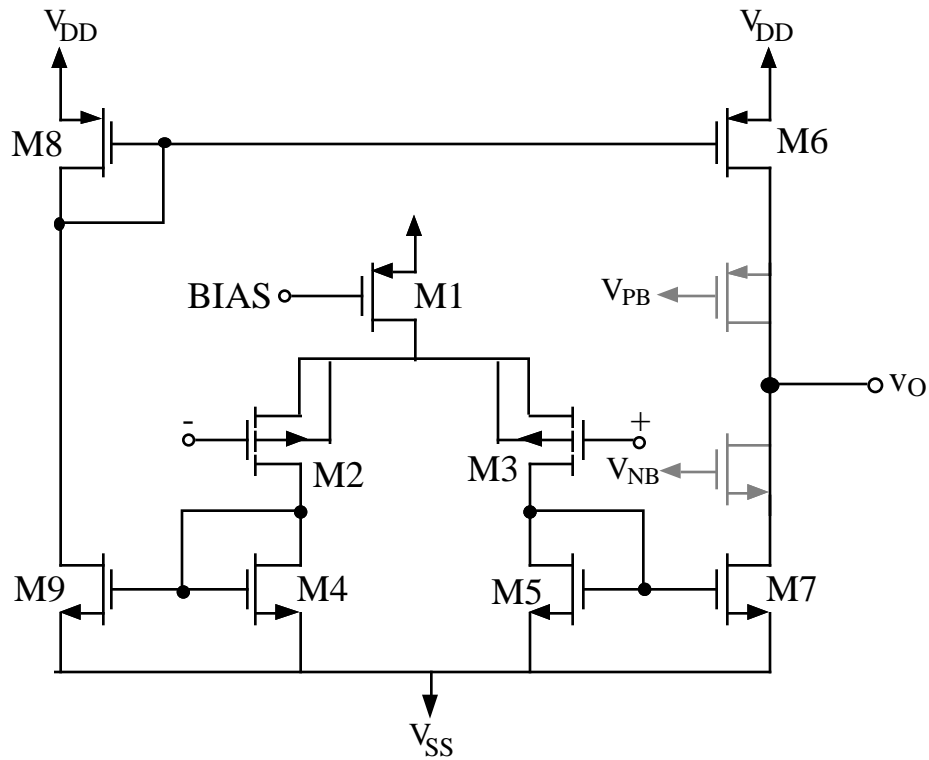
$$\text{Propagation delay} = 1 \mu\text{s}$$

$$\text{Slew rate} = 2.7 \text{ Volts}/\mu\text{s}$$

$$\text{Loop Gain} = 32,000$$

Comments

The inverter pair of M8-M9 and M10-M11 are for the purpose of providing an output drive capability and minimizing the propagation delay.

CLAMPED CMOS VOLTAGE COMPARATOR

Drain of M2 and M3 clamped to the gate voltages of M4 and M5.

M6 and M7 provide a current, push-pull output drive capability similar to the current, push-pull CMOS OP amp.

Comparator is really a voltage comparator with a current output.

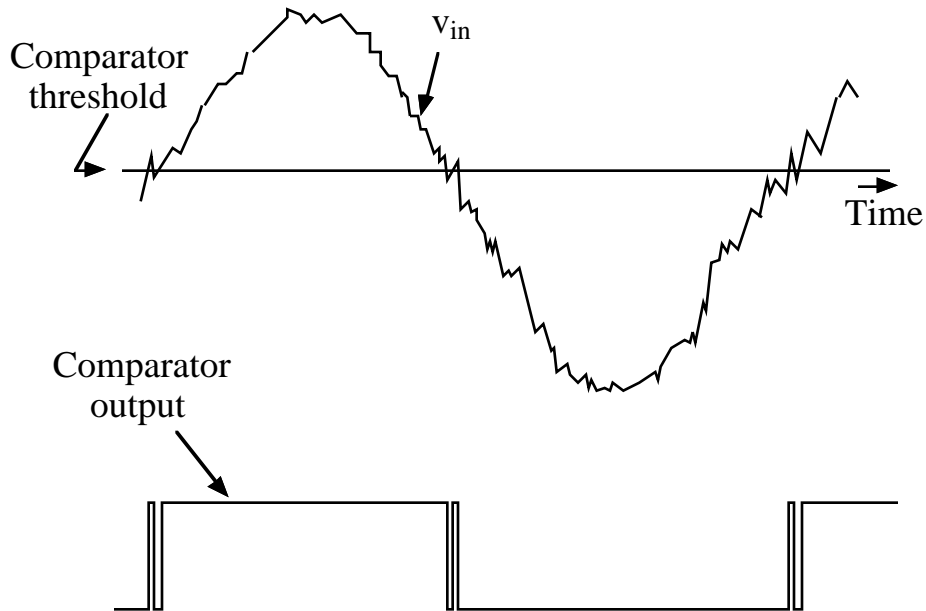
VII.5 - COMPARATORS WITH HYSTERESIS

HYSTERESIS

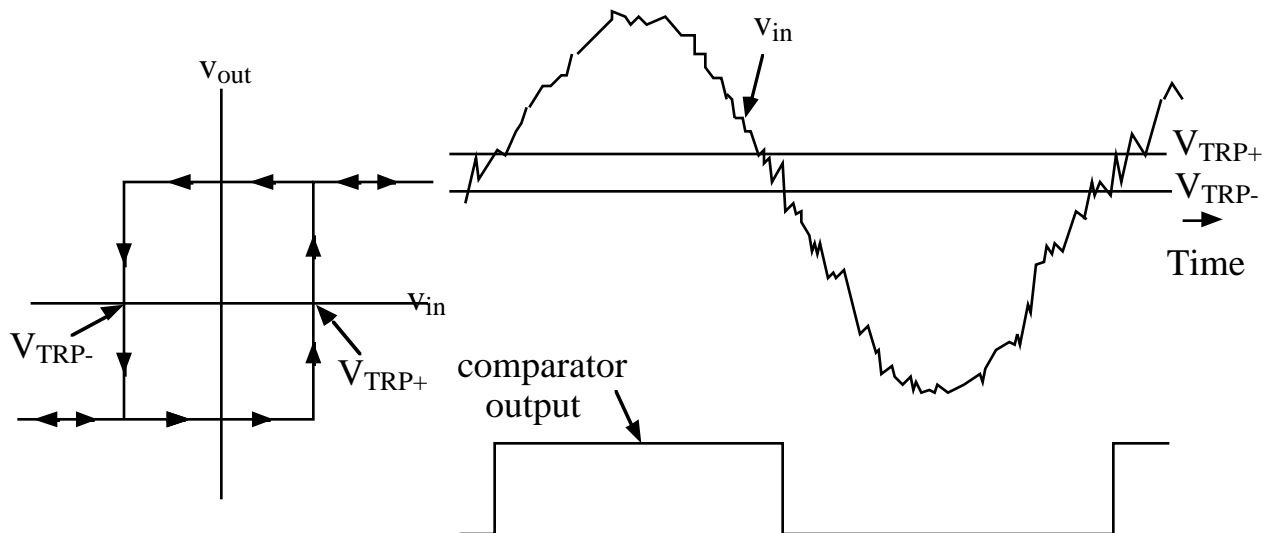
Why Hysteresis?

Eliminates "chattering" when the input is noisy.

Comparator with no Hysteresis

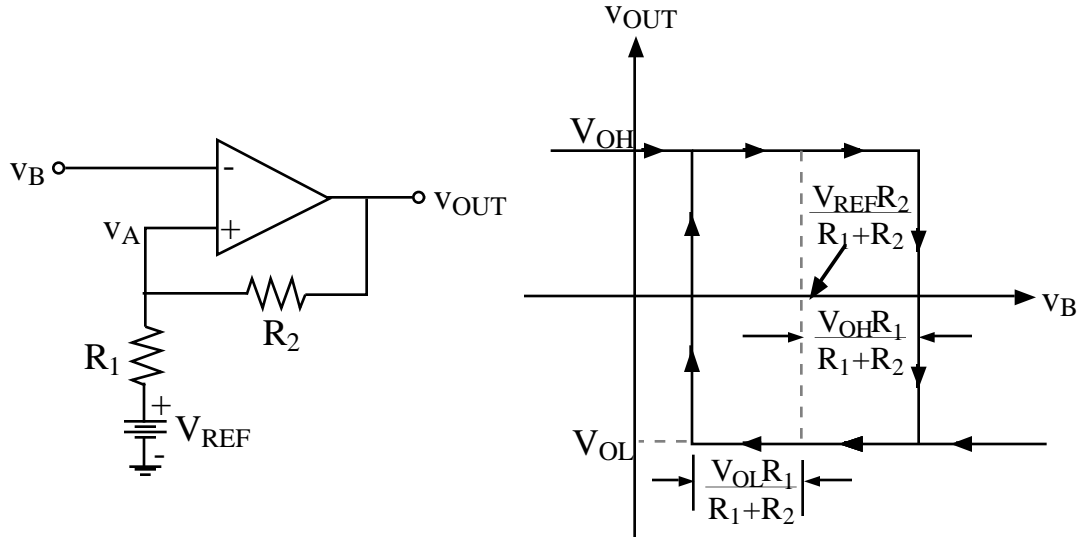


Comparator with Hysteresis

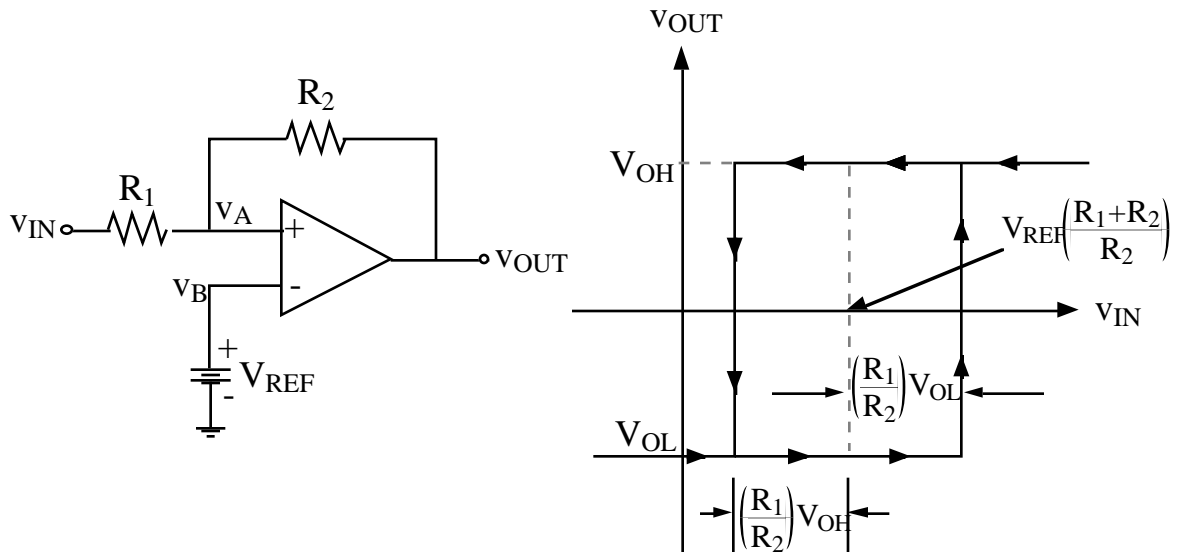


VOLTAGE COMPARATORS USING EXTERNAL FEEDBACK

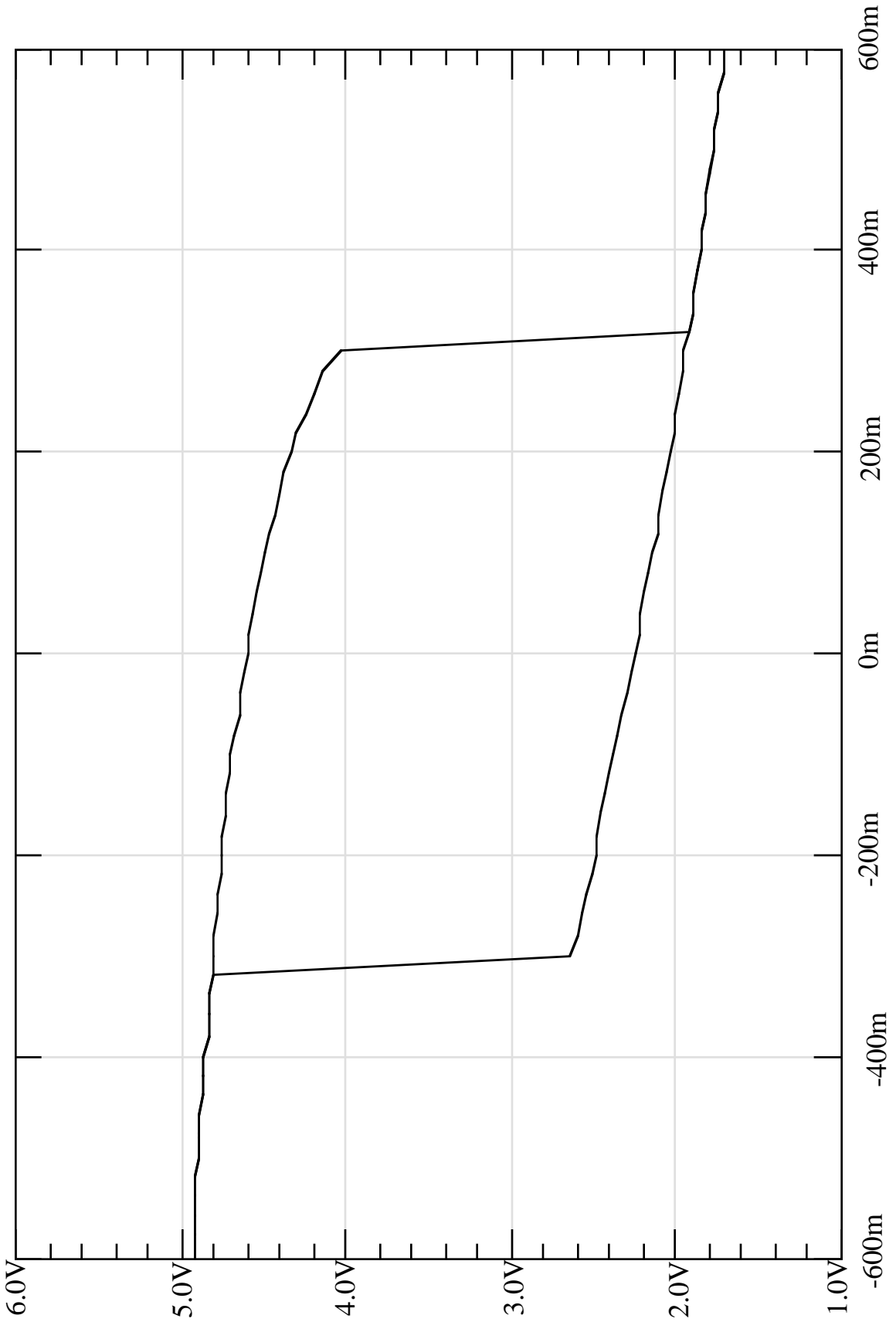
Inverting



Noninverting

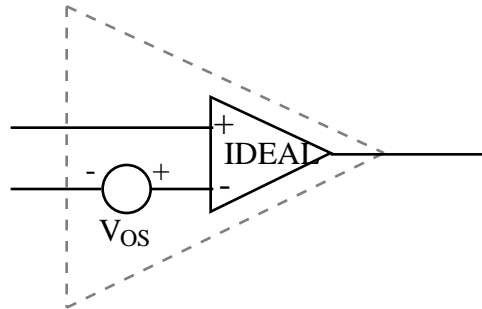


EXAMPLE 7.4-1 COMPARATOR WITH HYSTERESIS

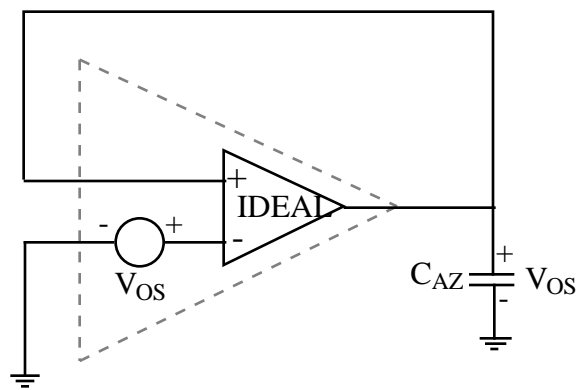


AUTO ZEROING OF VOLTAGE COMPARATORS

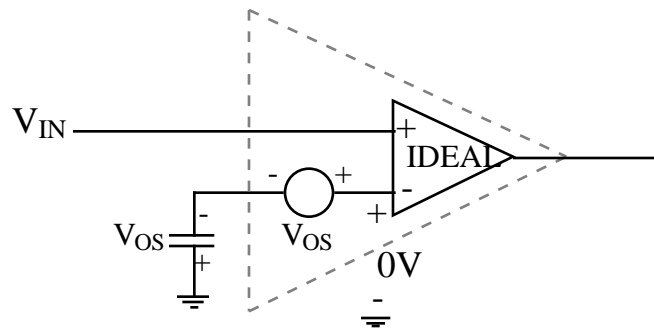
Model of the Comparator Including Offset

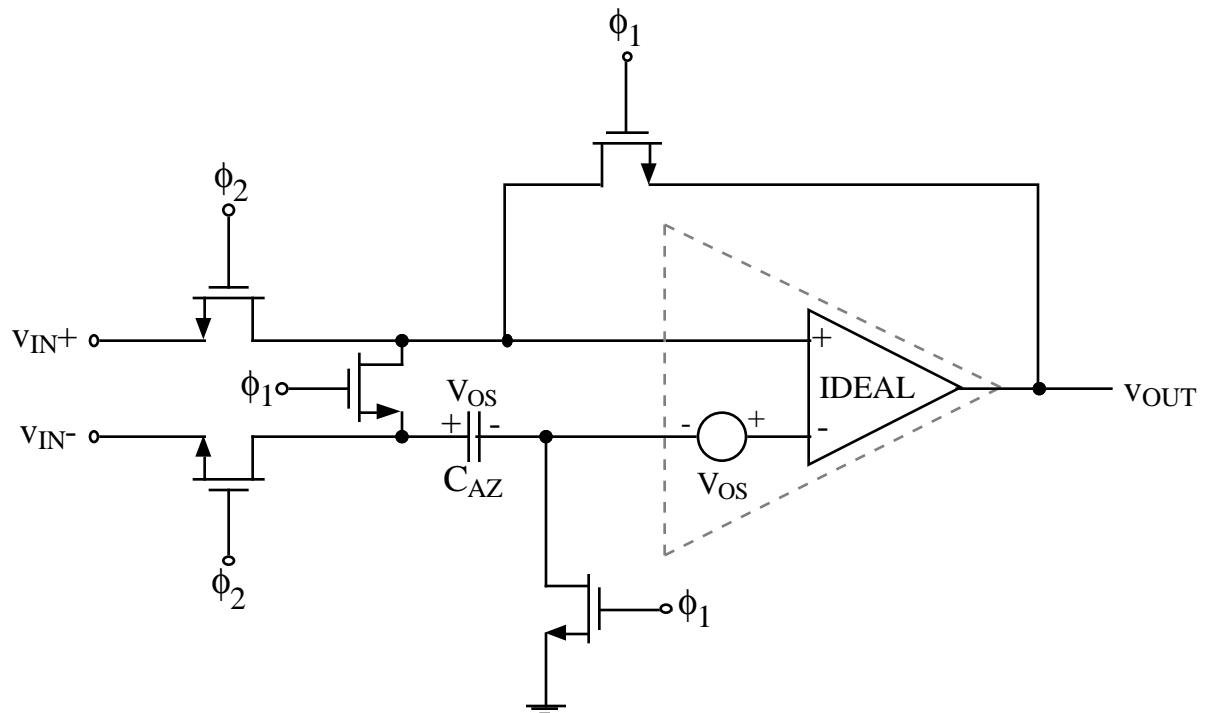


Auto Zero Scheme-First Half of Cycle

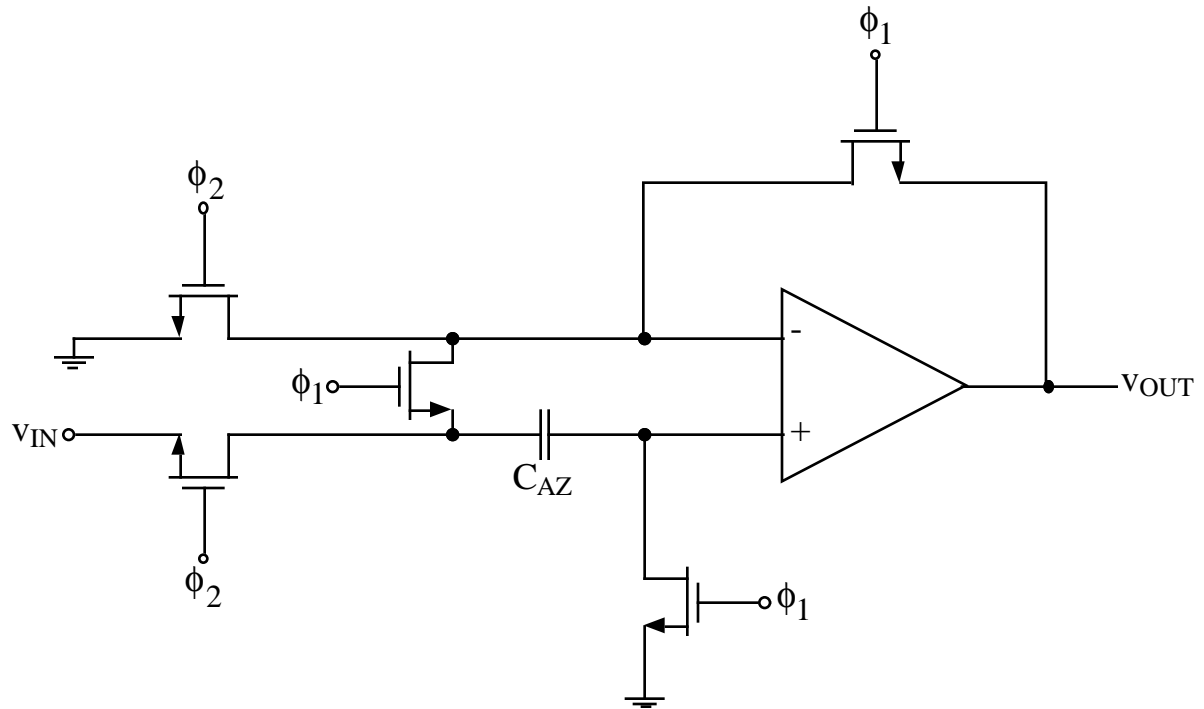
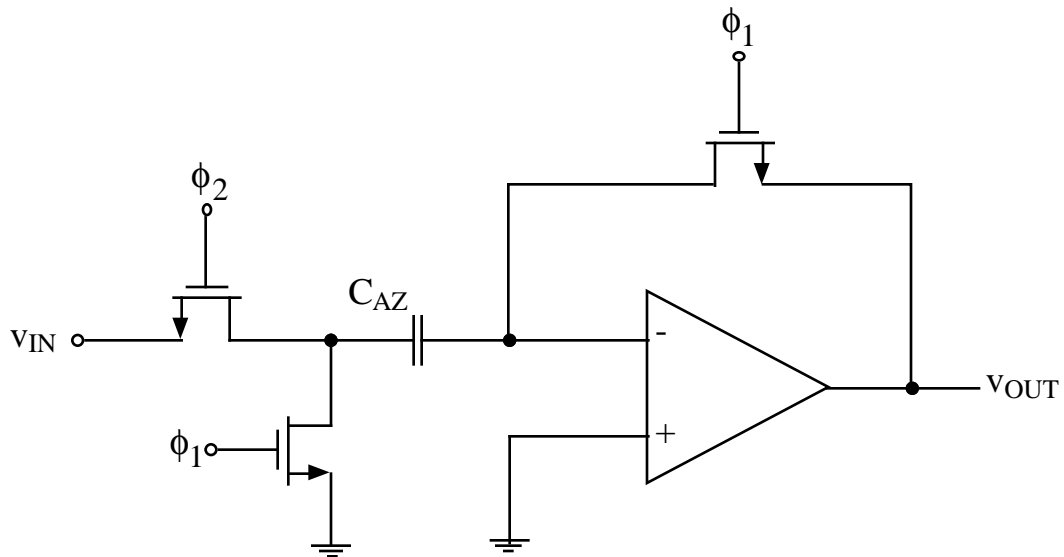


Auto Zero Scheme-Second Half of Cycle



GENERALIZED AUTO ZERO CONFIGURATION

Good for inverting or noninverting when the other terminal is not on ground.

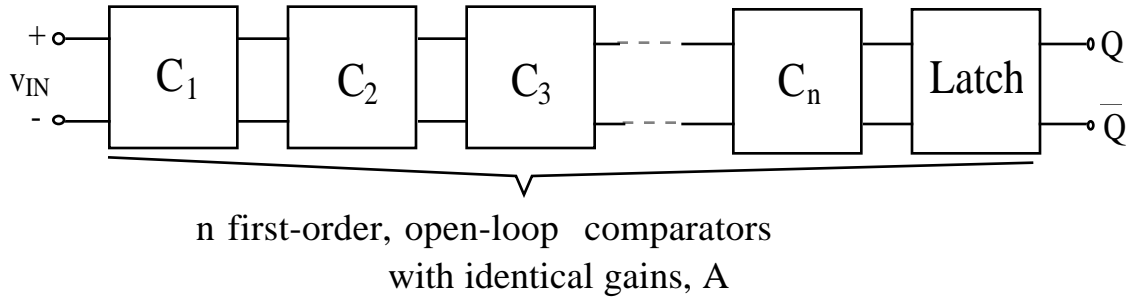
Noninverting Auto-Zeroed ComparatorInverting Auto-Zeroed Comparator

Use nonoverlapping, two-phase clock.

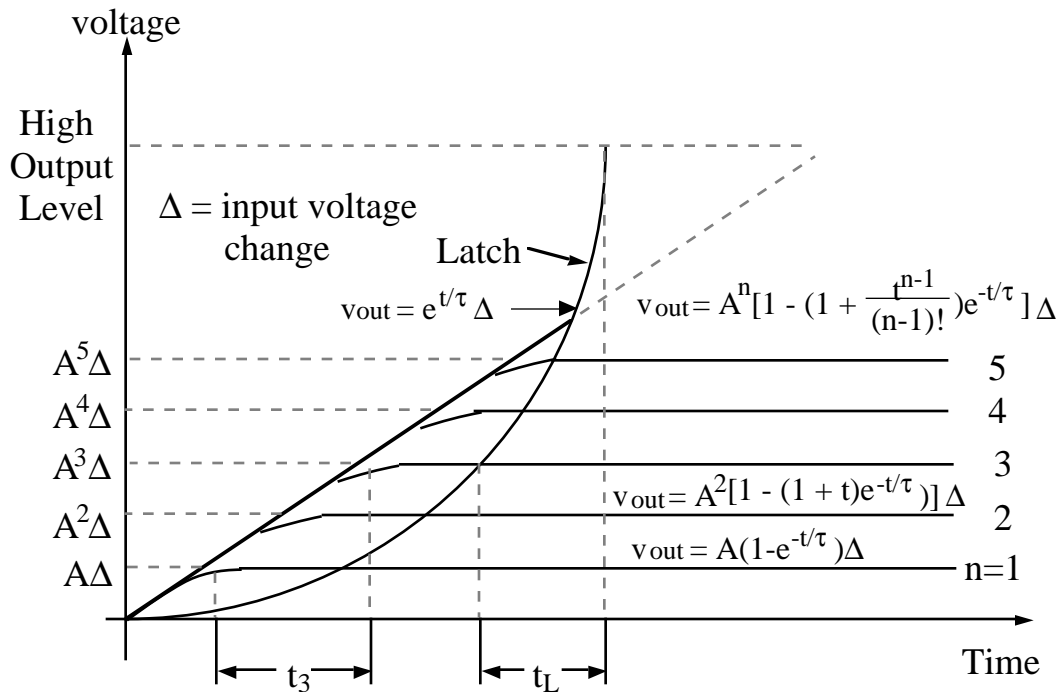
VII.6 - HIGH SPEED COMPARATORS

Concept

Question: For a given input change, what combination of first-order open-loop comparators and a latch gives minimum propagation delay?



Concept:



Answer:

$t_p(\text{min})$ occurs when $n=6$ and $A=2.72=e$

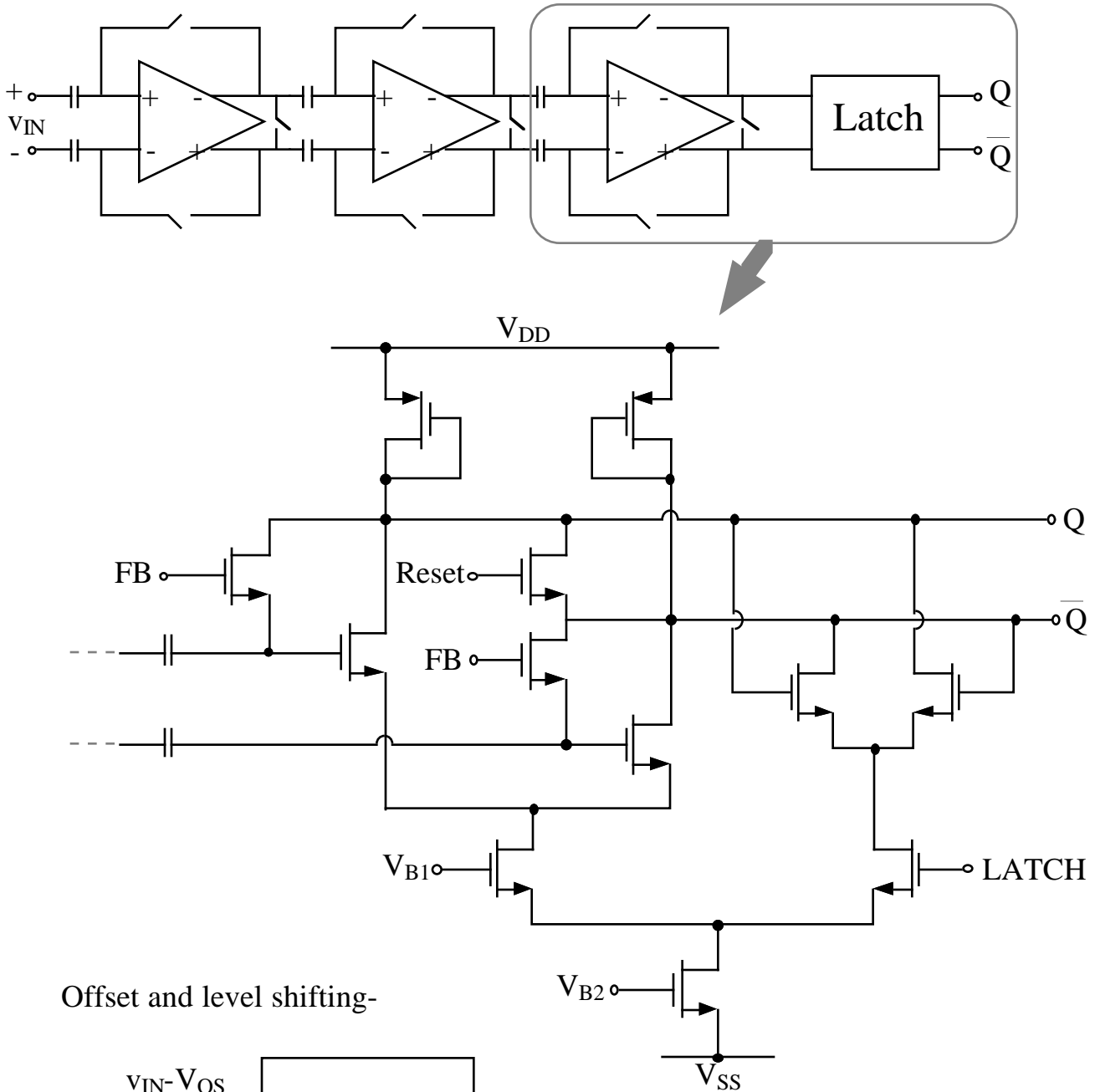
Implementation:

$n=3$ and $A \approx 6$ gave nearly the same result with less area.

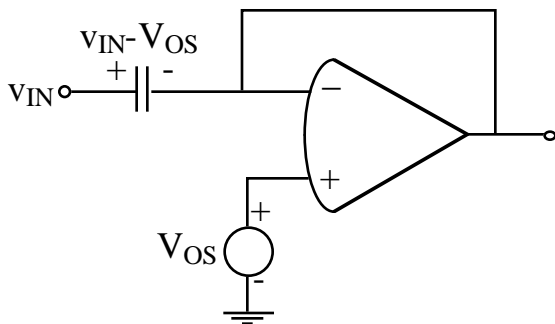
[Ref: Doernberg et al., "A 10-bit 5 MSPS CMOS Two-Step FLASH ADC" JSSC April 1989 pp 241-249]

HIGH SPEED COMPARATORS-CONT'D

Conceptual Implementation-



Offset and level shifting-



VII.7 - COMPARATOR SUMMARY

- Key performance parameters:
 - Propagation time delay
 - Resolving capability
 - Input common mode swing
 - Input offset voltage
- Types of comparators:
 - Open loop
 - Regenerative
 - Open loop and regenerative
 - Charge balancing
- Open loop comparator needs differential input and second stage
- Systematic offset error is offset (using perfectly matched transistors) that is due to current mirror errors.
- For fast comparators, keep all node swings at a minimum except for the output (current comparators?).
- Key design equations:

$$i_D = \frac{KW}{2L} (v_{GS} - V_T)^2, \quad v_{DS}(\text{sat}) = \sqrt{\frac{2i_D}{K(W/L)}}, \quad \text{and} \quad g_m = \sqrt{\frac{2KW i_D}{L}}$$
- Positive feedback is used for regenerative comparators.
- Use autozeroing to remove offset voltages (charge injection is limit).
- Fastest comparators using low-gain, fast open loop amplifiers cascaded with a latch.