VI. CMOS AMPLIFIERS

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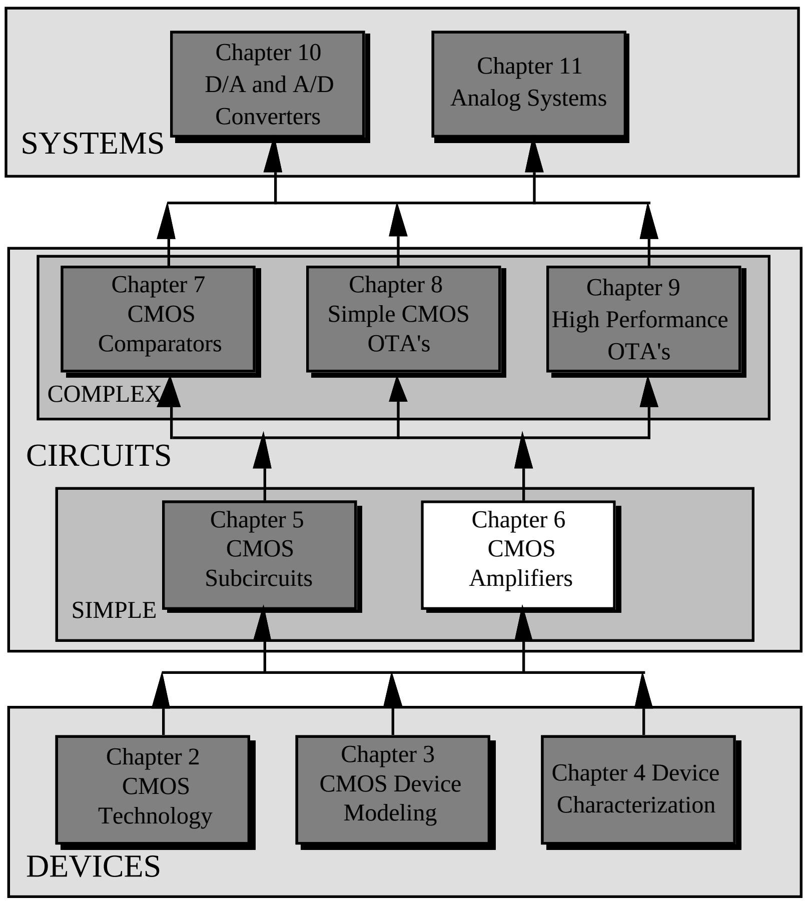
Organization



VI.1 SIMPLE INVERTING AMPLIFIERS

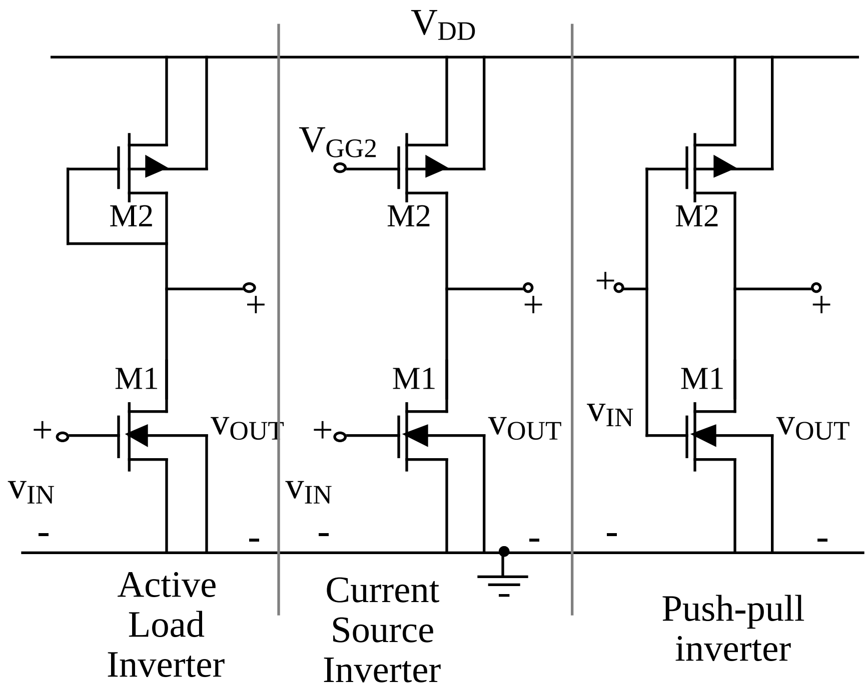
CHARACTERIZATION OF AMPLIFIERS

We shall characterize the amplifiers of this Chapter by the following aspects:

- Large Signal Voltage Transfer Characteristics
- Maximum Signal Swing Limits
- Small Signal Midband Performance
  - Gain
  - Input resistance
  - Output resistance
- Small Signal Frequency Response
- Other Considerations
  - Noise
  - Power
  - Etc.

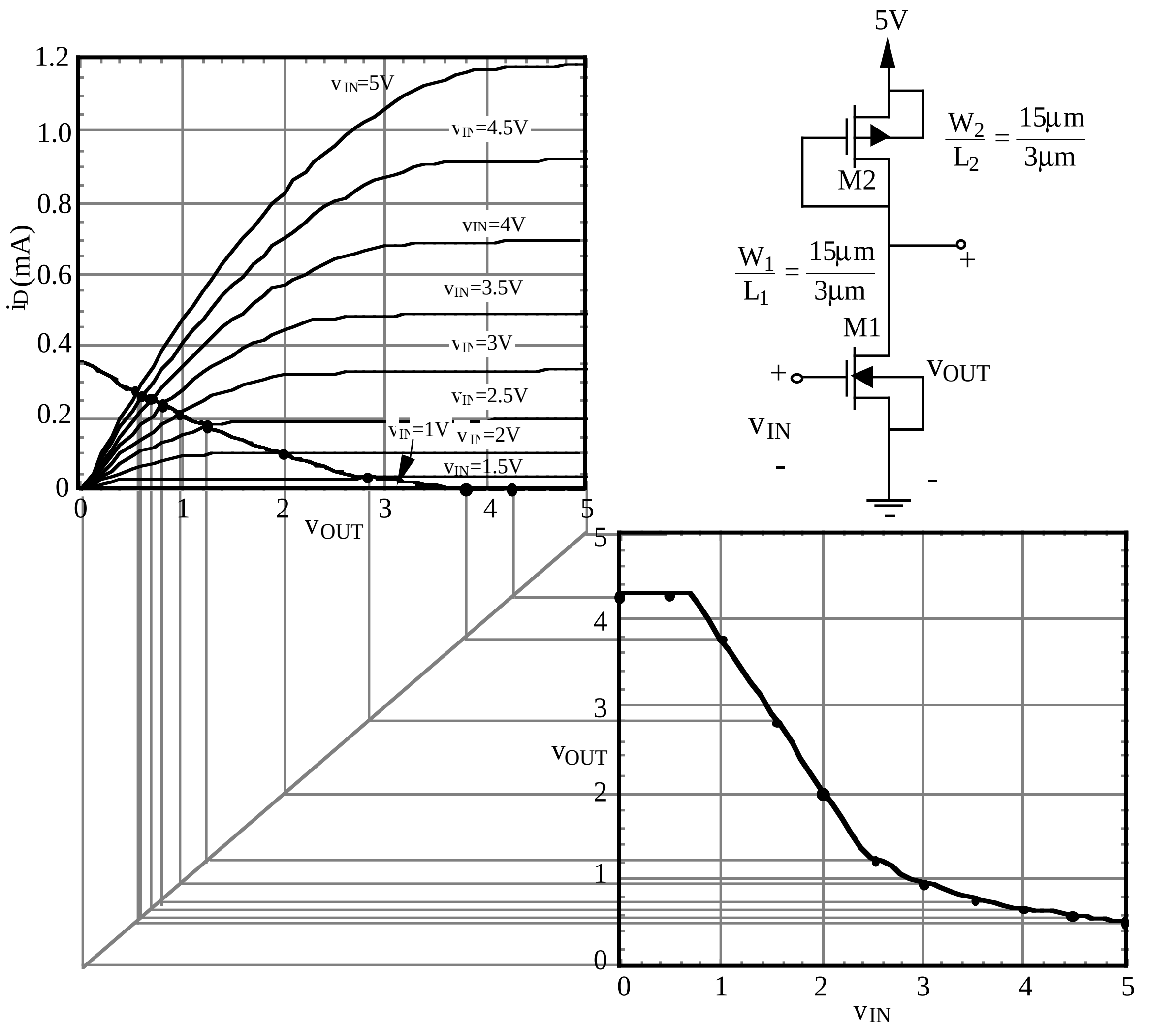
VI.1.1 - CMOS INVERTERS

Types



ACTIVE LOAD INVERTER - VOLTAGE TRANSFER CURVE

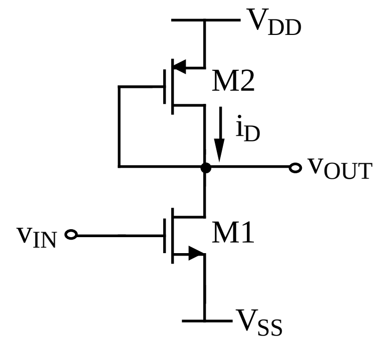
CMOS Active Load Inverter
VDD 3 0 DC 5.0



SPICE Input File:

```
VIN 1 0 DC 0.0
M1 2 1 0 0 MNMOS1 W=15U L=3U
M2 2 2 3 3 MPMOS1 W=15U L=3U
.MODEL MNMOS1 NMOS VTO=0.75 KP=25U LAMBDA=0.01 GAMMA=0.8 PHI=0.6
.MODEL MPMOS1 PMOS VTO=-0.75 KP=8U LAMBDA=0.02 GAMMA=0.4 PHI=0.6
.DC VIN 0 5 0.1
.OP
.PRINT DC V(2)
.PROBE
.END
```

Active Load CMOS Inverter Output Swing Limits



Maximum:

$v_{IN}=0 \Rightarrow i_D=0 \Rightarrow v_{SD2}=|V_{T2}|$

$$\therefore \boxed{v_{OUT}(max) \approx V_{DD} - |V_{TP}|}$$

Minimum:

Assume $v_{IN} = V_{DD}$, M1 active, M2 saturated, and $V_{T1} = V_{T2} = V_T$.

M1: $$i_D = \beta 1\left[(v_{GS1}-V_T)v_{DS1}-\frac{v_{DS1}{}^2}{2}\right]$$

$$= \beta 1\left[(V_{DD}-V_{SS}-V_T)(v_{OUT}-V_{SS})-\frac{(v_{OUT}-V_{SS})^2}{2}\right]$$

M2: $$i_D = \frac{\beta_2}{2}(v_{GS}-V_T)^2 = \frac{\beta_2}{2}(V_{DD}-v_{OUT}-V_T)^2 = \frac{\beta_2}{2}(v_{OUT}+V_T-V_{DD})^2$$

$$i_D = \frac{\beta_2}{2}(v_{OUT}-V_{SS}+V_{SS}+V_T-V_{DD})^2$$

$$=\frac{\beta_2}{2}\left[(v_{OUT}-V_{SS})-(V_{DD}-V_{SS}-V_T)\right]^2$$

Define $v_{OUT}' = v_{OUT} - V_{SS}$ and $V_X = V_{DD} - V_{SS} - V_T$

$$\therefore \quad i_D = \beta_1\left(V_X v_{OUT}' - \frac{(v_{OUT}')^2}{2}\right) \qquad \text{(M1)}$$

$$i_D = \frac{\beta_2}{2}\left(v_{OUT}' - V_X\right)^2 \qquad \text{(M2)}$$

Equate currents -

$$\frac{\beta_2}{2}\left(v_{OUT}'^2 - 2V_X v_{OUT}' + V_X{}^2\right) = \beta_1\left[V_X v_{OUT}' - \frac{v_{OUT}'^2}{2}\right]$$

or $$\frac{\beta_2}{\beta_1}\left(v_{OUT}'^2 - 2V_X v_{OUT}' + V_X{}^2\right) = 2V_X v_{OUT}' - v_{OUT}'^2$$

$$\left(1 + \frac{\beta_2}{\beta_1}\right) v_{OUT}'^2 - 2V_X\left(1 + \frac{\beta_2}{\beta_1}\right) v_{OUT}' + \frac{\beta_2}{\beta_1} V_X{}^2 = 0$$

$$v_{OUT}'^2 - 2V_X v_{OUT}' + \left(\frac{\beta_2/\beta_1}{1+\beta_2/\beta_1}\right) V_X{}^2 = 0$$

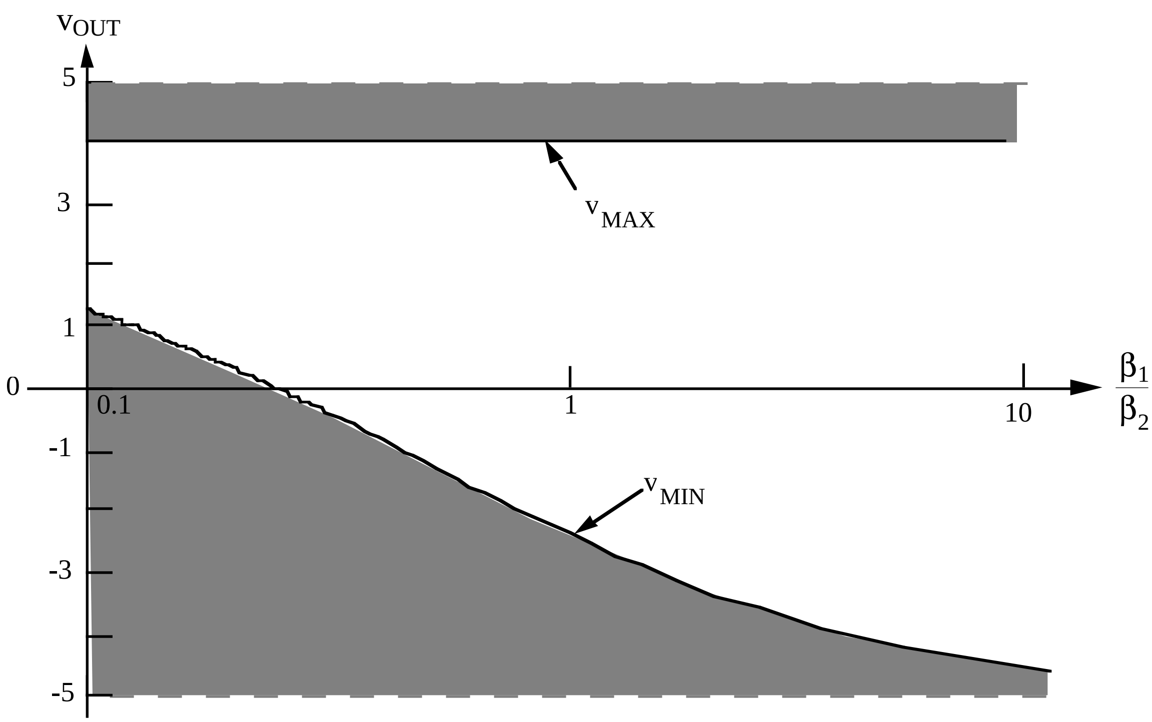
$$\therefore \qquad v_{OUT}' = V_X\left[1 \pm \sqrt{1 - \frac{\beta_2/\beta_1}{1+\beta_2/\beta_1}}\;\right] = V_X\left(1 - \frac{1}{\sqrt{1 + \beta_2/\beta_1}}\right)$$

$$\boxed{v_{OUT}(\text{min.}) = V_{DD} - V_T - \frac{V_{DD} - V_{SS} - V_T}{\sqrt{1 + \beta_2/\beta_1}}}$$

Interpretation of $v_{OUT(min.)}$

$$v_{OUT(min.)} = (V_{DD} - V_{SS} - V_T)\left[1 - \frac{1}{\sqrt{1 + \frac{\beta_2}{\beta_1}}}\right] + V_{SS}$$

$V_{DD} = -V_{SS} = 5V$
$V_T = 1V$

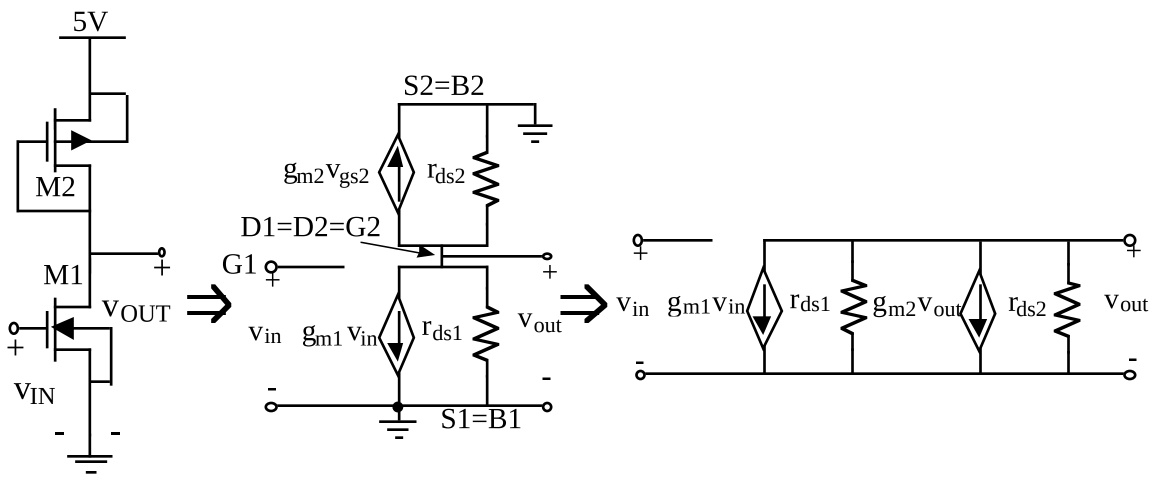


$$\text{Gain} \sim \sqrt{\frac{\beta_1}{\beta_2}}$$

Active Load Inverters

Small Signal Characteristics

Model:



Small Signal Voltage Gain

$$v_{out} = -(g_{m1}v_{in} + g_{m2}v_{out})(r_{ds1} \,||\, r_{ds2})$$

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2} + g_{m2}} \approx \frac{-g_{m1}}{g_{m2}} = -\sqrt{\frac{2K_N\left(\frac{W_1}{L_1}\right)I_1}{2K_P\left(\frac{W_2}{L_2}\right)I_2}} = -\sqrt{\frac{\beta_1}{\beta_2}}$$

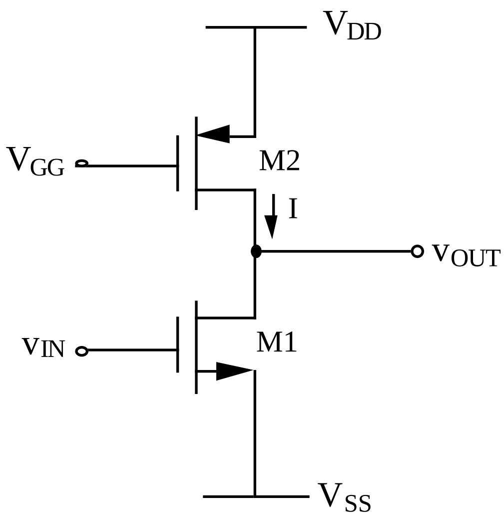
$$\frac{v_{out}}{v_{in}} = -\sqrt{\left(\frac{K_N'}{K_P'}\right)\left(\frac{W_1L_2}{W_2L_1}\right)} = -\sqrt{\left(\frac{\mu_{NO}}{\mu_{PO}}\right)\left(\frac{W_1L_2}{W_2L_1}\right)}$$

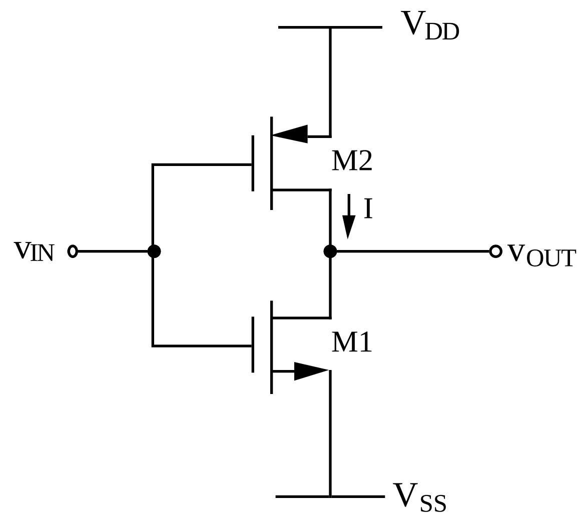
If $\frac{W_1/L_1}{W_2/L_2} = 20$, then $\frac{v_{out}}{v_{in}} = -6.67$ using the parameters of Table 3.1-2

Small Signal Output Resistance

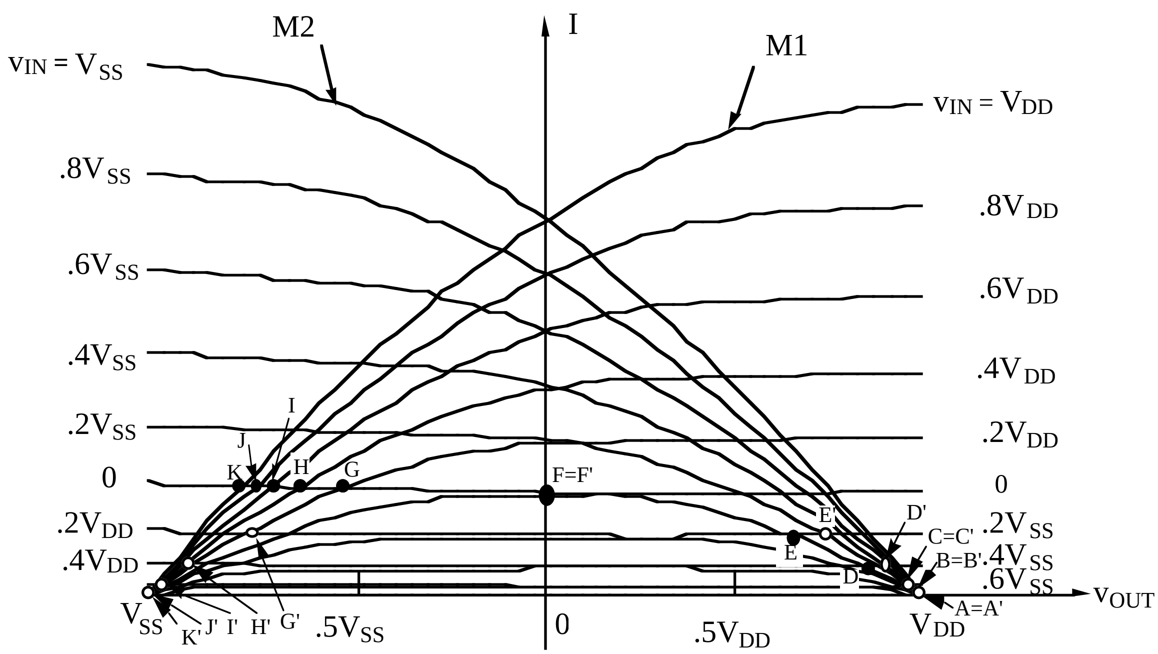
$$r_{out} = \frac{1}{g_{ds1} + g_{ds2} + g_{m2}} \approx \frac{1}{g_{m2}}$$

High Gain CMOS Inverters





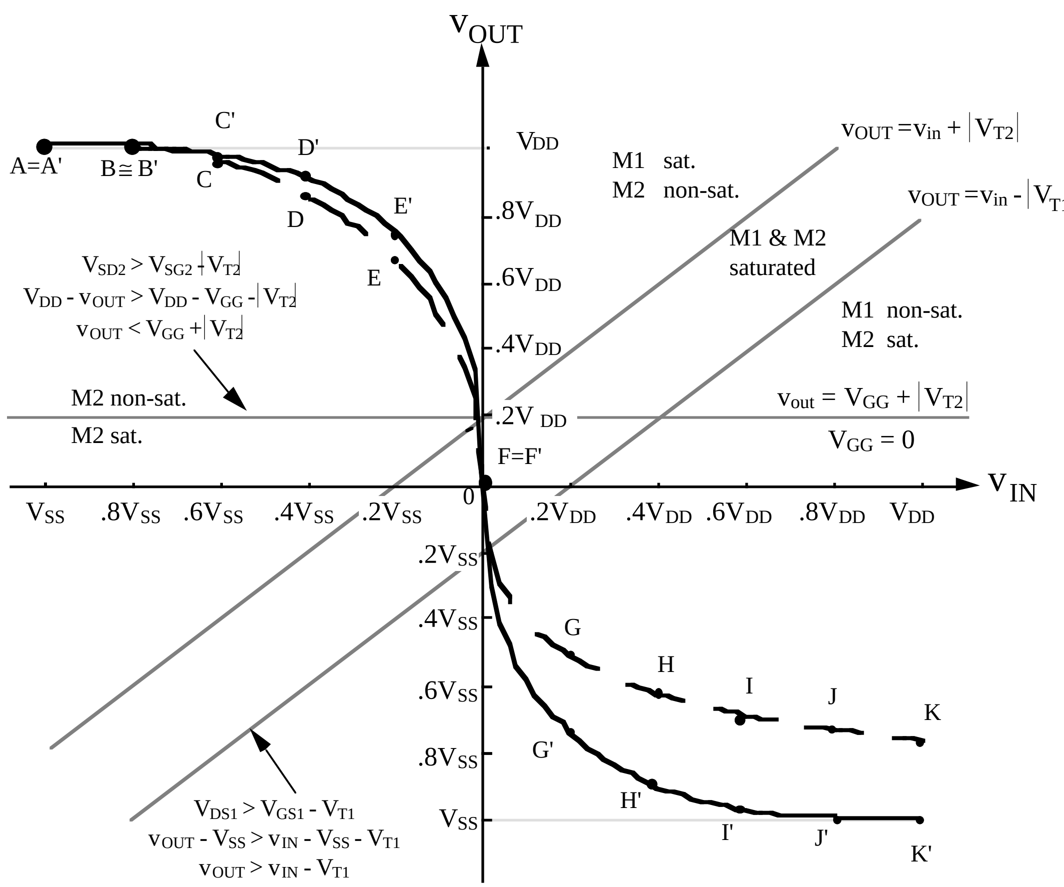
Inverter with current source load Push-pull, inverter



Large signal transfer characteristics of inverter with a current source and push pull inverter

High Gain, CMOS Inverter

Large Signal Transfer Characteristics

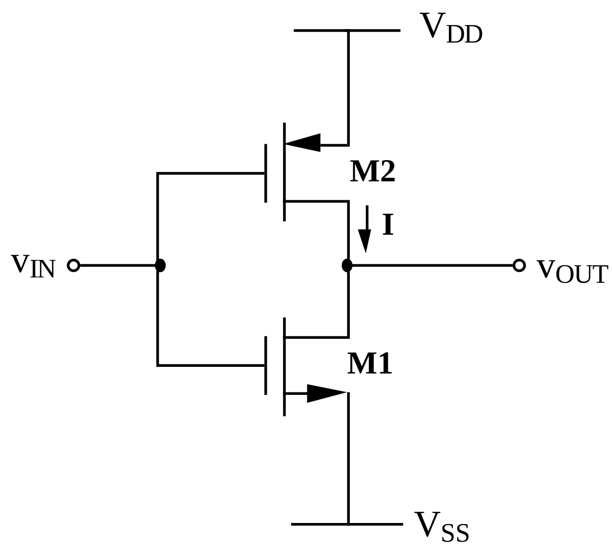


Advantages:

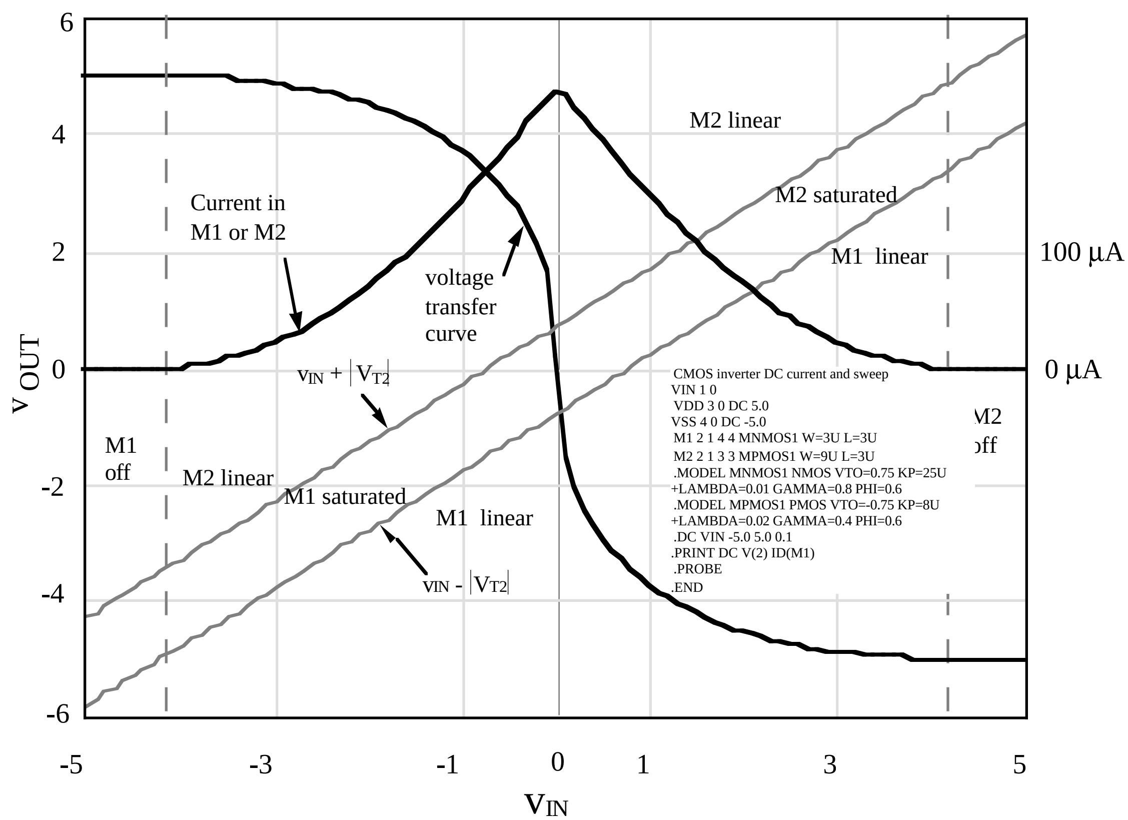
1. High gain.
2. Large output signal swing.
3. Large current sink and source capability in push pull inverter.

CMOS Inverter Characteristics

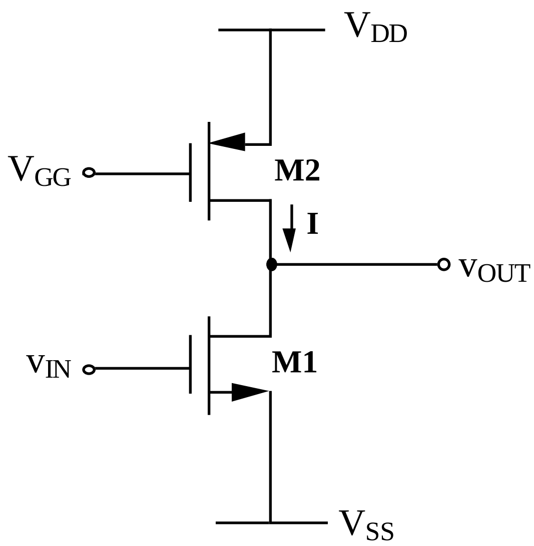
Circuit:



PSPICE Characteristics:



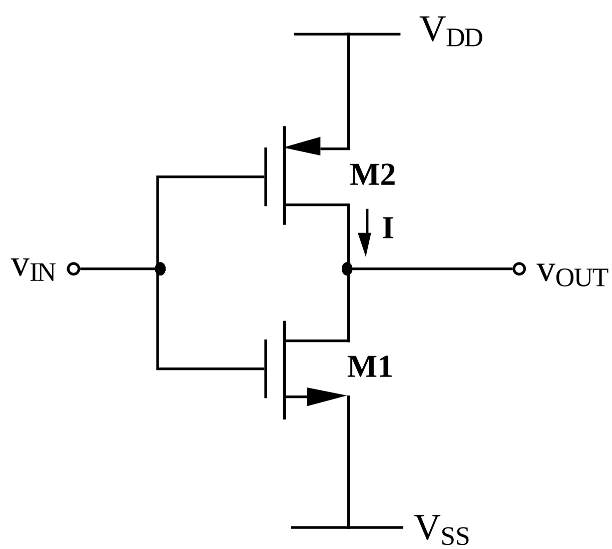
Current Source Inverter - Output Swing Limits



$$v_{OUT(max.)} \approx V_{DD}$$

$$v_{OUT(min.)} = V_{DD}-V_{T1}-(V_{DD}-V_{SS}-V_{T1})\sqrt{1-\left(\frac{\beta_2}{\beta_1}\right)\left(\frac{V_{DD}-V_{GG}-V_{T2}}{V_{DD}-V_{SS}-V_{T1}}\right)}$$

CMOS Push - Pull Inverter - Output Swing Limits



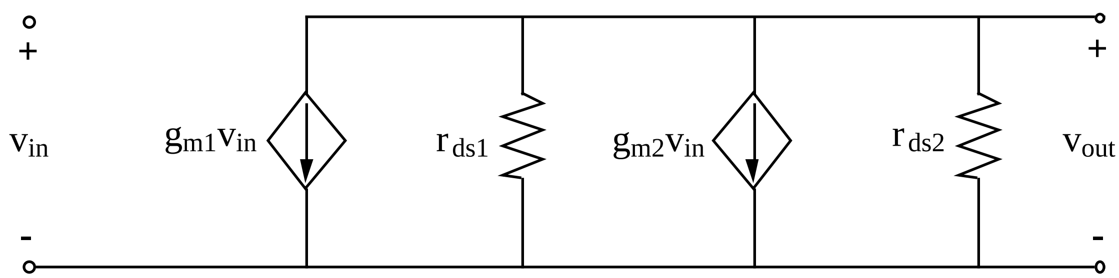
$$v_{OUT(max.)} \approx V_{DD}$$

$$v_{OUT(min.)} \approx V_{SS}$$

High Gain, CMOS Inverters

Small Signal Characteristics

Model



Small Signal Voltage Gain:

$$v_{OUT} = -(g_{m1}v_{in} + g_{m2}v_{in})(r_{ds1} \,||\, r_{ds2})$$

OR

$$\frac{v_{out}}{v_{in}} = \frac{-(g_{m1} + g_{m2})}{(g_{ds1} + g_{ds2})} = \frac{-\sqrt{\left(\frac{2}{I_D}\right)}\left[\sqrt{K_N'\frac{W_1}{L_1}} + \sqrt{K_P'\frac{W_2}{L_2}}\right]}{\lambda_1 + \lambda_2} = \frac{K}{\sqrt{I_D}} \quad !!!$$

Set $g_{m2} = 0$ for the current source inverter

Assume that $i_D = 1\ \mu A$ and $\frac{W_1}{L_1} = \frac{W_2}{L_2}$, using the values of Table 3.1-2 gives

$$\frac{v_{OUT}}{v_{in}} = -328 \qquad \text{for the push-pull inverter (L=10 µm)}$$

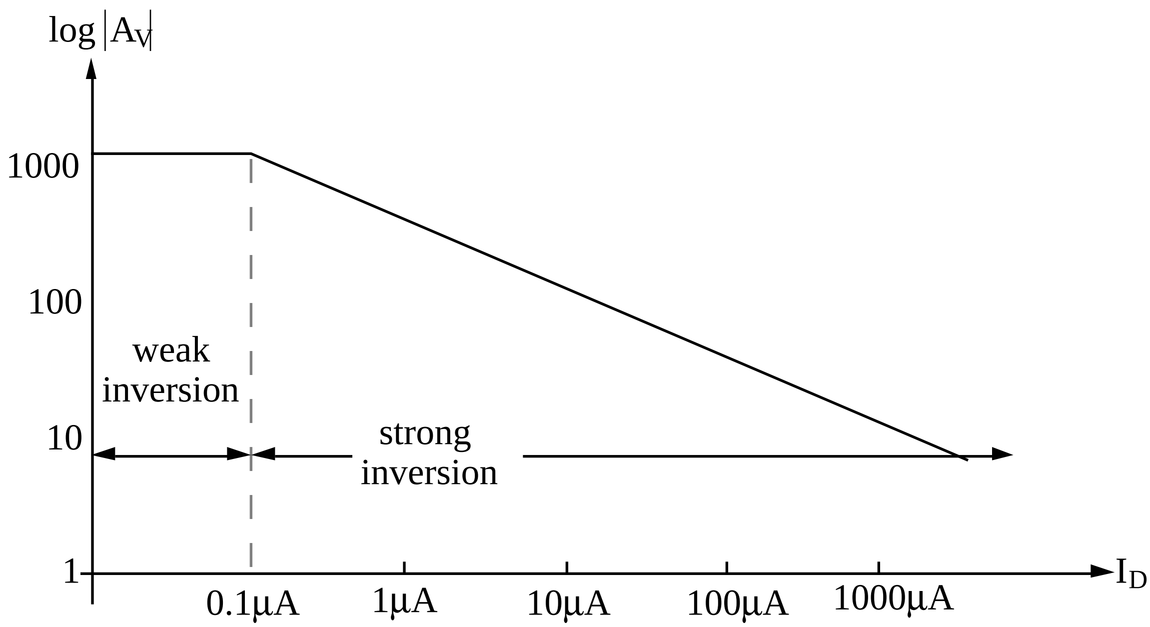
$$= -194 \qquad \text{for the current source inverter (L=10 µm)}$$

Small Signal Output Resistance:

$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}}$$

High Gain, CMOS Inverters

Dependence of Gain upon Bias Current



Limit is the subthreshold current where square law characteristic turns into an exponential characteristic.

Assume that the level where subthreshold effects begin is approximately 0.1µA, the maximum gains of the CMOS inverters become:

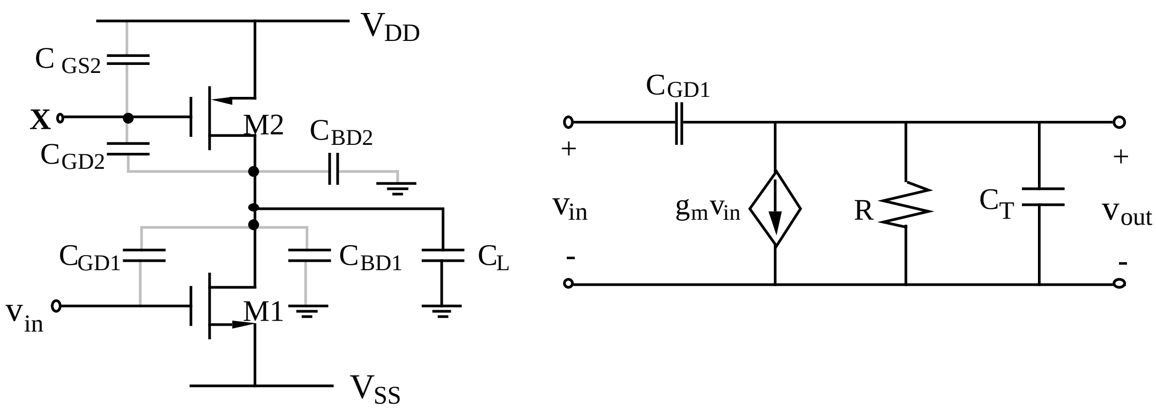
The CMOS inverters become:

$$\left.\begin{array}{ll}\text{Push-Pull:} & -1036 \\ \text{Current source load:} & -615 \\ \text{Current sink load:} & -422\end{array}\right\} \frac{W}{L} = 1,\ L = 10\ \mu\text{m}$$

Frequency Response of CMOS Inverters

General Configuration

$X = v_{OUT}$; Active Load CMOS Inverter ($g_m = g_{m1}$)
$X = V_{GG}$; CMOS Inverter with a Current Source Load ($g_m = g_{m1}$)
$X = v_{IN}$; CMOS Push Pull Inverter ($g_m = g_{m1} + g_{m2}$)



(a) General configuration of an inverter illustrating parasitic capacitances.
(b) Small signal model of (a)

C_{GD1} and C_{GD2} are overlap capacitances
C_{BD1} and C_{BD2} are the bulk-drain capacitances
C_L is the load capacitance seen by the inverter

Frequency Response

$$\frac{v_{OUT}}{v_{IN}} = \frac{-g_m R\omega_1(1- s/z)}{\left(s + \omega_1\right)} , \qquad \omega_1 = \frac{1}{RC} \quad \text{and} \quad z = \frac{g_m}{C_{GD1}}$$

$$R = \frac{1}{g_{ds1}+g_{ds2}+g_{m2}}$$ ($g_{m2} = 0$ for push pull and current source inverters)

$C \approx C_{GD1}+C_{GS2}+C_{BD1}+C_{BD2}+C_L$ (Active load inverter)

$C \approx C_{GD1}+C_{GD2}+C_{BD1}+C_{BD2}+C_L$ (Current source & push-pull inverter)

if $g_m R >> 1$

Frequency Response of CMOS Inverters

Dependence of Frequency Response on Bias Current -

When $g_{m2} \neq 0$ (active load inverter):

$$R \approx \frac{1}{g_{m2}} \quad \text{or} \quad \omega_{-3dB} = \frac{\sqrt{2K'\frac{W}{L} I_D}}{C} \sim \sqrt{I_D}$$

When $g_{m2} = 0$ (push pull and current source inverter):

$$R = \frac{1}{(\lambda_1 + \lambda_2)\, I_D} \quad \text{or} \quad \omega_{-3dB} = \frac{(\lambda_1 + \lambda_2)\, I_D}{C} \sim I_D$$

Example:

Find the –3dB frequency for the CMOS inverter using a current source load and the CMOS push pull inverter assuming that i_D = 1µA, $C_{GD1}=C_{GD2}=0.2$pF and $C_{BD1}=C_{BD2}=0.5$pF

Using the parameters of Table 3.1-2 and assuming that $\frac{W_1}{L_1} = \frac{W_2}{L_2} = 1$

Gives,

For the active load CMOS inverter,

$$\omega_{-3dB} = \frac{g_{m2}}{C} = 3.124\text{x}10^{-6} \text{ rads/sec or 512KHz}$$

For the push pull or current source CMOS inverter,

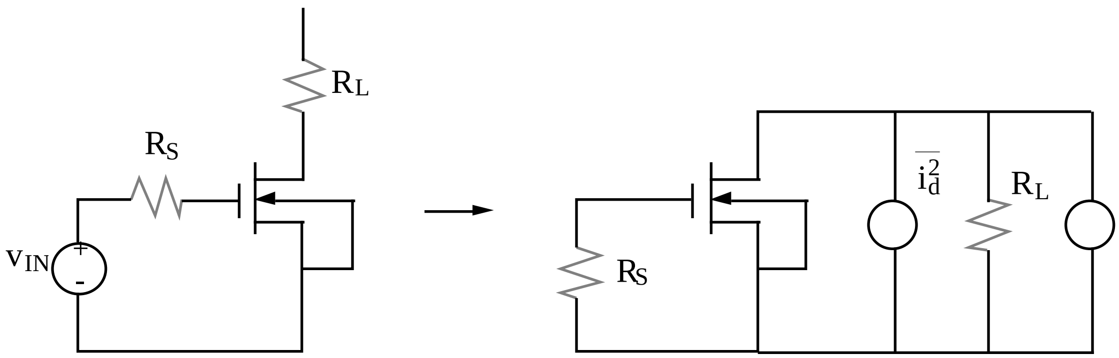
$$\omega_{-3dB} = \frac{g_{gd1} + g_{ds2}}{C} = 14.3\text{x}10^{3} \text{ rads/sec or 2.27 KHz}$$

$$z = \frac{g_{m1}}{C_{GD1}} = 29.155 \text{ Mrads/sec or 4.64 MHz}$$

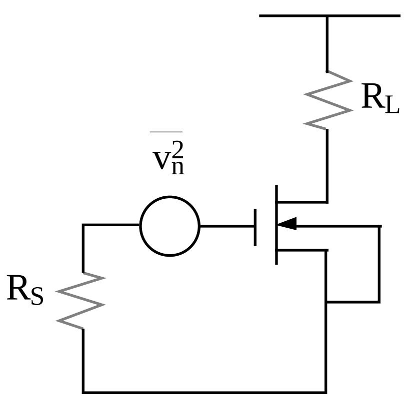
The reason for the difference is the higher output resistance of the push pull or current source CMOS inverters

NOISE IN MOS INVERTERS

Noise Calculation



We wish to determine the equivalent input noise voltage, $\overline{v_n^2}$ as shown below:



$$\overline{i_d^2} = \frac{8}{3}KTg_m \quad (A^2/Hz)$$

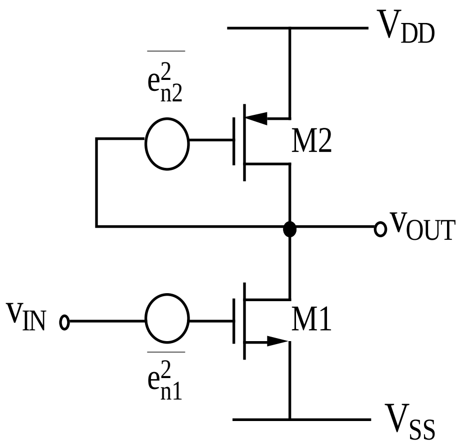
$$\overline{i_L^2} = \frac{4KT}{R_L} \quad (A^2/Hz)$$

Comments:

1.) 1/f noise has been ignored.

2.) Resistors are noise-free, they are used to show topological aspects. Can repeat the noise analysis for the resistors if desired.

Noise in an Active Load Inverter



$$\overline{e_{out}^2}\Big|_{v_{IN}=0} = \overline{e_{n1}^2}\left(\frac{g_{m1}}{g_{m2}}\right)^2 + \overline{e_{n2}^2}$$

$$\overline{e_{eq}^2} = \frac{\overline{e_{out}^2}}{\left(\frac{g_{m1}}{g_{m2}}\right)^2} = \overline{e_{n1}^2} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \overline{e_{n2}^2}$$

$$\overline{e_{eq}^2} = \overline{e_{n1}^2}\left[1 + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \left(\frac{\overline{e_{n2}^2}}{\overline{e_{n1}^2}}\right)\right]$$

Sec 3.2, Eq (15)

1/f noise: $\overline{e_n^2} = \frac{B}{fWL}$; B=constant for a process

Sec. 3.3, Eq (6)

$$g_m = \sqrt{\frac{2K'W}{L} I_D}$$

So $$\overline{e_{eq}^2} = \overline{e_{n1}^2}\left[1 + \frac{\left(2K_P'\left(\frac{W_2}{L_2}I_D\right)\right)}{\left(2K_N'\left(\frac{W_1}{L_1}I_D\right)\right)}\left(\frac{B_P}{fW_2L_2}\right)\left(\frac{fW_1L_1}{B_N}\right)\right]$$

$$\boxed{\overline{e_{eq}^2} = \overline{e_{n1}^2}\left[1 + \left(\frac{K_P'B_P}{K_N'B_N}\right)\left(\frac{L_1}{L_2}\right)^2\right]}$$

To minimize 1/f noise -

1). $L_2 >> L_1$ -----> Gain = $-\sqrt{\frac{K_N'W_1}{K_P'W_2}}\sqrt{\frac{L_2}{L_1}}$

2). $\overline{e_{n1}^2}$ small

Noise in An Active Load Inverter - (Cont'd)

Suppose the noise is thermal - Sec. 3.2, Eq,(13)

$$\overline{e_n^2} = \frac{8kT(1+\eta)}{3g_m}$$

$$\overline{e_{eq}^2} = \frac{8kT(1+\eta_1)}{3g_{m1}}\left[1 + \left(\frac{g_{m2}{}^2}{g_{m1}{}^2}\right)\left(\frac{(1+\eta_2)g_{m1}}{(1+\eta_1)g_{m2}}\right)\right]$$

$$\boxed{\overline{e_{eq}^2} = \frac{8kT(1+\eta_1)}{3g_{m1}}\left[1 + \frac{(1+\eta_2)}{(1+\eta_1)}\left(\frac{K_P'\frac{W_2}{L_2}}{K_N'\frac{W_1}{L_1}}\right)^{1/2}\right]}$$

or

$$\boxed{\overline{e_{eq}^2} = \frac{8kT(1+\eta_1)}{3g_{m1}}\left[1 + \left(\frac{1+\eta_2}{1+\eta_1}\right)\left(\frac{g_{m2}}{g_{m1}}\right)\right]}$$

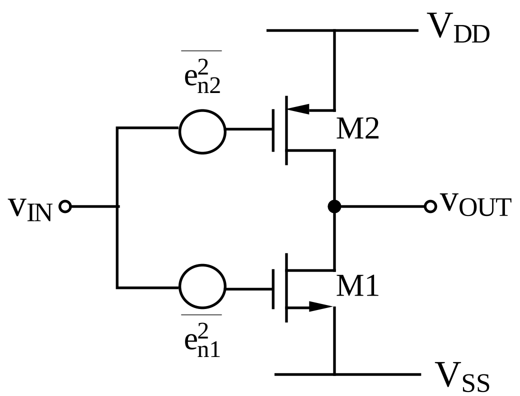
To minimize thermal noise -

1. Maximize gain $\left(\frac{g_{m1}}{g_{m2}}\right)$
2. Increase $g_{m1} = \sqrt{\frac{2K_N W_1}{L_1} I_D}$

Noise in Other Types of Inverters

Current Source Load Inverter -> same as active load inverter

Push-Pull Inverter-



$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}}$$

$$\overline{e_{out}^2} = (g_{m1}r_{out})^2\,\overline{e_{n1}^2} + (g_{m2}r_{out})^2\,\overline{e_{n2}^2}$$

$$v_{out} = -(g_{m1} + g_{m2})r_{out}v_{in}$$

$$\overline{e_{eq}^2} = \left(\frac{g_{m1}}{g_{m1} + g_{m2}}\right)^2 \overline{e_{n1}^2} + \left(\frac{g_{m2}}{g_{m1} + g_{m2}}\right)^2 \overline{e_{n2}^2}$$

$$\overline{e_{eq}^2} = \overline{e_{n1}^2}\left[\frac{1 + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \frac{\overline{e_{n2}^2}}{\overline{e_{n1}^2}}}{\left(1 + \frac{g_{m2}}{g_{m1}}\right)^2}\right] = \overline{e_{n1}^2}\left[\frac{1 + \left(\frac{K'_P B_P}{K'_N B_N}\right)\left(\frac{L_1}{L_2}\right)^2}{\left(1 + \frac{K'_P W_2 L_1}{K'_N W_1 L_2}\right)^2}\right]$$

To minimize noise - Reduce $\overline{e_{n1}^2}$ and $\overline{e_{n2}^2}$.

SUMMARY OF MOS INVERTERS

Inverter Type	AC Voltage Gain	AC Output Resistance	Bandwidth (C_{GB}=0)	Equivalent, input-referred, mean-square noise voltage
p-channel active load sinking inverter	$\frac{-g_{m1}}{g_{m2}}$	$\frac{1}{g_{m2}}$	$\frac{g_{m2}}{C_{BD1}+C_{GS1}+C_{GS2}+C_{BD2}}$	$\overline{v_{n1}^2}\left(\frac{g_{m1}}{g_{m2}}\right)^2+\overline{v_{n2}^2}$
n-channel active load sinking inverter	$\frac{-g_{m1}}{g_{m2+gmb2}}$	$\frac{1}{g_{m2}+g_{mb2}}$	$\frac{g_{m2}+g_{mb2}}{C_{BD1}+C_{GD1}+C_{GS2}+C_{BD2}}$	$\overline{v_{n1}^2}\left(\frac{g_{m1}}{g_{m2}}\right)^2+\overline{v_{n2}^2}$
Current source load sinking inverter	$\frac{-g_{m1}}{g_{ds1}+g_{ds2}}$	$\frac{1}{g_{ds1}+g_{ds2}}$	$\frac{g_{ds1}+g_{ds2}}{C_{BD1}+C_{GD1}+C_{GS2}+C_{BD2}}$	$\overline{v_{n1}^2}\left(\frac{g_{m1}}{g_{m2}}\right)^2+\overline{v_{n2}^2}$
Push-Pull inverter	$\frac{-(g_{m1}+g_{m2})}{g_{ds1}+g_{ds2}}$	$\frac{1}{g_{ds1}+g_{ds2}}$	$\frac{g_{ds1}+g_{ds2}}{C_{BD1}+C_{GD1}+C_{GS2}+C_{BD2}}$	$\left(\frac{\overline{v_{n1}^2}g_{m1}}{g_{m1}+g_{m2}}\right)^2+\left(\frac{\overline{v_{n2}^2}g_{m2}}{g_{m1}+g_{m2}}\right)^2$

KEY MOSFET RELATIONSHIP USEFUL FOR DESIGN

Assume MOSFET is in saturation.

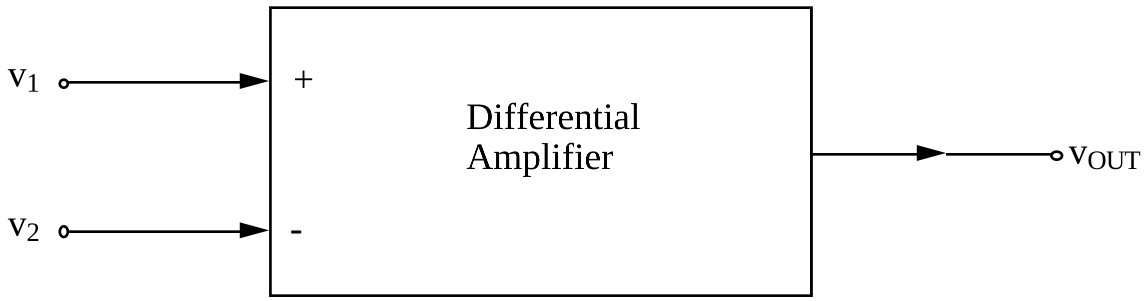
1.) $i_D = \frac{KW}{2L}(v_{GS} - V_T)^2$ or $v_{GS} = \sqrt{\frac{2i_D}{KW/L}} - V_T$

2.) $v_{DS}(sat) = \sqrt{\frac{2i_D}{KW/L}}$ or $i_D(sat) = \frac{KW}{2L} v_{DS}(sat)^2$

3.) $g_m = \sqrt{\frac{2I_D KW}{L}}$ or $g_m = \frac{KW}{L}(V_{GS} - V_T)$

VI.2 - DIFFERENTIAL AMPLIFIERS

Definition of a Differential Amplifier



$$v_{OUT} = A_{VD}(v_1 - v_2) \pm A_{VC}\left(\frac{v_1 + v_2}{2}\right)$$

Differential voltage gain = A_{VD} (100)

Common mode voltage gain = A_{VC} (1)

Common mode rejection ratio = $\frac{A_{VD}}{A_{VC}}$ (1000)

Input offset voltage = $V_{OS}(in) = \frac{V_{OS}(out)}{A_{VD}}$ (2-10mV)

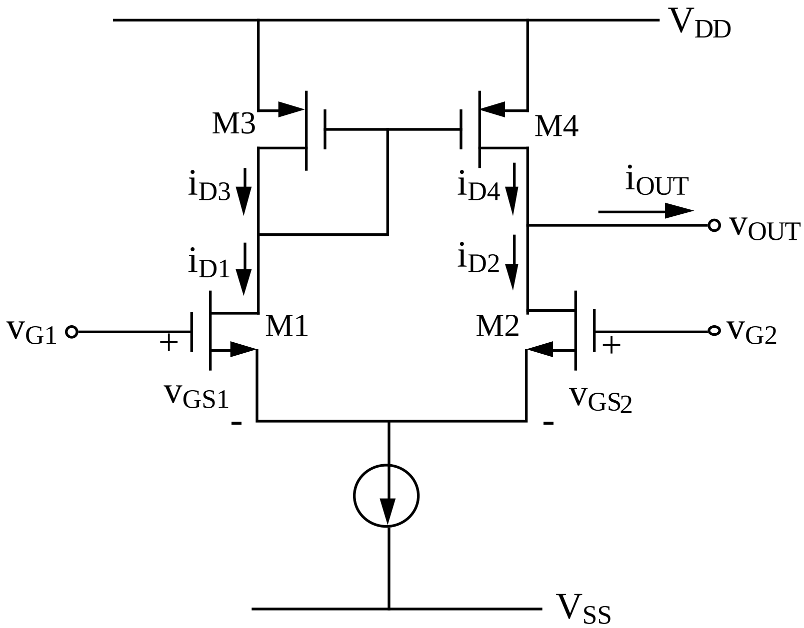
Common mode input range = V_{ICMR} ($V_{SS}+2V<V_{ICMR}<V_{DD}-2V$)

Power supply rejection ratio (PSRR)

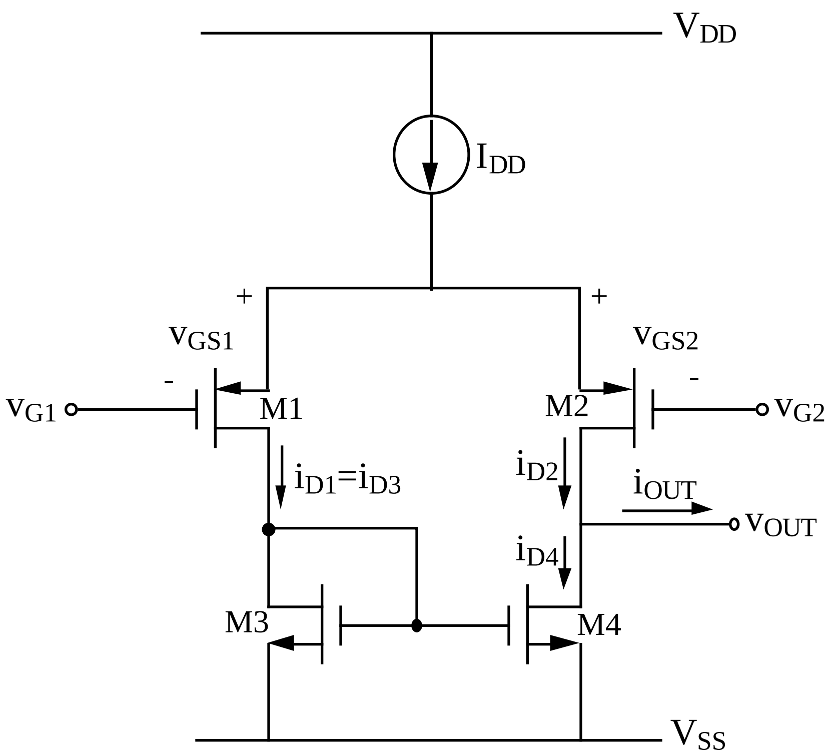
Noise

VI.2-1 - CMOS DIFFERENTIAL AMPLIFIERS

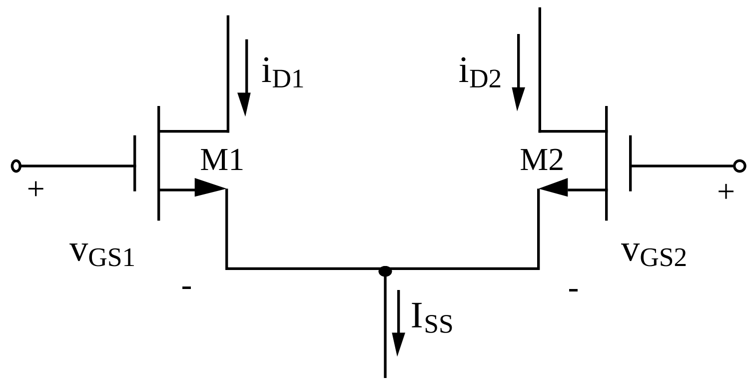
N-Channel Input Pair Differential Amplifier



P-Channel Input Pair Differential Amplifier



Large Signal Analysis of CMOS Differential Amplifiers



(1). $v_{ID} = v_{GS1} - v_{GS2} = \sqrt{\frac{2i_{D1}}{\beta}} - \sqrt{\frac{2i_{D2}}{\beta}}$

(2). $I_{SS} = i_{D1} + i_{D2}$

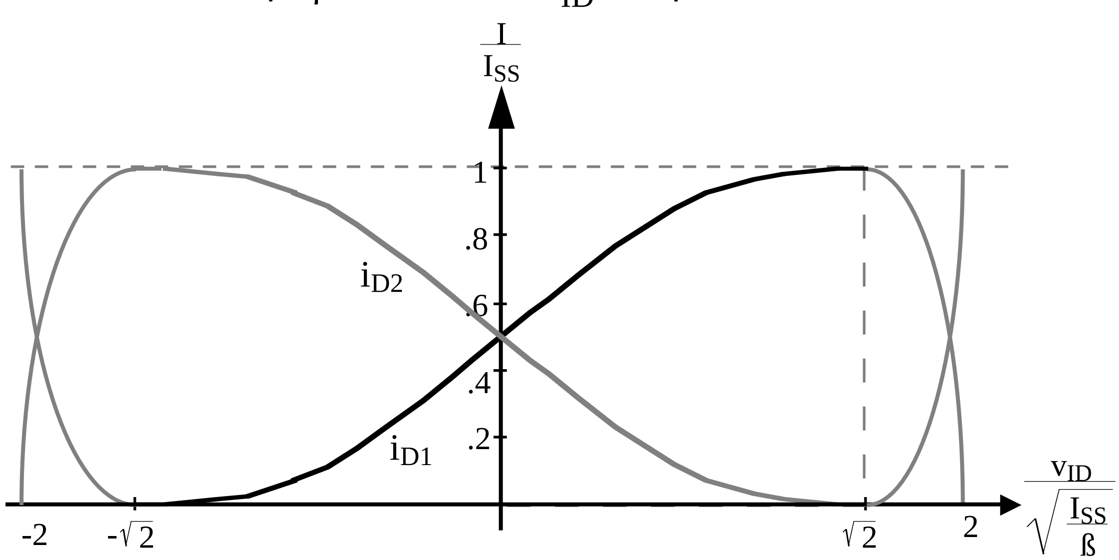
Solving for i_{D1} and i_{D2} gives,

(3). $i_{D1} = \left(\frac{I_{SS}}{2}\right) + \left(\frac{I_{SS}}{2}\right) v_{ID} \sqrt{\frac{\beta}{I_{SS}} - \frac{\beta^2 v_{ID}^2}{4I_{SS}^2}}$

And

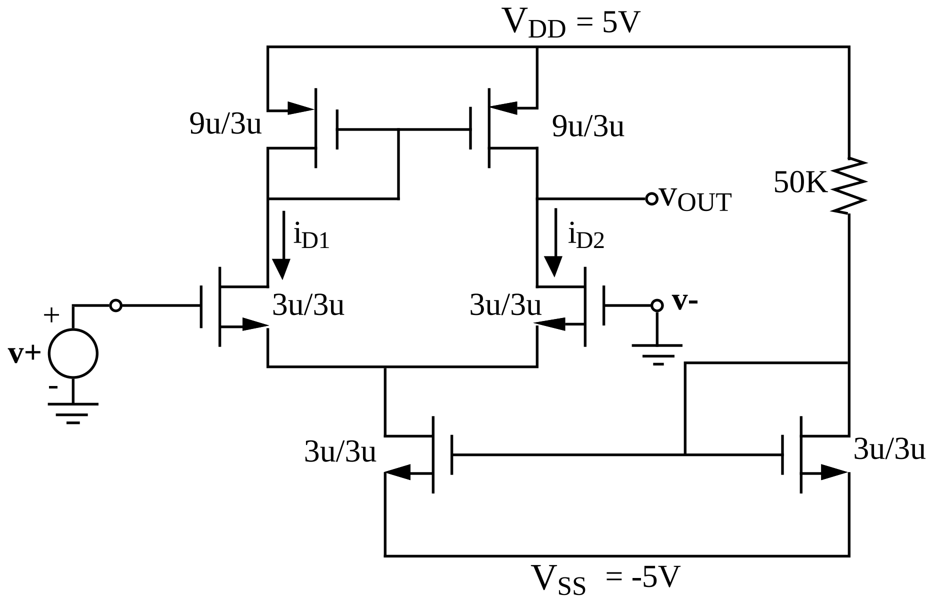
(4). $i_{D2} = \left(\frac{I_{SS}}{2}\right) - \left(\frac{I_{SS}}{2}\right) v_{ID} \sqrt{\frac{\beta}{I_{SS}} - \frac{\beta^2 v_{ID}^2}{4I_{SS}^2}}$

Where $v_{ID} < 2\sqrt{\frac{I_{SS}}{\beta}}$ $\qquad g_m = \frac{\partial i_{D1}}{\partial v_{ID}} = \sqrt{\frac{\beta I_{SS}}{4}}$

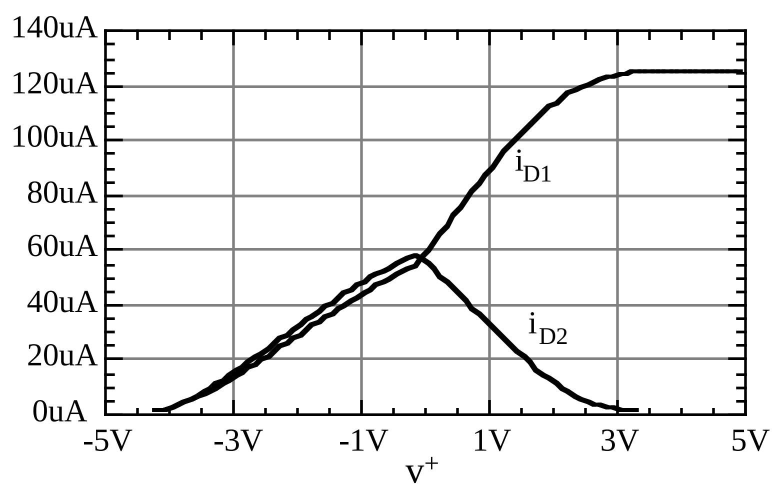


Transconductance Characteristics of the Differential Amplifier

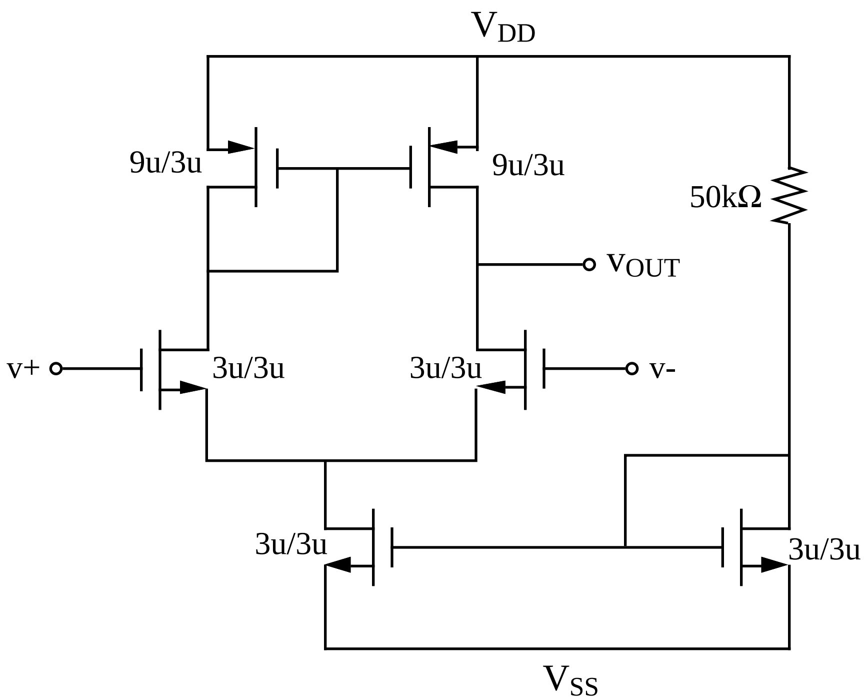
Circuit

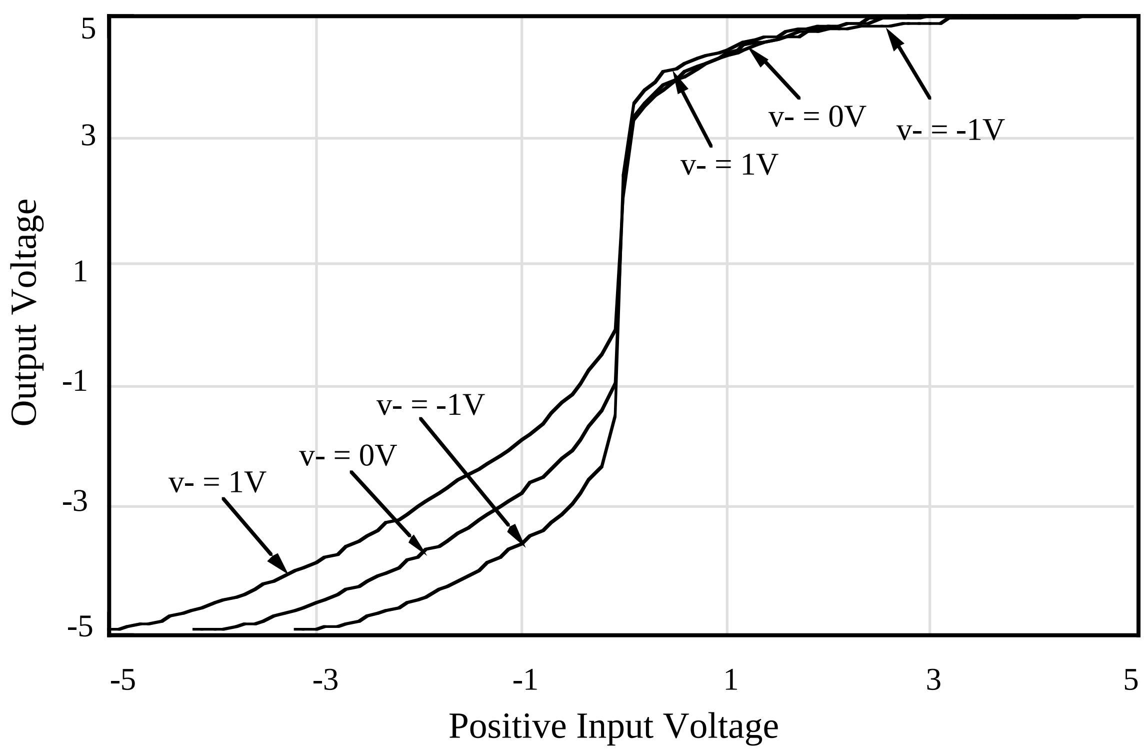


Simulation Results

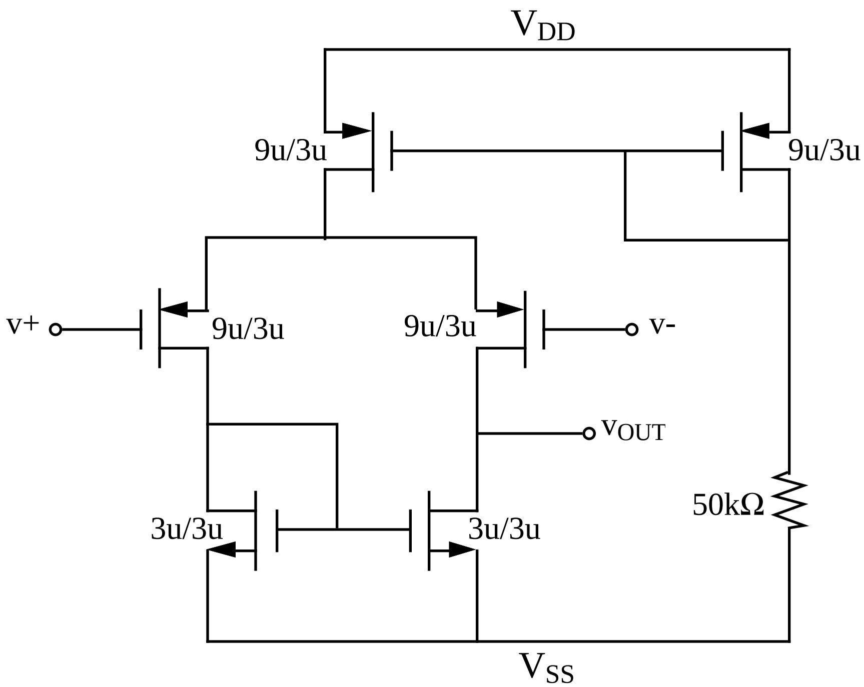


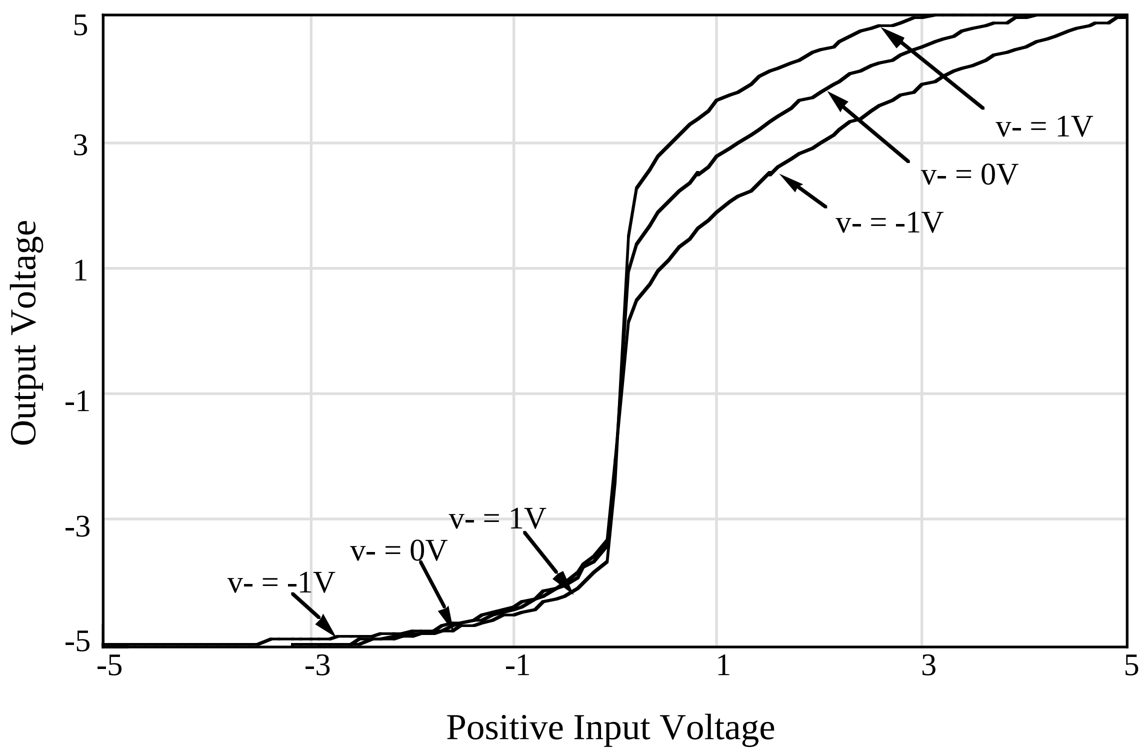
Voltage Transfer Curve of n-channel Differential Amplifier





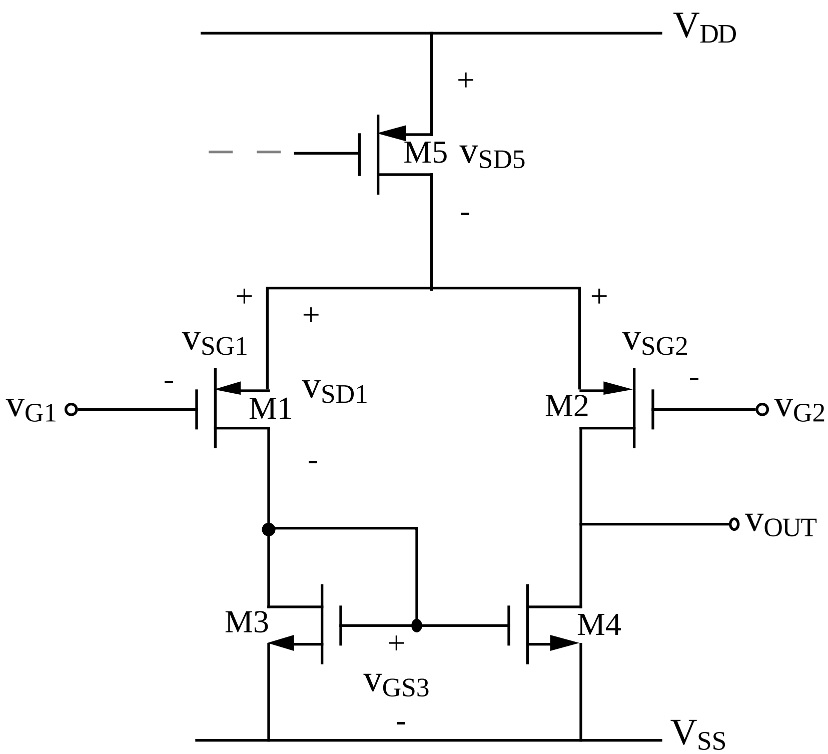
Voltage Transfer Curve for a p-channel Differential Amplifier





COMMON MODE INPUT RANGE

P-Channel Input Pair Differential Amplifier



Lowest common mode input voltage at gate of M1(M2)

$v_{G1(min)} = V_{SS} + v_{GS3} + v_{SD1} - v_{SG1}$

for saturation, the minimum value of $v_{SD1} = v_{SG1} - |V_{T1}|$

Therefore, $v_{G1(min)} = V_{SS} + v_{GS3} - |V_{T1}|$

or, $v_{G1(min)} = V_{SS} + \sqrt{\frac{I_{SS}}{\beta}} + V_{TO3} - |V_{T1}|$

$v_{G1(max)} = V_{DD} - v_{SD5} - v_{SG1} = V_{DD} - v_{SD5} - \sqrt{\frac{2I_{D1}}{\beta_1}} - |V_{T1}|$

COMMON MODE RANGE-CONT'D

Example

Assume that V_{DD} varies from 8 to 12 volts and that V_{SS} = 0. Using the values of Table 3.1-2, find the common mode range for worst case conditions. Assume that I_{SS} = 100µA, $W_1/L_1 = W_2/L_2 = 5$, $W_3/L_3 = W_4/L_4 = 1$, and v_{SD5} = 0.2V. Include the worst case value of K' in the calculations.

If V_{DD} varies 10 ± 2V, then we get

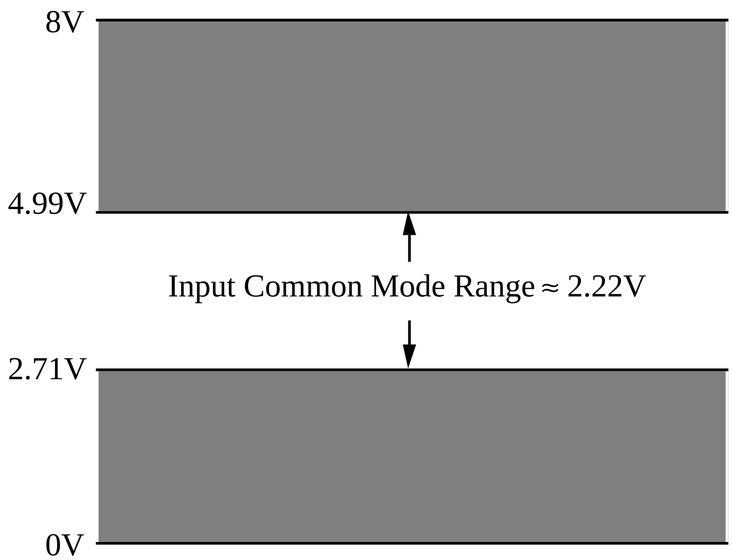
$$v_{G1(max)} = V_{DD} - v_{SD5} - \sqrt{\frac{I_{SS}}{\beta_1}} - |V_{T1}|$$

$$= 8 - 0.2 - \sqrt{\frac{100}{5x7.2}} - 1.2 = 6.6 - 1.67 = 4.99V$$

$$v_{G1(min)} = V_{SS} + \sqrt{\frac{I_{SS}}{\beta_3}} + V_{TO3} - |V_{T1}|$$

$$= 0 + \sqrt{\frac{100}{1x18.7}} + 1.2 - 0.8 = 0.4 + 2.31 = 2.71V$$

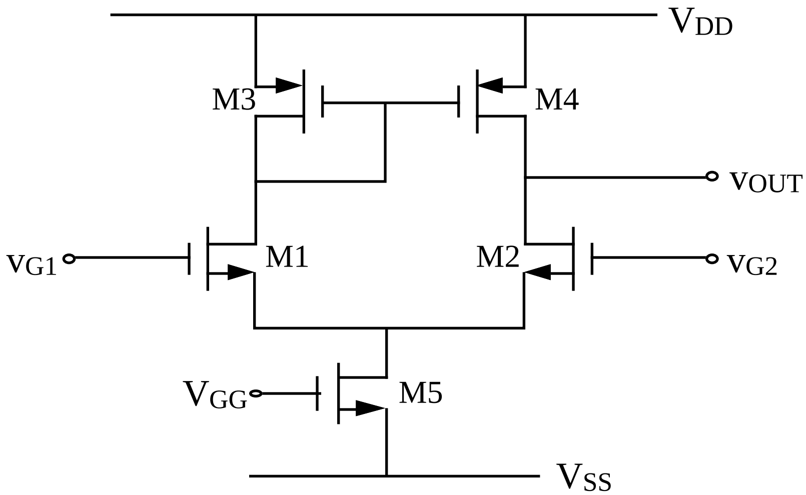
Therefore, the input common mode range of the p-channel input differential amplifier is from 2.71V to 4.99V


8V
4.99V
Input Common Mode Range ≈ 2.22V
2.71V
0V

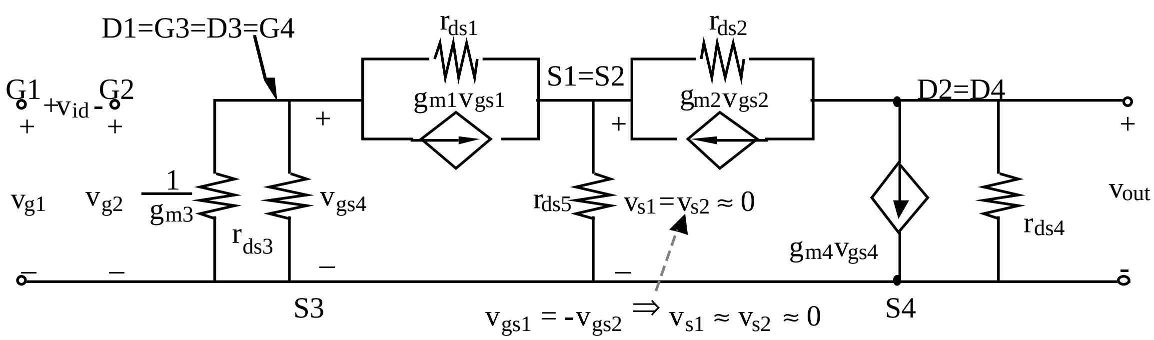
CMOS DIFFERENTIAL AMPLIFIER

Small Signal Differential Mode Gain

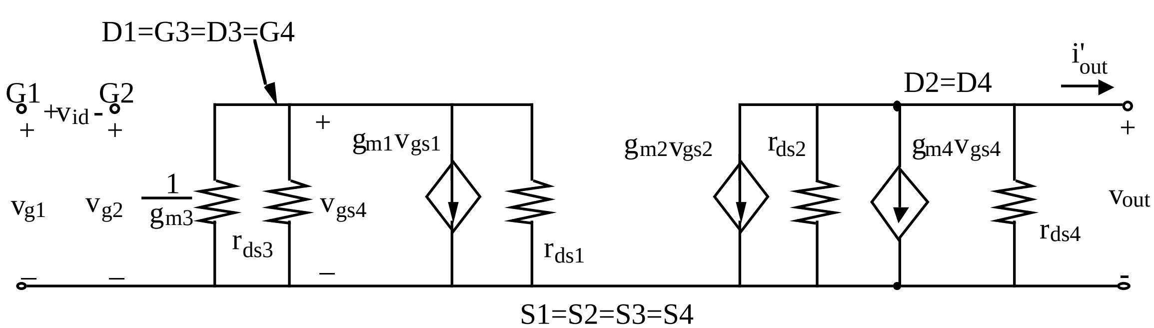
N-Channel input differential amplifier -



Exact small signal model -



Simplified small signal model using symmetry -



$v_{gs1} = 0.5v_{id}$ and $v_{gs2} = -0.5v_{id}$

CMOS DIFFERENTIAL AMPLIFIER

Unloaded Differential Transconductance Gain
(R_L =0)

$$i_{out}' = -g_{m4}v_{gs4} - g_{m2}v_{gs2} = \frac{g_{m1}g_{m4}(r_{ds1} \| r_{ds3})}{1 + g_{m3}(r_{ds1} \| r_{ds3})} v_{gs1} - g_{m2}v_{gs2}$$

If $g_{m3}(r_{ds1} \| r_{ds3}) >> 1$, $g_{m3} = g_{m4}$, and $g_{m1} = g_{m2} = g_{md}$, then

$$i_{out}' \approx g_{m1}v_{gs1} - g_{m2}v_{gs2} = g_{md}(v_{gs1} - v_{gs2}) = g_{md}v_{id}$$

or

$$\boxed{i_{out}' \approx g_{md}v_{id} = \sqrt{\frac{K_N'WI_{SS}}{L}}\, v_{id}}$$

Unloaded Differential Voltage Gain
($R_L = \infty$)

$$\boxed{v_{out} \approx \frac{g_{md}}{g_{ds2} + g_{ds4}} v_{id} = \frac{2}{(\lambda_N + \lambda_P)}\sqrt{\frac{K_N'W}{I_{SS}L}}\, v_{id}}$$

Example

If all W/L ratios are 3µm/3µm and I_{SS} = 10µA, then

$$g_{md}(\text{N-channel}) = \sqrt{(17\text{x}10^{-6})(10\text{x}10^{-6})} = 13\ \mu A/V$$

$$g_{md}(\text{P-channel}) = \sqrt{(8\text{x}10^{-6})(10\text{x}10^{-6})} = 8.9\ \mu A/V$$

and

$$\frac{v_{out}}{v_{id}}(\text{N-channel}) = \frac{2(13\text{x}10^{-6})}{(0.01+0.02)10\text{x}10^{-6}} = 86.67$$

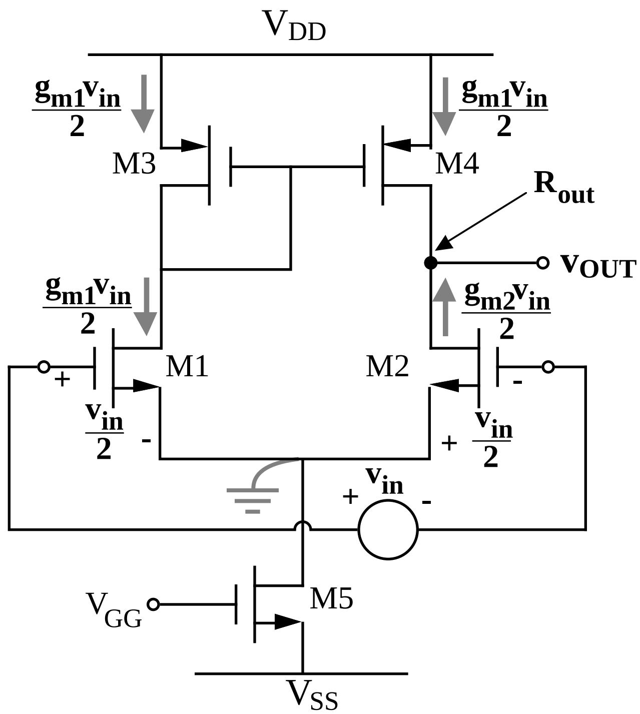
$$\frac{v_{out}}{v_{id}}(\text{P-channel}) = \frac{2(8.9\text{x}10^{-6})}{(0.01+0.02)10\text{x}10^{-6}} = 59.33$$

INTUITIVE SMALL SIGNAL ANALYSIS OF MOSFET CIRCUITS

Principle: Consider only small changes superimposed on the dc conditions.

Technique: Identify the transistor(s) that convert input voltage to current (these transistors are called the active devices). Trace the currents to where they flow into the resistance seen from a given node and multiply this resistance times the currents to find the voltage at this node.

Example - Differential Amplifier



Current flowing into the output node (drains of M2 and M4) is

$$i_{out} = \frac{g_{m1}v_{in}}{2} + \frac{g_{m2}v_{in}}{2}$$

Output resistance, R_{out}, seen at this node is

$$R_{out} = r_{ds2}||r_{ds4} = \frac{1}{g_{ds2}+g_{ds4}}$$

Therefore, the open circuit voltage gain is

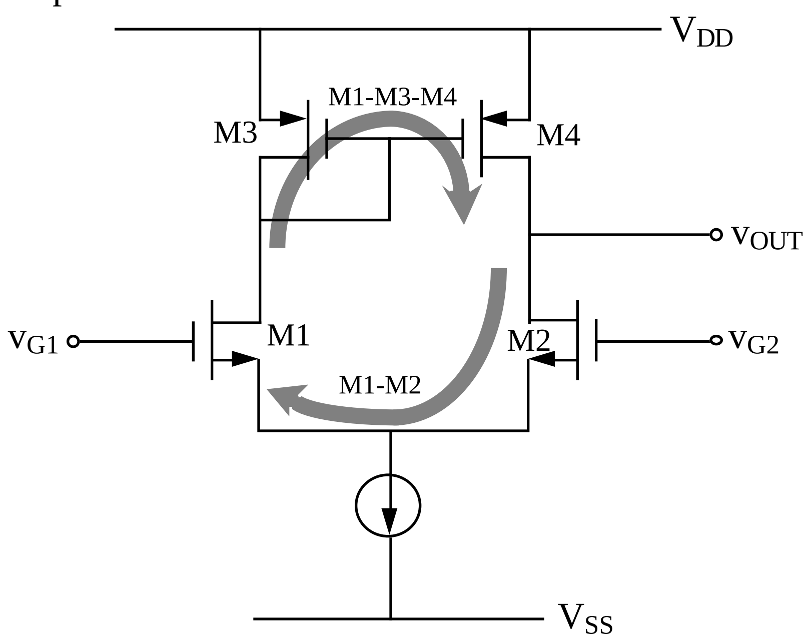
$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}+g_{m2}}{2(g_{ds2}+g_{ds4})} = \frac{g_{m1}}{g_{ds2}+g_{ds4}} = \frac{g_{m2}}{g_{ds2}+g_{ds4}}$$

CMOS DIFFERENTIAL AMPLIFIER

Common Mode Gain

The differential amplifier that uses a current mirror load should theoretically have zero common mode gain.

For example:

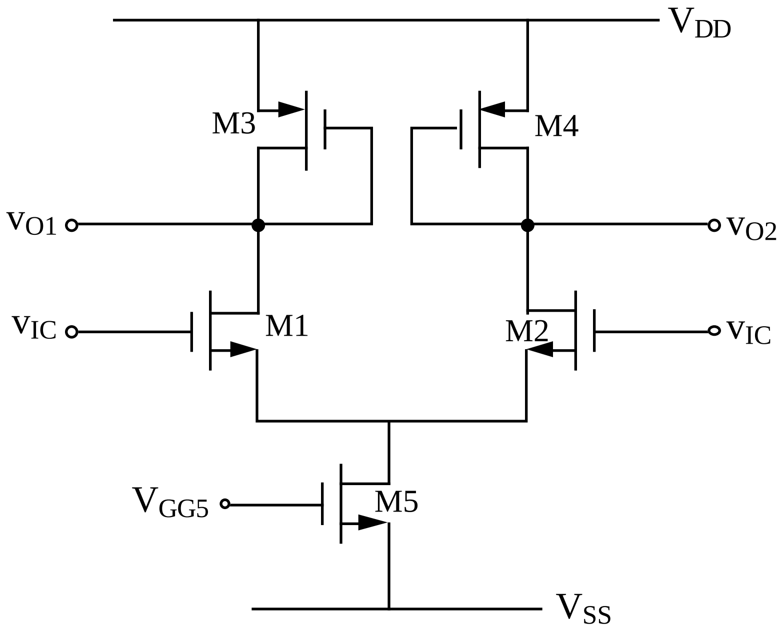


$$\begin{bmatrix}\text{Total Common}\\ \text{mode output}\\ \text{due to } v_{IC}\end{bmatrix} = \begin{bmatrix}\text{Common mode}\\ \text{output due to}\\ \text{M1-M3-M4 path}\end{bmatrix} - \begin{bmatrix}\text{Common mode}\\ \text{output due to}\\ \text{M1–M2 path}\end{bmatrix}$$

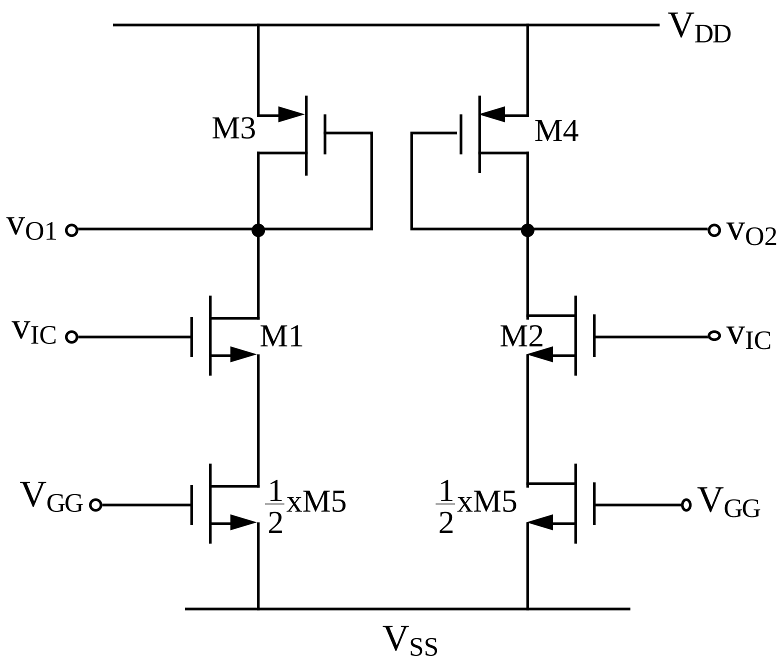
Therefore, the common mode gain will approach zero and is nonzero because of mismatches in the gain between the two paths.

CMOS DIFFERENTIAL AMPLIFIER

Consider the following differential amplifier -

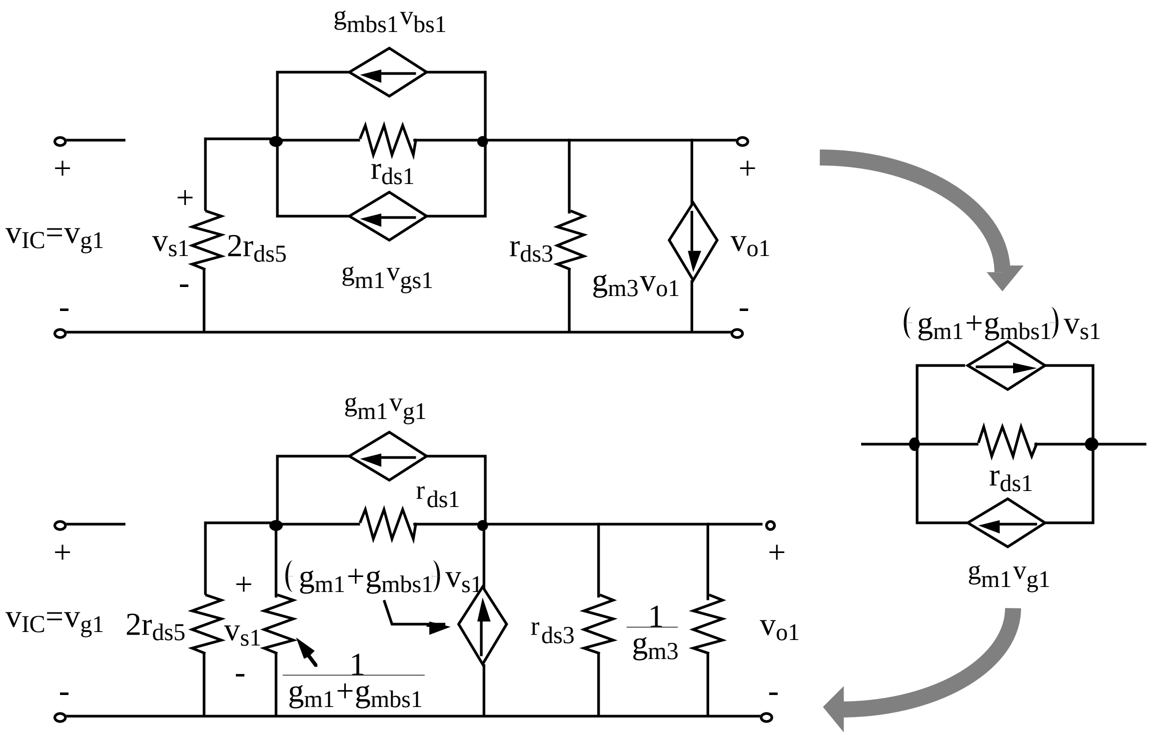


Use of symmetry to simplify gain calculations -



CMOS DIFFERENTIAL AMPLIFIER

Small signal model -



Writing nodal equations -

$$\left[0.5g_{ds} + g_{ds1} + g_{mbs1}\right] v_{s1} - \left[g_{ds1}\right] v_{o1} = g_{m1}v_{IC}$$
$$-\left[g_{ds1} + g_{m1} + g_{mbs1}\right] v_{o1} + \left[g_{ds1} + g_{ds3} + g_{m3}\right] v_{o1} = -g_{m1}v_{IC}$$

Solving for $\frac{v_{o1}}{v_{IC}}$ gives,

$$\frac{v_{o1}}{v_{IC}} = \frac{-0.5g_{m1}g_{ds5}}{\left(g_{ds3}+g_{m3}\right)\left[0.5g_{ds} + g_{m1} + g_{mbs1} + g_{ds1}\right] + 0.5g_{ds1}g_{ds5}}$$

or

$$\frac{v_{o1}}{v_{IC}} \approx \frac{-0.5g_{m1}g_{ds5}}{g_{m3}\left(g_{m1} + g_{mbs1}\right)} \approx \frac{-g_{ds5}}{2g_{m3}}$$

COMMON MODE REJECTION RATIO (CMRR)

$$\text{CMRR} = \frac{\text{Differential mode gain}}{\text{Common mode gain}} = \frac{A_{vd}}{A_{vc}}$$

For the previous example,

$$|\text{CMRR}| = \frac{\left(\frac{g_{m1}}{g_{m3}}\right)}{\left(\frac{g_{m1}g_{ds5}}{2g_{m3}\left(g_{m1} + g_{mbs1}\right)}\right)} = \frac{2(g_{m1} + g_{mbs1})}{g_{ds5}} \approx \frac{2g_{m1}}{g_{ds5}}$$

Therefore, current sinks/sources with a larger output resistance(r_{ds5}) will increase the CMRR.

Example

Let all W/L ratios be unity, I_{SS} = 100µA, and use the values of Table 3.1-2 to find the CMRR of a CMOS differential amplifier.

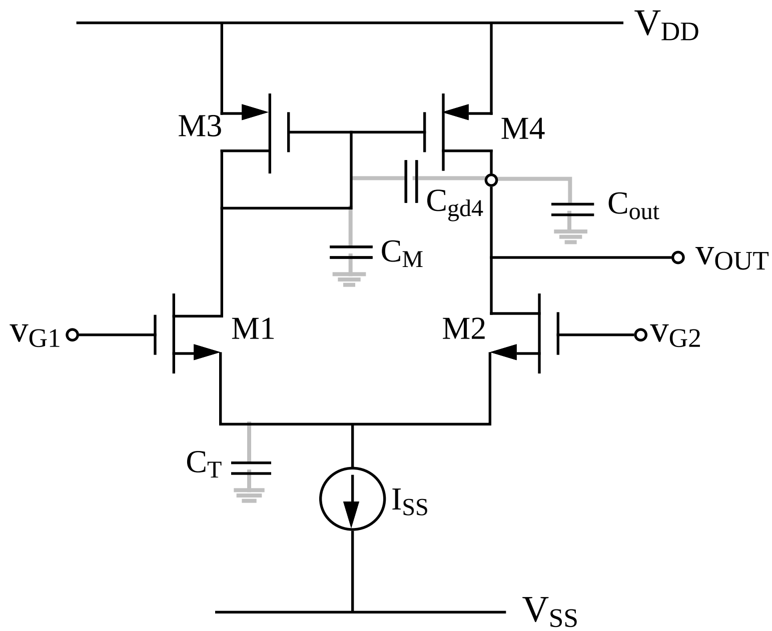
$g_{m1} = \sqrt{2\text{x}17(\mu\text{A/V}^2)\text{x}100\mu\text{A}} = 58.3\mu\text{S}$

$g_{ds5} = 0.01\text{V}^{-1} \text{ x } 100\mu\text{A} = 1\mu\text{S}$

Therefore, |CMRR| = 116

CMOS DIFFERENTIAL AMPLIFIERS

Parasitic Capacitances

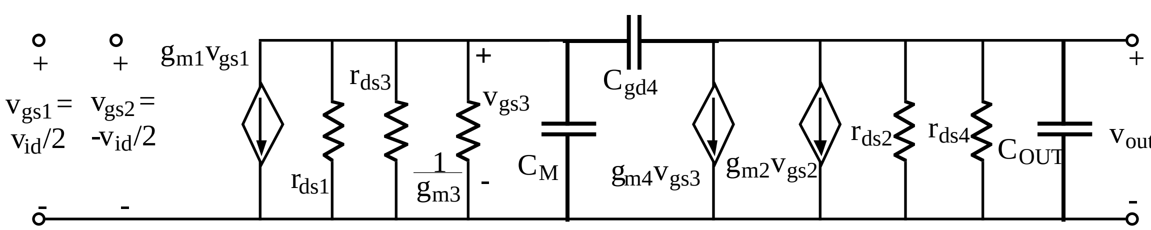


C_T = tail capacitor (common mode only)

C_M = mirror capacitor = $C_{dg1} + C_{db1} + C_{gs3} + C_{gs4} + C_{db3}$

C_{OUT} = output capacitor ≈ $C_{bd4} + C_{bd2} + C_{gd2} + C_L$

Small Signal Model



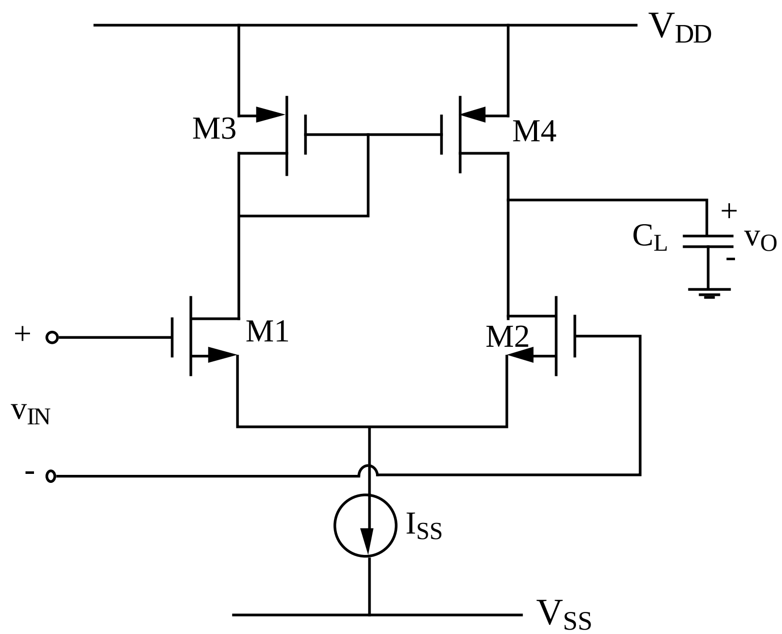
We will examine the frequency response of the differential amplifier in more detail later.

SLEW RATE

Slew rate is defined as an output voltage rate limit usually caused by the current necessary to charge a capacitance.

i.e. $i = C\left(\frac{dV}{dT}\right)$

For the CMOS differential amplifier shown,



Slew rate $= \frac{I_{SS}}{C_L}$

where C_L is the total capacitance seen from the output node to ground.

If C_L = 5pF and I_{SS} = 10µA, then the SR = 2V/µS

CMOS DIFFERENTIAL AMPLIFIERS

NOISE

Assumption:

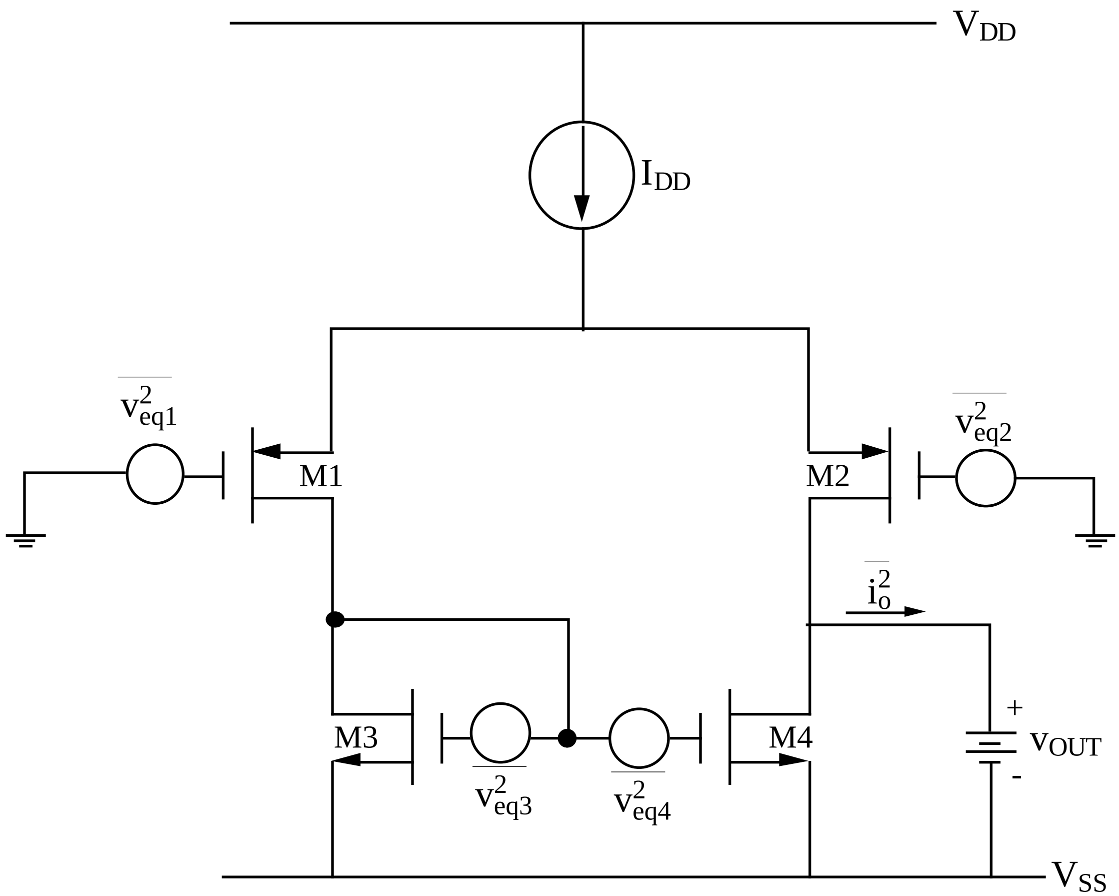
Neglect thermal noise(low frequency) and ignore the thermal noise sources of r_d and r_s .

Therefore:

$$\overline{i_{nd}^2} = \left(\frac{KF}{fC_{ox}L^2}\right) i_D^{AF} \quad (AF = 0.8 \text{ and } KF = 10^{-28})$$

or

$$\overline{v_{nd}^2} = \frac{\overline{i_{nd}^2}}{g_m^2} = \left(\frac{KF}{2f\mu_o C_{ox}{}^2 WL}\right) i_D^{(AF-1)}$$



VDD
IDD
veq1
M1
M2
veq2
io
M3
M4
veq3
veq4
+
vOUT
-
VSS

CMOS DIFFERENTIAL AMPLIFIERS

NOISE

Total output noise current is found as,

$$\overline{i_{od}^2} = g_{m1}^2\,\overline{v_1^2} + g_{m2}^2\,\overline{v_2^2} + g_{m3}^2\,\overline{v_3^2} + g_{m4}^2\,\overline{v_4^2}$$

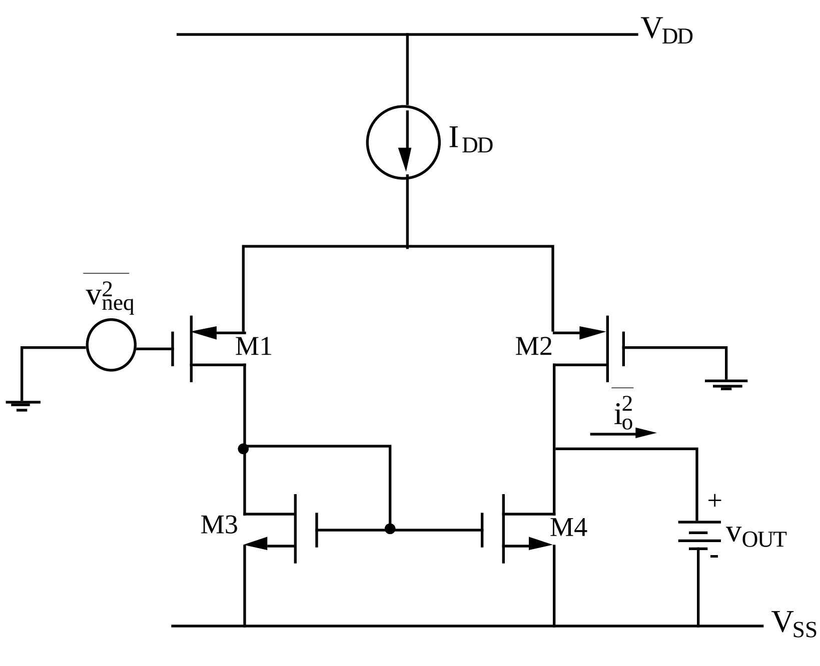
Define $\overline{v_{neq}^2}$ as the equivalent input noise voltage of the differential amplifier. Therefore,

$$\overline{i_{od}^2} = g_{m1}^2\,\overline{v_{neq}^2}$$

or

$$\overline{v_{neq}^2} = \overline{v_{eq1}^2} + \overline{v_{eq2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2\left(\overline{v_{eq3}^2} + \overline{v_{eq4}^2}\right)$$

Where $g_{m1} = g_{m2}$ and $g_{m3} = g_{m4}$



It is desirable to increase the transconductance of M1 and M2 and decrease the transconductance of M3 and M4. (Empirical studies suggest p-channel devices have less noise)

CMOS DIFFERENTIAL AMPLIFIERS

Minimization of Noise

$$\overline{v_{neq}^2} = \overline{v_{eq1}^2} + \overline{v_{eq2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \left(\overline{v_{eq3}^2} + \overline{v_{eq4}^2}\right)$$

In terms of voltage spectral-noise densities we get,

$$\overline{e_{eq}^2} = \overline{e_{n1}^2} + \overline{e_{n2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \left(\overline{e_{n3}^2} + \overline{e_{n4}^2}\right)$$

1/f noise

Let $\overline{e_n^2} = \dfrac{KF}{2fC_{ox}WLK'} = \dfrac{B}{fWL}$

assume $\overline{e_{n1}^2} = \overline{e_{n2}^2}$ and $\overline{e_{n3}^2} = \overline{e_{n4}^2}$

$$\therefore \quad \overline{e_{eq}^2}\,(1/f) = \left(\frac{2B_P}{fW_1L_1}\right)\left[1 + \frac{K_N'B_N}{K_P'B_P}\left(\frac{L_1}{L_3}\right)^2\right]$$

1) Since $B_N \approx 5B_P$ use PMOS for M1 and M2 with large area.

2) Make $\dfrac{L_1}{L_3} < \dfrac{K_P'B_P}{K_N'B_N} \approx \dfrac{1}{12.5}$ so that $\overline{e_{eq}^2}\,(1/f) \approx \sqrt{\dfrac{2B_P}{fW_1L_1}}$

Thermal Noise

$$\overline{e_{eq}^2}\,(th) = \frac{16KT(1+\eta_1)}{3\sqrt{2K_P'I_1\left(\frac{W_1}{L_1}\right)}} \left[1 + \frac{K_N'\left(\frac{W_3}{L_3}\right)}{K_P'\left(\frac{W_1}{L_1}\right)}\right]$$

1) Large value of g_{m1}.

2) $\dfrac{L_1}{L_3} < 1$.

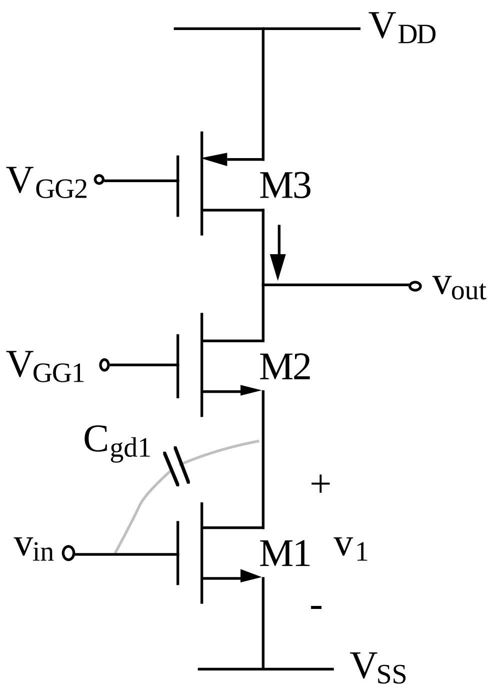
VI.3 - CASCODE AMPLIFIERS

VI.3.1-CMOS CASCODE AMPLIFIERS

Objective

Prevent C_{gd} of the inverter from loading the previous stage. Gives very high gain.

Cascode Amplifier Circuit



Miller effect:

Inverter

$C_{in} \approx$ Gain x C_{gd1}

Cascode

$C_{in} \approx 3C_{gd1}$

$$\left(\frac{v_1}{v_{in}} \approx 2\right)$$

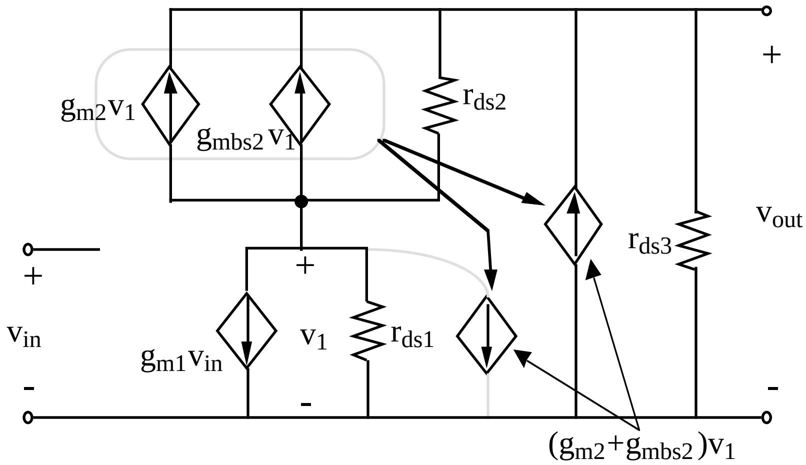
Large Signal Characteristics

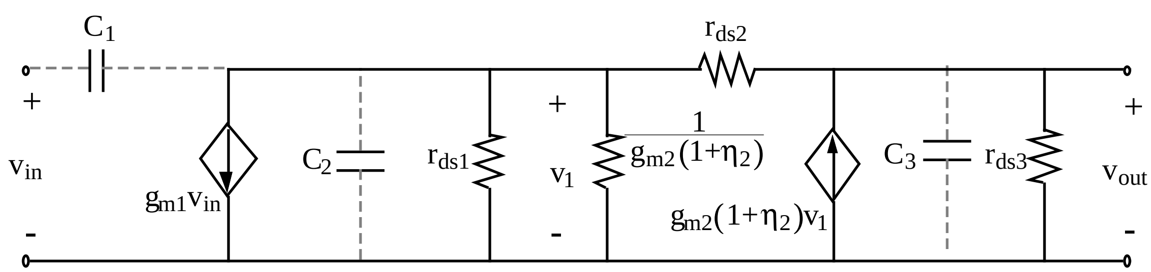
When V_{GG1} designed properly,

$v_{out(min)} = V_{on1} + V_{on2}$

CASCODE AMPLIFIER-CONTINUED

Small Signal Model





Nodal Equations:

$$(g_{m1} - sC_1)v_{in} + (g_{m2} + g_{mbs2} + g_{ds1} + g_{ds2} + sC_1 + sC_2)v_1 - (g_{ds2})v_{out} = 0$$

$$-(g_{ds2} + g_{m2} + g_{mbs2})v_1 + (g_{ds2} + g_{ds3} + sC_3)v_{out} = 0$$

Solving for v_{out}/v_{in} gives

$$\cong \frac{(sC_1 - g_{m1})g_{m2}(1+\eta)}{s^2(C_3C_1+C_3C_2)+s\left[(C_1+C_2)(g_{ds2}+g_{ds3}) + C_3g_{m2}(1+\eta)\right]+g_{ds3}g_{m2}(1+\eta)}$$

Small Signal Characteristics

Low-frequency Gains:

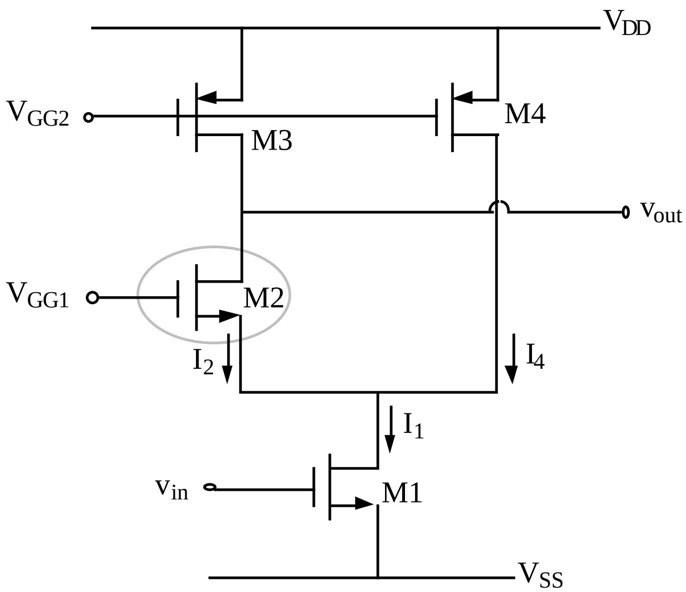
$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}(g_{ds2} + g_{m2} + g_{mbs2})}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{mbs2} + g_{ds1} + g_{ds2})}$$

$$\approx \frac{-g_{m1}}{g_{ds3}} = \frac{\sqrt{2K'(W_1/L_1)I_{D1}}}{\lambda_3 I_{D3}}$$

Also (see next page),

$$\frac{v_1}{v_{in}} = \frac{-2g_{m1}}{g_{m2}(1 + \eta_2)}$$

Gain Enhancement:



$$\frac{v_{out}}{v_{in}} \approx \frac{-g_{m1}}{g_{ds3}}$$

$$\frac{v_{out}}{v_{in}} \approx \frac{\sqrt{\frac{2K'W_1}{L_1}}\sqrt{I_1}}{\lambda I_2}$$

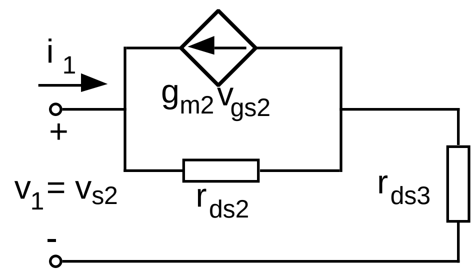
But $I_1 = I_2 + I_4$

$I_4 = 24I_2 \Rightarrow$ x5 Gain enhancement

Voltage Gain of M1:

$$\frac{v_1}{v_{in}} = \frac{-g_{m1}}{g_{m2}} \quad ?$$

What is the small signal resistance looking into the source of M2?
Consider the model below:



$$v_{s2} = (i_1 + g_{m2}v_{gs2})r_{ds2} + i_1r_{ds3} = r_{ds2}i_1 + g_{m2}(-v_{s2})r_{ds2} + i_1r_{ds3}$$

or

$$v_{s2}(1 + g_{m2}r_{ds2}) = i_1(r_{ds2} + r_{ds3})$$

Therefore,

$$R = \frac{v_{s2}}{i_1} = \frac{r_{ds2} + r_{ds3}}{1 + g_{m2}r_{ds2}} \approx \frac{r_{ds2} + r_{ds3}}{g_{m2}r_{ds2}} = \frac{1}{g_{m2}}\left(1 + \frac{r_{ds3}}{r_{ds2}}\right)$$

Some limiting cases:

$$r_{ds3} = 0 \Rightarrow R = \frac{1}{g_{m2}}$$

$$r_{ds3} = r_{ds2} \Rightarrow R = \frac{2}{g_{m2}}$$

and

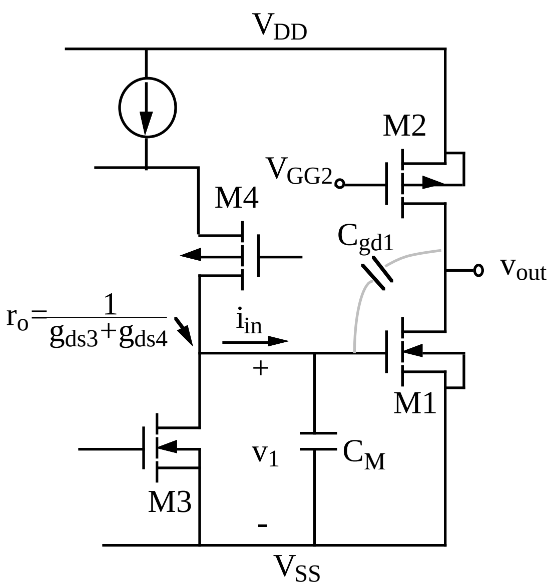
$$r_{ds3} >> r_{ds2} \Rightarrow R = \frac{r_{ds3}}{g_{m2}r_{ds2}}$$

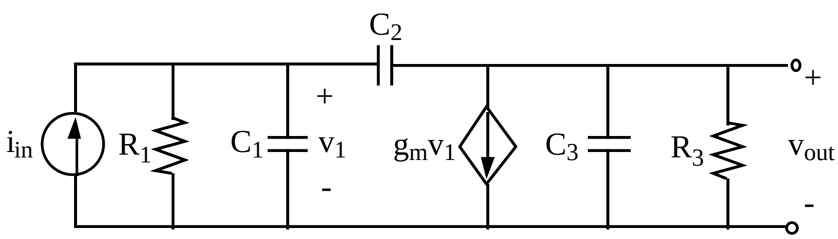
Therefore, the gain v_{in} to v_1 is

$$\frac{v_1}{v_{in}} \approx \frac{-g_{m1}(g_{ds2} + g_{ds3})}{(g_{m2} + g_{mbs2})g_{ds3}} \approx \frac{-2g_{m1}}{g_{m2} + g_{mbs2}} \approx \frac{-2g_{m1}}{g_{m2}}$$

CASCODE AMPLIFIER-CONTINUED

High Resistance Driver for the Inverter M1-M2





$R_1 = (g_{ds3} + g_{ds4})^{-1} \quad R_3 = (g_{ds1} + g_{ds2})^{-1}$

$C_1 = C_{gs1} + C_{bd3} + C_{bd4} + C_{gd3} + C_{gd4}$

$C_2 = C_{gd1} \quad C_3 = C_{bd1} + C_{bd2} + C_{gd2} + C_L$

$$\frac{v_{out}(s)}{i_{in}(s)} = \left(\frac{\left[\frac{-g_{m1}}{G_1G_3}\right]\left[1 - s\left(\frac{g_{m1}}{C_2}\right)\right]}{1 + \left[R_1(C_1+C_3) + R_3(C_2+C_3) + g_{m1}R_1R_3C_2\right]s + (C_1C_2 + C_1C_3 + C_2C_3)R_1R_3s^2} \right)$$

Note:

$$d(s) = 1 + as + bs^2 = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1 p_2}$$

If $|p_2| >> |p_1|$, then

$$d(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2} \quad \text{or} \quad \boxed{p_1 = -\frac{1}{a}} \quad \text{and} \quad \boxed{p_2 = -\frac{a}{b}}$$

Using this technique we get,

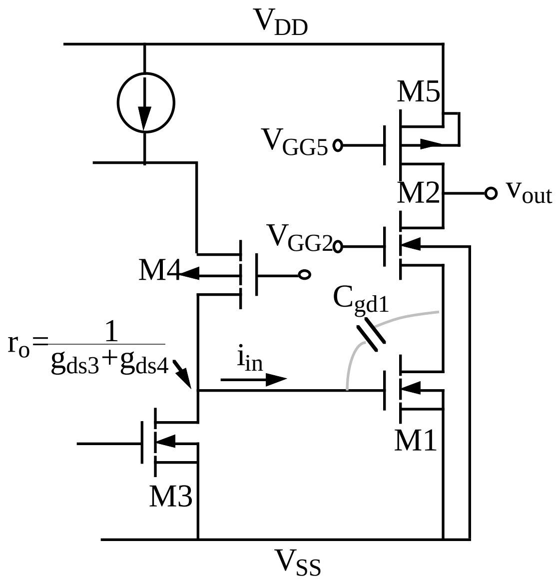
$$p_1 \approx \frac{-1}{R1(C1+C3)+R3(C2+C3)+gm1R1R3C2} \approx \frac{-1}{g_{m1}R_1R_3C_2}$$

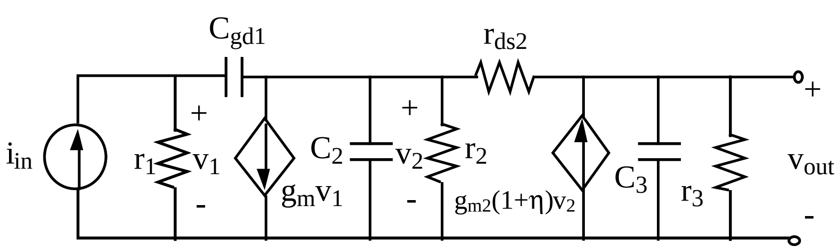
(Miller effect on C_2 causes p_1 to be dominant; $C_M \approx g_{m1}R_2C_{gd1}$)

$$p_2 \approx \frac{-g_{m1}C_2}{C_1C_2+C_1C_3+C_2C_3}$$

CASCODE AMPLIFIER - CONTINUED

How does the Cascode Amplifier solve this problem?





$$r_1 = r_o = (g_{ds3} + g_{ds4})^{-1}$$

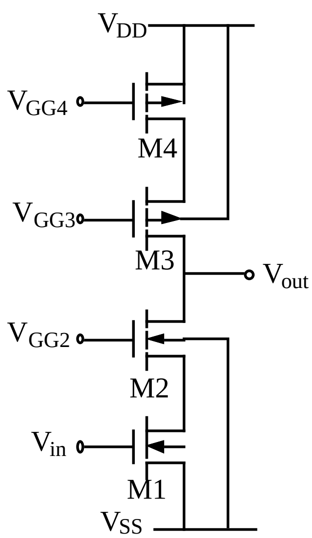
$$C_2 = C_{gs2} + C_{sb2} + C_{db1} + C_{gd1}$$

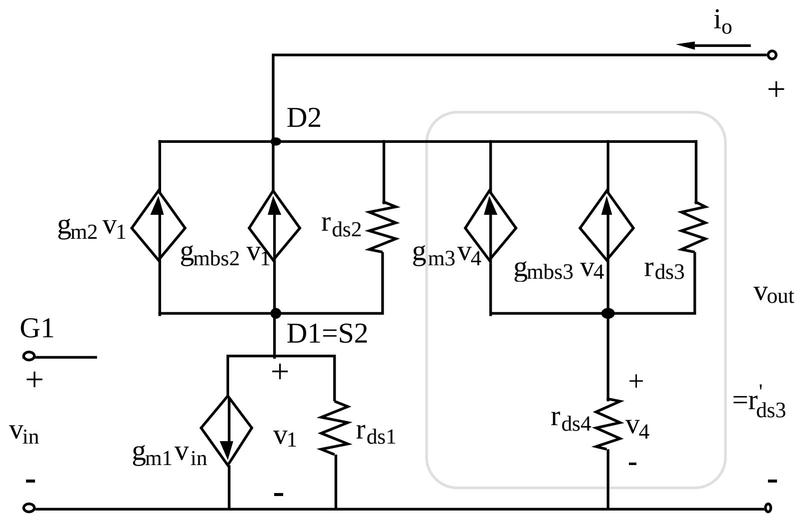
$$r_2 = \left[g_{ds1} + g_{m2}(1+\eta)\right]^{-1} \approx \frac{1}{g_{m2}}$$

$$C_3 = C_{gd2} + C_{db2} + C_{gd5} + C_{db5} + C_L$$

$$r_3 \approx \left(\frac{g_{m2}}{g_{ds1}\, g_{ds2}} + g_{ds5}\right)^{-1} \approx \frac{1}{g_{ds5}}$$

Cascode amplifier with higher gain and output resistance





VI.4 - OUTPUT AMPLIFIERS

Requirements

1. Provide sufficient output power in the form of voltage or current.

2. Avoid signal distortion for large signal swings.

3. Be efficient.

4. Provide protection from abnormal conditions.

Types of Output Stages

1. Class A amplifier.

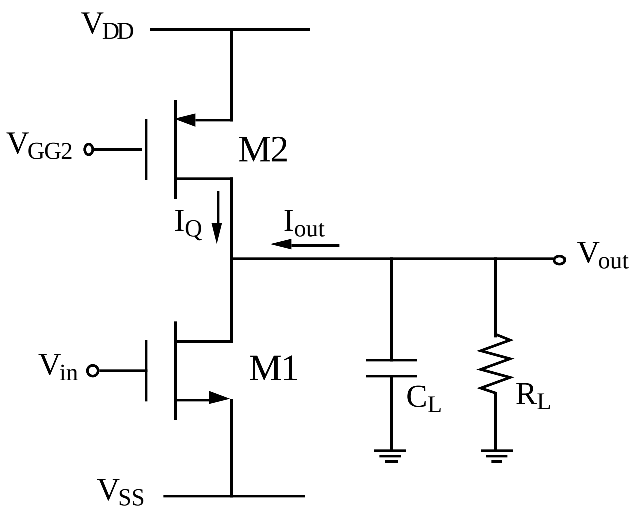
2. Source follower.

3. Push-Pull amplifier (inverting and follower).

4. Substrate BJT.

5. Negative feedback (OP amp and resistive).

CLASS A AMPLIFIER



$$I_{out}^{+} = \frac{KnW_1}{2L_1}(V_{DD} - V_{SS} - V_{T1})^2 - I_Q$$

$$I_{out}^{-} = \frac{KpW_2}{2L_2}(V_{DD} - V_{GG2} - |V_{T2}|)^2 < I_{out}^{+}$$

$|I_{out}|$ determined by:

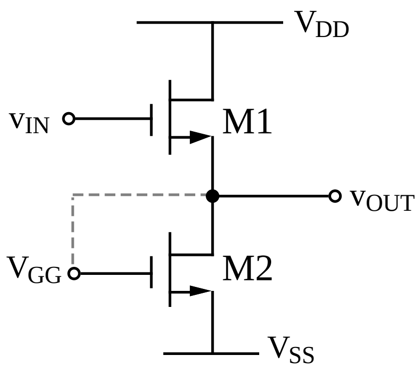
1. $|I_{out}| = C_L \dfrac{dv_{out}}{dt} = C_L$ (slew rate)
2. $|I_{out}| = \dfrac{v_{out}(peak)}{R_L}$

$$\text{Efficiency} = \frac{P_{RL}}{P_{supply}} = \left(\frac{V_{out}(peak)}{(V_{DD} + V_{SS})}\right)^2 \leq 25\%$$

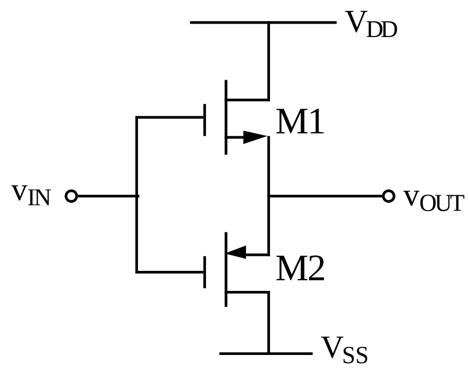
$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}} = \frac{1}{2\lambda I_D} \qquad \text{(typically large)}$$

SOURCE FOLLOWER

N-Channel



Push Pull



Large Signal Characteristics

$v_{OUT} = v_{IN} - v_{GS1}$

Maximum Output Swing Limits

$v_{OUT}(MAX) = V_{DD} - V_{T1}$
(V_{T1} greater than V_{T0} because of v_{BS})

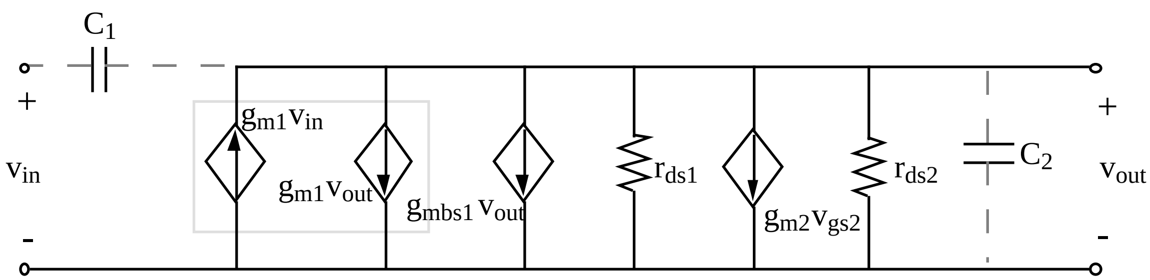
Single Channel Follower:
$v_{OUT}(MIN) = V_{SS}$

Push Pull Follower:
$v_{OUT}(MIN) = V_{SS} + |V_{T2}|$
(V_{T2} greater than V_{T0} because of v_{BS})

SOURCE FOLLOWERS

<u>Small Signal Characteristics</u>

Single Channel Follower (Current source and active load):



Small Signal Voltage Transfer Function:

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{ds1}+g_{ds2}+g_{m1}+g_{mbs1}+g_{m2}} \quad \text{where } g_{m2} = 0 \text{ if } v_{GS2} = V_{GG}$$

Example:

If $V_{DD} = -V_{SS} = 5V$, $v_{OUT} = 0V$, $i_D = 100\mu A$, and $\frac{W}{L} = \frac{10\ \mu m}{10\ \mu m}$,

then;

$$\frac{v_{out}}{v_{in}} = \frac{41.23}{1+1+41.23(1+0.2723)+41.23} = 0.4309 \text{ when } v_{GS2} = v_{OUT}$$

$$\frac{v_{out}}{v_{in}} = \frac{41.23}{1+1+41.23(1+0.2723)} = 0.751 \text{ when } v_{GS2} = V_{GG}$$

Approximation gives $\frac{vout}{v_{in}} \approx 0.786 \quad (g_{ds1} = g_{ds2} \approx 0)$

Output Resistance:

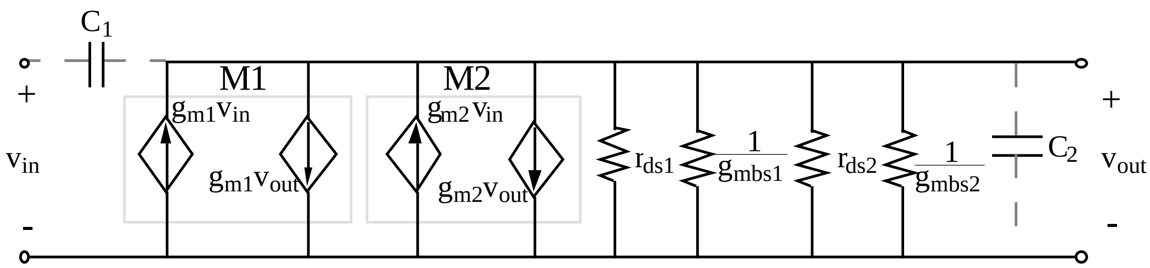
$$r_{out} = \frac{1}{g_{ds1}+g_{ds2}+g_{m1}+g_{mbs1}+g_{m2}} \quad \text{where } g_{m2} = 0 \text{ if } v_{GS2} = V_{GG}$$

$r_{out} = 10.5\ K\Omega$ ($v_{GS2} = v_{OUT}$) and $r_{out} = 18.4\ K\Omega$ ($v_{GS2} = V_{GG}$)

SOURCE FOLLOWERS

Push Pull Source Follower

Model:



Small Signal Voltage Transfer Function:

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_{m2} + g_{mbs2}}$$

Example:

If $V_{DD} = -V_{SS} = 5\text{V}$, $v_{OUT} = 0\text{V}$, $i_D = 100\mu\text{A}$, and $\frac{W}{L} = \frac{10\mu\text{m}}{10\mu\text{m}}$

then,

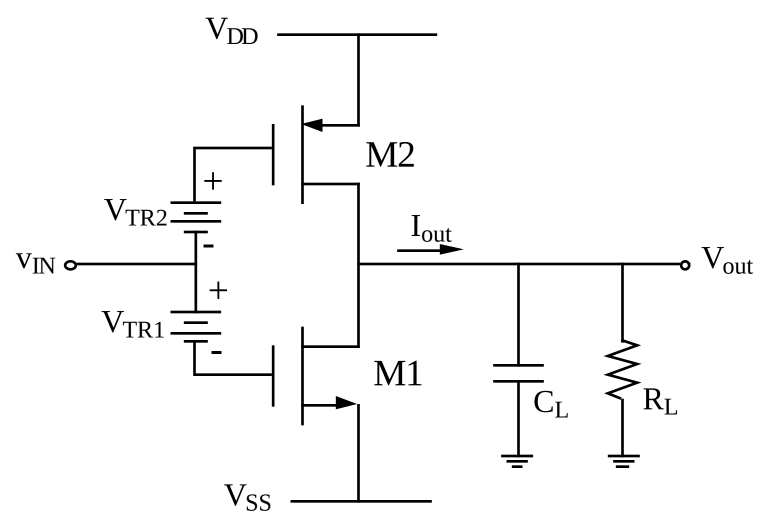
$$\frac{v_{out}}{v_{in}} = \frac{41.23 + 28.28}{1 + 0.5 + 41.23(1 + 0.2723) + 28.28(1 + 0.1268)} = 0.81$$

Output Resistance:

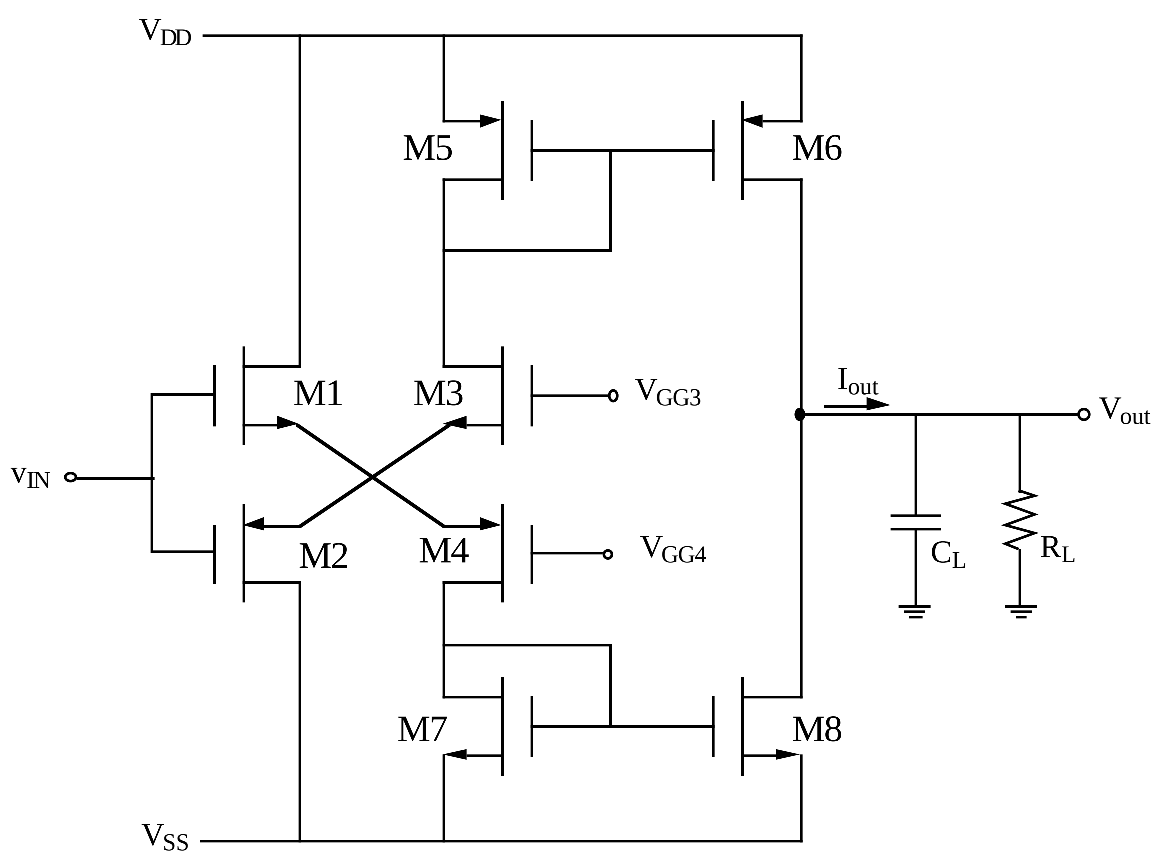
$$r_{out} = \frac{1}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_{m2} + g_{mbs2}} = 11.7\text{K}\Omega$$

PUSH-PULL INVERTERING CMOS AMPLIFIER

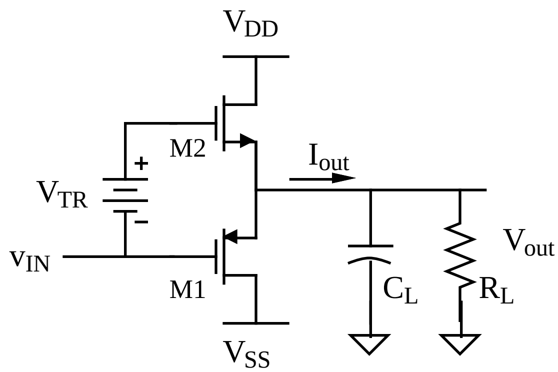
Concept-

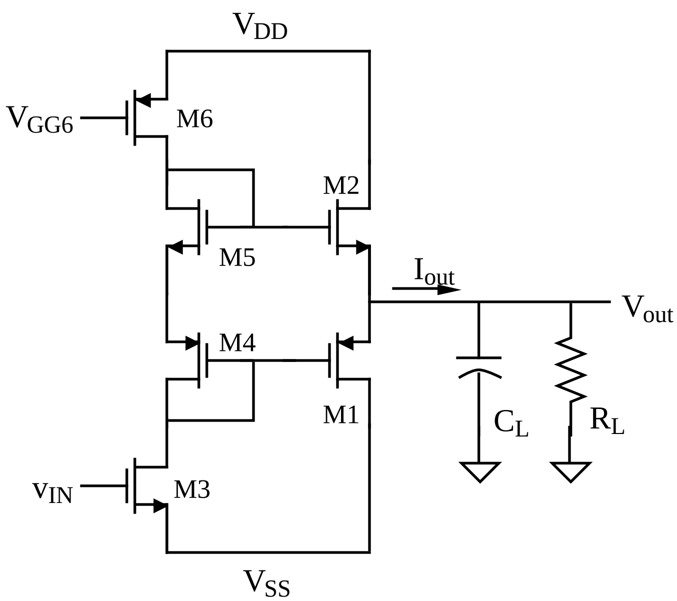


Implementation-

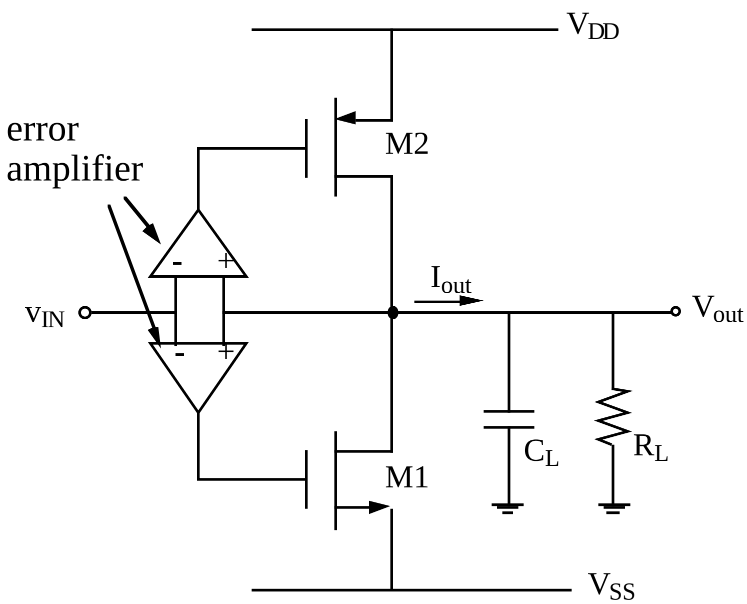


PUSH-PULL SOURCE FOLLOWER

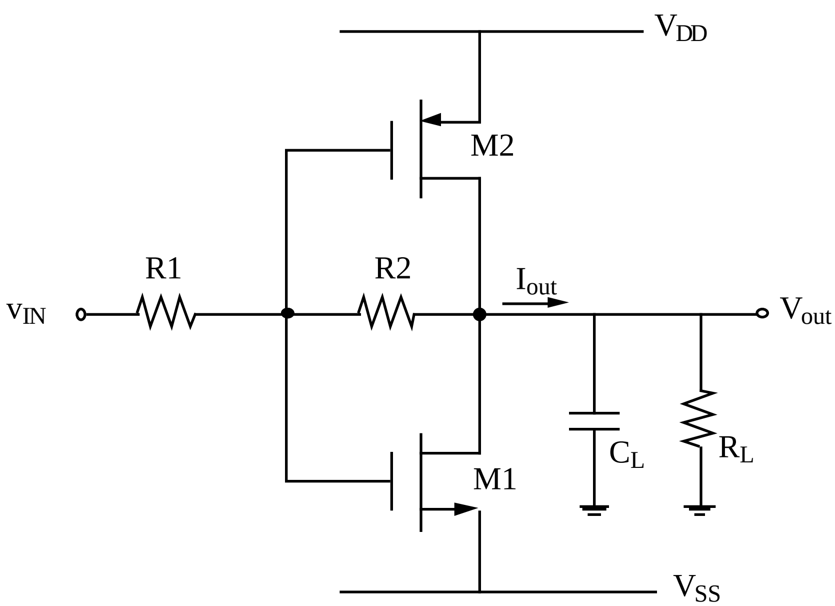




USE OF NEGATIVE FEEDBACK TO REDUCE ROUT



Use of negative feedback to reduce the output resistance of Fig. 6.3-4.



Use of resistive feedback to decrease the output resistance of Fig.6.3-4.

VI.5 - SUMMARY

- Analog Amplifier Building Blocks

  Inverters - Class A
  Push-Pull - Class AB or B
  Cascode - Increased bandwidth
  Differential - Common mode rejection, good input stage
  Output - Low output resistance with minimum distortion