

Design of analog integrated circuits part 1: Operational Amplifiers

Note: some figures were taken from references:

1.- *B. Razavi, Design of Analog CMOS Integrated Circuits, Mc Graw-Hill, 2001*

2.- *R. J. Baker et al., CMOS Circuit Design, Layout and Simulation, Wiley Interscience, 1st Edition, 1998.*

An overview of opamps

General purpose operational amplifiers

High voltage gain

High input impedance

Low output impedance

Tradeoffs of Opamps for Specific Application

Voltage gain

Input impedance

Output impedance

Speed

Noise

Output swing

Power dissipation

Typical structure of an OPAMP

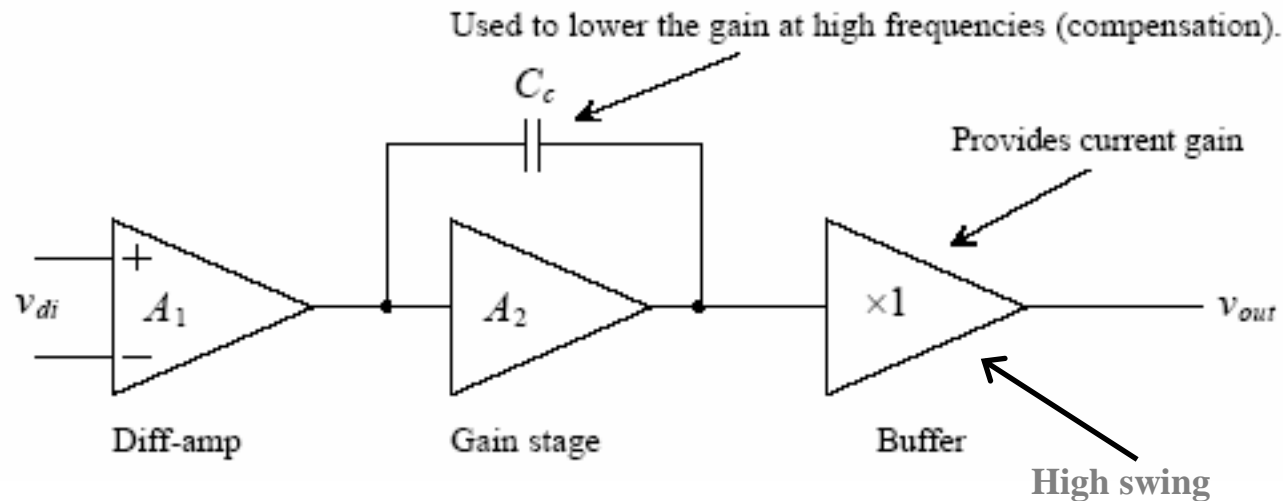


Fig.1: Block diagram of two stage Opamp

If the opamp is intended to drive small capacitive loads the output buffer is not used.

If the opamp is used to drive resistive or large capacitive loads then the output buffer is used.

Example of CMOS OPAMP

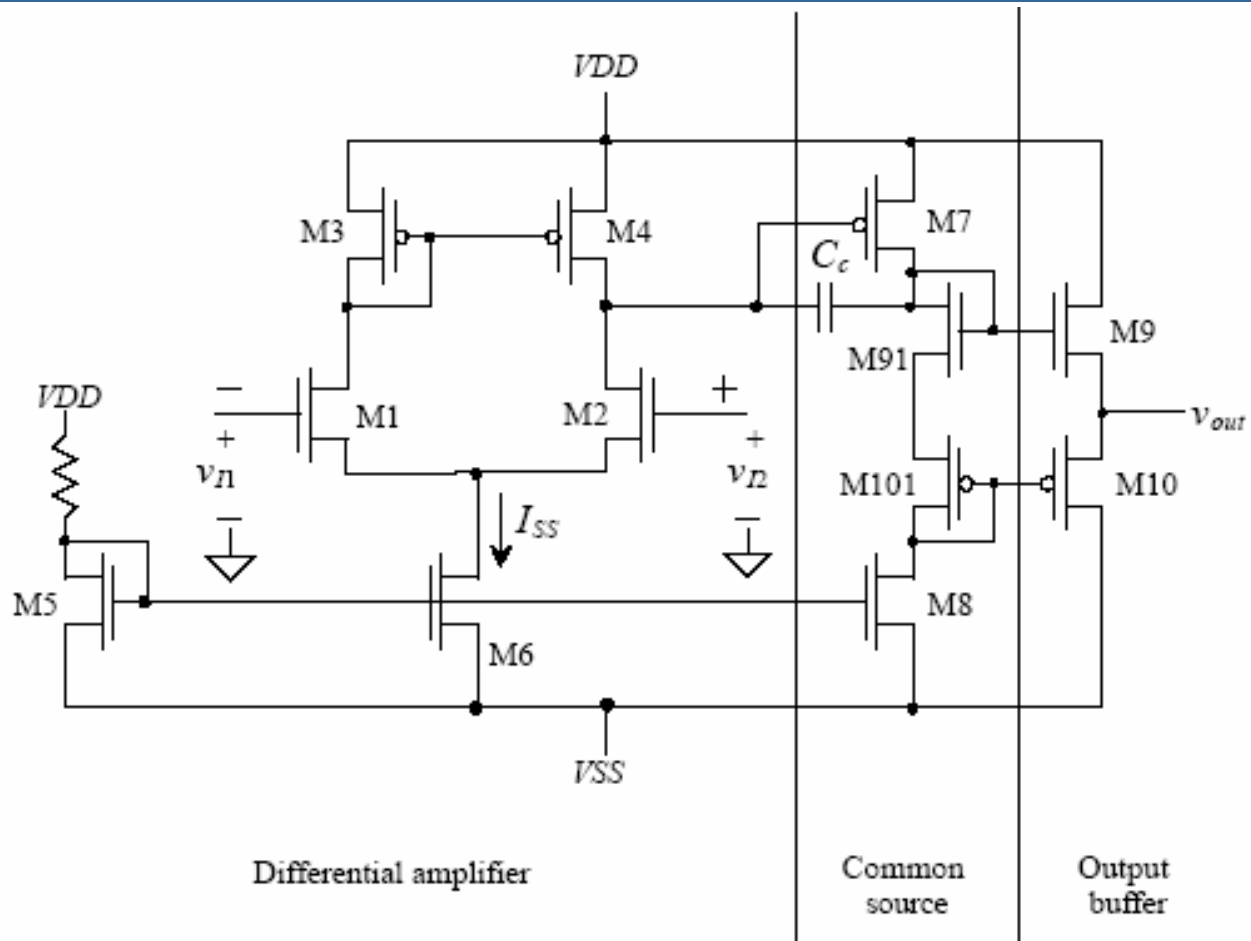


Fig.2: Example of Operational Amplifier with output buffer

Back to basics: Basic Differential Amplifier

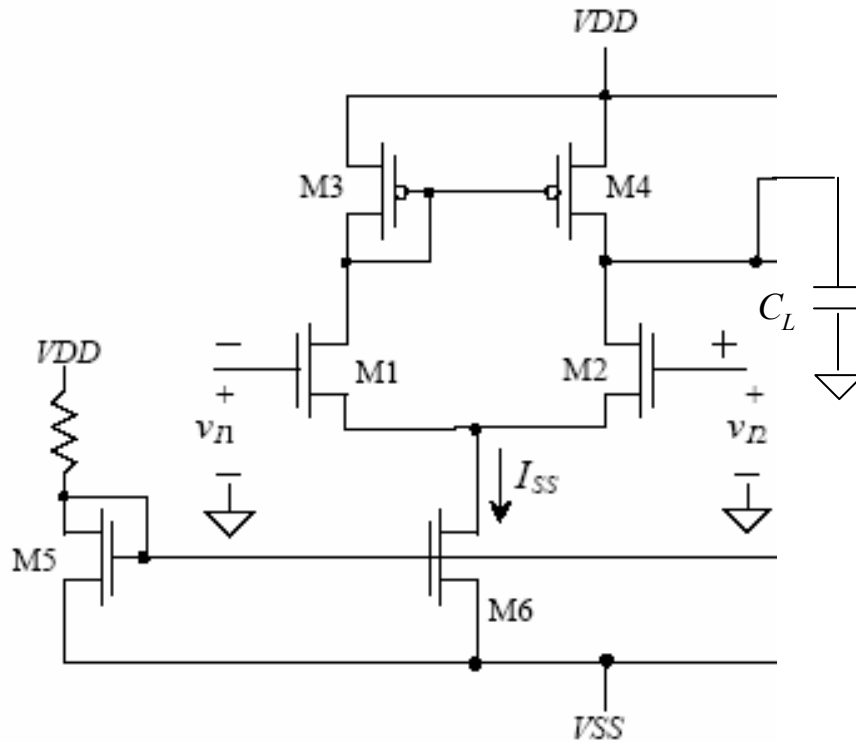


Fig.3 Differential amplifier

$$A_{v_dm} = g_{m1,2} [(r_{O2}) // (r_{O4})]$$

$$\begin{aligned} V_{in_CM_min} &= V_{GS1,2} + V_{DS6} \\ &= V_{GS1,2} + V_{GS6} - V_{THN} \end{aligned}$$

$$V_{in_CM_max} = V_{DD} - V_{SG3,4} + V_{THN}$$

$$SR = dV_O/dt = I_{SS}/C_L$$

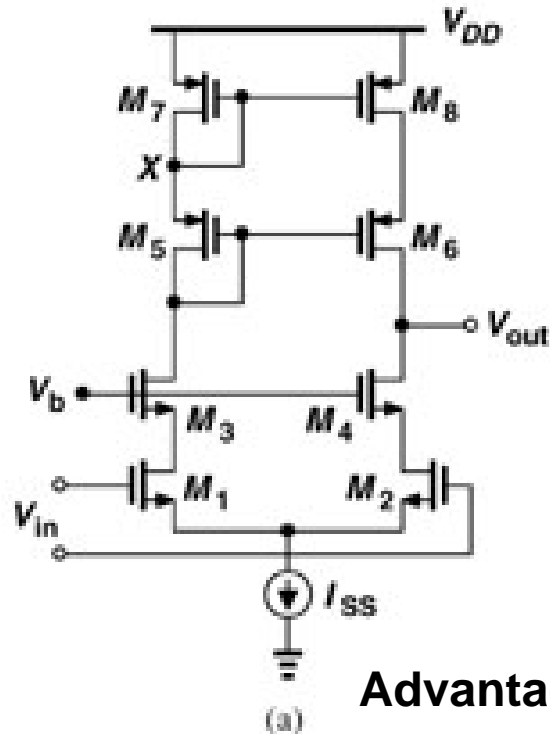
$$f_h = 1 / [2\pi(r_{O2} // r_{O4})C_{Tot}]$$

$$\text{with } C_{Tot} = C_L + C_{db4} + C_{gd4} + C_{db2} + C_{gd2}$$

$$A_{v_cm} = -1 / (2g_{m4}r_{O6})$$

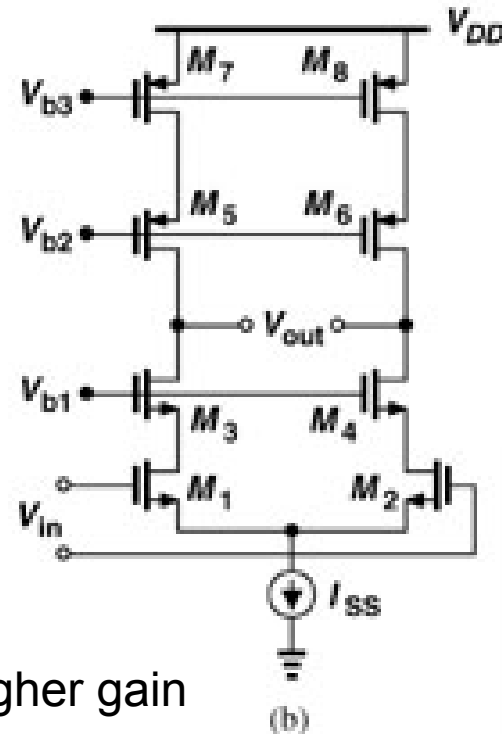
$$CMRR = 20 \log \left| \frac{g_{m1}r_{O2} // r_{O4}}{2g_{m4}r_{O6}} \right|$$

Back to basics: boosting diff. gain with Cascode

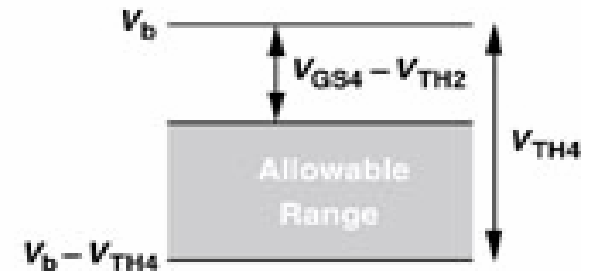


Advantage: higher gain

$$A_v = g_{mN} [(g_{mN} r_{ON}^2) / (g_{mP} r_{OP}^2)]$$



Drawbacks: cascode suffers of low output swing. Difficulty in shorting input and output, e.g. to implement a unity-gain buffer.



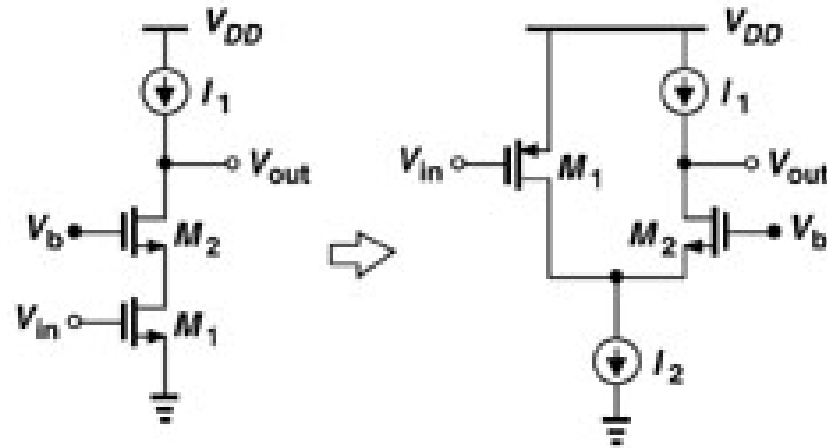
The V_O range can be maximized minimizing V_{OD4} but always less than V_{TH2} .

$$\text{Output Swing: } V_O = 2[V_{DD} - (V_{OD1} + V_{OD3} + V_{OD_{CS}} + V_{OD5} + V_{OD7})]$$

$$\text{Input Common Mode Range } V_{in\ CM\ min} = V_{GS1} + V_{GS_{CS}}$$

Back to basics: boosting output swing with folded Cascode

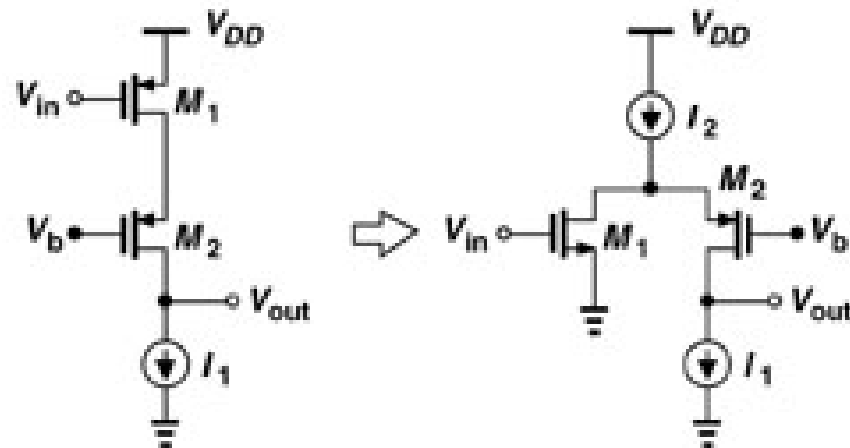
Advantages: it allows to short input and output with negligible swing limitation.



(a)

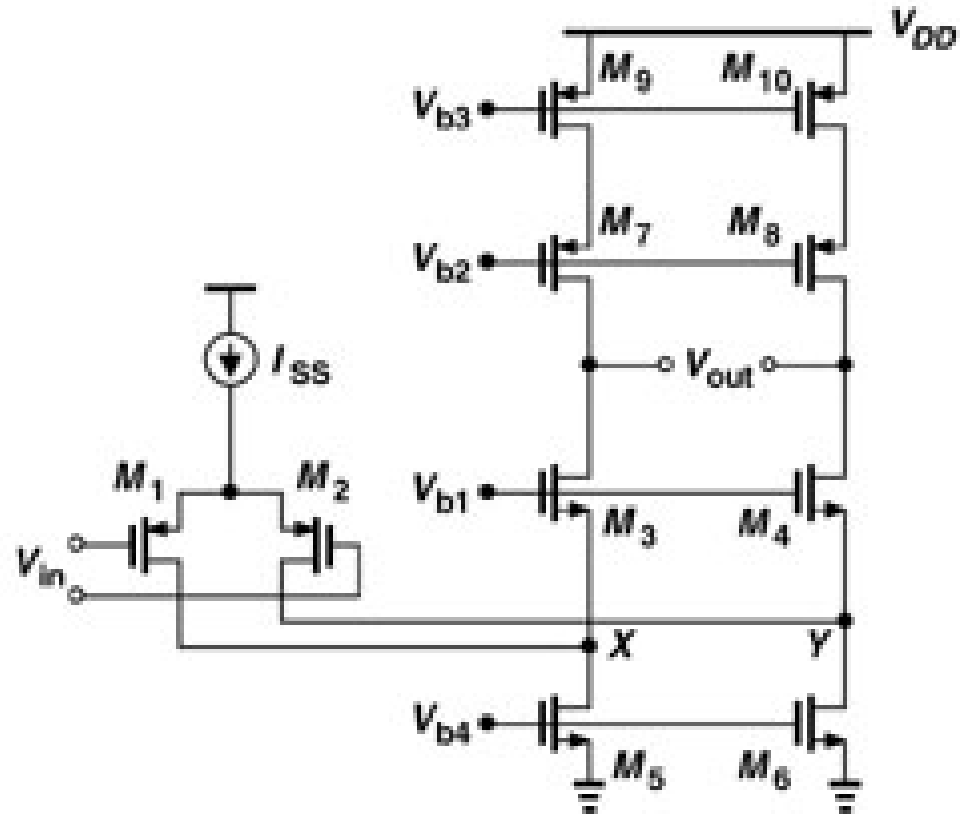
Disadvantages:

Generally folded cascode consumes higher power.



(b)

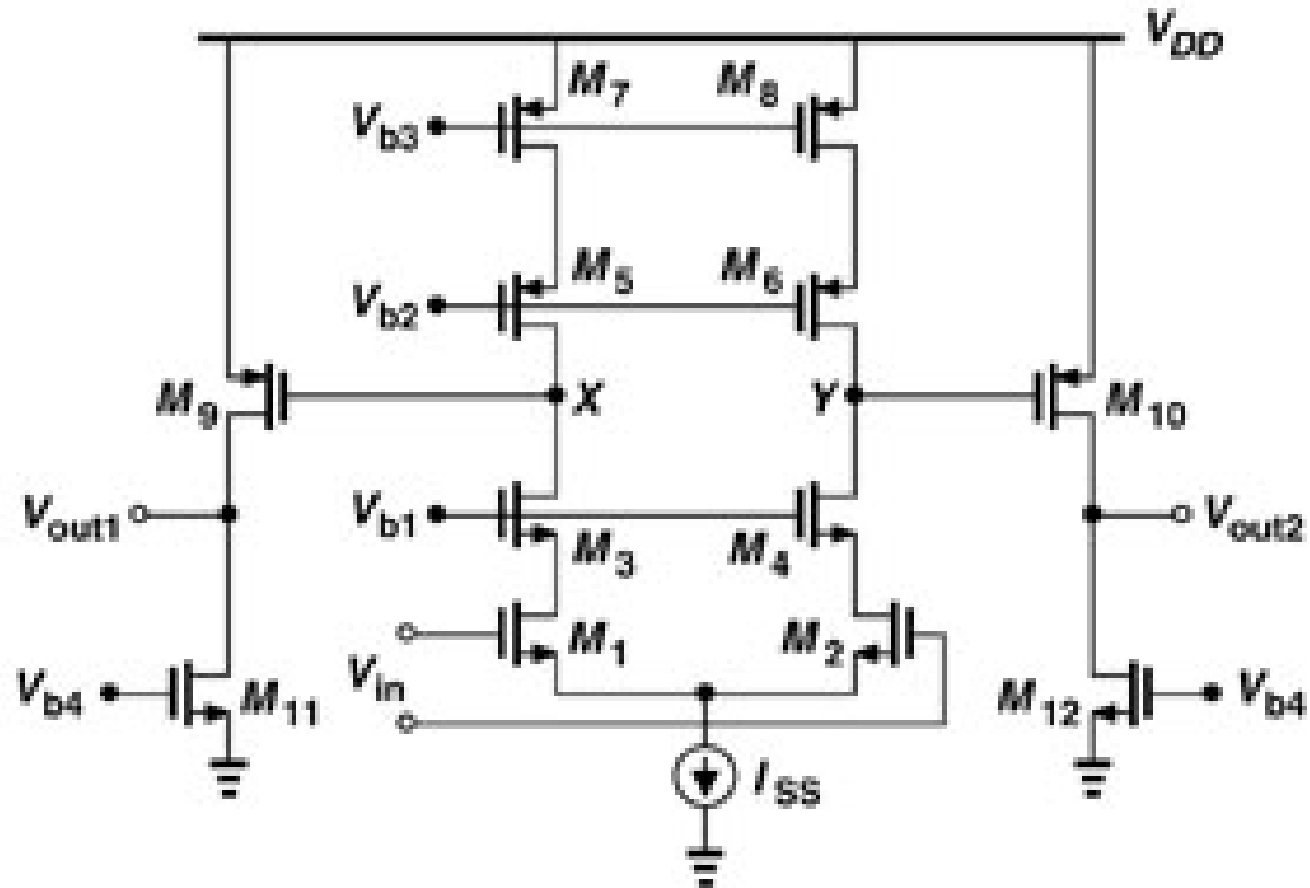
Improved Diff. Amplifier stage



Output swing at each side: $V_{O1,2} = V_{DD} - (V_{OD3} + V_{OD5} + |V_{OD7}| + |V_{OD9}|)$

Voltage Gain: $A_v = g_{m1} \left\{ \frac{[(g_{m3} + g_{mb3})r_{O3}(r_{O1} // r_{O5})]}{[(g_{m7} + g_{mb7})r_{O7}r_{O9}]} \right\}$

Two stage OpAmp employing cascode



Design Considerations of an OPAMP

Design procedure consist in:

- **Device sizes and biasing conditions,**
- **Compensation the opamp for stability,**
- **Simulating and characterizing the opamp:**

Open-Loop gain; A_{OL}

input common mode range; V_{in_CM}

common mode rejection ratio; $CMRR$

output voltage swing; V_O

power supply rejection ratio; $PSRR$

current source/sinking capability; I_{SS}

power dissipation; P_D

Example of CMOS OPAMP design 1

1st step: Device Sizes

(a) selection of I_{SS} *of first stage*; this is an iterative process, we select a value of I_{SS} and verify that the characteristics of “ A_{OL} , V_{in_CM} , $CMRR$, power dissipation, noise, matching considerations, and SR “ are met.

(b): selection of V_{GS} ; in general, the larger (increasing W while holding L constant) we make the MOSFET in the differential stage at a given I_{SS} , the lower V_{GS} :

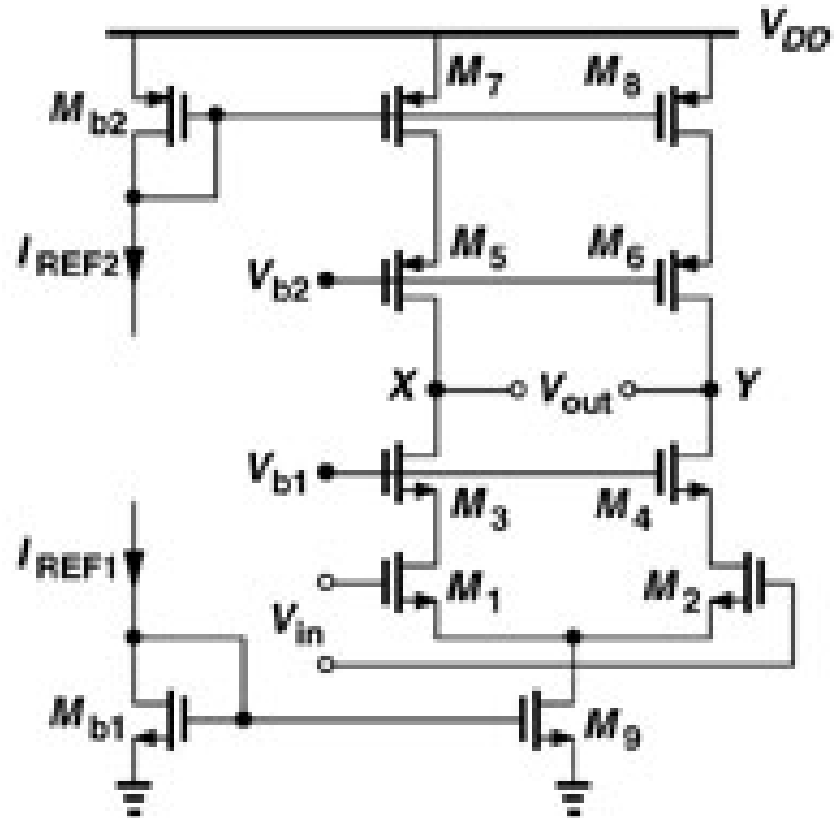
Advantages: V_{in_CM} is increased, the noise is lowered, and matching is better (i.e. offset is reduced),

Disadvantages: layout area is increased, and parasitic capacitances, and thus lower speed.

Example: design of Cascode diff. stage

Exercise 1: design a fully differential cascode diff. amplifier (see figure at side) with the following specifications: $V_{DD} = 3V$, differential output swing = $3V$, power dissipation = $10mW$, and Voltage gain = 2000 . Assume $L = 0.5\mu m$, $\mu_n C_{ox} = 60mA/V^2$, $\mu_p C_{ox} = 30mA/V^2$, $\lambda_n = 0.1V^{-1}$, $\lambda_p = 0.2V^{-1}$, $\gamma = 0$, $V_{THN} = 0.7V$, $V_{THP} = -0.7V$

To be solved in the classroom



Example of CMOS OPAMP design 2

(c): selection the **size devices** of the **2nd stage and output stage**;

The same considerations that applied to selection of diff. amp I_{SS} apply to the selection of I_{SS} for the 2nd stage.

Notice that with both inputs of the opamp (i.e. Gates of M1 and M2 in Fig. 3) at the same potential, the same current flows in M3 and M4. The result is that the Drain of M4 is at the same potential as its Gate. Therefore, if we want to set $I_{M7} = I_{M4}$, we must use the same size for M7 and M4. But if we want to set $I_{M7} = \frac{1}{2} I_{M4}$, then size of M7 is $\frac{1}{2}$ of size of M4.

On the other hand, $I_{M8} = I_{M7}$, then we size M8 to drive this current.

Note: the following steps of design procedure are based on basic two stage opamp (Fig.2)

Example of CMOS OPAMP design 3

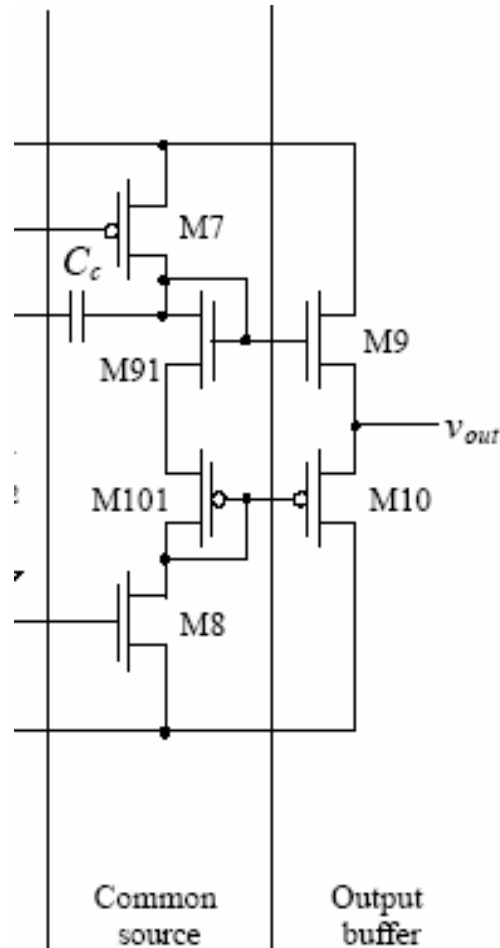


Fig.4: 2nd and output stage of opamp

Voltage Gain of 2nd stage (C-S Amplifier):

$$A_2 = -g_{m7}(r_{O7} // r_{O8})$$

Voltage Gain of the opamp:

$$A_1 A_2 = [g_{m1}(r_{O2} // r_{O4})] [-g_{m7}(r_{O7} // r_{O8})]$$

The output stage is a Class AB amplifier:

M91 and M101 are used to bias the source-followers buffers M9 and M10 (see Fig.4).

Notice that for a given $V_{GS9,10}$ the maximum and minimum current we can source will be respectively:

$$I_{O_max} = \frac{\beta_9}{2} (V_{GS9} - V_{THN})^2 \quad I_{O_min} = \frac{\beta_{10}}{2} (V_{GS10} - V_{THP})^2$$

The size of M9 and M10 are defined by I_{out_max} and I_{out_min} respectively.

Example of CMOS OPAMP design 4

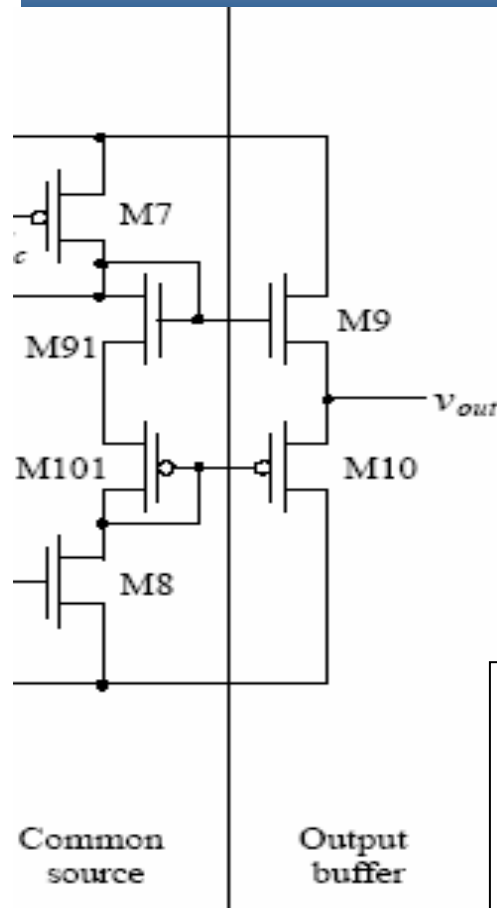


Fig.5: output stage of opamp

The output swing is given by:

$$V_{out_max} = V_{DD} - V_{GS9}$$

$$V_{out_min} = V_{SS} + V_{GS10}$$

The dissipated power at output stage is :

$$P_D = V_{DD} I_O$$

The P_D in the opamp is the product of the sum of the currents flowing in the current sources with the power supply voltages

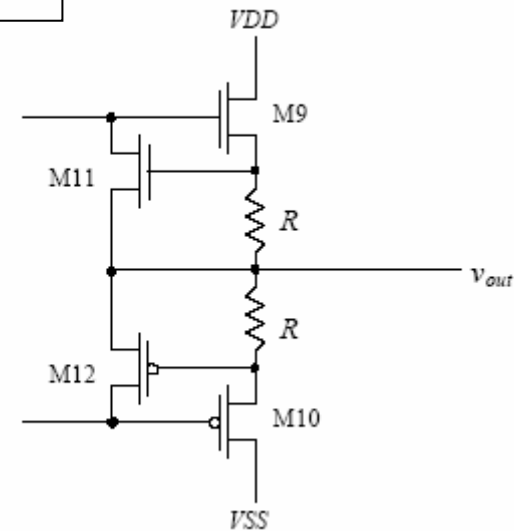


Fig.6 Short-circuit protection circuit, with $R = V_{TH}/I_O$

If dissipated power is large enough, the runaway drawback will be present and a short-circuit protection must be added (see Fig.6) to the output stage in order to reduce $V_{GS9,10}$ variations.

Example of CMOS OPAMP design 5

2nd step, Compensating the opamp:

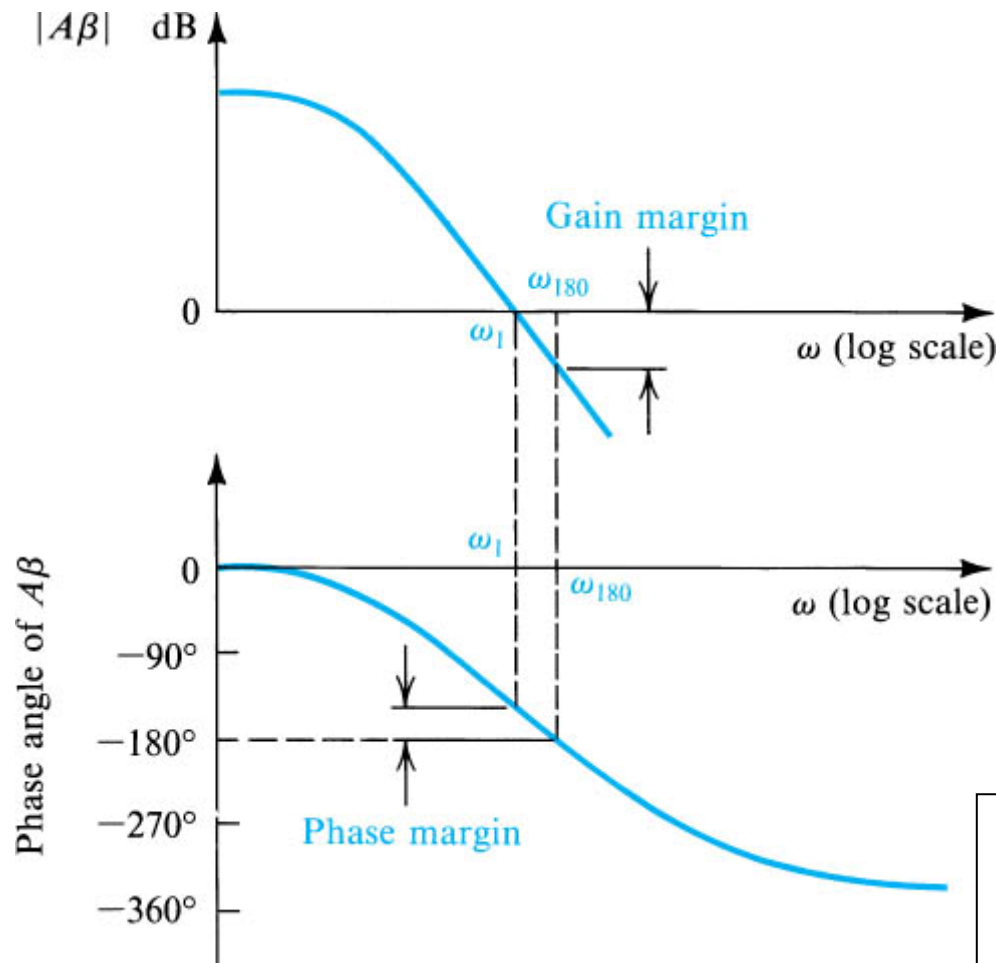


Fig.7: stability criterion

For a feedback amplifier:

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta}$$

unstable _ when : $A_{OL}\beta = -1$

$$|A_{OL}\beta| = 1, \text{ for } \angle A_{OL}\beta = \pm 180^\circ$$

To ensure stability

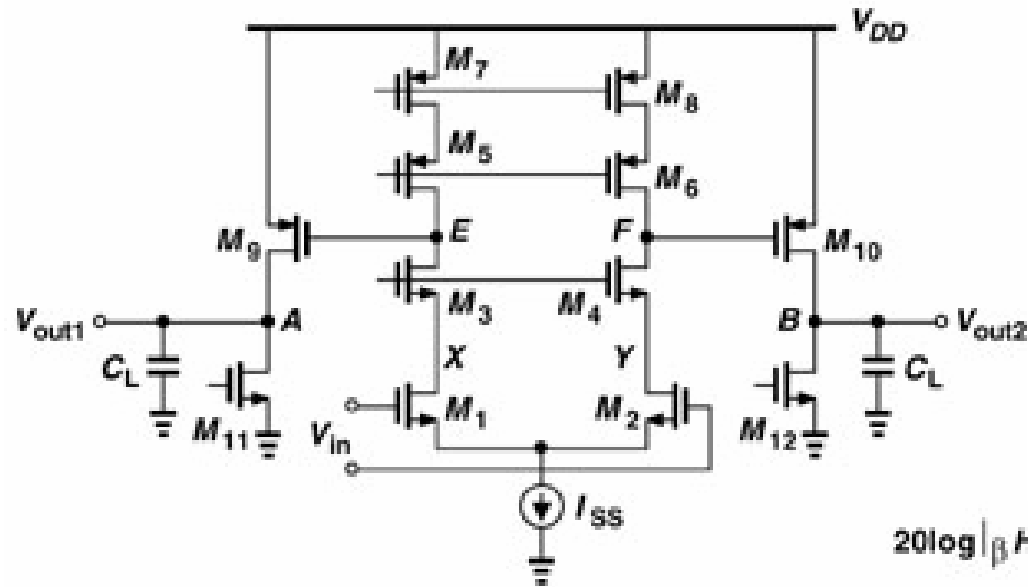
$$|A_{OL}\beta| = 1$$

Must drop to unity before

$$\angle A_{OL}\beta = -180^\circ$$

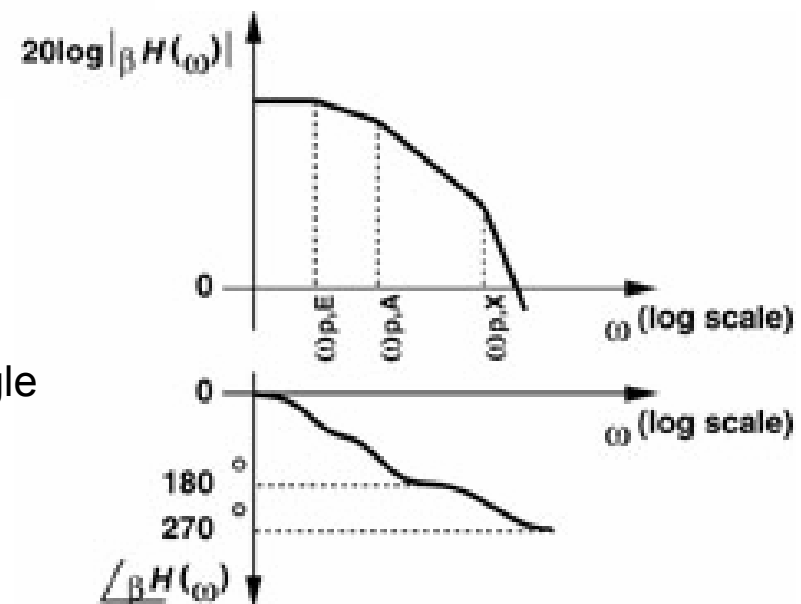
The open-loop transfer function must be modified such that the closed-loop circuit is stable and the time response is well-behaved.

Frequency response of two stage Opamp

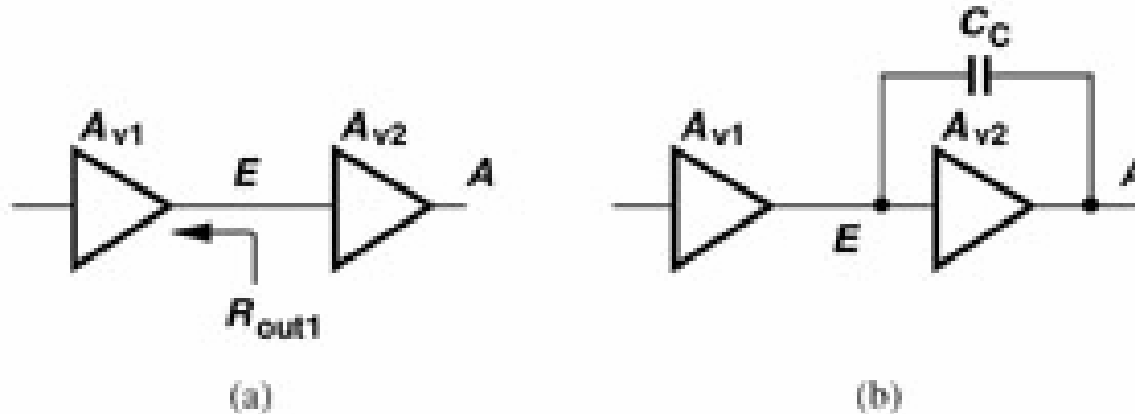


The circuit exhibits two dominant poles at nodes E and A.

Note that, since the poles at E and A are relatively close to the origin, the phase angle approaches -180° well below the pole at X. “the PM may be quite close to zero even before the pole at X contributes significant phase shift”.



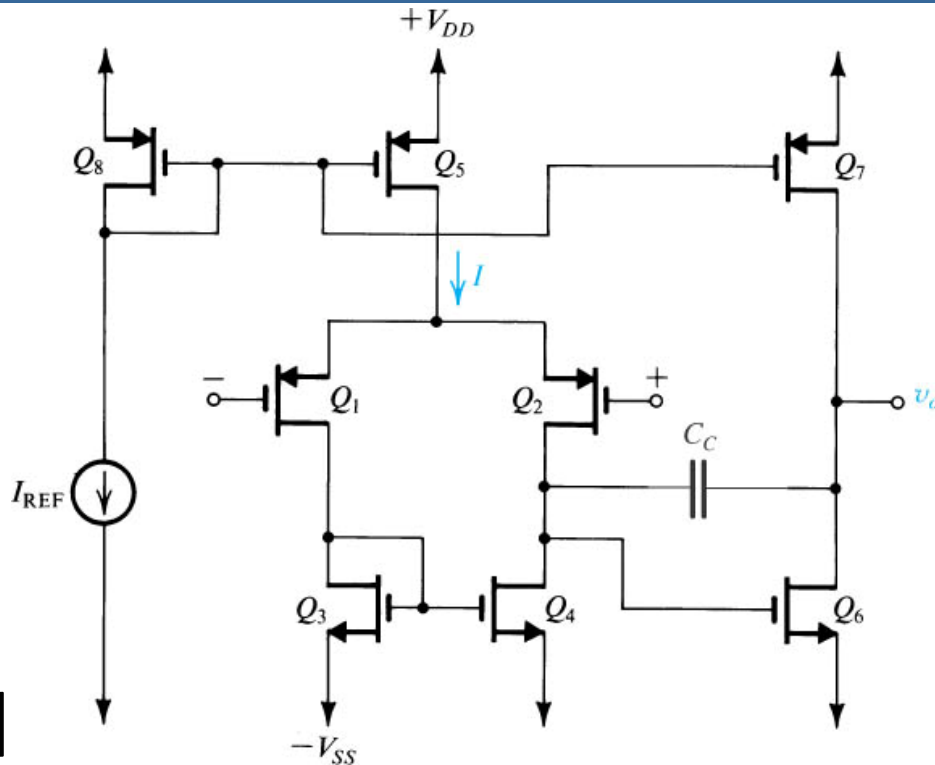
Frequency compensation of two stage Opamp



Notice that the 1st stage exhibits a high R_o and the 2nd stage provides moderate gain, thereby providing a suitable environment for Miller multiplication of capacitors:

“the idea is to create a large capacitance at node $E = (1 + A_{V2})C_C$ ”
moving the corresponding pole at lower frequency $\omega_{pE} = 1/\{R_o[C_E + C_C(1+A_{V2})]\}$, where C_E denotes the capacitance before C_C is added.

Frequency response of two stage Opamp



$$G_{m1} = g_{m1} = g_{m2}$$

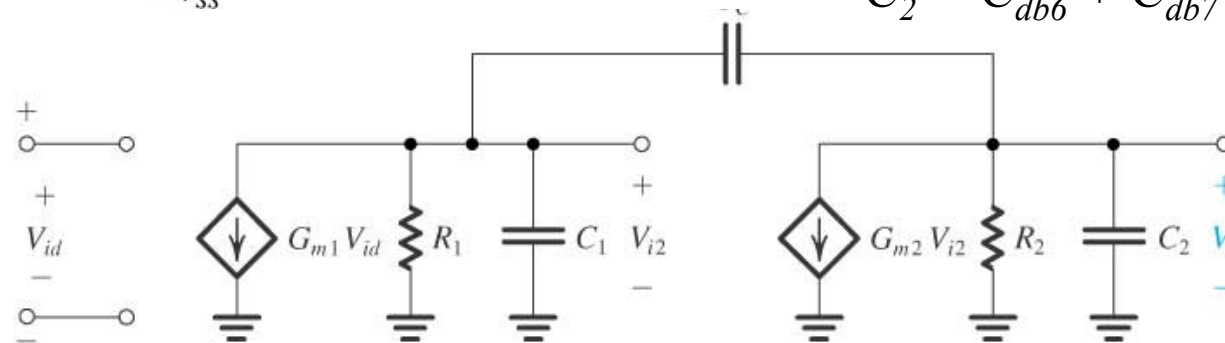
$$G_{m2} = g_{m6}$$

$$R_1 = r_{O1} // r_{O2}$$

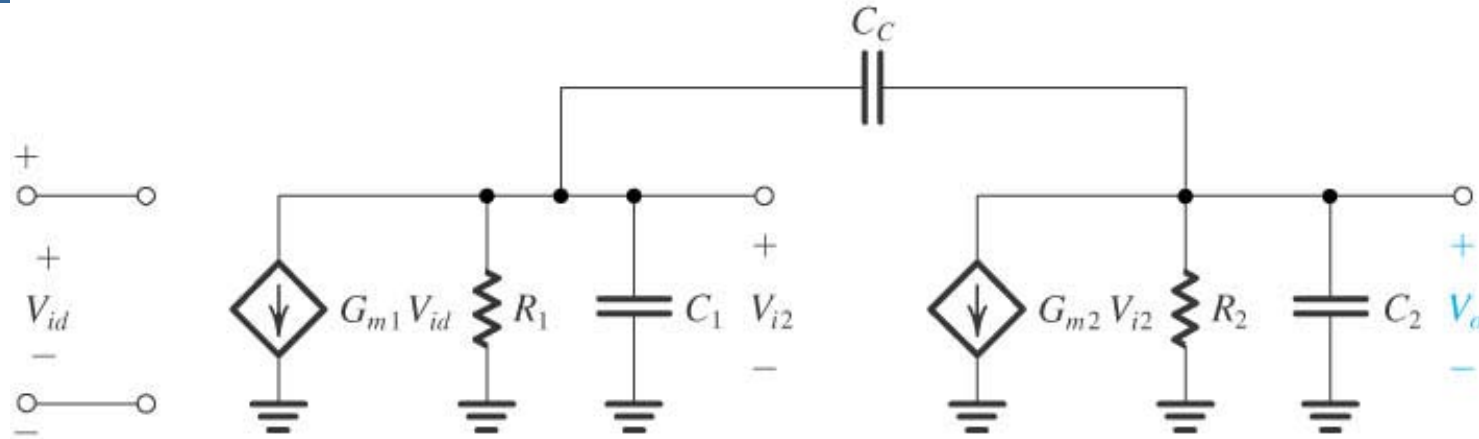
$$R_2 = r_{O6} // r_{O7}$$

$$C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6}$$

$$C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L$$



Frequency response of two stage Opamp



$$G_{m1} = g_{m1} = g_{m2}$$

$$G_{m2} = g_{m6}$$

$$R_1 = r_{O1} // r_{O2}$$

$$R_2 = r_{O6} // r_{O7}$$

$$C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6}$$

$$C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L$$

$$f_{p1} = 1/(2\pi R_1 G_{m2} R_2 C_c)$$

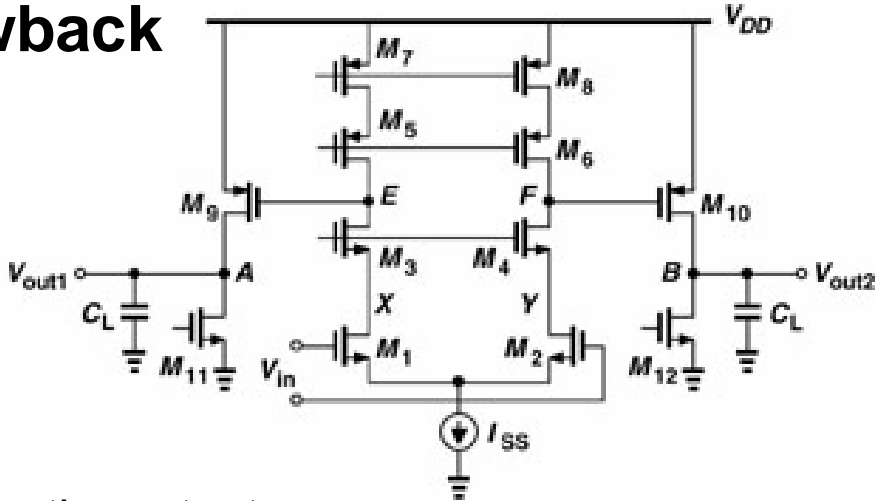
$$f_{p2} = G_{m2} / (2\pi C_2)$$

$$f_T = G_{m1} / (2\pi C_c)$$

$$f_Z = G_{m2} / (2\pi C_c)$$

Frequency response of two stage Opamp

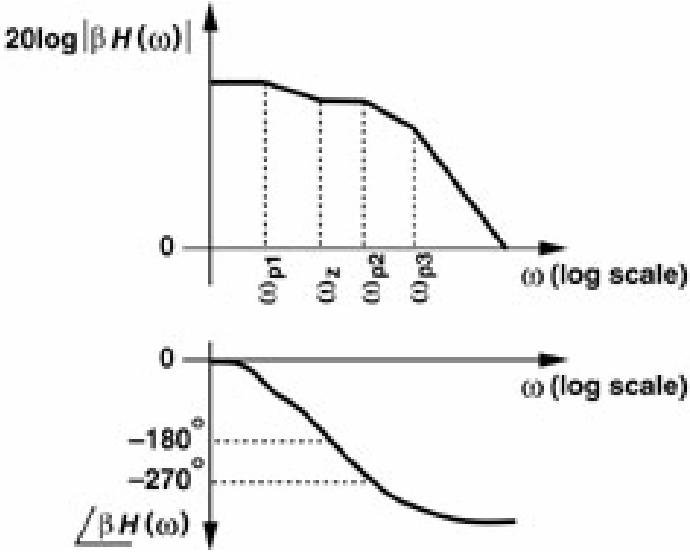
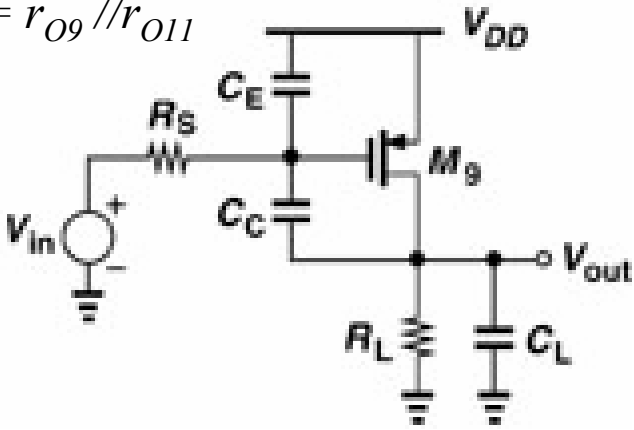
drawback



The zero is moved at lower frequency: $\omega_z = g_{m9} / (C_C + C_{gd9})$

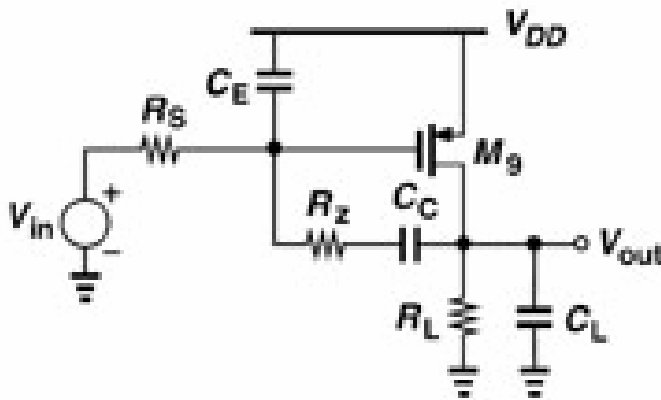
and the pole $\omega_{p2} = g_{m9} / (C_E + C_L)$

R_S denotes the output resistance of the 1st stage and, $R_L = r_{O9} // r_{O11}$



Frequency compensation of two stage Opamp

One **solution** consist in place a resistor R_z in series with C_C .



$$\omega_z = \frac{1}{C_C (1/g_{m9} - R_z)}$$

Notice that we can make $R_z = 1/g_{m9}$

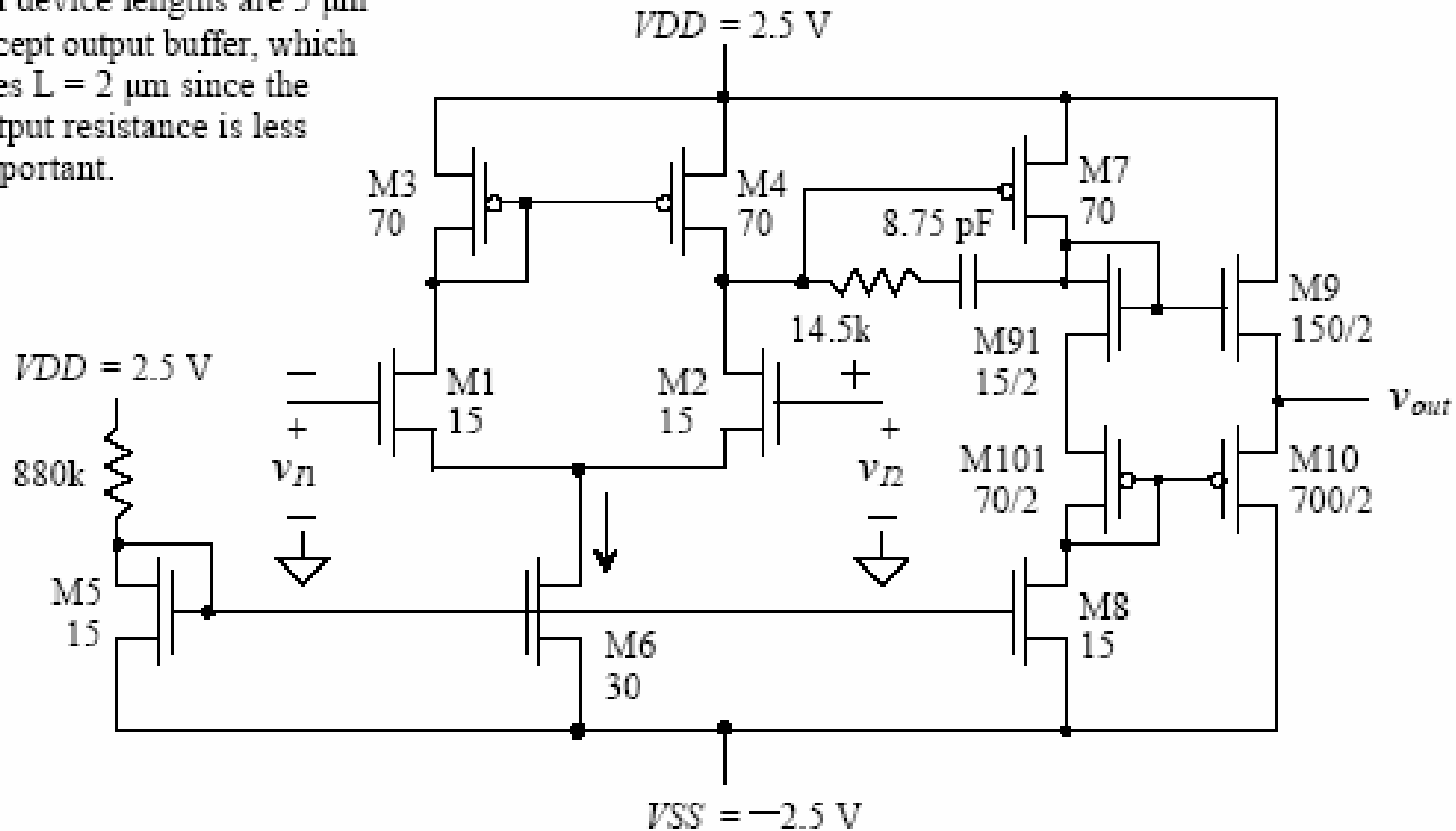
In practice we cancel the nondominant pole by making:

$$\frac{1}{C_C (g_{m9}^{-1} - R_z)} = \frac{-g_{m9}}{C_L + C_E}$$

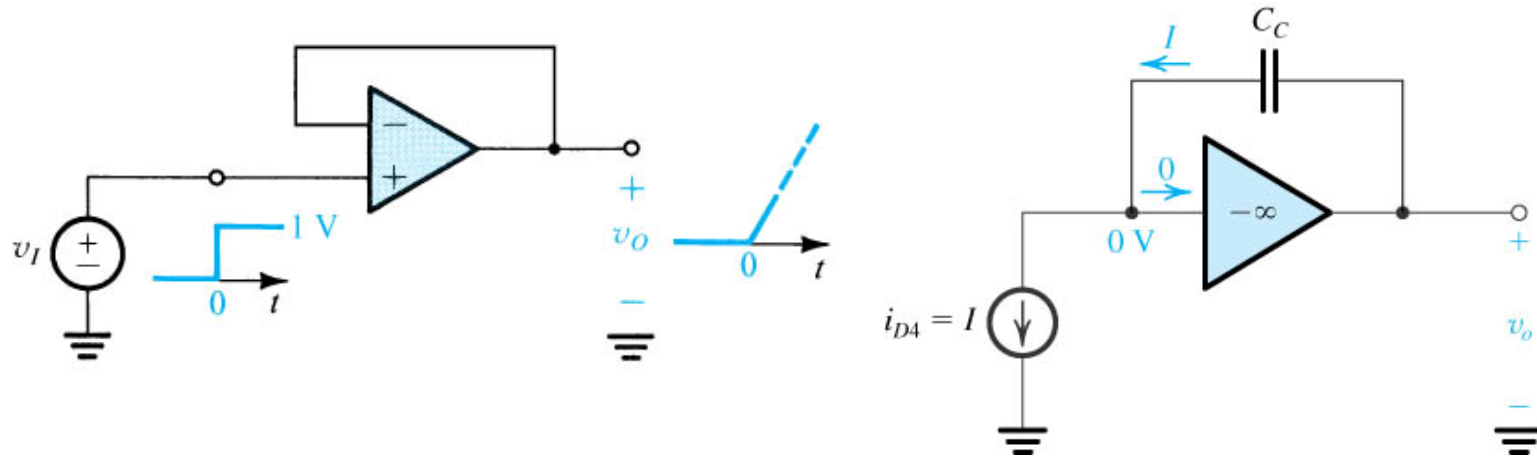
$$\text{then : } R_z = \frac{C_L + C_E + C_C}{g_{m9} C_C}$$

Example of compensated two stage opamp

All device lengths are $5\ \mu\text{m}$ except output buffer, which uses $L = 2\ \mu\text{m}$ since the output resistance is less important.



Slew Rate in two stage opamp

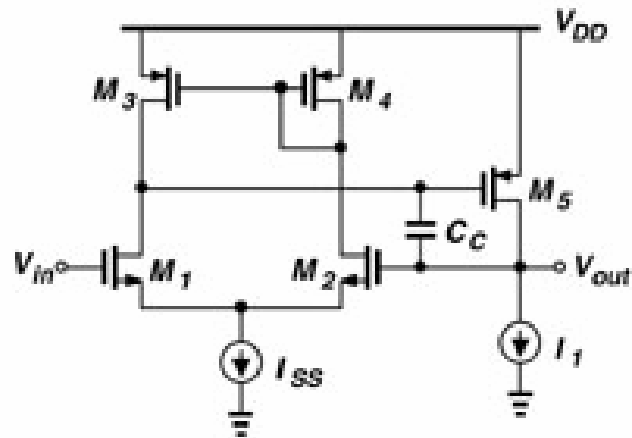
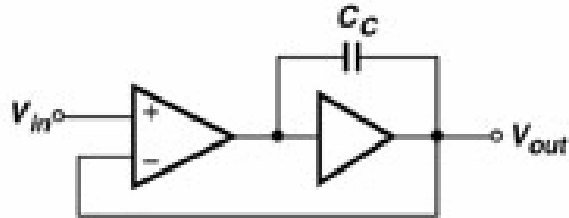


$$v_O(t) = It / C_C \quad \longrightarrow \quad \boxed{SR = I / C_C}$$

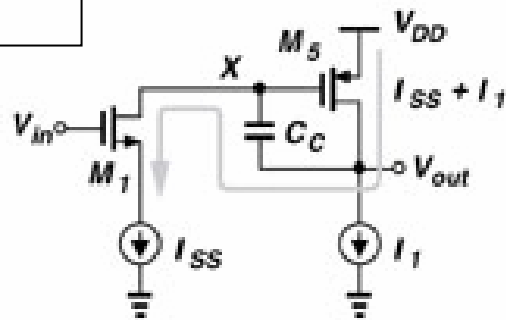
Slew Rate in two stage opamp

Due to large positive step $M_{2,3,4}$ turn off, then C_C is charged by a constant current I_{SS} if parasitic capacitances at X are negligible, then:

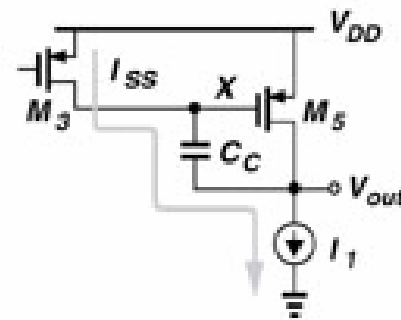
$$SR = I / C_C$$



(a)



(b)



(c)

From:

$$f_T = G_{m1} / (2\pi C_C)$$

or

$$SR = 2\pi f_T V_{OD1}$$

A higher SR can be obtained if M_1 and M_2 are at larger V_{OD} .

Similar situation for negative SR .