Instituto Tecnológico de Estudios Superiores de Occidente

Maestría en Diseño Electrónico

Análisis y Diseño Asistido por Computadora

Final Project

"Voltage Gain Optimization of an OTA Miller"

Teacherr: Dr. J. E. Rayas Sánches

Student: Luis Nathán Pérez Acosta

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"Optimization of voltage gain of an OTA Miller Amplifier"

Objective:

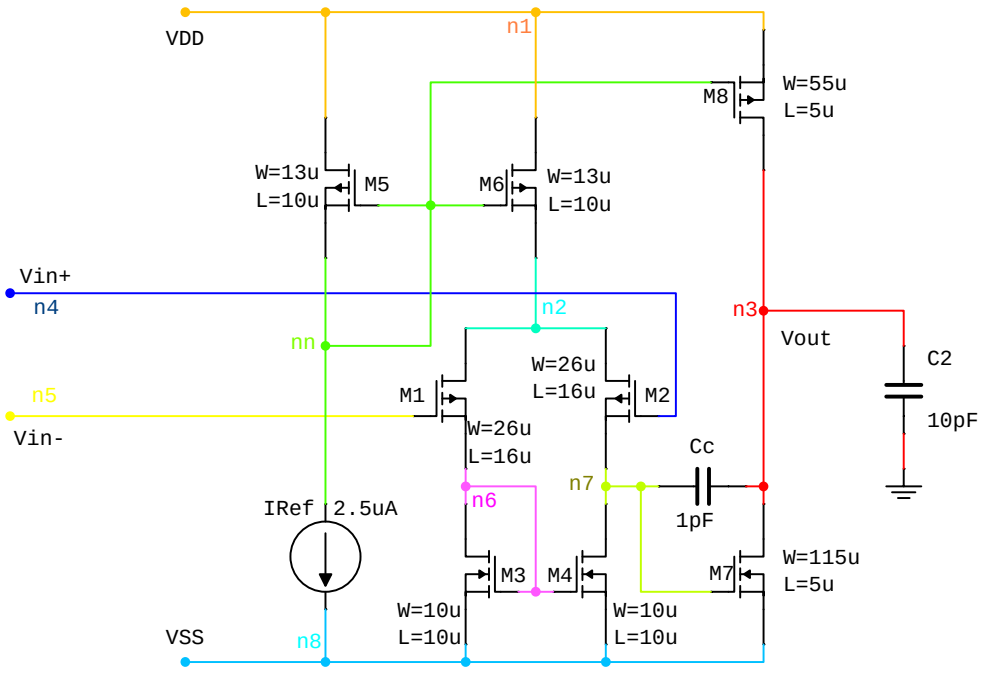
Use the knowledge acquired during the CAD curse to optimize an OTA Miller amplifier to increase the voltage gain by changing the sizes of transistors, value of compensation capacitor and the reference current.

Introduction:

An OTA Miller amplifier is the first stage of an OP-AMP, is where the differentiation of signals occurs. Those amplifiers have a voltage gain commonly above 60dB. This optimization problem will increase the voltage gain over 70dB with out affect the phase margin of 60°. The problem will be solve with Matlab and WinSPICE interacting.

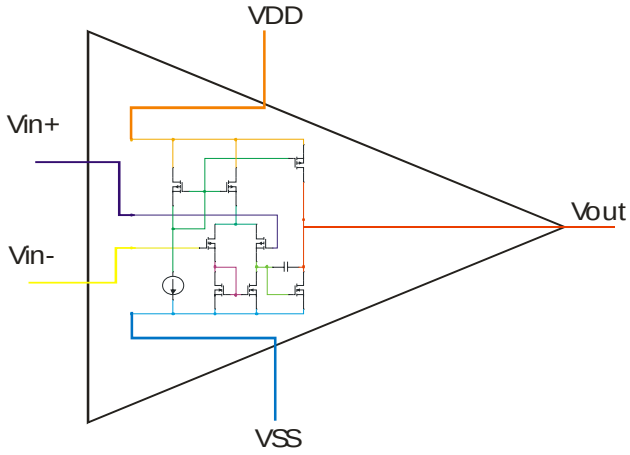
Development:

The schematic circuit to optimize appears in figure F1.



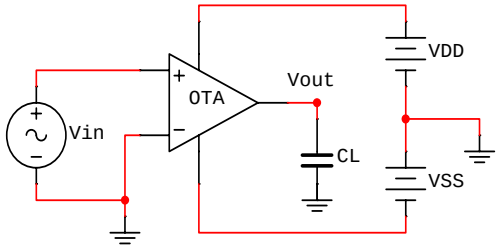
F1.- Initial circuit proposed

To simplify the circuit configuration for simulation, the OTA macromodel in figure F2 will be used.



F2.- OTA Macromodel

Before increase the gain lest see the actual gain and phase margin with parameters showed in F1, using the configuration illustrated en figure F3.



F3.- Open loop schematic

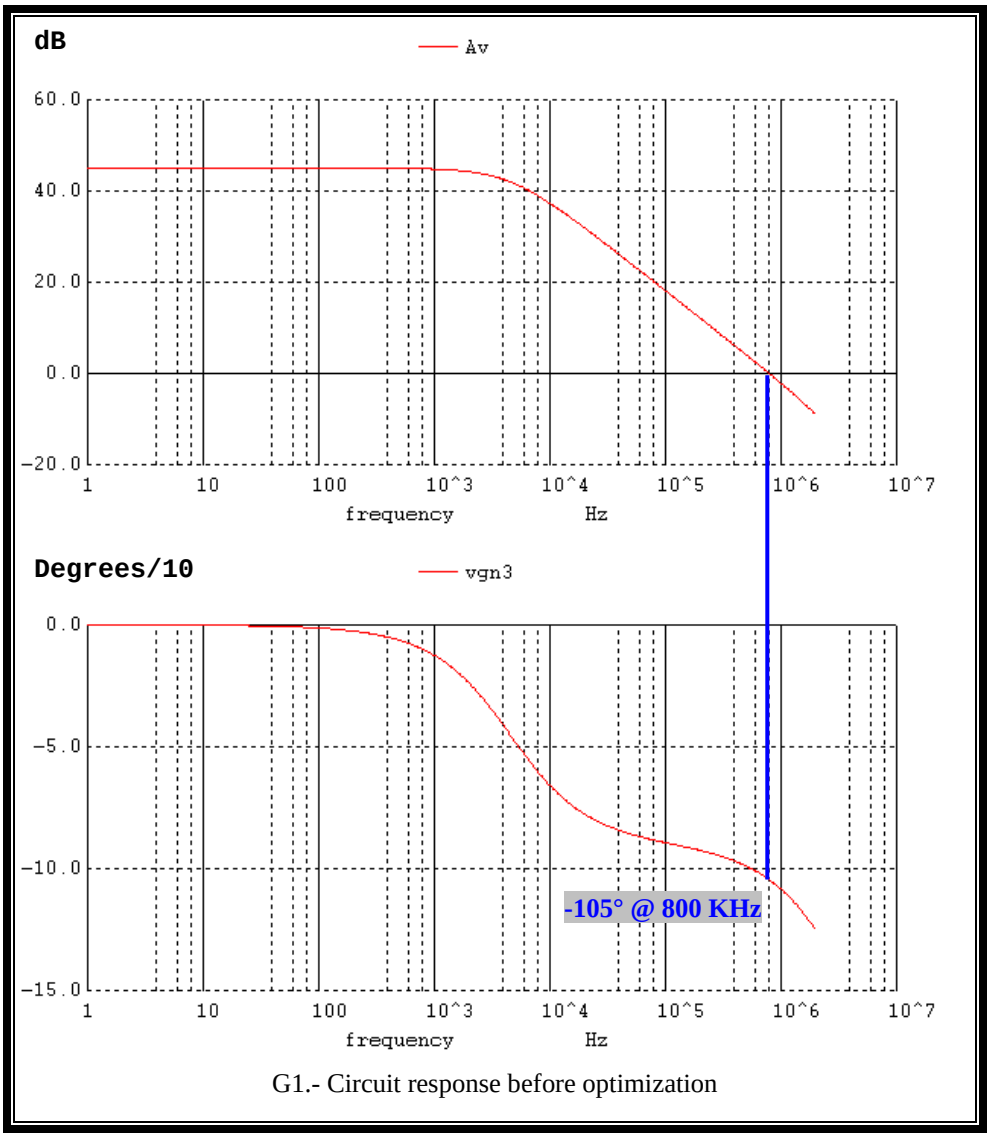
The corresponding WinSPICE Netlist for circuit in F3 appears in square text T1.

```
Op-Amp OTA Miller, Open loop 2, Av, initial circuit
*CAD, ITESO
*Luis Nathán Pérez Acosta
*current mirror
M5          nn nn n1 n1 MOD2           w=13u l=10u
M6          n2 nn n1 n1 MOD2           w=13u l=10u
* Differential pair
M1          n6 n5 n2 n2 MOD2           w=26u l=16u
M2          n7 n4 n2 n2 MOD2           w=26u l=16u
M4          n7 n6 n8 n8 MOD1           w=10u l=10u
M3          n6 n6 n8 n8 MOD1           w=10u l=10u
*output amplifier
M8          n3 nn n1 n1 MOD2           w=55u l=5u
M7          n3 n7 n8 n8 MOD1           w=115u l=5u

Cc          n7 n3 1p
CL          n3 0 10p

*Reference current
iss     nn n8 2.5uA

*external sources
VDD         n1 0 DC 2.5
VSS         n8 0 DC -2.5
Vinn        n5 0 DC 0
Vinp        n4 0 DC 0 AC .001
                                        *continues next page
```

```
.control
AC DEC 100 1 2MEG
Av = 20*log(mag(v(n3)/v(n4)))
vgn3 = 5.73*vp(n3)
plot Av
plot vgn3
.endc

*2-MICRON MOSIS SPICE LEVEL 2 PARAMETERS [BAKER APENDICE A]
.MODEL MOD1 NMOS
+ (LEVEL=2 VTO=0.8756 LAMBDA=2.9330E-02 KP=4.5494E-05)
.MODEL MOD2 PMOS
+ (LEVEL=2 VTO=-0.8889 LAMBDA=4.2290E-02 KP=1.5035E-05)
.end
```

T1.- Netlist of circuit in F3

G1 shows the graphics after execution of T1 in WinSPICE.



G1.- Circuit response before optimization

Note: Degrees in phase margin graphic are divided by 10, thus, 10.5° x 10 = 105°

As we see the voltage gain (Av) is 45dB and phase margin is 105° - 180° = 75°. Margin phase is 15° higher than desired and Av is 15dB lower than a good OTA design.

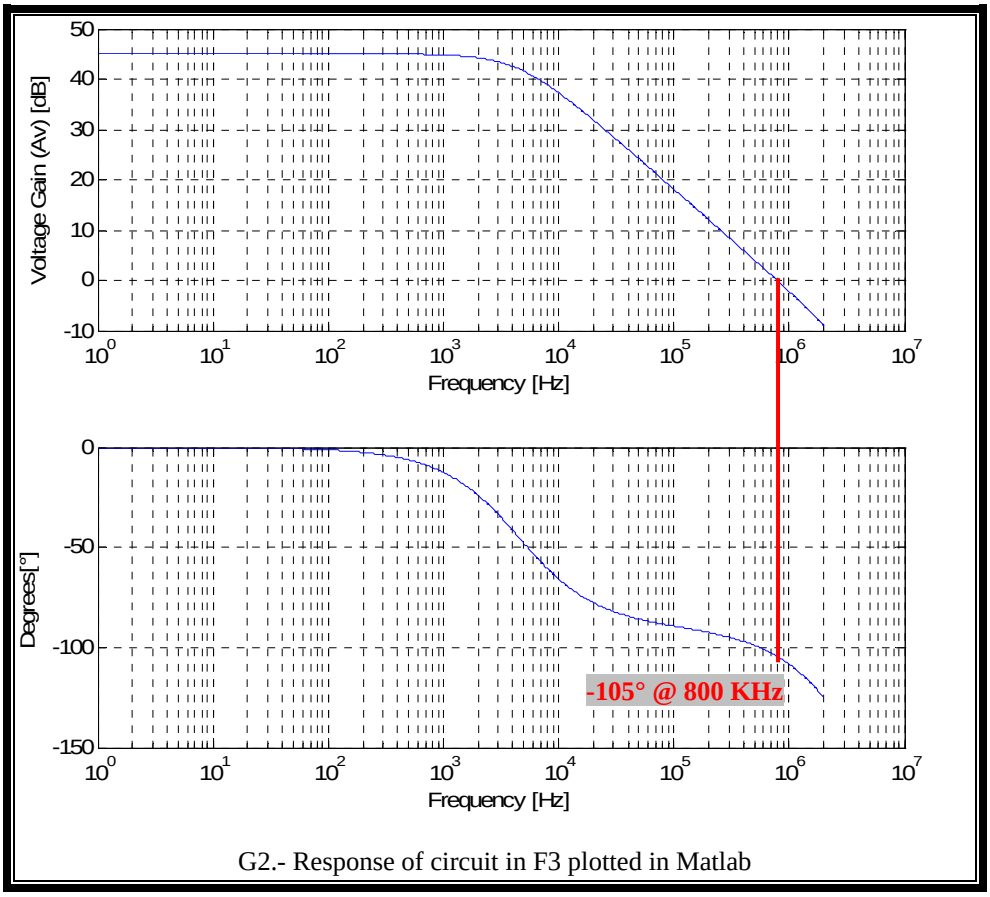
Matlab will be used to optimize the design, calling WinSPICE to probe the changes done in previous Netlist in T1. First, the Matlab code (shown in square text T2) that calls WinSPICE will plot the response using Matlab, the resulting graphics have to be the same than G1. The files "FormatSpiceFile.m" [1] and executable file "WSPICE3.exe" have to be in the same folder (see appendix A).

```
%Op-Amp OTA, open loop, Lunes 08 de Mayo de 2006
%*Final Project, CAD, Maestría en Diseño Electrónico ITESO
%*Voltage Gain and phase margin
%This code calls WinSPICE and extracts the circuit response,
%then Matlab plots that responses
title = 'OTA optimization';
%Current mirror
nb{1} = ['M5         nn nn n1 n1 MOD2 w=13u l=10u'];
nb{2} = ['M6         n2 nn n1 n1 MOD2 w=13u l=10u']
%*Differential Pair
nb{3} = ['M1         n6 n5 n2 n2 MOD2 w=26u  l=16u'];
nb{4} = ['M2         n7 n4 n2 n2 MOD2 w=26u  l=16u'];
nb{5} = ['M4         n7 n6 n8 n8 MOD1 w=10u  l=10u'];
nb{6} = ['M3         n6 n6 n8 n8 MOD1 w=10u  l=10u'];
%*Output amplifier
nb{7} = ['M8         n3 nn n1 n1 MOD2 w=55u l=5u'];
nb{8} = ['M7         n3 n7 n8 n8 MOD1 w=115u  l=5u'];
nb{9} = 'Cc         n7 n3 1p';
nb{10}= 'CL         n3 0 10p';
%*Reference current surce
nb{11} = 'iss  nn n8 2.5u';
%*Voltage sources
nb{12} = 'VDD        n1 0 DC 2.5';
nb{13} = 'VSS        n8 0 DC -2.5';
nb{14} = 'Vinn       n5 0 DC 0 ';
nb{15} = 'Vinp       n4 0 DC 0 AC .001';
Netlistblock = '';
for i = 1:15
    Netlistblock = str2mat(Netlistblock, nb{i});
end
cb{1} = '.control';
cb{2} = ['AC dec 100 1 2meg'];
cb{3} = 'Av = 20*log(mag(v(n3)/v(n4)))';
cb{4} = 'vgn3 = 57.3*vp(n3)';
cb{5} = 'write AC.csv Av';
cb{6} = 'write Ph.csv vgn3';
cb{7} = 'DC vinp -2.5 2.5 .1';
cb{8} = 'write DC.csv v(n3)';
cb{9} = 'quit';
cb{10} = '.endc';
controlblock = '';
for i = 1:10
    controlblock = str2mat(controlblock, cb{i});
end
%*2-MICRON MOSIS SPICE LEVEL 2 PARAMETERS [BAKER APENDICE A]
mb{1} = '.MODEL MOD1 NMOS';
mb{2} = '+ (LEVEL=2 VTO=0.8756 LAMBDA=2.9330E-02 KP=4.5494E-05)';
mb{3} = '.MODEL MOD2 PMOS';
mb{4} = '+ (LEVEL=2 VTO=-0.8889 LAMBDA=4.2290E-02 KP=1.5035E-05) ';
mb{5} = '.end'
modelblock = '';
for i = 1:5
    modelblock = str2mat(modelblock, mb{i});
end

%save WinSPICE circuit
ckt_file = str2mat(title, Netlistblock, controlblock, modelblock);
```

```
[rows, columns] = size(ckt_file);
fp = fopen('ota_spice.cir','w+');
for i=1:rows
    for j=1:columns
        fprintf(fp,'%s',ckt_file(i,j));
    end
    fprintf(fp,'%s\n','');
end
fclose(fp);

%Run WinSPICE
! wspice3 ota_spice.cir
%read WinSPICE output file
FormatSpiceFile('AC.csv', 'AC.txt');
load AC.txt;
frec = AC(:,1);
Av = AC(:,3);
FormatSpiceFile('Ph.csv', 'Ph.txt');
load Ph.txt;
subplot(2,1,1)
semilogx(frec,Av)
grid
xlabel('Frequency [Hz]'), ylabel('Voltage Gain (Av) [dB]')
freq = Ph(:,1);
gr = Ph(:,3);
subplot(2,1,2)
semilogx(freq,gr)
xlabel('Frequency [Hz]'), ylabel('Degrees[°]'),grid
```

T2.- Matlab code that plot the WinSPICE response of circuit in F3.

The resulting graphics after the execution of T2 in Matlab appears in G2.



G2.- Response of circuit in F3 plotted in Matlab

Bout graphics (G1 and G2) match perfectly, then, the next step is to write three different Matlab code: 1) Optimization code, 2) Objective function and 3) a code that modify parameters in WinSPICE netlist.

The selected method to optimize the circuit is Minimax [2], and the Matlab codes appear in T3, T4 and T5.

```
%Op-Amp OTA, Optimization, Lunes 08 de Mayo de 2006
%*Final Project, CAD, Maestría en Diseño Electrónico ITESO
%
w5 = 13; %=w6
w1 = 90; %=w2
w3 = 15; %=w4
w8 = 130;
w7 = 150;
Cc = 2;
iss = 2.5;
Xo=[w5, w1, w3, w8, w7, iss, Cc];
options = optimset('MaxFunEvals',300);
[x,FunVal,EF,output] = fminsearch('OF_ota',Xo,options)

w5_opt = x(1)
w1_opt = x(2)
w3_opt = x(3)
w8_opt = x(4)
w7_opt = x(5)
Cc_opt = x(7)
iss_opt = x(6)

%after optimization
[frec,Av,freq,gr] = otaph(x,1,5e6);
subplot(2,1,2)
semilogx(freq,gr)
xlabel('Frequency [Hz]'), ylabel('Degrees[°]'),grid
subplot(2,1,1)
semilogx(frec,Av)
xlabel('Frequency [Hz]'), ylabel('Voltage Gain (Av) [dB]')
grid
```

T3.- Optimization function.

```
%Op-Amp OTA, Objetive Function, Lunes 08 de Mayo de 2006
%*Final Project, CAD, Maestría en Diseño Electrónico ITESO
%
function u = OF_ota(x)
Avmin = 60; %dB
fi = 1;%Hz
ff = 100;%Hz
[frec, Av, freq, gr] = otaph(abs(x),fi,ff);
% calculing objective function
e1 = -100*ones(length(frec),1);%initializing error vectors
for i=1:length(frec)
    e1(i) = 1 – Av(i)/Avmin;
end
e2 = 1-(x(7)/2.5); % compensation Capacitor
e3 = (x(7)/3)-1; % 3pF < Cc < 2.5pF
e4 = 1-(x(1)/2); % minimal width size = 2um
e5 = 1-(x(2)/2); % minimal width size = 2um
e6 = 1-(x(3)/2); % minimal width size = 2um
e7 = 1-(x(4)/2); % minimal width size = 2um
e8 = 1-(x(5)/2); % minimal width size = 2um

e = max(e1');
u =max([e,e2,e3,e4,e5,e6,e7,e8]);
```

T4.- Objective Function.

```
Function [frec, Av, freq, gr] = otaph(x,fi,ff)
%fi = initial frequency (AC sweep)
%ff = final frequency
%x = variables
%Op-Amp OTA  rojec, Lunes 08 de Mayo de 2006
%*Final  roject, CAD, Maestria en Diseño Electrónico ITESO
title = 'OTA optimization';
x(1,:)=x(1,:)*1e-6;
x(1,7)= x(1,7)*1e-6;
nb{1} = ['M5         nn nn n1 n1 MOD2 w=' abs(num2str(x(1))) ' l=5u'];
nb{2} = ['M6         n2 nn n1 n1 MOD2 w=' abs(num2str(x(1))) ' l=5u'];
%*Par Diferencial
nb{3} = ['M1         n6 n5 n2 n2 MOD2 w=' abs(num2str(x(2))) ' l=5u'];
nb{4} = ['M2         n7 n4 n2 n2 MOD2 w=' abs(num2str(x(2))) ' l=5u'];
nb{5} = ['M4         n7 n6 n8 n8 MOD1 w=' abs(num2str(x(3))) ' l=5u'];
nb{6} = ['M3         n6 n6 n8 n8 MOD1 w=' abs(num2str(x(3))) ' l=5u'];
%*Amplificador de salida
nb{7} = ['M8         n3 nn n1 n1 MOD2 w=' abs(num2str(x(4))) ' l=5u'];
nb{8} = ['M7         n3 n7 n8 n8 MOD1 w=' abs(num2str(x(5))) ' l=5u'];

nb{9} = ['Cc         n7 n3 ' abs(num2str(x(7)))];
nb{10}= 'CL         n3 0 10p';
nb{11}= '*Rl         n3 0 100k';
%*fuente de corriente 5uA
%Mi1       nn ni n8 n8 MOD1    w=56.4u l=5u
%Mi2       ni ni n8 n8 MOD1    w=56.4u l=5u
%Ri1       n1 ni 140.74kohm
nb{12} = ['iss nn n8 ' abs(num2str(x(6)))];

%*Fuentes de alimentación y excitación
nb{13} = 'VDD        n1 0 DC 2.5';
nb{14} = 'VSS        n8 0 DC -2.5';
nb{15} = 'Vinn       n5 0 DC 0 ';
nb{16} = 'Vinp       n4 0 DC 0 AC .001';
Netlistblock = '';
for i = 1:16
    Netlistblock = str2mat(Netlistblock, nb{i});
end

cb{1} = '.control';
cb{2} = ['AC dec 100 ' mat2str(fi) ' ' mat2str(ff)];
cb{3} = 'Av = 20*log(mag(v(n3)/v(n4)))';
cb{4} = 'vgn3 = 57.3*vp(n3)';
cb{5} = 'write AC.csv Av';
cb{6} = 'write Ph.csv vgn3';
cb{7} = 'DC vinp -2.5 2.5 .1';
cb{8} = 'write DC.csv v(n3)';
cb{9} = 'quit';
cb{10} = '.endc';
controlblock = '';
for i = 1:10
    controlblock = str2mat(controlblock, cb{i});
end

%*2-MICRON MOSIS SPICE LEVEL 2 PARAMETERS [BAKER APENDICE A]
mb{1} = '.MODEL MOD1 NMOS';
mb{2} = '+ (LEVEL=2 VTO=0.8756 LAMBDA=2.9330E-02 KP=4.5494E-05)';
mb{3} = '.MODEL MOD2 PMOS';
mb{4} = '+ (LEVEL=2 VTO=-0.8889 LAMBDA=4.2290E-02 KP=1.5035E-05) ';
mb{5} = '.end'
modelblock = '';
for i = 1:5
    modelblock = str2mat(modelblock, mb{i});
end

%save WinSPICE circuit
ckt_file = str2mat(title, Netlistblock, controlblock, modelblock);
[rows, columns] = size(ckt_file);
fp = fopen('ota_spice.cir','w+');
for i=1:rows
    for j=1:columns                              %continues next page
```

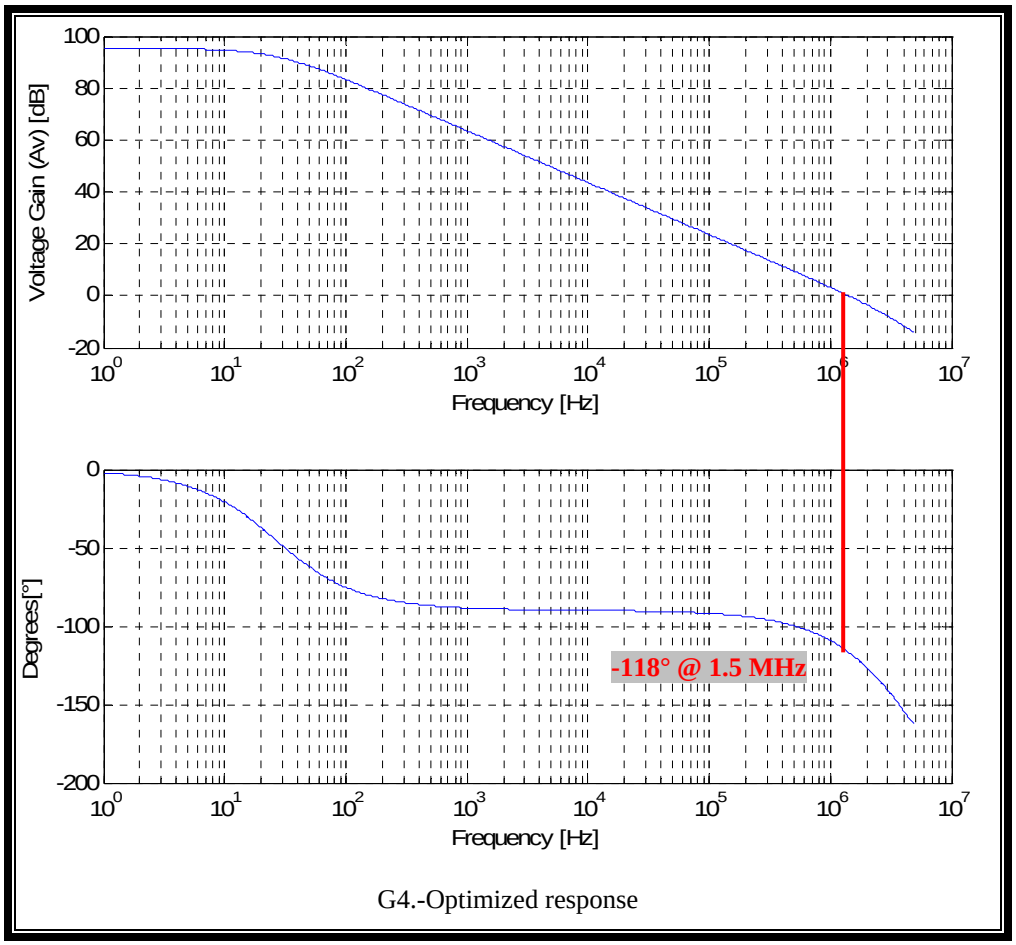
```
        fprintf(fp,'%s',ckt_file(i,j));
    end
    fprintf(fp,'%s\n','');
end
fclose(fp);

%Run WinSPICE
! wspice3 ota_spice.cir
%read WinSPICE output file
FormatSpiceFile('AC.csv', 'AC.txt');
load AC.txt;
frec = AC(:,1);
Av = AC(:,3);
FormatSpiceFile('Ph.csv', 'Ph.txt');
load Ph.txt;
freq = Ph(:,1);
gr = Ph(:,3);
```

T5.- Netlist generador

Note: T5 has different sizes for the channel length of transistor, where all of then are 5µm

Conditions established in T4 for the width of transistors ensures an optimization with values acceptable for the process parameter of 2µm, conditions for compensation capacitor makes the phase margin near by 60° [3-1] "FormatSpiceFile.m" and executable file "WSPICE3.exe" have to be in the same folder than T3, T4 and T5 (see Appendix A).

The graphics after optimization appears in G3.



G4.-Optimized response

The optimized width sizes of transistors, Cc and I_{REF} are the next:

$W_{1\&2}$	$W_{3\&4}$	$W_{5\&6}$	W_7	W_8	Cc	I_{REF}
92.078µm	12.473µm	12.54µm	180.209µm	100.268µm	2.72pF	2.182µA

A new WinSPICE netlist with rounded values appears in T6, and the resulting graphics appears in G5.

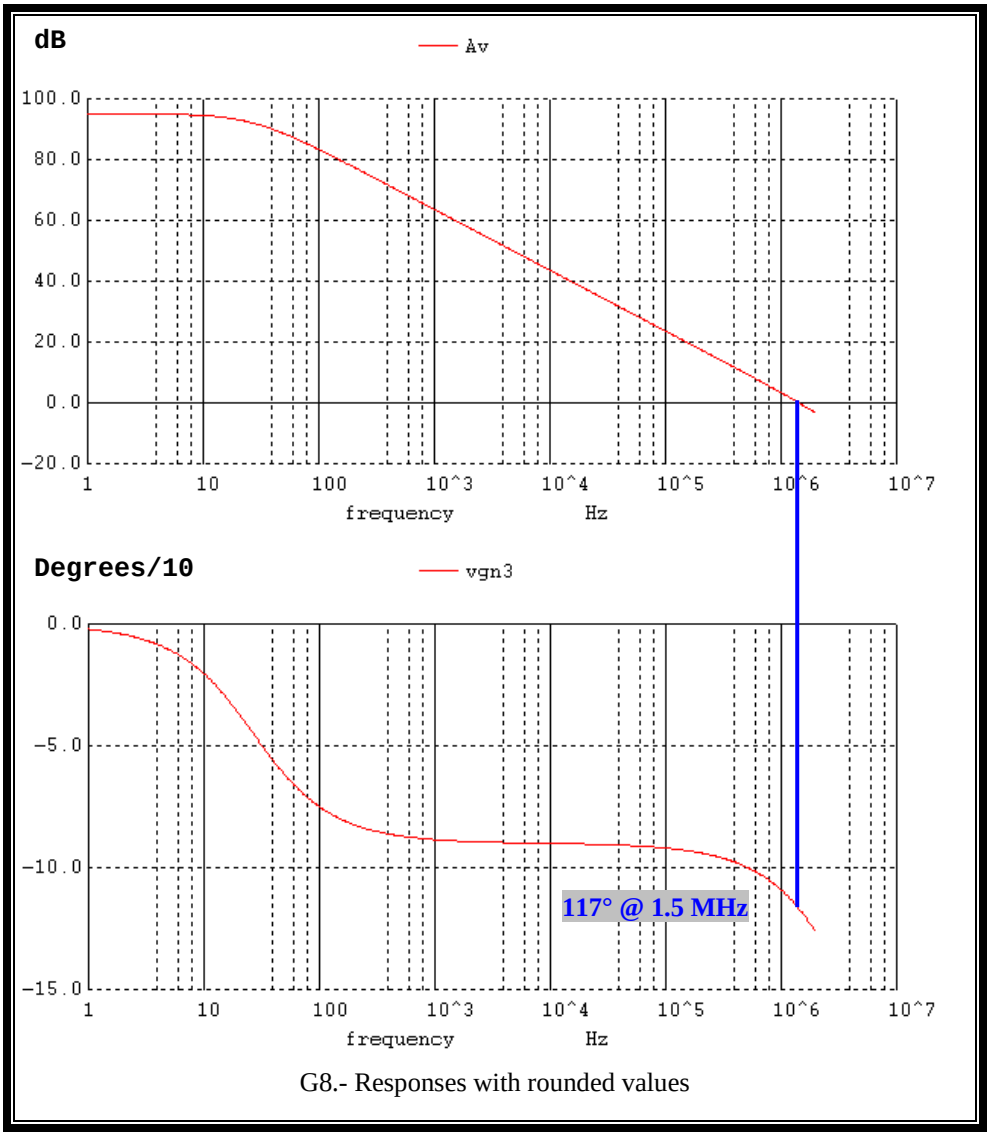
```
Op-Amp OTA Miller, Open loop 2, Av, optimized circuit
*CAD, ITESO
*Luis Nathán Pérez Acosta
*current mirror
M5          nn nn n1 n1 MOD2          w=12.5u l=5u
M6          n2 nn n1 n1 MOD2          w=12.5u l=5u
*Differential pair
M1          n6 n5 n2 n2 MOD2          w=92u l=5u
M2          n7 n4 n2 n2 MOD2          w=92u l=5u
M4          n7 n6 n8 n8 MOD1          w=12.5u l=5u
M3          n6 n6 n8 n8 MOD1          w=12.5u l=5u
*output amplifier
M8          n3 nn n1 n1 MOD2          w=100u l=5u
M7          n3 n7 n8 n8 MOD1          w=180u l=5u

Cc          n7 n3 2.72p
CL          n3 0 10p

*Reference current
iss     nn n8 2.2uA

*external sources
VDD         n1 0 DC 2.5
VSS         n8 0 DC -2.5
Vinn        n5 0 DC 0
Vinp        n4 0 DC 0 AC .001

.control
AC DEC 100 1 2MEG
Av = 20*log(mag(v(n3)/v(n4)))
vgn3 = 5.73*vp(n3)
plot Av
plot vgn3
.endc

*2-MICRON MOSIS SPICE LEVEL 2 PARAMETERS [BAKER APENDICE A]
.MODEL MOD1 NMOS
+ (LEVEL=2 VTO=0.8756 LAMBDA=2.9330E-02 KP=4.5494E-05)
.MODEL MOD2 PMOS
+ (LEVEL=2 VTO=-0.8889 LAMBDA=4.2290E-02 KP=1.5035E-05)
.end
```

T6.- WinSPICE netlist with rounded optimized values.

As we see, the changes between G4 and G5 are almost nothing, just the margin phase moved form 62° to 63°. A summary of changes before and after optimization appears in table T7. Table T8 shows the common parameters of Op-Amps before and after optimization (see appendix B).

	$(W/L)_{1\&2}$	$(W/L)_{3\&4}$	$(W/L)_{5\&6}$	$(W/L)_7$	$(W/L)_8$	Cc	I_{REF}
Before	(26/16) µm	(10/10) µm	(13/10) µm	(115/5) µm	(55/5) µm	1 pF	2.5 µA
After	(92/5) µm	(12.5/5)µm	(12.5/5)µm	(180/5) µm	(100/5) µm	2.72 pF	2.2 µA

T7.- Components values before and after optimization.



G8.- Responses with rounded values

Characteristics	Before	After
Voltage Gain (Av)	45dB	95dB
Phase Margin	75°	63°
CMRR	84.9dB	99.8dB
Slew Rate	2V/µS	0.66 V/µS
Output Swing	-2.4V a 2.4	-2.5 a 2.5

T8.- OTA characteristics before and after optimization.

Conclusions:

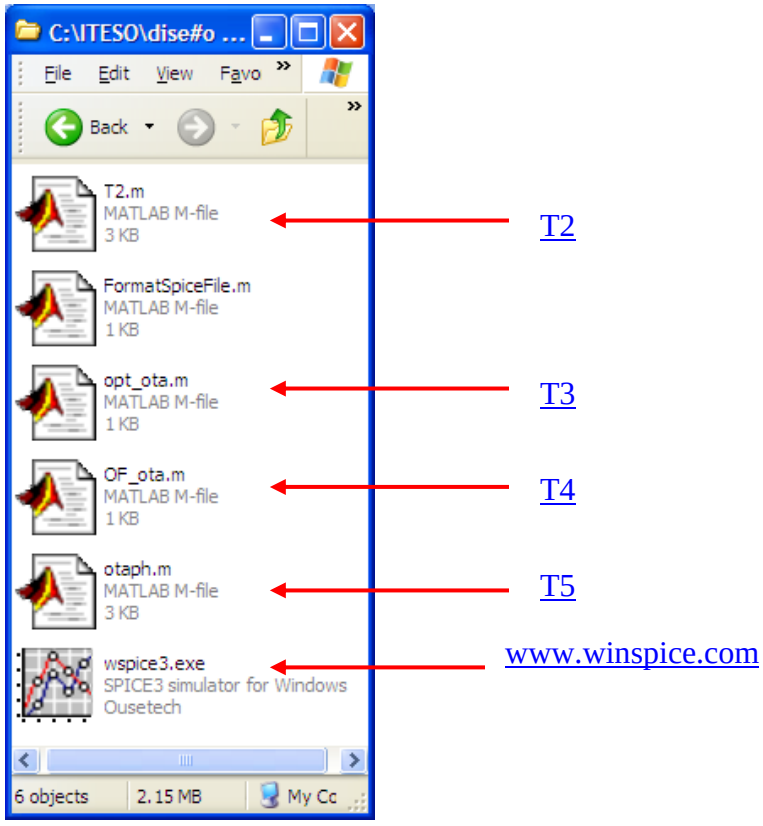
Not any calculus had to be made to optimize the OTA circuit in F1, just by the interaction between Matlab and WinSPICE. This kind of iterations can help to any electronics designer to find optimal components values for a specific design.

Appendix A

"FormatSpiceFile.m"

```
%Esta funcion convierte los archivos .csv a .txt
%uso:   FortmatSpiceFile(file1, file2)
%       file1: nombre del archivo a convertir (.csv)
%       file2: nombre del archivo convertido (.txt)

function FormatSpiceFile (file1, file2)
fid1 = fopen(file1);
fid2 = fopen(file2,'w+');

line = fgetl(fid1);
line = fgetl(fid1);
while line~=-1
    line_length = length(line);
    for i = 1:line_length
        if line(i) == ','
           line(i) = ' ';
        end
        fprintf(fid2, '%s', line(i));
    end
    fprintf(fid2, '%s\n', '');
    line = fgetl(fid1);
end
fclose(fid1);
fclose(fid2);
```

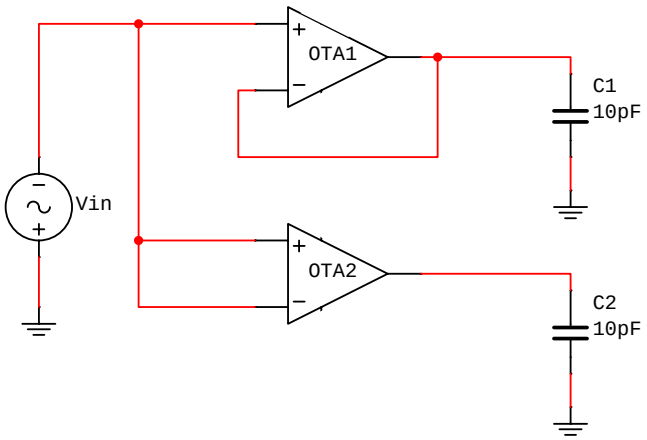
Files needed to run the optimization problem



Appendix B

CMRR simulation.

Common Mode Rejection Ratio can be simulated using the schematic circuit shown in figure F4 [4]. The corresponding netlist for circuit before and after optimization appears in T9, and the resulting graphics in G9.



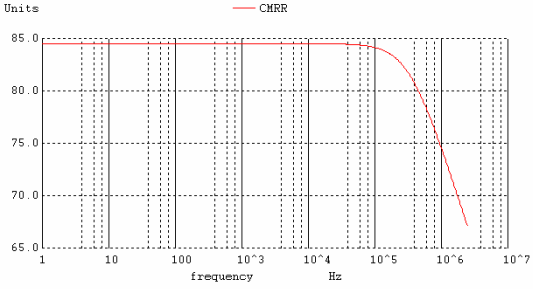
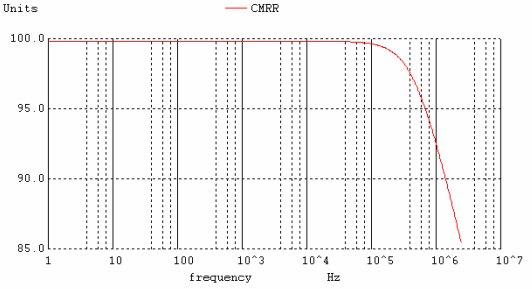
F4.- Schematic for CMRR simulation.

Before	After
Op-Amp OTA Miller,level 2, *lazo abierto OTA1 *entrdas comunes OTA2 Analógico, ITESO ********OTA 1******************** M5 nn nn n1 n1 MOD2 w=13u l=10u M6 n2 nn n1 n1 MOD2 w=13u l=10u *Par Diferencial M1 n6 0 n2 n2 MOD2 w=26u l=16u M2 n7 n4 n2 n2 MOD2 w=26u l=16u M4 n7 n6 n8 n8 MOD1 w=10u l=10u M3 n6 n6 n8 n8 MOD1 w=10u l=10u *Amplificador de salida M8 n3 nn n1 n1 MOD2 w=55u l=5u M7 n3 n7 n8 n8 MOD1 w=115u l=5u Cc n7 n3 1p CL n3 0 10p *fuente de corriente 5uA iss nn n8 2.5u **********OTA2****************** M52 nn2 nn2 n1 n1 MOD2 w=13u l=10u M62 n22 nn2 n1 n1 MOD2 w=13u l=10u *Par Diferencial M12 n62 n4 n22 n22 MOD2 w=26u l=16u M22 n72 n4 n22 n22 MOD2 w=26u l=16u M42 n72 n62 n8 n8 MOD1 w=10u l=10u M32 n62 n62 n8 n8 MOD1 w=10u l=10u *Amplificador de salida M82 n32 nn2 n1 n1 MOD2 w=55u l=5u M72 n32 n72 n8 n8 MOD1 w=115u l=5u *continues next page	Op-Amp OTA Miller,level 2, *lazo abierto OTA1 *entrdas comunes OTA2 Analógico, ITESO ********OTA 1******************** M5 nn nn n1 n1 MOD2 w=12.5u l=5u M6 n2 nn n1 n1 MOD2 w=12.5u l=5u *Par Diferencial M1 n6 0 n2 n2 MOD2 w=92u l=5u M2 n7 n4 n2 n2 MOD2 w=92u l=5u M4 n7 n6 n8 n8 MOD1 w=12.5u l=5u M3 n6 n6 n8 n8 MOD1 w=12.5u l=5u *Amplificador de salida M8 n3 nn n1 n1 MOD2 w=100u l=5u M7 n3 n7 n8 n8 MOD1 w=180u l=5u Cc n7 n3 2.72p CL n3 0 10p *fuente de corriente 5uA iss nn n8 2.2u **********OTA2****************** M52 nn2 nn2 n1 n1 MOD2 w=12.5u l=5u M62 n22 nn2 n1 n1 MOD2 w=12.5u l=5u *Par Diferencial M12 n62 n4 n22 n22 MOD2 w=92u l=5u M22 n72 n4 n22 n22 MOD2 w=92u l=5u M42 n72 n62 n8 n8 MOD1 w=12.5u l=5u M32 n62 n62 n8 n8 MOD1 w=12.5u l=5u *Amplificador de salida M82 n32 nn2 n1 n1 MOD2 w=100u l=5u M72 n32 n72 n8 n8 MOD1 w=180u l=5u *continues next page

```
Cc2          n72 n32 1p
CL2          n32 0 10p

*fuente de corriente 5uA
iss2         nn2 0 2.5u

*Fuentes de alimentación y excitación
VDD         n1 0 DC 2.5
VSS         n8 0 DC -2.5
*Vinn        n5 0 DC 0
Vinp        n4 0 DC 0 AC .001

.control
AC DEC 100 1 2.5MEG
CMRR = 20*log(mag(v(n3)/v(n32)))
plot CMRR
.endc

*2-MICRON MOSIS SPICE LEVEL 2 PARAMETERS
.MODEL MOD1 NMOS
+ (LEVEL=2 VTO=0.8756 LAMBDA=2.9330E-02
KP=4.5494E-05)
.MODEL MOD2 PMOS
+ (LEVEL=2 VTO=-0.8889 LAMBDA=4.2290E-02
KP=1.5035E-05)
.end
```

```
Cc2          n72 n32 2.72p
CL2          n32 0 10p

*fuente de corriente 5uA
iss2         nn2 0 2.2u

*Fuentes de alimentación y excitación
VDD         n1 0 DC 2.5
VSS         n8 0 DC -2.5
*Vinn        n5 0 DC 0
Vinp        n4 0 DC 0 AC .001

.control
AC DEC 100 1 2.5MEG
CMRR = 20*log(mag(v(n3)/v(n32)))
plot CMRR
.endc

*2-MICRON MOSIS SPICE LEVEL 2 PARAMETERS
.MODEL MOD1 NMOS
+ (LEVEL=2 VTO=0.8756 LAMBDA=2.9330E-02
KP=4.5494E-05)
.MODEL MOD2 PMOS
+ (LEVEL=2 VTO=-0.8889 LAMBDA=4.2290E-02
KP=1.5035E-05)
.end
```

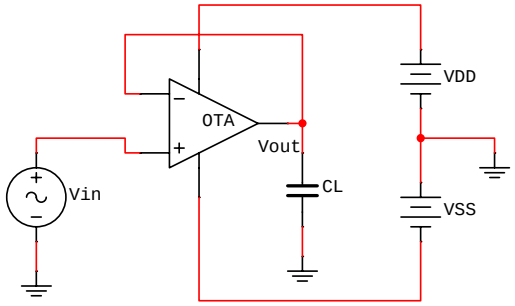
T9.- CMRR netlist, before and after optimization.

Before	After
	

G9.- CMRR response for circuit in F1 before and after optimization.

Slew Rate:

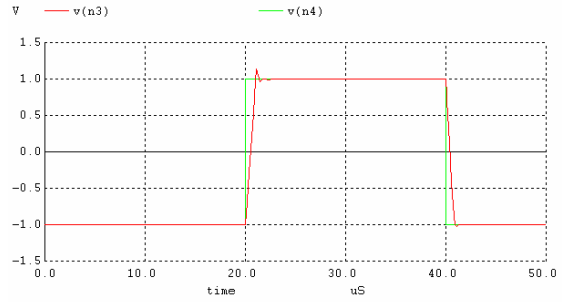
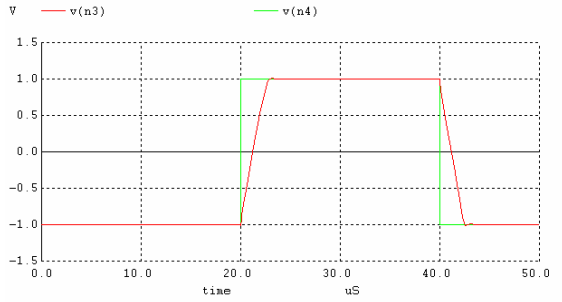
Slew Rate can be simulated using the schematic circuit shown in figure F5 [3-2]. The corresponding netlist for circuit before and after optimization appears in T10, and the resulting graphics in G10.



F5.- Schematic for SR simulation

Before	After
M5 nn nn n1 n1 MOD2 w=13u l=10u M6 n2 nn n1 n1 MOD2 w=13u l=10u *Par Diferencial M1 n6 n3 n2 n2 MOD2 w=26u l=10u M2 n7 n4 n2 n2 MOD2 w=26u l=10u M4 n7 n6 n8 n8 MOD1 w=10u l=10u M3 n6 n6 n8 n8 MOD1 w=10u l=10u *Amplificador de salida M8 n3 nn n1 n1 MOD2 w=55u l=5u M7 n3 n7 n8 n8 MOD1 w=115u l=5u Cc n7 n3 1p CL n3 0 10p *fuente de corriente iss nn n8 2.5uA *Fuentes de alimentación y excitación VDD n1 0 DC 2.5 VSS n8 0 DC -2.5 Vinn n5 0 DC 0 Vinp n4 0 DC 0 AC .001 +PWL(0s -1v 20Us -1 20.01Us 1v 40Us 1v +40.01Us -1v 50US -1) .control TRAN 1us 50Us plot v(n3) v(n4) .endc *2-MICRON MOSIS SPICE LEVEL 2 PARAMETERS [BAKER APENDICE A] .MODEL MOD1 NMOS + (LEVEL=2 VTO=0.8756 LAMBDA=2.9330E-02 KP=4.5494E-05) .MODEL MOD2 PMOS + (LEVEL=2 VTO=-0.8889 LAMBDA=4.2290E-02 KP=1.5035E-05) .end	M5 nn nn n1 n1 MOD2 w=12.5u l=5u M6 n2 nn n1 n1 MOD2 w=12.5u l=5u *Par Diferencial M1 n6 n3 n2 n2 MOD2 w=92u l=5u M2 n7 n4 n2 n2 MOD2 w=92u l=5u M4 n7 n6 n8 n8 MOD1 w=12.5u l=5u M3 n6 n6 n8 n8 MOD1 w=12.5u l=5u *Amplificador de salida M8 n3 nn n1 n1 MOD2 w=100u l=5u M7 n3 n7 n8 n8 MOD1 w=180u l=5u Cc n7 n3 2.72p CL n3 0 10p *fuente de corriente iss nn n8 2.2uA *Fuentes de alimentación y excitación VDD n1 0 DC 2.5 VSS n8 0 DC -2.5 Vinn n5 0 DC 0 Vinp n4 0 DC 0 AC .001 +PWL(0s -1v 20Us -1 20.01Us 1v 40Us 1v +40.01Us -1v 50US -1) .control TRAN 1us 50Us plot v(n3) v(n4) .endc *2-MICRON MOSIS SPICE LEVEL 2 PARAMETERS [BAKER APENDICE A] .MODEL MOD1 NMOS + (LEVEL=2 VTO=0.8756 LAMBDA=2.9330E-02 KP=4.5494E-05) .MODEL MOD2 PMOS + (LEVEL=2 VTO=-0.8889 LAMBDA=4.2290E-02 KP=1.5035E-05) .end

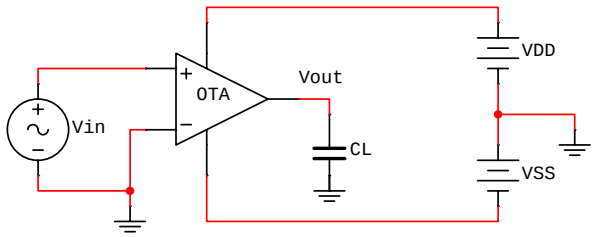
T10.- Netlist for Slew Rate simulation before and after optimization.

Before	After
	

G10.- Response of Slew Rate after and before optimization.

Output Swing:

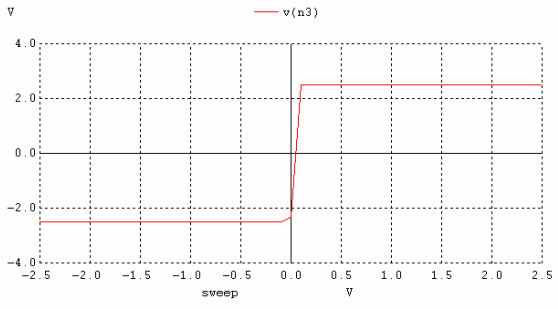
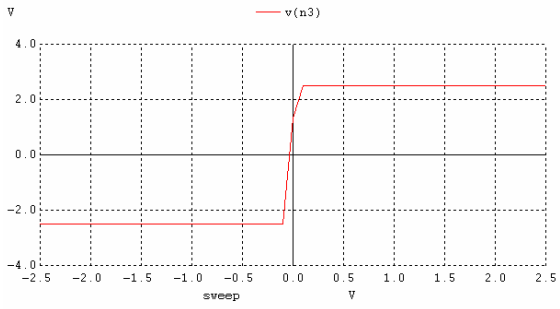
Output Swing can be simulated using the schematic circuit shown in figure F6 [3-3]. The corresponding netlist for circuit before and after optimization appears in T11, and the resulting graphics in G11



F6.- Schematic to simulate the Output Swing

Before	After
Output Swing M5 nn nn n1 n1 MOD2 w=13u l=10u M6 n2 nn n1 n1 MOD2 w=13u l=10u *Par Diferencial M1 n6 n5 n2 n2 MOD2 w=26u l=16u M2 n7 n4 n2 n2 MOD2 w=26u l=16u M4 n7 n6 n8 n8 MOD1 w=10u l=10u M3 n6 n6 n8 n8 MOD1 w=10u l=10u *Amplificador de salida M8 n3 nn n1 n1 MOD2 w=55u l=5u M7 n3 n7 n8 n8 MOD1 w=115u l=5u Cc n7 n3 1p CL n3 0 10p *fuente de corriente iss nn n8 2.5uA *Fuentes de alimentación y excitación VDD n1 0 DC 2.5 VSS n8 0 DC -2.5 Vinp n4 0 DC 0 Vinn n5 0 DC 0 .control DC vinp -2.5 2.5 .1 plot v(n3) .endc *2-MICRON MOSIS SPICE LEVEL 2 PARAMETERS [BAKER APENDICE A] .MODEL MOD1 NMOS + (LEVEL=2 VTO=0.8756 LAMBDA=2.9330E-02 KP=4.5494E-05) .MODEL MOD2 PMOS + (LEVEL=2 VTO=-0.8889 LAMBDA=4.2290E-02 KP=1.5035E-05) .end	Output Swing M5 nn nn n1 n1 MOD2 w=12.5u l=5u M6 n2 nn n1 n1 MOD2 w=12.5u l=5u *Par Diferencial M1 n6 n5 n2 n2 MOD2 w=92u l=5u M2 n7 n4 n2 n2 MOD2 w=92u l=5u M4 n7 n6 n8 n8 MOD1 w=12.5u l=5u M3 n6 n6 n8 n8 MOD1 w=12.5u l=5u *Amplificador de salida M8 n3 nn n1 n1 MOD2 w=100u l=5u M7 n3 n7 n8 n8 MOD1 w=180u l=5u Cc n7 n3 2.72p CL n3 0 10p *fuente de corriente iss nn n8 2.2uA *Fuentes de alimentación y excitación VDD n1 0 DC 2.5 VSS n8 0 DC -2.5 Vinp n4 0 DC 0 Vinn n5 0 DC 0 .control DC vinp -2.5 2.5 .1 plot v(n3) .endc *2-MICRON MOSIS SPICE LEVEL 2 PARAMETERS [BAKER APENDICE A] .MODEL MOD1 NMOS + (LEVEL=2 VTO=0.8756 LAMBDA=2.9330E-02 KP=4.5494E-05) .MODEL MOD2 PMOS + (LEVEL=2 VTO=-0.8889 LAMBDA=4.2290E-02 KP=1.5035E-05) .end

T11.- Netlist for Output Swing simulation.

Before	After
	

G11.- Response of Output Swing before and after simulation

References:

[1] "FormatSpiceFile.m" converts .csv files to .txt, http://iteso.mx/~erayas

[2] Dr. José Ernesto Rayas, "Circuit Design using Classical Optimization Methods" Pp: 6-8, http://iteso.mx/~erayas

[3] Allen Phillip E., Holberg Douglas R.; "CMOS Analog Circuit Design", Second edition. Oxford, (1)Pp: 271, (2)Pp: 317, (3)Pp: 315

[4] Baker R.J., Boyce D.E.; "CMOS Circuit Design, Lay out and simulation"; IEEE Press, 1998,