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1.5 GHz Fully Differential Folded Cascode CMOS OTA

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A novel circuit simulation for fully differential folded cascode (FDFC) CMOS operational transconductance amplifier (OTA) is presented. The proposed (FDFC) OTA provides sufficiently large gain-bandwidth product with approximately 1.5 GHz at low values of load capacitor. The large dc gain, high slew rate, low settling time coupled with low power consumption around 3.25 mW are attractive features of the proposed scheme. The circuit exhibits slightly higher harmonic distortion (HD) which can be reduced using source degeneration resistor technique. The simulation results are included.

Keywords: OTA, circuit simulation, 0.5 μm CMOS, fully differential folded cascode technique.

1 INTRODUCTION

Modern wireless and wire line communication systems require high-performance analog base-band circuits. The trends for modern communication systems are higher data rate, large bandwidth and high linearity which are required for analog front-end circuits and analog filters as well [1]. When it comes to high frequency applications coupled with electronic tenability operational transconductance amplifiers (OTAs) have proven to be the best candidate for implementation continuous time filters [2]. The major disadvantage of OTAs is the large harmonic distortion caused by the nonlinear behavior of the CMOS transistors [2]. Harmonic distortion (HD) is undesirable in most signal processing applications including audio and video systems. High-quality audio products such as compact disc (CD) players require a THD

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of about 0.01% (-60 dB) [3]. Several fundamental issues, trade-offs exist when selecting an optimal architecture for the operational trans-conductance amplifier (OTA) [4]. The advent of deep submicron technologies enable increasingly high speed circuits, but makes designing high DC gain OTAs more difficult [5]. The primary advantage of a single stage folded cascode OTA is that the frequency response and settling time can be improved, due to elimination of phase shift of the extra stage, in addition to this power dissipation is also reduced [6].The folded cascode OTA is designed to be fully differential for a number of reasons. This doubles the effective output swing and the amount of current available for slewing. Because the signal power quadruples while the noise power only doubles, the dynamic range is also doubled. Moreover, fully differential circuits have been shown to effectively attenuate even-order harmonic distortion, substrate noise, supply noise, and common mode disturbances. One drawback in adopting a fully differential amplifier is the amplifier need for common-mode feedback circuits [4]. These design requirements have been addressed in literature [1,2,4–11]. Some of the proposed designs enhance high frequency performance of OTAs with out any improvement in linearity [4–6,11], however any effort to achieve the required linearity results in increase in the circuit complexity [7–11]. In the available literature new OTA circuits for high frequency signal processing applications are proposed. These schemes use various techniques to enhance linearity of OTAs such as feed-forward linearized technique, Nedungadi-Visvanathan input cell, Krummenacher's input circuit, and cross coupled input circuit [7,8]. Source degeneration resistor technique , nonlinearity cancellation techniques and cross-coupled differential pair source degeneration resistors are also used [1–3]. These papers used different architectures for OTAs which employ extra complex circuits to enhance, gain bandwidth product (GBW), DC gain, and linearity for high frequency signal processing applications.

This paper present a novel design technique of fully differential folded cascode (FDFC) CMOS OTA using simple circuit of common mode feedback circuit (CMFB) [3] connected to tail current to stabilize output voltage with no effect on performance of OTA in high frequency operation. In addition using source degeneration technique to reduce harmonic distortion (HD). Measurement results for 0.5 μm CMOS implementation of these OTAs are included. Their performance are compared with the existing designs available in the literature [1–11].

2 DESIGN OF FULLY DIFFERENTIAL FOLDED CASCODE (FDFC) CMOS OTA

Figure 1 shows the architecture of an Operational Transconductance Amplifier (OTA) called fully differential folded cascode (FDFC) CMOS OTA. This OTA uses cascoding in the output stage combined with an unusual implementation

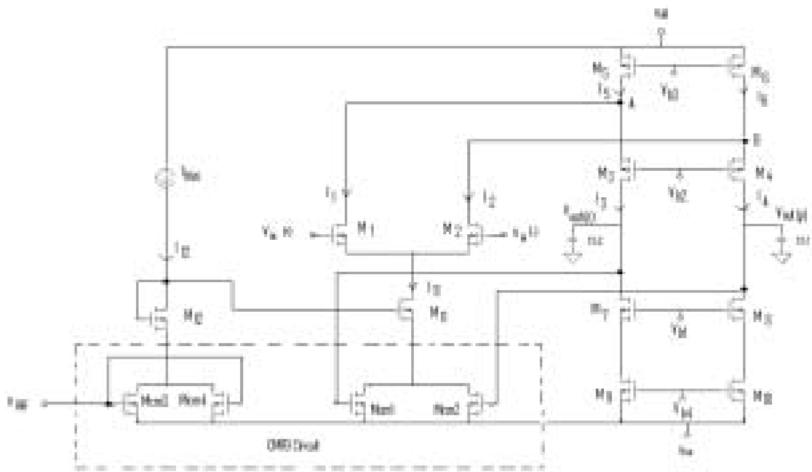

FIGURE 1
Circuit schematic of fully differential folded cascode CMOS OTA without source degeneration resistors.

of the differential amplifier to achieve good input common-mode range. Thus, the folded cascode OTA offers self-compensation, good input common-mode range, and the gain of a two-stage OTA [12]. The (FDFC) OTA does not require perfect balance of currents in the differential amplifier because excess dc current can flow into or out of the current mirror. Because the drains of M_1 and M_2 are connected to the drains of M_5 and M_6, the positive input common-mode voltage of Figure 1 is achieved [12]. With the bias current and overdrive voltage of each transistor is known, we can easily determine the aspect ratios from

$$I_D = (1/2)\mu C_{OX}(W/L)(V_{GS} - V_{TH})^2 \tag{1}$$

To minimize the device capacitances, we choose the minimum length for each transistor, obtaining a corresponding width. The design has thus far satisfied the output swing, power dissipation, and supply voltage specifications [3]. Let us now calculate the maximum output voltage swing of the FDFC CMOS OTA in Figure 1, where $M_5 - M_{10}$ represents current sources with proper choice of V_{b1} and V_{b2}, the lower end of the swing is given by

$$V_{SS} + V_{OD3} + V_{OD5}$$

and the upper end by

$$V_{DD} - (V_{OD5} + V_{OD3} + (|V_{OD7} + V_{OD9}|).$$

We now determine the small-signal voltage gain of FDFC CMOS OTA. The voltage gain is given by:

$$|A_v| = G_m R_{out}.$$

where G_m and R_{out} represents the transconductance and output resistance of FDFC CMOS OTA respectively. We must calculate G_m and R_{out}. The output short-circuit current is approximately equal to the drain current of M_1 because the impedance seen looking into the source of M_3, that is, $(g_{m3} + g_{mb3})^{-1}//r_{O3}$ is typically much lower than $r_{O1}//r_{O5}$. Thus, $G_m \approx g_{m1}$. To calculate R_{out}, we use $R_{OP} \approx (g_{m7} + g_{mb7})r_{O7}r_{O9}$, which gives $R_{out} \approx R_{OP}//[(g_{m3} + g_{mb3})r_{O3}(r_{O1}//r_{O5})]$.

It follows from [3].

$$|A_v| \approx g_{m1}[[(g_{m3} + g_{mb3})r_{O3}(r_{O1}//r_{O5})]//[(g_{m7} + g_{mb7})r_{O7}r_{O9}]] \quad (2)$$

The frequency response of the folded-cascode OTA in Figure 1 is determined primarily by the output dominant pole which is given from [12] as.

$$p_{out} = \frac{-1}{R_{out}C_{out}} \quad (3)$$

where C_{out} is the total capacitance connected from the output of the OTA to ground. The success of the output pole being dominant depends on the fact that there are no other poles whose magnitude is less than GBW which is given as

$$GBW = \frac{g_{m1,2}}{C_L} \quad (4)$$

where $g_{m1,2}$ represent the input transconductance of folded-cascade OTA. The non dominant poles are located at node A and B which are given as

$$p_{A,B} = \frac{-g_{m3,4}}{C_p} \quad (5)$$

where $g_{m3,4}$ is the transconductance of the common gate transistorss (M_3, M_4), and C_p is the total parasitic capacitance at the source of the common gate transistors [12]. Slew rate is given as

$$SR = \frac{I_{bias}}{C_L} \quad (6)$$

where I_{bias} is represents the bias current.

The power supply rejection ratio of the folded-cascode OTA has been greatly improved over the two-stage op-amp. The negative power supply-ripple is transferred directly to the gates of M_{11}, M_7, M_8, M_9, and M_{10}. Here a slightly different approach is made to calculate the PSRR. In this case, we will find the transfer function from the ripple to the output rather than the PSRR. We know that for good PSRR, this transfer function should be small. The transfer function V_{out}/Vss can be found as

$$\frac{V_{out}}{V_{ss}} \approx \frac{sC_{gd8}R_{out}}{sC_{out}R_{out} + 1} \quad (7)$$

The positive power-supply injection is similar to the negative power supply injection the ripple appears at the gates of M_5, M_5, M_3,and M_4.The primary source of injection is through the gate-drain capacitor of M_4, which is the same situation as for the negative power supply injection [12].

2.1 Common-mode feedback circuit (CMFB)

In high-gain amplifiers, the output Common Mode (CM) level is quite sensitive to device properties and mismatches and it cannot be stabilized by means of differential feedback. Thus, a common-mode feedback network must be added to sense the CM level of the two outputs and accordingly adjust one of the bias currents in the OTA. We now apply technique of comparing the measured CM level with a reference and returning the error to the OTA's bias network [3]. The CMFB circuit connected to the current sources of OTA suffers from several drawbacks. First, the value of the output CM voltage level is a function of device parameters. Second, the voltage drop across output resistors of CMFB circuit limits the output voltage swings. To minimize this voltage drop, MOS transistors should work in triode region which represents the output resistors of CMFB with high aspect ratio. The capacitive effect of CMFB of OTA in high frequency operation is thus neutralized [3]. We now introduce a modification to the previous technique which makes the output level relatively independent of device parameters and lowers the sensitivity to the value of biasing voltage of tail current source transistor. The idea is to define biasing voltage of tail current source by a current mirror arrangement such that I_{bias11} "track" I_{12} and V_{REF} of CMFB circuit. For simplicity we suppose that $(W/L)_{11} = (W/L)_{12}$ and $(W/L)_{\mathrm{CM}3,4} = (W/L)_{\mathrm{CM}1,2}$. Thus $I_{bis11} = I_{bias}$ only if $V_{out,\mathrm{CM}} = V_{\mathrm{REF}}$. In other words, the circuit produce an output CM level equal to a reference but it requires no resistors in sensing $V_{out,\mathrm{CM}}$ [3].

2.2 Biasing circuit

In the OTA of Figure 1, the input CM level and the bias voltages must be chosen so as to allow maximum output swing. The minimum allowable CM level equals $V_{GS1} + V_{OD11} = V_{TH1} + V_{OD1} + V_{OD11} = 1.42\,\mathrm{V}$. The minimum value of $V_{b1} = V_{SS} + V_{GS7} + V_{OD9} = -1.43\,\mathrm{V}$. Similarly, $V_{b2} = V_{DD} - (|V_{GS3}| + |V_{OD5}|) = 1.12\,\mathrm{V}$, $V_{b4} = V_{G9} = V_{GS9} - V_{S9} = V_{OD9} + V_{TH9} - V_{SS} = -1.7\,\mathrm{V}$, and $V_{b3} = V_{G5} = V_{GS5} - V_{S5} = V_{DD} - V_{OD5} + V_{TH5} = 1.42\,\mathrm{V}$. We can Use simple voltage divider circuit to produce these voltages [13]. Where V_{OD1}, V_{OD5}, V_{OD9}, and, V_{OD11} represents over drive voltages of M_1, M_5, M_9, and M_{11} respectively. V_{DD} and V_{SS} represents supply voltage. Table 1 presents gate dimension and biasing currents of FDFC CNOS OTA. Table 1 presents a gate dimension, overdrive voltage (V_{OD}), and biasing currents of FDDC CMOS OTA.

3 HARMONIC DISTORTION OF FDFC CMOS OTA

The conventional input stage for an OTA circuit is the differential pair of Figure 1.

Transistors no.	W (μm)	L (μm)	Biasing Current (μA)	Overdrive Voltage (V)
M_1, M_2	12.0	0.5	50.0	0.16
M_3, M_4	16.1	0.5	50.0	0.3
M_5, M_6	11.59	0.5	100.0	0.5
M_7, M_8, M_9,M10	6.21	0.5	50.0	0.225
M_{11},M12	2.51	0.5	100.0	0.5
M_{cm1}, M_{cm2}, M_{cm3}, M_{cm4}	0.49	1.0	50.0	0.63

TABLE 1
Gate dimension and biasing currents of FDFC CMOS OTA

If we ignore the channel length modulation and body effect of MOSFETs, the current voltage relationship is given by

$$I_1 = \frac{\mu C_{OX}}{2}\left(\frac{W}{L}\right)_1 [V_{GS1} - V_{TH1}]^2 \tag{8}$$

$$I_2 = \frac{\mu C_{OX}}{2}\left(\frac{W}{L}\right)_2 [V_{GS2} - V_{TH2}]^2 \tag{9}$$

Differential input signal can be defined as,

$$\Delta V_1 = V_{in}(+) - V_{in}(-) = V_{GS1} - V_{GS2} \tag{10}$$

If we combine the equations (2) and (3) we achieve,

$$\Delta I = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)\Delta V_1\sqrt{\frac{2I_{bias}}{\mu C_{OX}\left(\frac{W}{2L}\right)} - (\Delta V_1)^2} \tag{11}$$

or

$$\Delta I = g_{m1}\Delta V\sqrt{1 - \left(\frac{\Delta V_1}{2V_{OD1}}\right)^2} \tag{12}$$

Where V_{GS} is the gate to source voltage, V_{TH} is the threshold voltage, ΔI is the dc drain current, and g_{m1} and V_{OD1} are the transconductance and overdrive voltage of the input transistors, respectively.

The equation (11) is valid only for the signals that are,

$$\Delta V_1 \le \sqrt{\frac{2I}{\mu C_{OX}\left(\frac{W}{L}\right)}} \tag{13}$$

But if the input signal is larger than this limit, the conductivity of one the input MOSFETs become larger than the other and current from this MOSFET becomes $\Delta I = I_{bias}$.

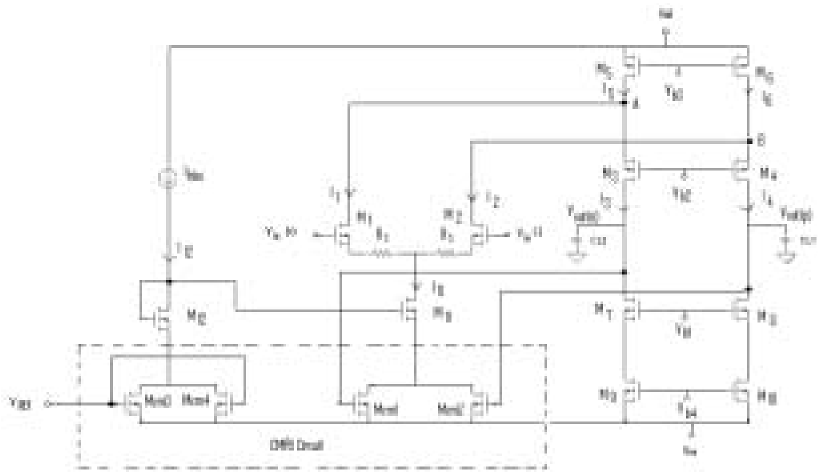

FIGURE 2
Circuit schematics of fully differential folded cascode CMOS OTA with source degeneration resistors Rs.

Expanding (12) in Taylor series and considering only the first terms, we have

$$\Delta I = g_{m1}\Delta V_1 - \frac{g_{m1}}{8V_{OD1}^2}V_{OD1}^3 \tag{14}$$

The fully differential OTA with source degeneration shown in Figure 2 have been used to achieve high linearity and high-frequency operation.

If we add the source degeneration resistor Rs and mobility degeneration (R_θ) effects, it can be shown that the differential output current can be approximated as [1],

$$\Delta I = \left(\frac{g_{m1}}{1+N_r}\right)\Delta V_1 - \frac{1}{8}\left(\frac{g_{m1}}{V_{OD1}^2(1+N_r)^3}\right)\Delta V_1^3 \tag{15}$$

where $V_{OD1} = V_{GS1} - V_{TH1}$, $N_r = g_{m1}(Rs + R_\theta)$. From (15), the low-frequency small-signal transconductance G_m, and HD_3 for differential pair with source degeneration yield

$$G_m = \frac{g_{m1}}{1+N_r} \tag{16}$$

$$HD_3 = \frac{\Delta V_{pk}^2}{32}\left|\frac{\frac{g_{m1}}{V_{OD1}^2(1+N_r)^3}}{\frac{g_{m1}}{1+N_r}}\right| \tag{17}$$

Where ΔV_{pk}^2 is the peak value of the differential input signal. Observe from (16), and (17) that the small signal transconductance inverse proportional to the input transconductance, and the HD_3 is proportional with the input transconductance g_{m1}, overdrive voltage of input transistors V_{OD1}, and source degeneration factor N_r [1]. The derivation of (17) dose not consider frequency-dependent parasitic capacitance effect, especially those at the source of input transistors M_1, and M_2. If we consider these capacitors, and frequency dependent harmonic distortion. an approximated analytical expression of the frequency dependent third order harmonic distortion yields

$$HD_3 = \frac{\Delta V_{pk}^2}{32} \frac{g_{m1}}{V_{OD1}^2(1+N_r)^3} \times \left| \frac{\left(\frac{N_r}{1+N_r}\right)\frac{3w}{w_{c1}} - 2w\left(\frac{C_{p1}}{g_{m1}}\right)}{\frac{g_{m1}}{1+N_r}} \right| \tag{18}$$

This expression shows that the third order harmonic distortion increases proportionally to the frequency of operation, and the parasitic capacitors in parallel with source degeneration resistors reduce the overall degeneration factor, thus increasing the harmonic distortion component at high frequencies [1].

4 MEASUREMENT RESULTS AND PERFORMANCE COMPARISON OF FDFC CMOS OTA WITHOUT SOURCE DEGENERATION RESISTORS AND FDFC CMOS OTA WITH SOURCE DENEGATION TECHNIQUE

An attractive features of fully differential folded cascode CMOS OTA for high frequency signal processing applications presents in this paper. Table 2, Figure 3(a), and Figure 3(b), shows that when varies load capacitor value of OTA, the performance parameters such as gain bandwidth product (GBW),

C_L (pF)	DC gain (dB)	GBW (MHz)	Phase margin degree	Settling time (nS)	HD_3 (dB)	$\%HD_3$
10.0	64.3	8.5	89.8°	303.0	−25.9	5.0%
8.0	=	10.9	89.7°	239.8	−25.8	5.1%
6.0	=	14.4	89.6°	175.1	−25.0	5.6%
4.0	=	21.2	88.6°	118.2	−23.1	6.9%
2.0	=	42.0	81.2°	49.6	−21.0	8.9%
1.0	=	81.45	79.2°	18.2	−20.6	9.3%
0.5	=	375.1	76.6°	13.1	−19.0	11.2%
0.1	=	726.2	75.7°	4.7	−14.0	19.9%
0.05	=	1.14 GHz	53.7°	2.1	−12.1	24.8%
0.035	=	1.50 GHz	46.5°	1.8	−11.3	27.2%

TABLE 2
GBW, DC gain, settling time, phase margin, and third harmonic distortion of FDFC CMOS OTA without source degeneration technique

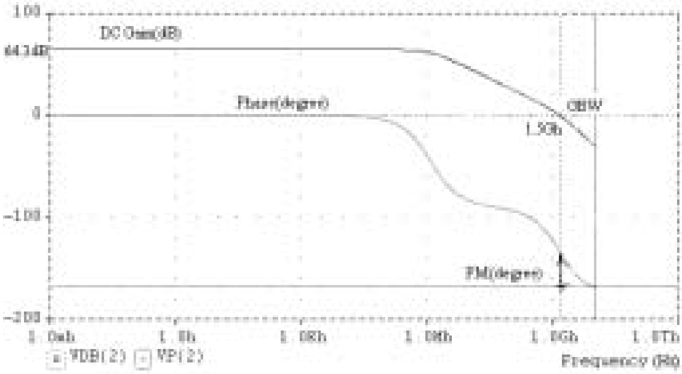

FIGURE 3a
Frequency response (magnitude and phase) of FDFC CMOS OTA without source degeneration technique.

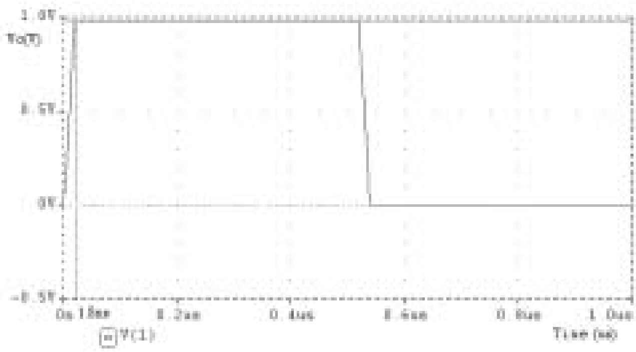

FIGURE 3b
Step response of FDFC CMOS OTA without source degeneration technique.

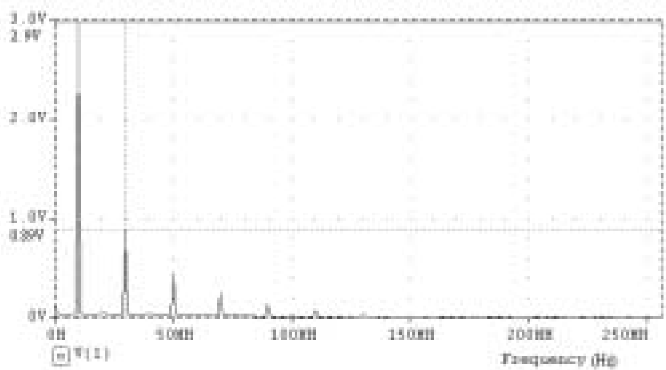

FIGURE 3c
Measured HD_3 of FDFC CMOS OTA without source degeneration technique.

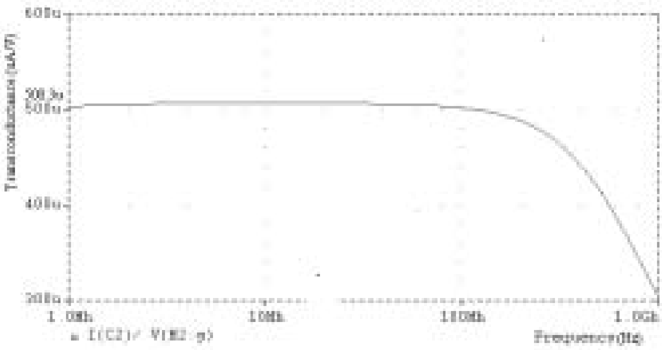

FIGURE 3d
Transconductance of FDFD CMOS OTA without source degeneration technique.

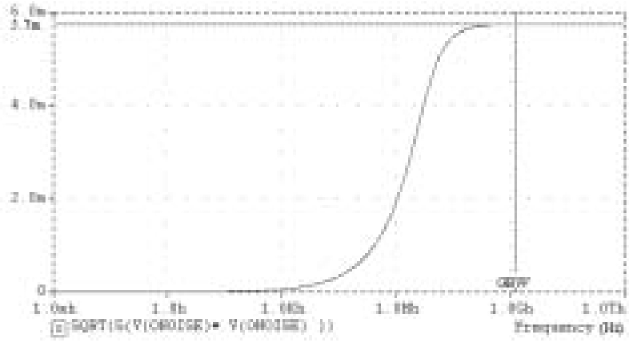

FIGURE 3e
Total output noise of FDFC CMOS OTA without source degeneration technique.

dc gain (DC Gain), and settling time will improve. But the linearity of OTA will decrease due to increasing in gain bandwidth value and parasitic capacitance of MOSFETs in high frequency operation. The measurement value of HD_3 for CMOS OTA without source degeneration value shown in Figure 3(c). Figure 4(a), Figure 4(b), and Table 3 shows that the linearity (third order of harmonic distortion HD_3) of OTA improve due to source degeneration technique. But this improved of linearity of CMOS OTA with sacrifice the other performance parameters GBW, DC Gain, Slew Rate, Settling time, and noise as well as. When compare Figure 3(d) and 4(d) we note that the Transconductance of CMOS OTA will decrease due to used source degeneration technique. These results confirm the conceptual theory of Harmonic Distortion that driven in this paper. Figure 5(a), and Figure 5(b) shows variation of percent third order harmonic distortion (%HD_3) and Transconductane of CMOS OTA with source degeneration resistor. We note that the (%HD_3) and transconductance of CMOS OTA will decrease due to using this technique.

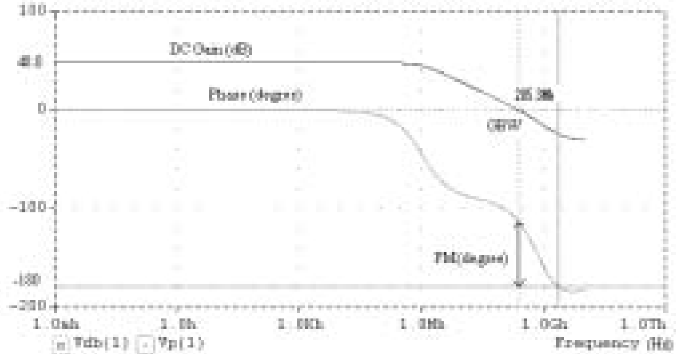

FIGURE 4a
Frequency response (magnitude and phase) of FDFC CMOS OTA with source degeneration technique.

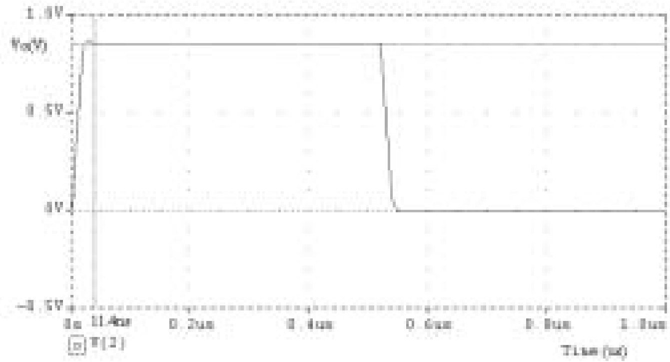

FIGURE 4b
Step response of FDFC CMOS OTA with source degeneration technique.

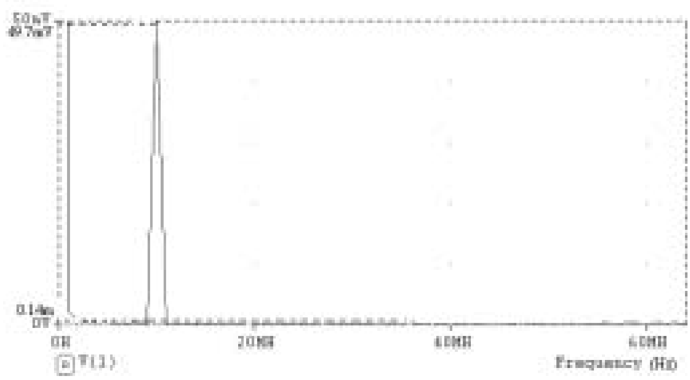

FIGURE 4c
Measured of HD3 of FDFC CMOS OTA with source degeneration technique.

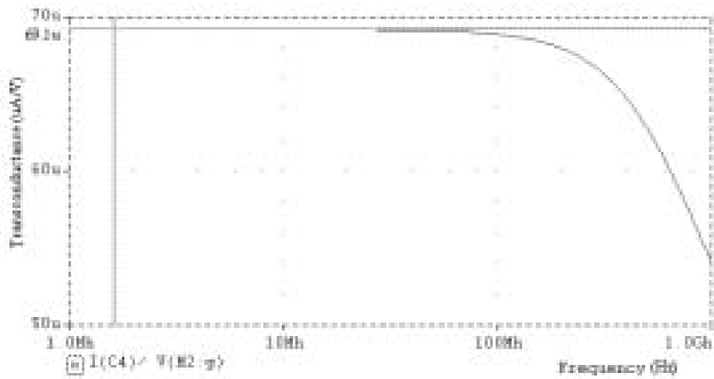

FIGURE 4d
Transconductance of FDFC CMOS OTA with source degeneration technique.

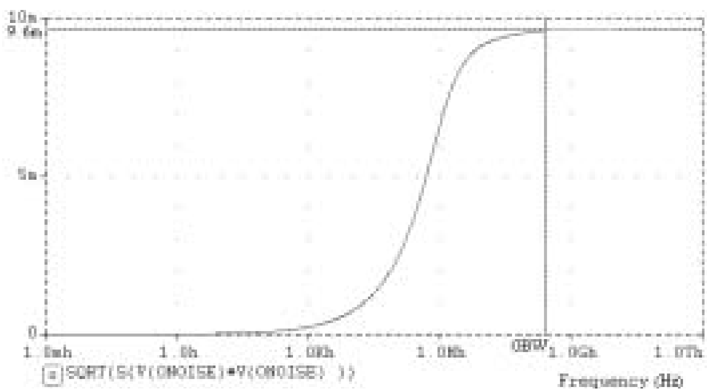

FIGURE 4e
Total output noise of FDFC CMOS OTA with source degeneration technique.

5 CONCLUSIONS

A 1.5 GHz gain bandwidth product, large dc gain, high slew rate, and low settling time fully differential CMOS OTA has been designed in a 0.5 μm process. Source degeneration technique have been adopted to minimize harmonic distortion for a given performance level. Additionally, to make the output of fully differential OTA stabilize for dc variation, a simple common mode feedback network are used. There is a trade off between linearity and gain-bandwidth product (GBW), dc gain (DC Gain), and noise. These parameters are decreased due to improvement in linearity of CMOS OTA, when source degeneration resistor are used. In addition signal to noise ratio (S/N) is also increased. However transconductance of proposed CMOS OTA is slightly

C_L (pF)	DC gain (dB)	GBW (MHz)	Phase margin (degree)	Settling time (nS)	HD_3 (dB)	$\%HD_3$
10.0	48.0	1.1	91.2°	495.8	−64.8	0.05%
8.0	=	1.4	91.2°	490.9	−61.2	0.08%
6.0	=	1.8	91.1°	449.6	−58.1	0.12%
4.0	=	2.9	90.0°	386.8	−56.0	0.15%
2.0	=	5.2	89.9°	194.7	−51.7	0.26%
1.0	=	11.7	89.3°	112.3	−44.6	0.58%
0.5	=	21.7	88.6°	65.3	−36.4	1.5%
0.1	=	112.0	80.7°	22.17	−33.3	2.1%
0.05	=	221.0	73.4°	14.3	−31.3	2.7%
0.035	=	248.9	66.7°	11.2	−29.8	3.2%

TABLE 3
GBW, DC gain, settling time, phase margin, and third harmonic distortion of FDFC CMOS OTA with source degeneration technique

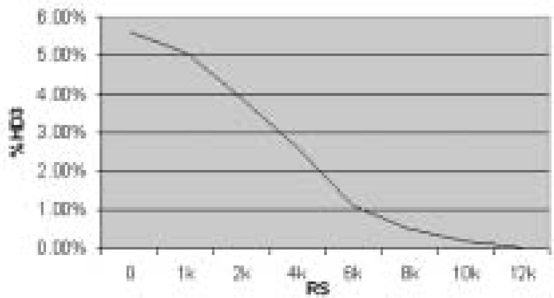

FIGURE 5a
Variation of % HD_3 with source degeneration resistor Rs.

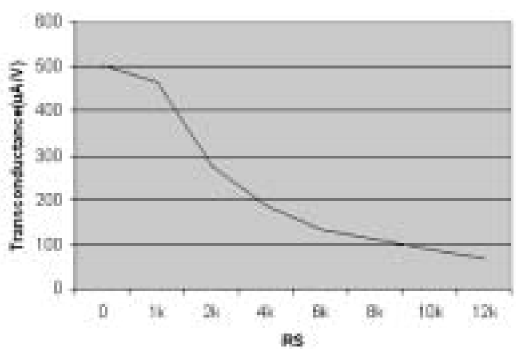

FIGURE 5b
Variation of source degeneration resistor Rs with trasconductance of OTA.

Rs(KΩ)	GBW (MHz)	DC gain (dB)	Transconductance (μA/V)	%HD_3
0.0	8.5	64.3	503.0	5.6%
1.0	5.2	61.0	463.0	5.1%
2.0	3.8	58.6	273.4	3.9%
4.0	2.5	55.2	158.8	2.6%
6.0	1.9	52.8	133.4	1.1%
8.0	1.5	50.9	111.2	0.5%
10.0	1.3	49.3	89.2	0.19%
12.0	1.1	48.0	69.1	0.05%

TABLE 4
Source degeneration resistor (Rs), GBW, DC gain, transconductance of OTA, and percentage of third harmonic distortion

Parameters	CMOS OTA in Figure 1	CMOS OTA in Figure 2
(DC) Gain	64.3 dB	48.0 dB
GBW	1.5 GHz	248.9 MHz
Phase Margin	46.5°	66.7°
Slew rate(+)	48.4 V/μS	39.6 V/μS
Slew rate(−)	−44.7 V/μS	−37.6 V/μS
Settling time	1.8 ns	11.2 ns
Output swing	+2.1 V, −2.4 V	+1.6 V, −2.5 V
HD_3(1 Vpp@10 MHz))	−25.9 dB	−64.8 dB
Dynamic range	30.9 dB	34.9 Db
Total Output Noise	5.7 mV	9.6 mV
$PSRR^+$	74.0 dB	72.0 dB
$PSRR^-$	69.7 dB	69.7 dB
Power consumption	3.25 mW	3.32 mW
Die Area	0.047 mm^2	0.048 mm^2

TABLE 5
The comparison results between the FDFC CMOS OTA without Source degeneration technique and FDFC CMOS OTA with source degeneration technique

decreased by the use of source degeneration technique. In a nutshell it can be concluded that the proposed CMOS OTA is better compared to the earlier CMOS OTA schemes vis-à-vis frequency response and linearity with slightly increased harmonic distortion which in taken care of if source degeneration technique is used.

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