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magisterska

Projekt odczytowej części monolitycznego detektora mozaikowego z aktywnymi komórkami wykonanego w technologii ST 0,13 μm

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Oświadczam, świadomy odpowiedzialności karnej za poświadczenie nieprawdy, że niniejszą pracę dyplomową wykonałem osobiście i samodzielnie i że nie korzystałem ze źródeł innych niż wymienione w pracy.

AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY IN KRAKÓW

ELECTRICAL ENGINEERING
DEPARTMENT OF ELECTRONICS

Master Thesis

Design of the readout part of a Monolithic Active Pixel Sensor in the ST 0.13μm technology

by Paweł Starzyk

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KRAKÓW, SEPTEMBER 2007

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I would like to dedicate this work to my parents.

ACKNOWLEDGMENTS

I am very grateful to my supervisor Prof. Dr hab. inż. Wojciech Kucewicz for his guidance and giving opportunity of realizing this project.

I am very thankful to my advisor in Rome, Dr Eleuterio Spiriti for his patience and understanding throughout this work.

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I take this opportunity to thank Dr Halina Niemiec. She taught me a lot of about detectors.

Contents

ABBREVIATIONS

CMOS	Complementary Metal Oxide Semiconductor
PMOS	Positive Channel Metal Oxide Semiconductor
NMOS	Negative Channel Metal Oxide Semiconductor
MAPS	Monolithic Active Pixel Sensor
SNR	Signal to noise ratio
RMS	Root mean square
CMRR	Common-mode rejection ratio
C_{db}	drain-bulk capacitance
C_{gd}	gate-drain capacitance
C_{gs}	gate-source capacitance
C_n	node capacitance
λ	channel length modulation parameter
C_{ox}	oxide capacitance
t_{ox}	oxide thickness
μ_{0n}	nMOS transistor mobility
μ_{0p}	pMOS transistor mobility
ϵ_o	permittivity of free space
ϵ_o	permittivity of SiO_2
V_{TN1}	threshold voltage of M1 which is NMOS transistor
$A_C(s)$	common-mode frequency response
$A_V(s)$	differential mode frequency response
g_m	channel conductive parameter
V_E	Early voltage

STRESZCZENIE

Praca magisterska “Projekt odczytowej części monolitycznego detektora mozaikowego z aktywnymi komórkami wykonanego w technologii ST 0,13 μm” jest rezultatem pobytu na Uniwersytecie Roma3 w ramach programu Sokrates-Erasmus. Autor wziął udział w projekcie, którego celem było opracowanie i wykonanie nowych detektorów MAPS.
Zadaniem autora było opracowanie odczytowej części detektora, na którą składały się dekodery kodu Graya i wzmacniacz wyjściowy.

Dekodery kodu Graya miały na celu konwersję sygnału wejściowego będącego kodem Graya na licznik z krążącą jedynką. Dało to możliwość wyboru jeden po drugim kolejnych wierszy matrycy komórek i ich resetowanie lub odczytywanie. Ponieważ zmiana wierszy miała odbywać się z częstotliwością 10MHz, zatem czas narastania mógł stanowić znaczny procent ze 100ns przewidzianych na resetowanie(odczytywanie) jednej komórki. Dlatego też zdecydowano się dla prawie każdej matrycy użyć, oprócz klasycznego licznika z krążącą jedynką, dekodera w którym co 100ns wybierana jest kolejna cela, ale stan wysoki na niej trwa przez 200ns (jednocześnie dwie sąsiednie komórki są w stanie wysokim).
Matryce komórek różniły się między sobą:

- liczbą celi: 32×32, 64×64, 128×128
- wielkością celi: $10\mu m \times 10\mu m$, $20\mu m \times 20\mu m$, $25\mu m \times 25\mu m$
- napięciem zasilania: $1,2V$ lub $2,5V$

Z kombinacji powyższych parametrów powstało 16 matryc komórek, dla których należało zaprojektować dekodery. I były to w większości przypadków po dwa typy dekoderów dla każdej matrycy. Oprócz sygnałów wejściowych będących kodem Graya potrzebny był także sygnał:

- Enable - wybór matrycy dekoderów
- ON/OFF - wybór typu wykorzystywanego dekodera w danej chwili

Wymiary dekoderów powinny być tak małe jak tylko reguły projektowe na to pozwalają. Niezbędne było wykonanie symulacji, pozwalające ocenić, czy rezystancje i pojemności linii łączących dekodery z komórkami nie stanowią przeszkody w poprawnym działaniu dekoderów.

Na wyjściu sygnału z każdej matrycy detektorów należało umieścić wzmacniacz operacyjny zapewniający wysoką impedancję i odseparowujący układ odczytu komórki od wyjścia układu scalonego . W tym celu wybrano wzmacniacz w konfiguracji nieodwracającej. Kolejną funkcją wzmacniacza było wzmocnienie napięciowe $2 \div 3$ sygnału wejściowego, co zostało wykonane przez odpowiedni dobór rezystorów stanowiących zamkniętą pętlę wzmacniacza. Należało zaprojektować wzmacniacz dla napięcia wejściowego $0,1V \div 0,8V$. Tak duża rozbieżność przewidywanego poziomu sygnału wejściowego związana była z nieznaną wartością prądu upływu na diodzie i tranzystorach komórki w używanej nowej technologii ST 0,13μm. Pojemność wyjściowa wzmacniacza równa była 10pF, gdyż wyjście wzmacniacza było jednocześnie wyjściem układu scalonego. Częstotliwość zmian sygnału wejściowego ustalono na 10MHz. Pomimo istnienia wielu matryc komórek, dla każdej z nich taki sam wzmacniacz mógł być użyty.

Po obliczeniach i symulacji wielu konfiguracji wzmacniacza, m.in. wzmacniacza z zawiniętą kaskodą, autor zdecydował się użyć dwustopniowego wzmacniacza z pojemnością kompensującą. Wymiary tranzystorów i wartość pojemności zostały wyliczone a wyniki symulacji zostały porównane z obliczeniami. Wzmacniacz spełniał założenia a symulacje Monte Carlo nie dały żadnych argumentów, iż wzmacniacz mógłby nie działać po fabrykacji.

Następnie autor szukał sposobu zaprojektowania wzmacniacza o podobnych wymiarach ale lepszych parametrach, tak aby praca ze wzmocnieniem 5 była możliwa. Rozwiązaniem okazało się zastosowanie bufora na wyjściu wzmacniacza, zmniejszającego pojemność obciążającą wzmacniacza. Jako bufor wyjściowy został użyty wtórnik źródłowy na tranzystorach PMOS. Nie odwraca on fazy a jego wzmocnienie jest nieco mniejsze od jedności. Wtórnik zmniejszał pojemność obciążającą wzmacniacza z 10pF do $1pF \div 5pF$ i dla tak zdefiniowanego obciążenia, dwustopniowy wzmacniacz został jeszcze raz zaprojektowany. Dodatkowo wykorzystując bramkę transmisyjną autor umożliwił wybór wzmocnienia spośród wartości: 2x lub 5x. Wzmocnienie 5-krotne będzie używane, jeśli okaże się, iż prąd upływu nie jest duży i tym samym zmiana napięcia wejściowego jest mniejsza od założonej $0.1V \div 0.8V$. Wzmacniacz z buforem wyjściowym także został poddany symulacjom Monte Carlo, z równie dobrym skutkiem jak dla pierwszego wzmacniacza.

Przyjęte przez autora założenia zostały w pełni zrealizowane. Dekodery i wzmacniacz wyjściowy zostały zaprojektowane, przesymulowane i będą stanowiły integralną część projektowanego nowego detektora MAPS.

Chapter 1

HISTORY AND TYPES OF SILICON DETECTORS

A silicon detector is a matrix of reverse polarized diodes. The idea of that kind of detector was born in the 1950s, but the first detectors were fabricated in the 1970s and nowadays are irreplaceable if a precision of measurement energy, time or position is crucial.

In scientific experiments (especially in the High-Energy Physics projects) tracking and vertex detectors are used. The features of an ideal detector are: [2]

- noiseless
- 100% quantum efficiency
- perfectly uniform response
- unlimited dynamic range

Detectors have to:

- register high energy particles
- be produced in a cheap technology because it is a niche market
- have good radiation hardness

Of course the ideal detector does not exist. That is the reason why many types of detectors are available. Detectors can be divided into two groups:

1. Strips Detectors - one- or two-dimensional position resolution with external readout electronics
2. Pixel(Mosaic) Detectors - two-dimensional position resolution

In this chapter the most popular Pixel Detectors are described.

1. ***Hybrid Pixel Detectors*** [9]

   The first Mosaic Detector discussed is a Hybrid Pixel Detector.

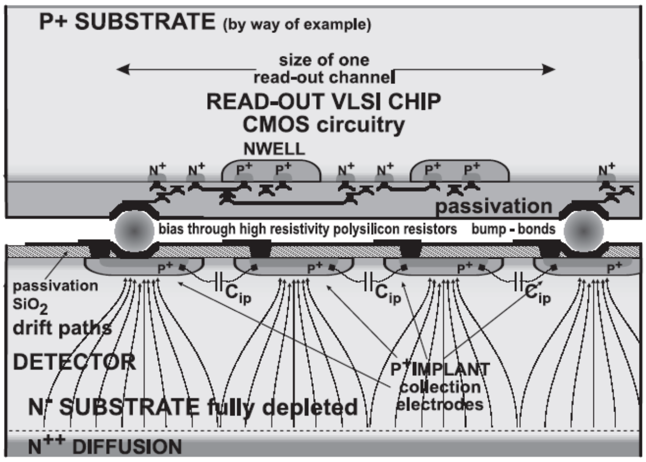

Figure 1.1: A cross section view of a Hybrid Pixel Detector: detector chip (bottom) bump bonded to the readout chip (top)[9]

   As it is expressed in Figure 1.1, the bump bonding process connects the detector chip to the output device. This bump bonding is difficult, makes it expensive to decrease dimensions of the pixels and is a limitation for adopting Hybrid Pixel Detectors in the future scientific applications.

2. ***Charged Coupled Devices*** [16]

   The development of CCD detectors began in the 1970s and was driven by their use as photon detectors in the visible band. These were also successfully used in High Energy Physics applications in the CERN.

   In the end of columns of pixels on the sensor there is a storage column. The sensor integrates a frame of data and after that quickly transfers it to the storage column, where it is shifted one row as shown in Figure 1.2. The data next are readout during a horizontal shift readout register. [8]

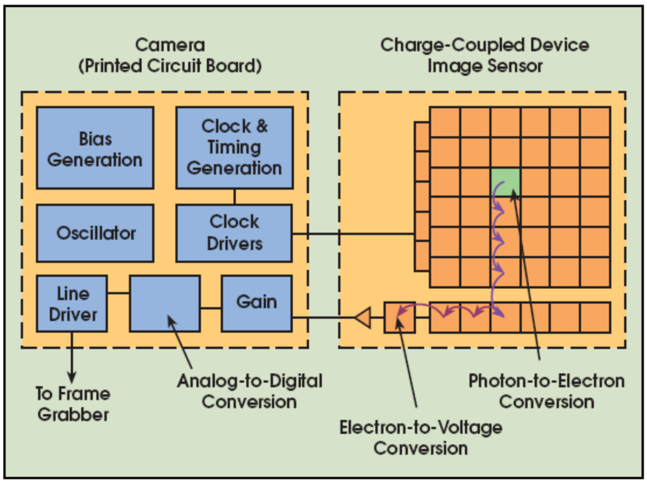

Figure 1.2: Scheme of CCD detector: detector chip (right) connected to the readout chip (left)[21]

The main advantage was very high spatial resolution. CCD does not experience any dead zone or any dead time and are continuously sensitive to the radiation. The main disadvantage is that this requires a long time for a readout. In big CCD matrices the readout time of the whole detector can be even few milliseconds because the charge has to be serially shifted under one gate to the next across the columns and rows of the pixel matrix. The next weak point of CCD detector is their poor radiation hardness. Due to the technological limitations, on the pixel there is only charge to voltage conversion and the rest of processing is implemented on the separated chip which is the next disadvantage.

3. ***Monolithic Pixel Detectors***

The main advantage of Monolithic Pixel Detectors is to integrate the detector and readout electronics on the same substrate. It gives possibility to make a thin and compact detector.

Silicon on Insulator(SOI) detector

Silicon on Insulator detector is the example of Monolithic Pixel Detector. SOI wafers for detectors are fabricated in some different, non standard and complicated technologies. In Figure 1.3 three layers are shown:

(a) high resistive($> 4k\Omega/cm$), 400μm thin layer in which diode is implemented

(b) isolated burried oxide layer, 1μm splitted detector layer and readout layer

(c) thin($1.2\mu m$), low resistive, readout layer

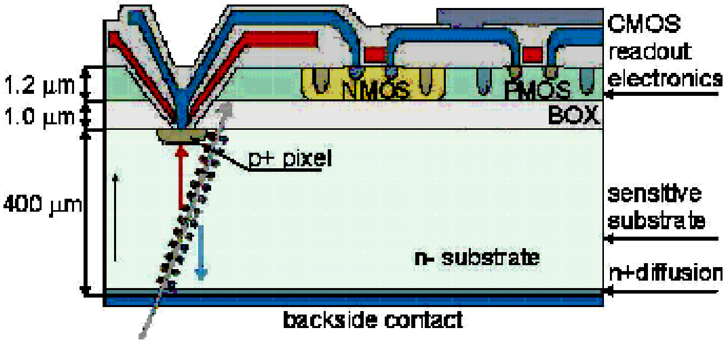

Figure 1.3: Cross section view of the SOI detector: detector part (bottom) and readout part (top)[1]

These detectors were designed and fabricated in Poland. The only one disadvantage is a non standard, dedicated technology.

The most important advantages are: fully depleted detector layer which gives high Signal Noise Ratio(SNR), good sensitivity and possibility of using both types of transistors (in MAPS detectors only nMOS transistors are used).

DEPFET (DEpleted P-channel Field Effect Transistor) detector [10]

In order to increase SNR, DEPFET detector was proposed. It is a charge sensing element for charged particle detection with the first amplification stage built into pixel.

DEPFET detector includes a p-channel JFET element integrated on a high resistivity material as it is shown in Figure 1.4. In the bulk, the buried n-type implant is created, which is the second, internal gate. As a result of a particle passage the electrons are liberated and next are in the internal gate collected. The collected electrons change the gate potential and as a result modify a current channel of the JFET transistor.

The collected electrons need to be cleared which is done by biasing a clearing electrode and the collected charge is transferred into the clearing electrode. Next the charge is carried away.

This detector has a very good SNR parameter. The advantage is small power consumption - because power concumption of readout cycles is practically zero,

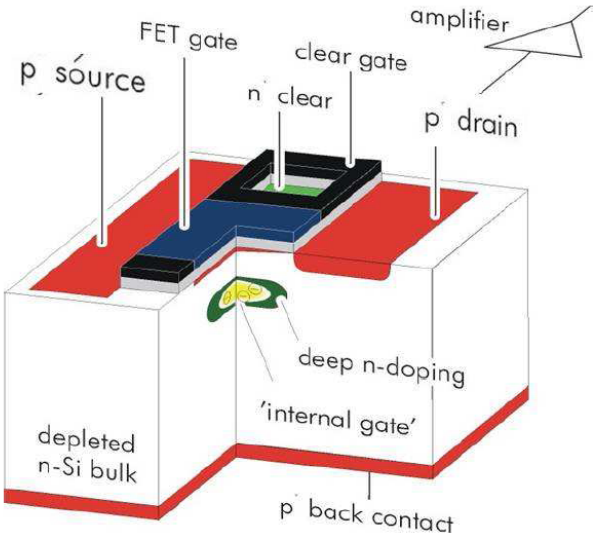

Figure 1.4: Cross section view of the DEPFET detector [17]

although the pixels are also sensitive to ionising particles between readout cycles [18]. The next advantage is a fast readout.

The disadvantage is that it is hard to avoid charge collection by the additional circuitry more than by the detection element itself. Also specialised external circuits are needed to readout a DEPFET detector.

Monolithic Active Pixel Sensor(MAPS) detector [11]

Monolithic Active Pixel Sensor is a novel technique for silicon position sensitive detectors. The first MAPS detectors were fabricated in 1999. The sensors are fabricated in a standard CMOS process. The baseline architecture of this technique is similar to a visible light CMOS camera, which has been in common usage recently for digital photography and video applications.

There is one element distinguishing MAPS from classical detectors on a fully depleted and high resistivity substrate. It is a lightly doped undepleted epitaxial layer used as an active volume for the charge collection.

The view of MAPS detector is in Figure 1.5 presented. N well diode on the p-type epitaxial layer is a charge collecting element. Because of the difference in doping levels the p-well and p++ substrate act as reflective barriers and the generated electrons are collected by the n-well - p-epitaxial diode. The epitaxial layer is underneath the readout electronics and that is why fill factor is almost

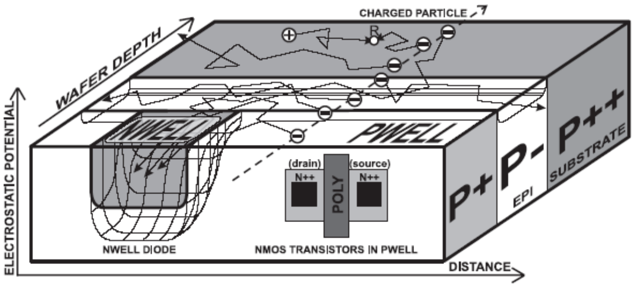

Figure 1.5: Cross section view of the MAPS detector for charged particle tracking [12]

100%.

Advantages of MAPS detectors: [28]

- are made in standard CMOS technology,
  Are used in commercial applications: photography and video applications. It gives assurance that this technology is going to be developed.
- being monolithic,
  MAPS avoid problems related to connections between readout part and detector chip, like bump bonding. Gives opportunity to perform some processing operations independently on each pixel.
- shrinking size of the transistors,
  Pixels can be very small and more functionality can be integrated in the same pixels.
- very low power consumption,
- deep submicron CMOS is radiation resistant.

Active pixel means that the first stage of signal amplification is integrated directly within the pixel area. Active pixel is important because it gives opportunity to perform some processing operations independently on each pixel before the signals are transfered to the common processing blocks outside the pixels.

The above advantages explain why nowadays MAPS technology is becoming the most popular method of producing detector. Also in this project MAPS technology is used.

Chapter 2

PURPOSE OF THE PROJECT

Monolithic Active Pixel Sensors (MAPS) are becoming popular because they use a standard CMOS process which was described in the previous chapter. Their advantages are low cost and integration as one integrated circuit of the whole high speed imaging system. This is the reason why MAPS are used not only in commercial applications like video cameras but also in niche market like scientific applications(High Energy Physics).

The author of this thesis had an opportunity to cooperate in designing the chip for MAPS detector in technology ST $0.13\mu m$ during Socrates - Erasmus scholarship in Rome at Università degli Studi Roma3.

The project is funded by INFN (National Institute of the Nuclear Physics) and developed at Università degli Studi Roma3.

The project leader is Dr Eleuterio Spiriti. He is cooperating with Dr Janusz Mlynarczyk. Also the author of this thesis has contribution to the project which is described in the next chapters.

Generally the signal in the High Energy Physics applications is detected only at a small fraction of the pixel (1%). MAPS detector gives possibility to perform some processing operations on each pixel. The most important challenge in this project is to readout only pixels, in which the signal is registered. It will give chance to increase frequency which is important parameter of detectors.

To obtain these results the new technology ST $0.13\mu m$ is used.

The chip in discussing project includes a few separate pixel matrices. Most of them are only matrices of different kind of diodes to give knowledge about what kind of diode will get us the best results in the future implementations. The rest of matrices include pixels with a system of specification, only the pixel with signal over a defined level will be read out. This allows to reduce strongly the overall readout time.

The goal of this thesis was to design the readout part of MAPS detector in this new technology: gray decoders of different types of detector matrices and an output amplifier.

Different kind of software has been used to design and simulate a chip:

1. Composer

   Part of Cadence Design System. Gives possibility to schematic design. It is necessary to implement libraries with the technology files, in which the device is going to be fabricated.

2. Virtuoso

   It is used to design a layout. Also a part of Cadence Design System

3. Spectre

   It is used in schematic and postlayout simulations. There are a lot of simulations programs but spectre makes possible the most precisely simulation scores.

4. Calibre

   It is supported by Mentor Graphics and is helpful in LVS(Layout Versus Schematic) simulations. The default program for the LVS is Diva mady by Cadence, but using Calibre is easier. Also the algorithm of checking whether the schematic suits to the layout is more precise and it is easier to find wrong elements, layers or connections in the layout. The general idea of working LVS simulators is the same: first the netlist is extracted from the layout; using info generated by the DRC(Design Rule Checker) and then all circuits elements are recognized; after that the netlist of the schematic is compared to the netlist of the layout.

Chapter 3

GRAY DECODER

Gray coder is a system of binary counting in which two adjacent codes differ in only one position as in Table 3.1.

This method of reseting and readout pixels is used because it has a couple of advantages.

Table 3.1: Gray code versus binary and integer code

Integer	Binary	3-bit Gray code
0	000	000
1	001	001
2	010	011
3	011	010
4	100	110
5	101	111
6	110	101
7	111	100

Advantages of gray coding:

1. Gray decoder built on CMOS transistors use less power because in every cycle only one address cell is changing. For CMOS devices the most consuming energy process is switching over transistors.

2. The first and the last value of the coding sequence differ by only one bit. This kind of rotary decoder to reset pixel matrix is needed.

3. When several bits change in the binary representation, a misread can result because of the fact that some bits change before others. In gray decoder only one address bit is changing and therefore a possibility of misread is avoided.

3.1 REQUIREMENTS FOR GRAY DECODER

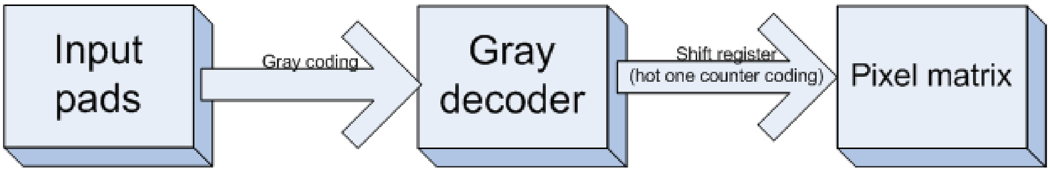

Figure 3.1: Block scheme, method of reseting and reading out pixels

Signals on the input of the detector chip are given as gray code, which is described in the previous section and is presented in Figure 3.1. We are interested in readout or resetting pixels one by one so it is necessary to convert this gray code to the hot one counter coding.

On the chip there are matrices of detectors, which consist of:

- different number of pixels (32x32, 64x64 of 128x128),
- different distance between pixels(10μm, 20μm, 25μm,)
- different power supply (1.2V or 2.5V)

Different decoders are used for every combination of these parameters, as shown in Table 3.2.

3.2 SCHEMATIC

The basic decoder component is an AND structure (NAND structure + INVERTER) in Figure 3.2 and in Figure 3.3. If we want to ensure high signal at the output it is necessary to have high signal at all inputs and then this output line is resetting decoders.

In every basic decoder component to the input number X could be connected signal $In < X >$ or signal $\overline{In < X >}$ as it is shown in Figure 3.4. There are 2^X combinations of input signals. Therefore we can ensure that for X inputs, we have high signal

Table 3.2: Parameters of different kinds of gray decoders

Power supply	outputs line spacing	inputs	outputs	decoder area
$(0V,\ 1.2V)$	$10\mu m$	5inputs + 1EN	32	$(12.4\mu m,\ 319\mu m)$
$(0V,\ 1.2V)$	$20\mu m$	5inputs + 1EN	32	$(12.4\mu m,\ 641\mu m)$
$(0V,\ 1.2V)$	$25\mu m$	5inputs + 1EN	32	$(12.4\mu m,\ 797\mu m)$
$(0V,\ 2.5V)$	$10\mu m$	5inputs + 1EN	32	$(13.6\mu m,\ 319\mu m)$
$(0V,\ 2.5V)$	$20\mu m$	5inputs + 1EN	32	$(13.6\mu m,\ 641\mu m)$
$(0V,\ 2.5V)$	$25\mu m$	5inputs + 1EN	32	$(13.6\mu m,\ 797\mu m)$
$(0V,\ 1.2V)$	$10\mu m$	6inputs + 1EN	64	$(12.4\mu m,\ 638\mu m)$
$(0V,\ 1.2V)$	$20\mu m$	6inputs + 1EN	64	$(12.4\mu m,\ 1268\mu m)$
$(0V,\ 1.2V)$	$25\mu m$	6inputs + 1EN	64	$(12.4\mu m,\ 1583\mu m)$
$(0V,\ 2.5V)$	$10\mu m$	6inputs + 1EN	64	$(13.6\mu m,\ 639\mu m)$
$(0V,\ 2.5V)$	$20\mu m$	6inputs + 1EN	64	$(13.6\mu m,\ 1269\mu m)$
$(0V,\ 2.5V)$	$25\mu m$	6inputs + 1EN	64	$(13.6\mu m,\ 1584\mu m)$
$(0V,\ 1.2V)$	$10\mu m$	7inputs + 1EN	128	$(12.4\mu m,\ 1278\mu m)$
$(0V,\ 2.5V)$	$10\mu m$	7inputs + 1EN	128	$(12.4\mu m,\ 1279\mu m)$

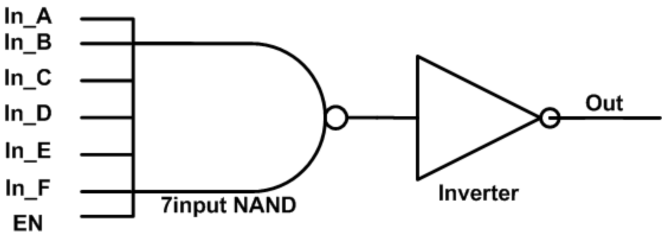

Figure 3.2: Block scheme of basic gray decoder element: 6 bits input signal + enable signal

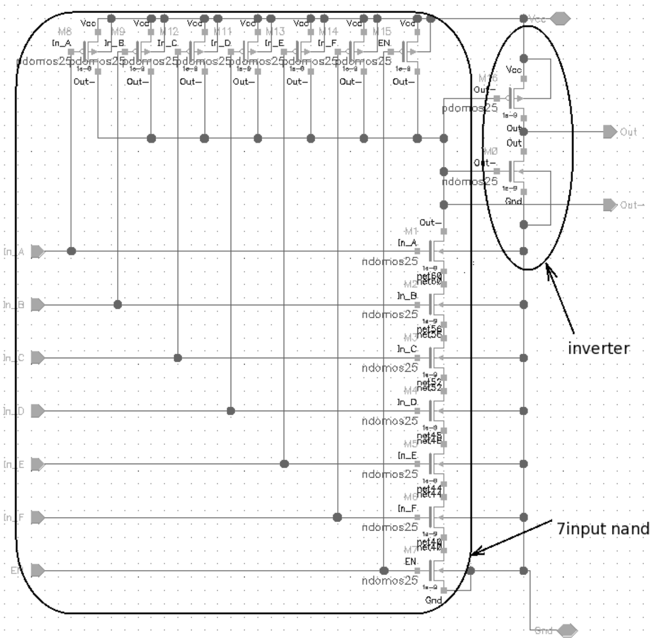

Figure 3.3: Block scheme of basic gray decoder element: 6 bits input signal + enable signal

always at only one of the 2^X outputs. Using gray decoder every output line one by one is reseted. An example of this is in Figure 3.6 presented.

Besides of the signals called $In < X >$ or $\overline{In < X >}$ we have also a signal called EN(enable). One enable is connected to all decoders in one pixel matrix. Every pixel matrix has its own enable signal. If $EN = 0$ we do not reset any line or row and therefore do not reset any pixel. We should remember that on the chip we have a few independent matrices of pixels and our purpose is to reset or read data from only one of them, at the same time. Without the enable signal it will be impossible because pin $In < X >$ and $\overline{In < X >}$ is the same for different decoders in every detector matrix. So we control every decoder's row and decoder's line using the same pins and choosing which matrix we are interested in, using enable signals(EN).

The principle of operation of decoders is clearly shown in Figure 3.5. At the same time only one row line and one column line has a high signal. As a result only one pixel is being reseted or read at the same time.

Using line decoders and row decoders we are able to reset all pixels one by one.

The results from testbenches are shown in Figure 3.6, where two methods of resetting and reading data from pixels are presented. The first method, in which the pixels are reset exactly one by one, and the second method, in which the two pixels are reset at

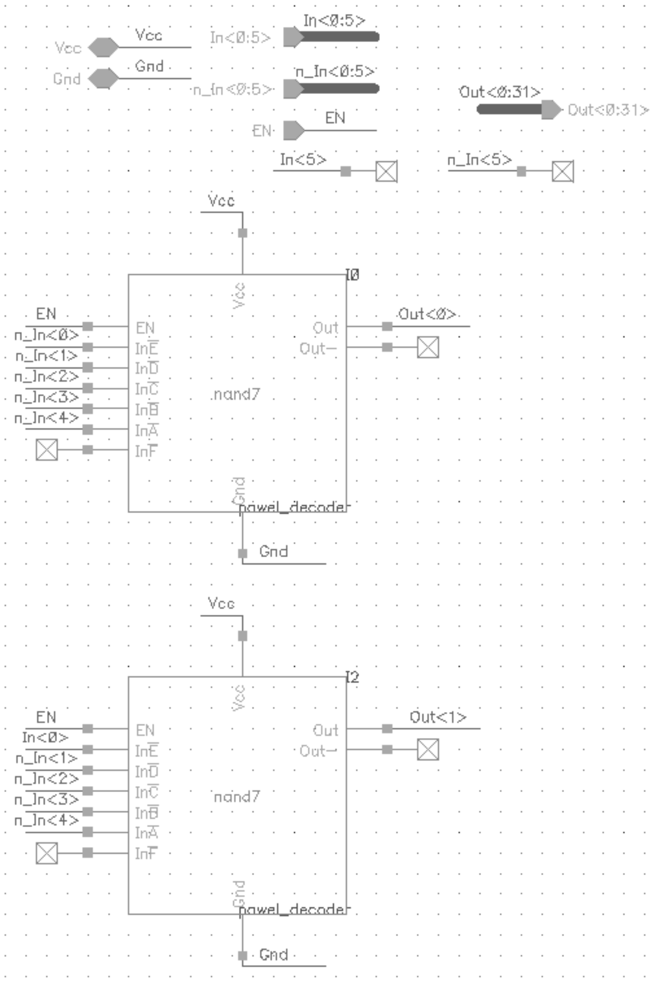

Figure 3.4: Scheme of fragment the whole gray decoder structure

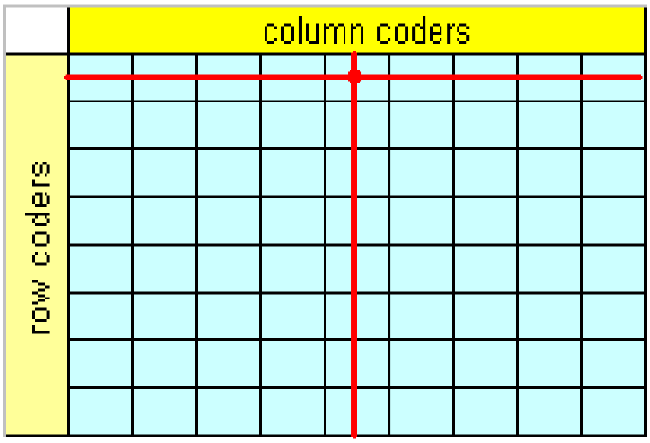

Figure 3.5: Description how one pixel from pixel matrix is chosen: pixel in the first row, fifth column

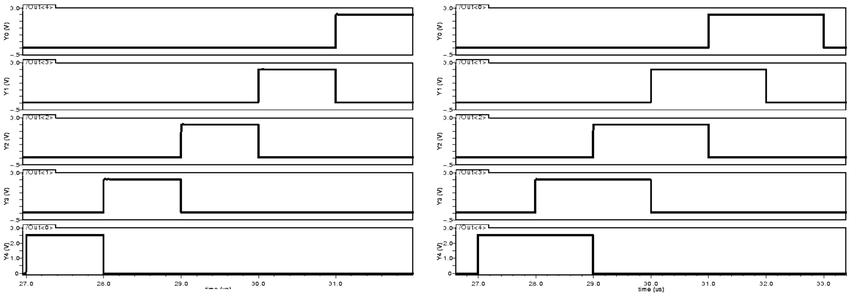

Figure 3.6: Results from testbench for gray decoders

the same time. The disadvantage of the first one is that some reset time is lost because of the rising time. In the second method this disadvantage is eliminated.

To get the results as in Figure 3.6(right) it is necessary to put one input in every basic decoder to the high power supply. This input is chosen as power supply which differs in the next basic decoder element as it is in Table 3.3 explained.

Table 3.3: Table of inputs which are connected to VDD for modified Gray decoder

Integer	3-bit Gray code	number of input connected to VDD
0	000	0
1	001	1
2	011	0
3	010	2
4	110	0
5	111	1
6	101	0
7	100	2

Using the second method of reseting the pixel matrix a few different decoders were also produced. Their parameters are described in Table 3.4.

3.3 METHODS OF MEASURING NODE CAPACITANCE

One of the essential parameter to check during decoder designing process was a decoder output node capacitance. The long metal line provides the reset signal to the 32, 64 or 128 diodes and connects the same number of the transistor gates. Every con-

Table 3.4: Parameters of different kinds of modificated gray decoders

Power supply	outputs line spacing	inputs	outputs	decoder area
$(0V,\ 1.2V)$	$10\mu m$	5inputs + 1EN	32	$(12.4\mu m,\ 319\mu m)$
$(0V,\ 1.2V)$	$20\mu m$	5inputs + 1EN	32	$(12.4\mu m,\ 641\mu m)$
$(0V,\ 1.2V)$	$25\mu m$	5inputs + 1EN	32	$(12.4\mu m,\ 797\mu m)$
$(0V,\ 2.5V)$	$10\mu m$	5inputs + 1EN	32	$(13.6\mu m,\ 319\mu m)$
$(0V,\ 2.5V)$	$20\mu m$	5inputs + 1EN	32	$(13.6\mu m,\ 641\mu m)$
$(0V,\ 2.5V)$	$25\mu m$	5inputs + 1EN	32	$(13.6\mu m,\ 797\mu m)$
$(0V,\ 1.2V)$	$10\mu m$	6inputs + 1EN	64	$(12.4\mu m,\ 638\mu m)$
$(0V,\ 1.2V)$	$20\mu m$	6inputs + 1EN	64	$(12.4\mu m,\ 1268\mu m)$
$(0V,\ 1.2V)$	$25\mu m$	6inputs + 1EN	64	$(12.4\mu m,\ 1583\mu m)$
$(0V,\ 2.5V)$	$10\mu m$	6inputs + 1EN	64	$(13.6\mu m,\ 639\mu m)$
$(0V,\ 2.5V)$	$20\mu m$	6inputs + 1EN	64	$(13.6\mu m,\ 1269\mu m)$
$(0V,\ 2.5V)$	$25\mu m$	6inputs + 1EN	64	$(13.6\mu m,\ 1584\mu m)$
$(0V,\ 1.2V)$	$10\mu m$	7inputs + 1EN	128	$(12.4\mu m,\ 1278\mu m)$
$(0V,\ 1.2V)$	$20\mu m$	7inputs + 1EN	128	$(12.4\mu m,\ 2544\mu m)$
$(0V,\ 2.5V)$	$10\mu m$	7inputs + 1EN	128	$(13.6\mu m,\ 1279\mu m)$
$(0V,\ 2.5V)$	$20\mu m$	7inputs + 1EN	128	$(13.6\mu m,\ 2545\mu m)$

nection to the transistor gate gives C_{GS}, C_{GD} and C_{GB} capacitances. The decoders are going to work with a clock 10MHz and it was important to find out if these parasitic capacitances are not too big and if a proper reset of every pixel is possible.

To estimate node capacitance resonance effect is used. Circuit as in Figure 3.7 was prepared. It is necessary to add resistor because Spice programs do not simulate circuits in which there are current-inductance branches. The value of this resistor is very small so this element has no influence on results of simulations. Also it is important to add capacitance, because then the added circuit does not consume any direct current from measured node and does not change operating point of measured node.

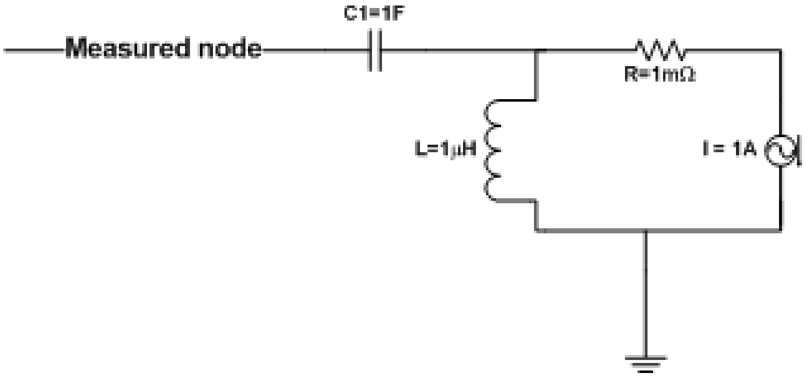

Figure 3.7: Scheme of the circuit used to calculate node capacitance

Using this circuit and making an AC simulation in an easy way resonance frequency is estimated.

$$\omega = \frac{1}{\sqrt{LC}} \tag{3.1}$$

where:

$$C = \frac{C_1 C_2}{C_1 + C_2} \tag{3.2}$$

C_2 is a measured node capacitance and $C_1 = 1F$.

$C_2 \ll C_1$ then $C \approx C_2$ and as a result we can calculate that:

$$C_2 = \frac{1}{L\left(2\pi f\right)^2} \tag{3.3}$$

The examples of AC simulations of this resonance effect are shown in Figure 3.8, where two nodes capacitances are calculated. Using equation 3.3 for resonance frequency 140MHz node capacitance is $C_I = \frac{1}{10^{-6} \times (2 \times 3.14 \times 140 \times 10^6)^2} = 1.3pF$. For the second node presented in Figure 3.8 resonance frequency was equal to 263MHz and

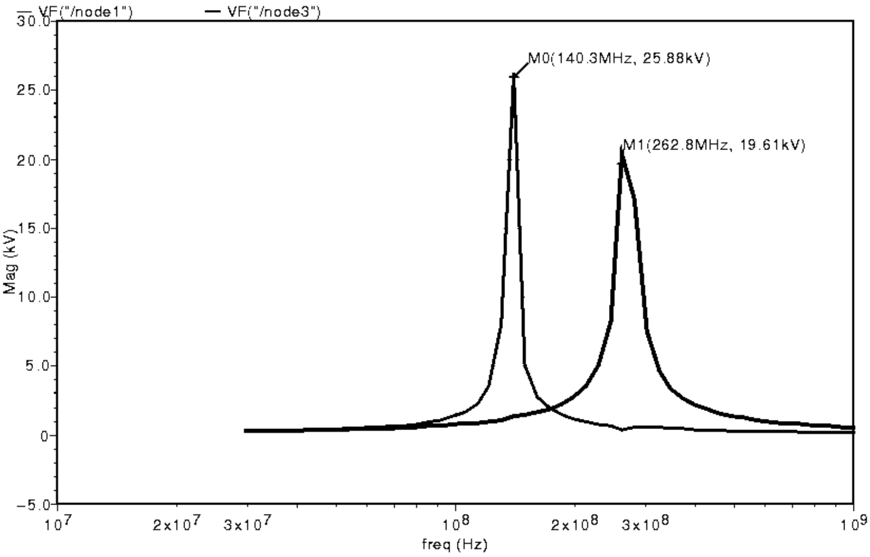

Figure 3.8: Exemplary result of measuring node capacitance

therefore this node capacitance is: $C_{II} = \frac{1}{10^{-6}\times(2\times3.14\times263\times10^6)^2} = 367fF$.

This method was used not only to estimate node capacitance of the decoders but especially to calculate node capacitances in the amplifier as it is described in the next chapters.

The main advantage of the presented method is that the added circuit does not change any parameters, like operating points, of the measured circuits.

In spectre simulator, pole-zero analysis is implemented. But as a score of this pole-zero analysis there are only values of poles and zeros without any information where the nodes of these poles or zeros are. If there are a lot of nodes it can be difficult to suit the values to the proper nodes. Using the presented method this kind of difficulty does not exist.

Besides, for other simulators, like Eldo or hSpice-S, there is no pole-zero analysis.

3.4 LAYOUT AND POSTLAYOUT SIMULATIONS

The example layout of the basic decoder component is shown in Figure 3.9 its functionality is an equivalent of Scheme 3.3.

A list of basic decoders gives a full decoder logic, a fragment of which is shown in Figure 3.10.

Every basic decoder is using the same input lines $\overline{In < 0 : 7 >}$ and $In < 0 : 7 >$. But

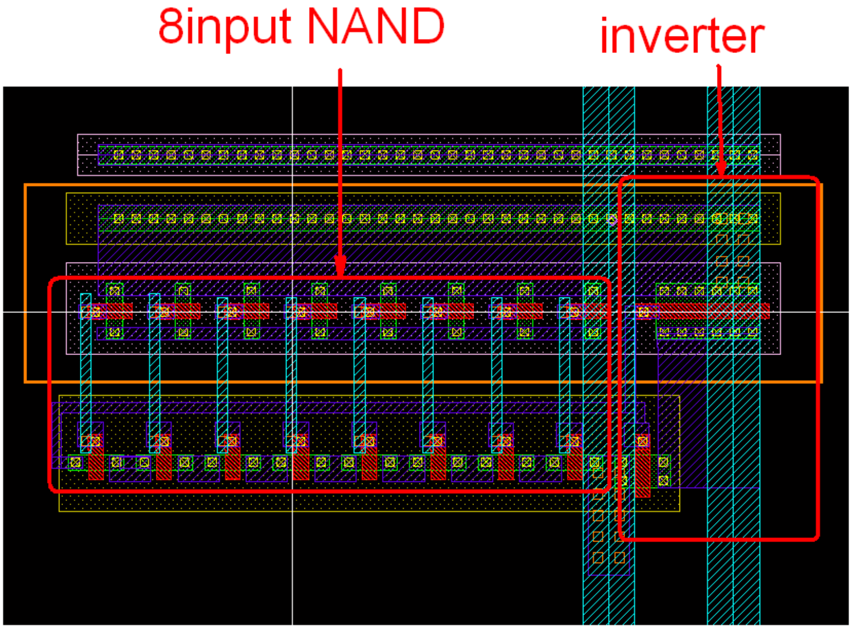

Figure 3.9: Layout of the basic decoder component

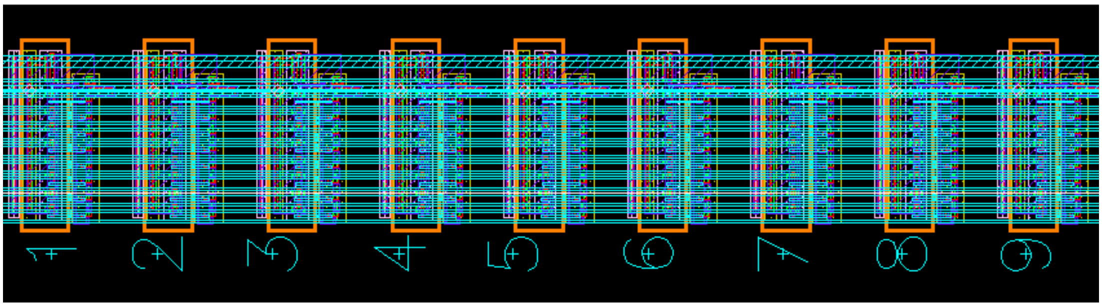

Figure 3.10: Decoder, fragment of layout

for every decoder component different inputs are chosen and therefore every decoder component has a different input logic.

There are two types of resetting every pixel matrix as it was shown in Figure 3.6. But there is only one Enable signal so transmission gate was designed to decide which type of resetting is used. The layout of this transmission gate is shown in Figure 3.11.

ON and OFF are the complementary signals and the transmission gate works as a switch, controlled by ON/OFF signal Transistors of the transmission gate have a $4\mu m$ channel width to keep a small resistance(R_on=200Ω). The length of transistors is as small as possible($0.28\mu m$).

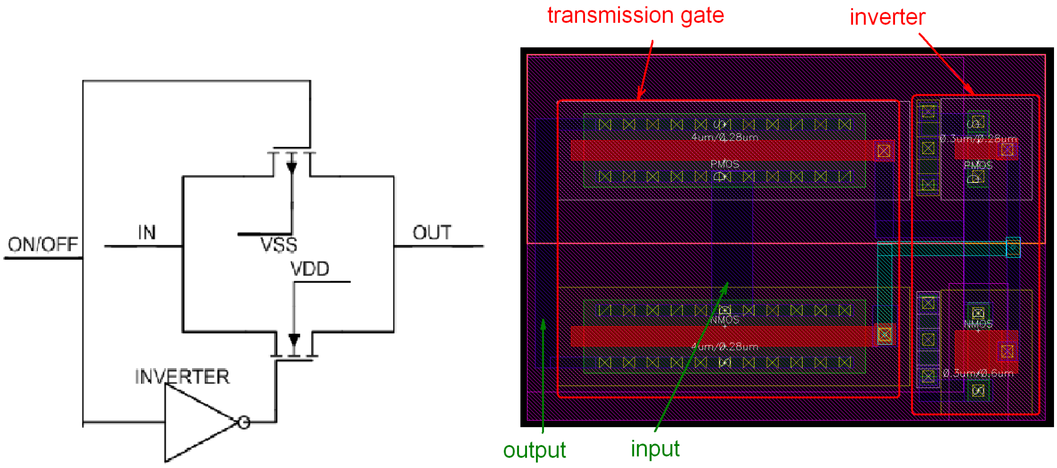

Figure 3.11: Scheme and layout of transmission gate used to choose one of two different decoding methods

While designing decoders it was necessary to make simulations concerning delay of the signal at the output of the decoders. The connection between the output of every decoder to the pixels is a long metal line. The length is from $300\mu m$ for the smallest pixel matrix to $2500\mu m$ for the biggest one. It was essential to choose as wide metal connection so that the resistance of this metal could be neglected. It is important to choose the proper width of this metal line.

After simulations only power supply lines which were provided on metal 2, were designed wide. The smallest possible width was chosen for the rest of input lines.

In postlayout simulations it is necessary to estimate output load. Output of every basic decoder component is connected to 32, 64 or 128 transistors by long metal line. The

length of metal line is even $2.5mm$ for matrix 128×128, where area between pixels is $20\mu m$. Every connected transistor gives capacitance and it is necessary to simulate if in spite of large capacitances correct resetting pixel matrix is possible.
The capacitance of this long metal output line is not more than $0.2pF \div 1pF$ (depending on the number of output transistors) and there are no problems with reseting or reading out these matrices.

Chapter 4

THE TWO-STAGE OPERATIONAL AMPLIFIER

4.1 NECESSITY OF AMPLIFIER USAGE

After decoders were finished it is time to design output amplifier. First description and features of amplifier which is needed are presented.

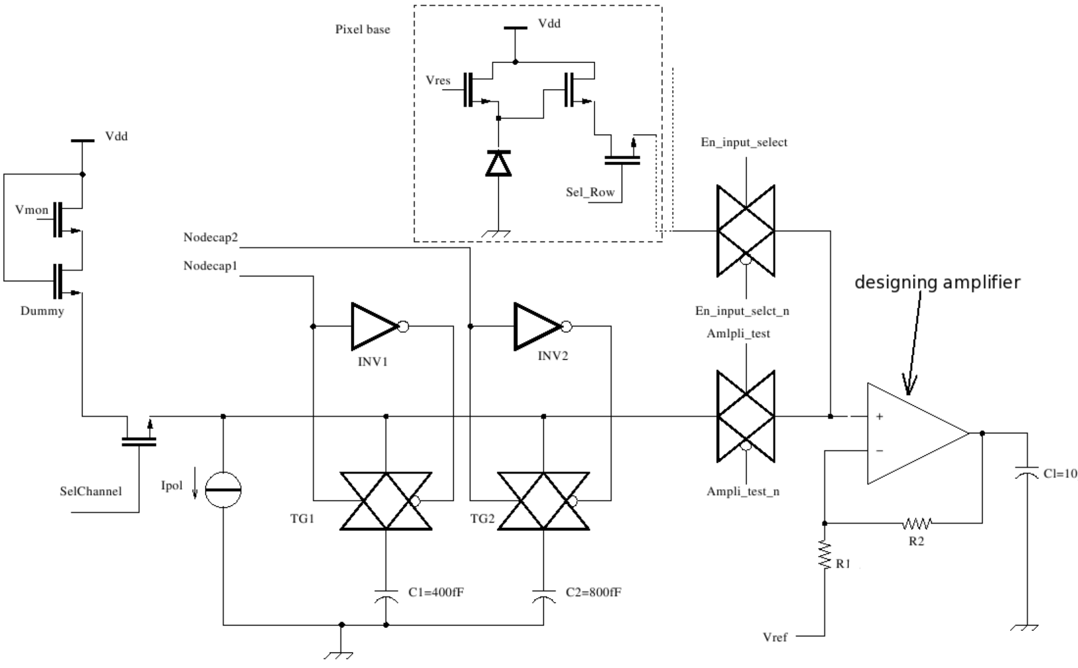

Figure 4.1: Circuit in which amplifier is used [26]

The amplifier will be integrate on the CMOS detector chip but outside the diode matrix. It means that the area of amplifier is not really a limitation . Only one amplifier per matrix is needed so it is possible to design it quite large. It is possible to use both types of transistors(nMOS and pMOS). The application, in which amplifier is used, is presented in Figure 4.1.

The pixel base is the source of the signal, as shown in Figure 4.2. The pixel base consists of transistors: M_1, M_2 and M_3. Transistor M_1 resets the diode to the reverse bias. Transistor M_2 is in source follower configuration and has large current gain and low output resistance. In that configuration the body effect is observed but it is not a problem because transistor M_1 is only working as an ON/OFF switch. It is impossible to avoid the body effect because on the pixel matrix only NMOS transistors can be used. Transistor M_3 is a row switch, whereas a line switch is located outside the pixel. This kind of picture configuration makes possible continuous charge integration between reset operations.

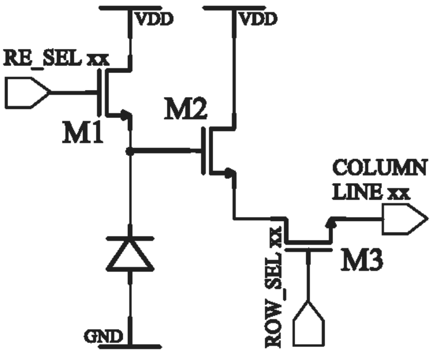

Figure 4.2: Single cell architecture in CMOS MAPS detector [13]

Next signal is coming through the transmission gate, which is used to choose whether to put this signal to the non-inverting input amplifier or to cut off this signal from amplifier as in Figure 4.1. The other option is to put test(marker) signal to this non-inverting input instead of signal from detector.

The voltage level from the diode mostly depends on the level of reverse voltage on the diode and is decreasing on the transistors M_2 and M_3. The input voltage signal change from $0.1V$ to $0.8V$ is expected. It is hard to estimate input voltage signal more precisely because it is the first chip in ST $0.13\mu m$ technology and the leakage current of the diode is unknown.

The main function of amplifier is to ensure a high impedance for the signal com-

ing from diode matrix. The source follower could be simply used to enable a high impedance. But then small signal gain, smaller than 1 and not constant for the whole ICMR, is obtained.
It is necessary to use an amplifier if we are interested in not only high input impedance, but also stable gain and possibility of regulation output voltage.

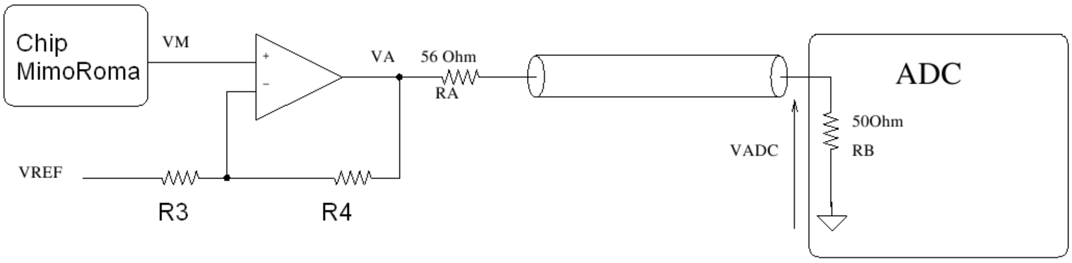

Figure 4.3: Reading the output signal from the chip: external amplifier and ADC converter [27]

The way of the signal outside the chip is presented in Figure 4.3. Outside the chip there is one more amplifier whose function is similar to the amplifier inside the chip. One more value which should be known is the proper voltage level of the output of this external amplifier. To estimate this value Figure 4.3 is very helpful. As it is shown in the equation 4.1 input voltage of the ADC converter is in rough estimation twice as small as output voltage of the amplifier.

$$V_A = \frac{R_A + R_B}{R_B} = \frac{50 + 56}{50} \tag{4.1}$$

and therefore:

$$V_A = A_V \frac{R_A + R_B}{R_B} \tag{4.2}$$

where:
V_A - output signal of the operational amplifier outside the chip,
V_M - output signal of the operational amplifier inside the MAPS chip detector
Besides of external amplifier it is good to amplify the signal as much as it is possible inside the chip. Signal which is amplified outside the chip includes more noises.

The author's purpose is to design such an amplifier which would work as an ideal amplifier, which would be able to amplify the input signal as much as it is possible, from $0.1V$ to $0.8V$, changing with frequency $10MHz$ and results in the signal on the proper output level voltage.

4.2 DESCRIPTION OF THE CLOSED LOOP AMPLIFIER

Before we start thinking about specific application of amplifier it is good to remind the assumptions of an ideal amplifier.

Properties of the ideal amplifier:

1. infinite gain

   The finite gain causes errors but we can neglect these, if the other errors like the inverse of the matching accuracy of integrated components is larger. A gain larger than $60 - 70dB$ is normally enough for most applications and then usually we have matching accuracy around 0.1%. [22]

2. infinite input impedance, so any signal can be supplied to the op-amp without loading problems

   In CMOS technology the input impedance is not normally a problem. Since we use the gate of a MOS transistor as input of amplifier, we have a very large impedance.

3. output impedance equal to zero

   Obtaining low output impedance can be a problem. But the typical use of op-amps in integrated systems, which also concern us, is operational transconductance amplifier and does not have a strict request for a low output impedance.[23]

4. wide bandwidth

   Wide bandwidth is important as well, especially if amplifier works in a high frequency. This parameter depends on all capacitances which are in device, especially load capacitance and therefore Miller capacitance. The method of increasing bandwidth is to increase current I_0 as in Figure 4.4 and not to use large transistors.

If we follow the above approximations, by analyzing op-amp circuits we can assume:

1. the input currents are zero

   In CMOS technology current of the gate of transistors is very small because of high input resistance of the gate and we can make assumption that is equal to zero.

2. the voltages V- and V+ are equal

   In CMOS applications this condition is usually fulfilled for gain bigger than $60 - 70dB$.

Negative feedback is require to apply these rules. It is used to stabilize and control the gain of amplifier because without negative feedback the gain is too large to be useful, technological mismatches and noises will make the circuit clip.
Amplifier works in non-inverting configuration, therefore does not change the sign of the input signal and does not change the phase. Closed loop gain for ideal amplifier is given by equation:

$$A_{cl} = 1 + R_2/R_1 \tag{4.3}$$

where R_1 and R_2 are in Figure 4.1.
Then the gain depends only on resistors R_2 and R_1.

Real amplifier:

In real applications we have finite open loop gain and equation 4.3 is no longer actual but closed loop gain is now:

$$A_{cl} = \frac{A_{ol}}{1 + A_{ol}\frac{R_1}{R_1+R_2}} \tag{4.4}$$

If in formula 4.4 $A_{ol} \rightarrow \infty$ then we get exactly equation 4.3.

The second thing to consider is an advantage of using reference voltage:
Because $\frac{V_{-}-V_{ref}}{R_1} = \frac{V_{out}-V_{ref}}{R_1+R_2}$
and $V_{-} = V_{+} = V_{in}$
so it is correct to write:
$V_{out}R_1 = V_{in}(R_1 + R_2) - V_{ref}R_2$
and as a result:
$V_{out} = V_{in}\frac{R_1+R_2}{R_1} - V_{ref}\frac{R_2}{R_1}$.
In our application we want to have amplification about $2(R_2 = R_1)$ so $V_{out} = 2V_{in} -$

V_{ref} and using V_{ref} it could be a method to ensure proper output level voltage.

4.3 DIFFERENTIAL STAGE

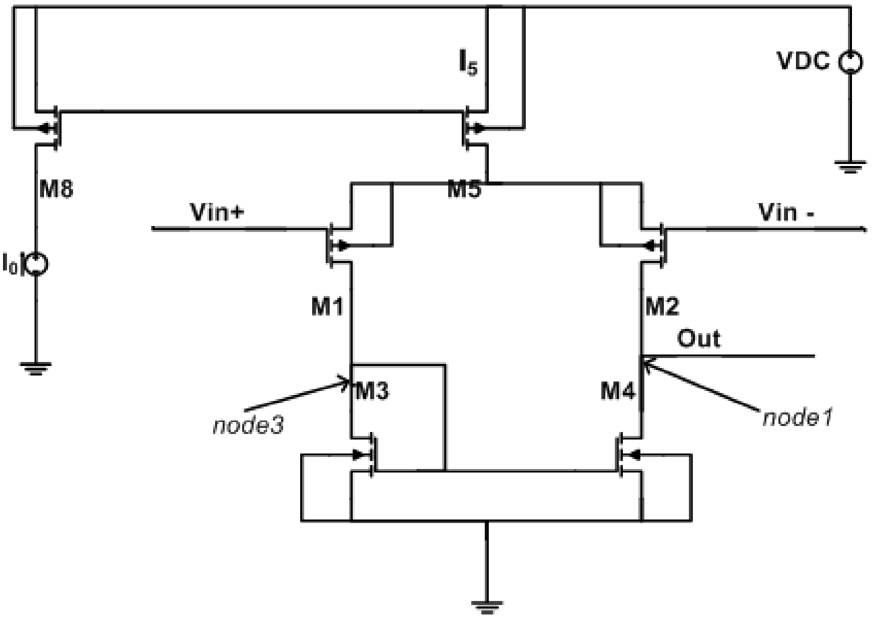

Figure 4.4: Differential stage amplifier

In Figure 4.4 the differential amplifier, which consists of self–biasing differential stage with active load is shown. M_1 and M_2 are equal and form a matched pair which produce reasonably large gain. Also $M_3 = M_4$ and form active current mirror, which adds current into two branches and doubles the gain while performing differential to single ended conversion. Current source I_5 determines current level. Half of current I_5 flows through transistors M_1 and M_3 so the other half of current flows through transistors M_2 and M_4.

The advantage of using differential pair and current source as PMOS transistors is the fact that substrates are connected to the source, as in Figure 4.4. In this way the body effect is excluded and matching is improved.

But there is also a disadvantage of that architecture: smaller gain, because of smaller transconductance parameter for pMOS than for nMOS.

Before two-stage amplifier designing is started, it is necessary to remember some equations and dependencies between parameters useful in designing differential stage:

Transconductance:

Amplifier will be designed as an operational transconductance amplifier so transconductance parameter has to be known.

At low frequencies the transconductance of amplifier is given by formula:

$$g_m = g_{m1} = g_{m2} = \sqrt{K'_p I_5 \left(\frac{W}{L}\right)_1} \tag{4.5}$$

where:

K'_p - transconductance parameter of pMOS transistor in saturation

and $g_m = \frac{\partial i_D}{\partial v_{GS}}$ - channel conductance.

Voltage gain:

A voltage gain can be calculated, if output resistance is known:

$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}} = \frac{V_{Ep} L_1}{I_5}, \tag{4.6}$$

where:

$g_{ds} = \frac{\partial i_D}{\partial v_{DS}}$,

V_{Ep} - Early voltage, typical value for pMOS is $8.3V/\mu m$

and as a result:

$$A_V = g_m r_{out} = V_{Ep}\sqrt{\frac{2K'_p W_1 L_1}{I_5}} = \frac{V_{Ep} L_1}{V_{SG1} - V_T} \tag{4.7}$$

As in formula 4.7 only dimensions of transistors are not technological parameters, but depend on decision of the designer and should be chosen for optimum performance.

Input Common-Mode Range

Another important feature of the differential amplifier is ICMR. For minimal input common voltage formula 4.8 has to be followed.

$$V_{ic}(min) = V_{SS} + V_{GS3} - V_{TP1} \tag{4.8}$$

where: V_{TP1} - threshold voltage of PMOS transistor M_1

and results in maximum input common voltage:

$$V_{ic}(max) = V_{DD} - V_{SD5}(sat) - V_{SG1} \tag{4.9}$$

and where:

$$V_{SD5}\left(sat\right)=\sqrt{\frac{2\cdot I_5\cdot L_5}{K'\cdot W_5}} \tag{4.10}$$

so if a proper $V_{ic}\left(max\right)$ cannot be assumed, $V_{DS}\left(sat\right)$ has to be decreased by decreasing current I_5 or increasing aspect ratio of transistor M_5.

Gain-bandwidth and phase margin[19]

Gain-bandwidth product and phase margin are determined by pole and zero positions. In our configuration we have two poles:

A dominant one which is on the $node1$ as in Figure 4.4:

$$f_d=f_1=\frac{1}{2\pi r_{out}\left(C_{n1}+C_L\right)} \tag{4.11}$$

in which $C_{n1}=C_{gd4}+C_{db4}+C_{gd2}+C_{db2}$.

And the value of GB is then obtained as:

$$GB=A_V f_d=\frac{g_{m1}}{2\pi\left(C_{n1}+C_L\right)}=\frac{\sqrt{2K_n' I_B}}{2\pi}\frac{\sqrt{S_1}}{C_{n1}+C_L} \tag{4.12}$$

And a non-dominant is $node3$ which is shown in Figure 4.4:

$$f_{nd}=\frac{1}{2\pi R_{n3}C_{n3}} \tag{4.13}$$

in which:

$R_{n3}\approx 1/g_{m3}\approx 1/g_{m4}$,

$C_{n3}=C_{gd1}+C_{db1}+C_{db3}+C_{gs3}+C_{gs4}+C_{gd4}+C_{gb3}+C_{db4}$,

and C_L is a load capacitance.

The value of f_{nd} ought to be, and usually is, larger than the value of GB. Using GB phase margin can be calculated:

$$PM=90deg-arctan\frac{GB}{f_{nd}}+arctan\frac{GB}{2f_{nd}} \tag{4.14}$$

Equation 4.14 clearly shows that the phase shift of the zero compensates the non dominant pole and the PM is always larger than $70deg$.[20]

Optimization for maximum GB:

Now we will find the method how to optimize the differential amplifier for maximum GB, if we assume constant current I_5 and output load. We will learn how to choose the optimum dimensions of transistors.

Let's assure that $C_L = 10pF$, $I_5 = 10\mu A$ and $W_1 = W_3 = L_1 = L_3 = 1\mu$
It is important to choose the same dimensions of mirror transistors and differential transistors because then $g_{m1} = g_{m3}$ and adequate capacitances of every transistor are the same.
Therefore we decided to allow f_{nd} and GB to be equal as in the expression below:

$$\frac{g_{m3}}{C_{n3}} = \frac{g_{m1}}{C_{n1} + C_L} \tag{4.15}$$

Then the pole - zero doublet do not occur in the useful range of frequencies and we have settling time as small as possible.
Using formula 4.5 and assumption of $K'_n = 3K'_p$, which is confirmed in the subsection 4.4, we have:

$$(W/L)_4 \approx \frac{1}{3}(W/L)_1 \left(\frac{C_{n3}}{C_L + C_{n1}}\right)^2 \tag{4.16}$$

Now using formula 4.16 and method of calculating node capacitances from chapter 3.3 we have:
$S_1 = 3 \times \frac{1.1\times10^{-13}}{1.02\times10^{-14}} = 352.$

Equation 4.12 shows that GB is proportional to the square root of S_1, if we make assumption that node capacitances are not dependent on dimensions of transistor and are constants. Of course that way of thinking is not correct, because for larger dimensions of transistors, we get larger node capacitances as well. If dimensions of differential pair transistors are small and we start increasing S_1, we enlarge GB as well, but there is an optimum of GB and if we still increase S_1, we get smaller GB as a result. This is very well shown in Figure 4.5.

The question is why the maximum value of GB in Figure 4.5 is not for calculated $S_1 = 352$ but for $S_1 = 200$. To find the answer once again equation 4.16 is used. Aspect ratio of transistor M_1 was calculated for C_{n3} and C_{n1}, which were measured for dimensions of all transistors: $(1\mu, 1\mu)$. Of course if dimensions of transistors are increased then C_{n1} and C_{n1} are bigger so $\frac{C_L+C_{n1}}{C_{n3}}$ and the calculated S_1 are also decreased.
It is important to remember these limitations related to capacitances of transistors.

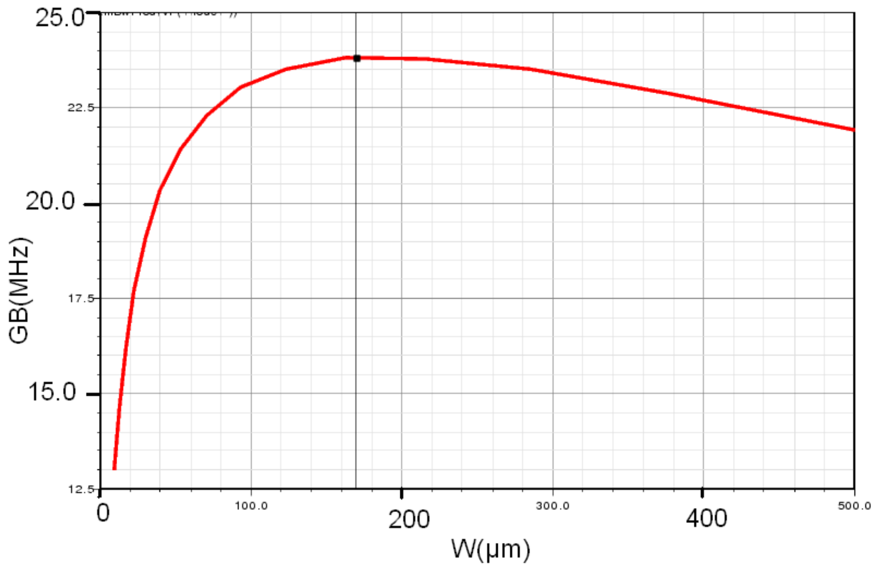

Figure 4.5: Gain Bandwidth product of the differential stage in function of aspect ratio of differential pair transistors

We have understood equation 4.12 and the proper aspect ratio of differential pair transistors has been chosen ($S_1 = 200$). Now we will estimate which are the best dimensions for transistors M_1.

That is why we will change dimensions of all transistors, but we are going to keep the aspect ratio constant $(S_4 = 1, S_1 = 200)$, so we use formula $L = L_1 = L_2 = L_3 = L_4$, where $W_1 = W_2 = 200 \times L$ and $W_3 = W_4 = 1 \times L$. Figure 4.6 clearly shows for which length of transistor the GB parameter is the biggest.

The smallest value is not advisable and the best results for $L = 0.3\mu m$ are achieved. This knowledge is valuable when we need to choose the minimum length of transistors.

To explain results shown in Figure 4.6 we use equation 4.17, given in the next section. λ is getting bigger for $L < 0.3\mu m$ and as an effect we have smaller GB as well.

The above considerations will be helpful during designing differential amplifier and a two-stage amplifier.

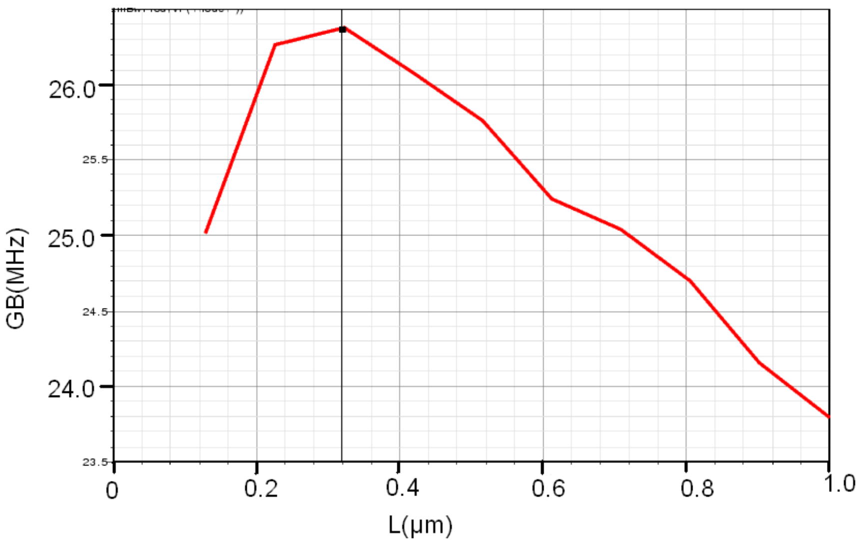

Figure 4.6: Gain Bandwidth product of the differential stage in function of different length of mirror transistors and differential transistors where $S_1 = S_2 = 200$ and $S_3 = S_4 = 1$

4.4 TWO-STAGE AMPLIFIER - DESIGN PROCEDURE

After consideration about the differential stage, the two-stage amplifier will be presented.

The difference between this simple two-stage amplifier and differential stage amplifier is that the two-stage amplifier presented in Figure 4.7 includes two more transistors: M_6 which defines the second stage small signal gain and M_7 which ensures desired

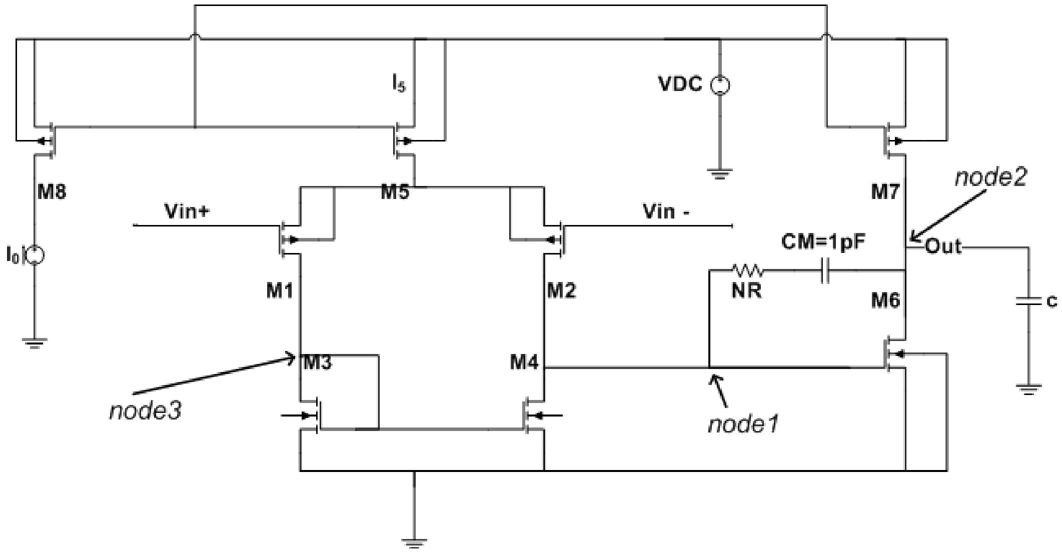

Figure 4.7: Two-stage amplifier

second stage current. Often in the differential stage, to increase gain, cascode is used. But in this application using cascode is the wrong decision, because it decreases input common minimum voltage.

For a two-stage amplifier there is always a phase margin problem and Miller capacitance (CM) is used to give a proper phase margin. Also a nulling resistor (NR) can be used to improve gain-bandwidth.

The low frequency gain of the two-stage amplifier is simply given by the product of two gains:

First-stage gain:

$$A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{-2g_{m1}}{I_5\left(\lambda_2 + \lambda_4\right)} \tag{4.17}$$

Second-stage gain:

$$A_{v2} = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = \frac{-g_{m6}}{I_6\left(\lambda_6 + \lambda_7\right)} \tag{4.18}$$

At low frequency the second stage does not load the output of the differential stage and therefore as a result of multiplication these two gains we have:

$$A_v = \frac{g_{m1}g_{m6}}{\left(g_{ds2} + g_{ds4}\right)\left(g_{ds6} + g_{ds7}\right)} \tag{4.19}$$

Equation 4.19 is true for assumption that all transistors are working in saturation region.

The most important conclusion is that gain of our amplifier depends on dimensions of four transistors.

Two important poles for differential stage amplifier were shown. Also for two-stage amplifier two poles are crucial: **output pole**, shown in Figure 4.7 as a $node2$, described by below equation:

$$p_2 = \frac{-g_{m6}}{C_L} \tag{4.20}$$

and it is called **first non-dominant pole**.

The **dominant pole** is also shown in Figure 4.7 as $node1$ and is given by equation:

$$p_1 = \frac{-g_{m1}}{C_C} \tag{4.21}$$

The equivalent pole to $node1$ is the same called pole in Figure 4.4. But in equation 4.21 capacitances of the transistors M_2 and M_4 are not included because C_C is much bigger and we can omit the rests of capacitances. But we remember that for big dimensions of differential stage transistors the equation 4.21 is not precise and we expect dependence like in Figure 4.5.

The purpose is to have $2.2 \times p_1 = p_2$, because then there is no influence of non-dominant pole for our amplifier and as a result, no problem with phase margin and stability is observed.

By contrast to the above two poles which are in the left s-plane of the transfer function, the **zero** in the right s-plane also exists.

$$z_1 = \frac{g_{m6}}{C_C} \tag{4.22}$$

There are two design strategies about z_1. We calculate this parameter if we want to check if this zero is in the right side of the s-plane.We need also value of this parameter if our purpose is to put zero in the left side of the s-plane and in this case increase gain-bandwidth which is later discussed in section 4.4.

Differential-frequency response and output voltage

After low frequency gain and poles are calculated, it is time to write the differential-frequency response, which is given as:

$$A_V(s) = \frac{A_{V0}}{\left(\frac{s}{p_1} - 1\right)\left(\frac{s}{p_2} - 1\right)\left(\frac{s}{p_3} - 1\right)...} \tag{4.23}$$

And the output voltage can be defined as:

$$V_{out}\left(s\right) = A_V(s)[V_1(s) - V_2(s)] \pm A_c(s)\left(\frac{V_1(s) + V_2(s)}{2}\right) \tag{4.24}$$

where:

$A_C(s)$ - common-mode frequency response

Assumptions for two-stage amplifier:

- Power supply: $V_{SS} = 0V$ and $V_{DD} = 1.2V$ or $V_{DD} = 2.5V$.

  In ST $0.13\mu m$ technology these two kinds of power supply are available. For $V_{DD} = 1.2V$ the width of gate oxide is smaller like for $V_{DD} = 2.5V$ and as a result g_m parameter is about 2.5 times bigger for lower power supply than for $2.5V$.

- Gain=$60dB \div 70dB$
  This value should be enough to make assumption that gain of amplifier is infinite like for the ideal amplifier.

- Gain-Bandwidth$(GB) = 100$MHz
  The input signal for amplifier is going to be changed with a clock $10MHz$. GB=100MHz is definitely enough to amplify input signal because the three first harmonics of the input signal are being amplified. Even GB=30MHz is usually sufficient but in simulations smaller GB than in calculations is achieved.

- Input Common-Mode Range$(ICMR) = 0.7V$
  - $V_{in}(min) = 0.1V$
  - $V_{in}(max) = 0.8V$

  The level of the signal from diode is not known and that is the reason why such a big ICMR was defined.

- Load capacitance$(C_L) = 10pF$
  Output of amplifier is an output of the chip and that is why such a large capacitance as a load has been assumed.

The rest of parameters which are useful in calculations:

- Slew Rate$(SR) = 100V/\mu s$
  Gain-bandwidth of the amplifier is 100MHz and we know that our amplifier should be prepared to work in frequency 10MHz and therefore value of SR as $100V/\mu s$ sounds reasonable.

- $K'_n = 397 \times 10^{-6} \frac{A}{V^2}$

- $K'_p = 117 \times 10^{-6} \frac{A}{V^2}$

Because

$$K' = \mu_0 \cdot C_{ox}, \tag{4.25}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \cdot \epsilon_0}{t_{ox}} = \frac{3.9 \times 8.8 \times 10^{-14}}{2.4 \times 10^{-9}} \frac{\frac{F}{cm}}{m} = 1.43 \times 10^{-6} \frac{F}{cm^2} \tag{4.26}$$

and

$\mu_{0n} = 278\frac{cm^2}{V\times s}$, $\mu_{0p} = 81\frac{cm^2}{V\times s}$

where:

C_{ox} - oxide capacitance,

t_{ox} - oxide thickness,

μ_{0n} - nMOS transistor mobility,

μ_{0p} - pMOS transistor mobility,

ϵ_o - permittivity of free space,

ϵ_{ox} - permittivity of SiO_2.

Design procedure: [3]

1. *Choose the smallest transistor length that will keep the channel modulation parameter constant, give good matching for current mirrors and differential pair.*
   L_{min} =***1***μ
   Good matching of the transistors is especially important in the first stage. In the second stage usually the length of transistors can be smaller, as in the first stage, if it improves GB of amplifier.
   The argument why not to use the smallest length which is possible is that for submicronic dimensions the channel length modulation parameter is getting bigger. As a result, we have smaller gain, like in Formula 4.17 and as it was proved in section 4.3, especially in Figure 4.5. When we consider the length of differential transistors, the most important is good matching, even at the expense of GB of amplifier. That is why we do not choose smaller dimensions than $1\mu m$ for the first stage transistors.

2. *From the desired phase margin, choose the minimum value of Miller capacitance(Cc).*
   Miller capacitance is always necessary in two-stage amplifiers. Without compensation, the op - amp will oscillate in the feedback circuits. If we need 60^0 phase margin, we use the following relationship for calculating Miller capacitance:

$$2.2 \times p_1 = p_2 \qquad (4.27)$$

In the book *"CMOS Analog Circuit Design, second edition" written by Phillip E.*

Allen and Douglas R. Holberg the dependence $C_C = 0.22C_L$ is suggested. Then when we put values from 4.21 and 4.20 to the 4.27, dependence $g_{m6} \geq 10 \times g_{m1}$ is given.

Despite of the advice from this book dependence of C_C was chosen:

$$C_C = 0.1C_L \tag{4.28}$$

so C_C =***1pF*** and as the result

$$g_{m6} \geq 22g_{m1} \tag{4.29}$$

Even for this smaller Miller capacitance a lot of place in layout is consumed. Therefore it was advisable to decrease value of Miller capacitance.

3. *Determine the minimum value for "tail current" (I_5).*

$$I_5 = SR \cdot C_C \tag{4.30}$$

and

$I_5 = 100 \times 10^6 \times 1 \times 10^{-12} A$ =***100***μA

4. *Design aspect ratio of mirror transistors, from the minimum input voltage specification.*

Condition for aspect ratio in the formula below is described.

$$S_3 \geq \frac{I_5}{K_n' \left[V_{in}(min) - V_{SS} - |V_{TO3}|(max) + V_{T1}(min)\right]^2} \geq 1, \tag{4.31}$$

Using simulations S_3 =***40*** is chosen. For that aspect ratio of mirror transistors for $ICM = 0.1V$ all transistors of the first stage are still in saturation region. This method is more precise than choosing proper S_3 by using equation 4.31.

5. *Verify whether the pole and zero due to C_{gs3} and C_{gs4} will not be dominant by assuming p_3 to be greater than 10GB.*

There is no influence of p_3 if the formula below is executed.

$$\frac{g_{m3}}{2C_{gs3}} > 10GB, \tag{4.32}$$

and then because

$$g_{m3} = \sqrt{2K\prime_n S_3 I_3} \tag{4.33}$$

and

$$C_{gs3} = 0.67 W_3 L_3 C_{ox} \tag{4.34}$$

we get

$$p3 \approx \frac{-gm_3}{2C_{gs3}} = \frac{-\sqrt{2K\prime_n S_3 I_3}}{2\left(0.667\right) W_3 L_3 C_{ox}} = 6.6 \times 10^{14} Hz \tag{4.35}$$

and $5.84 \times 10^{13} > 10GB$.

As we see, there is no influence of this pole and zero.

6. *Design $S_1 (S_2)$ to achieve the desired GB.*

   Gain - bandwidth depends on g_{m1} and load capacitance. Current was defined so only aspect ratio of differential pair transistors is unknown. To define S_1 the formulas below are used:

   $$S_1 = S_2 = \frac{gm_1^2}{K\prime_p I_5}, \tag{4.36}$$

   where:

   $$g_{m1} = GB \cdot 2 \cdot \pi \cdot C_C \tag{4.37}$$

   we have:

   $S_1 = S_2 = \frac{\left(10^8 \times 6.28 \times 10^{-12}\right)^2}{117 \times 10^{-6} \times 100 \times 10^{-6}}$ =***27***.

7. *Design S_5 from maximum input voltage.*

   First we calculate $V_{DS}\left(sat\right)$:

   $$V_{DS}\left(sat\right) = V_{DD} - V_{in}\left(max\right) - V_{gs1} \geq 100mV \tag{4.38}$$

   $V_{DS} = 2.5V - 0.8V - 0.7V = 1V$

   and next

   $$S_5 = \frac{2I_5}{K\prime_p \left[V_{DS5}\left(sat\right)\right]^2} \tag{4.39}$$

   so $S_5 = \frac{2 \times 100 \times 10^{-6}}{1.17 \times 10^{-4} [1]^2} = 2$

   Finally after simulations S_5 =***5*** was chosen, because for the calculated value of S_5 transistors were not in saturation region for the whole ICMR.

8. *Find S_6 and I_6 by letting the second pole(p_2) be equal to 2.2×GB.*

$$g_{m6} = 2.2 g_{m1} \left(C_L/C_C\right) \tag{4.40}$$

$g_{m6} = 22 g_{m1}$ =***12.4mS***.

Assuming that $g_{m6} = 12.4mS$, from formula 4.32 calculate g_{m3} =***1.26 mS***, to choose S_6, the following equation was used:

$$S_6 = S_3 \frac{g_{m6}}{g_{m3}}, \tag{4.41}$$

$S_6 = 40 \times \frac{12.4\times10^{-3}}{1.26\times10^{-3}}$ =***394***.

The aspect ratio for M_6 is really huge. Let's think if it is possible to decrease this value. S_6 from formulas 4.40 and 4.33 to equation 4.41 depends on:

$$S_6 = S_3 \frac{2.2 g_{m1} \frac{C_L}{C_C}}{g_{m3}} = S_3 \frac{2.2\sqrt{2K'_p S_1 I_3}\frac{C_L}{C_C}}{\sqrt{2K'_n S_3 I_3}} = 2.2\frac{C_L}{C_C}\sqrt{S_3 S_1}\sqrt{\frac{K'_p}{K'_n}} \tag{4.42}$$

As it was shown in Equation 4.42, to reduce dimensions of M_6 transistor, it is necessary to:

- increase Miller capacitance (C_C) - it is worthy to be done, if dimensions of Miller capacitance are smaller than dimensions of M_6 transistor. It is expected that C_C is bigger and that is why there is no sense to reduce S_6 by using this method.

or

- decrease S_3 - then ICMR is not ensured.

or

- decrease S_1 - as a result gain and gain-bandwidth is smaller

It was proved that there is no method to decrease S_6.

Remembering about the problems with gain of large transistors, which were shown in Figure 4.5, length of M_6 was chosen $0.5\mu m$

Knowing g_{m6} and S_6 allows us to solve for I_6 as:

$$I_6 = \frac{g_{m6}^2}{2K'_n S_6}, \tag{4.43}$$

$I_6 = \frac{\left(12.4\times10^{-3}\right)^2}{2\times3.97\times10^{-4}\times394} \cong \boldsymbol{493}\mu A.$

9. Design S_7 to achieve the desired current ratios between I_5 and I_6.

   The device size of M_7 can be determined from balance equation given below:

$$S_7 = S_5 \frac{I_6}{I_5}, \tag{4.44}$$

   where we assume correct value of S_6 and S_7 calculated in step 8.

   $S_7 = 5 \times \frac{493\times10^{-6}}{100\times10-6} \cong \mathbf{25}.$

10. Check gain and power dissipation specifications

    Using equations: 4.17 and 4.18 we can roughly calculate gain of our amplifier:

$$A_V = \frac{2g_{m2}g_{m6}}{I_5\left(\lambda_2+\lambda_3\right)\left(\lambda_6+\lambda_7\right)} \tag{4.45}$$

    We assume that $\lambda = 0.01$. Usually for the submicron length of transistor λ is about 0.04 but for $L \geq 1\mu$ is only 0.01.

    $A_V = \frac{2\times565\times10^{-6}\times12.4\times10^{-3}}{100\times10^{-6}(0.01+0.01)(0.01+0.01)} = 351 = \mathbf{51dB}$

    And

$$P_{diss} = \left(I_5+I_6\right)\left(V_{DD}+\left|V_{SS}\right|\right) \tag{4.46}$$

    $P_{diss} = \left(100\times10^{-6}+497\times10^{-6}\right)(2.5+0) = \mathbf{1.48mW}$

why 2.5V, not 1.2V power supply is used

Differential pair transistors are not in saturation region for $ICM = 0.8V$, for $1.2V$ power supply. To improved this $V_{DS5}\,(sat)$ is calculated:

$$V_{DS5}\,(sat) = V_{DD} - V_{in}\,(max) - V_{gs1} \geq 100mV \tag{4.47}$$

$V_{GS1} = 0.3V$ and $V_{DS5} = 0.1V$ is assumed. Then using formula 4.39 aspect ratio of M_5 is calculated as $S_5 = 172$.

But for huge transistor M_5 it is very difficult to design the second stage, especially transistor M_7. Moreover even for $S_5 = 172$ differential pair transistor are still not in saturation region for all ICMR and as a consequence bias node in $node1$ in Figure 4.4 is not fixed and it is impossible to design second stage for assumed ICMR. The problems of fix bias point of output differential stage is clearly shown in Figure 4.8. Bias point is presented in the function of input common voltage for different currents. Even

Table 4.1: Parameters of the two-stage amplifier

parameters	calculating	scheme sim.	postlayout sim.
$M_1(W_1, L_1)$	27μm,1μm	27μm,1μm	27μm,1μm
$M_3(W_3, L_3)$	40μm,1μm	40μm,1μm	40μm,1μm
$M_5(W_5, L_5)$	5μm,1μm	5μm,1μm	5μm,1μm
$M_6(W_6, L_6)$	197μm,0.5μm	197μm,0.5μm	197μm,0.5μm
$M_7(W_7, L_7)$	25μm,1μm	25μm,1μm	25μm,1μm
I_5, I_7	100μA,500μA	$99.2\mu A, 397\mu A$	-
$Gain$	$51dB$	$62 \div 66dB$	$61 \div 66dB$
GB	$100MHz$	$36MHz$	$33MHz$
PM	$> 60^0$deg	55^0deg	$57^0 - 59^0$deg
f_{3dB}	-	$33kHz \div 50kHz$	$33kHz \div 49kHz$
$CMRR$	-	$87dB$	$85dB$
$PSSR$	-	$64dB \div 67dB$	$64dB \div 66dB$
$Slew\ Rate$	$100V\mu s$	$37V/\mu s$	$37V/\mu s$
$RMS\ noises$	-	$188\mu V$	$187\mu V$
$Power\ diss.$	$1.48mW$	$1.091mW$	$1.13mW$

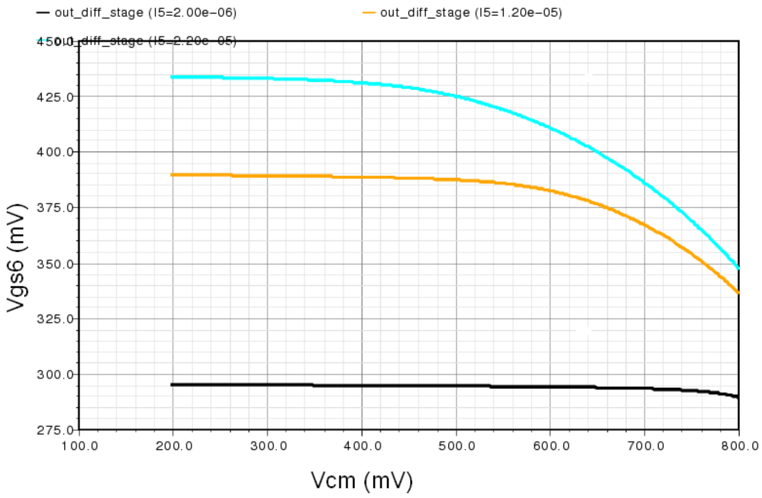

Figure 4.8: Input voltage of the output stage(V_{gs6}) in function of input common voltage for different current I_5, $V_{DD} = 1.2V$

for a small current value as $12\mu A$, output differential stage voltage is not fixed, which is evidence that M_5 transistor is not in saturation region.

As a result of not fixed V_{gs5} there are problems to achieve good gain of the amplifier

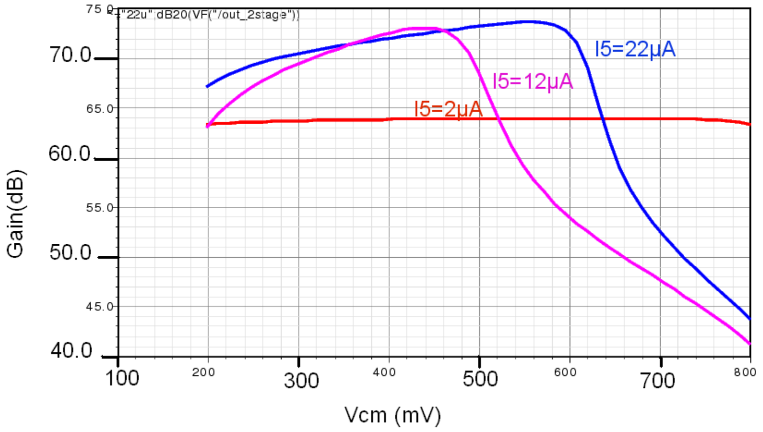

Figure 4.9: Gain of the amplifier in function of input common voltage for different currents I_5, $V_{DD} = 1.2V$

as in Figure 4.9, which is the perfect proof, why it is better to choose higher power supply than $1.2V$.

Optimisation of the two-stage amplifier

1. <u>second stage optimization</u>

   Let's consider if the second stage is really optimized. One of the designing rules is:

   $$2 \cdot \frac{S_4}{S_5} = \frac{S_6}{S_7} \tag{4.48}$$

   To explain equation 4.48,scheme 4.10 is helpful.

   On this scheme the inputs are connected to the same voltage and the input stage is becoming symmetrical. This gives us possibility to split the input stage into two equal parts.

   The output stage can be regarded as being made by two current generators: M_6 sinking the current injected by M_7.

   The two current sources have a high output impedance, so the output voltage approaches the value $\frac{V_{DD}-V_{SS}}{2}$ only if the two currents I_{M6} and I_{M7} are almost equal. Because the current in M_4 is a replica of the current in M_5 the equation 4.48 has to be verified.

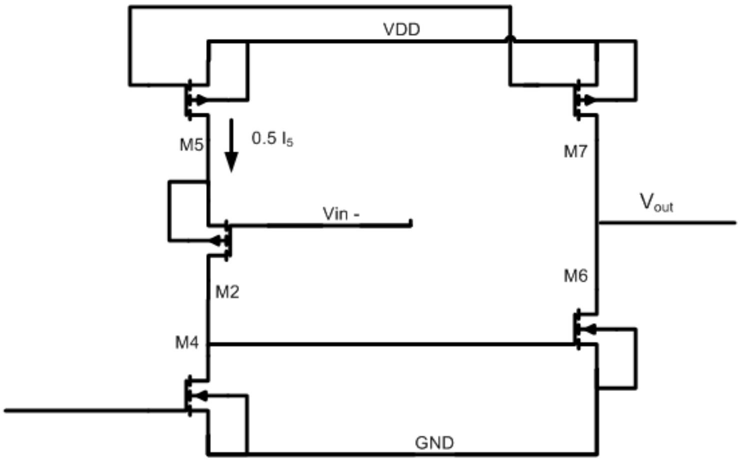

Figure 4.10: Scheme of two-stage amplifier for the common mode signal analysis

And for our aspect ratios: $2 \times \frac{40}{5} = \frac{394}{25}$ so $16 \approx 15.76$.

The result above is very good if we remember about integer values of micrometers for every transistor and we can say that the second stage is optimized.

Moreover, remember that equation 4.48 assumes the use of ideal current mirrors. Because of the transistor's finite output resistance the current in one branch and its mirrored replica do not match perfectly. Thus, even if the above condition is respected, the slight mismatch between the currents in M_5 and M_6 causes a residual offset. Of course, we can trim the transistor sizing and bring the residual offset to zero with simulations. However, this is not advisable for two reasons: zeroing results achieved with a given simulation condition are not exactly verified in the experimental verifications. A second reason, is that for optimizing the layout we need transistors with properly ratioed widths. Often the results of the trimming process is unreal transistor sizing which makes the layout problematic and irregular. [24]

To sum up, second stage is designed correctly.

2. Add nulling resistor

   As the result of using nulling resistor a better gain-bandwidth is achieved.

   In bipolar implementations g_{m6} can be designed suitably larger than g_{m1}, while with CMOS we cannot achieve the same result easily. That is why zero often is close to the expected unity frequency(f_T) and modifies significantly the frequency response near zero dB, degrading the stability conditions.Usually we cannot leave our circuit as it is, but we try to increase phase margin. The influence of the zero in the right s - plane can be solved by the following three methods: [25]

(a) use a zero nulling resistor

(b) use a unity gain amplifier

(c) use an unity gain current amplifier

As a remedy of zero in the right s - plane we use the first solution.

The compensation is made by a series connection of a resistance and the compensation capacitance as in Figure 4.7.

$$z = \frac{1}{C_C\left(\frac{1}{g_{m6}} - R_Z\right)} \tag{4.49}$$

Now zero can be described as in Formula 4.49. We can see that depending on the R_Z, zero could be on the left or right side of the s - plane . When $R_Z = g_{m6}$ the zero goes to the infinity (is nulled). Having a zero on the left -s plane is also useful, achieving a pole - zero cancellation we enlarge the bandwidth of amplifier.

In our amplifier, pole-zero is deeply above unity frequency so it is not necessary to move it more in the infinity frequency. But we will try to move this pole-zero to the left side of the s-plane and enlarge the op-amp bandwidth.

Now we will design compensation circuitry so that the RHP zero is moved from the RHP to the LHP and placed on top of the output pole p_2.

$NR = 4500$ were chosen and then according to equation 4.49 $z_2 = 226 \times 10^6$. The AC simulation for amplifier with nulling resistor is shown in Figure 4.11. The gain-bandwidth is increased to the value 92MHz and phase margin is equal to 50^0.

The transient simulations for amplifier with nulling resistor and without nulling resistor are presented in Figure 4.12. Although nulling resistor increased GB almost three times, the transient response does not look better. Moving zero more to the LHP is not recommended because then phase margin is smaller than 45^0 and it is possible that after fabrication, the device would not work properly.

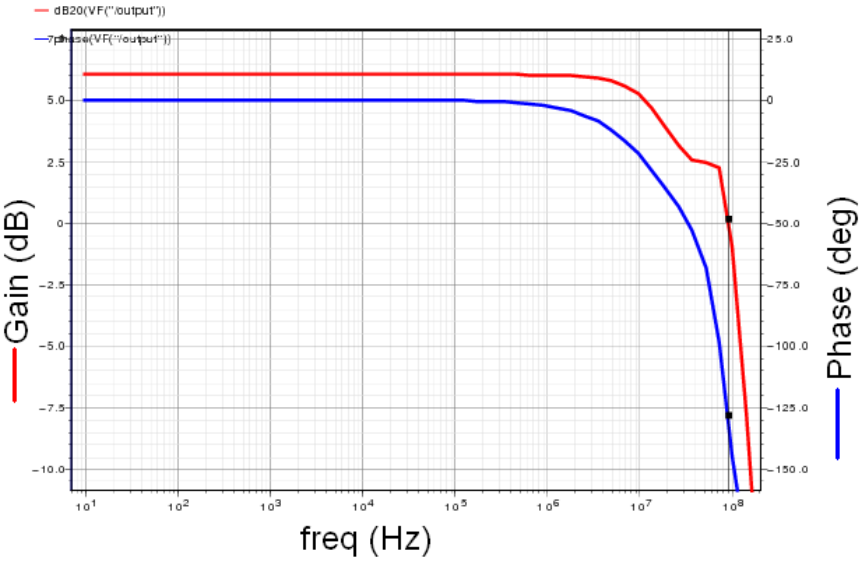

Figure 4.11: AC simulation of GB and PM for two-stage amplifier with nulling resistor $NR = 4500$

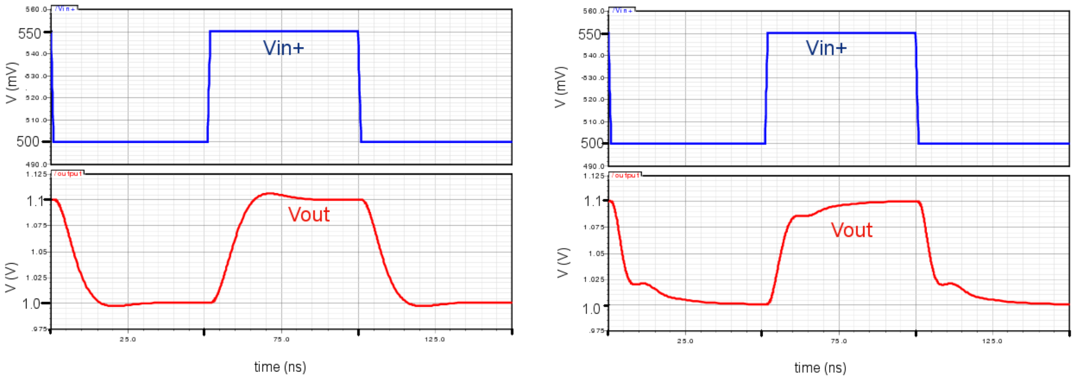

Figure 4.12: Transient simulations for amplifier without nulling resistor(left) and with nulling resistor NR=4500(right), frequency of input signal: 20MHz

The accuracy of integrated resistors is not really high, thus it is hard to get a pole-zero cancellation in practical case.

To sum up the author gives advice to use nulling resistor only to move zero pole to ∞. It is not an advisable method trying pole-zero cancellation by having a zero in the left s-plane.

4.5 LAYOUT

After calculations and scheme simulations the layout of the final amplifier will be designed.

There are some global rules for designing the layout: [15]

- Multifinger transistors

  Transistors matched well if they have the same lengths and widths. Even minimally matched devices should have identical channel lengths. Usually widths of transistor are large and different for almost every transistor, that is why they are divided into fingers. Each of these fingers should have exactly the same length and width.

  Transistors should be similar to square so if the transistor has one of the dimensions really bigger the multifinger transistors are solution to keep shape similar to square. Then the gate resistance is reduced.

- Connect gate fingers using metal lines

  Connect the gate fingers using metal rather than poly. Use poly only if simplifying of connections of the gate electrodes is crucial.

- Dummy transistors

  Dummy transistors are added at both sides of multifinger transistors. Usually gate of dummy transistor is connected to bulk to ensure that the transistor is in the cut-off region. The roles of dummy transistor are: an electrostatic protection and improving symmetry (every transistor see the same environment).

- A lot of bulk contacts, close to the transistor

- Cross coupling structures for large transistors and pair transistors

  Symmetry is especially important for large transistors to avoid mismatches. Also for pair transistors, like differential pair it is necessary to reduce mismatches. Common centroid(cross coupling) configuration as presented below in Figure 4.13 and Figure 4.14 is a very good solution.

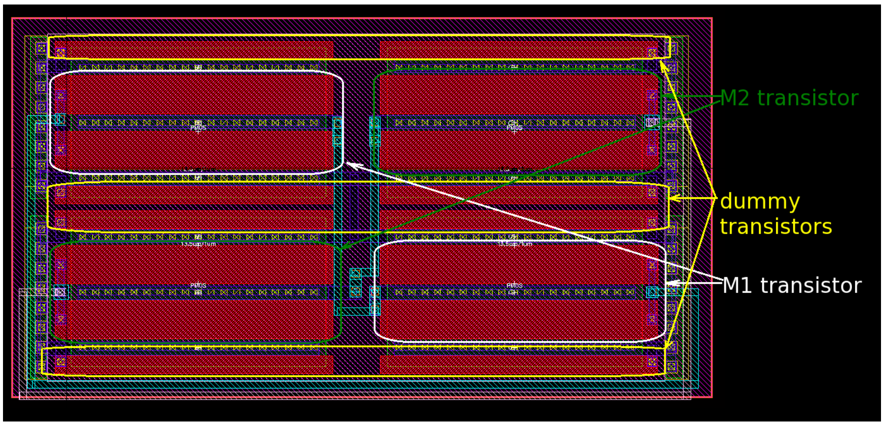

Figure 4.13: Layout of the differential pair transistor of the amplifier

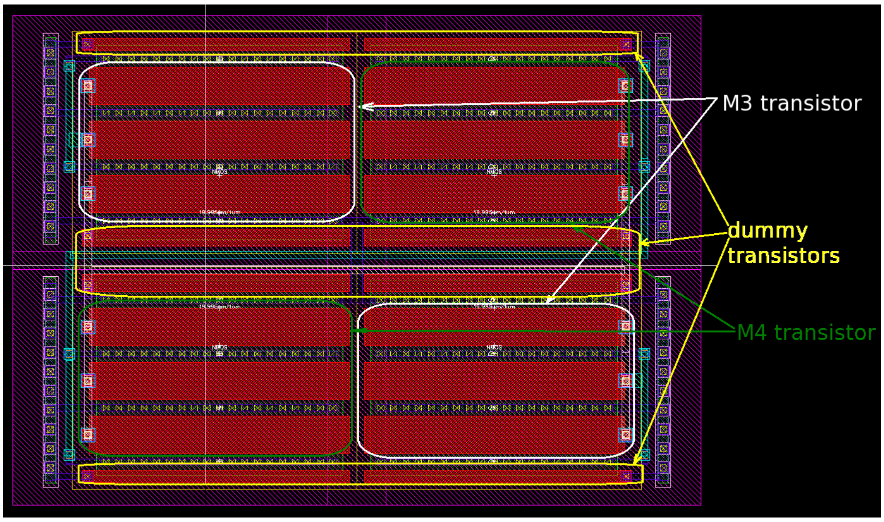

Figure 4.14: Layout of the mirror transistors of the amplifier

The idea is to decompose each transistor into two halves that are placed diagonally opposite of each other and connected parallel. However, this configuration is not simple to be implemented in a proper way, especially if the transistors are multifinger transistors.

The symmetry should be not only between transistors but also between wires. To connect differential pair transistors and mirror transistors in a configuration cross coupling, three different metal wires were used. It causes capacitances from the wires to ground and between wires. Also these capacitances are expected to be symmetrical.

- The same orientation for transistors

  Also the same orientation is important for good matching as it is in Figure 4.15 demonstrated in which current transistors: M_5, M_7 and M_8 are presented.

  Transistors that do not lie parallel become more vulnerable to tilt- or stress-induced mobility variations that cause variations in their transconductance.

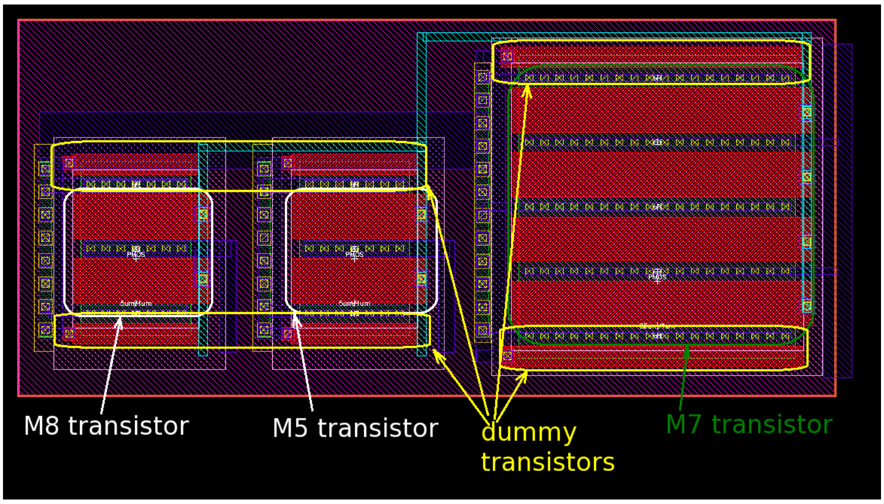

Figure 4.15: Layout of the current transistors of the amplifier

- Transistors in close proximity and compact devices

  MOS transistors are vulnerable to gradients in: stress, temperature and oxide thickness. Devices should reside to one another as close as designing rules makes it possible.

  Common-centroid and multifingers techniques gives possibility to decrease vulnerability to gradient. But this cannot entirely eliminate this unfavourable effect. Therefore the designer should make an effort to create as compact and well organized layout as possible.

- Do not route metal across the active gate region

  If only it is possible, avoid routing metal across the active gate region of precisely matched MOS transistors. In the other case add dummy metals in the same location on each transistor.

Passive elements

Resistors and capacitors that are elements which are not easy to be precisely fabricated into integrated circuits. That is why the general rule is to use these elements only if they are really necessary.

It was essential to use two resistors as a closed loop. Poly resistors were chosen because they have the biggest resistance per square.

Capacitance is the biggest element of amplifier. Its a Metal-Insulator-Metal (MIM) capacitor with a capacitance $2fF/\mu m^2$. There are possibilities to use other kinds of capacitors which have bigger capacitances but one cover of this capacitance is a bulk and for this amplifier that kind of capacitor is useless. It would be possible to adopt capacitor with one cover as a bulk if we were sure that one cover is always on higher potential than the second one. But for out amplifier this assumption is not right.

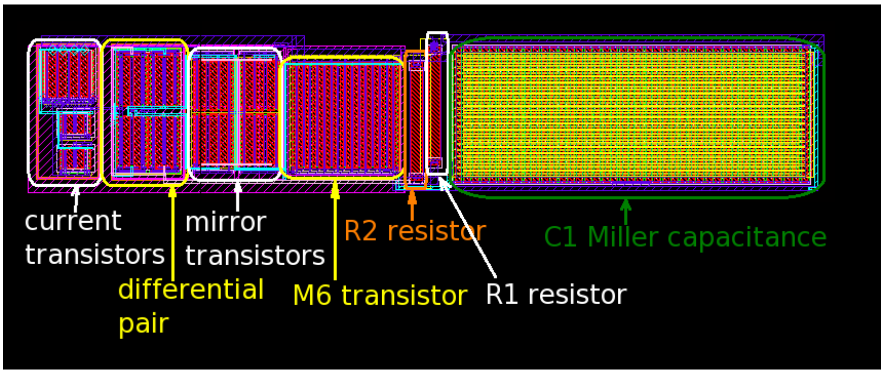

Figure 4.16: Layout of the amplifier

The dimensions of whole amplifier are $111\mu m \times 23\mu m$.

Oblong structure of amplifier was chosen, because then it is easier to find place and suit this amplifier in the chip architecture.

4.6 POSTLAYOUT SIMULATIONS

Next design step is a postlayout simulation. In Table 4.2 results of simulations are collected and presented. The amplifier was simulated for whole ICMR and for two different currents: $I_0 = 100\mu A$ because this current was chosen in section 4.4 and $I_0 = 200\mu A$ because then GB is bigger.

The results for these two differents currents are shown in Figure 4.17.

Table 4.2: Parameters of the two-stage amplifier with closed loop

	GB	PM
100μA, sch. sim.	$41 \div 43$MHz	$60^0 \div 68^0$deg
100μA, postlay. sim.	$39 \div 42$MHz	$64^0 \div 70^0$deg
200μA, postlay. sim.	$53 \div 54$MHz	$72^0 \div 76^0$deg

The disadvantage of increasing I_0 is decreased open loop gain. As it was presented in Figure 4.18 even for $I_0 = 100\mu A$ gain is not large, especially for small input common voltage. After increasing this current, better gain-bandwidth, better phase margin and better transient response was achieved. But then, for small input common voltage, open loop gain is not enough and closed loop gain do not amplify exactly two times so amplifier does not work as the ideal one.

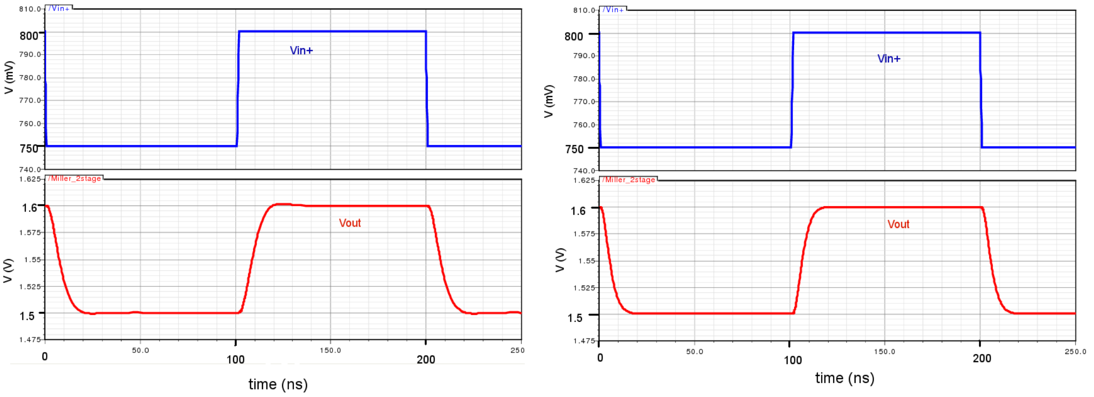

Figure 4.17: Transient simulations for $I_0 = 100\mu A(left)$ and $I_0 = 200\mu A$ (right) for 10MHz input signal

In Figure 4.19 schemes simulations and postlayout simulations are compared.

Monte Carlo simulations.

After checking that amplifier is working and assumptions are done it is time to check if it works after fabrication. To estimate the probability that the amplifier will work

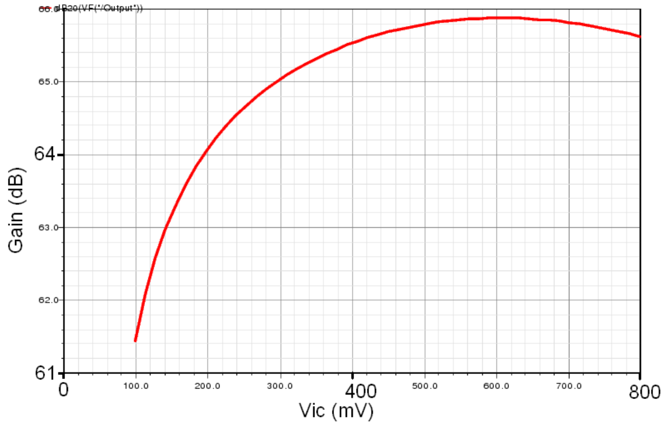

Figure 4.18: Gain of the amplifier in function of input common voltage

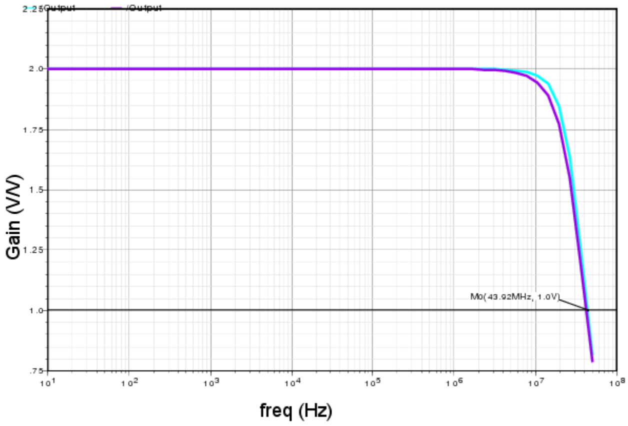

Figure 4.19: AC simulations of the scheme(color blue) and layout(color navy-blue)of the two-stage amplifier in closed loop configuration

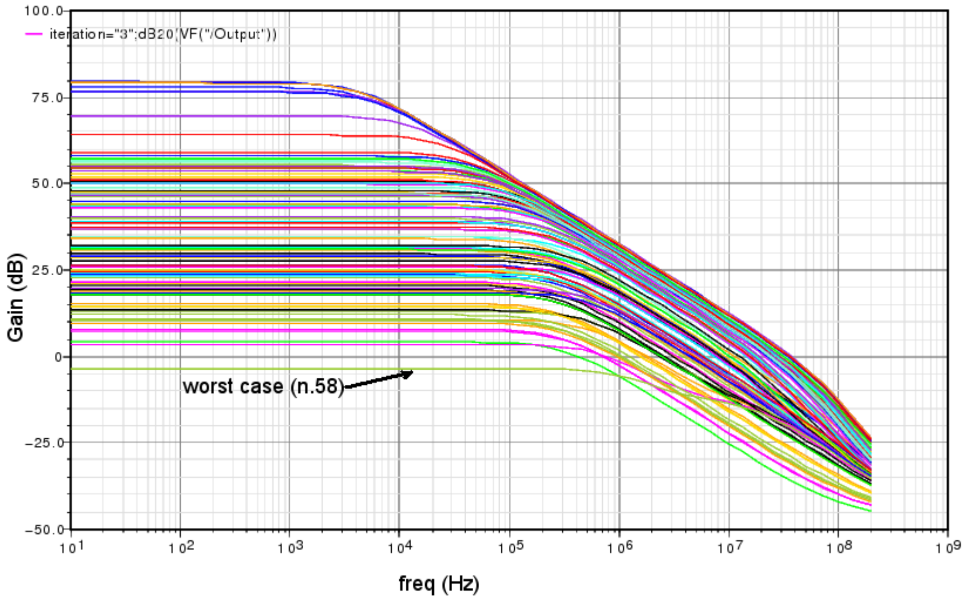

Figure 4.20: Monte Carlo AC simulation for open loop configuration

correctly, Monte Carlo simulations are used. The Monte Carlo simulations for open loop amplifier are shown in Figure 4.20. It shows that only for 5 from 100 different Monte Carlo analyses the gain is bigger than $60dB$. But it does not mean, that this amplifier is working with probability 5%. The same Monte Carlo simulations but for amplifier with closed loop give 100% chances for working correctly and therefore satisfying results for transient simulations are observed as in Figure 4.21.

The question is why the amplifier works with closed loop even if with open loop the differential gain is really small (for one Monte Carlo simulation even smaller than $0dB$)?

To answer, let's consider which transistors are the most sensible for every mismatches. They are mirror transistors. For example, let's make assumption that after fabrication length of transistor M_4 is not $1\mu m$ as it should be but is equal to $0.9\mu m$.

Then, for open loop amplifier, V_{DS} gets smaller and as a result the bias point of transistor M_6 is changed greatly. Transistor M_6 is cut off, the amplifier does not work properly and as a result very small differential gain is given, as in Figure 4.20.

But for the closed loop amplifier mismatch of transistor M_4 does not cut of transistor M_6. Closed loop resistors give self compensation. If the length of transistor M_4 is smaller, then to omit this mismatch value of Vin- is not equal to Vin+ but a little bit lower and as a result the current which flows through transistors M_4 and M_2 is bigger

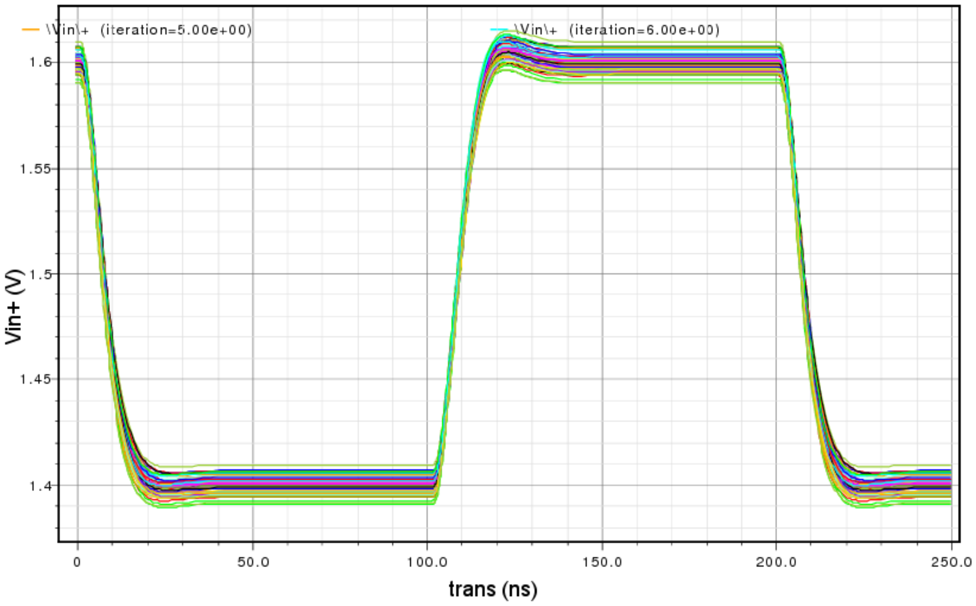

Figure 4.21: Monte Carlo transient simulation for closed loop configuration

than current of transistors M_1 and M_3. Bigger current I_4 ensures proper bias voltage for transistor M_6.

The easiest way to check this theory in practice was to choose one Monte Carlo simulation. Simulation number 58 was chosen, as shown in Figure 4.20. For open loop configuration the gain is even smaller than $0dB$. Next, this simulation number 58 was executed for closed loop amplifier and value of Vin- were measured. Vin- is not like $Vin+ = 0.8V$ but is $2.5mV$ bigger. After that, ones again simulation number 58 was executed for open loop amplifier but with $Vin- = 0.8025mV$ and $Vin+ = 0.8$. The gain was about $65dB$ as it was expected and which is the proof of self compensation theory.

But in spite of self-compensation of the closed loop amplifier, there are disadvantages of dispersions. Every mismatch and difference between both inputs of amplifier generate input offset. After Monte Carlo simulations the input offset not bigger than $5mV$ is expected, as in Figure 4.22.

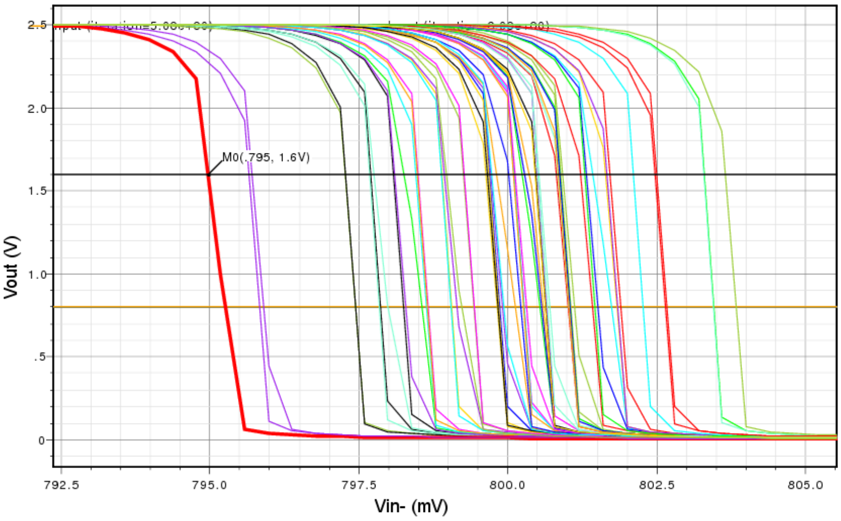

Figure 4.22: Input offset of V_{in-} in Monte Carlo AC simulation for open loop configuration, $V_{in+} = 0.8$

Chapter 5

AMPLIFIER WITH OUTPUT BUFFER

5.1 DESCRIPTION OF OUTPUT BUFFER AND REGULATED CLOSED LOOP GAIN

The parameters of amplifier in the previous chapter are enough for assumptions. But let's think if it is possible to design an amplifier which would have better parameters and similar dimensions. The solution is to decrease output capacitance of the amplifier using output buffer as in Figure 5.1. Therefore Miller capacitance can be smaller as well.

As an output buffer p-channel source follower configuration is chosen. Source follower provides current gain but voltage gain is almost unity. It is a noninverting buffer which assures also low output impedance. Designing source follower as in Figure 5.2

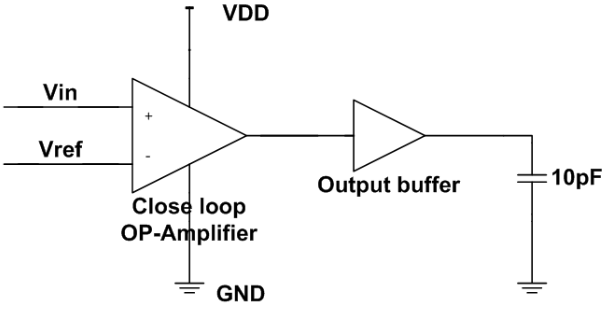

Figure 5.1: Amplifier with output buffer to decrease influence of output capacitance (10pF)

it is necessary to consider two discrepancies:

1. large aspect ratio of transistor M_9 to ensure high current and as a result gain-bandwidth not smaller than GB of the amplifier
2. large value of $M8/M9$ to get similar gain for the whole ICMR $(0.2V \div 1.6V)$

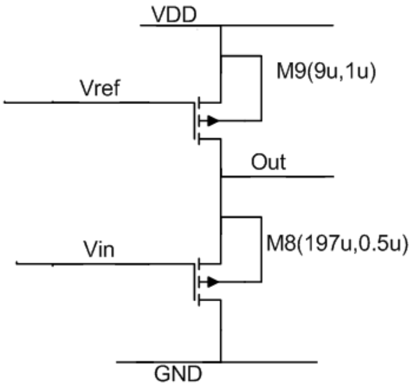

Figure 5.2: Scheme of the output buffer

The result of compromise between two above discrepancies is shown in Figure 5.3. Reference voltage is about $0.5V$ and to the two-stage amplifier's mirror transistors gate is connected. Then to assure proper work of output buffer no extra pins are needed.

The ideal situation is if for every value of input voltage small signal gain is the same.

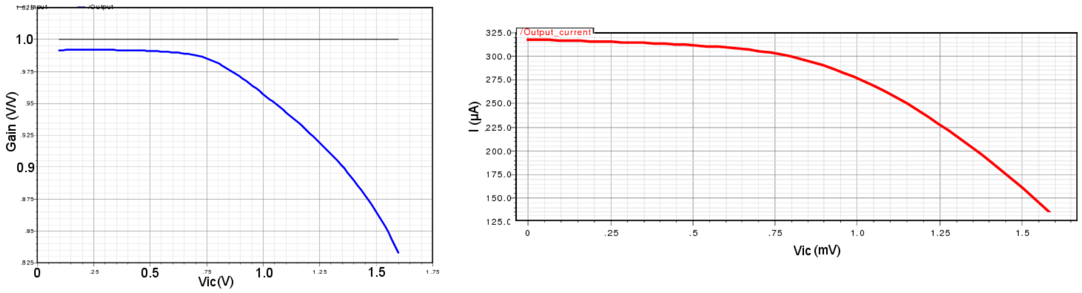

Figure 5.3: Parameters at the output of the output buffer in the function of input voltage: AC gain(left) and current(right)

Constant gain, almost unity, is achieved for input voltage $0.1V \div 0.7V$ and for higher input voltage is decreased as in Figure 5.3. To assure constant gain for input voltage $0.1V \div 1.6V$ it is necessary to decrease current but therefore bandwidth of output buffer is insufficient.

The result of using output buffer is amplifier's output capacitance not $10pF$ but $1pF \div$

$5pF$.

Other disadvantage of amplifier from the previous chapter was gain equal to 2 as a result of leakage current's unknown value.

Now it is possible to choose value of gain as it is shown in Figure 5.4. For large leakage current input voltage is changing from $0.1V$ to $0.8V$ and then gain of 2 is chosen:

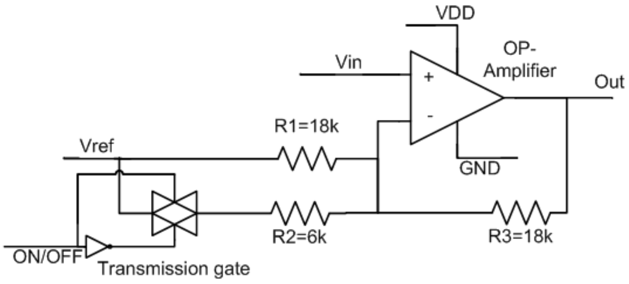

Figure 5.4: Scheme of the amplifier with possibility to choose gain: 2 or 5

OFF: $V_{out} = A_V \frac{R_3+R_1}{R_1} = \frac{18000\times 18000}{18000+18000} = \mathbf{2}$

If the leakage current is smaller then gain of 5 is possible:

ON: $R_{1\|2} = 18000\|6000 = 4500\Omega$, $V_{out} = A_V \frac{R_3+R_{1\|2}}{R_{1\|2}} = \frac{18000+4500}{4500} = \mathbf{5}$.

In spite of another amplifier outside the chip it is better to amplify signal on the chip as much as possible, because outside the chip noises are bigger.

Transmission gate used is the same as the one in Section 3.4.

5.2 SCHEMATIC

The consequence of adding the output buffer is smaller output capacitance of the amplifier. Therefore it is possible to modify the amplifier from Chapter 4. Two times smaller load capacitance gives opportunity to decrease Miller capacitance also two times. It was decided to decrease Miller capacitance from $1pF$ to $0.8pF$. Moreover, aspect ratio of differential pair transistors is changed from 27 to 72.

As a result larger gain and gain-bandwidth is expected.

Results are presented in Table 5.1.

Almost two times better gain-bandwidth is achieved as it was expected. Increase of GB is especially necessary if the gain is not 2 but 5. Besides, PM is better as it was in

Table 5.1: Parameters of the two-stage amplifier with output buffer($C_L = 1pF \div 5pF$)

parameters	calculating	after scheme sim.	after postlayout sim.
$M_1(W_1, L_1)$	72μm,1μm	72μm,1μm	72μm,1μm
$M_3(W_3, L_3)$	40μm,1μm	40μm,1μm	40μm,1μm
$M_5(W_5, L_5)$	5μm,1μm	5μm,1μm	5μm,1μm
$M_6(W_6, L_6)$	197μm,0.5μm	197μm,0.5μm	197μm,0.5μm
$M_7(W_7, L_7)$	25μm,1μm	25μm,1μm	25μm,1μm
$M_8(W_8, L_8)$	200μm,0.5μm	197μm,0.5μm	197μm,0.5μm
$M_9(W_9, L_9)$	8μm,1μm	8μm,1μm	8μm,1μm
I_5, I_7	100μA,500μA	$99.7\mu A, 398\mu A$	-
I_9	-	$150mA \div 320mA$	$155mA \div 320mA$
$Gain$	$60dB$	$59dB \div 67dB$	$60 \div 67dB$
GB	$200MHz$	$72MHz$	$72MHz$
f_{3dB}	-	$24kHz \div 50kHz$	$24kHz \div 51kHz$
PM	$> 60^0$deg	$61^0 \div 67^0$deg	$60^0 \div 67^0$deg
$CMRR$	-	$94dB$	$93dB$
$PSSR$	-	$74dB$	$74dB$
$Slew\ Rate$	$100V/\mu s$	$56V/\mu s$	$56V/\mu s$
$RMS\ noises$	-	$325\mu V$	$325\mu V$
$Power\ diss.$	$1.5mW$	$1.2mW$	$1.3mW$

the previous configuration. Also value of Slew Rate for amplifier with output buffer is increased.

Gain is roughly the same as it was in the previous chapter which is the proof that there is a limit for large aspect ratio of differential pair transistors and further increase of this value does not improve the gain of the whole amplifier.

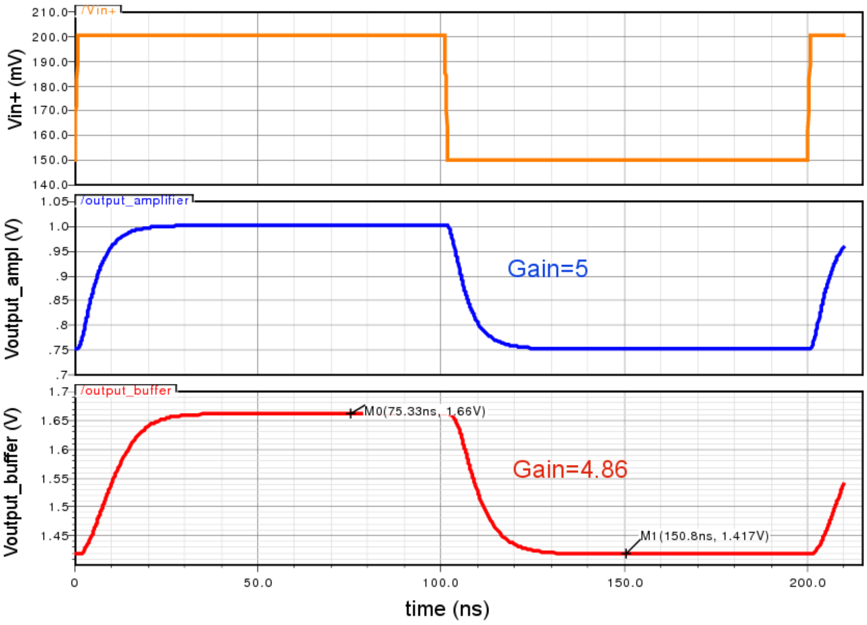

Figure 5.5: Transient simulations, input signal 10MHz and response at output of the amplifier and output of the buffer

In Figure 5.5 transient response to the input signal on the output of the amplifier and output of source follower is presented. The input signal at the output of amplifier is exactly 5 times amplified. At the output of buffer the signal is 4.86 times amplified because of the source follower's gain equal to 0.97.

5.3 LAYOUT AND POSTLAYOUT SIMULATIONS

While designing layout only differential pair has to be made once again as in Figure 5.6.

The design rules from the previous chapter are used to design this differential pair. There are multifinger transistors and cross coupling structures which is common for

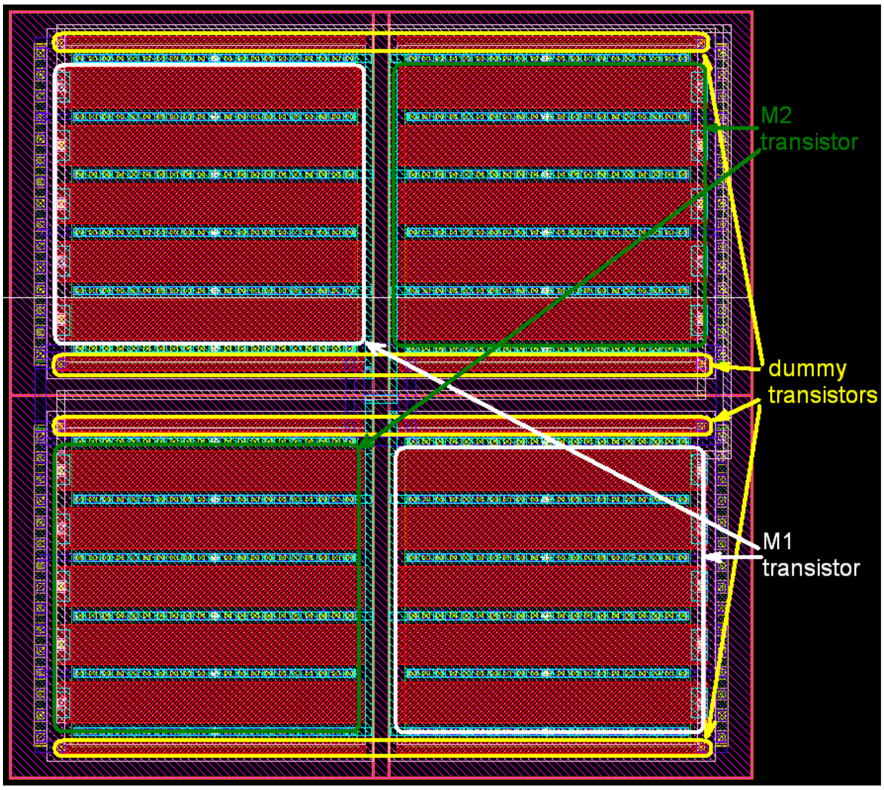

Figure 5.6: Layout of the differential pair transistor of amplifier with output buffer

pair transistors. Apart from dummy transistors and metal lines as a gate fingers connections are used. Also a lot of bulk contacts, close to the transistors and the same orientation for transistors is presented in Figure 5.6.

The whole layout of the amplifier with output buffer is shown in Figure 5.7.

The area of layout is $131\mu m \div 22\mu m$.

The dimensions of the amplifier from the previous chapter are similar ($111\mu m \div 23\mu m$), so it was possible to get better parameters of the amplifier and keep similar layout area.

Transient simulations of possible input signal are presented in Figure 5.8.

Input value is decreased because of leakage current. If the signal was registered on the pixel then as a result value of the signal on this pixel is higher than neighbouring pixels.

According to the above transient simulation, Monte Carlo simulations are done and the results are shown in Figure 5.9.

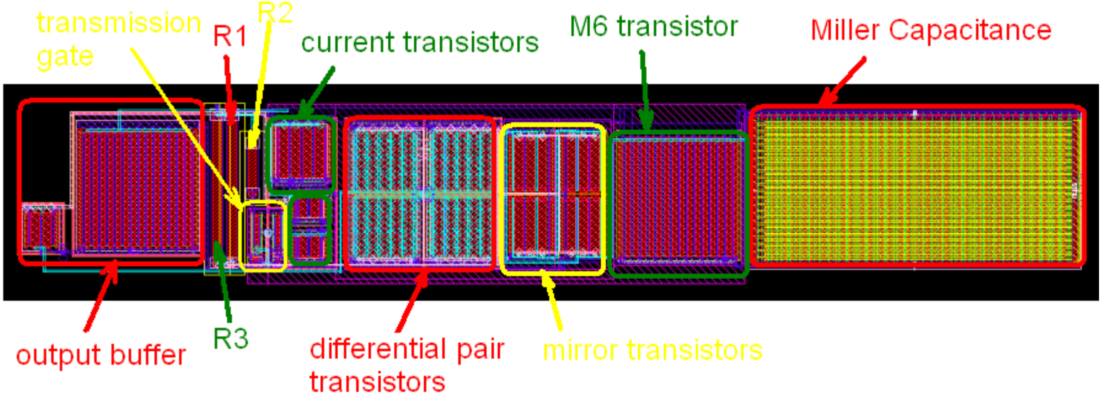

Figure 5.7: Layout of the amplifier with output buffer

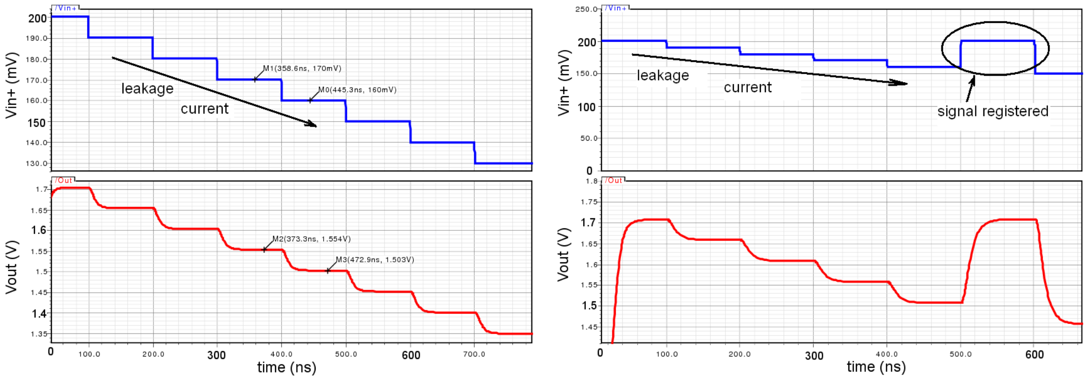

Figure 5.8: Transient simulation of the amplifier with possible input signal from pixel matrix when none of the pixels registered the signal(left) and when one pixel registered the signal(right)

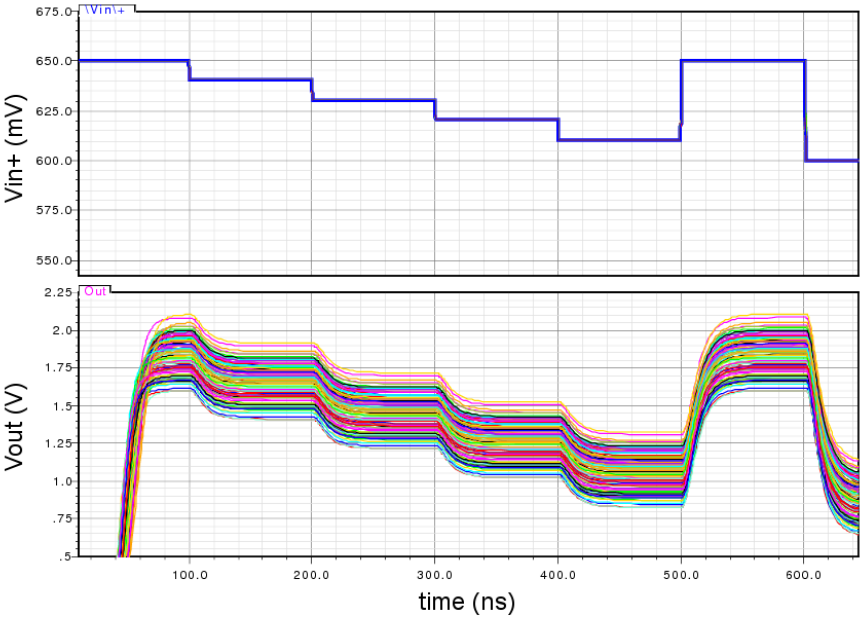

Figure 5.9: Monte Carlo transient simulation of an amplifier with an expected input signal from pixel matrix when one pixel registered the signal

Chapter 6

FOLDED-CASCODE AND OTHER CONFIGURATIONS OF AMPLIFIER

6.1 DISADVANTAGES OF AMPLIFIER IN OTHER CONFIGURATIONS

In the previous chapters two-stage amplifier is presented. But for the author of this thesis it was not obvious at the begining that the best performances are achieved when this configuration is used. A lot of attempts were done for other configurations. In this chapter some helpful general rules are given to choose a proper architecture of the amplifier. Folded-cascode amplifier is precisely described as an example of an unsuccessful attempt of designing amplifier.

Discussion about some ideas, which give insufficient results:

- *Add one more stage, three stage amplifier should ensure gain about* $90dB$.
  There are applications in which it is difficult to achieve satisfying gain. Especially if a large current is necessary. Then the designer could try to solve this problem by adding one more stage.
  It is important to know that every stage gives not only better gain but especially extra dominant poles. Therefore, frequency compensation becomes complex. That is why unless it is absolutely desired, more gain stages should be avoided.
  If the above argument is not convincing enough there is one more disadvantage

of adding extra stages: the output stage is a common source NMOS amplifier with current sink load and requires input bias point's difference not more than $10mV$(then it is possible to achieve 40dB on this output stage and output swing is still smaller than the power supply: $10mV \times 40dB = 1V$). It is not a problem if its input is an output of a differential stage. But when input of this common source amplifier is an output of two-stage amplifier it is getting more complex. It is especially difficult to ensure proper bias point after the second stage if ICMR is big as it is in the author's assumptions concerning the amplifier.

- *Cascode in the first stage, commonly used in a lot of books and abstracts.*
  Cascode in the first stage increases the output resistance of the first stage significantly and as a result ensures better gain. By adding one cascode pair it is possible to increase gain at about $10dB \div 20dB$. Other advantage of cascode is that stacking cascode transistors reduce output voltage swing.
  But remembering about ICMR voltage the uselessness of adding cascode gets obvious. It is a problem to ensure input common voltage $100mV$ even with no cascode as it is shown in Equation 4.31 and in Figure 4.18. So any cascode in the first stage is completely useless.

- *Cascode in the second stage.*
  If it is hard to add cascode in the first stage, usually there is possibility to add cascodes in the second stage to improve amplifier's gain.
  The author does not advise adding cascodes in the second stage of amplifier. The argument that the output impedance of the amplifier should be very low is the best explanation. Moreover, usually adding cascodes current of the second stage is limited and output stage becomes more complex to design.

- *Folded-cascode amplifier as a remedy for minimum input common voltage.*
  Folded-cascode sounds a good solution especially if low input voltage is a problem. This configuration is popular for devices with capacitive-only loads. Miller compensation is not needed. In this way the largest and less precise element for amplifiers in previous chapters is avoided.
  Unfortunately, the results of folded-cascode amplifier are not better than for two-stage amplifier designed in the previous chapter. It is difficult to ensure proper gain-bandwidth. Also gain is not sufficient. Even for gain $78dB$ amplifier does

not work like an ideal one. It means that for the author's assumptions this configuration is not better than the two-stage amplifier.

6.2 FEATURES OF FOLDED-CASCODE AMPLIFIER[4]

In Section 6.1 advantages and disadvantages of folded-cascode amplifier were shortly described. Here they are more precisely discussed.
One stage folded-cascode amplifier uses cascode in the output stage combined with an unusual implementation of differential stage to achieve a good input common-mode range as in Figure 6.1.
Low input common voltage becomes a problem for a standard two-stage amplifier configuration, as it is described in Section 4.4. A folded-cascode amplifier could be a solution to this difficulty.
To explain how the folded-cascode amplifier works see Figure 6.1.

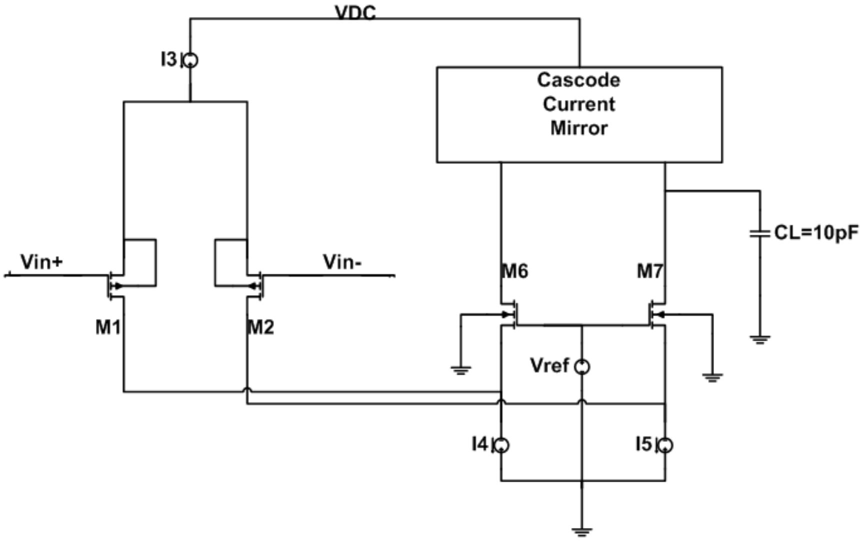

Figure 6.1: Simply version of one stage folded-cascode amplifier

This figure shows p-channel differential amplifier with a current-sink load. For a configuration with current mirror in the two-stage amplifier's differential stage $ICM_{min} = V_{GS3} - V_{TN}$ as in Figure 4.7, therefore with folded-cascode its $ICM_{min} = V_{DS4} - V_{TN}$ and gives possibility of working for lower input common voltage.
To achieve a better gain cascode current mirror is used.

Another optimistic feature is that folded-cascode amplifier does not require perfect bias of current in differential pair, because excess of DC current can flow out or into current mirror.

Also the power-supply rejection ratio has been improved in comparison with the amplifier in previous chapter. [5]

The disadvantage of folded-cascode configuration is difficulty to get single-ended output voltage without losing half of the gain.

Practical implementation of folded-cascode amplifier is presented in Figure 6.2.

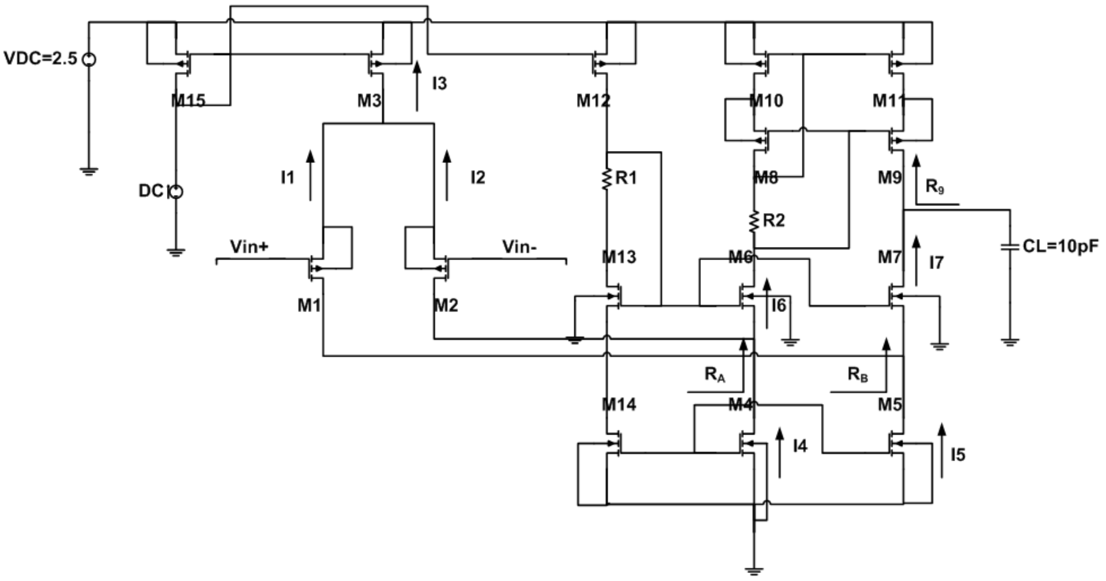

Figure 6.2: Scheme of the one stage folded-cascode amplifier

Using the small-signal differential-input voltage gain which is shown in Figure 6.3

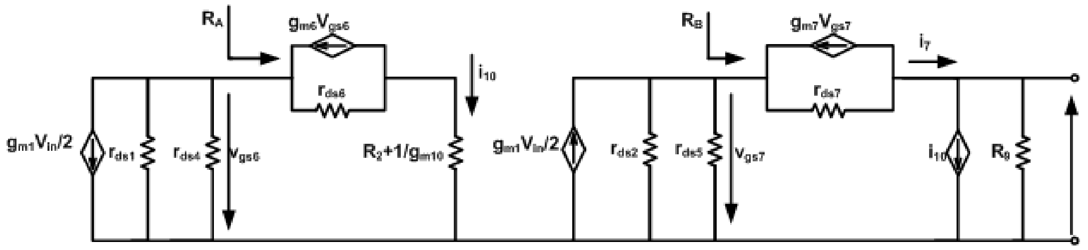

Figure 6.3: Small signal circuit of the one stage folded-cascode amplifier

the resistances looking into the sources of M_6 and M_7 are calculated in the equations 6.1 and 6.2.

$$R_A = \frac{r_{ds6} + R_2}{1 + g_{m6} r_{ds6}} \approx \frac{1}{g_{m6}} \tag{6.1}$$

and

$$R_B = \frac{r_{ds7} + R_9}{1 + g_{m7} r_{ds7}} \approx \frac{R_9}{g_{m7} r_{ds7}} \approx r_{ds} \tag{6.2}$$

where: $R_9 \approx g_{m9} r_{ds9} r_{ds11}$.

The equations for currents i_6 and i_7 are written in Formulas 6.3 and 6.4.

$$i_6 = i_{10} = \frac{-g_{m1}(r_{ds1} \| r_{ds4}) v_{in}}{2\left[R_A + (r_{ds1} \| r_{ds4})\right]} \approx \frac{-g_{m1} v_{in}}{2} \tag{6.3}$$

and

$$i_7 = i_{11} = \frac{g_{m2}(r_{ds2} \| r_{ds5}) v_{in}}{2\left(\frac{R_9}{g_{m7} r_{ds7}} + (r_{ds2} \| r_{ds5})\right)} = \frac{g_{m2} v_{in}}{2\left(1 + \frac{R_9(g_{ds2} + g_{ds5})}{g_{m7} r_{ds7}}\right)} = \frac{g_{m2} v_{in}}{2(1+k)} \tag{6.4}$$

where k is a low-frequency unbalance factor given by:

$$k = \frac{R_9(g_{ds2} + g_{ds5})}{g_{m7} r_{ds7}} \tag{6.5}$$

and usually parameter k is greater than one. The **output voltage** to the sum of currents i_7 and i_{10} is flowing through output resistance R_{II} and therefore **differential gain** is given as equation 6.6.

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2(1+k)}\right) R_{II} = \left(\frac{2+k}{2+2k}\right) g_{mI} R_{II} \tag{6.6}$$

where the **output resistance** R_{II}:

$$R_{II} \approx g_{m9} r_{ds9} r_{ds11} \| \left[g_{m7} r_{ds7} (r_{ds2} \| r_{ds5})\right] \tag{6.7}$$

Easier and more useful in calculation version of differential gain is: [7]

$$A_v(0) = \frac{g_m}{\frac{g_{02} + g_{09}}{g_{m4} r_{04}} + \frac{g_{05}}{g_{m7} r_{07}}} \tag{6.8}$$

The **frequency response** is determined the most by the **output pole**,which is the dominant pole and it is given by:

$$p_1 = \frac{-1}{R_{II} C_L} \tag{6.9}$$

Situation when the other poles are above GB is desired. The **first nondominant poles** are located at nodes A, B and are defined by formulas:

$$p_A \approx \frac{-1}{R_A C_A}, \tag{6.10}$$

$$p_B \approx \frac{-1}{R_B C_B}, \tag{6.11}$$

The other nondominant poles are drains of M_6, M_8, M_{10} and M_{11}. The expressions for each of these poles are:

$$p_6 \approx \frac{-1}{\left(R_2 + \frac{1}{g_{m10}}\right) C_6}, \tag{6.12}$$

$$p_8 \approx \frac{-g_{m8}}{C_8}, \tag{6.13}$$

$$p_9 \approx \frac{-g_{m9}}{C_9}, \tag{6.14}$$

and

$$p_{10} \approx \frac{-g_{m10}}{C_{10}}. \tag{6.15}$$

6.3 THE FOLDED-CASCODE AMPLIFIER - DESIGN PROCEDURE

After that, there is a moment to confront and adopt this configuration to the author's project.
First, assumptions are once again defined. They are the same as for the two-stage amplifier.
Assumptions:

- Power supply: **2.5V**
- Input common-mode voltage: **0.1V**$\div$ **0.8V**
  In previous chapter there were problems with designing an amplifier for $0.1V$. Folded-cascode configuration is a solution to these problems.
- Load capacitance: $1pF \div 10pF$
  This parameter can be chosen using output buffer. For calculations value **5pF** is used. If the phase margin is insufficient increasing load capacitance is a remedy.
- Slew rate: about **50V**$/\mu s$
- Gain and gain-bandwidth
  For previous configuration gain about $65dB$ and gain-bandwidth about 85MHz has been achieved. The purpose is to find the best configuration of amplifier therefore better or similar results for folded-cascode amplifier are expected.

GB=85MHz in calculation is used. This is also the best result for previous amplifier therefore it will be easy to compare transient response results for amplifiers in both architectures.

Design procedure: [6]

1. *Choose the smallest length of transistors.*

   Default length of transistors as **1**μm is chosen. But if aspect ratio of any transistor is large (150 or more) then length smaller than $1\mu m$ even for differential pair transistor is preferred. Therefore mismatches are bigger but for folded-cascode amplifier perfect symmetry of differential pair transistors is not required.

2. *Determine the value of current flowing through transistor M_3.*

   $$I_3 = SR \cdot C_L \tag{6.16}$$

   so $I_3 = 50 \times 10^6 \times 1 \times 10^{-12} = \boldsymbol{50}\ \mu A$

3. *Define bias currents in output cascodes.*

   Bias currents in output cascodes should be designed to avoid zero current in cascode. Imagine v_{in} so big, that M_1 is in saturation region but M_2 is in cut off region. As a result all I_3 current flows through transistor M_1, therefore $I_1 = I_3$ and $I_2 = 0$. If I_4 and I_5 are not bigger than I_3, then the current $I_6 = 0$. To ensure $I_6 > 0$ usually I_4 and I_5 between $1.2I_3$ and $1.5I_3$ are defined.

   $I_4 = I_5 = 1.5 \cdot I_3 = \boldsymbol{75}\ \mu A$

4. *Choose aspect ratio of differential pair transistors to achieve proper gain-bandwidth.*

   To calculate aspect ratio of differential pair transistors equations 6.17 and 6.18 are used.

   $$S_1 = S_2 = \frac{g_{m1}^2}{K_p' I_3} \tag{6.17}$$

   where:

   $$g_{m1} = GB \cdot C_L \tag{6.18}$$

   and aspect ratio $S_1 = S_2 = \frac{\left(85\times10^6\times1\times10^{-12}\right)^2}{1.17\times10^{-4}\times5\times10^{-5}}$ =***123***

5. *Define S_3 to achieve maximum input common-mode voltage.*

   In equation 6.19 how to estimate a proper value of aspect ratio transistor M_3 is described.

$$S_3 = \frac{2I_3}{K'_P\left[V_{DD} - V_{in}(max) - \sqrt{\frac{I_3}{K'_P S_1}} - V_{T1}\right]^2} \tag{6.19}$$

But it is easier to define S_3 using simulations. For defined ICMR the smallest possible S_3 is about 5 but to have possibility of working with greater current as $50\mu A$ value of ***20*** is chosen.

6. *Define aspect ratio of transistors M_4 and M_5 from minimum input common-mode voltage*

   To ensure working in saturation region for transistors M_4 and M_5 aspect ratio of this transistors has to be defined by equation 6.20.

   $$S_4 = S_5 = \frac{2I_4}{K'_N\left(V_{in}(min) + V_{T1}\right)} \tag{6.20}$$

   Also for this parameter it is better to choose proper value using simulation. For this assumption aspect ratio for transistors M_4 and M_5 as ***30*** was chosen.

7. *Define S_6, S_7, S_{13} and S_{14} to choose proper minimum output voltage*

   To have a possibility to decide what is the minimum output voltage equations 6.21, 6.22 and 6.23 are helpful.

   $$V_{DS5}(sat) + V_{DS7}(sat) = V_{out}(min) - V_{SS}, \tag{6.21}$$

   where from formula 4.10:

   $$S_7 = \frac{2I_7}{K'_N V_{DS7}^2} \tag{6.22}$$

   and

   $$S_4 = S_{14} = S_5 \tag{6.23}$$

   From equation 6.23 S_{14}=**30** was chosen.

   Using simulations as the analogy to formula 6.23: $S_6 = S_7 = S_{13}$ =**10**.

   Therefore from formula 6.21 $V_{out}(min) = 0.11V + 0.19V = 0.3V$.

   If the next stage at the output was added, then output voltage has to be precisely defined. But defining output voltage in this application is not crucial. The amplifier is going to work with closed loop and resistors will define the output voltage. So different value of $V_{out}(min)$ could be chosen as well. That is why it is a good design strategy of using simulations as method to choose proper dimensions of M_6, M_7 and M_{13} transistors.

8. *Choose S_8, S_9, S_{10} and S_{11} and as a result define maximum output voltage.*

   The same as in Point 7 also maximum output voltage is not a crucial parameter for closed loop configuration of amplifier. It is only convenient to have maximum output voltage larger than minimum output voltage. Important dependencies are: $S_{10} = S_{11}$ and $S_8 = S_9$.

   To simplify calculations all aspect ratios were chosen the same and are equal to ***30***. For this value great gain is achieved.

9. *Self-bias cascode.*

   To avoid external reference voltages for gates of transistors M_{13} and M_8 resistors R_1 and R_2 are used. To achieve proper voltages equations 6.24 and 6.25 are useful.

   $$R_0 = V_{SD13}(sat)/I_{12} \tag{6.24}$$

   so $R_0 = 0.358/0.000075 = 4774\Omega$

   and

   $$R_1 = V_{SD8}(sat)/I_6 \tag{6.25}$$

   therefore $R_1 = 0.169/0.00005 = 3375\Omega$.

   The above values after simulations for R_0 =**8000**Ω and R_0 =**6000**Ω were chosen because then the small signal gain was the greatest.

10. *Power dissipation.*

    When all parameters are defined it is important to check what is the value of power dissipation. Power dissipation is given by equation 6.26.

    $$P_{diss} = (V_{DD} - V_{SS})(I_3 + I_{12} + I_{10} + I_{11}) \tag{6.26}$$

    so $P_{diss} = 2.5V(50 + 75 + 50 + 50)\mu A$ =***562.5*** μW. This value of dissipation is acceptably small and any redesigning does not have to be done.

6.4 PROBLEMS WITH USAGE OF THE FOLDED-CASCODE AMPLIFIER

Parameters of folded-cascode amplifier are presented in Table 6.1. Values calculated and achieved during simulations are compared.

Table 6.1: Parameters of the folded-cascode amplifier, $C_L = 1pF$

parameters	calculating	scheme sim.
$M_1(W_1, L_1)$	123μm,1μm	120μm,0.5μm
$M_3(W_3, L_3)$	20μm,1μm	20μm,1μm
$M_4(W_5, L_5)$	30μm,1μm	30μm,1μm
$M_6(W_6, L_6)$	10μm,1μm	10μm,1μm
$M_8(W_8, L_8)$	30μm,1μm	30μm,1 μm
$M_{10}(W_{10}, L_{10})$	30μm,1μm	30μm,1μm
$M_{12}(W_{12}, L_{12})$	30μm,1μm	30μm,1μm
R_0, R_1	4.8kΩ, 3.4kΩ	8kΩ, 6kΩ
I_3, I_4, I_7	50μA, 75μA, 50μA	50μA, 83μA, 58μA
$Gain$	-	$77.5 \div 78.5dB$
GB	$85dB$	$72dB$
PM	$> 60^0 deg$	$65^0 deg$
f_{3dB}	-	$10kHz \div 12kHz$
$SlewRate$	50$V\mu s$	37$V/\mu s$
$RMS\ noises$	-	220μV
$Power\ diss.$	$562.5\mu W$	$622.5\mu W$

Gain parameter is better than for the two-stage amplifier. There are no problems for low input common voltage as it was expected. Also phase margin is satisfactory. Gain-bandwidth results are similar to the previous amplifiers. Dimensions of transistors and resistors give opportunity to design layout which is not larger than for previous amplifiers(111μm$\times$23μm) especially that no capacitors are used.

But in spite of such good parameters transient simulations reveal disadvantages of this configuration. In Figure 6.4(right) transient simulation for closed loop amplifier is presented.

Vin+ voltage should be two times amplified but output voltage differs from the expected value. It is a proof that the small signal gain of this amplifier is too small and the amplifier does not work as an ideal amplifier. For ideal amplifier Vin- and Vin+ are equal but in Figure 6.4(right) these inputs differ. For two-stage amplifier small signal gain about 60dB was enough but for folded-cascode even 78dB like in Figure 6.4(left) does not give sufficient results.

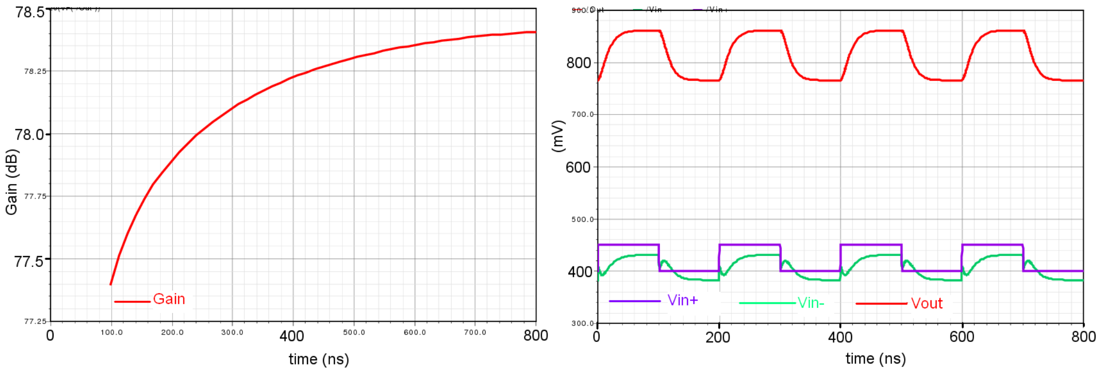

Figure 6.4: Small signal gain in function of input common voltage(left); Transient response for closed loop configuration, $gain = 2$, $f = 10MHz$(right)

In Figure 6.5 AC simulations of Gain and Phase for different load capacitances are shown.

Increasing C_L is a method of improving phase margin because the dominant pole is with the output associated as in Equation 6.9. The consequence of increasing load capacitance is smaller output pole, therefore smaller -3dB frequency and as a result smaller unity frequency as in Table 6.2.

But let's think how to design this amplifier and choose proper load capacitance if

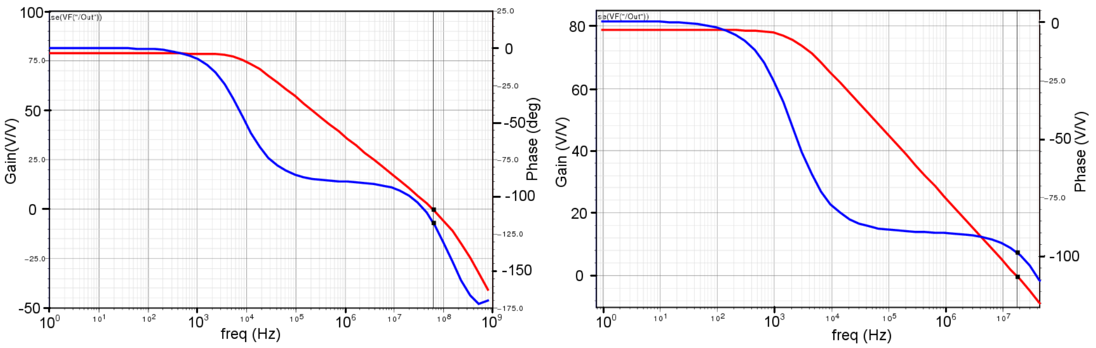

Figure 6.5: Gain and phase margin for AC simulations with load:1pF(left) and 5pF(right)

Table 6.2: Parameters of the folded-cascode amplifier for different load

Load	GB	PM	f_{-3dB}
1pF	72MHz	65^0deg	12kHz
5pF	16MHz	83^0deg	3kHz

the purpose is Gain-bandwidth about 100MHz. Of course it is possible to choose $C_L < 1pF$ but even for GB=72MHz phase margin was not large. As a solution first nondominant poles given by equations 6.10 and 6.11 have to be moved to higher frequency. It means that dimensions of transistors should be smaller because then C_A and C_B are decreased. The other method is to increase current flowing through transistors and as a result decreased R_A and R_B, but then small signal gain is going to be decreased as well.

Problems with not enough small signal gain and difficulties to achieve stable amplifier working for frequency about 100MHz gives basis to suppose that this configuration is not proper for author's assumptions.
Folded-cascode amplifier is a good example that for some amplifiers even 78dB is not sufficient, although two-stages configuration works as an ideal amplifier for small signal gain of 60dB. Also methods of phase compensation for these two configurations are totally different. It is the next proof that usually the best configuration is the simplest one.

All these insufficient results give possibility to get better knowledge about amplifiers and choose the best configuration.

Chapter 7

CONCLUSIONS

The aim of the thesis was to design output part of MAPS detectors: the Gray code decoders and the output amplifier.
Each pixel matrix on the chip differs and therefore it was necessary to design different Gray decoders for every matrix. Moreover, two methods of resetting pixels were suggested and for each pixel matrix two different Gray code decoders had to be implemented as well.
Besides, it was necessary to design an operational amplifier, working in a closed loop, non-inverting configuration with a gain about $2 \div 3$. The frequency of input signal is 10MHz.

The assumptions of the project are presented and realized.
Advantages of Gray coding are discussed and requirements for decoders are described. Schematic and layout of decoders are presented. Parameters of all decoders are collected in the tables.

The theory of an ideal amplifier is discussed and assumptions for author's amplifier are presented. Parameters of ST $0.13\mu m$ technology are calculated. Then equations and calculations useful during designing two-stage amplifier are shown. Scheme simulations and postlayout simulations including Monte Carlo simulations are presented and satisfying work of amplifier is proven. The results of scheme and postlayout simulations are collected in the tables and compared with assumptions. Global rules for designing layout of analogue circuits are described. Layout of amplifier is shown.
Then scheme and layout of the amplifier with output buffer, as a possibility of decreasing capacitance at the output of the amplifier is presented. Postlayout simulations,

especially Monte Carlo simulations are shown. The method of choosing gain of the amplifier is explained. Other architectures of amplifier are characterized and their disadvantages are discussed.

Moreover, the author of this thesis presents different types of detectors, especially MAPS detectors. Features of every type of these detectors are emphasized.
Method of measuring node capacitance is described.

Designed decoders and amplifiers will be used in the microchip.
The author believes, that this thesis will be helpful also in future projects and will be a good case-study of designing amplifiers.

List of Tables

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