MOS FET Operational Amplifier Introduction

Introduction

The MOSFET Operational amplifier is one of the most important circuits used in analogue design. This tutorial will discuss the basic features of a two-stage op-amp, define the equations required to meet specific design goals and most important of all the frequency response and stability of op-amps.

The basic MOS two-stage compensated OP-AMP – using a capacitive load is shown in Figure 1.

M6 sets the 'tail' current and by mirroring the bias current to the output stage. M3 and M4 form the differential amplifier – note P-type devices have been used as these have better noise performance. M5 is the current source for the differential amplifier and has been initially set in our example at 100uA, thus giving 50uA down each arm of the differential amplifier.

The current mirror formed by M1 and M2 'combine' the differential output voltage to give a single voltage output feeding into M8.

M8 is a simple current source inverter (M7 is the current source load for this amplifier) with miller compensating capacitor Cc (more on this later).

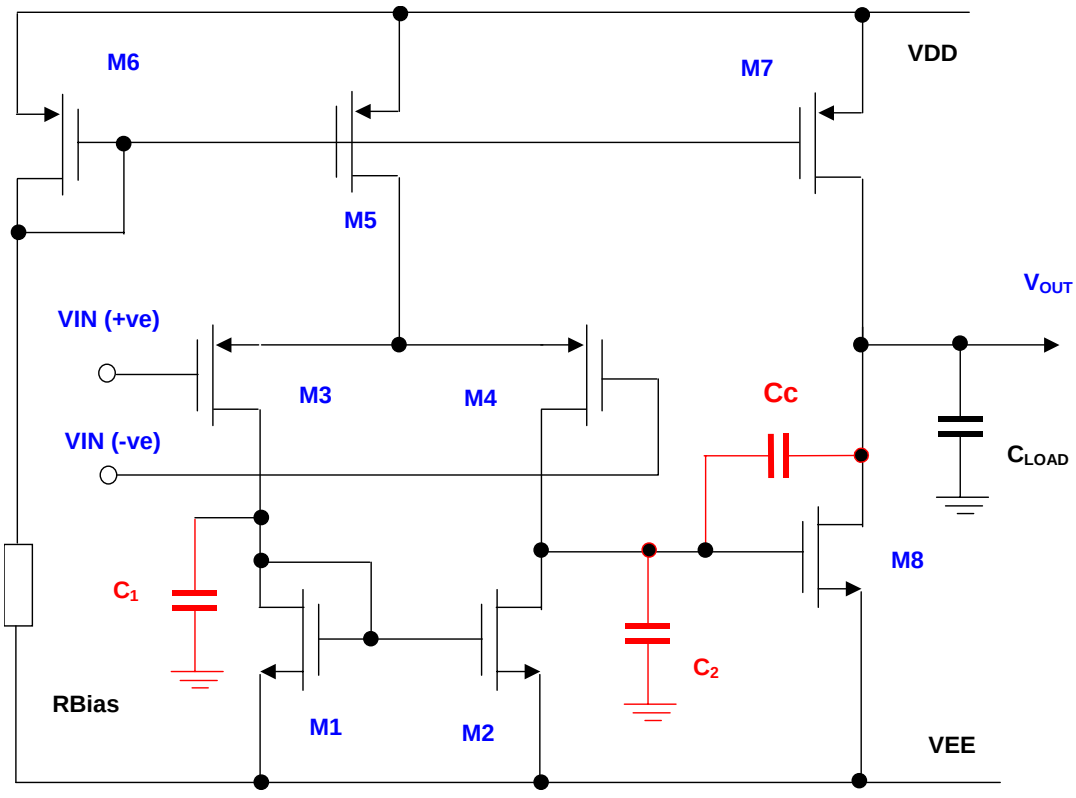

Figure 1 Simple Compensated OP-Amp circuit with capacitive load

Basic Design Drivers & Calculations

(1) Slew Rate

The slew rate is the non-linear ability of the op-amp to respond to a large stepped impulse on the inputs. Ideally a square waveform input should remain a square wave after amplification. The limitations of the op-amp cause the waveform edges to become ramped.

The slew rate is specified as a voltage attained after a preset time and is dependant on the tail current through M5 on the differential amplifier ie

$I_5 = S.R.\,Cc$ typical slew rates are 10V/us.

Generally if slew rate is not given as a design driver then settling time may be given instead. In this case use

$I_5 = 10(\text{Settling time}).\,Cc$

(2) Gain Bandwidth

The gain bandwidth is a function of the differential amplifier stage gm and the miller compensation capacitor Cc. ie

$G.B = \dfrac{gm3}{Cc}$ typical gain bandwidths are 5MHz

(3) First Stage Gain

The gain of the differential amplifier, is given by the product of gm3 and the load conductance

$$AV_{diff} = \frac{-gm_3}{go_2 + go_4} \quad \text{as} \quad go = gds = I_d.\lambda$$

$$AV_{diff} = \frac{-gm_3}{\frac{I_5}{2}(\lambda_2 + \lambda_4)} = \frac{-2gm_3}{I_5(\lambda_2 + \lambda_4)} \quad \text{as} \quad go = I_d.\lambda$$

(4) Second Stage Gain

The gain of the current source inverting amplifier, is given by the product of gm8 and the load conductance ie

$$AV_{O/P} = \frac{-gm_8}{go_7 + go_8} \quad \text{as} \quad go = gds = I_d.\lambda$$

$$AV_{O/P} = \frac{-gm_8}{I_7(\lambda_7 + \lambda_8)} = \quad \text{as} \quad go = I_d.\lambda$$

(5) Positive CMR V_{IN} MAX

$$V_{IC(MAX)} = V_{DD} - V_{SD5} - V_{GS3}$$

Where $V_{GS3} = \sqrt{\frac{Io}{2\beta_3}} + V_{T3}$ and $V_{DS5} = \sqrt{\frac{2Io}{\beta_5}}$

$$= V_{DD} - \sqrt{\frac{2I_0}{\beta_5}} - \sqrt{\frac{I_0}{2\beta_3}} - |V_{T3}|$$

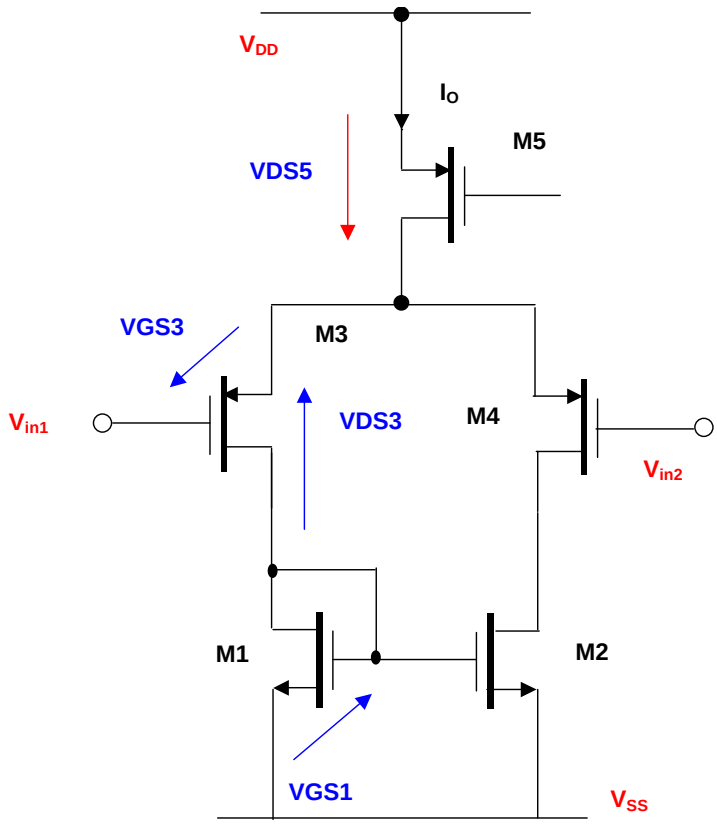

Figure 3 Showing PMOS Differential amplifier and the voltages effecting the maximum and minimum output voltages.

(6) Negative CMR V_{IN} (MIN)

This is the minimum output from the differential amplifier and is given by:-

$$V_{IC(MIN)} = V_{SS} + V_{GS1} + V_{DS3} - V_{GS3}$$

With Q3 in saturation $V_{DS3} = V_{GS3} - V_{T3}$

$$\therefore V_{IC(MIN)} = V_{SS} + V_{GS1} + (V_{GS2} - V_{T3}) - V_{GS3} = V_{SS} + V_{GS1} - |V_{T3}|$$

$$V_{GS3} = \sqrt{\frac{Io}{2\beta_3}} + V_{T1} \quad \text{Where} \quad \beta = K\frac{W}{L}$$

$$\therefore V_{IC(MIN)} = V_{SS} + \sqrt{\frac{Io}{2\beta 3}} + V_{T1} - V_{T3}$$

(7) Frequency Response & Stability

This section deals with the frequency response of an op-amp in relation to gain bandwidth product and phase-margin.

Figure 1 shows the three main capacitors that effect the frequency response of the op-amp C1, C2, C3 and CL.

(1) Input Load capacitor C1 – Figure 2

This capacitor consists of the parasitic capacitors around M1, M2 & M3. In most cases the bulk will be connected to VSS or VDD, which will be AC ground, so in fact these capacitors will all add together ie

Cgd3+Cdb3+Cgs1+Cgb1+Cdb1+Cgb2+Cgs2

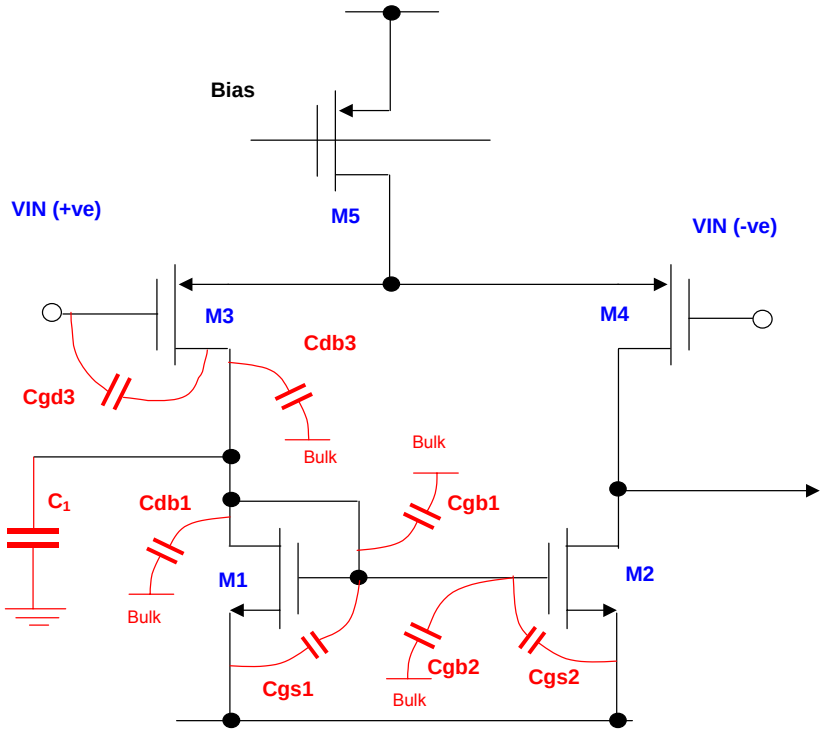

Figure 2 Input parasitic capacitances that make up the equivalent capacitor C1. In most cases the bulk will be connected to VSS or VDD which will be AC ground, so in fact these capacitors will all add together.

(2) Output Load capacitor C2 – Figure 3

This capacitor consists of the parasitic capacitors around M2, M4 & M8. ie

C2 = Cgd4+Cdb4+Cgd2+Cdb2+Cgs8+Cgb8+(A2.Cgd8)

Note A2 is the gain of the output stage AVout:–

$$Av_{out} = \frac{-gm_8}{go_7 + go_8}$$

The miller effect multiplies Cgd8 by the gain of the output stage.

(3) Tail capacitor C3 – Figure 3

This capacitor in not critical as it only effects common-mode signals.

(4) Load capacitor CL – Figure 3

CL_{total} = CL+Cdb7+Cgd7+Cdb8

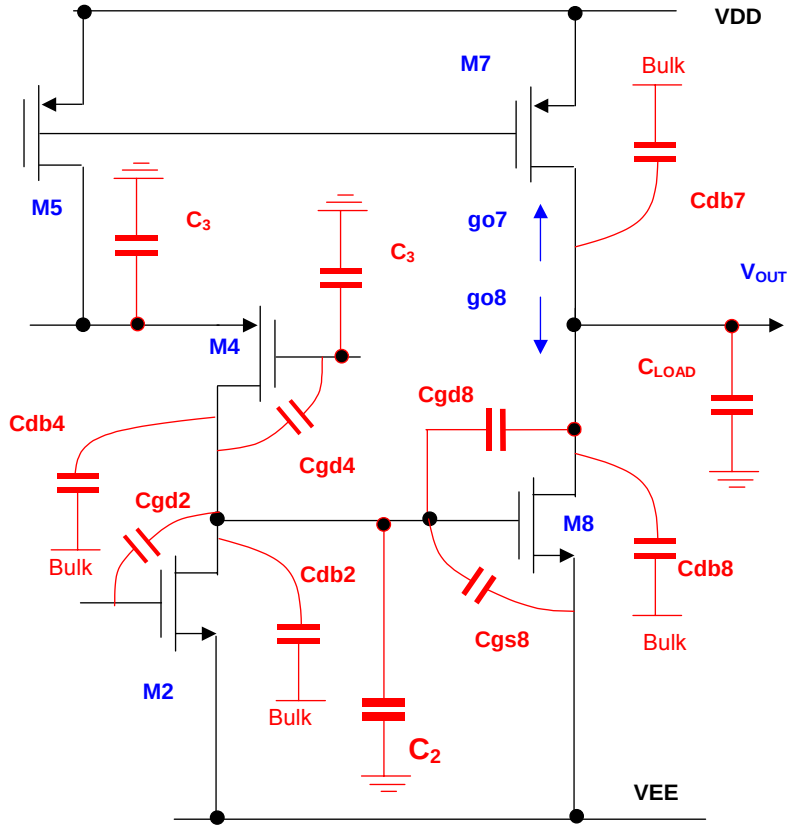

Figure 3 First stage output parasitic capacitances that make up the equivalent capacitor C2. In most cases the bulk will be connected to VSS or VDD, which will be AC ground, so in fact these capacitors will all add together. C3 is the tail parasitic capacitance but has little impact as it only effects common mode signals. The Output capacitance is dominated by Cload, but also has contributions from M7 & M8.

All these parasitic capacitors generate poles in the frequency response of the op-amp especially where the capacitor is connected to a high impedance point of the circuit, generated a large time constant (low frequency pole).

Note In general in CMOS Op-amps most points of the circuit are at low impedance except the output and usually provides the dominant pole.

Simple analysis of figure2 gives rise to the following expressions:

$$\text{Freqpole1 (fp1)} = \frac{1}{2\pi.\text{Ro}_1.\text{C}_2} \quad \text{Where} \quad \text{Ro}_1 = \frac{1}{\text{go}_2 + \text{go}_4}$$

$$\text{Freqpole2 (fp2)} = \frac{1}{2\pi.\text{Ro}_2.\text{C}_{\text{LOAD}}} \quad \text{Where} \quad \text{Ro}_2 = \frac{1}{\text{go}_7 + \text{go}_8}$$

$$\text{First stage gain (A1)} = -\text{G}_{\text{M3}}.\text{Ro}_1$$

$$\text{Second stage gain (A2)} = -\text{G}_{\text{M8}}.\text{Ro}_2$$

$$\text{Total gain} = \text{A1.A2} = \text{G}_{\text{M3}}.\text{G}_{\text{M8}}\text{Ro}_1.\text{Ro}_2$$

$$\text{Gain Bandwidth of first stage (G.B1)} = \text{A1.fp1} = \frac{-\text{G}_{\text{M3}}}{2\pi.\text{C}_2}$$

$$\text{Gain Bandwidth of second stage (G.B2)} = \text{A2.fp2} = \frac{-\text{G}_{\text{M8}}}{2\pi.\text{C}_{\text{LOAD}}}$$

Stability

In order for the op-amp to be stable (assuming it is an inverter) is to have a reasonable phase margin (typically ~ 60 degrees) at the point where the gain response has fallen to 0dB. Addition of pole will degrade this phase margin and if close together in frequency may degrade the phase margin to zero while there is still gain giving rise to instability or oscillation.

Therefore, we try to space the poles out, unfortunately the impedances and parasitic capacitances of the first and second amplifier stages of figure 4 are of a similar order a simulation in ADS (shown in figure) shows that the phase margin is poor as a result (figure 5).

However, we note that capacitor between the gate and drain of the output amplifier is multiplied by the stage gain due to the '**Miller Effect'**. Therefore, if we add another small capacitor (Cc) in parallel with Cgd8 then we will cause the pole formed of C2 (including A2.Cc) to move down infrequency away from the pole caused by C_{LOAD}.

As was states earlier low impedance points have associated high frequency poles that can be generally ignored. As the impedance looking into the diode M1 is low we can **ignore** the effects of the input parasitic capacitance C1.

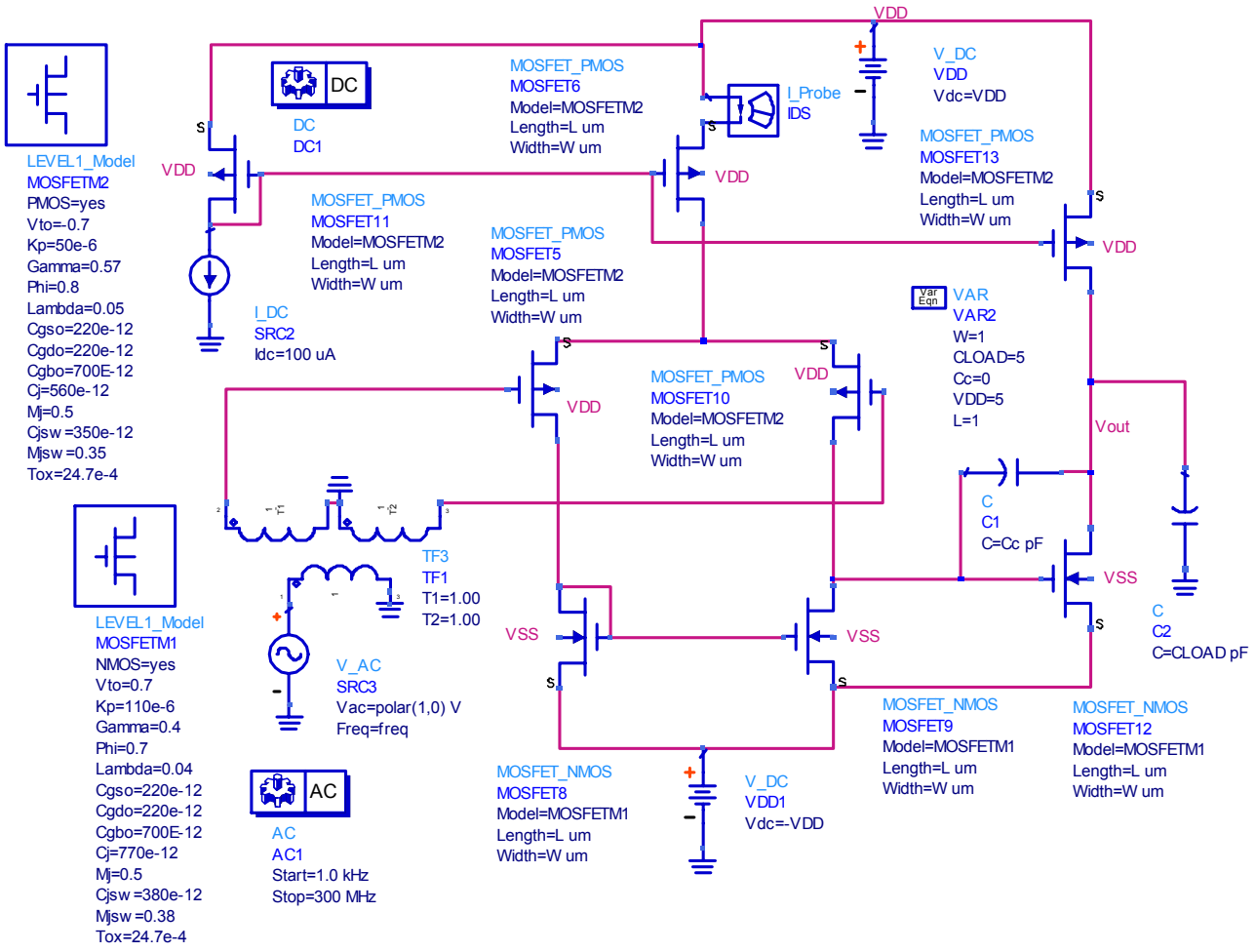

Figure 4 ADS simulation of a two-stage op-amp with no compensation, resulting in poor phase margin as the poles of C1 & C2 (figure1) are of a similar order. The resulting gain and phase plot of this circuit is shown in figure 5.

The Balun on the input generates a differential voltage from the single ac source SRC3. The current source SRC2 sets the bias currents to the two amplifiers and is set to 100uA.

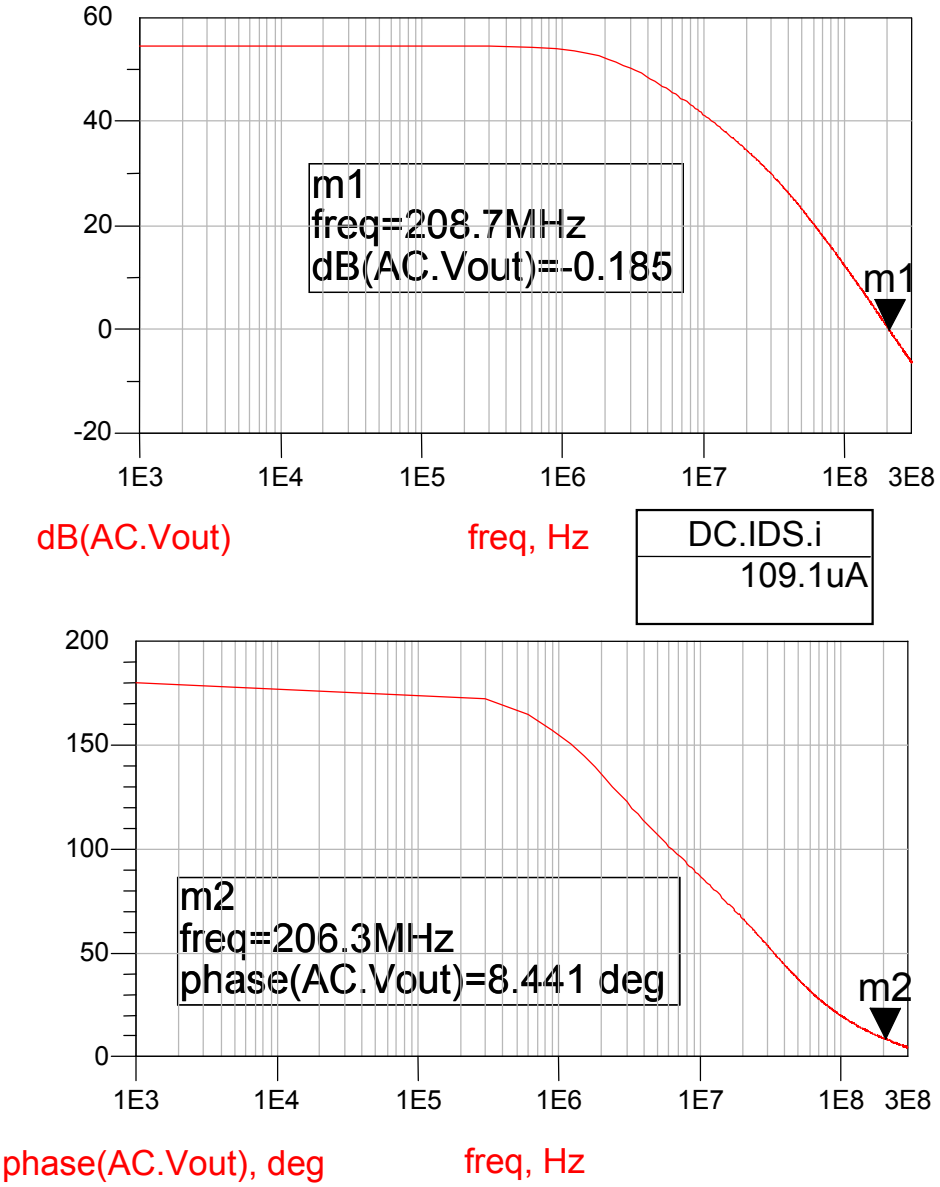

Figure 5 Showing the Gain & Phase response of the two-stage Op-Amp simulated using the ADS schematic of figure 4. In this example there is no frequency compensation and as a result the phase margin is very poor at ~ 8 degrees – a more acceptable phase margin is around 60 degrees.

With the Miller capacitor fitted the equations for the poles 1 & 2 become modified to:-

$$\text{freqpole1(fp1)} = \frac{1}{2\pi.Gm_3.Ro_1.Ro_2.Cc} \quad \text{and}$$

$$\text{freqpole2(fp2)} = \frac{Gm_8}{2\pi.C_{LOAD}}$$

Phase Margin

The expression for phase margin is given below (Where pole1 is known as the Miller pole). The zero term will be discussed later but we assume that this is either cancelled out or is pushed far up in frequency eg zero1 = 10 x GB to gives GB/zero1 = 0.1 (arctan(0.1) = 5.7 degrees.)

$$\text{PhaseMargin}\Phi_M = \pm 180^\circ - \tan^{-1}\left(\frac{2\pi.f}{|\text{freqpole1}|}\right) - \tan^{-1}\left(\frac{2\pi.f}{|\text{freqpole2}|}\right) - \tan^{-1}\left(\frac{2\pi.f}{|\text{freqzero1}|}\right)$$

$$\text{Assume desired phase margin} \sim 60 \text{ degrees} \therefore \ 180 - 60 = 120 \text{ degrees. Also assume that } 2\pi.f \text{ (unity - gain frequency)} = \text{G.B (Gain bandwidth product)-}$$

$$120 = \tan^{-1}\left(\frac{\text{G.B}}{|\text{freqpole1}|}\right) + \tan^{-1}\left(\frac{\text{G.B}}{|\text{freqpole2}|}\right) + \tan^{-1}\left(\frac{\text{G.B}}{|\text{freqzero1}|}\right)$$

$$\text{freqpole1} = \frac{1}{2\pi.Gm_8.Ro_1.Ro_2.Cc} \quad \text{and} \quad \text{G.B} = \frac{Gm_3}{2\pi.Cc} \ \therefore$$

$$\tan^{-1}\left(\frac{\text{G.B}}{|\text{freqpole1}|}\right) = \tan^{-1}\left(\frac{\frac{Gm_3}{2\pi.Cc}}{\left|\frac{1}{2\pi.Gm_8.Ro_1.Ro_2.Cc}\right|}\right)$$

$$= \tan^{-1}\left(\frac{Gm_3.2\pi.Gm_8.Ro_1.Ro_2.Cc}{2\pi.Cc}\right) = \tan^{-1}(Gm_3.Gm_8.Ro_1.Ro_2)$$

$$\text{As } Gm_3.Gm_8.Ro_1.Ro_2 = A_V \text{ is very large then } \tan^{-1}(Gm_3.Gm_8.Ro_1.Ro_2) = 90 \text{degrees}$$

$$120 = 90 + \tan^{-1}\left(\frac{\text{G.B}}{|\text{freqpole2}|}\right) + 5.7 \quad \Rightarrow \quad 24.3^\circ = \tan^{-1}\left(\frac{\text{G.B}}{|\text{freqpole2}|}\right) \text{ Rearranging gives}$$

$$|\text{pole2}| > 2.2\text{G.B}$$

The previous equations give rise to the following relationships that are used at the beginning of the op-amp design process:-

$$\frac{Gm_8}{2\pi.Cc} > 10\left(\frac{Gm_3}{2\pi.Cc}\right) \quad \therefore Gm_8 > 10.Gm_3$$

$$\frac{Gm_8}{2\pi.Cc} > 2.2\left(\frac{Gm_3}{2\pi.Cc}\right) \quad \therefore Cc > \frac{2.2(C_2)}{10} \quad Cc = 0.22C_2$$

Summary

The input features of the op-amp are based on the differential amplifier with high impedance inputs. The output stage has a low impedance output and the total gain of the op-amp is the product of the two individual stage gains.

As the output impedances of each stage are similar (ie RO1 ~ RO2) then without compensation the frequency poles caused by the interaction of C1.RO1 and C2.RO2 are at similar frequencies resulting in poor phase margin.

To split the poles (ie move them further apart) we introduce the miller capacitor (Cc) to ensure a lower frequency dominant pole (Miller pole) formed by Cc.RO1.RO2.

The addition of the miller compensation capacitor Cc introduces a high frequency zero (More on this in another tutorial) that will degrade the phase margin and peak up the gain so efforts have to be made to increase the frequency of the zero or eliminate it all together.

Finally, we ideally require the following relationships in the op-amp design

The tail current I5 determines the slew rate ie

$I5 = S.R.Cc$ Where Cc is the Miller capacitor

There, are however constaints on Cc : -

$$Cc > 0.22.C2 \text{ and } Cc <= \frac{GM3}{2\pi.G.B}$$

$$\text{freqpole2} >> 2.2G.B \quad \text{ie} \quad \frac{GM3}{2\pi.C_{LOAD}} >> 2.2G.B$$

As these relationships are inter-dependant then the design of the op-amp will require trade-offs with the designer deciding what parameters are key for the application.

Other related tutorials will discuss a simple un-buffered OP-Amp design and the effect of the Miller zero and how to minimise it.