Basic Two-stage unbuffered Op-Amp Example

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1 ABSTRACT

This paper uses theory discussed in the op-amp tutorial to provide a step-by-step design of a practical op-amp using the CN20 process. ADS simulations and results have been given to verify the hand calculations during the design process.

2 INTRODUCTION

This tutorial describes the step-by-step process in designing an op-amp to meet specific goals including gain, gain bandwidth, phase margin, CMRR and voltage swing.

From the OP-Amp design tutorial we described the main equations required in order to define bias currents, W/L ratios and op-amp topography.

The equations given refer to the circuit elements of the op-amp shown in **Figure 1**.

3 DESIGN EQUATIONS

(1) Slew Rate (setting of I5)

$I_5 = S.R.Cc$ (typical slew rates are 10V/us).

$I_5 = 10(\text{Settling time}).Cc$

The tail current I5 determines the slew rate ie

$I5 = S.R.Cc$ Where Cc is the Miller capacitor

There, are however constaints on Cc : -

$Cc > 0.22.CLoad$ and $Cc <= \frac{GM2}{2\pi.G.B}$

$freqpole2 >> 2.2G.B$ ie $\frac{GM2}{2\pi.C_{LOAD}} >> 2.2G.B$

Alternatively I5 is given by:

$I5 \approx 10\left(\frac{V_{DD} + |V_{SS}|}{2.Ts}\right)$ Where Ts = settling time (s)

(2) Gain & Gain Bandwidth

The gain bandwidth is a function of the differential amplifier stage gm and the miller compensation capacitor Cc. ie

$G.B = \frac{gm_2}{Cc}$ (typically gain bandwidths are 5MHz).

Also $gm_6 > 10.gm_1$

(3) First Stage Gain

The gain of the differential amplifier, is given by the product of gm3 and the load conductance

$AV_{diff} = \frac{-gm_2}{go_2 + go_4}$ as $go = gds = I_d.\lambda$

$AV_{diff} = \frac{-gm_2}{\frac{I_5}{2}(\lambda_2 + \lambda_4)} = \frac{-2gm_2}{I_5(\lambda_2 + \lambda_4)}$ as $go = I_d.\lambda$

(4) Second Stage Gain

The gain of the current source inverting amplifier, is given by the product of gm6 and the load conductance ie

$AV_{O/P} = \frac{-gm_6}{go_7 + go_6}$ as $go = gds = I_d.\lambda$

$AV_{O/P} = \frac{-gm_6}{I_6(\lambda_7 + \lambda_6)}$ = as $go = I_d.\lambda$

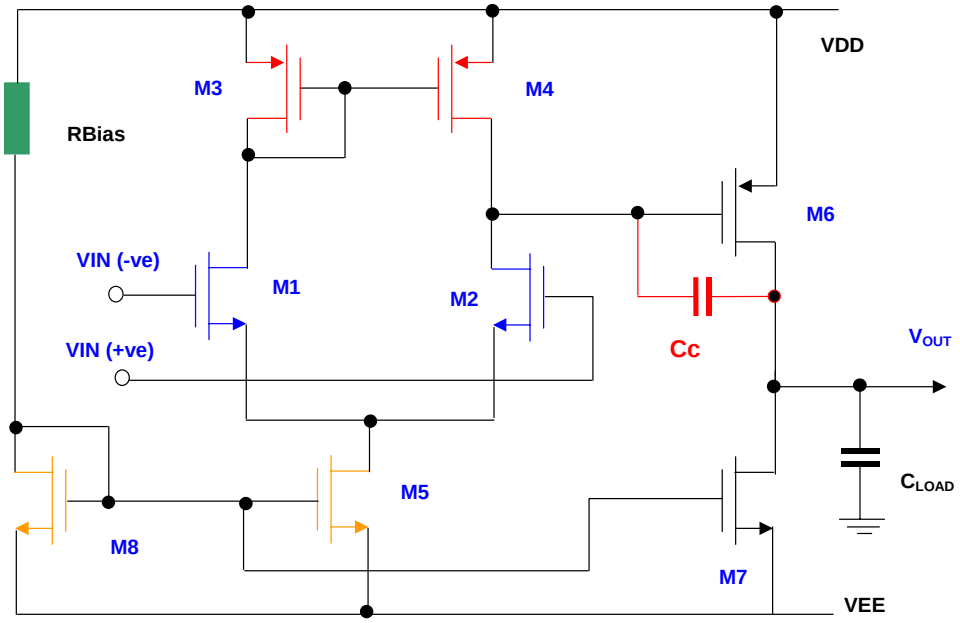


Figure 1 Simple Compensated OP-Amp circuit with capacitive load, using N-type differential amplifier input stage. Note that many of the devices are paired with the same W/L ratio's as shown by the colours (ie M8 = M5, M1 = M2 and M3 = M4).

(5) Positive CMR V_{IN} MAX

This is the maximum output from the differential amplifier and is given by:-

$$V_{IC(MAX)} = V_{DD} - V_{GS3} + V_{T1}$$

$$\text{Where } V_{GS3} = \sqrt{\frac{I_5}{\beta_3}} + V_{T3}$$

$$= V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T3}| + V_{T1}$$

(6) Negative CMR V_{IN} (MIN)

This is the minimum output from the differential amplifier and is given by:

$$V_{IC(MIN)} = V_{SS} + V_{GS1} + V_{DS5} \quad \text{With Q5 in saturation} \quad V_{DS5} = \sqrt{\frac{2I_5}{\beta_5}}$$

$$V_{GS1} = \sqrt{\frac{I_5}{\beta_1}} + V_{T1} \quad \text{Where } \beta = K\frac{W}{L}$$

$$\therefore V_{IC(MIN)} = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1} + \sqrt{\frac{2I_5}{\beta_5}}$$

4 SPECIFICATION

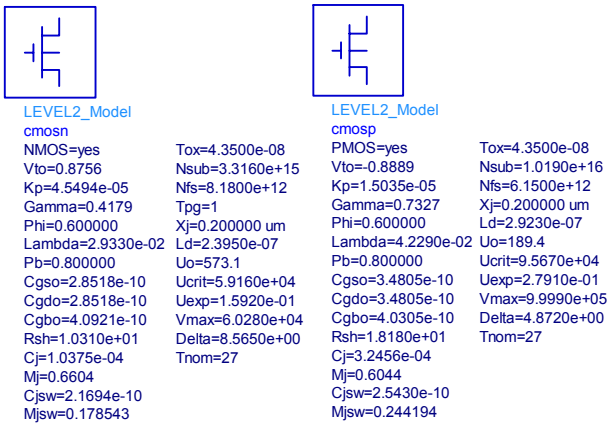
The specification of the op-amp to design is given in **Table 1** below:

Parameter	Target value	Units
Voltage Gain (Av)	>=60	dB
Supply Voltage	± 5	V
Gain Bandwidth (GB)	1	MHz
Slew Rate	> 5	V/us
Gate Length	1	um
CMVR	+4, -3	V
Output swing (unbuffered)	± 4	V
Power consumption	<5	mW
Output Load Capacitance	15	pF

Table 1 Op-Amp example specification table

5 SPICE MODELS

CN20 Process Level 2 spice Models



Spice models used (Orbit CN20)

6 INITIAL DESIGN

We can design the op-amp in stages by considering the first stage differential amplifier. We need to define the tail current (to define M5), the gain bandwidth (to define M1 & M3) and finally the maximum CMRR (to define M3 & M4).

The slew rate allows us to determine the tail current I5 and hence the gate dimensions of this device.

$Cc > 0.22.CLoad$

$Cload <= 15pF$ which makes $Cc = 0.22 * 15 = 3.3pF$,

let this be 4pF

The tail current I5 determines the slew rate ie

$I5 = S.R.Cc$ Where Cc is the Miller capacitor and $= 4pF$

$I5 = 5x10^{6} * 4x10^{-12} = 20uA$

We can now define the W and L dimensions of M5 and M8.

(2) Gain bandwidth product (GB)

To be safe set GB from 1MHz to 2MHz

$Cc <= \frac{G_{M1}}{2\pi.G.B}$ Rearrange to give GM1 ie

$G_{M1} = 2\pi.G.B.Cc = 2\pi.2E^{6}.4E^{-12} = 50uAV^{-2}$

Now find $\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{(G_{M2})^2}{K_N.I_5} =$

$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{(50E^{-6})^2}{4.5494E^{-5} x\ 20E^{-6}} = 2.7$

Initially set $\frac{W_1}{L_1} = \frac{W_2}{L_2}$ to 3

$Vgs_1 = \sqrt{\frac{2.I_1}{\beta_1}} + V_{T1}$ but $I_1 = \frac{I_5}{2}$

$\therefore Vgs_1 = \sqrt{\frac{I_5}{\beta_1}} + V_{T1} = \sqrt{\frac{20E^{-6}}{50E^{-6}}} + 0.8756 = 1.5V$

3) CMV

As we have a 5V rail and want CMV to be >3 then we can allow 2V drop across the differential amplifiers and their bias FET's ie

CMV(MAX) – to find M3/M4 details:

$$V_{IC(MAX)} = V_{DD} - V_{GS3} - V_{DS1} + V_{gs1}$$

$$-V_{DS1} + V_{gs1} = V_{T1} \quad \therefore$$

$$V_{IC(MAX)} = V_{DD} - V_{GS3} + V_{T1} \quad \text{so}$$

$$V_{GS3} = V_{T3} + \sqrt{\frac{2.I_3}{\beta_3}}$$

$$V_{T1} - V_{GS3} <= 2V \quad \therefore \quad V_{T1} - V_{T3} + \sqrt{\frac{2.I_3}{\beta_3}} <= 2V$$

Rearrange to get β_3

Where $I_3 = \frac{I_5}{2}$

$$\beta_3 = \frac{I_5}{.[(V_{DD} - V_{IC(MAX)}) - V_{T1} + |V_{T3}|]^2}$$

$$= \frac{20E^{-6}}{[(5-4) - |0.8889| + 0.8756]^2} = 20.5uAV^{-2}$$

$$\frac{W_3}{L_3} = \frac{\beta_3}{K_P} = \frac{20.5E^{-6}}{1.5035E^{-5}} = 1.33 \quad \therefore \text{ Set } \frac{W_3}{L_3} = \frac{W_4}{L_4} = 1$$

(4) CMV(MIN) – to find M5/M8 details:

$$V_{IC(MIN)} = V_{SS} + V_{GS1} + V_{DS5}$$

$$V_{GS1} = 1.5V$$

With Q5 in saturation $V_{DS5} = \sqrt{\frac{2I_5}{\beta_5}}$ Rearrange to get β_5

$$ie \quad 4 = 5 - 1.5 - \sqrt{\frac{2I_5}{\beta_5}} \quad \Rightarrow$$

$$\frac{2.20E^{-6}}{[-3-(-5)-1.5]^2} = \beta_5 = 160uAV^{-2}$$

$$\frac{W_5}{L_5} = \frac{\beta_5}{K_N} = \frac{160E^{-6}}{4.5494E^{-5}} = 3.5$$

This completes the design of the first differential amplifier stage. The estimated gain of this stage will be:

$$A_1 = \frac{2.G_{M2}}{I_5(\lambda_4 + \lambda_2)} = \frac{2.\ 50E^{-6}}{20E^{-6}(2.933E^{-2} + 4.229E^{-2})} = 69$$

In dB = 20log(69) = 37dB

The simulation using a transient analysis (Pspice) within ADS is shown in **Figure 2**. This simulation uses Level 1 Spice models for the CN20 MOSFETS. This is the simplest spice model and is used to check the hand calculations. The data required is Vto (Threshold voltage), Kappa (Transconductance parameter), Gamma (Bulk threshold parameter), Lambda (Channel length modulation parameter) and Phi (Surface potential at strong invertion).

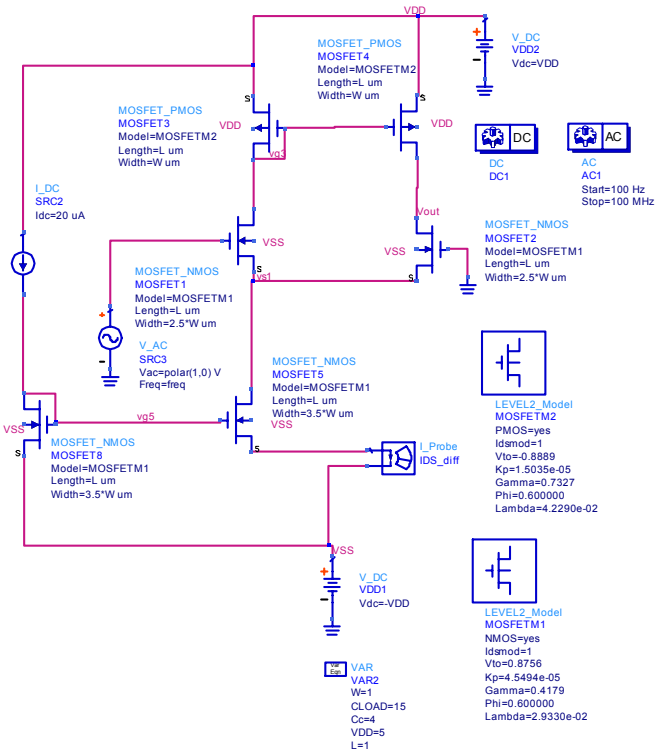


Figure 2 ADS Simulation setup for Input differential amplifier stage using level 1 Spice models.

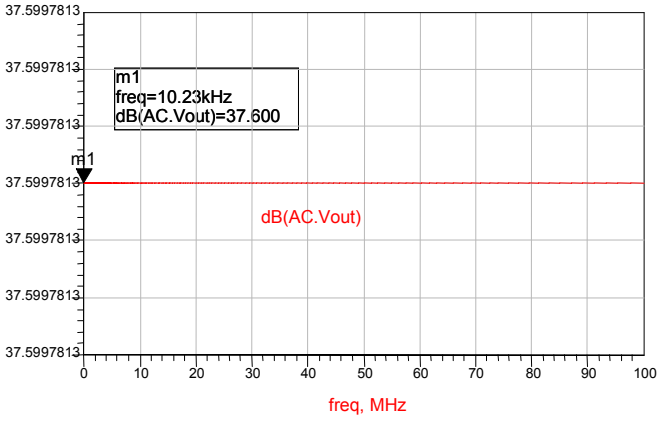


Figure 3 ADS simulation result showing a voltage gain of ~ 37dB as predicted using hand calculations.

(5) Find I_6 and W/L_6

There are two expressions for M6:

$$G_{M6} = 2.2.G_{M2}\frac{C_{Load}}{Cc} \quad \text{and} \quad G_{M6} \geq 10.G_{M2} \quad \text{These give}$$

$$G_{M6} = 2.2 * 50E^{-6}\frac{15E^{-12}}{4E^{-12}} = 412uAV^{-2}$$

$$\text{and } G_{M6} \geq 10.50E^{-6} = 500uAV^{-2}$$

Lets go for the higher GM of $500uAV^{-2}$

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{\frac{W_6}{L_6}}{\frac{G_{M6}}{G_{M4}}} \quad \text{Rearrange to get } \frac{W_6}{L_6} \text{ ie } = \frac{W_4}{L_4}\frac{G_{M6}}{G_{M4}}$$

$$\frac{W_6}{L_6} = 1.\frac{500E^{-6}}{20.5E^{-6}} = 24$$

$$G_{M6} = \sqrt{\frac{2.K_P.W_6.I_6}{L_6}} \quad \text{Rearrange to get } I_6 \Rightarrow$$

$$I_6 = \frac{G_{M6}^{\ 2}}{2K_P\frac{W_6}{L_6}} = \frac{\left(500E^{-6}\right)^2}{2.\ 1.5035E^{-5}(24)} = 346uA$$

(7) W/L_7

$$\frac{W_7}{L_7} = \frac{I_6}{I_5}.\frac{W_5}{L_5}$$

$$\frac{W_7}{L_7} = \frac{I_6}{I_5}.\frac{W_5}{L_5} = \frac{346E^{-6}}{20.5E^{-6}}.3.5 = 60$$

(8) Gain check (two-stages)

$$A_1 = \frac{2.G_{M2}}{I_5(\lambda_4 + \lambda_2)} = \frac{2.\ 50E^{-6}}{20E^{-6}\left(2.933E^{-2} + 4.229E^{-2}\right)} = 68$$

$$A_2 = \frac{G_{M6}}{I_6(\lambda_7 + \lambda_6)} = \frac{500E^{-6}}{346E^{-6}\left(2.933E^{-2} + 4.229E^{-2}\right)} = 20$$

$$A1.A2 = 20\log(68 * 20) = 62dB$$

We can now analyse the whole circuit using the AC ADS analysis shown in.

NOTE For this simulation the model for the FET's has been set at level 1 which uses similar formulae found in the hand calculations. To get a more repre-

sentative simulation the levels have to be set to level 2.

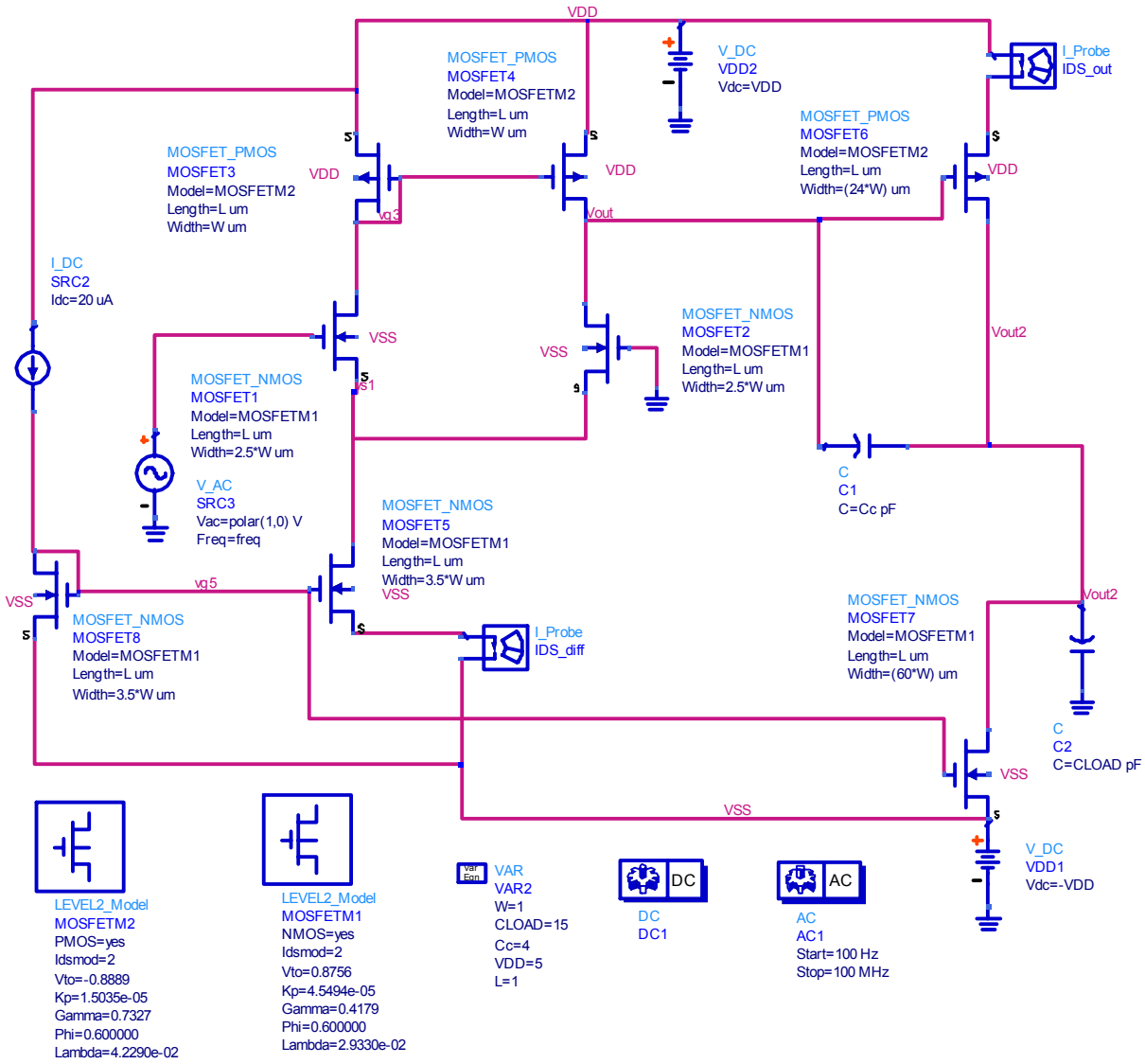


Figure 4 Two-stage op-amp using level 1 mosfet data for the Orbit CN20 process. The Op-amp is configured in open loop by ground the non-inverting input and applying an ac source to the inverting input.

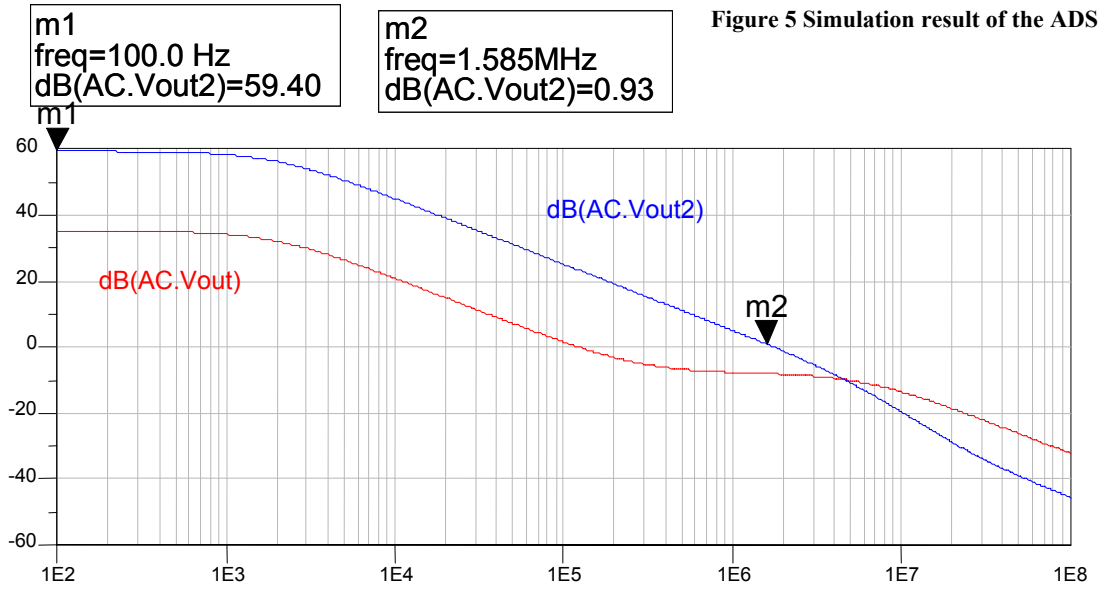


Figure 5 Simulation result of the ADS setup of

Eqn vgs1=0-DC.vs1

Eqn vgs3=DC.VDD-DC.vg3

Eqn Vsat4=DC.VDD-DC.Vout

Eqn Vds1=vgs3-DC.vs1

...S_diff.i	...S_out.i
21.16uA	348.6uA

vgs1	vgs3	Vsat4	Vds1
1.790	2.220	2.220	4.010

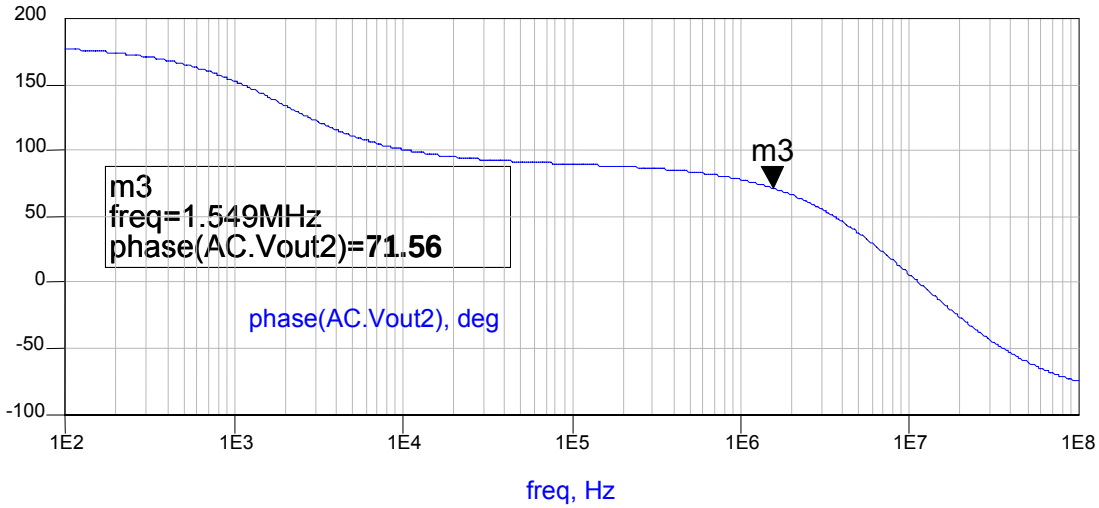


Figure 4. A number of parameters need some optimization ie gain (we require >60dB simulation predicts 59dB) slightly more gain bandwidth (Although our specification is 1MHz we decided on a GB of 2MHz, so we can trade GB for a slightly degraded phase margin that currently stands at 71 degrees).

7 DESIGN OPTIMISATION

The design doesn't quite meet the gain and gain bandwidth specification. However we can trade off the excess phase margin of this design. The following table ( ) gives an indication on what parameters effect key design drivers.

Parameter	Slew rate	Gain	Phase Margin	Gain Bandwidth
Increase I5	↑	↓	↓	↑
Increase Cc	↓	-	↑	↓
Increase $W/L)_1$	-	↑	↓	↓
Increase Rz	-	-	↑	-

Table 2 Design drivers for key op-amp performance parameters.

We can degrade the phase margin by reducing Cc from 4pF to 3.5pF. This should increase the gain bandwidth and also increase the slew rate. Increasing W/L1 & 2 (from 2.5 to 4) will increase the gain and gain bandwidth again at the expense of phase margin.

Simulation using the new circuit values results in the new gain and phase response of **Figure 6** & **Figure 7**.

We can see that the gain is now >60dB (61.5dB) the gain bandwidth is now >2MHz with the phase margin reducing to 62 degrees.

The op-amp design now meets the given specification.

Figure 9 uses a transient simulation to allow the pulse rise time to be measured.

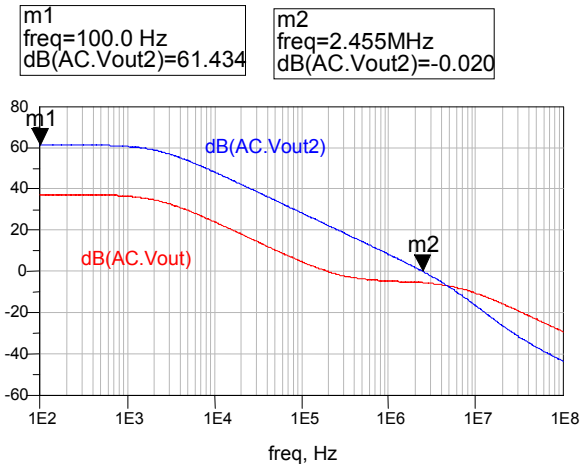


Figure 6 Optimised Op-Amp gain response showing gain and gain bandwidth (markers 1 & 2 respectively).

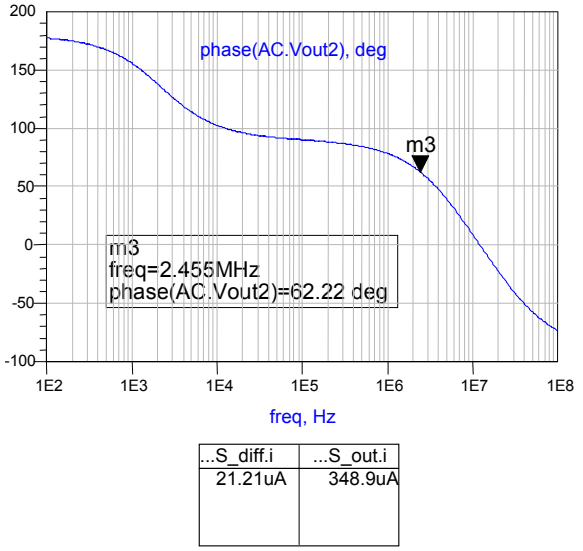


Figure 7 Optimised Op-Amp phase response showing the phase margin to be 62 degrees (Marker3). The tail current (21.2uA) and output stage current (349uA) are also shown.

8 SIMULATIONS

This section will check the basic design against the specification. We have verified open loop gain and phase margin and now we will take a look at the slew rate. The ADS simulation of

(1) Slew rate

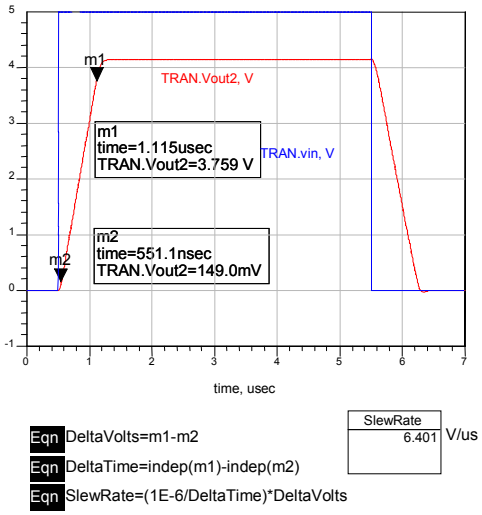


Figure 8 Slew rate simulation result

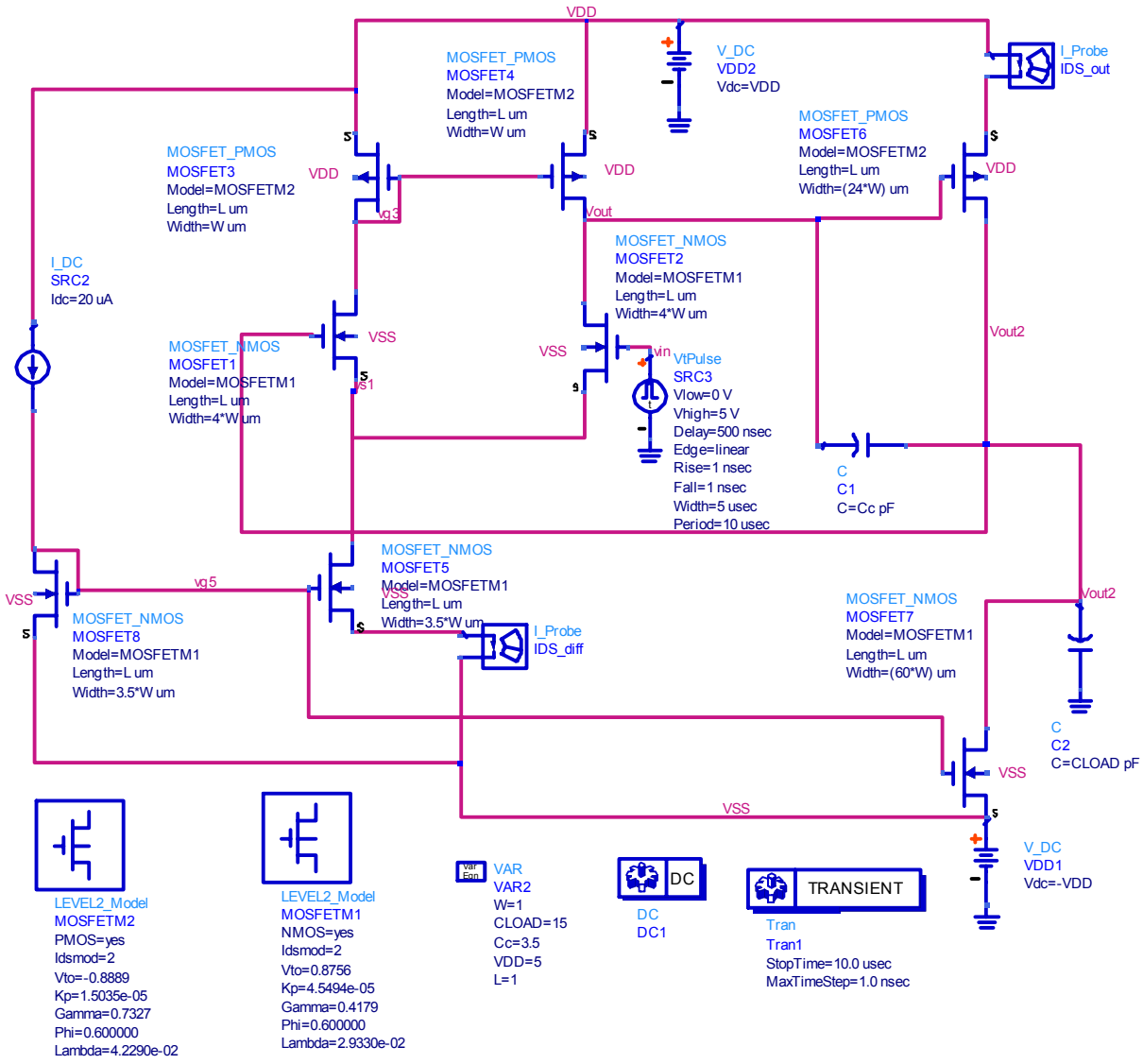


Figure 9 ADS simulation to predict the op-amp slew-rate. The Op-Amp is configured as a unity gain buffer amplifier with a pulsed input of magnitude +5V. The simulation result is shown in Figure 8. Here we have added two markers m1 & m2, we first calculate the voltage difference between them, then the time difference between them (by using the indep function). We divide 1uS by the deltaTime and multiply by the DeltaVolts to get slew rate, which easily meets our specification of 5V/us with some margin at ~6V/uS.

We can use the same ADS simulation of **Figure 9** to predict the output voltage swing by setting the pulse to be ± 5V. This results in the plot of **Figure 10**.

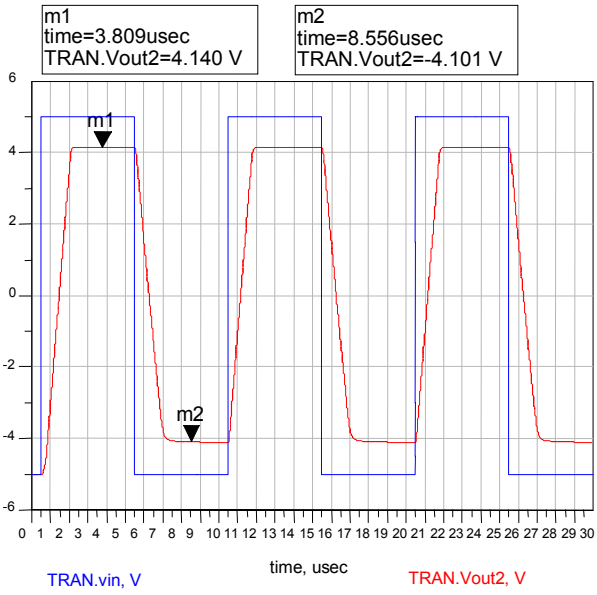


Figure 10 Maximum and minimum output voltage swing prediction.

(2) Power consumption

Total supply voltage = + 5V - (-5) = 10V
Current from mirror = 21uA
Current I5 (Tail current) = 21uA
Current through output stage = 346uA

Total current = 388uA
Total power consumption = $10 * 388E^{-6}$ = 3.88mW

Now all the parameters have been simulated we can produce a table with our performance predictions as shown in **Table 3**.

Finally the CMVR voltage inputs have simulated by adding an AC voltage source to each input. The simulation resulted in the plot shown in **Figure 11**.

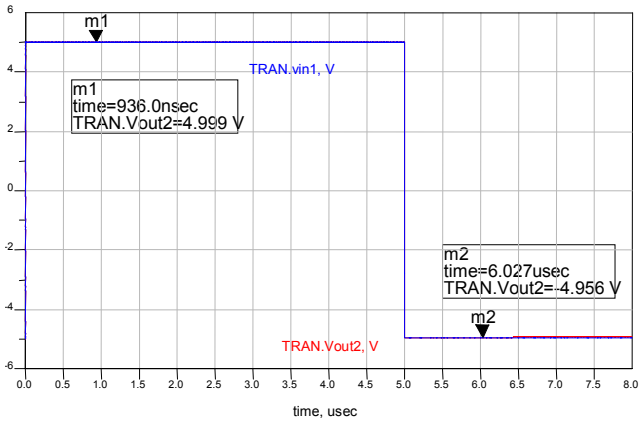


Figure 11 Simulation result of CMVR

Parameter	Predicted value	Units
Voltage Gain (Av)	>=61	dB
Supply Voltage	± 5	V
Gain Bandwidth (GB)	2	MHz
Slew Rate	> 6	V/us
Gate Length	1	um
CMVR	± 4.9	V
Output swing (unbuffered)	± 4.1	V
Power consumption	3.8	mW
Output Load Capacitance	15	pF

Table 3 Op-Amp example predicted performance table.

9 CONCLUSION

This tutorial has described the step-by-step design of a simple two-stage un-buffered op-amp designed to have a phase margin of at least 60 degrees, with >60dB of gain and a gain bandwidth of >1MHz.

Future tutorials will discuss:

(1) The driving of resistive loads with buffered op-amps.
(2) The increase of gain using cascode and folded cascode op-amp topographies.
(3) The increase of bandwidth and the degradation of phase margin and how to improve this (by eliminating the zero).