

Lab 7: Opamp Circuit

Objectives:

- To layout and simulate an opamp circuit with compensating capacitor and with both positive and negative power rails.

Figure 1 shows the opamp circuit, whose layout is to be created. This circuit power rails requirement are $V_{DD}=5V$, $V_{SS}=-5V$, and intermediate reference $GND=0V$. It also includes a $1pF$ compensating capacitor C_c . In addition, it includes a $17.5k$ biasing resistor R_b , which is not part of the layout. This resistor is external to the IC chip, which needs to be adjusted to achieve the desired biasing current.

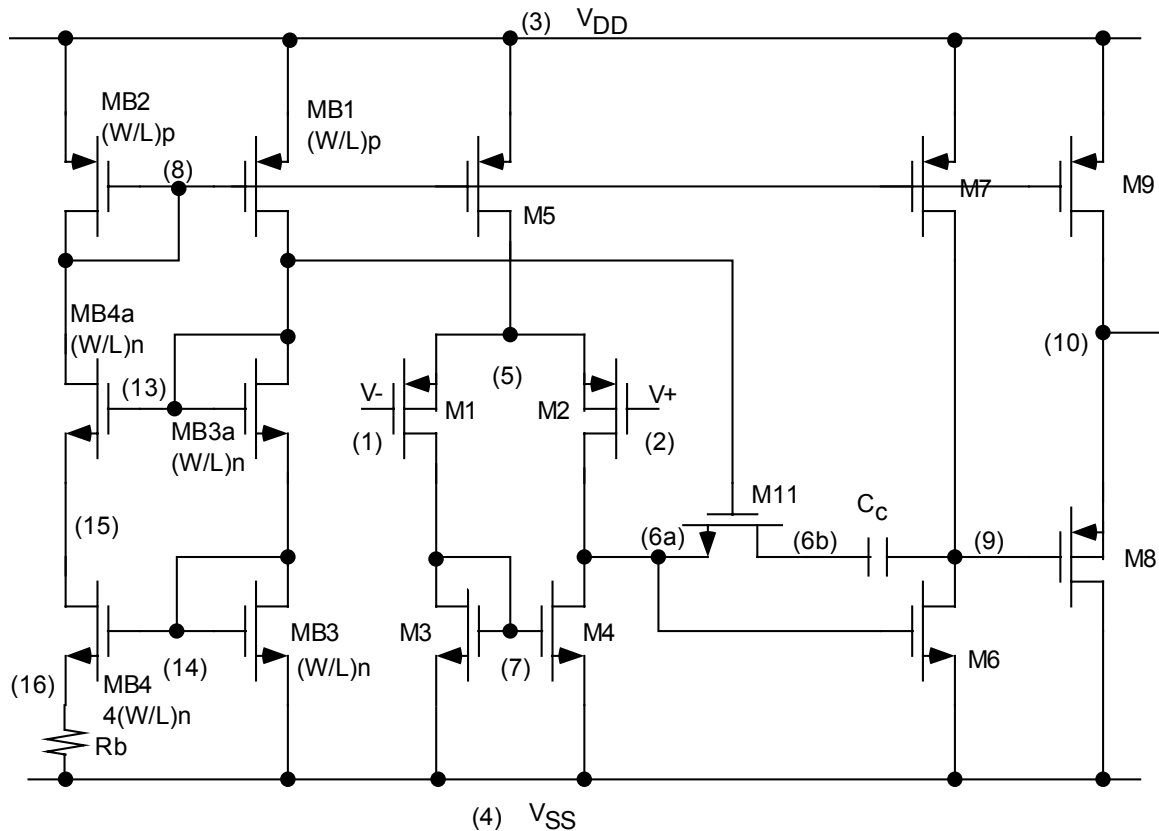


Figure 1: Opamp Design with Process and Temperature Independent Implementation

Transistor	Type	W	L
M1	P	146.4U	6.6U
M2	P	146.4U	6.6U
M3	N	5.4U	6.6U
M4	N	5.4U	6.6U
M5	P	30U	6.6U
M6	N	24U	6.6U
M7	P	90U	6.6U
M8*	P	873.6U	6.6U
M9*	P	300U	6.6U
M11	N	20.4U	6.6U
MB1	P	30U	6.6U
MB2	P	30U	6.6U
MB3a	N	10.8U	6.6U
MB3	N	10.8U	6.6U
MB4a	N	10.8U	6.6U
MB4	N	43.2U	6.6U

$C_c = 1\text{pF}$, $R_b = 17.5\text{k}$

* Too big to be modified later.

The general procedure is explained from labs 1 to 5, according to which the first step is to capture design in VSE (Virtuoso Schematic Editor). As learned in the oscillator project design, Cadence does not provide direct layout of capacitor, so we will treat capacitor as a different design and draw the schematic and generate a symbol of it as what was done in oscillator. Briefly, the steps followed in completing this design are as follows:

- Capture the schematic of a capacitor in VSE
- Generate a symbol for the capacitor in VSE.
- Capture the opamp design in VSE without capacitor and resistor (see instructions and figure for details).
- Generate a symbol for the opamp in VSE.

Note: the final opamp design schematic will differ from the one shown in figure 1, for more details refer the instructions and explanations.

Once we have both the symbols of the capacitor and the opamp without capacitor, we are all set to capture the final opamp design with the capacitor and the resistor.

- Capture the final opamp design in VSE.
- Generate a symbol for the final opamp in VSE.
- Capture a testbench.
- Do the pre-layout simulation in AFFIRMA.

If we get the desired output then we go ahead with the layout process of the design.

- Create the layout for the capacitor.
- Create the layout for the opamp without capacitor.
- Do the post-layout simulation in AFFIRMA

I. Create the Capacitor Schematic and symbol

Recall the steps followed in earlier project/exercises to create capacitor schematic and symbol.

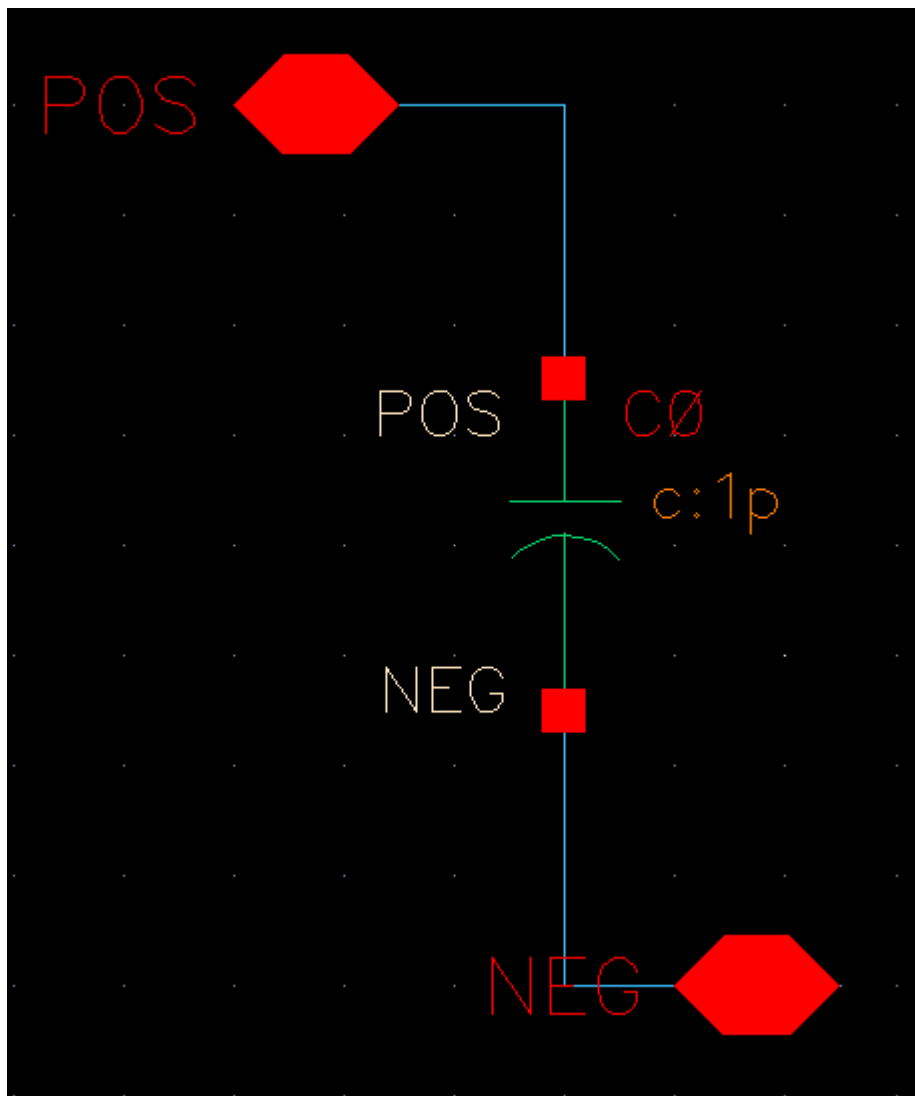


Figure 2. cap1p schematic diagram

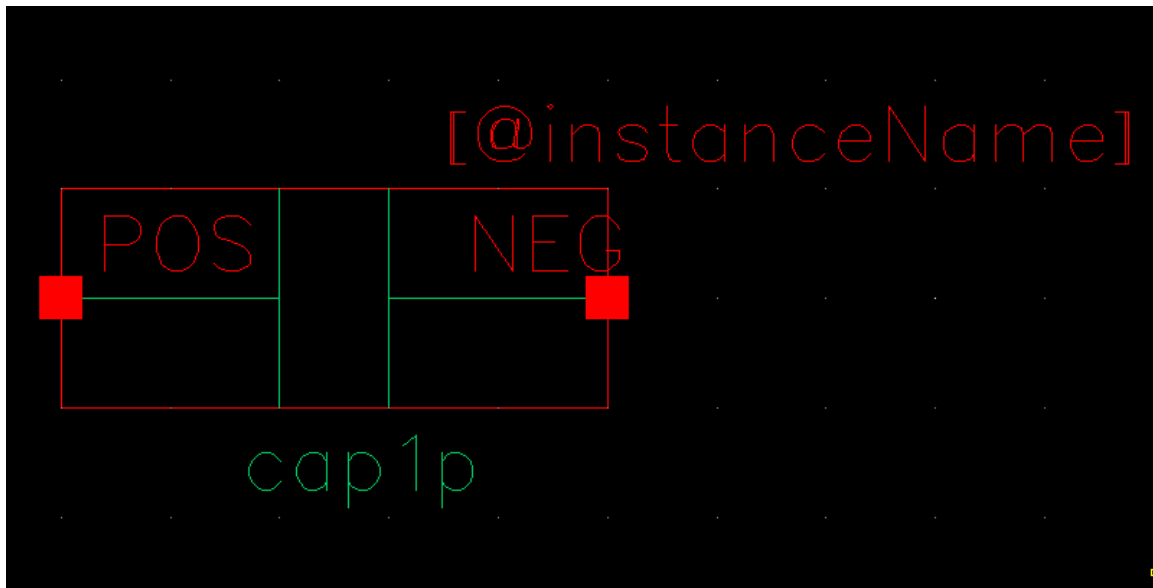


Figure 3: Capacitor Symbol

Notice, this shown capacitor symbol is a modified version of the one created by “Create Cellview”. However, it is not necessary to change the original box-like symbol, in terms of the correctness.

II. Modify Opamp Schematic for MOSIS process

Now we need to capture the opamp design without the capacitor and the resistor. The modification required to satisfy the MOSIS process is described as following:

In the original design, the bulk of PMOS M1, M2 and M8 are connected to the source of themselves to avoid the body effect and obtain higher and environmental independent output gain. However, in MOSIS’s design process, it is not allowed to connect the bulk of PMOS to places other than VDD. (Similar situation for NMOS connecting to GND) Therefore, the solution is to sacrifice the good property and connect M1, M2 and M8's bulk to VDD.

To satisfy MOSIS constraints, modify the schematic in Figure 1 to include transistors only and their default bulk connection. In addition, ports must be provided for connecting the capacitor and resistor. To provide a negative power rail, VSS is used instead of GND as the lowest power rail. GND is used to provide as intermediate reference.

Three additional pins for connecting external capacitor and resistor are added at appropriate places.

Figure 4 illustrates the modified opamp circuit. Name your component as “opamp”. Once you have completed the schematic, check and save the schematic. Then generate the symbol with name of “opamp”.

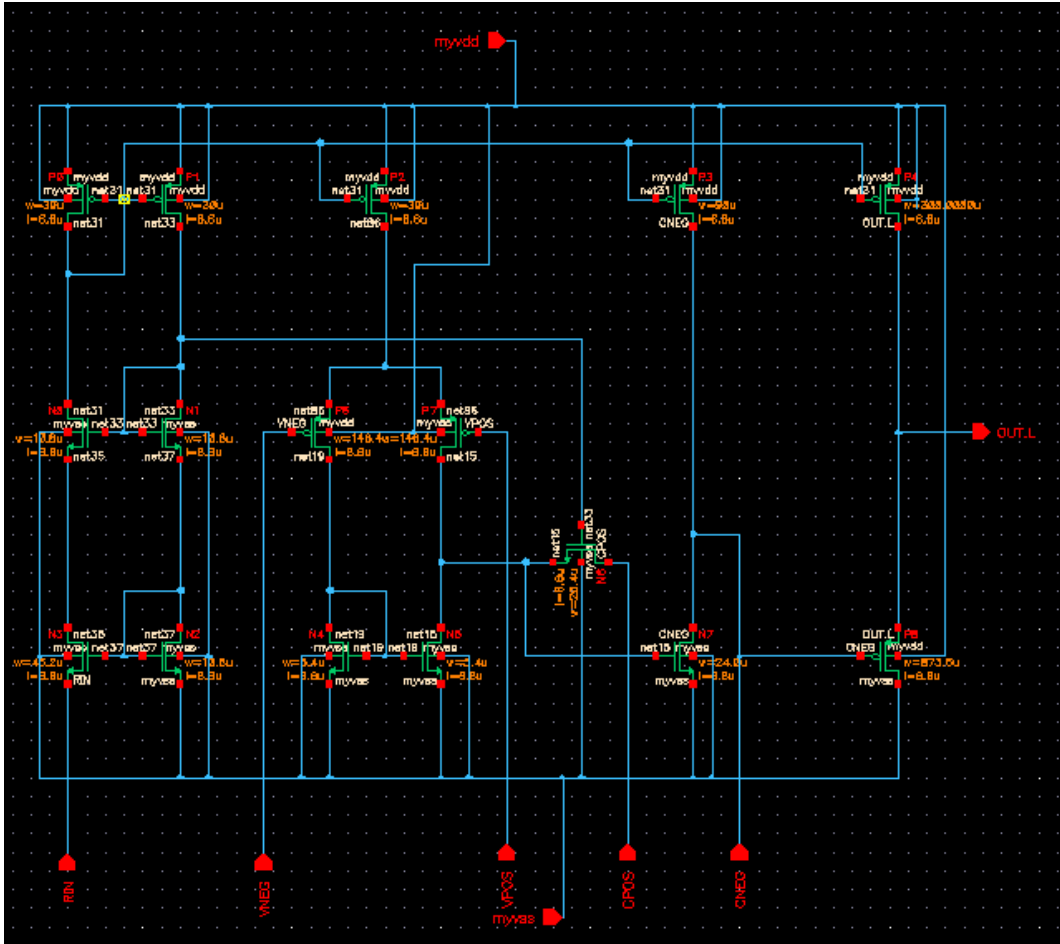


Figure 4. Modified Opamp Circuit for MOSIS

Now generate a symbol for the above design the symbol is shown below.

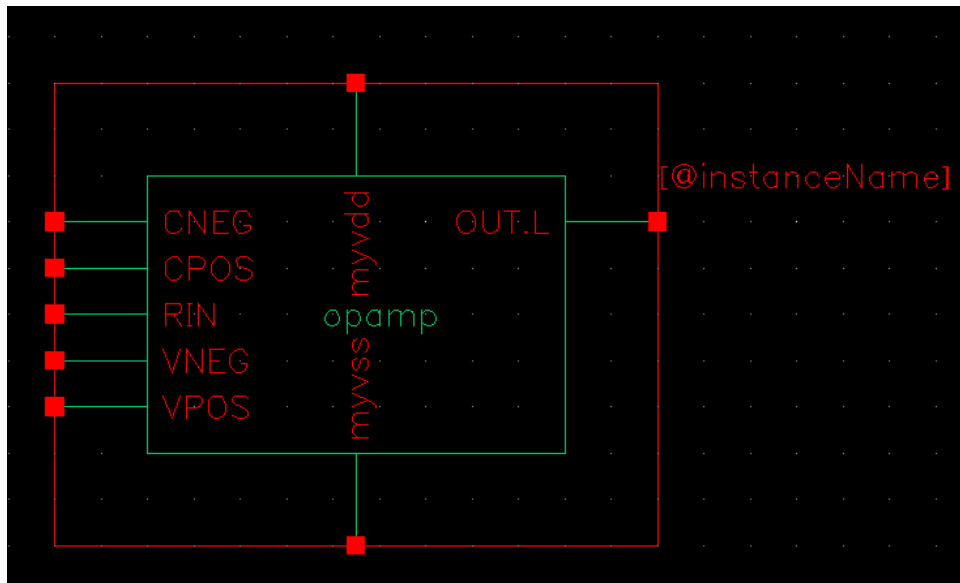


Figure 5: Opamp Symbol

III. Creating the Complete Opamp Circuit

The symbol of opamp in Figure 5, the created capacitor symbol in figure 3, and the symbol of resistor from the NCSU Library are combined to complete the opamp circuit. Figure 4 shows the complete opamp circuit. Name the schematic “opamp_wc”.

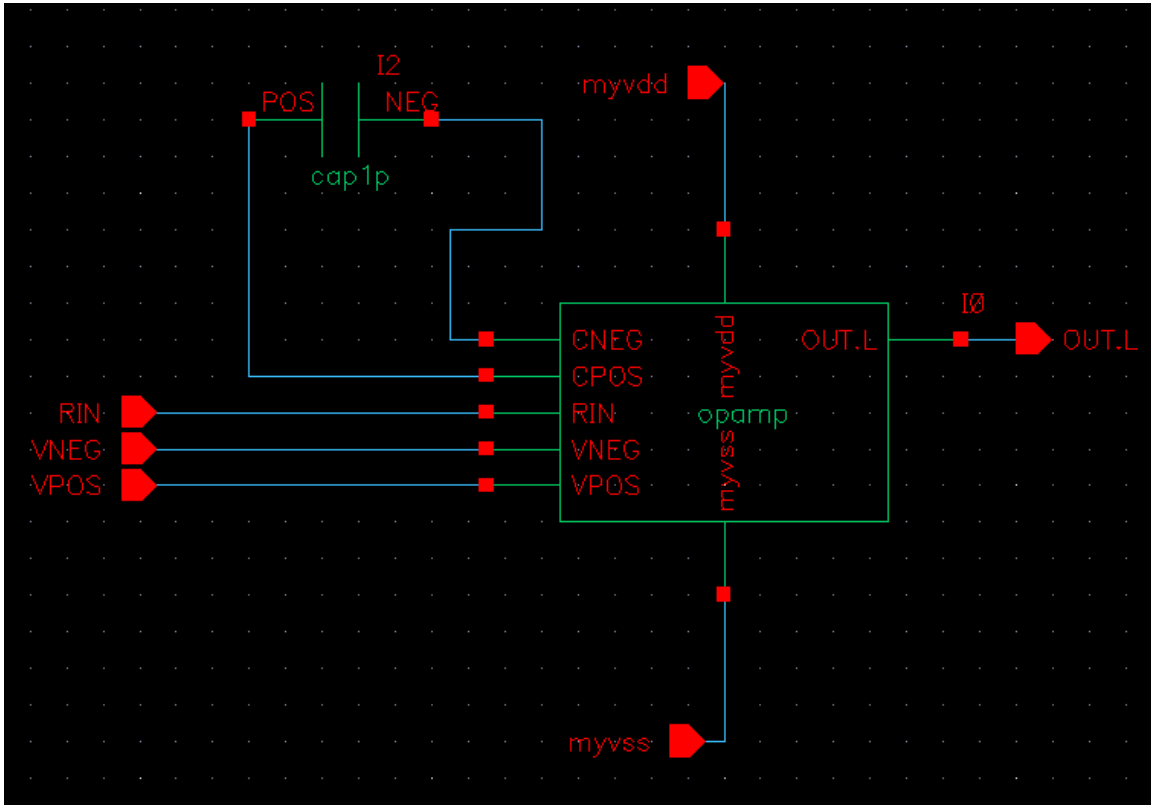


Figure 6: Complete Opamp with Capacitor

Generate a symbol of the complete Opamp circuit as shown below:

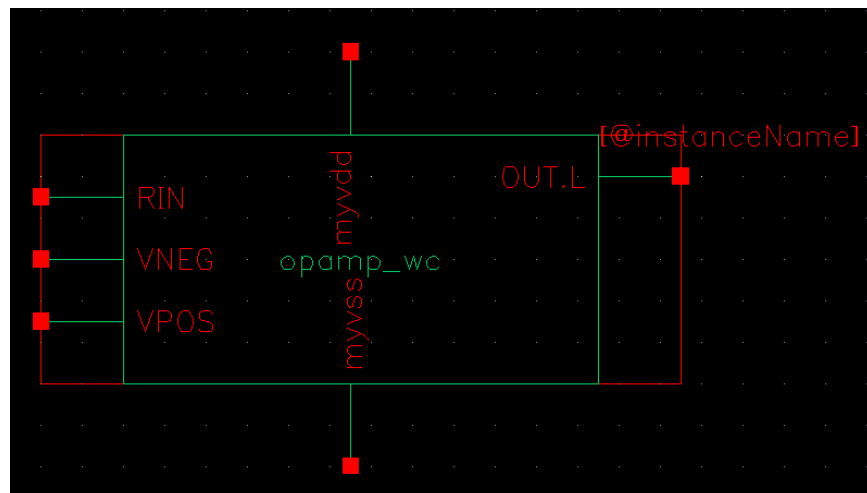


Figure 7: Opamp_wc Symbol

IV. Create Testbench

Use the opamp_wc symbol, vdd, gnd, vss, OUT.L pin, resistor, and 4 vdc sources to create a testbench as shown below:

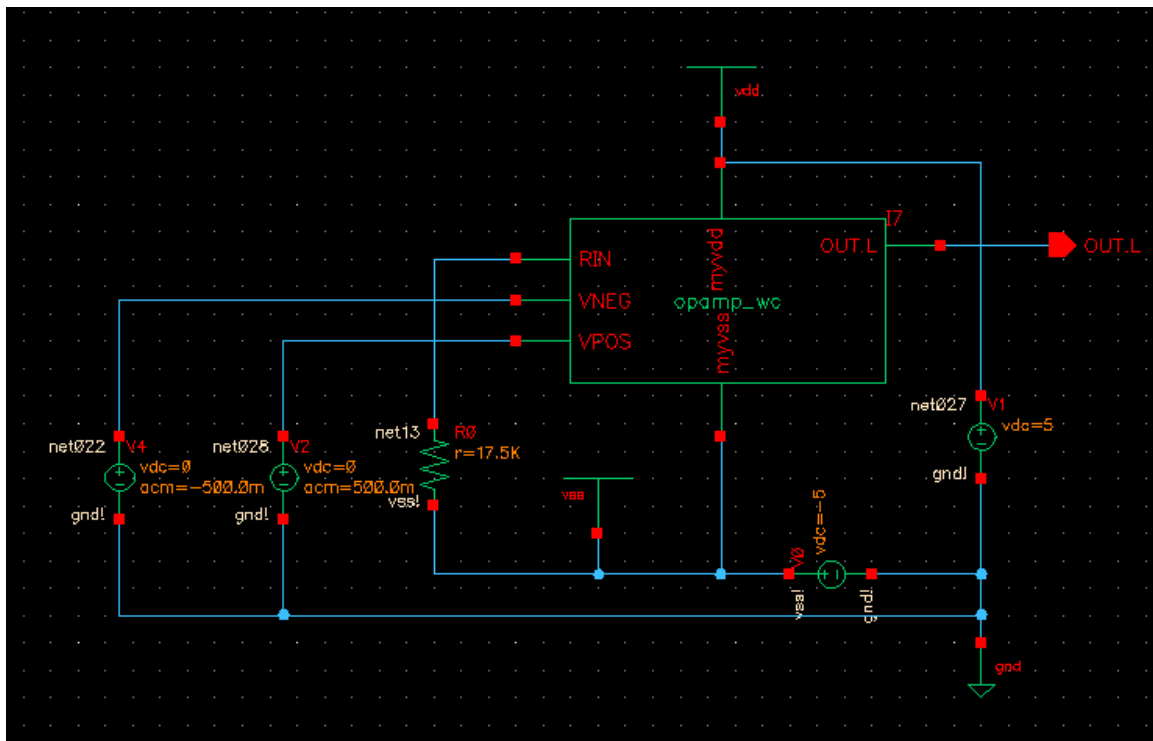


Figure 8: Testbench

Notice, the two DC sources supplied to VPOS and VNEG should have a 0V dc and $\pm 0.5V$ AC magnitude, respectively, while the two DC sources supplied to myvdd and myvss should have $\pm 5V$ DC respectively.

V. Functional Simulation with AFFIRMA

Follow the previous handouts to simulate this testbench. Choose analyses to be AC, starting 1Hz, ending 1G Hz, as shown in this window:

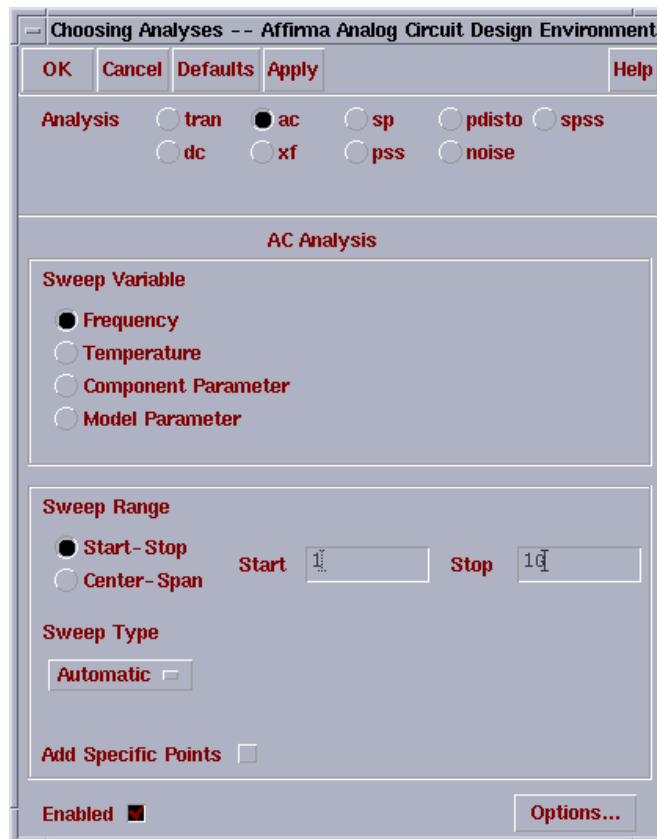


Figure 9: Analyses Setting

Select OUT.L signal to be plotted and run the simulation. You should get a waveform shown on next page:

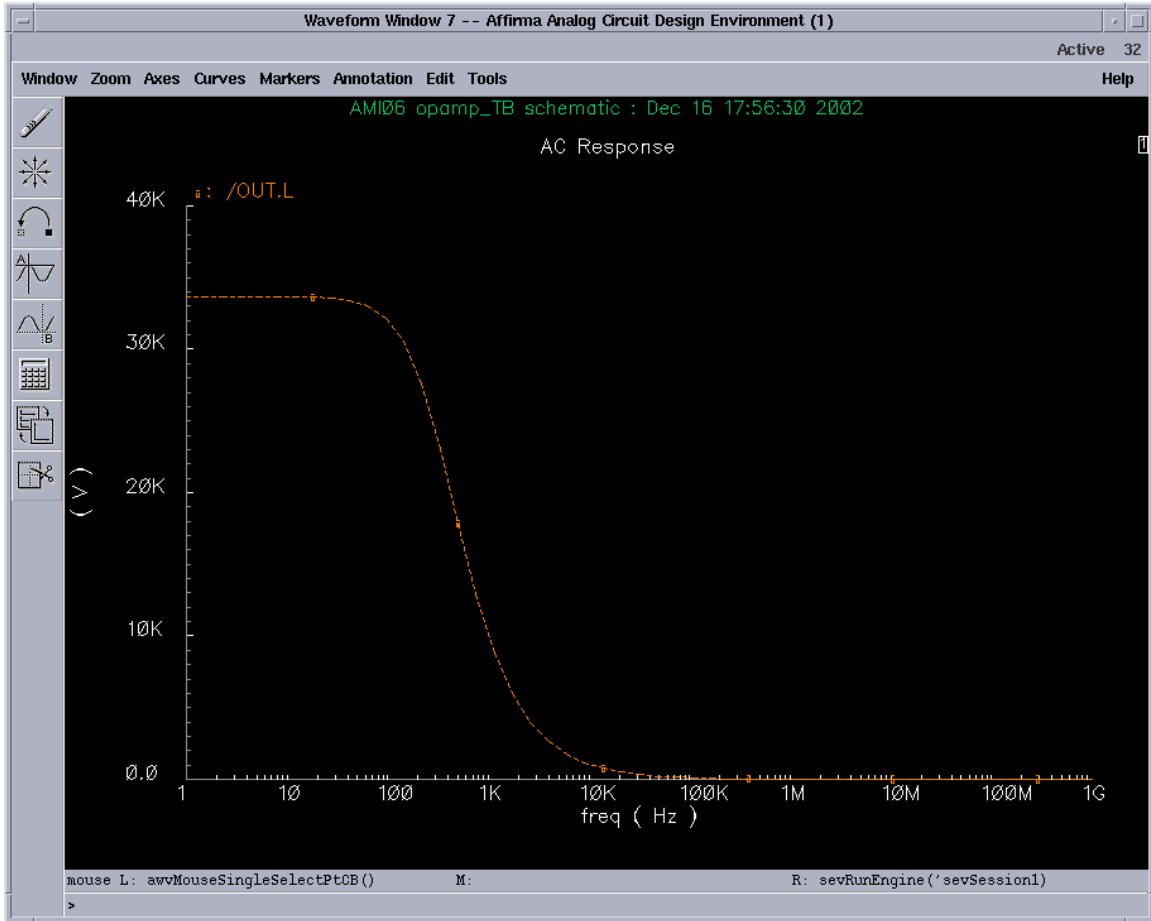


Figure 10: Waveform – AC Magnitude

V. Creating Capacitor Cell Layout

In previous exercises, we have learned how to draw a capacitor layout from scratch. This time, it has been implemented into a menu command.

Follow the similar steps as described in previous exercises. Once you open a blank Virtouso layout view of cap1p, click [menu] WSU -> Layout Capacitor. You will see a prompt window as shown:

The figure shows a dialog box titled "Capacitor Layout". It has a standard Windows-style title bar with a close button. Below the title bar are three buttons: "OK", "Cancel", and "Help". The dialog contains four input fields, each with a label and a value:

- Capacitance (farad): 0.1
- Capacitor Height (um): 0.1
- pin1 name: POS
- pin2 name: NEG

Figure 11: Layout Capacitor Prompt

Fill the form with proper capacitance value (1p) and capacitor height in μm (e.g. 30). Type in the two terminals' names according to your cap1p schematic. Click OK when you complete. A capacitor layout of 1pf should be displayed on your layout window.

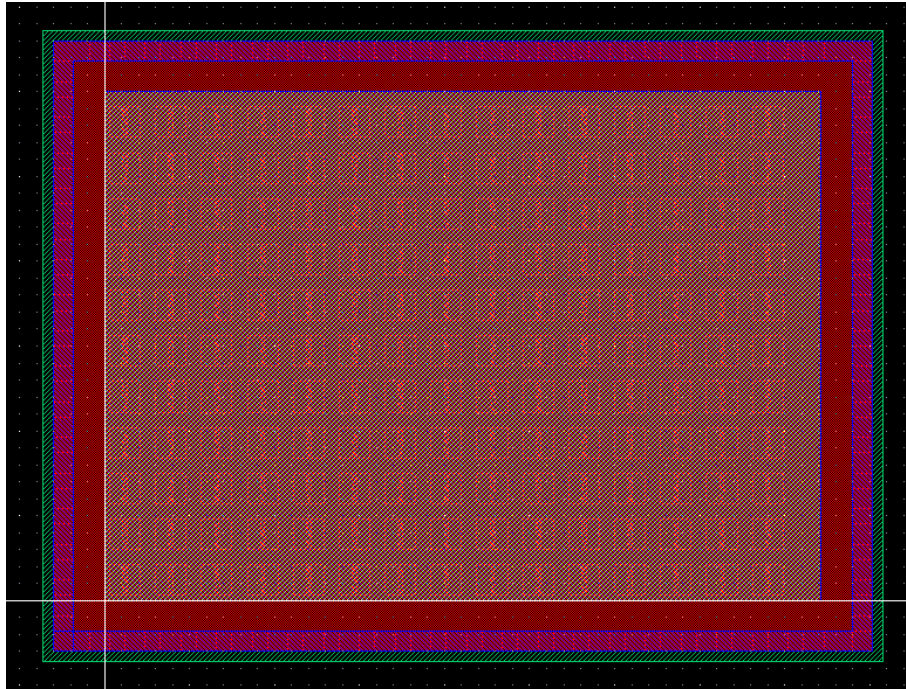


Figure 12: 1pf Capacitor Layout

Extract the layout to exam the capacitance value.

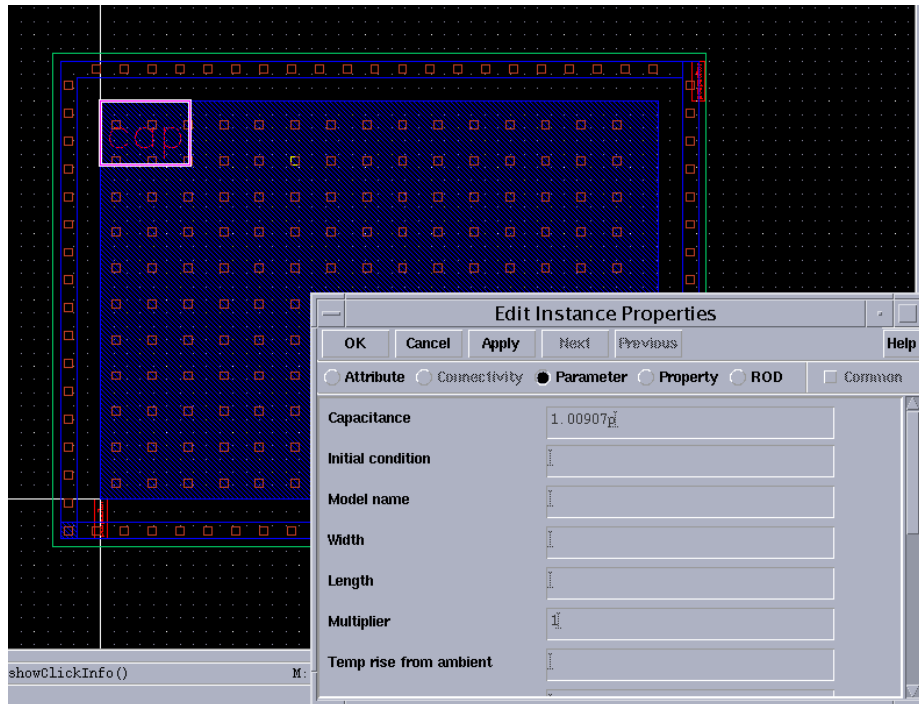


Figure 13: 1pf Capacitor Extracted View

As shown in figure 13, the capacitance value is 1.00907pf, which is sufficiently close to the design value.

VII. Create the Layout of the Opamp without capacitor

Follow the steps in lab 3 to create the layout using Layout XL, with the additional changes and steps given below.

Creating VSS Port

The schematic in Figure 1 does not have a *mygnd* pin, instead a *myvss* pin is required. The “pr” command creates *myvdd* and *mygnd* pins. The first step is to modify the *mygnd* pin to become *myvss* pin as follows:

Select the metal1 *mygnd* pin and modify its property. Change the “terminal name” to *myvss*. Now if you select and move *myvss* pin, you should see the connection between this pin and other components. At this moment, you should see something similar to figure 14 on the next page.

Modify M8 and M9

Notice the two PMOS (M8 and M9) on the right side of the layout are very high (large W). If we continue our layout with such big transistors, we are going to use a large area. This consideration requires us to find a more area-sufficient layout.

As we know, a wide transistor can be replaced by N parallel transistors with same L but W/N width. As a result, M8 is divided into 7 parallel PMOS with L=6.6U, W=124.8U; M9 is divided into 2 parallel PMOS with L=6.6U, W=150U.

The modified schematic with the huge transistors divided and connected in parallel is shown in figure 15.

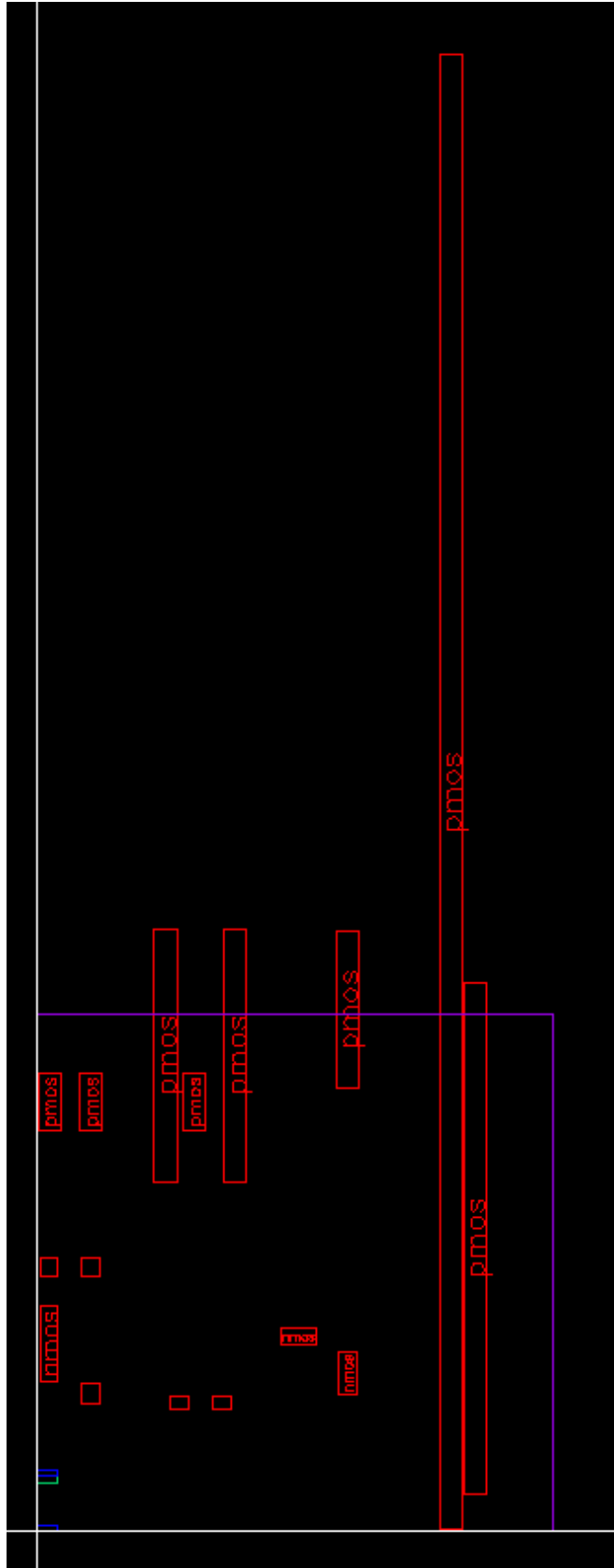


Figure 14: Opamp Layout Instances with Big W

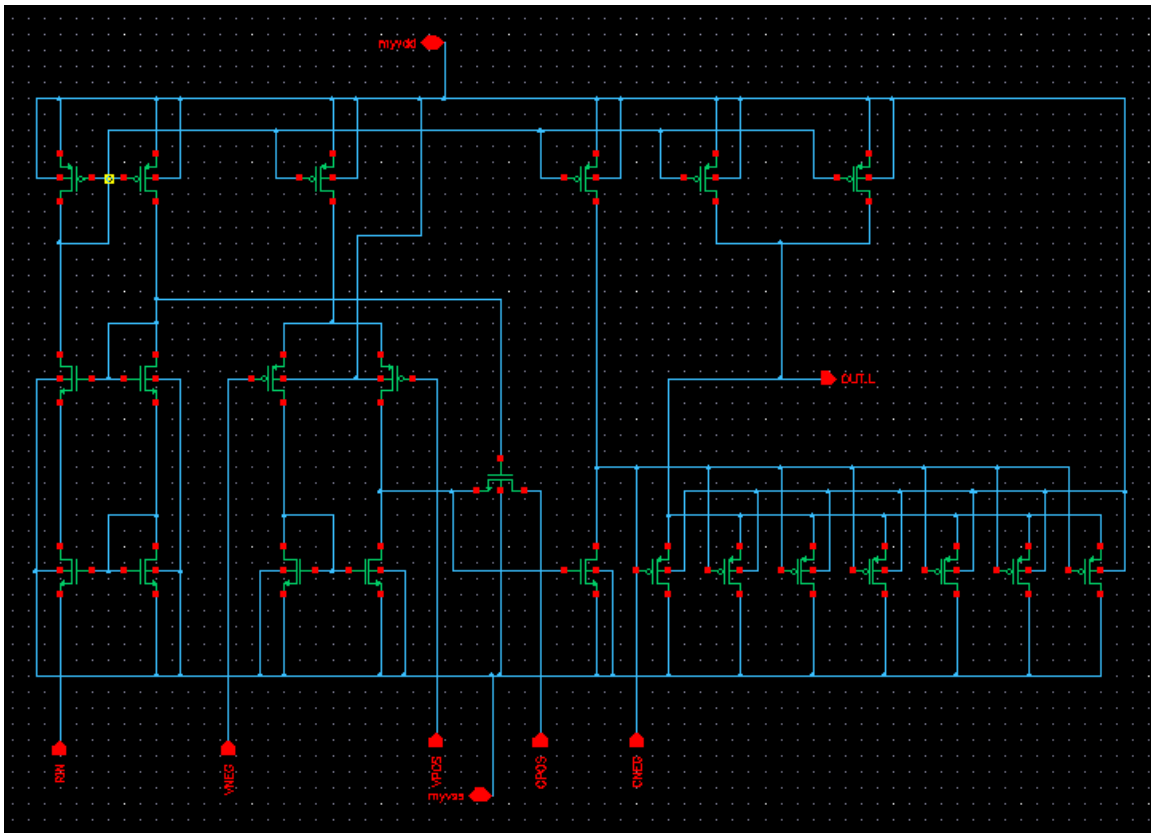


Figure 15: Opamp Schematic with Divided M8 & M9

NOTE: after you modify the schematic you have to do the AFFIRMA simulation of the design again to check if it is giving the same output. You don't need to generate new symbol and testbench since the pins on the new schematic matches the old one.

Transistor Chaining

Now start the Layout XL again and follow the same steps. You should notice now we have a number of smaller transistors instead of the two big ones.

As discussed in earlier handouts, it is important that you do the best (or near-best) transistor chaining to ensure area-efficiency.

A sample layout is shown in figure 16 on the next page. You should be able to distinguish the chained and unchained transistors by examining the number of metall strips between the adjacent poly gates. However, this layout does not represent the best chaining. You should discover the best chaining, as part of the exercise.

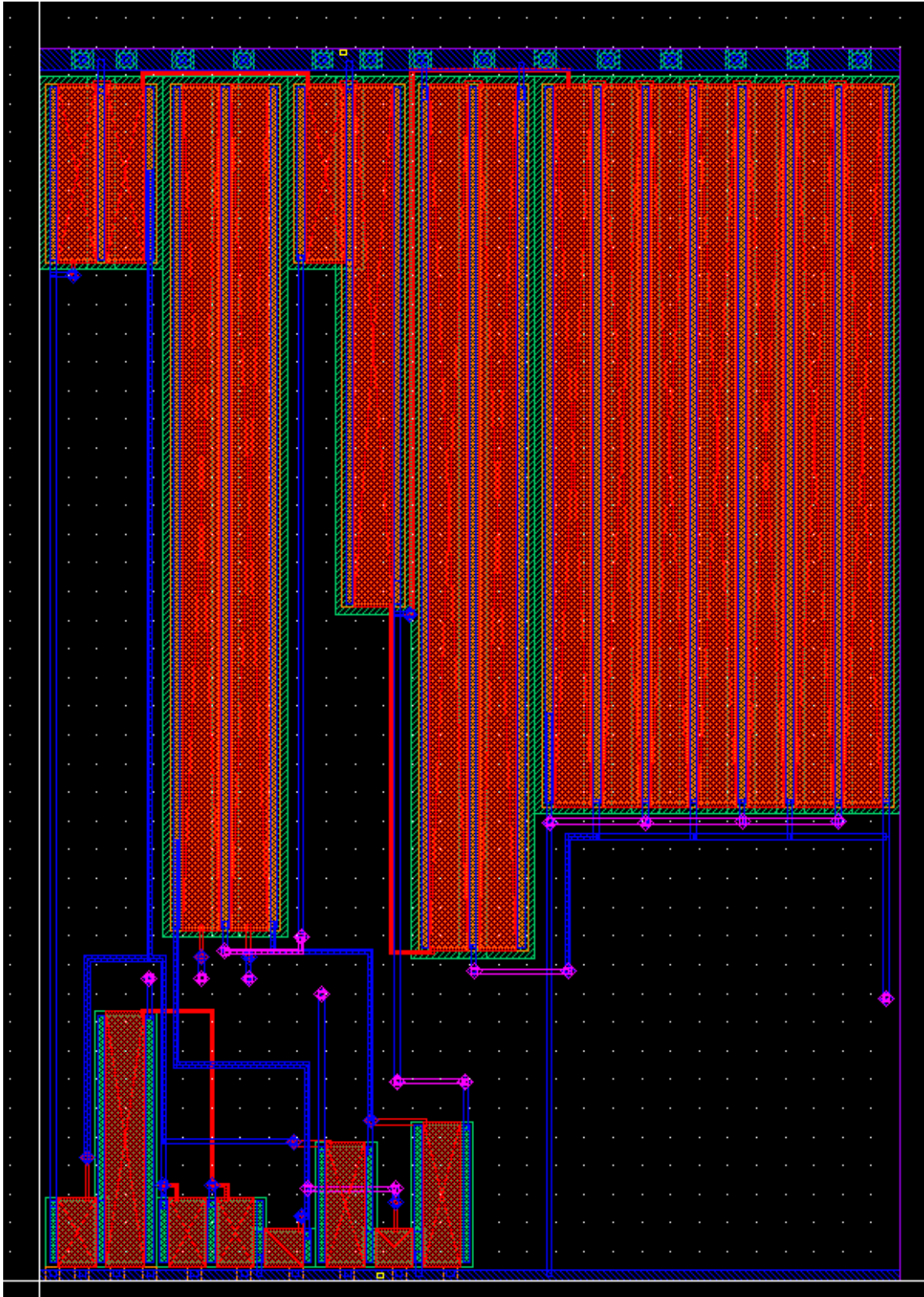


Figure 16: Sample Opamp Layout

Routing

Follow the previous handouts to invoke Custom Router to route the components automatically.

DRC and LVS Check

Follow the previous handouts to check the layout. Correct all errors if exist.

VIII. Create the Layout of the complete Opamp

Now that you have the layout of the capacitor and the opamp without capacitor and resistor you can go ahead with the complete opamp design. We need to follow the steps from lab 5 (hierarchical design) since we have two componenets.

Open the opamp_wc schematic and complete the hierarchical layout of this schematic. You should end up with a layout as shown:

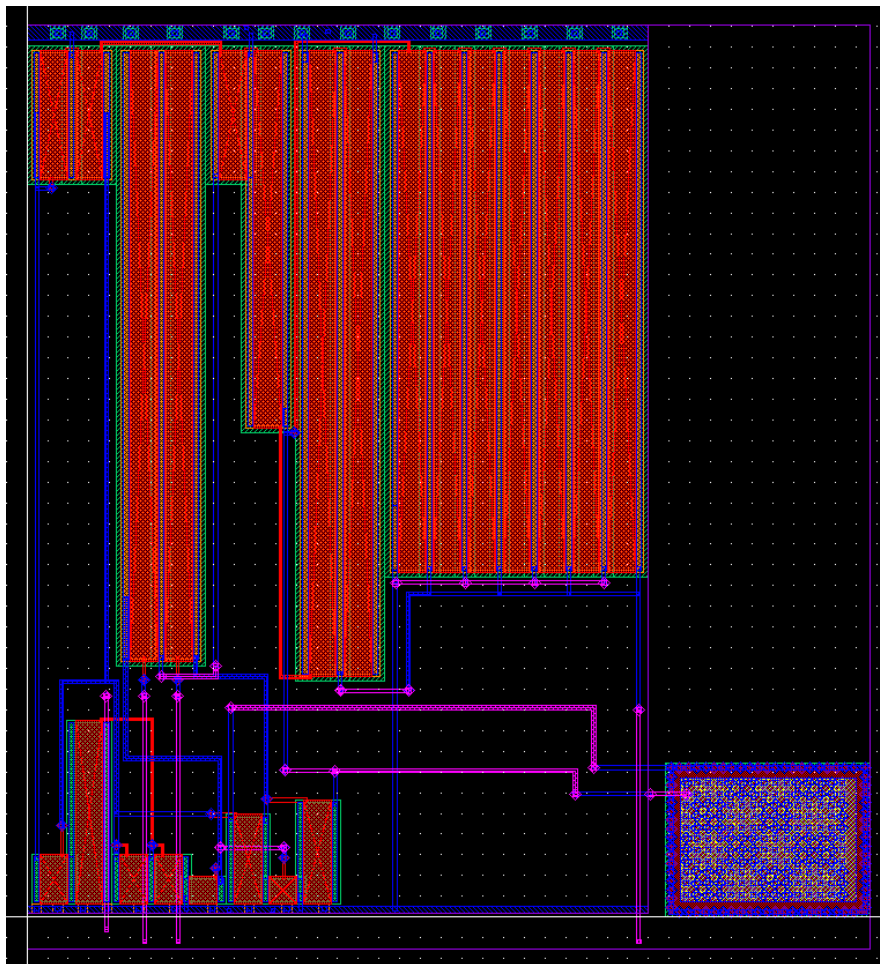


Figure 17: Sample Opamp_wc Layout

Again, you should check DRC and LVS before proceed to post-layout simulation.

IX. POST LAYOUT SIMULATION

Follow the previous handouts for post-layout simulation. You should get a simulation result very close to the pre-layout simulation. This concludes the OPAMP design.